ECSE 425 Project1 - Finite State Machines

Winter 2021

due date: Feb 1, 2021

1 Introduction

The goal of this deliverable is to build and test a finite-state machine to identify the commented characters in C code. Your finite-state machine will have the following ports:

- clk : in std_logic;

  std_logic allows you to have 9 different input/output data types: https://electronics.stackexchange.com/questions/51848/when-to-use-std-logic-over-bit-in-vhdl clk is for designing clocked (aka synchronous or sequential) logic in VHDL. This logic is only triggered by a clock signal. Flip-flops (or registers) work this way.

- reset : in std_logic; This is for initialization and setting to an initial value upon reset.

- input : in std_logic_vector (7 downto 0);

- output : out std_logic

You will feed one ASCII character per clock cycle to your FSM and will get '0' if the input text is not part of a comment and '1' if it is.

1.1 Example

In the following example, the characters where the output should be one is highlighted in green.

```
/*This is the\n
main method*/\n
int main()\n
{\n
                                    //this is a comment\n
                                            return 33;\n

}\n
```

Note that the '\n' represent the new-line character (ASCII 10). The exit sequence for the comment ('\n' or '*/') is considered a comment while the opening sequence ('//' or '/*') is not. Thus, the output should be equal to 1 in the clock cycle after the second character of the opening sequence appears, and the output should be equal to 0 in the clock cycle after the second character of the exit sequence appears. For example:

```
//comment\n code

001111111 1 0000
```

2 Where to start

Three files are provided to you for this assignment:

- fsm.vhd: You will implement your FSM in this file. Do not change the port map (entity).
- fsm_tb.vhd: You will implement a complete testbench for your fsm in this file.
- fsm_tb.tcl: You don't have to edit this file. It is a script to compile and run your testbench.

To compile, open ModelSim and change the directory (File, Change Directory) to the one containing those three files. In the Transcript section (ModelSim console), run the following command:
source fsm_tb.tcl

You would need to change the default resolution to 100 ps using: https://www.doulos.com/knowhow/fpga/clock_circuit_simulation/ If you don't have compilation errors, you should see the waves appear in the Wave section and your test results in the Transcript section.

3 Grading

The following aspects of your deliverable will be evaluated:

- 30% - Correctness of your implementation
- 25% - Completeness of your testbench (does it cover all test cases?)
- 40% - Report quality (does your report clearly explain the thoughts behind your design? does it contain all the contents required? are your test results clearly shown and explained in your report? is your report coherent?)
- 5% - Format of submission files (did you follow all the submission requirements?)

You are expected to write a short report (IEEE format, max 3 pages) summarizing your implementation. The structure/organization of the report is up to you, however it should at least include the following content:

- Explanation for your implementation
- The state diagram of your implementation (i.e. your VHDL implementation should follow the state diagram in your report)
- Discussion of your test results (e.g. can show screenshots of corresponding signal values found in ModelSim, etc.)

Late submission will be deducted 30% every 24 hours from the deadline, for up to 3 days. After 3 days, you will receive a grade of 0. (late by (0,24]hr $\rightarrow -30\%$, (24,48]hr $\rightarrow -60\%$, (48, 72]hr $\rightarrow -90\%$, >72hr $\rightarrow 0\%$)

4 Submission

Hand in, via MyCourses, in a single ZIP file:

- fsm.vhd, fsm_tb.vhd, fsm_tb.tcl
- Report as a PDF file **(failure to submit the report will result in a grade of 0)**

Name your submission folder as "GroupXX_FSM" and report as "GroupXX_FSM_Report".