DATA SHEET

74F10 Triple 3-input NAND gate
74F11 Triple 3-input AND gate

Product specification

1989 Sep 20

IC15 Data Handbook

PHILIPS

Gates

74F10, 74F11

74F10 Triple 3-input NAND gate
74F11 Triple 3-input AND gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0°C$ to $+70°C$	PKG DWG #
14-pin plastic DIP	N74F10N, N74F11N	SOT27-1
14-pin plastic SO	N74F10D, N74F11D	SOT108-1

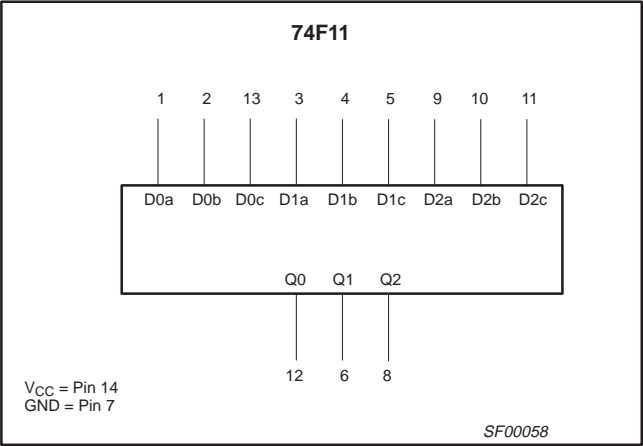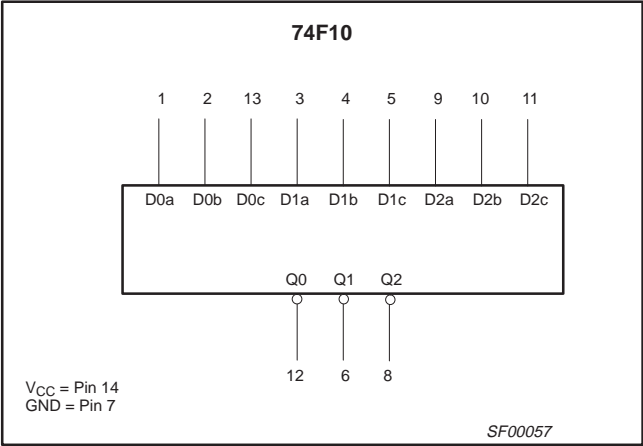## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}n$	Data output (74F10)	50/33	1.0mA/20mA
Qn	Data output (74F11)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.
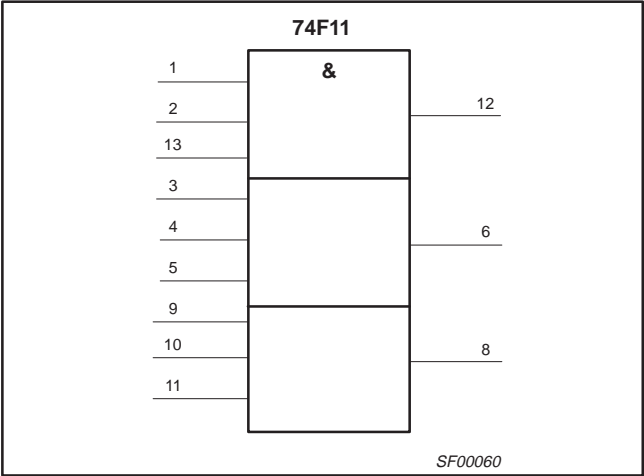
PIN CONFIGURATIONS

74F10

D0a	1	14 V_{CC}
D0b	2	13 D0c
D1a	3	12 $\overline{Q}0$
D1b	4	11 D2c
D1c	5	10 D2b
$\overline{Q}1$	6	9 D2a
GND	7	8 $\overline{Q}2$

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74F11

D0a	1	14 V_{CC}
D0b	2	13 D0c
D1a	3	12 Q0
D1b	4	11 D2c
D1c	5	10 D2b
Q1	6	9 D2a
GND	7	8 Q2

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LOGIC SYMBOLS

74F10

1 2 13 3 4 5 9 10 11

D0a D0b D0c D1a D1b D1c D2a D2b D2c

Q0 Q1 Q2

12 6 8

V_{CC} = Pin 14
GND = Pin 7

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74F11

1 2 13 3 4 5 9 10 11

D0a D0b D0c D1a D1b D1c D2a D2b D2c

Q0 Q1 Q2

12 6 8

V_{CC} = Pin 14
GND = Pin 7

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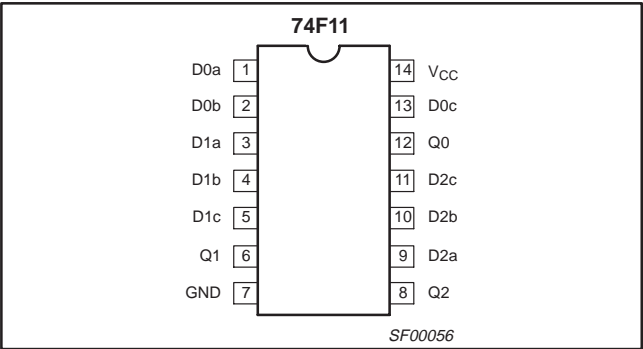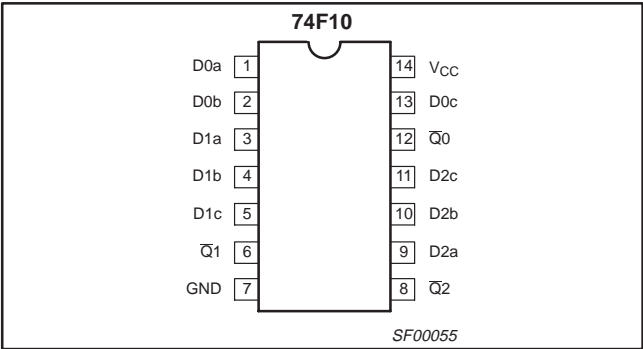
Gates

74F10, 74F11

IEC/IEEE SYMBOLS

74F10

1	&
2	
13	12
3	
4	6
5	
9	
10	8
11	

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74F11

1	&
2	12
13	
3	
4	6
5	
9	
10	8
11	

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LOGIC DIAGRAMS

74F10

D0a — 1
D0b — 2 — 12 — $\overline{Q}0$
D0c — 13

D1a — 3
D1b — 4 — 6 — $\overline{Q}1$
D1c — 5

D2a — 9
D2b — 10 — 8 — $\overline{Q}2$
D2c — 11

V_{CC} = Pin 14
GND = Pin 7

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74F11

D0a — 1
D0b — 2 — 12 — Q0
D0c — 13

D1a — 3
D1b — 4 — 6 — Q1
D1c — 5

D2a — 9
D2b — 10 — 8 — Q2
D2c — 11

V_{CC} = Pin 14
GND = Pin 7

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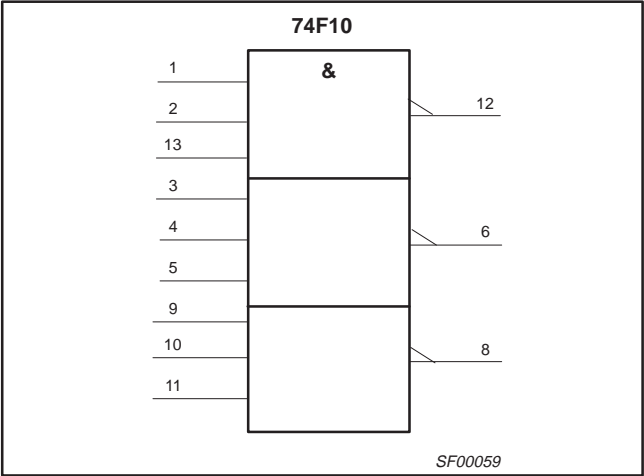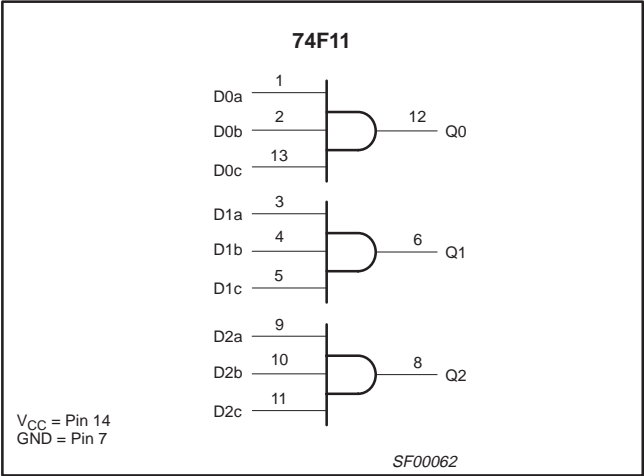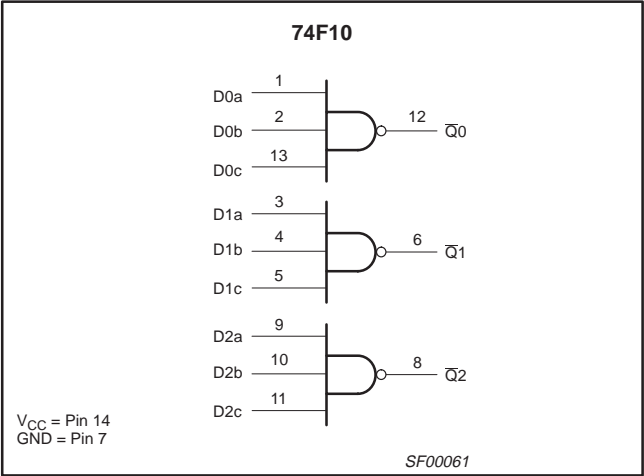
FUNCTION TABLE

INPUTS			OUTPUTS	
			74F10	74F11
Dna	Dnb	Dnc	$\overline{Q}n$	Qn
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

NOTES:
1. H = High voltage level
2. L = Low voltage level

Gates

74F10, 74F11

ABSOLUTE MAXIMUM RATINGS
(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS
(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	74F10	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	2.1	mA
			I_{CCL}		V_{IN} = 4.5V		6.0	7.7	
		74F11	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		4.7	6.2	mA
			I_{CCL}		V_{IN} = GND		7.2	9.7	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
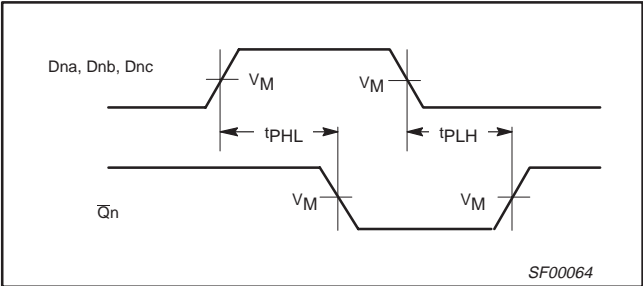
Gates

AC ELECTRICAL CHARACTERISTICS

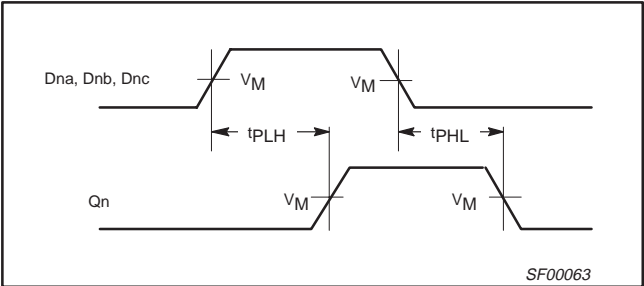| SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$V_{CC} = +5.0V$ $T_{amb} = +25°C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0°C$ to $+70°C$ $C_L = 50pF, R_L = 500\Omega$		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to $\overline{Q}n$	74F10	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F11	Waveform 2	3.0 2.5	4.2 4.1	5.6 5.5	3.0 2.5	6.6 6.5	ns

AC WAVEFORMS

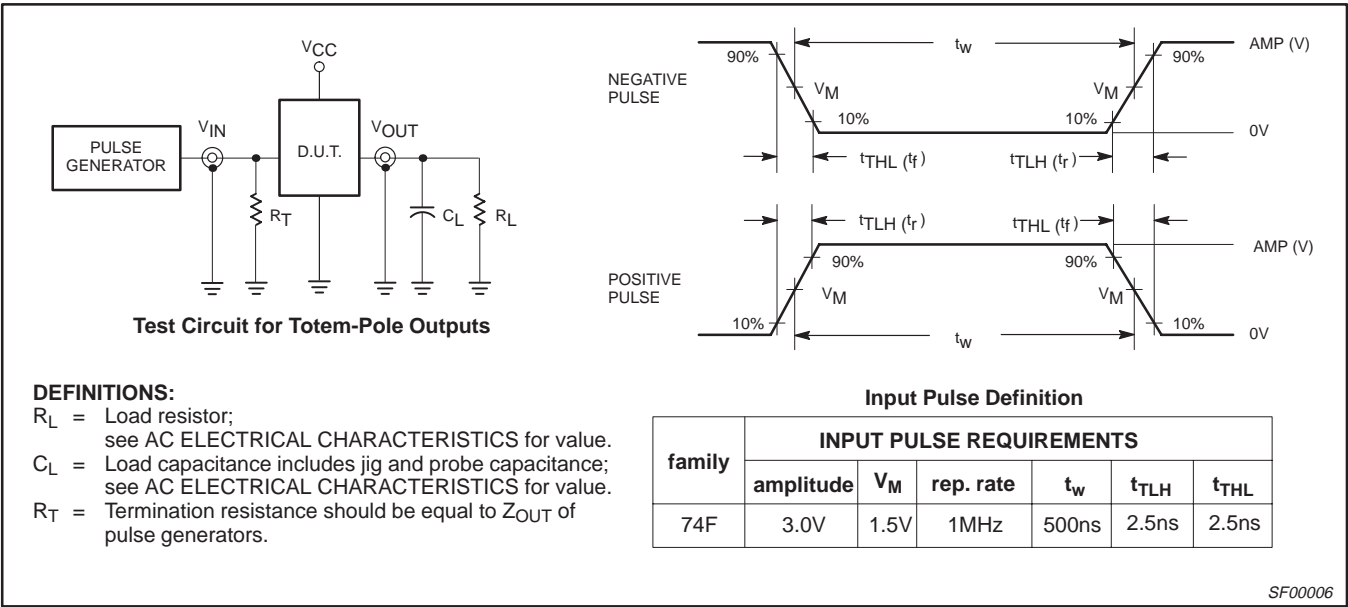For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay for Inverting Outputs (74F10)

Waveform 2. Propagation Delay for Non-Inverting Outputs (74F11)

TEST CIRCUIT AND WAVEFORM

Test Circuit for Totem-Pole Outputs

DEFINITIONS:
R_L = Load resistor;
   see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance;
   see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of
   pulse generators.

Input Pulse Definition

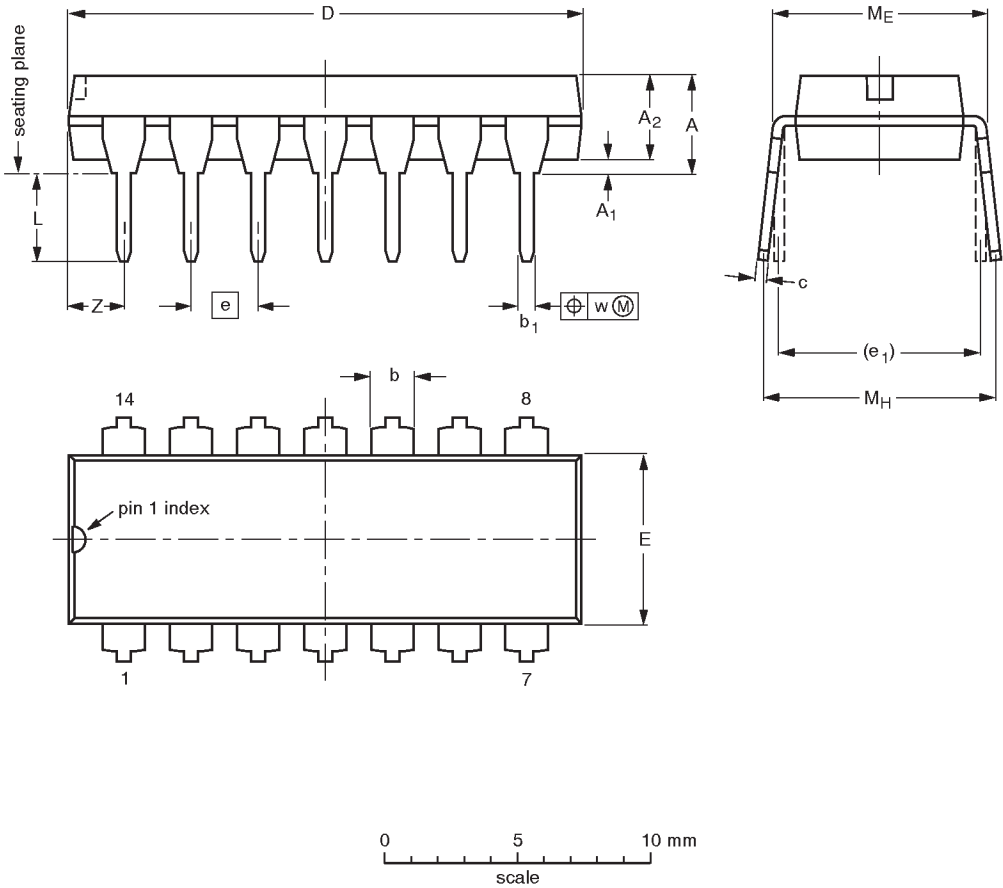| family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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Gates

74F10, 74F11

DIP14: plastic dual in-line package; 14 leads (300 mil)   SOT27-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$ min.	A$_2$ max.	b	b$_1$	c	D [1]	E [1]	e	e$_1$	L	M$_E$	M$_H$	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

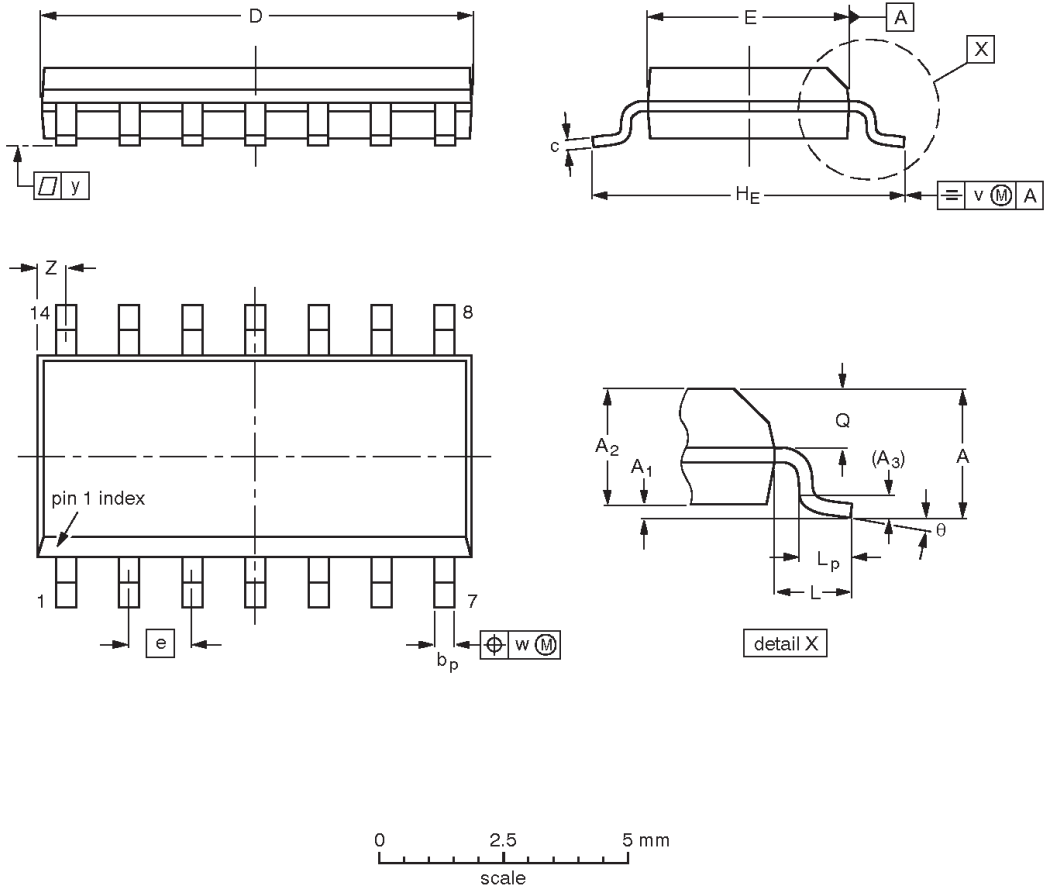1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Gates

74F10, 74F11

SO14:   plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1


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0        2.5        5 mm
|_._._._|_._._._|
        scale
```

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D(1)	E(1)	e	HE	L	Lp	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1]   Please consult the most recently issued datasheet before initiating or completing a design.

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