1.

Simulated timing (ns)

```
============================================================

Success!
The test result is .....PASS :)

============================================================

$finish called from file "RISCV_tb.v", line 159.
$finish at simulation time                25500
           V C S   S i m u l a t i o n   R e p o r t
Time: 255000 ps
CPU Time:      0.750 seconds;       Data structure size:   0.0Mb
Wed Apr 19 23:30:30 2023
CPU time: .623 seconds to compile + .615 seconds to elab + .502 seconds to link
+ .792 seconds in simulation
[b09036@cad33 verilog]$
```

2. Area (um^2)

```
Number of ports:                         1443
Number of nets:                          6356
Number of cells:                         4952
Number of combinational cells:           3871
Number of sequential cells:              1056
Number of macros/black boxes:               0
Number of buf/inv:                        717
Number of references:                      40

Combinational area:              39578.275877
Buf/Inv area:                     5957.874035
Noncombinational area:           26917.369667
Macro/Black Box area:                0.000000
Net Interconnect area:          690016.837311

Total cell area:                 66495.645544
Total area:                     756512.482855
1
design_vision> read_ddc CHIP_syn.ddc
```

report_area

3. Cost (A*T)

66495.65*0.792 = 52664.5548 um*s

4. ScreenShot Inferred memory devices in process

```
Inferred memory devices in process
        in routine REG_FILE_BITS5_WIDTH32 line 166 in file
                '/home/raid7_2/userb09/b09036/DSD_2023/DSD_HW2/verilog/CHIP.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|      reg_r_reg      | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
Statistics for MUX OPs
```

```
Inferred memory devices in process
        in routine CHIP line 92 in file
                '/home/raid7_2/userb09/b09036/DSD_2023/DSD_HW2/verilog/CHIP.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|      PC_r_reg       | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```