EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 3
Fall 2020 (Oct 6, 2020)

Instructions: There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam, on separate sheets of white paper, or on a tablet pc. When finished, scan or image and upload as a .pdf file on Canvas. Exams are due by 1:00 p.m.

Please show enough of your work on the problems so that the process you followed to obtain a solution is apparent. This will help during grading if partial credit is justified and help verify that the correct solution is obtained for the right reason. Credit will not be given for an answer that may be correct if the solution process is not shown.

Due to the online nature of this exam, students will be expected to adhere to the honor system and acknowledge adherence with a signature given below. This is an open-book open-notes exam and students can seek basic information using online resources but with the following absolute restrictions. Prior to the Canvas upload due time, no questions or problems should be posted on any electronic forum, no discussions are permitted relating to this exam with anyone else besides the course instructor, and no solutions obtained from any source other than by the student taking the exam are permitted. The course instructor will attempt to respond to questions by email that are sent between 11:00 a.m. and 1:00 p.m.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/V^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$. Correspondingly, assume all npn BJT transistors have model parameters $J_S= 10^{-14}A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S= 10^{-14}A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. If reference to a diode is made, assume the process parameter $J_S=10^{-17}A/\mu^2$, $V_{G0}=1.17V$, and m=2.3. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E- 5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

Honor System Adherence Signature:

I certify that I have adhered to the honor system policy described in the second paragraph above _____

Short Questions

1. (2pts) Which of the basic BJT amplifiers is characterized by a very high input impedance and a noninverting voltage gain of approximately 1 V/V?

2. (2pts) Why is the Q-point of a common-source amplifier often placed near the middle of the load line?

3. (2pts) The two-port small-signal model of an amplifier is often characterized by the amplifier parameters $\{R_{IN}, R_{OUT}, A_{VR}, A_V\}$. If the amplifier is unilateral, one of these parameters is 0. Which one is it?

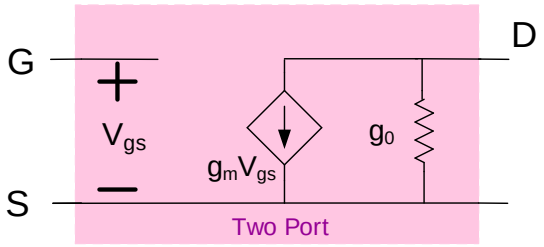
4. (2pts) A common centroid layout of the two transistors in a basic current mirror is often used to improve accuracy of the current mirror gain. What undesirable effect does the common centroid layout overcome?

5. (2pts) Why are current sources often used when biasing amplifier circuits instead of voltage sources, capacitors, and resistors?

6. (2pts) What model parameter in a JFET is analogous to the threshold voltage of a MOSFET?

7. (2pts) The dependent sources discussed in EE 201 are actually two-ports. Give the two-port model of the current-dependent current source (as defined in EE 201) in terms of either the Y-parameters $\{y_{11}, y_{12}, y_{21}, y_{22}\}$ or the amplifier parameters $\{R_{IN}, R_{OUT}, A_{VR}, A_V\}$.

8. (2pts) A two-port small signal model of an n-channel transistor is shown below where the small-signal parameters g_m and g_o are both positive.

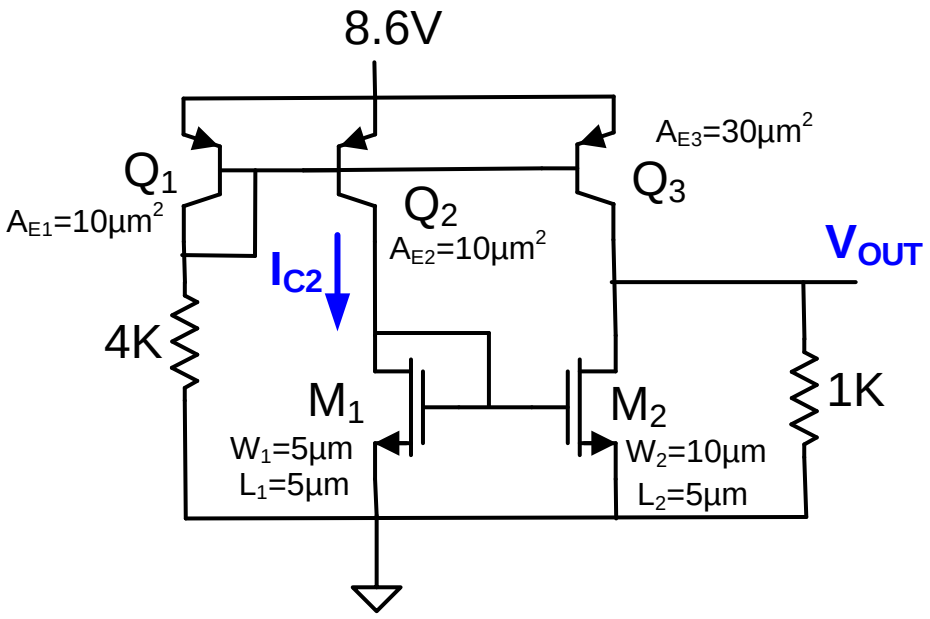


True of False : The two-port small signal model of a p-channel transistor is the same with one exception, the direction of the transconductance dependent current source is reversed.

9. (2pts) In the textbook used in this course, the high and low Boolean voltage levels for an inverter are defined to be the voltages where the slope of the inverter transfer characteristics are -1. Why is this not a good definition for the high and low logic levels for an inverter?

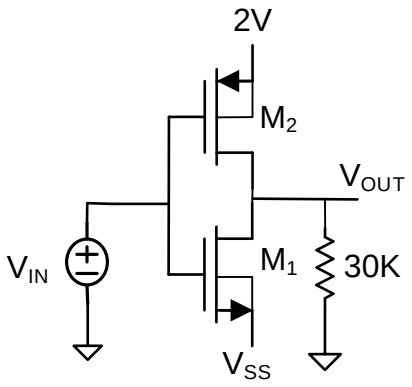
10. (2 pts) The small-signal model for a MOS transistor can be developed for operation in cutoff, saturation, or triode. What is the major reason we developed the small-signal model for the MOS transistor when it is operating in the saturation region?

Problem 1 (16 Pts.) Consider the following circuit. Assume the β of the BJT transistors are very large. Determine V_{OUT} and I_{C2}.



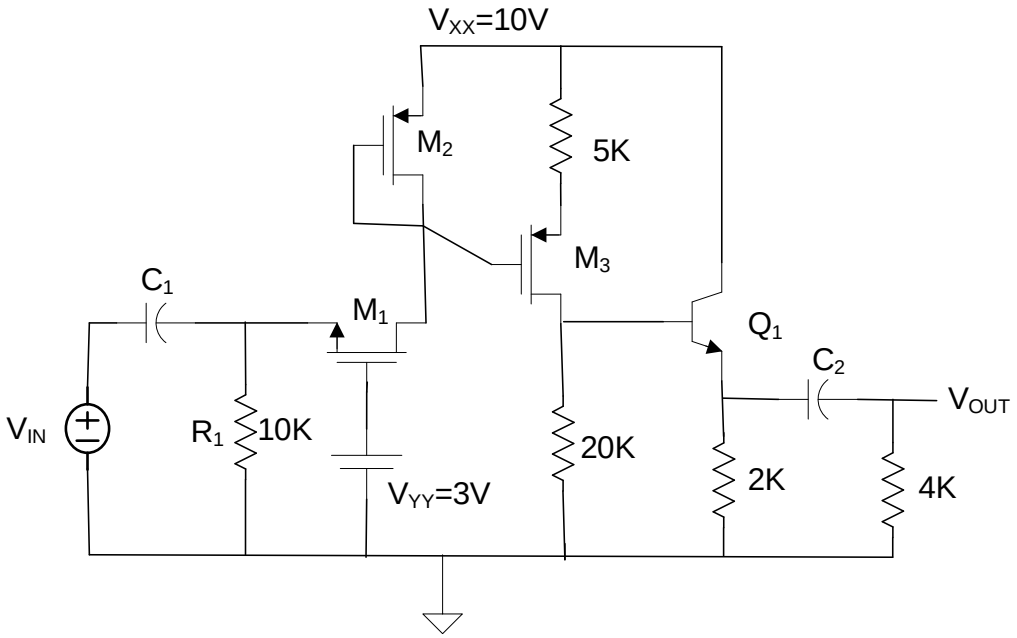
Problem 2 (16 Pts.) Consider the following amplifier where the dimension of M_1 and M_2 are W_1=10µm, W_2=30µm, L_1=1µm and L_2=1µm.. Assume that the dc voltage V_{SS} is adjusted so that the quiescent output voltage is 0V. Assume that the parasitic capacitances on the drain nodes of M_1 and M_2 are 10fF and 20fF respectively and that all other parasitic capacitances are negligible.

a) Draw the small-signal equivalent circuit that can be used to characterize the high frequency operation of the amplifier
b) Determine the small-signal voltage gain in terms of the small-signal model parameters of the devices and any other relevant components that can be used to characterize the high frequency performance of this amplifier
c) (extra credit 8 pts) numerically determine the 3dB bandwidth of this amplifier.



Problem 3 (16 Pts.) Consider the following circuit. Assume the device sizes of all transistors have been selected so that the MOS transistors are operating in the saturation region and the BJT is operating in the forward active region. Assume also that the capacitors C_1 and C_2 are large.

a) Draw the small signal equivalent circuit
b) Determine the small-signal voltage gain in terms of the small-signal model parameters

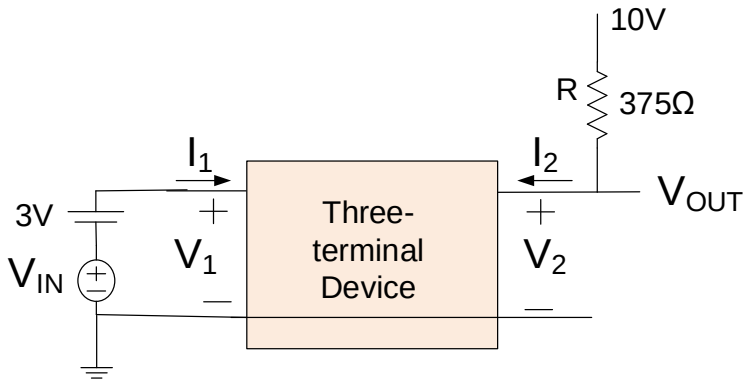


Problem 4 (16 Pts.) Design a voltage amplifier that has a gain of $A_V = 8$ that has a 20KΩ load resistor with one terminal connected to ground using bipolar junction transistors, a single 10V DC power supply, and any number of resistors and capacitors. Clearly indicate the size of the transistors and the values for all passive components. Include any biasing that is required for your amplifier.

Problem 5 (16 Pts) Consider the following circuit where the nonlinear device is characterized by the model given below.

$$I_1 = 10^{-4}\left(V_1 - 1\right)^2$$

$$I_2 = 10^{-3}\left(V_1 - 3\right)^3 V_2^2$$



a) Determine the quiescent values of I_1 and I_2
b) Develop a small-signal y-parameter model for the nonlinear 2-port at the Q-point determined in part a)
c) Determine the small signal voltage gain in terms of the small-signal model parameters and any other necessary circuit elements
d) Numerically determine the small-signal voltage gain

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON