EE 330

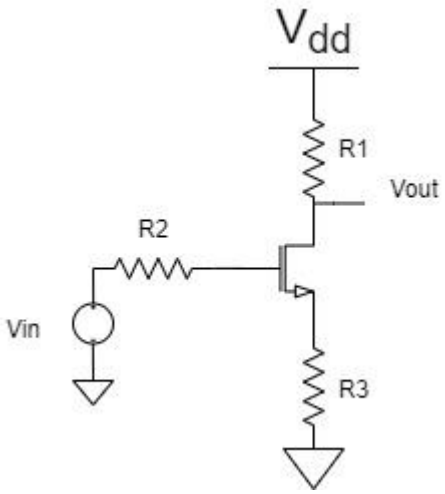
Homework 7

Fall 2020

Due Friday October 2

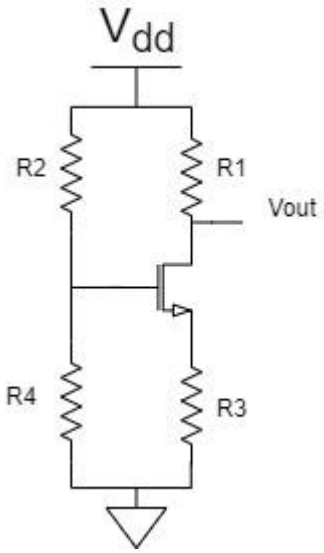
Problem 1

Find Vout for $Vdd = 10V, V_{in} = 3V, R1 = 2k\Omega, R2 = 100k\Omega, R3 = 2k\Omega$ in the AMI 06 process for a minimum sized NMOS.



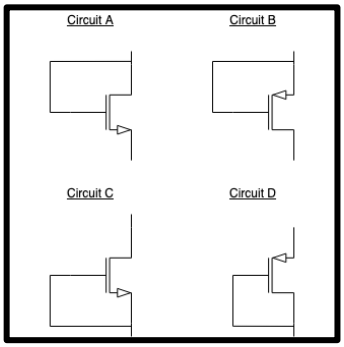
Problem 2

Find Vout for $Vdd = 10V,\ R1 = 5k\Omega, R2 = 10k\Omega, R4 = 90k\Omega, R3 = 2k\Omega$ in the AMI 06 process for a minimum sized NMOS.



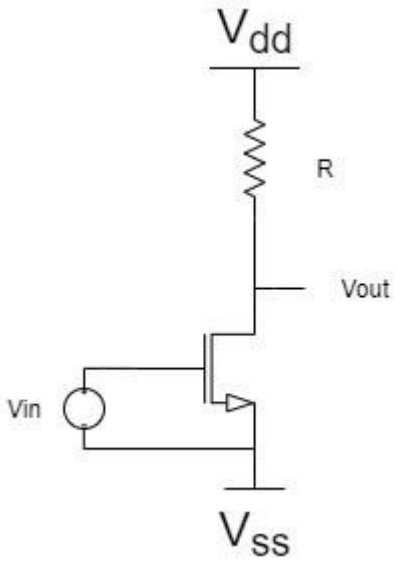
Problem 4

For each circuit below, identify the device's drain, gate, and source terminals (it is sufficient to write "D", "G", or "S" next to each terminal). Then, for each circuit, determine whether the NMOS or PMOS device is in the cutoff, triode, or saturation mode of operation. You may assume that the drain-source voltage of all NMOS devices is greater than the threshold voltage ($V_{DS} \geq V_{Tn}$) and that the source-drain voltage of all PMOS devices is greater than the absolute value of the threshold voltage ($V_{SD} \geq |V_{Tp}|$). Support your statements.



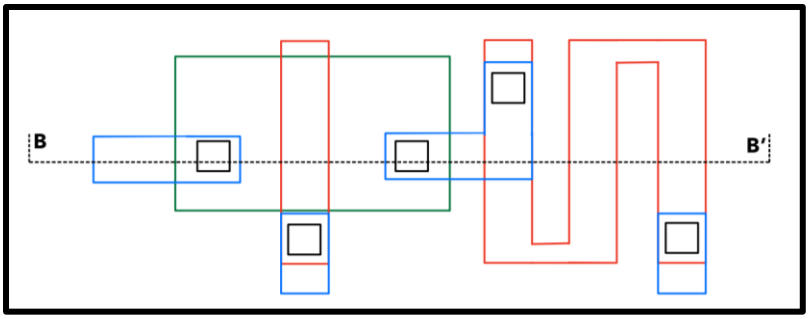
Problem 4

Assume the following configuration with V_{ss}=0V, V_{dd}=10V, Vin=1V and R=5000Ω. Find Vout given this is the AMI 06 process and using the extended square law model (with lamda). Assume the Early Voltage is 100V and the effect from the bulk leads to $\gamma = 0.4V^{\frac{1}{2}}$ and $\varphi = 0.6V$ (note that the bulk is connected to Vss)



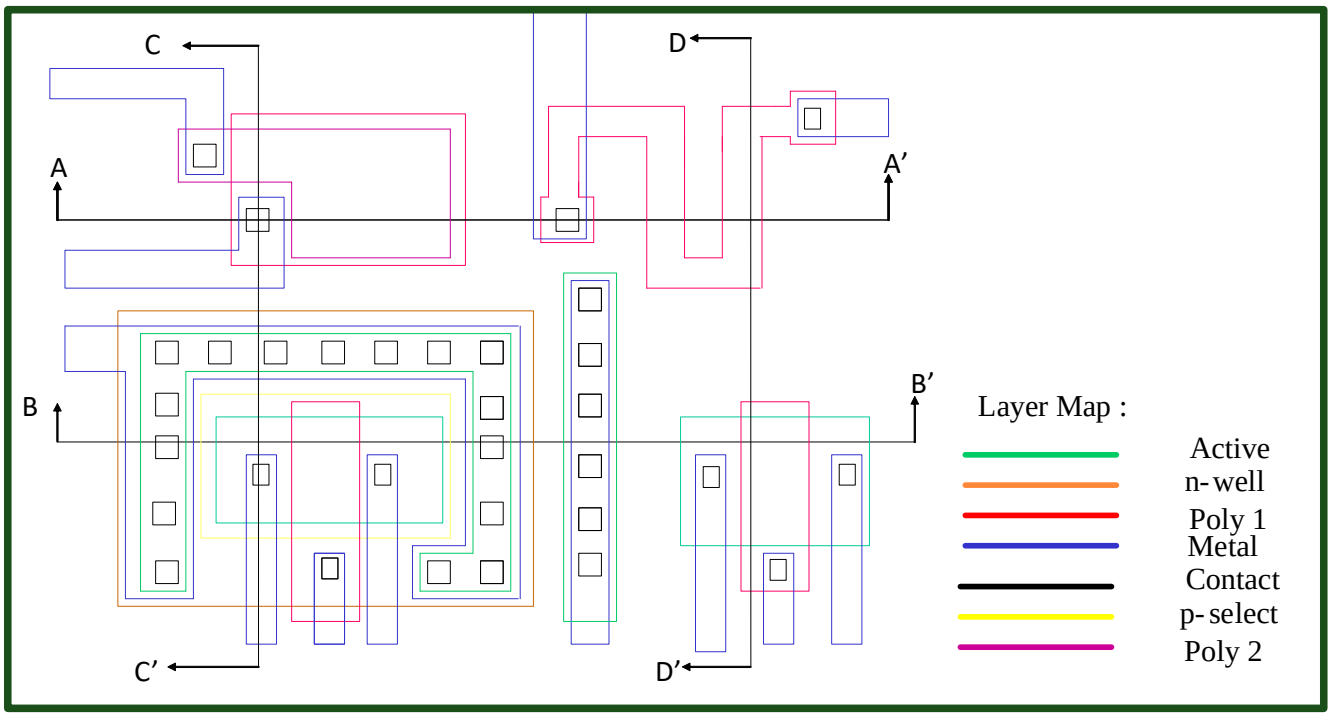
Problem 5

Two devices are shown below. Identify the devices.



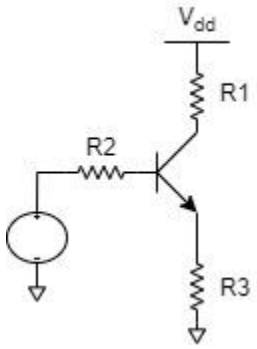
Problem 6

Sketch a cross-sectional view along the BB' cross-section for the CMOS layout shown below. Assume a basic CMOS process in which the n-select mask is generated from the compliment of the p-select mask.



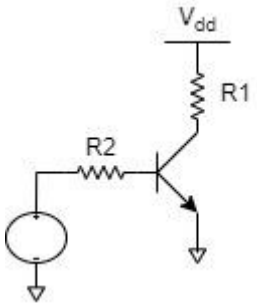
Problem 7

Find the voltage at the collector if $\beta = 100$, $V_{dd} = 5V$, $V_{in} = 2V$, $R_1 = 1k\Omega$, $R_2 = 100k\Omega$ and $R_3 = 1k\Omega$. Use the Further Sumplified model with VBE=0.7V



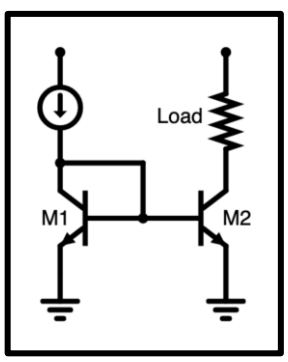
Problem 8

Find the voltage at the collector of a npn BJT with an area of $100\mu m^2$ if $\beta = 100, V_{dd} = 5V, V_{in} = 2V, R_1 = 1k\Omega, R_2 = 100k\Omega$ at 273 Kelvin. Use the simple DC model. ($J_{SX} = 20mA/\mu m^2, V_{GO} = 1.17V, m = 2.3$)



Problem 9

In the circuit below, assume that M_1 and M_2 are both in the forward-active mode of operation. Knowing that the junction area of M_1 is A_1 and the junction area of M_2 is A_2, and also that the current source has a value of I_{IN}, find the current flowing through the load resistor and M_2. Note that your final answer should be in terms of *only* A_1, A_2, and I_{IN}.



Problem 10 and 11

Create a positive edge triggered master-slave D flip flop in ModelSim. Provide a test bench to verify your flip flop. Include screenshots of your Verilog code and simulation waveforms.

Problem 12

Use Modelsim to create a one-bit Half Adder. For the inputs use two one-bit inputs. For the outputs, use a one-bit output and a carry out bit. Create a test bench for the code and show the results and waveforms.