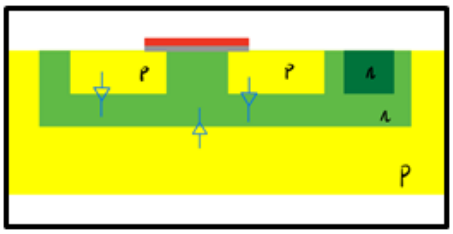
EE 330

Homework 4 Solutions

Fall 2020

Solution 1

Parasitic diodes in PMOS and NMOS devices are a very big deal, both because they can deteriorate the MOSFET's performance and because they can be used to create more complicated devices (which you'll learn about in lecture later). Below is a PMOS cross section with parasitic diodes drawn on it:



One negative effect that these diodes can have is that, even when the voltage across the diodes is less than 0.6V, current can flow from the anode of the diodes to the cathode. In precision integrated circuits, this leakage current may be significant and prove to be a design engineering challenge.

Solution 2

From online sources resistivity of copper is $\rho = 1.68 * 10^{-8}\ \Omega m$, $A = 22nm * 32nm = 704nm^2$

and $R = \frac{\rho L}{A} = 1.68 * 10^{-8} * \frac{800\mu m}{704nm^2} = 1.68 * 10^{-8} * \frac{800*10^{-6}}{704*10^{-18}} = 19090\Omega$

Solution 3

Area will be $L_x * \left(d_1 + d_1 + \frac{d_1}{2} + \frac{d_1}{2}\right) = L_x * 3d_1$

Solution 4

For copper:

$$R = \frac{\rho L}{A} = \frac{\rho}{h}\frac{L}{w} = R_{\square} * \frac{L}{w} \Rightarrow R_{\square} = \frac{20}{200} = 0.1\ \Omega/\square$$

$$R_{\square} = \frac{\rho}{h} \Rightarrow h = \frac{\rho}{R_{\square}} = \frac{1.68 * 10^{-8}}{0.1} = 168nm$$

For silver:

$$R = \frac{\rho L}{A} \Rightarrow 20 = \frac{1.59 * 10^{-8} * L}{1.5\mu m * 168nm} \Rightarrow L = 317\mu m$$

Solution 5

Implantation is a semiconductor doping process in which positive or negative ions are accelerated and forced to collide into a silicon region. This results in the ions becoming embedded in the silicon, causing the region to have a higher concentration of either positive or negative charges. The major advantage of implantation over diffusion is that implantation can be used to create consistent doping vertically through a silicon region, while diffusion always has a concentration gradient related to it.

Solution 6

A common problem that occurs during the implantation process is that, as the accelerated ions move through the silicon's lattice, they sometimes knock particles out of alignment. This leads to imperfections in the silicon's lattice structure, impeding current flow. At the small scale, this can lead to deviations in a semiconductor's threshold voltage or mobility constants, and at the large scale can lead to faulty devices.

Solution 7

A common problem that occurs with wet etching is that the etchant, once below the photoresist layer, frequently etches away at the material located below the photoresist, forming a "bowl" in the material being etched rather than a perfect trench. While the magnitude of this error can be controlled by carefully selecting the etchant and the time that the etchant will be applied for, it is impossible to eliminate this issue completely without under etching the region. This can lead to a number of problems, such as inconsistent current densities in regions. As we've seen in lecture, areas of abnormally high current density can lead to electromigration.

Solution 8

While copper has better electromigration characteristics than aluminum, it also diffuses into silicon rapidly, making it a difficult material to justify using in ICs. As a result, until fabrication houses were able to consistently include barrier metals in their processes, most locations used aluminum instead of copper for connecting to silicon regions.

Solution 9

a) The only real necessary part of the MOS is the channel which is the overlap of the Poly and the n-active region. Its width is 4um and its length is 1um.
b) For positive photoresist:
$W = 4 - 2 * 0.5 = 3.9\mu m$
$L = 1 - 2 * 0.2 = 0.6\mu m$
c) For negative photoresist:
$W = 4 + 2 * 0.5 = 4.1\mu m$
$L = 1 + 2 * 0.2 = 1.4\mu m$

Solution 10

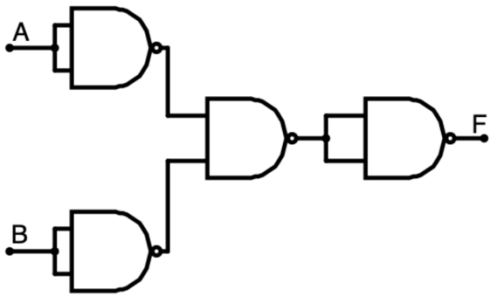
For a NMOS transistor, when V_{GS} is low I_D will be zero meaning that the switch is effectively "off". When V_{GS} is high the switch will be "on" and the V_{DS} will become zero. A PMOS transistor operates in a similar matter but it is in the "off" position when V_{GS} is close to zero, and the transistor is "on" when V_{GS} is close to $-V_{DD}$ (the source voltage).

Solution 11

To implement a 2-input NOR gate using only NAND gates, start by taking the logic expression for a NOR gate and using De Morgans' Law on it:

$$F = \overline{A + B} = \overline{\bar{A}\bar{B}}$$

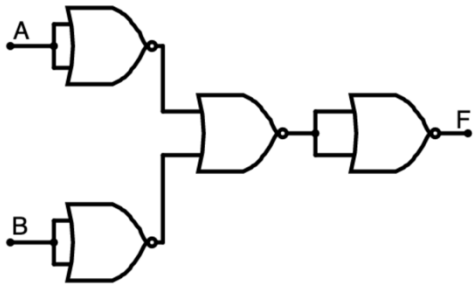
This can be made using NAND gates as follows:



To implement a 2-input NAND gate using only NOR gates, do the same as the previous solution:

$$F = \overline{AB} = \bar{A} + \bar{B} = \overline{\overline{\bar{A} + \bar{B}}}$$

Which can be implemented as follows:



Solution 12

The easiest way to prove or disprove that two expressions are equivalent is either to use a truth table or to algebraically simplify the expressions. A mix of these strategies will be used below:

a) $\bar{A}A + \bar{A}\bar{B}(C + B) = \bar{A}\bar{B}C$
Left Side: $\bar{A}A + \bar{A}\bar{B}(C + B) = \bar{A}\bar{B}C + \bar{A}\bar{B}B = \bar{A}\bar{B}C$
Right Side: $\bar{A}\bar{B}C$
Because the left side equals the right side, this expression is true.

b) $\bar{A}(\bar{B} + C\bar{B}) = \bar{A}\bar{B} + C\bar{A} + \bar{A}BA$
Left Side: $\bar{A}(\bar{B} + C\bar{B}) = \bar{A}\bar{B} + \bar{A}C\bar{B}$
Right Side: $\bar{A}\bar{B} + C\bar{A} + \bar{A}BA = \bar{A}\bar{B} + C\bar{A}$
Because the left side does not equal the right side, this expression is false.

c) $(A + B)(A + C) = A + BC$
Left Side: $(A + B)(A + C) = A + AC + BA + BC$
Right Side: $A + BC$
Because the left side does not equal the right side, this expression is false.

d) $A + (\bar{A}B) = A + B$
Left Side:

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

Right Side:

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

Because the left side equals the right side, this expression is true.

e) $AB + \bar{A}C + BC = AB + \overline{AC}$
Left Side:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Right Side:

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Because the left side does not equal the right side, this expression is false.