EE 330

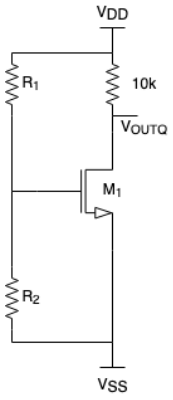
Homework 10

Fall 2020

Due Friday October 23

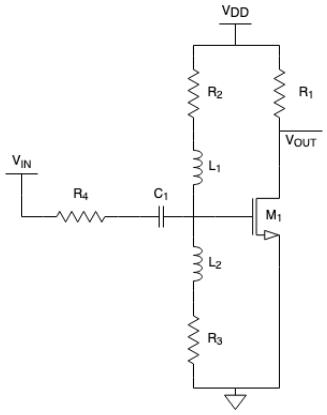
Problem 1

Choose appropriate values for R_2 and R_1 to ensure that the circuit below is biased such that M_1 is in saturation and $V_{OUTQ} = 2V$. You may assume that M_1 is fabricated in the AMI 05 process and is minimally sized. Assume that $V_{DD} = 5V$ and $V_{SS} = 0V$.



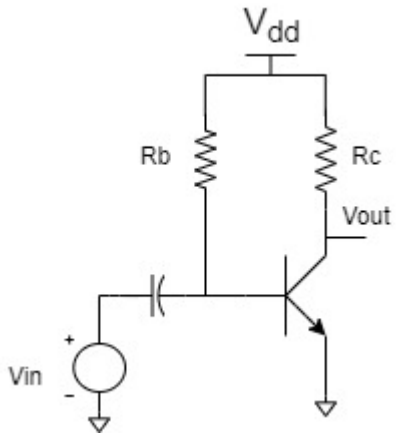
Problem 2

In the circuit below, assume that $V_{DD} = 5V$, V_{IN} is a small-signal AC input, C_1 is large, L_1 and L_2 are large, and M_1 is a minimally-sized device fabricated in the AMI 05 process. Suppose that $R_1 = 10k\Omega$, $R_2 = 17.5k\Omega$, $R_3 = 10k\Omega$, and $R_4 = 1.57k\Omega$. Find V_{OUTQ}.



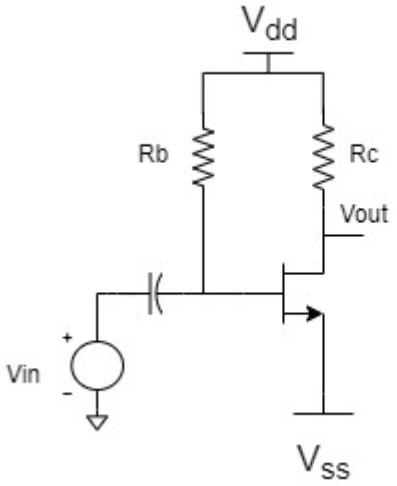
Problem 3

Determine Voutq and Vout(t) if Vin = 0.75sin(500t). Assume β=100 and Vdd = 10V with Rb = 150kΩ Rc = 1kΩ.



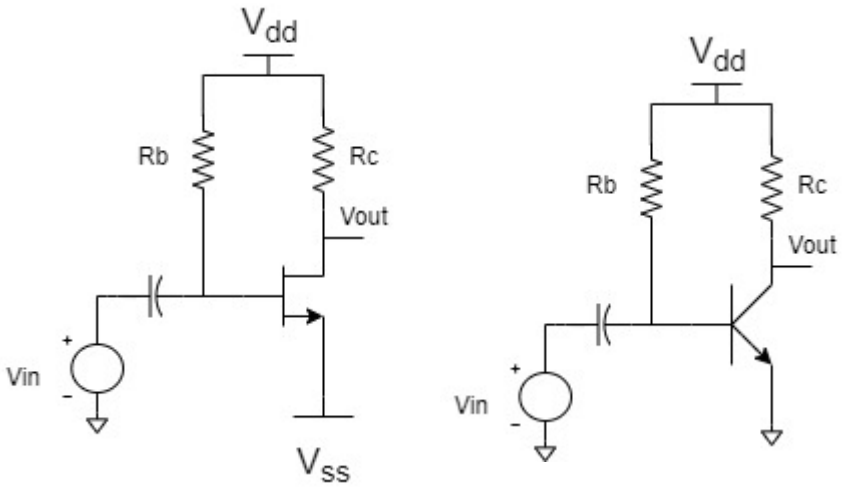
Problem 4

Determine Voutq and Vout(t) if Vin = 2 sin(500t). Assume the AMI06 process and Vdd = 10V, Vss= 5V with Rb = 150kΩ Rc = 2kΩ.



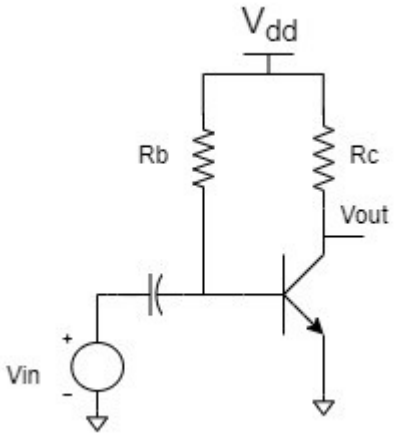
Problem 5

Given the following two circuits, with β=100, the MOSFET has a uCOX of $56.4 * 10^{-6}$ and $\frac{W}{L} = 1$ with $V_T = 0.71V$. Rb = 100kΩ and Rc = 150Ω for the BJT and 5kΩ for the MOSFET, find Vdd for each circuit such that their gain is the same (for the MOS you have control of VSS as well). Comment on how much the circuits differ and what changes to get the gain the same.



Problem 6

Draw out the two-port Thevenin equivalent amplifier for the following circuit. Equate the different parameters between the small signal circuit and the amplifier you drew out. After that, find Rin, Rout and Av for the amplifier. Explain how you found each value (**do not** just restate the final relationships).



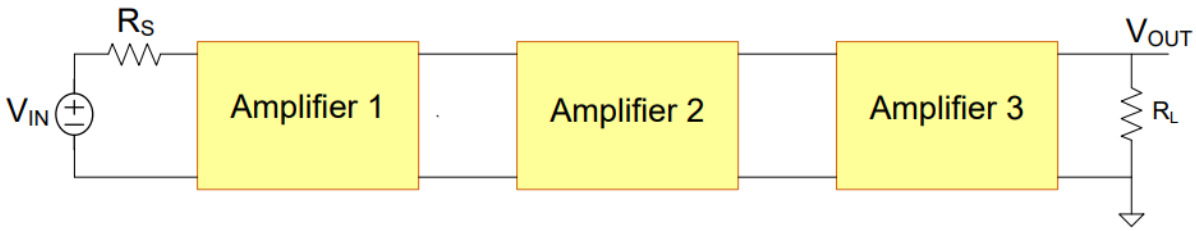
Problem 7

For the following array of amplifiers, note the output at each step as well as at Vout for the following values given Vin = 5V and Rs= 100kΩ and RL=5kΩ. At each step comment on the impact of Rin and Rout of each amplifier. What would be the ideal output of the array? Is it different from your calculations? Why? (try not to round too much so you get a better idea of possible differences).

Amp 1: $A_v = 100; R_{in} = \infty; Rout = 1\Omega;$

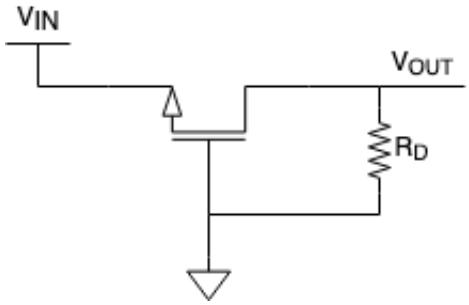
Amp 2: $A_v = \frac{1}{200}; R_{in} = 100k\Omega; Rout = 500\Omega;$

Amp 3: $A_v = 2; R_{in} = 50k\Omega; Rout = 1k\Omega;$



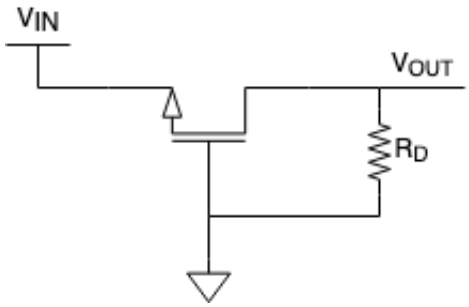
Problem 8

The below circuit is shown in the small-signal domain. Assume that the circuit is biased such that the MOSFET is operating in the saturation region. Derive the small-signal gain of the circuit. Assume $\lambda = 0$.



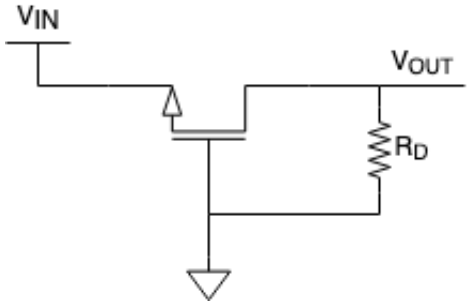
Problem 9

Derive (do not simply restate) the small-signal input impedance of the common-gate amplifier shown below. If necessary, you may assume that $\lambda = 0$.



Problem 10

Derive (do not simply restate) the small-signal output impedance of the common-gate amplifier shown below. If necessary, you may assume that $\lambda = 0$.

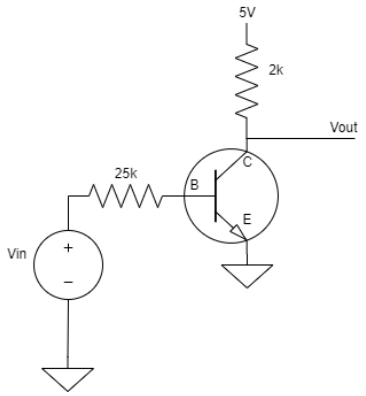


Problem 11 & 12

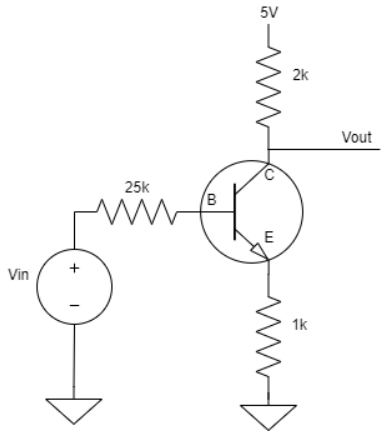
BJT review

For this problem, assume that β is 100. Remember that $I_E = I_B + I_C$ is true in all operating regions.

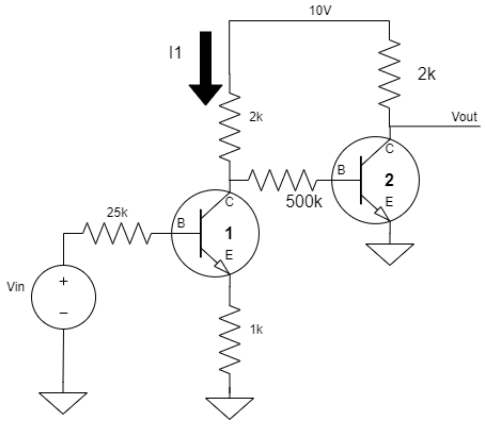
a) Find V_{OUT} for V_{IN} = 1V, 1.5V, and 2V. For each V_{IN}, state and prove what region the BJT is in.



b) For this second circuit, the emitter is no longer grounded. So, in forward active, V_B is no longer 0.6, instead it is V_E + 0.6V. Find V_{out} again for Vin = 1V, 1.5V, and 2V.



c) For this third circuit, an additional device has been added. Note that I1 is **NOT** I_{C1} since current can also go through the base of device 2, if it is active. Find V_{out} when Vin = 1V, 1.5V, and 2V.



MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							

angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON