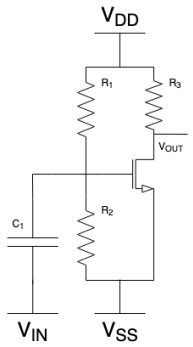
EE 330

Homework 11 Solutions

Fall 2020 (Problem 5 corrected 7 pm Nov 2)

Solution 1

To meet the given specifications, we need to choose an amplifier topology which has a high input impedance, a large gain, and a configurable output impedance. A common-source structure can be made to meet these specifications.



We will assume C_1 is large (perhaps $10\mu F$), meaning that it acts like a short-circuit in the small-signal domain and an open-circuit in the large-signal domain.

To bias the circuit, let's first look at the large-signal domain. We need the output voltage to be quiescently $5V$ when V_{DD} is $10V$. If we let R_3 be $10k\Omega$ (less than the upper limit of $15k\Omega$), this means that the MOSFET has a quiescent current flowing through it which is equal to $500\mu A$.

To achieve the gain that we need in this circuit, recall that the gain of a common-source structure is given by the following equation:

$$A_V = \frac{-2I_{DQ}R_3}{V_{EB}}$$

We have already set I_{DQ} to be $500\mu A$ and R_3 to be $10k\Omega$. So, we need to calculate for V_{EB}:

$$V_{EB} = -\frac{2I_{DQ}R_3}{A_V} = \frac{500\mu A * 10k\Omega}{5} = 1$$

If we assume that $V_T = 0.79V$, this means that the device's gate voltage needs to be $1.79V$. We can achieve that in the large-signal domain by noting that R_1 and R_2 form a voltage divider:

$$V_G = 1.79 = \frac{R_2}{R_1 + R_2}10$$

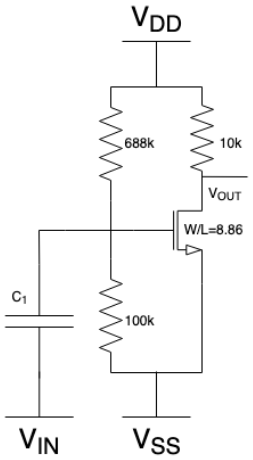
Letting $R_2 = 150k\Omega$ (chosen arbitrarily; it is only necessary that $R_2 > R_1 > 100k\Omega$), we can find R_1 to be $688k\Omega$.

Finally, using the V_{EB} that we calculated, along with the quiescent current, size the MOSFET:

$$I_D = 500\mu = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{EB})^2 = 56.4\mu\frac{W}{L}$$

$$\frac{W}{L} = 8.86$$

The final design is shown below:



Solution 2 & 3

Part A:

To find the circuit's quiescent input, perform a large-signal analysis. C_1 becomes an open-circuit in a large-signal analysis, meaning that the voltage at the MOSFET's gate is now simply the result of the voltage divider:

$$V_G = \frac{100k\Omega}{100k\Omega + 700k\Omega}10 = \frac{1}{8} * 10 = 1.25V$$

The amplifier's quiescent input voltage is then $1.25V$.

Part B:

To find the circuit's quiescent output, first determine the quiescent current flowing through the MOSFET:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GSQ} - V_{Tn}\right)^2 = 56.4\mu * 10 * (1.25 - 0.79)^2 = 119\mu A$$

Now, calculate the voltage:

$$V_{OUTQ} = V_{DD} - I_{DQ}15k\Omega = 8.21V$$

Part C:

This is a common-source amplifier. It's gain is thus given by the following expression:

$$A_V = -\frac{2I_{DQ}R}{V_{EB}} = -\frac{2[119\mu][15k\Omega]}{[1.25-0.79]} = -7.78$$

Part D:

Clipping will occur when either (a) the output voltage tries to exceed $10V$, (b) the output voltage tries to drop below $0V$. The device will drop out of saturation when either the input voltage drops below V_{Tn} and or when drain-source voltage of the device is less than V_{EB}. Let's express this mathematically:

Clips on upper extreme: $V_{OUT} = 10 = V_{OUTQ} + A_V v_{in} = 8.21 - 7.78v_{in} \rightarrow v_{in} = -0.23V$

Clips on lower extreme: $V_{OUT} = 0 = V_{OUTQ} + A_V v_{in} = 8.21 - 7.78v_{in} \rightarrow v_{in} = 1.06V$

Device turns off: $V_{GS} = V_{INQ} + v_{in} \leq V_{Tn} = 0.79V \rightarrow v_{in} \leq V_{Tn} - V_{INQ} = -0.46V$

Device drops out of saturation: $V_{DS} = V_{OUTQ} + A_V v_{in} \leq V_{GS} - V_{Tn} = V_{INQ} + v_{in} - V_{Tn} \rightarrow 0.883V$

The lowest magnitude of the input amplitude which will cause distortion of some form is $0.23V$. At this voltage, clipping will begin on the amplifier's upper extreme.

Part E:

Simply solve for current through the MOS will exposed to an input of $V_{INQ} + 0.23V$:

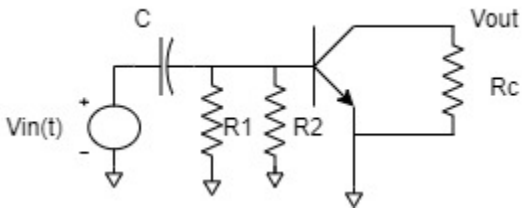
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{Tn})^2 = [56.4\mu][10]\left[V_{INQ} + 0.23 - 0.79\right]^2 = 269\mu A$$

Solution 4

a) For q points, we remove all AC components. This means Vin(t) source is an SC, and the capacitor is an OC. This means we can "cut off" the left part.

By definition, if the BJT is on, Vb = 0.7V $\Rightarrow I_b = I_{R1} - I_{R2} = \frac{Vdd-0.7}{100k\Omega} - \frac{0.7}{10k\Omega} = 23\mu A$
We start off assuming *F.A. so* $I_C = 100 * I_b = 2.3mA$
This means that $V_{outq} = 10 - 2.3 * 2.5 = 4.25V$ and $I_{CQ} = 2.3mA$
To confirm F.A, Vce > 0.2V, so it is in F.A.

b) For ss-equivalent, we remove all DC components. The capacitor, since it is large, is a SC.



c) <u>For Av:</u>

$$A_V = -\frac{I_{CQ}R_C}{v_t} = -\frac{2.3 * 2.5}{0.025} = -230$$

For Rin:

This will be R1, R2 and the BJT input resistance in parallel

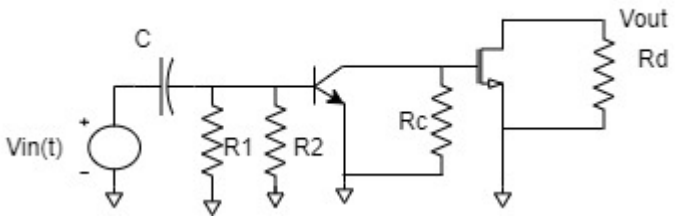
$$Rin = \left(\frac{1}{100*10^3} + \frac{1}{10*10^3} + \frac{1}{\frac{\beta v_t}{I_{CQ}}}\right)^{-1} = \left(\frac{1}{100*10^3} + \frac{1}{10*10^3} + \frac{1}{\frac{100*0.025}{2.3*10^{-3}}}\right)^{-1} = 970.87\Omega$$

For Rout:

This will just be Rc = 2.5kΩ

Solution 5

First I will draw out the SS-equivalent circuit. This tells be what amplifiers I should chain together.



This means I have a BJT CE amplifier and a MOS CE amplifier.

$$A_V = \frac{V_{out}}{V_{in}} = A_{V1BJT}A_{V2MOS}A_{in} = 1 * \left(-\frac{I_{CQ1}}{V_t} * R_{C\backslash\backslash R_{in2}}\right)\left(-\frac{2I_{DQ2}R_D}{V_{GSQ2} - V_{T2}}\right)$$

Since there is no resistor dropping the voltage to the input of the BJT, there is no gain on the input.

Since the MOS input resistance is infinite, it disappears from the term so we are left with:

$$A_V = \frac{V_{out}}{V_{in}} = A_{V1BJT}A_{V2MOS} = \left(-\frac{I_{CQ1}R_C}{V_t}\right)\left(-\frac{2I_{DQ2}R_D}{V_{GSQ2} - V_{T2}}\right)$$

Solutions 6

First we need to find the Qpoints for the voltages and currents. To do this we "remove" all AC components (Vin(t) is a short, and C is an OC.)

First MOS 1:

$$V_{GS1Q} = V_{dd} * \frac{R_2}{R_2 + R_1} = 3.33V$$

$$I_{D1Q} = \frac{uCox}{2}\frac{W}{L}\left(V_{GS_Q} - V_T\right)^2 = 56.4 * 10^{-6} * \frac{3}{0.6}(3.33 - 0.79)^2 = 1.83mA$$

$V_{D1Q} = 10 - 1.5 * 1.83 = 7.26V$

$V_{DS1} = 7.26 > 3.33 - .79 = V_{GS} - VT$ so we are in saturation like we assumed.

Second MOS 2:

$V_{GS2Q} = V_{DS1Q} = 7.26V$

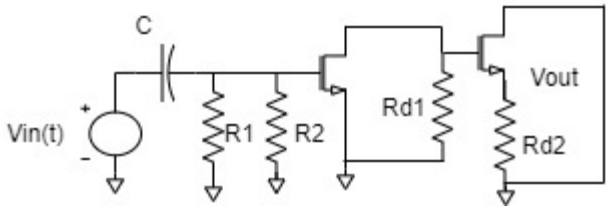
$I_{D2Q} = \frac{uCox}{2}\frac{W}{L}\left(V_{GS2_Q} - V_T\right)^2$

And also $I_{D2Q} = \frac{V_{S2Q}}{Rd2}$

So $\frac{V_{S2Q}}{5k\Omega} = 56.4 * 10^{-6} * \frac{3}{0.6}\left(7.26 - V_{S2Q} - 0.79\right)^2$

(using solver) $V_{S2Q} = \begin{cases} 4.65V \\ 9V \end{cases}$, $V_{S2Q} = 9V$ is not possible since $V_{GS} = 5.83 - 9 < 0$ meaning the MOS would be off. For $V_{S2Q} = 4.65V$ $V_{DS} = 10 - 4.65 = 5.35 > 5.83 - 0.79 = V_{GS} - VT$ confirming Saturation. Now that we have all the Q points, we can move on to SS. $I_{DQ2} = 0.93mA$

The SS-Equivalent circuit is:



This means we have a CS and a CD cascaded.

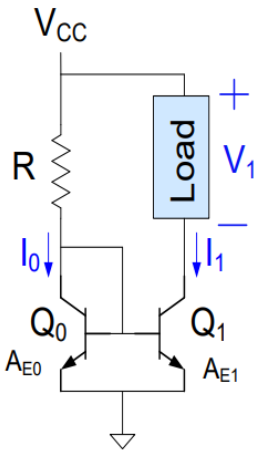
$$A_V = A_{V1BJT}A_{V2MOS}A_{in} = 1 * \left(-\frac{2I_{DQ1}}{V_{GSQ1} - V_{T1}} * R_{d1\backslash\backslash R_{in2}}\right)\left(-\frac{2I_{DQ2}R_{d2}}{2I_{DQ2}R_{d2} + V_{GSQ2} - V_{T2}}\right)$$

Since R_{in2} is the input resistance of the 2nd mosfet, and is infinite, it does not impact the previous gain. By plugging in out numbers we get:

$$A_V = \left(-\frac{2 * 1.83mA}{3.33 - 0.79} * 1.5k\Omega\right)\left(-\frac{2 * 0.93mA * 5k\Omega}{2 * 0.93mA * 5k\Omega + ((7.26 - 4.65) - 0.79)}\right) = \frac{51.06}{28.24} = 1.81$$

Solution 7

First we need to visualize the current mirror.



Since the base currents are extremely low, we can "approximate" them to be 0. This means:

$$\frac{I_{C2}}{I_{C1}} = \frac{J_S A_2 e^{\frac{V_{BE2}}{v_t}}}{J_S A_1 e^{\frac{V_{BE1}}{v_t}}} = \frac{A_2}{A_1}$$

Since the BJTs are from the same process, and their Bases are tied, their VBE will be the same and their Js will be the same.

$$I_{C2} = \frac{A_2}{A_1} I_{C1} \approx \frac{A_2}{A_1} \frac{Vdd - 0.7}{R} = \frac{A_2}{A_1} \frac{5 - 0.7}{R}$$

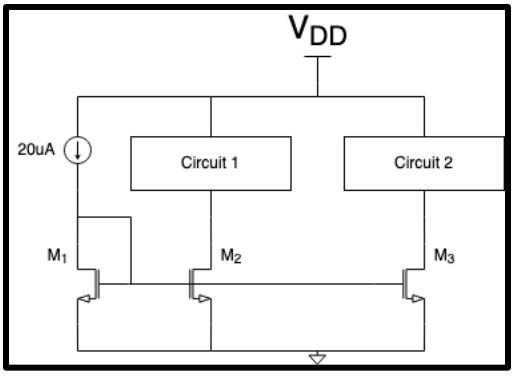
This means that $10mA = \frac{A_2}{A_1} \frac{5-0.7}{R}$. If I arbitrarily choose a resistor of 2.15kΩ :

$$10mA = \frac{A_2}{A_1} \frac{5 - 0.7}{4.3k\Omega} = \frac{A_2}{A_1} * 2 * 10^{-3}$$

then the areas can have a ratio of 5/1 and I will choose $80\mu m^2$ for A1 and $400\mu m^2$for A2.

Solution 8

Given a single current source and any number of MOSFETs to use, the easiest way to bias this circuit is to create a simple current mirror. The $20\mu A$ source will be used as a reference current, and two devices will mirror and scale the current to the needed values. This creates the circuit shown below.



The size of M_1 is a degree of freedom which is unused, so we can set it to whatever we want. Let's set the width-length ratio of M_1 to 10.

To draw $10\mu A$ from Circuit 1, we need to size M_2 such that it mirrors half of M_1's current:

$$I_{M2} = 20\mu * \frac{W_2/L_2}{W_1/L_1} = 20\mu * \frac{W_2/L_2}{10}$$

$$\frac{W_2}{L_2} = \frac{10\mu A}{20\mu A} * 10 = 5$$

The same process can be used for M_3:

$$I_{M3} = 20\mu * \frac{W_3/L_3}{W_1/L_1} = 20\mu * \frac{W_3/L_3}{10}$$

$$\frac{W_3}{L_3} = \frac{50\mu A}{20\mu A} * 10 = 25$$

Solution 9 & 10

For the first part, finding the current through R_L is as simple as recalling the basic current mirror equation:

$$I_{M2} = I_{M1}\frac{W_2/L_2}{W_1/L_1} = 20\mu\frac{20}{10} = 40\mu A$$

To see how the current changes when variation is introduced, begin by deriving the equation which allows us to find the current drawn through R_L. Do this by expressing the current through M_1 and M_2 separately, then divide them:

$$I_{M1} = 20\mu A = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_{Tn})^2 = \frac{1}{2}[112.8\mu][10][V_{GS1} - V_{Tn}]^2$$

$$I_{M2} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{GS1} - V_{Tn})^2$$

$$\frac{I_{M2}}{I_{M1}} = \frac{I_{M2}}{20\mu} = \frac{\mu_n C_{ox}\frac{W_2}{L_2}(V_{GS1} - V_{Tn})^2}{[112.8\mu][10][V_{GS1} - V_{Tn}]^2}$$

Now, substitute values in for each scenario and solve.

Scenario 1:

$$\frac{I_{M2}}{20\mu} = \frac{118.44\mu * 20(V_{GS1} - 0.79)^2}{[112.8\mu][10][V_{GS1} - 0.79]^2} = 2.1$$

$$I_{M2} = 42\mu A$$

Scenario 2:

$$\frac{I_{M2}}{20\mu} = \frac{112.8\mu * 20(V_{GS1} - 0.83)^2}{[112.8\mu][10][V_{GS1} - 0.79]^2} = 2\left(\frac{V_{GS1} - 0.83}{V_{GS1} - 0.79}\right)^2$$

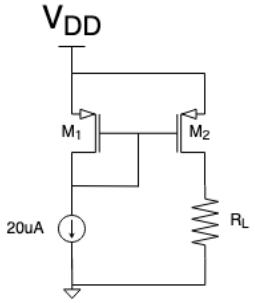
$$I_{M2} = 40\mu A\left(\frac{V_{GS1} - 0.83}{V_{GS1} - 0.79}\right)^2$$

Scenario 3:

$$\frac{I_{M2}}{20\mu} = \frac{112.8\mu * 21(V_{GS1} - 0.79)^2}{[112.8\mu][10][V_{GS1} - 0.79]^2} = 2.1$$

Solution 11

To create a current mirror which sources $20\mu A$ instead of sinks $20\mu A$, we need to use a current mirror with PMOS devices instead of NMOS devices. This is shown below.



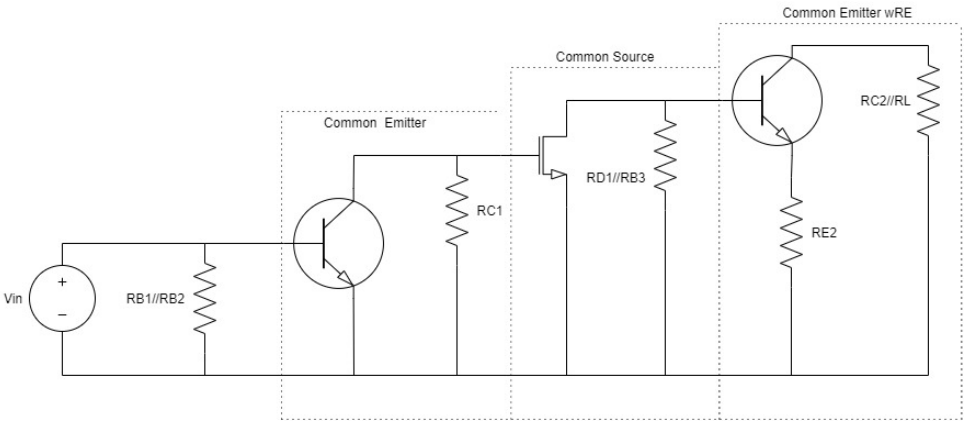
Lets assume that $\frac{W_1}{L_1} = 10$. To source $50\mu A$, we need to size $\frac{W_2}{L_2}$ as follows:

$$I_{M2} = 50\mu A = I_{M1}\frac{W_2/L_2}{W_1/L_1} = 2\mu A * W_2/L_2$$

$$\frac{W_2}{L_2} = 25\mu A$$

Solutions12

a)



b) $A_V = -g_{m1} * g_{m2}(R_{C1})(R_{D1}\backslash\backslash A_V = -g_{m1} * g_{m2}(R_{C1})(R_{D1}//R_{B3})(\frac{R_L//R_{C2}}{R_{E2}})$