

EE 330
Homework 5
Fall 2020
Due Wednesday September 16

Problem 1

Assume a resistor has a resistance of $1\text{K}\Omega$ at $T=273^\circ\text{K}$. If the TCR of this resistor is constant of value $1100\text{ ppm}/^\circ\text{C}$, what will be the resistance at $T=300^\circ\text{K}$?

Problem 2

Assume a resistor has a resistance with a function $R(T) = 5T + 1000$ where T is in Celsius. If you use the values $T=25^\circ\text{C}$ and 47°C , what is the TCR of the resistor?

Problem 3

Consider a 5K resistor that is made by the series connection of two resistors. One of the resistors is a n^+ doped $2\text{K}\Omega$ polysilicon resistor with a TCR of $-600\text{ ppm}/^\circ\text{C}$ and the other is a p^+ diffused silicon $3\text{K}\Omega$ resistor with a TCR of $1000\text{ ppm}/^\circ\text{C}$. What is the TCR of the series combination?

Problem 4

Design a 500Ω resistor with a 1% accuracy in the AMI 06 process. Use Poly 1 for the resistor and a width-length ratio of an imaginary box enclosing the resistor should be 1:1. Sketch out the boxes and count the resistance. For the minimum width look at the design rules on Dr. Geiger's website.

Problem 5

Design a 100fF capacitor in the AMI 06 process. Your only restrictions are you need to use 3 layers to do so. Clearly specify which layers you are using for this capacitor. The layout of the capacitor can be either sketched or come from a Cadence layout.

Problem 6

If the voltage of a forward-biased p - n junction is varied between 0.5V and 0.6V , what is the range in the diode current? Assume the junction area of the diode is $75\mu\text{m}^2$ and $J_s = 10^{-15}\text{ A}/\mu\text{m}^2$

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU
TECHNOLOGY: SCN05
microns

VENDOR: AMIS
FEATURE SIZE: 0.5

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	
ohms/sq								
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	
aF/um^2									
Area (N+active)			2434		35	16	11		
aF/um^2									
Area (P+active)			2335						
aF/um^2									
Area (poly)				938	56	15	9		
aF/um^2									
Area (poly2)					49				
aF/um^2									
Area (metal1)						31	13		
aF/um^2									
Area (metal2)							35		
aF/um^2									
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg, 5.0V)		95.31	MHz
D256_WIDE (31-stg, 5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg, 5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg, 5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON

T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 11/07

* LOT: T6AU WAF: 7101

* Temperature_parameters=Default

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.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ      = 1.5E-7       NCH  = 1.7E17      TOX   = 1.42E-8
+K1      = 0.8976376    K2   = -0.09255    VTH0  = 0.629035
+K3B     = -8.2369696   W0   = 1.041146E-8  K3    = 24.0984767
+DVT0W   = 0           DVT1W = 0          NLX   = 1E-9
+DVT0    = 2.7123969    DVT1 = 0.4232931  DVT2W = 0
+DVT0    = 2.7123969    DVT1 = 0.4232931  DVT2  = -0.1403765
+U0      = 451.2322004  UA   = 3.091785E-13  UB    = 1.702517E-18
+UC      = 1.22401E-11  VSAT = 1.715884E5    A0    = 0.6580918
+AGS     = 0.130484     B0   = 2.446405E-6    B1    = 5E-6
+KETA    = -3.043349E-3 A1   = 8.18159E-7    A2    = 0.3363058
+RDSW    = 1.367055E3  PRWG = 0.0328586    PRWB   = 0.0104806
+WR      = 1           WINT  = 2.443677E-7  LINT   = 6.999776E-8
+XL      = 1E-7        XW    = 0          DWG    = -1.256454E-8
+DWB     = 3.676235E-8  VOFF = -1.493503E-4  NFACTOR = 1.0354201
+CIT      = 0          CDSC  = 2.4E-4      CDSCD  = 0
+CDSCB   = 0          ETA0   = 2.342963E-3  ETAB   = -1.5324E-4
+DSUB    = 0.0764123   PCLM  = 2.5941582    PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505  DROUT  = 0.9919348
+PSCBE1  = 6.611774E8  PSCBE2 = 3.238266E-4  PVAG   = 0
+DELTA   = 0.01        RSH   = 83.5       MOBMOD = 1
+PRT     = 0           UTE   = -1.5       KT1    = -0.11
+KT1L    = 0           KT2   = 0.022      UA1    = 4.31E-9
+UB1     = -7.61E-18   UC1   = -5.6E-11    AT     = 3.3E4
+WL      = 0           WLN   = 1          WW    = 0
+WWN     = 1           WWL   = 0          LL    = 0
+LLN     = 1           LW    = 0          LWN   = 1
+LWL     = 0           CAPMOD = 2         XPART  = 0.5
+CGDO    = 2.32E-10    CGSO  = 2.32E-10    CGBO   = 1E-9
+CJ      = 4.282017E-4  PB    = 0.9317787    MJ     = 0.4495867
+CJSW    = 3.034055E-10  PBSW = 0.8          MJSW   = 0.1713852
+CJSWG   = 1.64E-10    PBSWG = 0.8          MJSWG  = 0.1713852
+CF      = 0           PVTH0 = 0.0520855  PRDSW  = 112.8875816
+PK2     = -0.0289036  WKETA = -0.0237483    LKETA  = 1.728324E-3
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.MODEL CMOSP PMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 49
+XJ      = 1.5E-7       NCH  = 1.7E17      TOX   = 1.42E-8
+K1      = 0.5464347    K2   = 8.119291E-3    VTH0  = -0.9232867
+K3B     = -0.8373484   W0   = 1.30945E-8    K3    = 5.1623206
+DVT0W   = 0           DVT1W = 0          NLX   = 5.772187E-8
+DVT0    = 2.0973823    DVT1 = 0.5356454  DVT2W = 0
+DVT0    = 2.0973823    DVT1 = 0.5356454  DVT2  = -0.1185455
+U0      = 220.5922586  UA   = 3.144939E-9  UB    = 1E-21
+UC      = -6.19354E-11 VSAT = 1.176415E5    A0    = 0.8441929
+AGS     = 0.1447245    B0   = 1.149181E-6    B1    = 5E-6
+KETA    = -1.093365E-3 A1   = 3.467482E-4    A2    = 0.4667486
+RDSW    = 3E3          PRWG = -0.0418549  PRWB   = -0.0212201
+WR      = 1           WINT  = 3.007497E-7  LINT   = 1.040439E-7
+XL      = 1E-7        XW    = 0          DWG    = -2.133809E-8

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+DWB	= 1.706031E-8	VOFF	= -0.0801591	NFACTOR	= 0.9468597
+CIT	= 0	CDSC	= 2.4E-4	CDSCD	= 0
+CDSCB	= 0	ETA0	= 0.4060383	ETAB	= -0.0633609
+DSUB	= 1	PCLM	= 2.2703293	PDIBLC1	= 0.0279014
+PDIBLC2	= 3.201161E-3	PDIBLCB	= -0.057478	DROUT	= 0.1718548
+PSCBE1	= 4.876974E9	PSCBE2	= 5E-10	PVAG	= 0
+DELTA	= 0.01	RSH	= 105.3	MOBMOD	= 1
+PRT	= 0	UTE	= -1.5	KT1	= -0.11
+KT1L	= 0	KT2	= 0.022	UA1	= 4.31E-9
+UB1	= -7.61E-18	UC1	= -5.6E-11	AT	= 3.3E4
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	XPART	= 0.5
+CGDO	= 3.12E-10	CGSO	= 3.12E-10	CGBO	= 1E-9
+CJ	= 7.254264E-4	PB	= 0.9682229	MJ	= 0.4969013
+CJSW	= 2.496599E-10	PBSW	= 0.99	MJSW	= 0.386204
+CJSWG	= 6.4E-11	PBSWG	= 0.99	MJSWG	= 0.386204
+CF	= 0	PVTH0	= 5.98016E-3	PRDSW	= 14.8598424
+PK2	= 3.73981E-3	WKETA	= 7.286716E-4	LKETA	= -4.768569E-3

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