EE 330

Homework 11

Fall 2020

Due Friday October 30

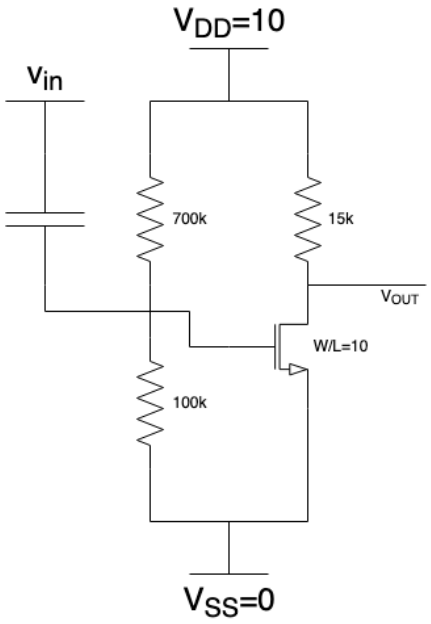
Problem 1

Design and bias an amplifier such that it has an input impedance which exceeds $100k\Omega$, a small-signal gain of -10, and an output impedance which is no greater than $15k\Omega$. You may use one power supply having a value of $10V$ and any number of resistors, capacitors, and MOSFETs. You may assume that your MOS device is fabricated in the AMI06 process. Your amplifier's quiescent output should be $5V$.

Problem 2 & 3

Suppose you are given the circuit seen below. Answer the following questions about the circuit. Assume the circuit was fabricated in the AMI06 process and that C_1 is large.

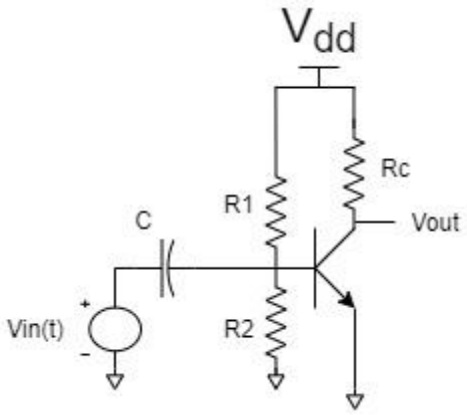
a) What is the circuit's quiescent input voltage?
b) What is the circuit's quiescent output voltage?
c) What is the circuit's small-signal gain?
d) What is the maximum amplitude that can be used for the small signal input (v_{in}) which will avoid clipping and keep the MOSFET in saturation?
e) What would be the maximum current drawn through the MOSFET if the small-signal input was set to the maximum amplitude that you calculated in part d?



Problem 4

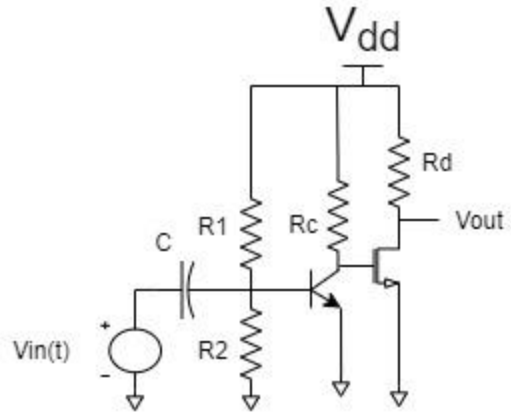
For the following amplifier assume C is large, Vdd = 10V, R1=100kΩ, R2=10kΩ, β=100, RC=2.5kΩ.

a) Find the quiescent Voutq and Icq
b) Draw the ss-equivalent circuit
c) Determin Av, Rin and Rout of the whole system (not just the BJT)



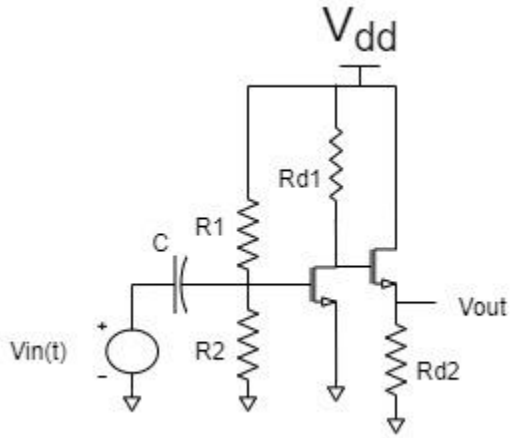
Problem 5

Find the gain of the following configuration. Your answer should be in terms of quiescent currents and voltages:



Problem 6

Find the gain of the following configuration. You will need to evaluate the quescent circuit first and plug in the values to get the actual gain: Vdd=10V, R1=20kΩ, R2=10kΩ, Rd1=1.5kΩ, Rd2=5kΩ, C: very large, all MOS devices in the AMI06 process

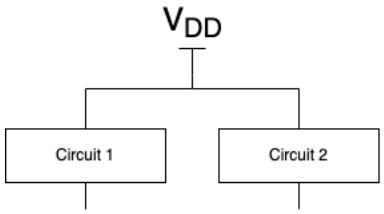


Problem 7

Design a current sink source with 2 BJT's and with Vdd of 5V. You have control of the areas of the BJTs and the resistor for biasing. Given these constraints, design the current mirror such that the load current (on the collector of the 2nd BJT) is 10mA. Prove your design step by step, do not simply use the equations from class. Use Vbe of 0.7V.

Problem 8

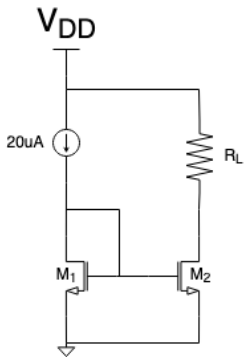
In the figure below, assume that Circuit 1 needs to be biased by a $10\mu A$ current to operate correctly, and that Circuit B needs to be biased with $50\mu A$. You have a single $20\mu A$ current source available to you. Using only MOSFETs fabricated in the AMI06 process and your single current source, design a circuit which will draw the necessary current from each circuit. You should sink the current from both circuits through the wires leading from the bottom of them. Your design should include width-length ratios for all MOSFETs.



It is not necessary, but if you would like a challenge, figure out how to implement the circuit using only MOSFET devices and the already-present voltage source. Assume the source voltage is $2.5V$.

Problem 9 & 10

Suppose you have the current mirror shown below.



Assume all MOSFETs are fabricated in the AMI06 process and that the μC_{ox} and V_T values for all devices are equal to minimally sized devices. Let the width-length ratio of M_1 be 10 and the width-length ratio of M_2 be 20. What is the expected current through R_L?

The current you just calculated is correct only if M_1 and M_2 operate *exactly* as specified. However, this is not realistic, and a number of sources introduce error and variation in real circuits. Calculate the current through R_L in each of the following scenarios:

	Specifications for M_1			**Specifications for M_2**		
Scenario #	μC_{ox}	V_T	W/L	μC_{ox}	V_T	W/L
1	$112.8\mu A/V^2$	$0.79V$	10	$118.44\mu A/V^2$	$0.79V$	20
2	$112.8\mu A/V^2$	$0.79V$	10	$112.8\mu A/V^2$	$0.83V$	20
3	$112.8\mu A/V^2$	$0.79V$	10	$112.8\mu A/V^2$	$0.79V$	21

Note that you may not be able to get an actual value for Scenario 2. Your answer should be in terms of V_{GS1} or V_{GS2}.

Problem 11

Design a current mirror which *sources (not sinks)* $50\mu A$ to a load. You have any number of MOSFETs available to use and only *one* $20\mu A$ current source.

Problem 12

Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

a) Draw the small signal equivalent circuit.

b) Determine an expression for the small-signal voltage gain in terms of the small signal model parameters of the transistors and the passive components