EE 330

Homework 10 Solutions

Fall 2020

Solution 1

Because M_1 is in saturation, the current through it can be modeled using the following equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GSQ} - V_T\right)^2$$

For a minimally sized device in the AMI 05 process, $W/L = 5$, $\mu_n C_{ox}/2 = 56.4\mu$, and $V_T = 0.79V$. If $V_{OUTQ} = 2V$ and $V_{DD} = 5V$, this implies that the current through the $10k\Omega$ resistor is:

$$I_D = \frac{5-2}{10k\Omega} = \frac{3}{10k\Omega} = 300\mu A$$

We can then solve for the V_{GSQ} which will ensure that M_1 is conducting the same amount of current.

$$300\mu A = [56.4\mu][5]\left[V_{GSQ} - 0.79\right]^2 \rightarrow V_{GSQ} = -0.241V\ OR\ 1.82V$$

It is not possible for V_{GSQ} to be $-0.241V$ since that would imply that (a) we have a voltage which is less than our minimum voltage source and (b) the MOSFET is off. So, $1.82V$ is the only valid option. What's more, this satisfies the conditions for M_1 to be in saturation:

$$V_{GS} \geq V_{Tn} \rightarrow 1.82 \geq 0.79 \rightarrow True$$

$$V_{DS} \geq V_{GS} - V_{Tn} \rightarrow 2 \geq 1.82 - 0.79 \rightarrow True$$

How do we achieve $1.82V$ at the gate of M_1? By sizing R_1 and R_2 appropriately:

$$1.82 = \frac{R_2}{R_2 + R_1} * 5 \rightarrow 1.82(R_2 + R_1) = 5R_2$$

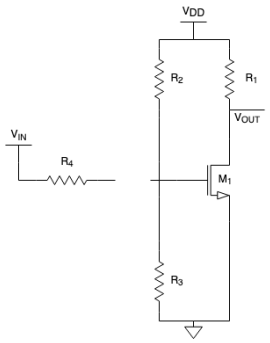
$$1.82R_1 = 3.18R_2$$

$$R_1 = 1.75R_2$$

Letting $R_2 = 10k\Omega$ means that R_1 is then equal to $17.5k\Omega$.

Solution 2

To begin, let us find V_{OUTQ}. To do so, draw the DC equivalent version of this circuit. Recall that, in DC, large inductors act as short-circuits and large capacitors act as open circuits.



We can find the voltage at the gate of M_1 by using the voltage divider equation:

$$V_{GS} = \frac{R_3}{R_3 + R_2} V_{DD} = \frac{10k}{10k + 17.5k} 5 = 1.82V$$

We can now find the current flowing through M_1, allowing us to find V_{OUTQ}:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \left(V_{GSQ} - V_T\right)^2 = [56.4\mu][5][1.82 - 0.79]^2 = 299\mu A$$

$$V_{OUTQ} = 5 - R_1 I_D = 2.01V$$

Solution 3

The capacitor will act as an open circuit. So:

Guessing FA:

$$V_{BE} = 0.7 \Rightarrow V_B = 0.7V \Rightarrow I_B = \frac{10 - 0.7}{150 * 10^3} = 0.062mA \Rightarrow I_C = 6.2mA \Rightarrow V_{out} = 10 - 6.2 * 1 = 3.8V$$

Since Vce >0.2V we confirm it is F.A

$$V_{out} = -g_m V_{BE} R_C = -g_m V_{in} R_C \Rightarrow \frac{V_{in}}{V_{out}} = A_V = -g_m R_C$$

$$A_V = -\frac{I_{CQ} R_C}{V_t} = -\frac{6.2 * 10^{-3} * 1 * 10^3}{0.026} = -238$$

So the output would be $0.75\sin(500t) * (-238) = -178.8\sin(500t)$

Solution 4

The capacitor will act as an open circuit. So:

Guessing Saturation:

$$I_{DQ} = \frac{1}{2}\mu Cox\frac{W}{L}(VGS - VT)^2 = 56.4 * 10^{-6}\frac{3}{0.6}(10 - 5 - 0.79)^2 = 5mA$$

$$\Rightarrow V_{out} = 10 - 0.1 * 5 = 9.5V$$

Since VDS = 9.5-5 > 10-5-0.79 we confirm it is Saturation

$$V_{out} = -g_m V_{BE} R_C = -g_m V_{in} R_C \Rightarrow \frac{V_{in}}{V_{out}} = A_V = -g_m R_C$$

$$A_V = -\frac{2I_{DQ}R_C}{V_{EB}} = -\frac{2 * 5 * 10^{-3} * 0.1 * 10^3}{5 - 0.79} = -0.2375$$

So the output would be $2\sin(500t) * (-0.2375) = -0.475\sin(500t)$

Solution 5

$$\frac{I_{CQ}R_C}{V_t} = \frac{2I_{DQ}R_C}{V_{EB}} \Rightarrow \frac{\beta I_{BQ}}{0.026}R_{C1} = R_{C2}\frac{2\frac{1}{2}\mu Cox\frac{W}{L}(VGS - VT)^2}{VGS - VT}$$

$$\Rightarrow \frac{100 * \frac{VDD_1 - 0.7}{100 * 10^3}}{0.026}R_{C1} = R_{C2}\frac{56.4 * 10^{-6}\frac{3}{0.6}(VDD_2 - 0.71)^2}{VDD_2 - 0.71}$$

$$\Rightarrow \frac{VDD_1 - 0.7}{26}R_{C1} = R_{C2} * 2.82 * 10^{-4}(VDD_2 - 0.71)$$

$$\Rightarrow \frac{VDD_1 - 0.7}{26}\frac{100}{5000 * 2.82 * 10^{-4}} + 0.71 = VDD_2$$

I will arbitrarily choose $VDD_1 = 1V$ for the BJT, and now I will check for saturation:

$V_{BE} = 0.7 \Rightarrow V_B = 0.7V \Rightarrow I_B = \frac{1-0.7}{100*10^3} = 0.003mA \Rightarrow I_C = 0.3mA \Rightarrow V_{out} = 3 - 0.3 * 10^{-3} * 100 = 2.97V$

$2.97 > 0.2V$ so we are in saturation.

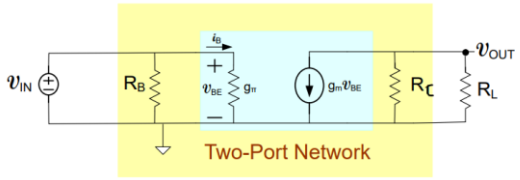
That means that VDD2 = 1.528V,

$$I_{DQ} = \frac{1}{2}\mu Cox\frac{W}{L}(VGS - VT)^2 = \frac{1}{2}56.4 * 10^{-6} * \frac{3}{0.6}(1.528 - 0.79)^2 = 0.077mA$$

$\Rightarrow V_{out} = 1.528 - 5 * 0.077 = 1.143V \Rightarrow VDS > VGS - VT$ so this is also in saturation

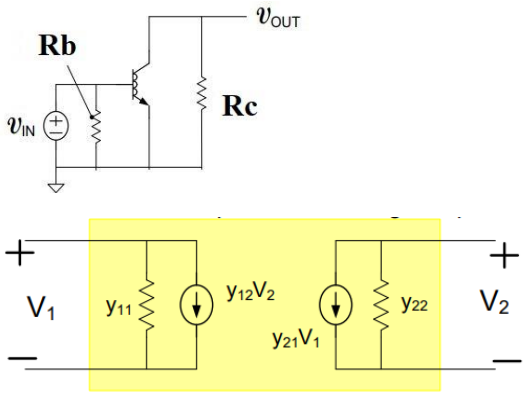
Since the BJT grows exponentially, it is clear that you need a lower Vdd to power the amplifier. Additionally, you need a much lower resistance in the BJT or higher in the MOS to get the amplifications to match.

Solution 6



The above is what the Thevenin equivalent would look like.

The quiescent circuit will look like this:



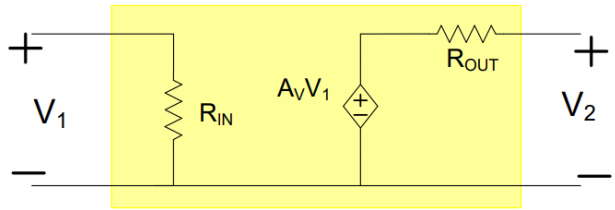
For the above two-port amplifier then I need to define y11,y12,y21 and y22 (keep in mind these are conductance not resistance terms). Which are clear from the first image:

<u>y22:</u> will be the value of 1/Rc since the output conductance of the BJT g_o is 0

<u>y11</u>: will be 1/Rb

<u>y12</u>: will be the BJT input conductance

<u>y21</u>: will be gm of the BJT



Now I need to find Rin, Rout and Av:

<u>Rin:</u> will be the parallel resistance of Rb and the input resistance of the BJT. The input resistance of the BJT is $\frac{I_{CQ}}{\beta V_t}$ and since Rb is many magnitudes of order larger than the BJT's input resistance, their parallel resistance can be rounded to just $\frac{I_{CQ}}{\beta V_t}$.

<u>Rout:</u> will just be R_c which is $\frac{1}{y22}$

Av: $A_v = -\frac{y_{21}}{y_{22}} = -\frac{gm}{\frac{1}{Rc}} = -g_m R_c$. The reason for this is, in the small signal amplifier circuit, y21 and y22 are in parallel, so the current going through the current source and that of y22 have to equal zero:

$$V_{out} * y_{22} + y_{21} * V_{in} = 0 \Rightarrow \frac{V_{in}}{V_{out}} = -\frac{y_{21}}{y_{22}}$$

Solution 7

For Amp1: its load is amp 2's input and its input resistance is Rs

$$Vout_1 = \frac{RL}{RL+Rout} A_V \frac{Rin}{Rs+Rin} Vin = \frac{100k}{100k+1} * 100 * \frac{\infty}{\infty+100k} * 5 = 500$$

Since we have an infinite input resistance, RS doesn't play a role. Also since the output resistance is low it doesn't affect the output noticeably. The output here will be 500V then.

For Amp2: its load is amp 3's input and its input resistance is amp1's outuput

$$Vout_2 = \frac{RL}{RL+Rout} A_V \frac{Rin}{Rs+Rin} V_{out1} = \frac{50k}{50k+500} * \frac{1}{200} * \frac{100k}{1+100k} * 500 = 2.475V$$

Since we have a relatively large input resistance, the previous chain's output resistance doesn't play a big role role. On the other hand since the output resistance is not very low it affect the output noticeably. The output here will be 2.457V then.

For Amp3: its load is RL and its input resistance is amp2's outuput

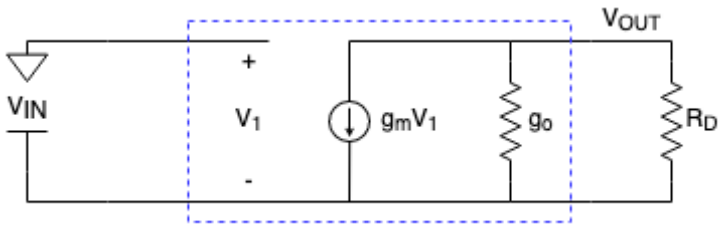
$$Vout_2 = \frac{RL}{RL+Rout} A_V \frac{Rin}{Rs+Rin} V_{out1} = \frac{5k}{5k+1k} * 2 * \frac{50k}{500+50k} * 2.475 = 4.084V$$

Since we have an even smaller input resistance from last time, the previous chain's output resistance plays a larger role on the output. Additionally to that, since the output resistance is very large, it affects the output very noticeably. The output here will be 4.084V then.

Ideally, we would multiply all the gains to get that of 1, meaning the ideal output would be 5V. 4.084 is noticeably different, mostly due to the high output resistance of amp2, and the high output resistance and low input resistance of amp 3.

Solution 8

To begin, draw the two-port model of the MOS device.



Now, using KCL, solve for V_{OUT}/V_{IN}:

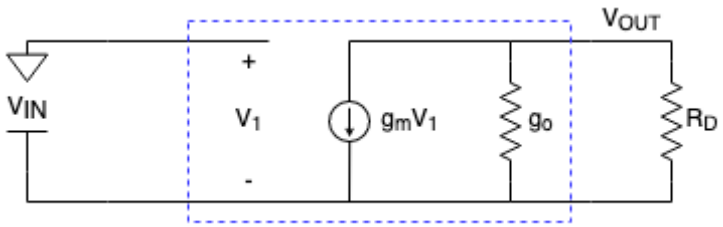
$$\frac{[V_{OUT} - V_{IN}]}{R_D} + g_m[-V_{IN}] + V_{OUT}[g_o] = 0$$

$$V_{OUT} - V_{IN} = V_{IN} g_m R_D - V_{OUT}[0] R_D$$

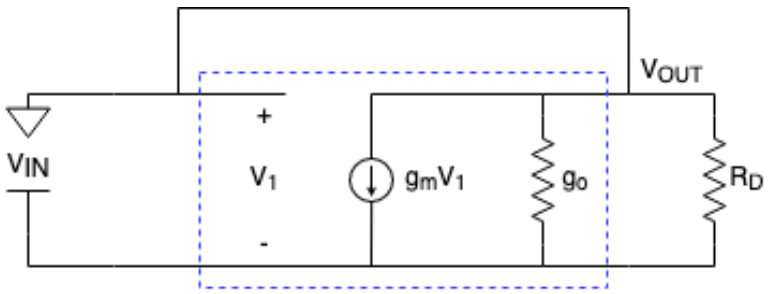
$$\frac{V_{OUT}}{V_{IN}} = [g_m R_D + 1] \approx g_m R_D$$

Solution 9

To begin, draw the two-port model of the MOS device.



To find the input-impedance, we terminate V_{OUT} to ground as a short circuit and apply a test voltage to the input. This results in a circuit which looks more like this:



Performing KCL:

$$I_{IN} = \frac{V_{IN}}{R_D} + V_{IN} g_o + g_m V_{IN}$$

$$\frac{I_{IN}}{V_{IN}} = \frac{1}{R_D} + 0 + g_m$$

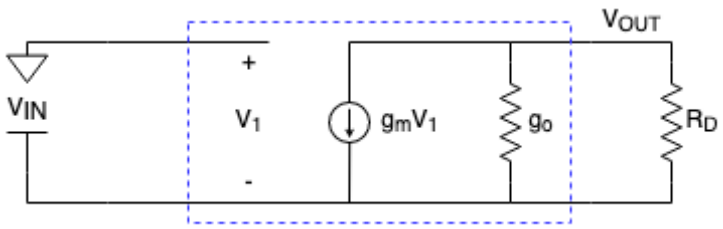
$$\frac{I_{IN}}{V_{IN}} = \frac{1 + g_m R_D}{R_D}$$

$$\frac{V_{IN}}{I_{IN}} = R_{IN} = \frac{R_D}{1 + g_m R_D}$$

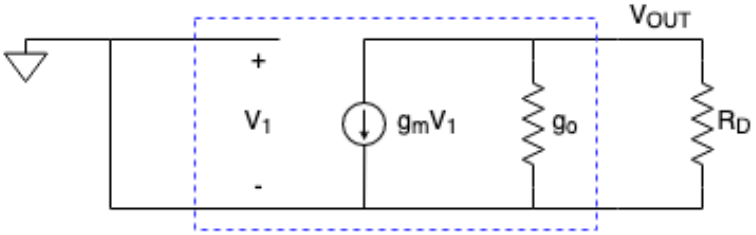
This solution is valid. We can make a further approximation, though, if we recall that $g_m R_D$ is the device gain. If the gain is much greater than 1, then $R_{IN} \approx \frac{1}{g_m}$.

Solution 10

To begin, draw the two-port model of the MOS device.



To find the output-impedance, we terminate V_{IN} to ground as a short circuit and apply a test voltage to the output. This results in a circuit which looks more like this:



Performing KCL:

$$I_{OUT} = \frac{V_{OUT}}{R_D} + V_{OUT} g_o + g_m V_{IN} = \frac{V_{OUT}}{R_D}$$

$$\frac{I_{OUT}}{V_{OUT}} = \frac{1}{R_D}$$

$$\frac{V_{OUT}}{I_{OUT}} = R_{OUT} = R_D$$

Solution 11 & 12

a)

Try forward active:

$$V_{out} = 5V - I_C * 2k\Omega$$

$$I_C = \beta * I_B = 100 * I_B$$

$$I_B = \frac{V_{in} - 0.6V}{25k\Omega}$$

V_{in}=1V	V_{in} = 1.5V	V_{in}=2V
$I_B = 16\mu A$	$I_B = 36\mu A$	$I_B = 56\mu A$
V_{out}=5-3.2=1.8V	V_{out}=5-7.2=**-2.2V**	V_{out}=5-11.2=**-6.2V**
Forward Active	Not Forward Active	Not Forward Active

Vin at 1V works in forward active, but it does not work in forward active for 1.5V and 2V.

Now to try saturation

V_{in}=1.5V	V_{in}=2V
$\beta I_B = 100 * \frac{1.5V - 0.7V}{25k\Omega} = 3.2mA$	$\beta I_B = 100 * \frac{2V - 0.7V}{25k\Omega} = 5.2mA$
$I_C = \frac{5V - 0.2V}{2k\Omega} = 2.4mA$	$I_C = \frac{5V - 0.2V}{2k\Omega} = 2.4mA$
$I_C < \beta I_B$	$I_C < \beta I_B$
Saturation	Saturation

b)

$$V_E = I_E * 1k\Omega = (I_C + I_B) * 1k\Omega = (\beta I_B + I_B) * 1k\Omega = 101k * I_B$$

$$I_B = \frac{V_{in} - (V_E + 0.6)}{25k\Omega}$$

$$I_B = \frac{V_{in} - 0.6 - 101k * I_B}{25k\Omega}$$

$$I_B = \frac{V_{in} - 0.6}{126k}$$

$$V_{out} = 5 - 100 * I_B * 2k$$

Vin=1V	V_{in}=1.5V	V_{in}=2V
V_{out}=4.37V	V_{out}=3.57	V_{out}=2.78V

c)

I_B, I_C, and I_E, are the same as part B still for BJT1.

$I1=I_{C1}+I_{B2}$

$$I1 = I_{C1} + I_{B2}$$

$$0 = 10 - I1 * 2k - I_{B2} * 200k - 0.6 = 10 - (I_{C1} + I_{B2}) * 2k - I_{B2} * 200k - 0.6$$

$$I_{B2} = \frac{10 - 2k * I_{C1} - 0.6}{502k}$$

Solve for I1 I_{B2}

$$Vout = 10V - 100 * I_{B2} * 2k\Omega$$

V_{in}=1V	V_{in}= 1.5V	V_{in}=2V
I_{C1}=0.3mA	I_{C1}= 0.7mA	I_{C1}=1.1mA
I_{B2}=17uA	I_{B2}=16uA	I_{B2}=14uA
V_{out}=6.5V	V_{out}=6.82V	V_{out}=7.14V

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							

angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON