EE 330

Homework 3

Fall 2020

Due Friday September 4

Problem 1

Draw the switch level equivalents of the NOT, NAND and NOR gates with the CMOS process. How can we make AND and OR gates with these?

Problem 2

An extremely important part of IC design is device modelling. Throughout this course, you will be introduced to a number of models for different devices, with each model increasing in complexity. Knowing a number of models, and being comfortable with each of them, is important for IC designers because choosing an overly simplified model may result in a faulty design but choosing an overly complicated model may result in many wasted hours of work. For example, if you are doing a basic back of the napkin design for a digital system, you probably do not need the square-law model of a MOSFET that you learned in EE 230 and will learn again in the coming weeks. However, if you are designing an op-amp, you should not use a switch-level model since it will fail to yield the information that you need.

So far, you have learned about two simple MOSFET models: the switch-level model and the improved switch-level model. Briefly explain the differences between these models. Why might you choose the switch-level model over the improved switch-level model? Why might you choose the improved switch-level model instead of the normal switch-level model?

Problem 3

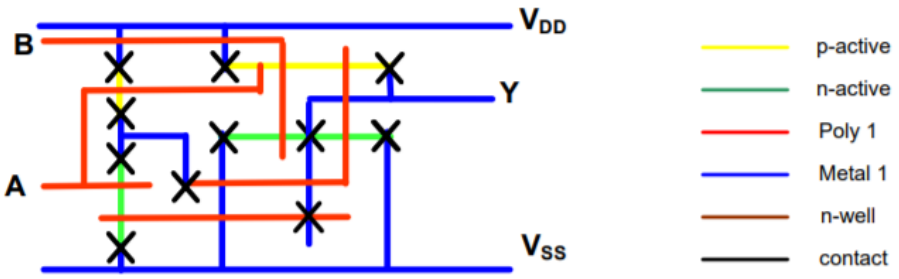
Assume a CMOS inverter designed in the ON 0.5µ CMOS process drives 6 identical inverter devices and the supply voltage is 5V. If a step input from 5V to 0V is applied at the input of the driving inverter, what is the LH output transition time? Assume minimum-sized devices are used and also assume VDD=5V.

Problem 4

Make a stick diagram for the function $F = A * B + \sim B * C$

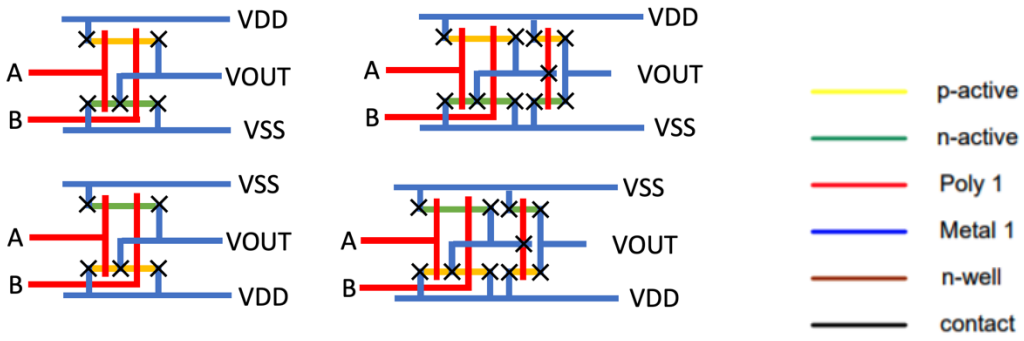
Problem 5

The stick diagram of a circuit is shown. Give a circuit schematic for this circuit. The color-code for the stick diagram is shown to the right.



Problem 6

Four stick diagrams and four logic expressions are given below. Match the logic function with the stick diagram that implements it. The color code for the stick diagram is also provided.



$VOUT = A * B$

$VOUT = A + B$

$VOUT = \overline{A + B}$

$VOUT = \overline{A * B}$

Problem 7

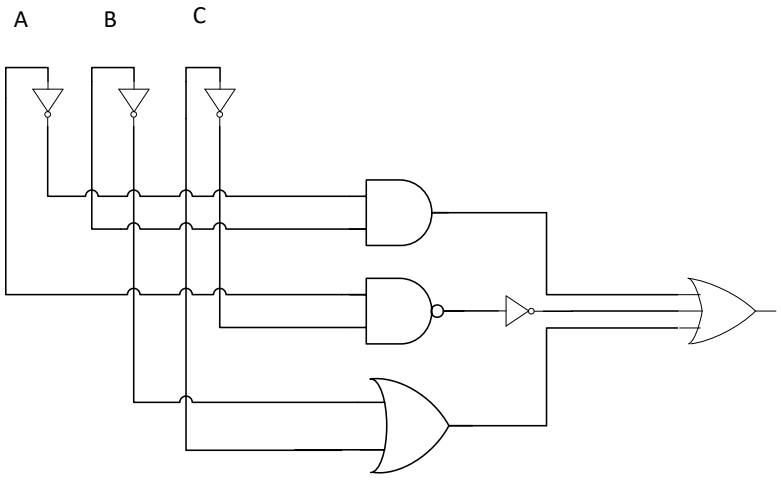
Using Complex Gates (instead of Static CMOS or Pass Transistor Logic), implement the following Boolean expression: $F = \overline{(A + B) * (C + D)}$. How many transistors does it take to implement this expression (without simplification) using Complex Gates? With Static CMOS? How many levels of logic are necessary for the Complex Gate implementation?

Problem 8

Draw the schematic for the Boolean expression $F = (A \oplus B) \cdot C$ using pass transistor logic. You have access to all inputs and their complements.

Problem 9

What is the expression for the following logic circuit? Can the expression be simplified? If so what is that expression?



Problem 10

Write the logic expression for a three-input XOR logic function using only NAND, NOR, and NOT functions. Then, create a circuit using logic gates (not transistors) to implement this function. Your circuit may use 3-input NAND and NOR gates; you are not restricted to 2-input gates.

Problem 11

The majority of the cost seen in the fabrication of integrated circuits comes from test, validation, and packaging costs. In theory, these costs could be significantly reduced by including more functionality in our integrated circuits; for example, instead of using a PCB to connect multiple individual ICs together on a motherboard, creating an entire integrated circuit which implements all of the functionality in one large chip. This would also reduce patristics and potentially improve circuit performance since bond wires and solder joints are significant sources of parasitic capacitance. This gives rise to the concept of "wafer scale integration," wherein an entire electrical system can be built at the IC level on a wafer of appropriate size. Provide at least one reason why this is not (currently) practical. Be quantitative.

Problem 12

If a die has a hard yield of 0.8 and an area of $1cm^2$, what is the defect rate of the wafer?