

EE330 Final Project Report

Digital Potentiometer & Programmable Amplifier

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Date: Apr 30th, 2021

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1 Introduction

In this project, we need to build a mixed-signal integrated circuit that will include inverting amplifier, non-inverting amplifier, digital to analog converter (DAC) and digital potentiometer. For all of the components will be programmable controlled by a four-bit input. Also, there is a two-bit control signal to decide which functionalities will be used for the output. There is a block high-level diagram given below. (Figure 1.1) From the block diagram, there are 3 major components in the project and they are the operational amplifier, the Multiplexer and the digital Potentiometer. By using the knowledge that we learned from the preview's labs and lectures, there are 4 major parts which are the Schematic, the Symbol, the Testbench and the Layout, we need to build. After creating the 4 major designing parts, the DRC and LVS check needs to be run.

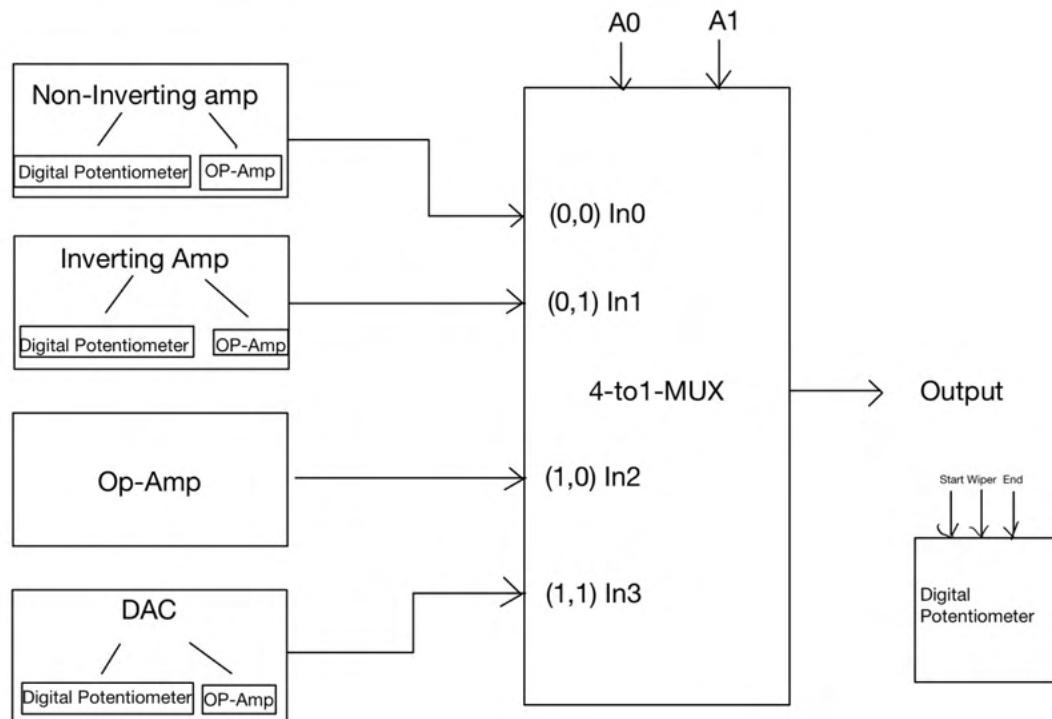


Figure 1.1: The Block Diagram

2. 4-to-1 Multiplexer

In order to meet the requirement of the project which is programmable, we need to create a 4 to 1 Multiplexer. To create the 4 to 1 Multiplexer we need Three 2 to 1 Multiplexer. There are two way to create it the first way is to use 3 NAND gate and 1 invertor which will use 14 transistors. The second way is to use the transmission gates which only use 6 transistors. We decided to use second way because there are more advantages such us cost less, less propagation delay, smaller layout. A 2-to-1 multiplexer can be implemented using transmission gates. Figure 2.1 below shows the connection diagram of the 2-to-1 multiplexer using transmission gates. The 2-to-1 MUX selects either A or B depending upon the control signal C. This is equivalent to implementing the Boolean function, $F = (A \cdot C + B \cdot \bar{C})$ When the control signal C is high then the upper transmission gate is ON and it passes A through it so that output = A. When the control signal C is low then the upper transmission gate turns OFF and it will not allow A to pass through it, at the same time the lower transmission gate is 'ON' and it allows B to pass through it so the output = B.

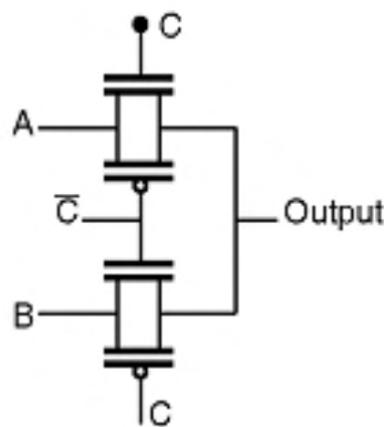


Figure 2.1 : The 2-to1 MUX using transmission gates

Then we created the schematics in Cadence by using 2 PMOS, 2 NMOS and an inverter which is created in the previous lab. (Figure 2.2)

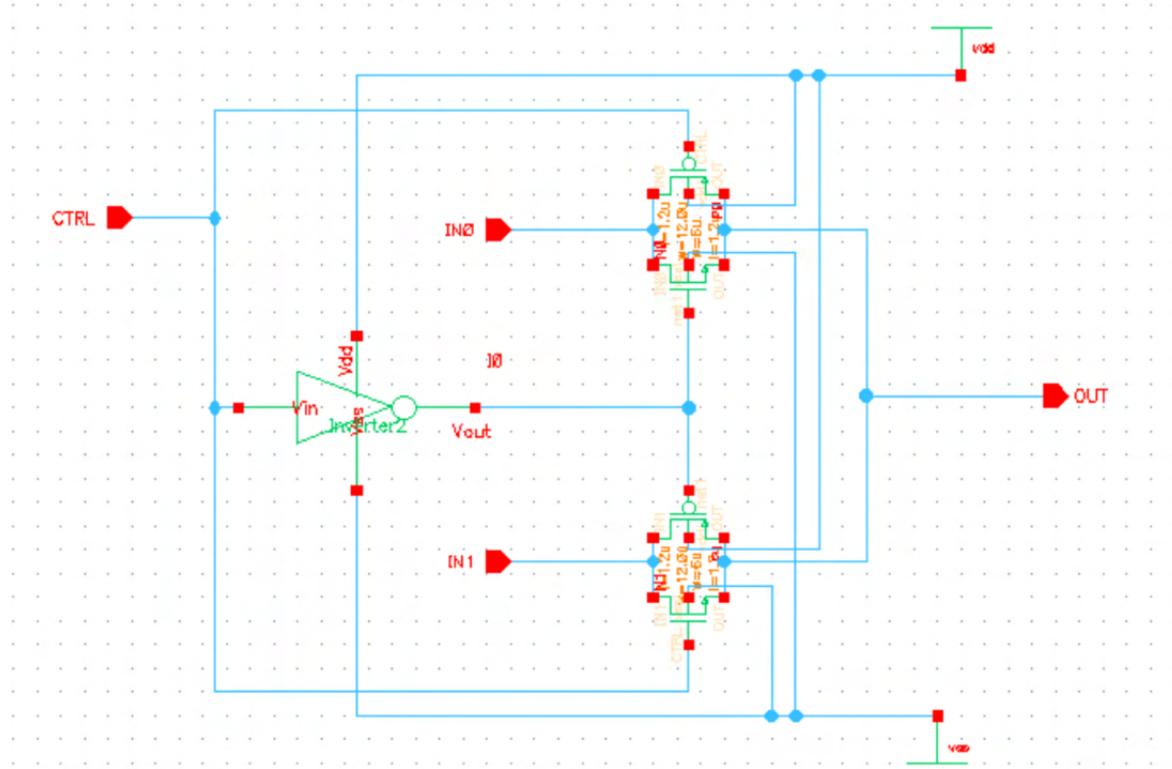


Figure 2.2: 2 to 1 MUX schematic

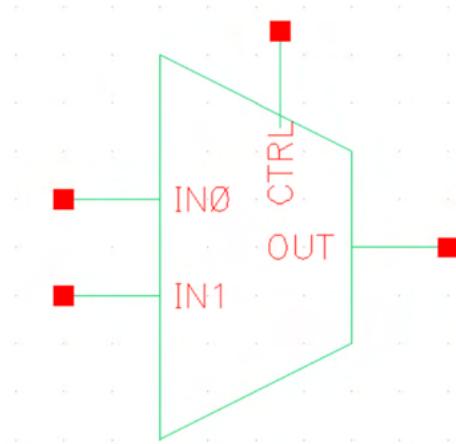


Figure 2.3: 2 to 1 MUX Symbol

After creating the 2 to 1 Multiplexer, we need to create the 4 to 1 Multiplexer. For this project we have two control signals A0 and A1, so we can get the table below.

A0	A1	Output
0	0	In0
0	1	In1
1	0	In2
1	1	In3

Then we can create the schematic of the 4 to 1 Multiplexer by using Three 2 to 1 Multiplexer. (Figure 2.4) Also we can create the symbol of the 4 to 1 Multiplexer. (Figure 2.5)

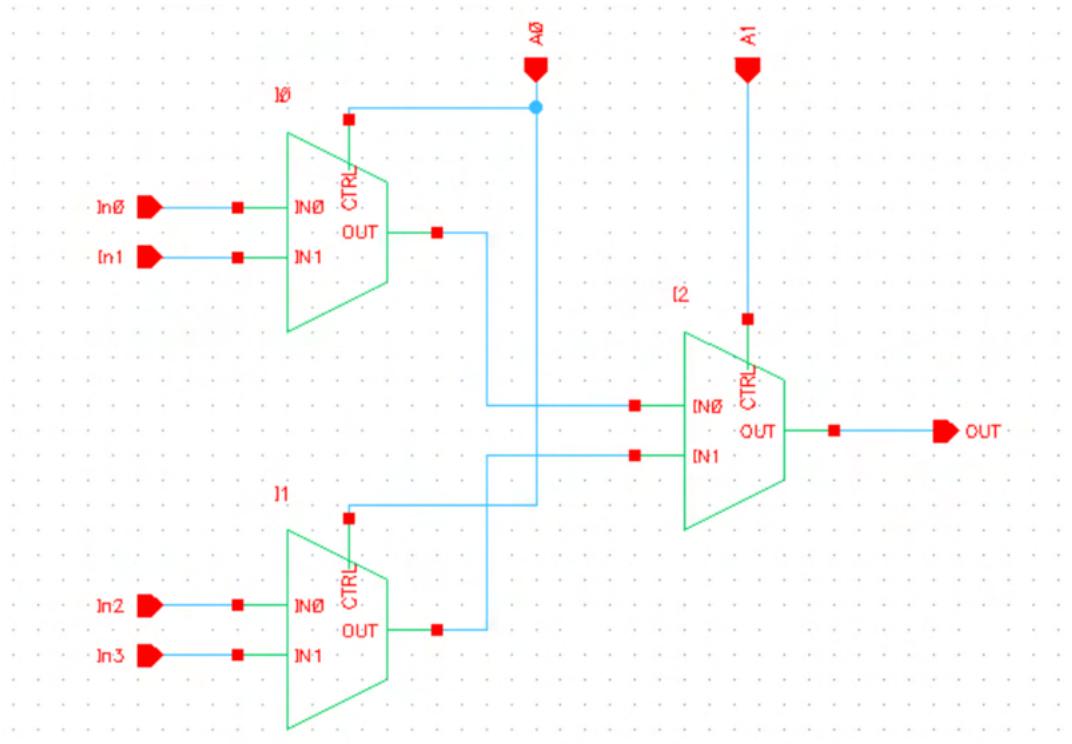


Figure 2.4: The 4-to-1 MUX Schematic

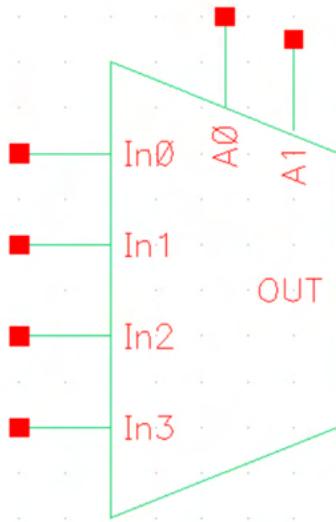


Figure 2.5: The 4-to-1 MUX Symbol

After creating all the components above, we need to build a test bench to see how our design work with DC and AC inputs. In Figure 2.6 below, this is the test bench we created. We have In0 with DC 1V, In1 with DC -1V, In2 with sine wave AC 1Vpk and In3 with sine wave AC 0.5Vpk.

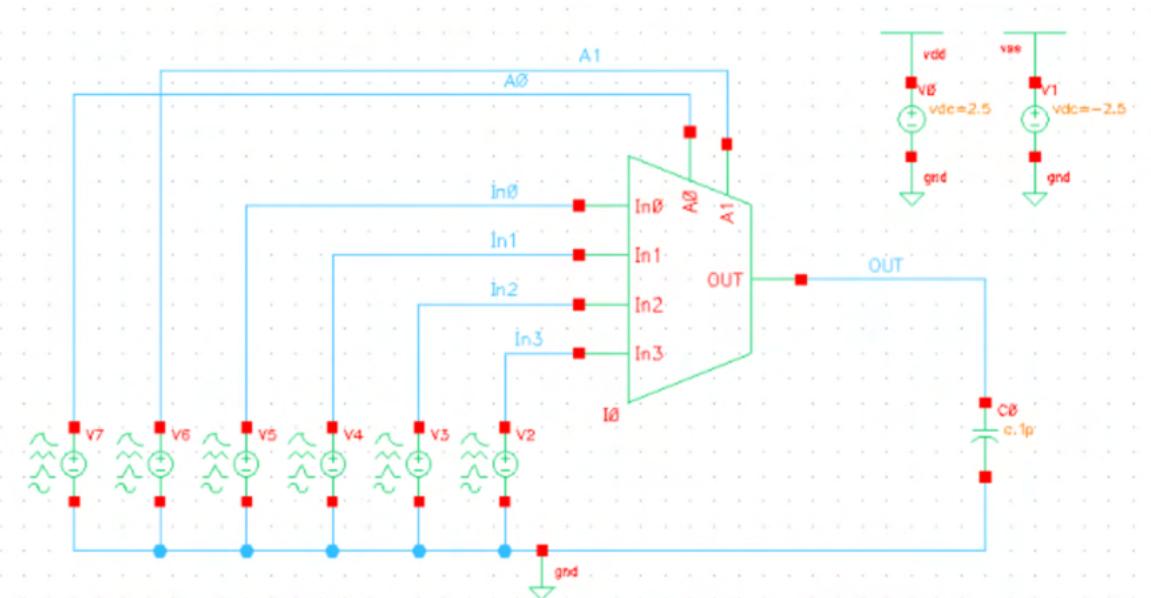


Figure 2.6: The Schematic of the 4-to-1 MUX Test Bench

After getting the simulation results (Figure 2.7), we found the result match our expected. Then we created the layout of the 4-to-1 MUX which is consisted by 3 2to1 MUX.

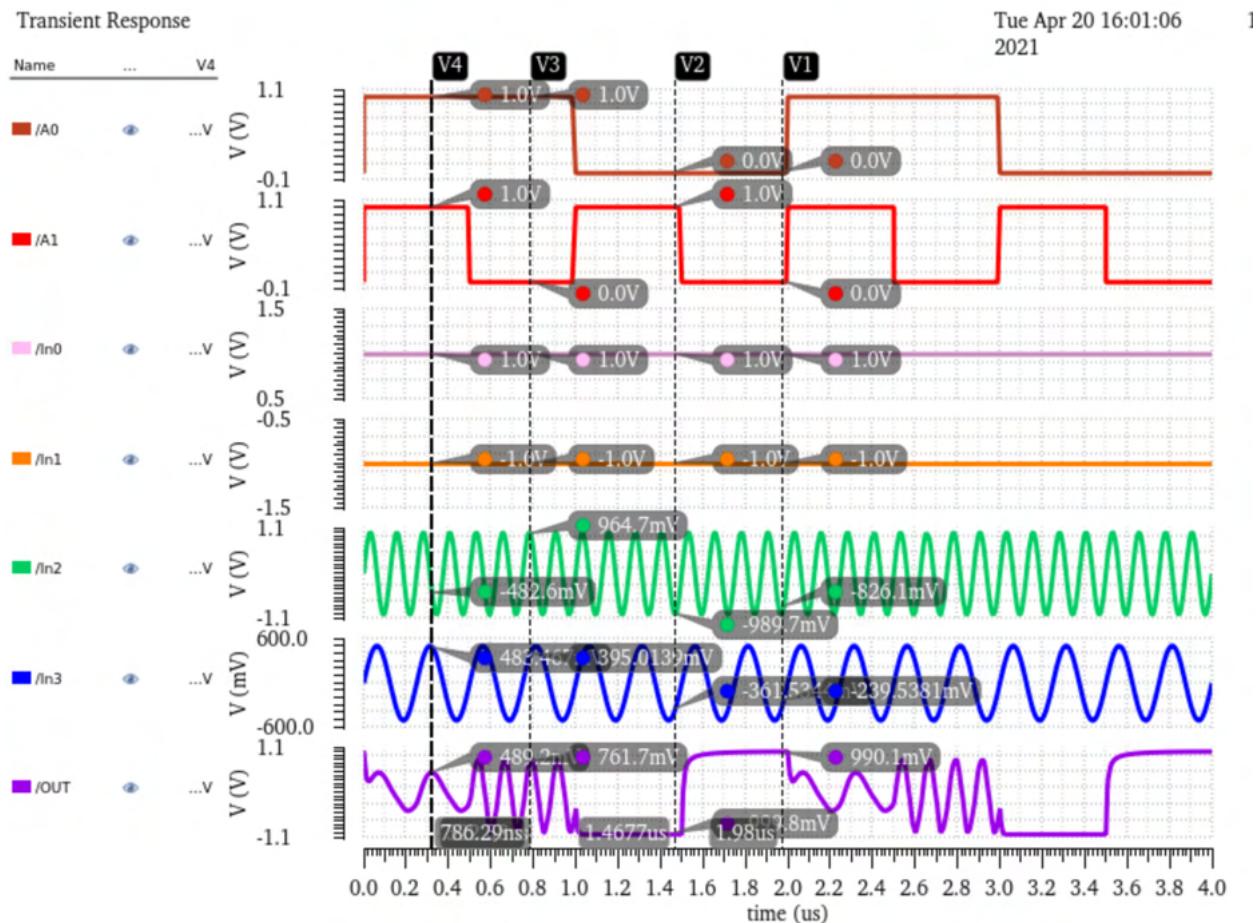


Figure 2.7: The Test Bench Test Result of 4-to-1 MUX

Then we created the layout for the 2-to-1 MUX and the 4-to-1 MUX. (Figure 2.8 and Figure 2.9) Then we passed the DRC and LVS check which is in the Appendix.

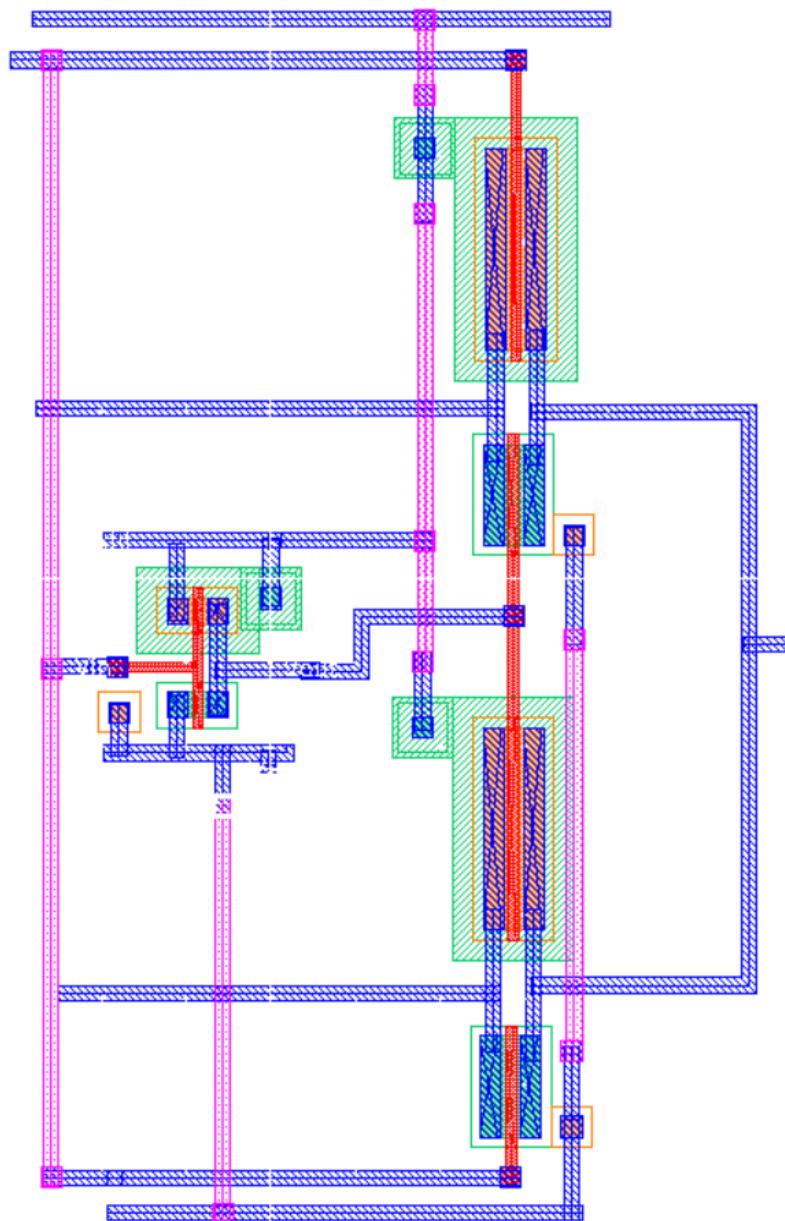


Figure 2.8: The layout of the 2-to-1 MUX

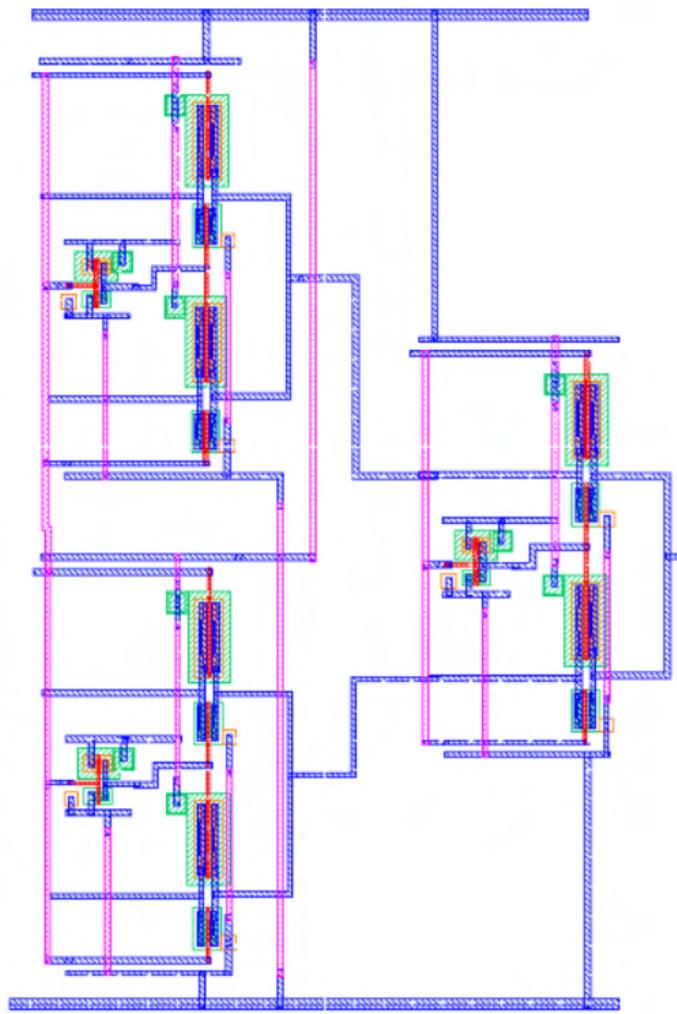


Figure 2.9: The layout of the 4-to-1 MUX

3 Digital Potentiometer

A digital potentiometer (also known as digital resistor) has the same function as a normal potentiometer but instead of mechanical action it uses digital signals and switches. This is done by making use of a 'resistor ladder', a string of small resistors in series. At every step of the ladder, an electronic switch is present. Only

one switch is closed at the same time and in this way the closed switch determines the 'wiper' position and the resistance ratio. The amount of steps in the ladder

determines the resolution of the digital pot. The Figure 3 below shows the working principle of a digital potentiometer with 64 steps.

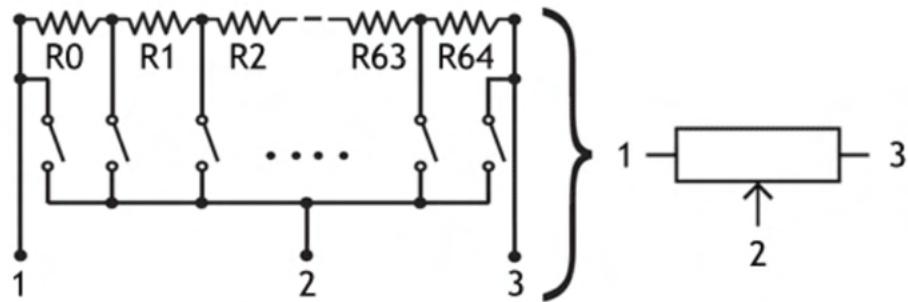


Figure 3: The Digital Potentiometer

To make the digital potentiometer for this project we need to use three components switch (transmission gate), resistors and decoder. In this project we used 16 transmission gates and 15 resistors to create the digital potentiometer. The reason to use 16 transmission gates and 15 resistors, it is because that can make our life easier.

3.1 Transmission Gate

In order to build a Potentiometer, the first component we need to create is the Transmission Gates which will act as a switch to vary the resistance. A transmission gate (TG) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. In principle, a transmission gate is made up of two field-effect transistors, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal

(bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET, are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a Inverter, to form the control terminal. (Figure 3.1.1) When the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off. The reason to use this circuit it is because it allows the output to be able to range from VDD to VSS without any loss. When we use a single NMOS, the output cannot reach VDD (The Gate to Source voltage cannot reach the value to turn on the device. However, the PMOS can provide enough Gate to Source voltage and the output will reach the VDD. The inverse would happen when endeavoring to arrive at VSS in this manner permitting a full yield voltage swing.

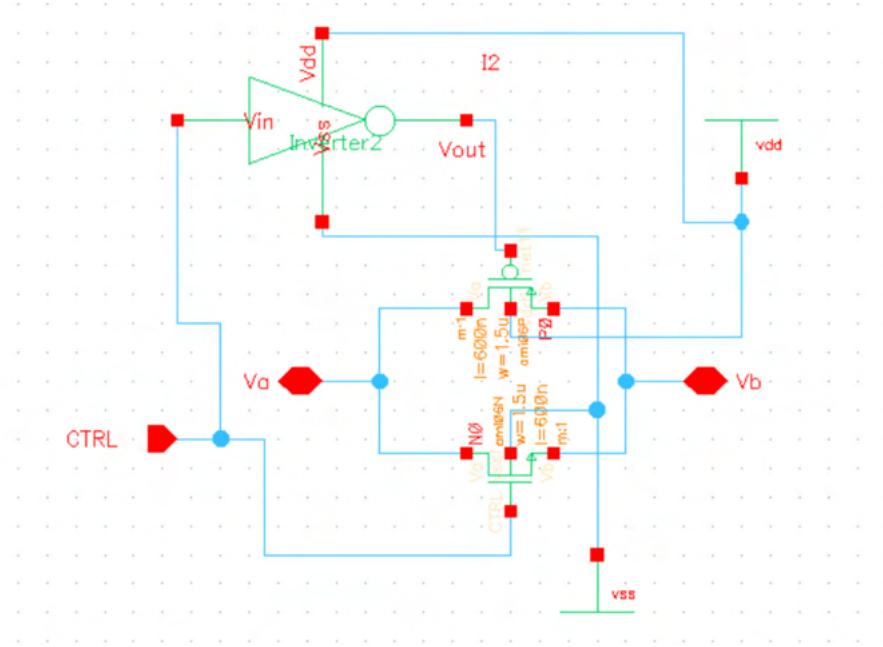


Figure 3.1.1: The Schematic of the Transmission Gate

In order to do make the test bench we need to create a symbol for the Transmission Gate (Figure 3.1.2). Then the testbench was built to simulate the behavior of the component. (Figure 3.1.3) Other than two Vsourse for the control and contribution of the transmission gate, two DC sources were additionally associated with VDD and VSS nets to supply the voltages to the bulk of the PMOS and NMOS. Also, a 1pF capacitor was set at the output.

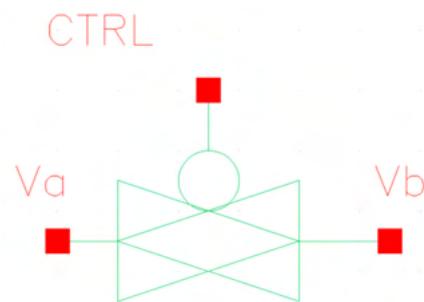


Figure 3.1.2: The Schematic of The Transmission Gate

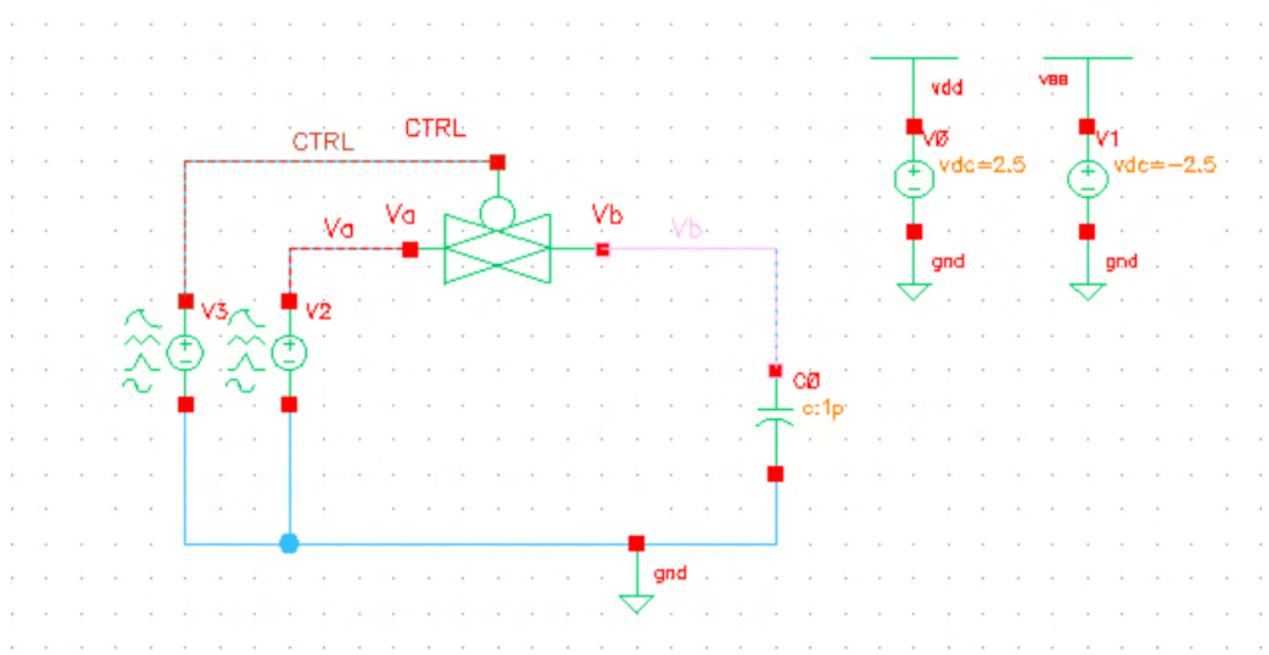


Figure 3.1.3: The Testbench of The Transmission Gate

The simulation result of the Transmission Gate is given below (Figure 3.1.4). We set low and high input for the control and a sine wave for the input. Form the transient response we can find that when the Control is low the gates will shut down and prevent voltage outputting. When the control is high, the gates will turn on and the voltage will go through from input to output with the same value. The simulates result shows that the circuit met our design propose. Then the layout of this device was created (Figure 3.1.5). The DRC and LVS test of the design will be in the Appendix.

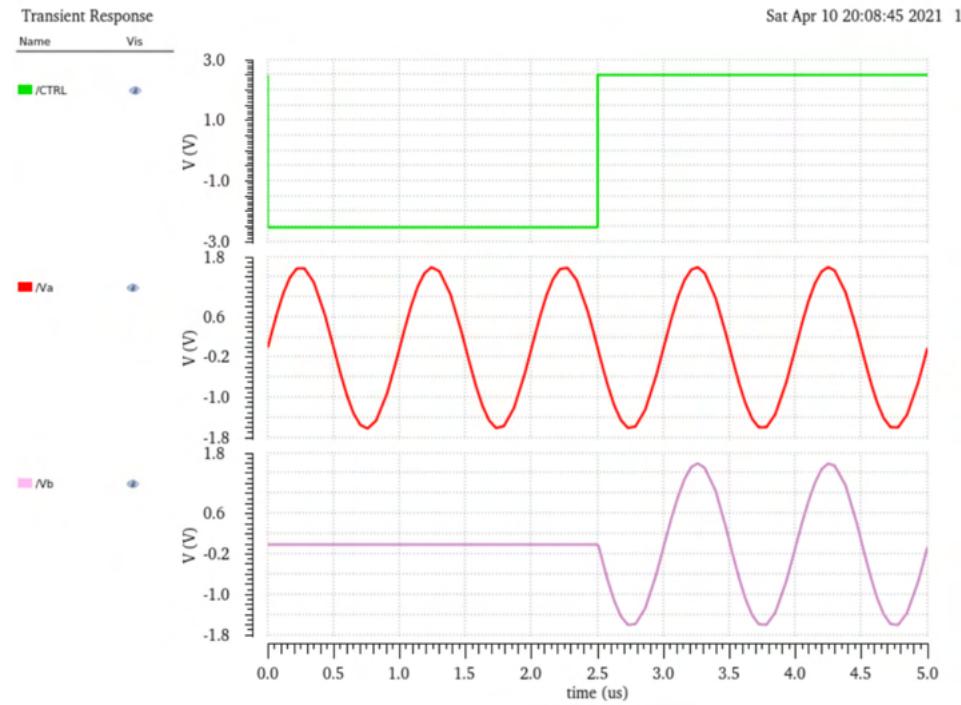


Figure 3.1.4: The Simulation result of The Transmission Gate

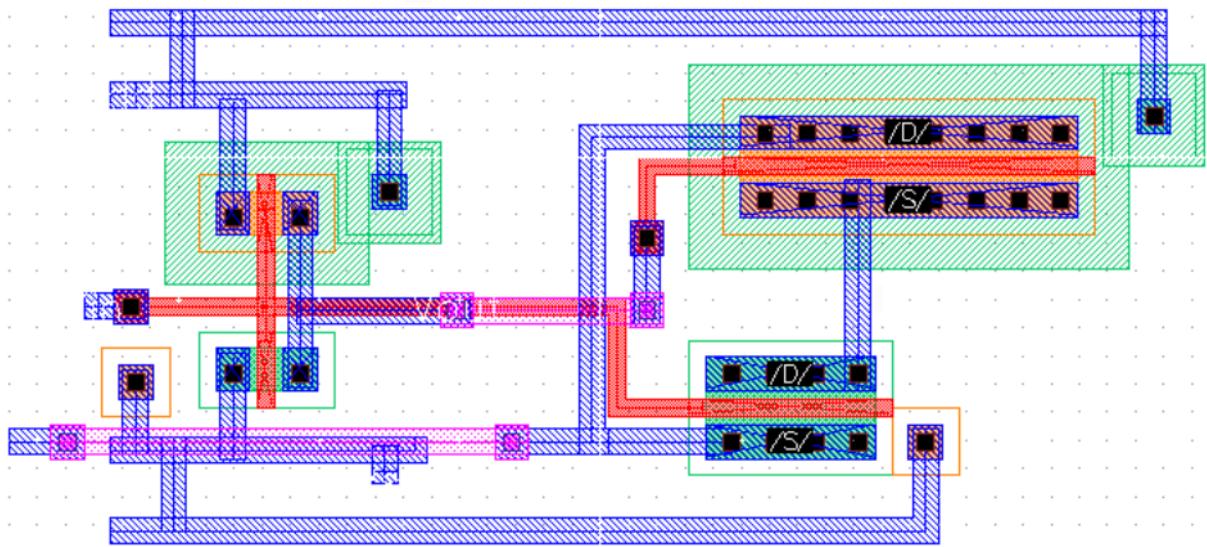
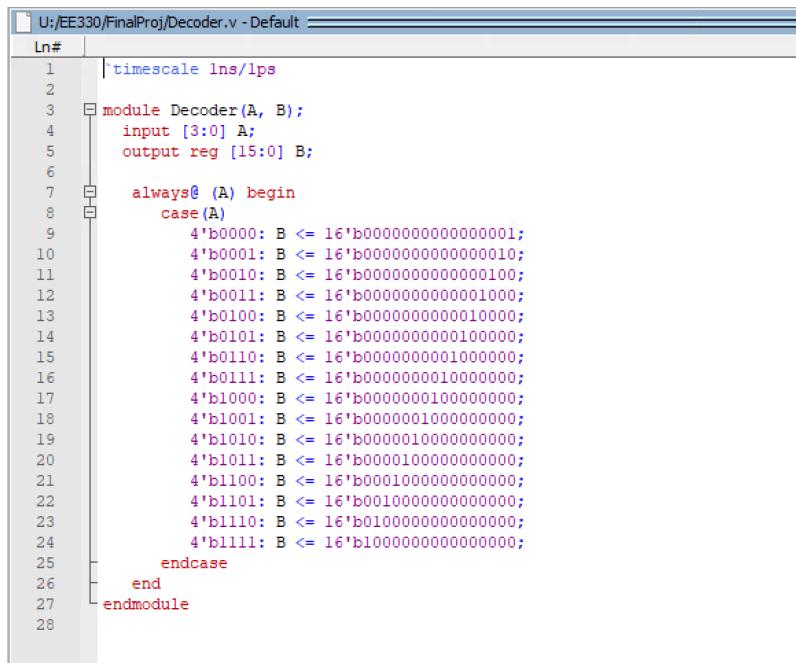


Figure 3.1.5: The layout of the transmission gate

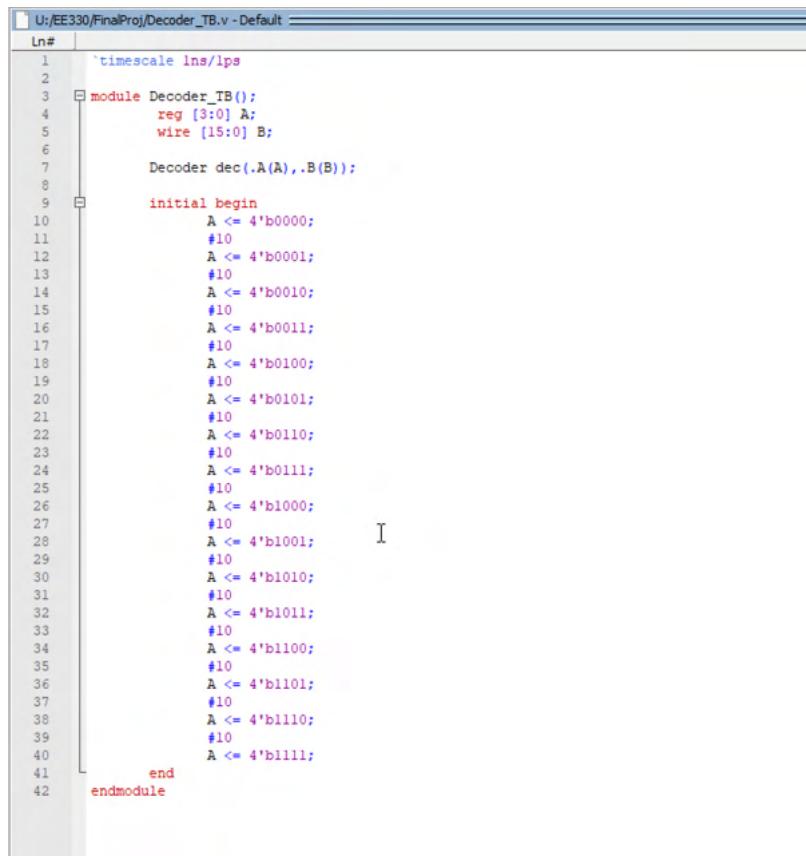
3.2 Decoder

Other than the transmission gate, a decoder is a required component for the Digital Potentiometer design. In order to control 16 Transmission Gates with a four-bit control signal, a 4 to 16 decoder need to be built. Because this is a complex logic component, it is time consuming to use PMOS and NMOS directly to create them. As a result in this project Modelsim with the Verilog code was used to create the component. By creating the Verilog with right syntax we can get the code below (Figure 3.2.1) and the testbench code which is the combinations of four bits were used as input, A, and the output will be observed at B (Figure 3.2.2)



```
U:/EE330/FinalProj/Decoder.v - Default
Ln# | timescale 1ns/1ps
1  | module Decoder(A, B);
2  |   input [3:0] A;
3  |   output reg [15:0] B;
4  | 
5  |   always@ (A) begin
6  |     case (A)
7  |       4'b0000: B <= 16'b0000000000000001;
8  |       4'b0001: B <= 16'b0000000000000010;
9  |       4'b0010: B <= 16'b00000000000000100;
10 |       4'b0011: B <= 16'b000000000000001000;
11 |       4'b0100: B <= 16'b00000000000010000;
12 |       4'b0101: B <= 16'b000000000000100000;
13 |       4'b0110: B <= 16'b0000000000001000000;
14 |       4'b0111: B <= 16'b00000000000010000000;
15 |       4'b1000: B <= 16'b00000000100000000;
16 |       4'b1001: B <= 16'b000000010000000000;
17 |       4'b1010: B <= 16'b0000001000000000000;
18 |       4'b1011: B <= 16'b00000100000000000000;
19 |       4'b1100: B <= 16'b000100000000000000000;
20 |       4'b1101: B <= 16'b0100000000000000000000;
21 |       4'b1110: B <= 16'b10000000000000000000000;
22 |       4'b1111: B <= 16'b100000000000000000000000;
23 |     endcase
24 |   end
25 | endmodule
```

Figure 3.2.1: The Verilog code of the 4 to 16 Decoder



```
U:/EE330/FinalProj/Decoder_TB.v - Default
Ln# | 1   `timescale 1ns/1ps
 2
 3   module Decoder_TB();
 4     reg [3:0] A;
 5     wire [15:0] B;
 6
 7     Decoder dec(.A(A), .B(B));
 8
 9     initial begin
10       A <= 4'b0000;
11       #10
12       A <= 4'b0001;
13       #10
14       A <= 4'b0010;
15       #10
16       A <= 4'b0011;
17       #10
18       A <= 4'b0100;
19       #10
20       A <= 4'b0101;
21       #10
22       A <= 4'b0110;
23       #10
24       A <= 4'b0111;
25       #10
26       A <= 4'b1000;
27       #10
28       A <= 4'b1001;
29       #10
30       A <= 4'b1010;
31       #10
32       A <= 4'b1011;
33       #10
34       A <= 4'b1100;
35       #10
36       A <= 4'b1101;
37       #10
38       A <= 4'b1110;
39       #10
40       A <= 4'b1111;
41     end
42   endmodule
```

Figure 3.2.2: The Testbench cod of the 4 to 16 Decoder

Then the result of the simulation is given below (Figure 3.2.3). By comparing the result with the truth table, we can find that the code is working as we expected. For the next step, the Verilog code will have both its circuit and layout automatically created for us through using Genus and Innovus. The optimized schematic can be observed in Figure 3.2.4 and the layout can be viewed in Figure 3.2.5. Connectivity and geometry tests for the layout have also been conducted which it has passed and will be set in the Appendix along with its DRC and LVS.

W	X	Y	Z	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

The Truth Table of the Decoder

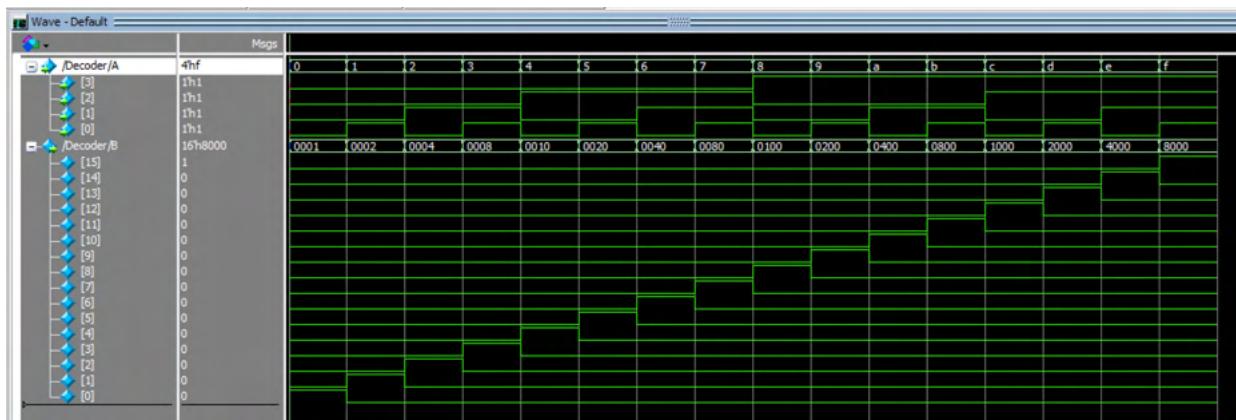


Figure 3.2.3: The Simulation result of the 4 to 16 Decoder

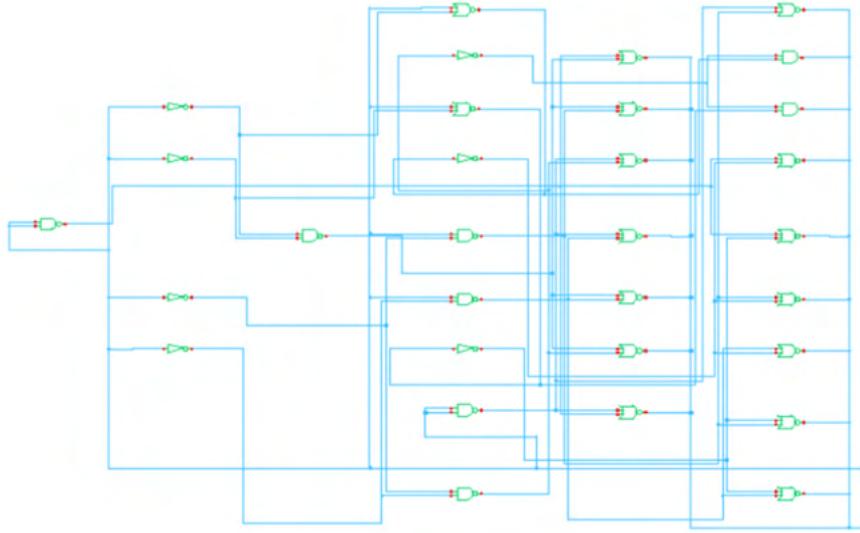


Figure 3.2.4: Optimized decoder circuit

In order the Decoder can work in Cadence, the testbench schematic was created below(Figure 3.2.6). Because this is a 4 to 16 decoder, there are 4 input and 16 output. As a result we need 4 Vpulse and 16 capacitor in the schematic. By labeling each input and output we can obtain the Vpulse wave similar with the result which we obtained from the ModelSim. (Figure 3.2.7, Figure 3.2.8 and Figure 3.2.9) From the result of the simulation we can find, this device worked as we expected.

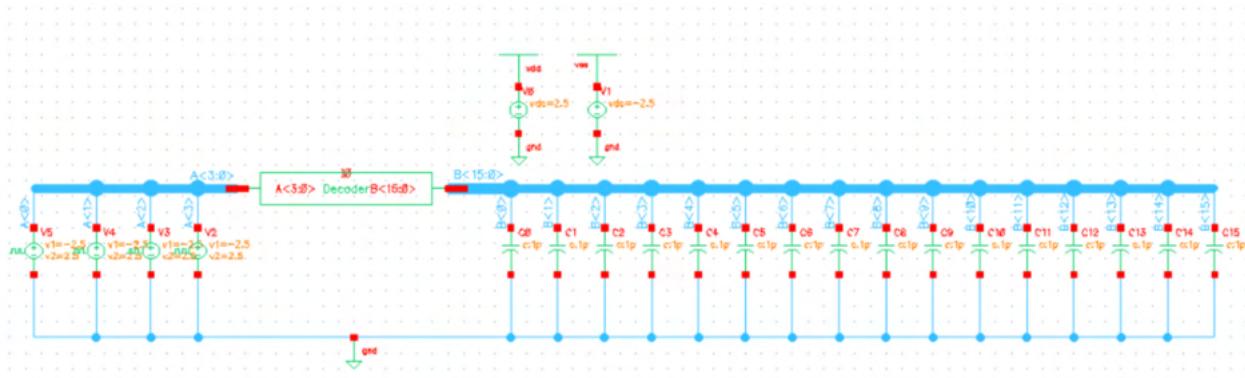


Figure 3.2.6: The Schematic of the Decoder Testbench

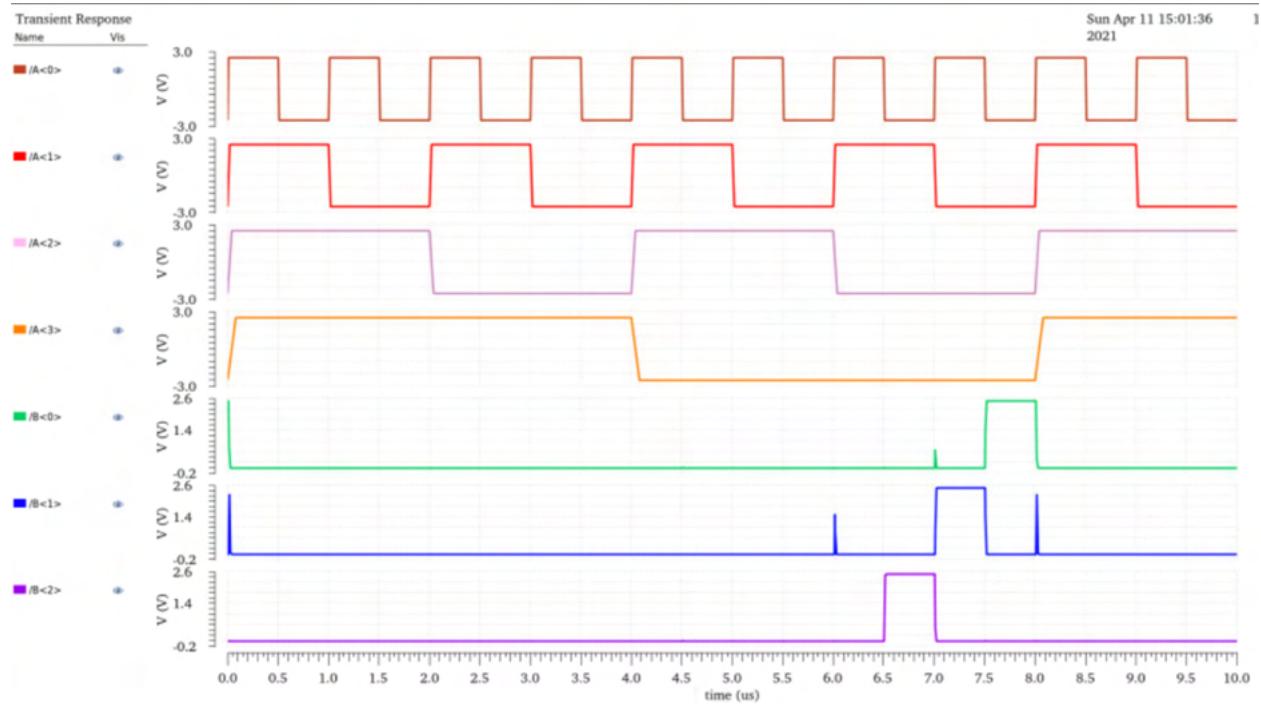


Figure 3.2.7: The Simulation Result of the Decoder



Figure 3.2.8: The Simulation Result of the Decoder

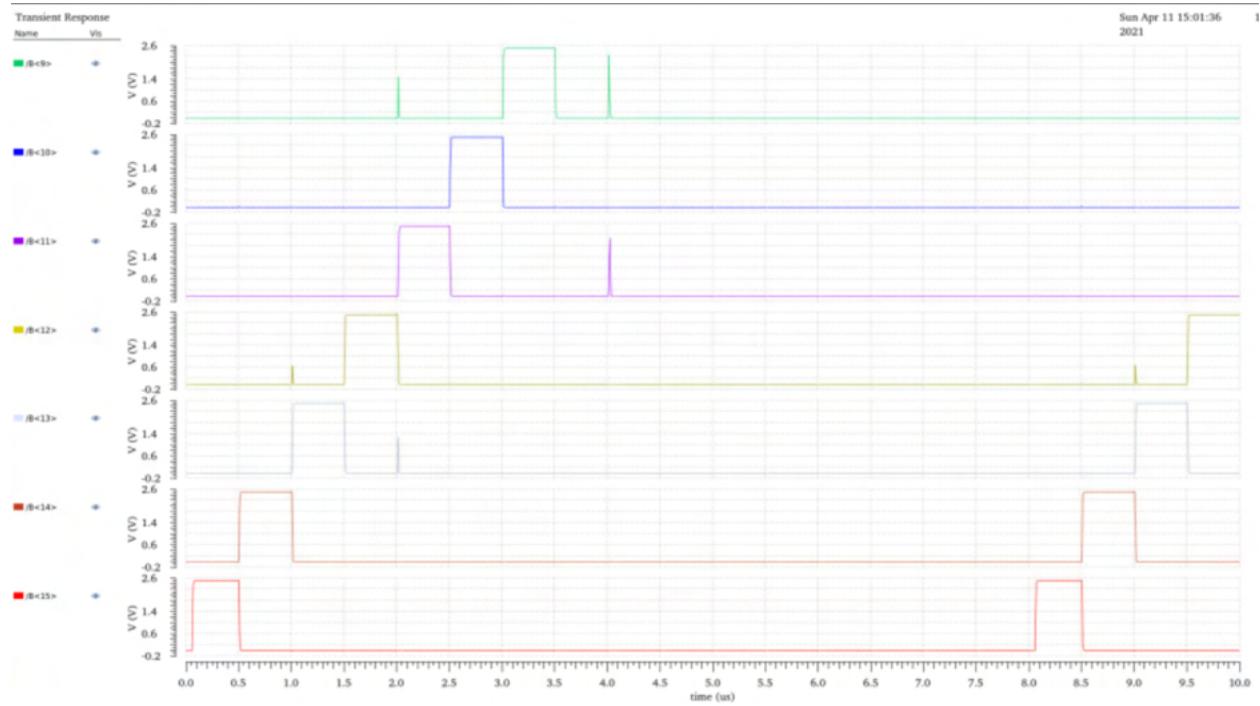


Figure 3.2.9: The Simulation Result of the Decoder

Then the layout is built (Figure 3.2.10) and we passed the DRC and LVS check which will show in the Appendix.

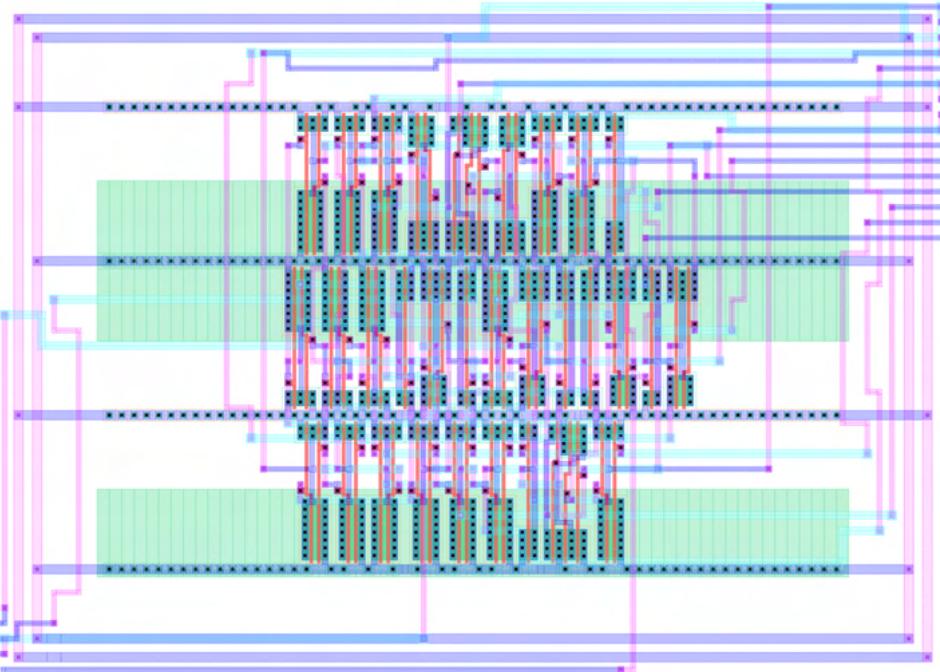


Figure 3.2.10: The Layout of the 4 to 16 decoder

3.3 Resistor

Resistor is a key component for the Digital Potentiometer. In order to keep the calculation as simple as possible, $5\text{k}\Omega$ resistors will be used in this project. By looking at the AMI06 process datasheet, the sheet resistance of ploy can be found($23.5\Omega / \text{square}$). After the calculation below, the number of squares can be found.

$$R = R_s N_s, R = 5\text{k}\Omega, R_s = 23.5\Omega/\text{square}$$

$$N_s = 212.77 \text{ squares}$$

Because the width of the minimum sized is 0.6um , the length will be 127.67um . Then we can get the layout and the Extracted view of the resistor below.(Figure 3.3.1)



Figure 3.3.1: The Extracted view of the Resistor

3.4 The Digital potentiometer

By creating all the requirement component of the Digital Potentiometer, the final step is to put them together. The 16 outputs of the decoder connected to the control of each transmission gate to control the it on or off. Also, the resistors was placed between each transmission gate. This is because the P1 to P2 is the sum of the resistance. For example, when the digital input is 0001 the 2ed transmission gate will close the resistance of this state will be $5\text{k}\Omega$. Moreover, we have a P3 which is the max resistance ($15*5\text{k}\Omega = 75\text{k}\Omega$) of the Digital Potentiometer. Then the

schematic design of the Digital Potentiometer is created at below (Figure 3.4.1). By some of the research we can find the symbol of the Digital Potentiometer P1 is the Vin P2 is the wiper and P3 connect to ground. (Figure 3.4.2)

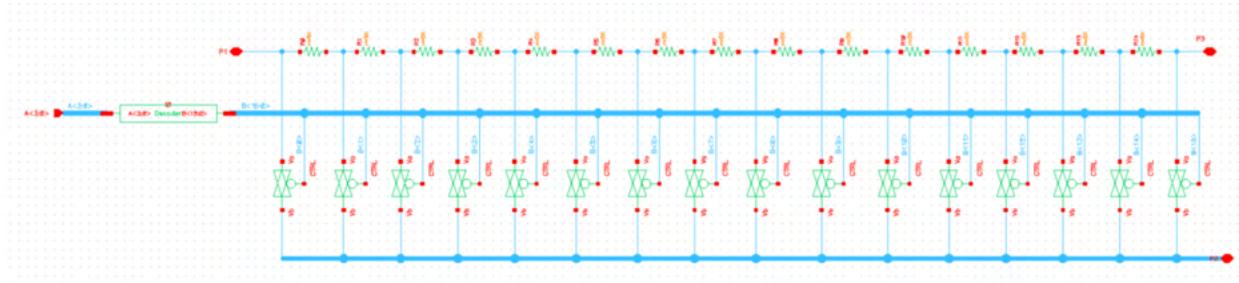


Figure 3.4.1: The Schematic of the

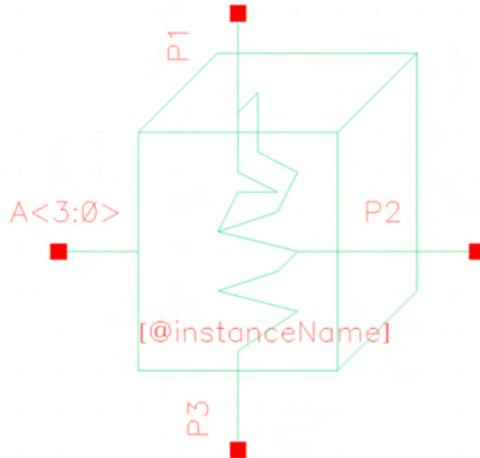


Figure 3.4.2: The Symbol of the Potentiometer

Then the testbench is created for the Potentiometer. By connecting the 4-signal input to the Vpulse its can generate the 0000,0001.....1111. Also, P1 connect to the Vin that have a constant 2V, P2 connect to Vout and P3 connect to the ground. (Figure 3.4.3)

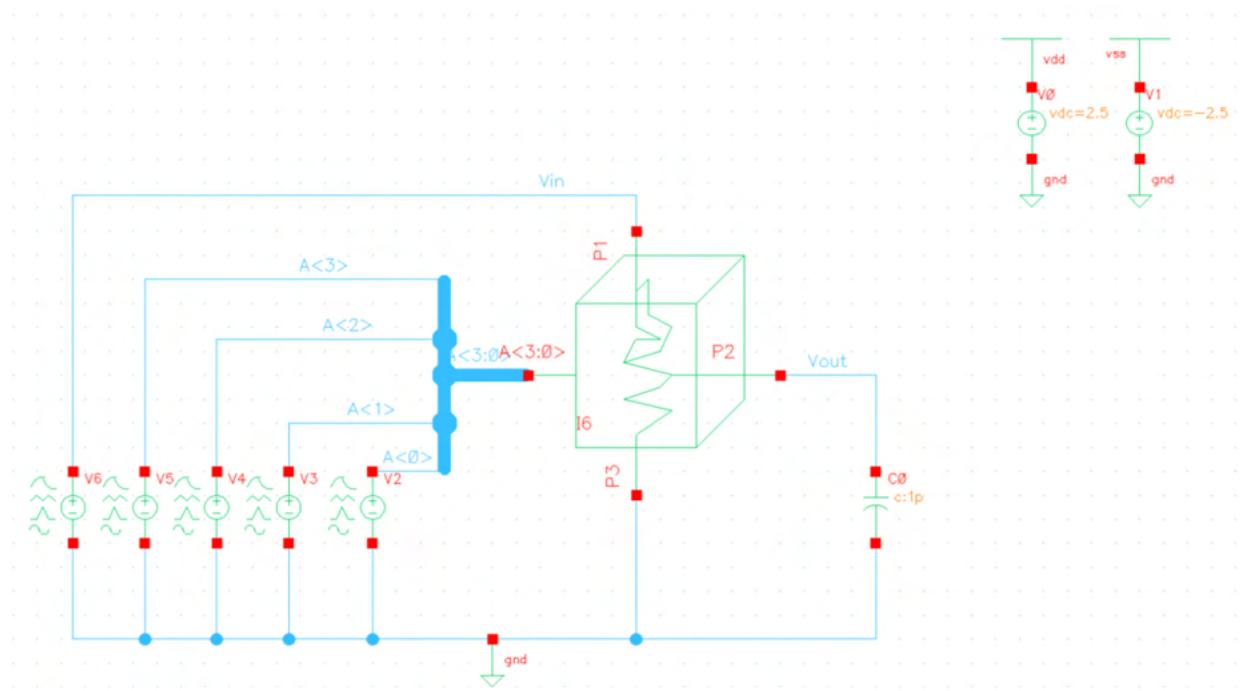


Figure 3.4.3: The Testbench of the Potentiometer

From the simulation result, we can see the output voltage is correct divided out. The ratio starts from 0, 1/15, 2/15, 3/15, 4/15...14/15, to 1. Because we have a 2.5V constant Vin so by measuring the Vout, we could proof if the design is correct. By comparing with the Table and the Simulation result below (Figure 3.4.4), it is proofed that the design is correct. Then the layout was then made which can be seen in Figure 3.4.5 which has passed both DRC and the LVS test (Appendix).

0	1/15	2/15	3/15	4/15	5/15	6/15	7/15	8/15	9/15	10/15	11/15	12/15	13/15	14/15	1
0	0.16	0.33	0.5	0.66	0.83	1	1.16	1.33	1.5	1.66	1.83	2	2.16	2.33	2.5

Table of the Voltage Output for each stage

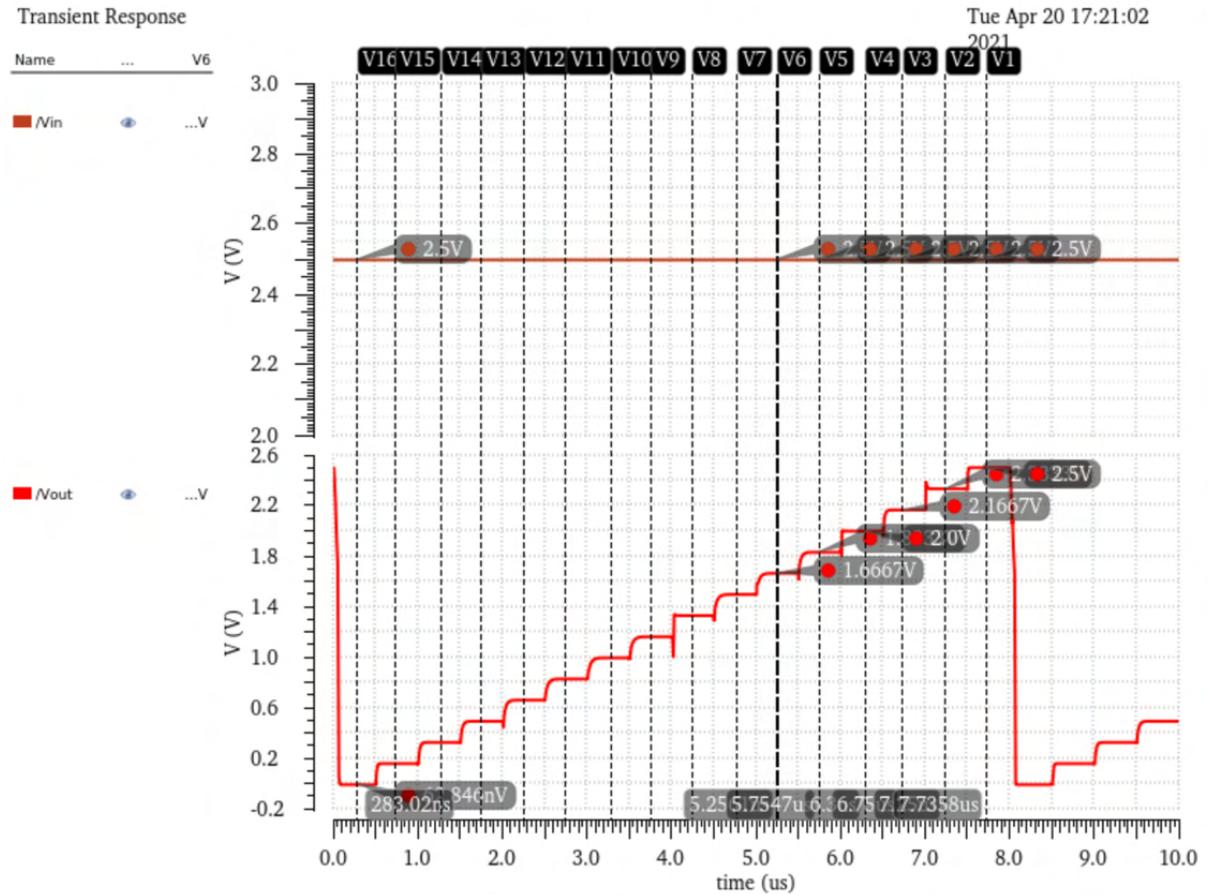


Figure 3.4.4: The Simulation result of the Potentiometer

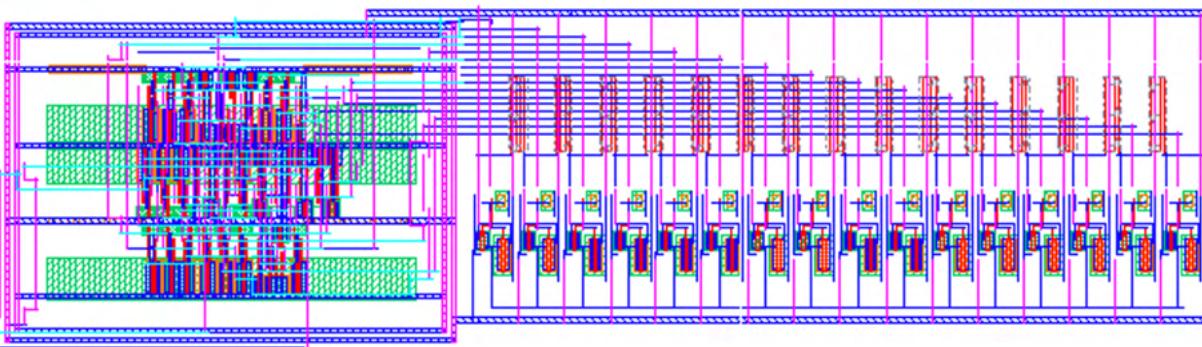


Figure 3.4.5 The Layout of the Digital Potentiometer

4 Operational Amplifier

To meet the project requirement another component is the operational amplifier that is significant for many of these functionalities as it will act as an amplifier and a buffer. The design of the operational amplifier is based on the two-stage design with external compensation which was done with the guidance from Douglas Zuercher's manual. The design of the OP-amp is given below. (Figure 4.1)

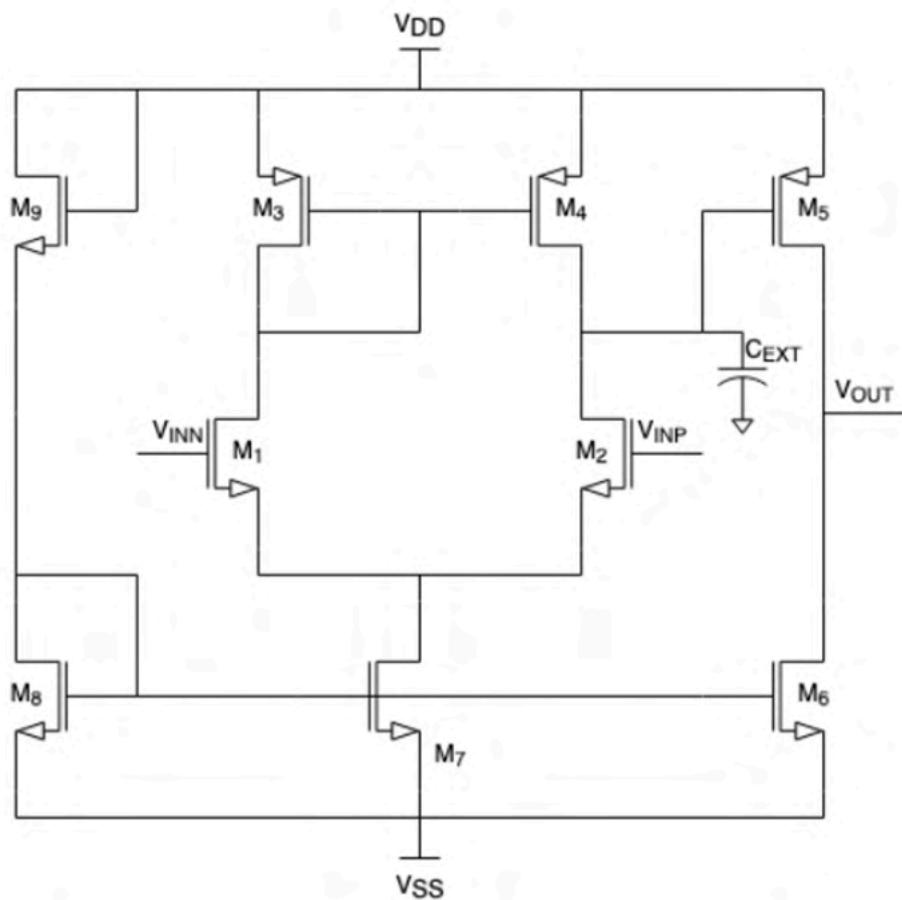


Figure 4.1: The Design of the OP-amp

The core of the operational amplifier are MOSFETs M1 to M4, but it has a low gain so M5 and M6 are used to amplify. M7 draws a constant current through it and M8 and M9 act as the biasing current to which the currents through M7 and M6 are referenced. Also there is a few equations will be used to calculate the size of the MOS. ($A_0 = \frac{-1}{V_{EB1}V_{EB5}\lambda^2}$, $GBW = \frac{2I_6}{V_{EB1}V_{EB5}C_L A_0 k}$, $C_{ext} = \frac{I_7}{I_6} C_L A_0 k$)

By using the Excel (Excel 1below) given to us, we obtained the following values which will be used to build the schematic of the op amp.

Excel 1

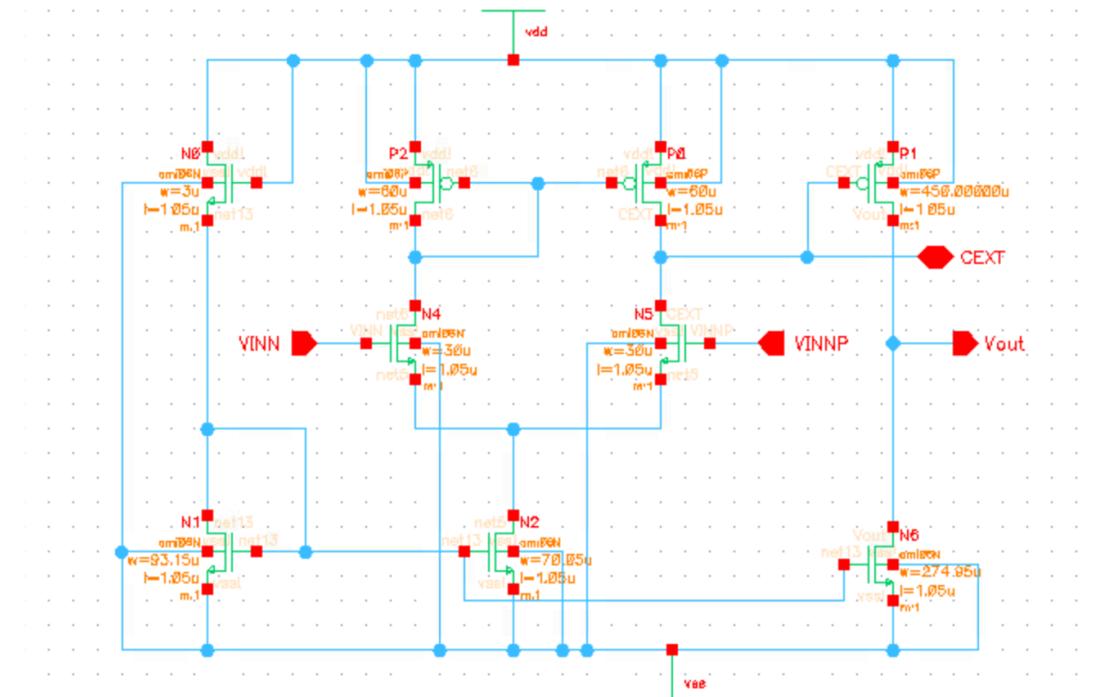


Figure 4.2: The Schematic of the OP-amp

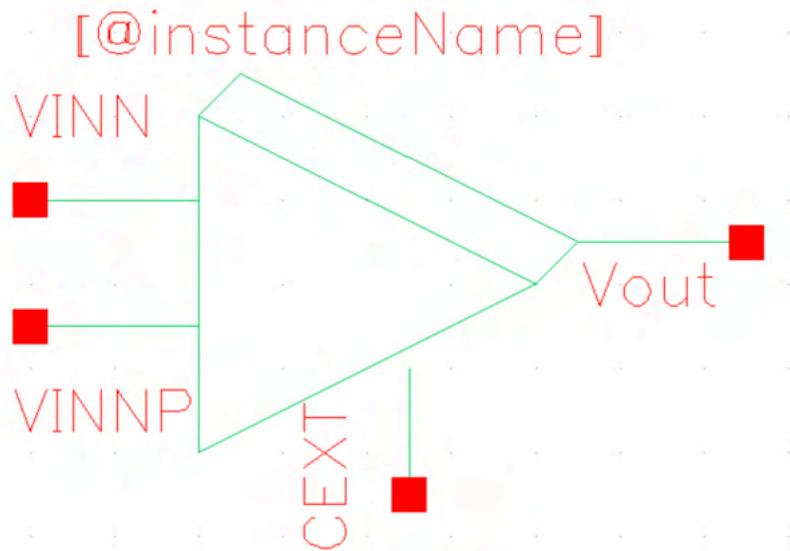


Figure 4.3: The Symbol of the OP-amp

Then the testbench was built for the simulation. (Figure 4.5) There are a few tests that we need to test. To begin with the testing of the inverting amplifier by using operational amplifier with an input of 1V. Thus, there are two resistors in the testbench schematic R₁ and R₀ with a ratio of 2. From the class (Figure) we know the voltage gain of the Inverting Amplifier is $= -\frac{R_f}{R_0} = -\frac{2}{1} = -2$. Then the simulation result (Figure 4.4) show that the output has an amplitude of -2V and that means the design worked with a gain of -2. (Figure 4.6)

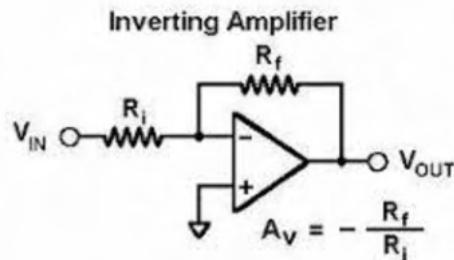


Figure 4.4: The voltage gain relationship the R_f and R_i

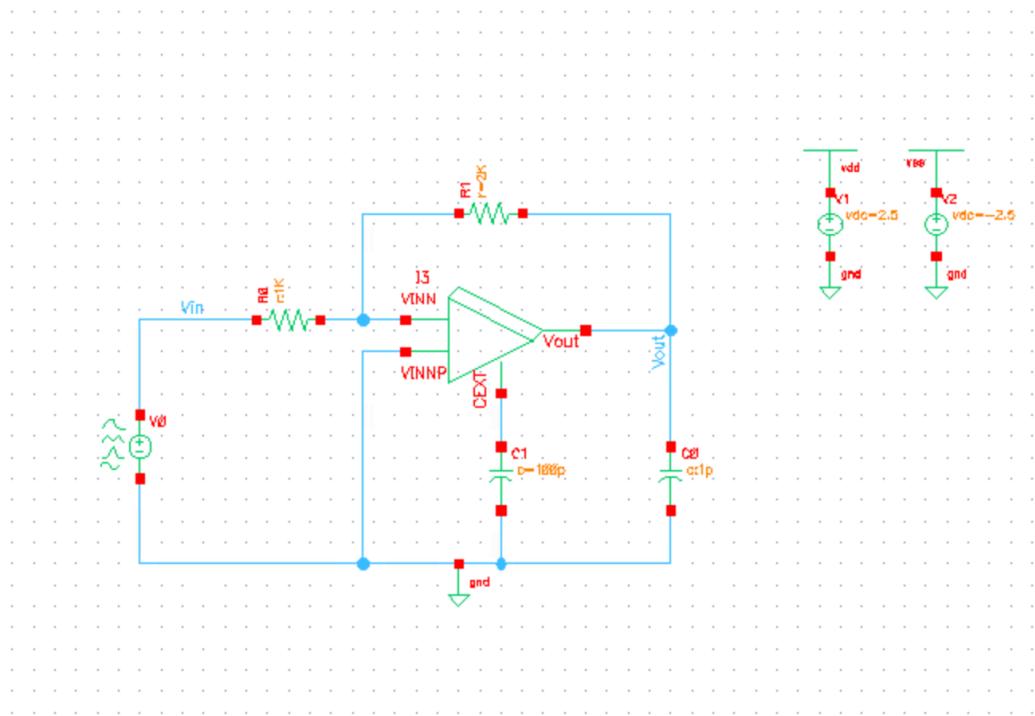


Figure 4.5: The Testbench of the OP-amp

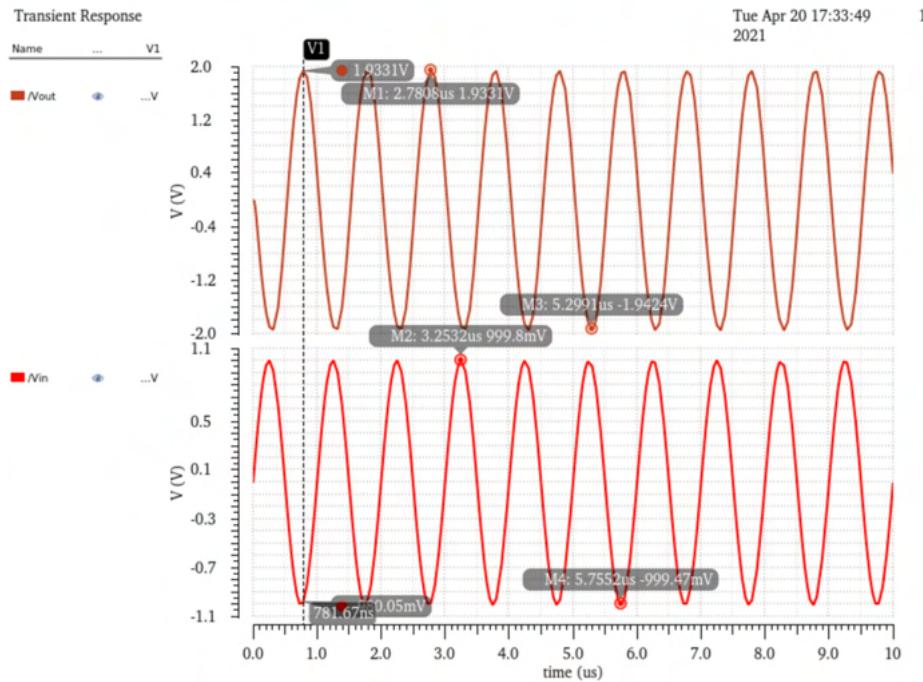


Figure 4.6: The Simulation result of the Op-amp with a gain of -2

Then we raised the input voltage to 786mV to test the accuracy of the design.

(Figure 4.7) From the simulation we can obtain that the output amplitude is about –1.4258V which is the result that super close to out expected to obtain with a gain of -2.

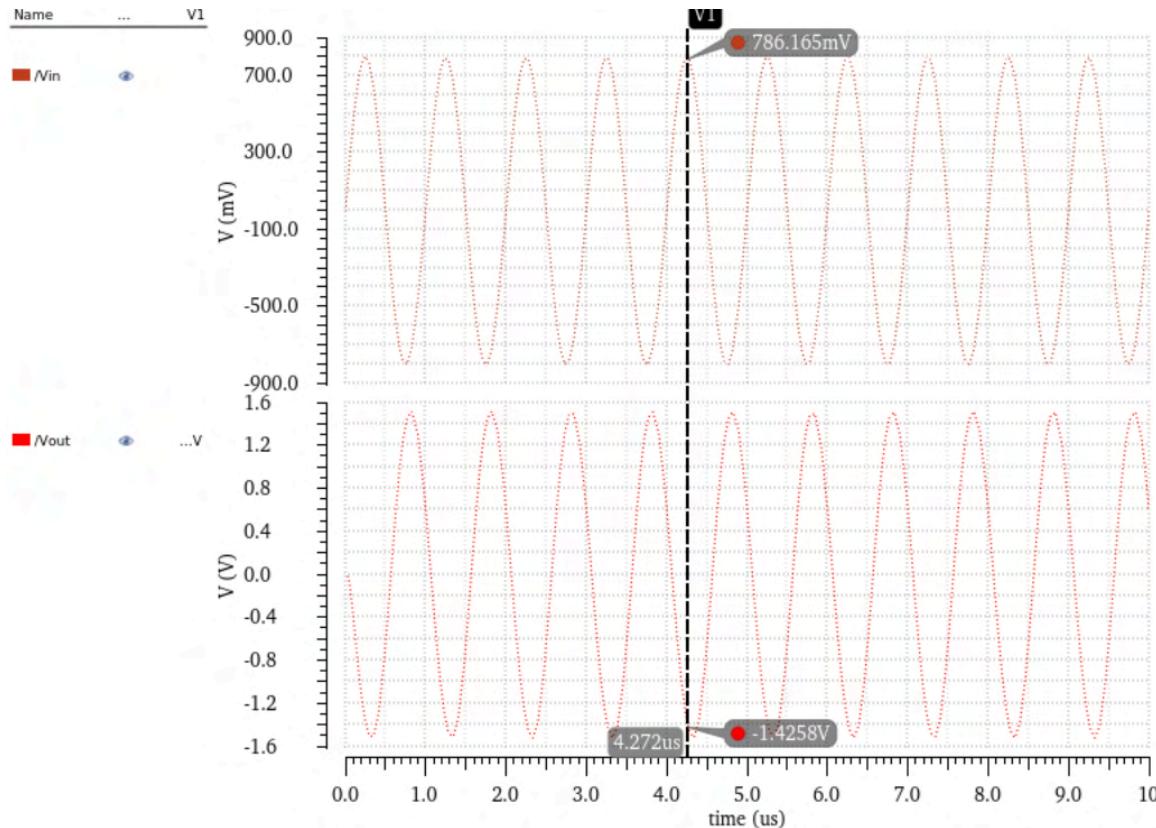


Figure 4.7: The simulation of the OP amp

Another test was built that will test the frequency response of the Operation amplifier. This allows us to determine the gain of the device as well as its 3dB point where it starts having no gain at higher frequencies due to it behaving as a low pass filter. A probe was connected in a unity gain configuration and the frequency was swept from 1Hz to 100MHz (Figure 4.8)

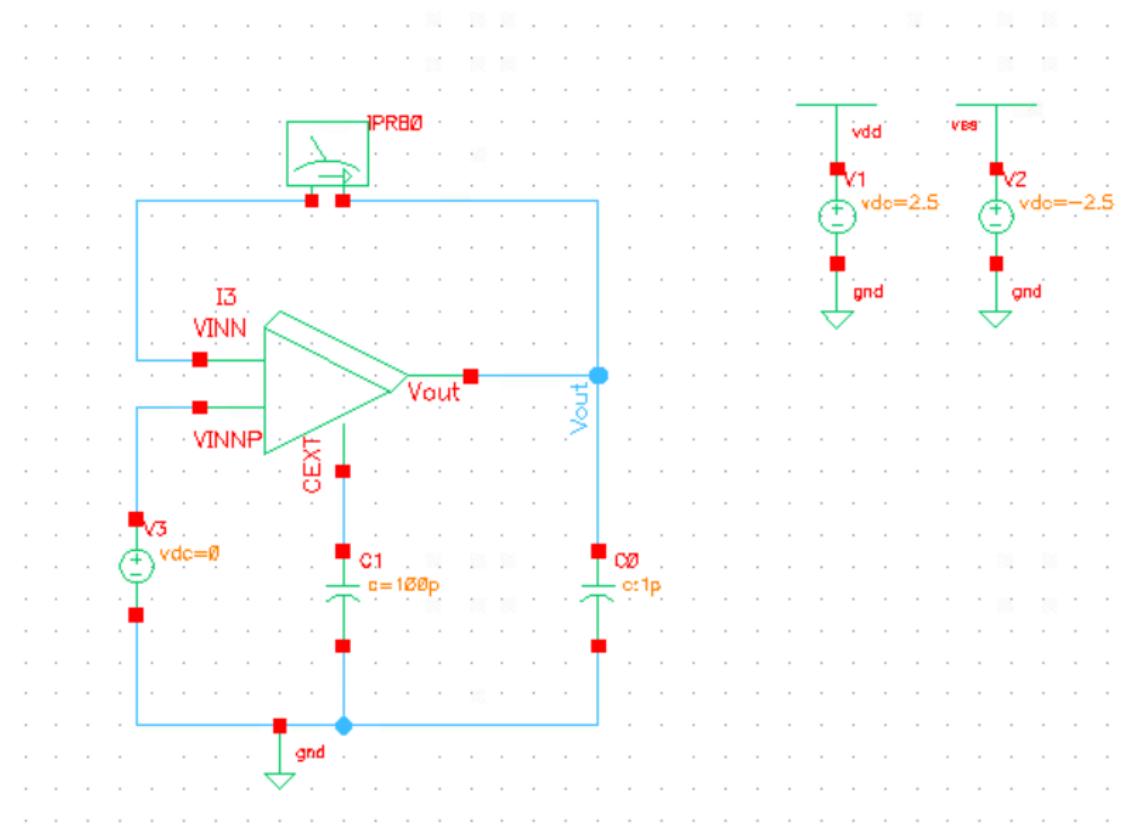


Figure 4.8: The noise test of the op amp

The frequency and noise simulation result can be seen in Figure 4.9 where it is seen that the max is at around 60dB which is we expected. The 3dB point where the size would be 0 is at 20.75MHz which is sufficient for this. The 3dB stage is at 37.3 degrees which is super off the values that we expected about 90 degrees but in this project this is not a big issue. Thus, we build our layout of the OP amp Figure 4.10.

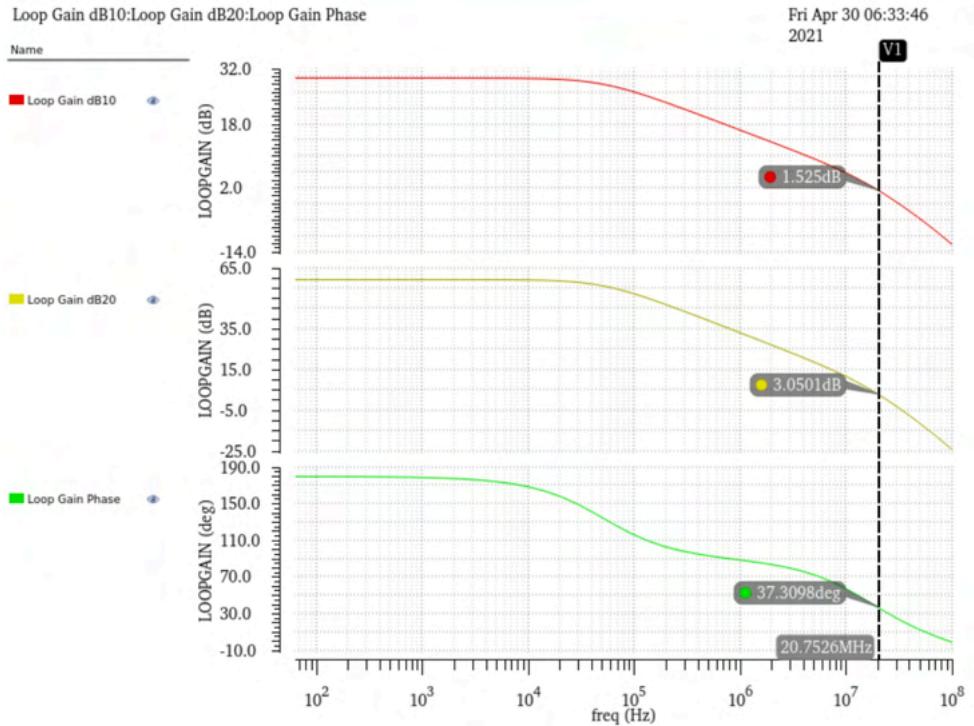


Figure 4.9: The Frequency test of the OP amp

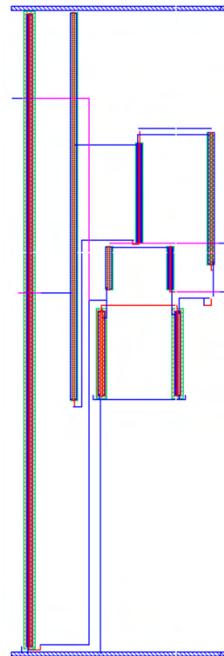


Figure 4.10: The layout of the OP amp

5 Digital to Analog Converter (DAC)

After we made the Operational amplifier and the Digital Potentiometer, the Digital to Analog converter can be created. This was done through utilizing the Potentiometer and its Resistor string as a voltage Divider. The voltage Divider proportion consistently increments in a stage of $1/15$ which is actually what a DAC does which builds each piece by a set measure of voltage. Nonetheless, the beginning of the Potentiometer should be associated with Ground and the end should be associated with the voltage Reference. The wiper terminals will be connected to the positive input of the operational amplifier with the negative terminal forming a unity gain configuration. The concept of the Design is given below Figure 5.1.

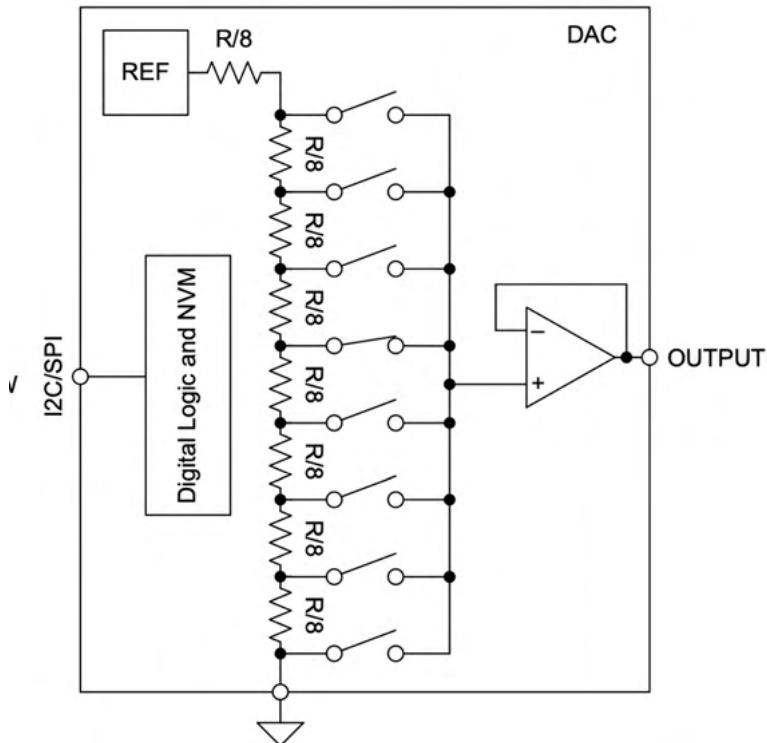


Figure 5.1: The Design concept of the digital to analog converter

Then the schematic of the design is created (Figure 5.2). The 4 bit input digital signal at the input, P1 connect to ground, P3 connect to Voltage Reference. Also the symbol of the DAC was created in Figure 5.3.

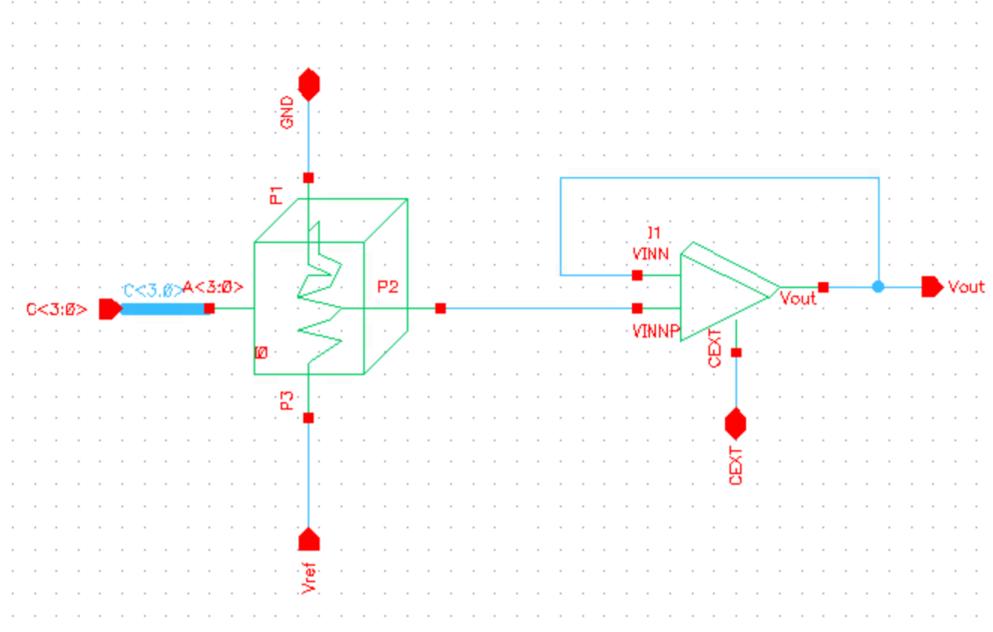


Figure 5.2: The Schematic of the Digital to Analog Converter

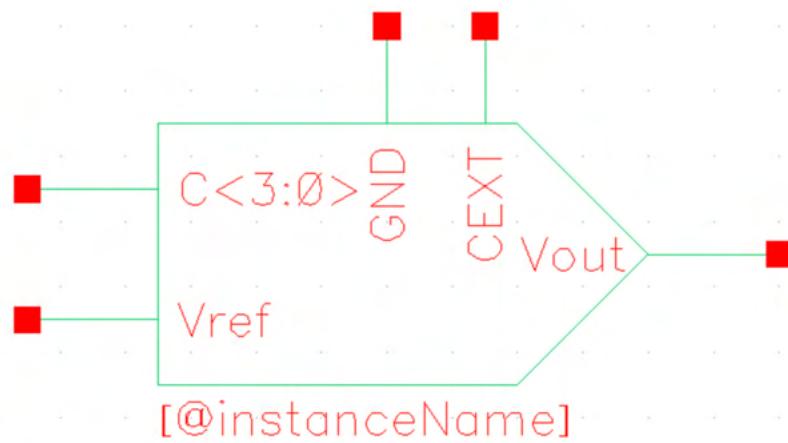


Figure 5.3: The symbol of the DAC

After getting the DAC symbol, the testbench was also created (Figure 5.4. A voltage reference of 1.5V was utilized to simplify everything to ascertain as there are fifteen stages so each piece increment would build the yield by 0.1V. The calculated output voltage table was made below that can be used to compare with the simulation result that generated by Cadence (Figure 5.5.1). We also tested then Vref is -1.5V (Figure 5.5.2)

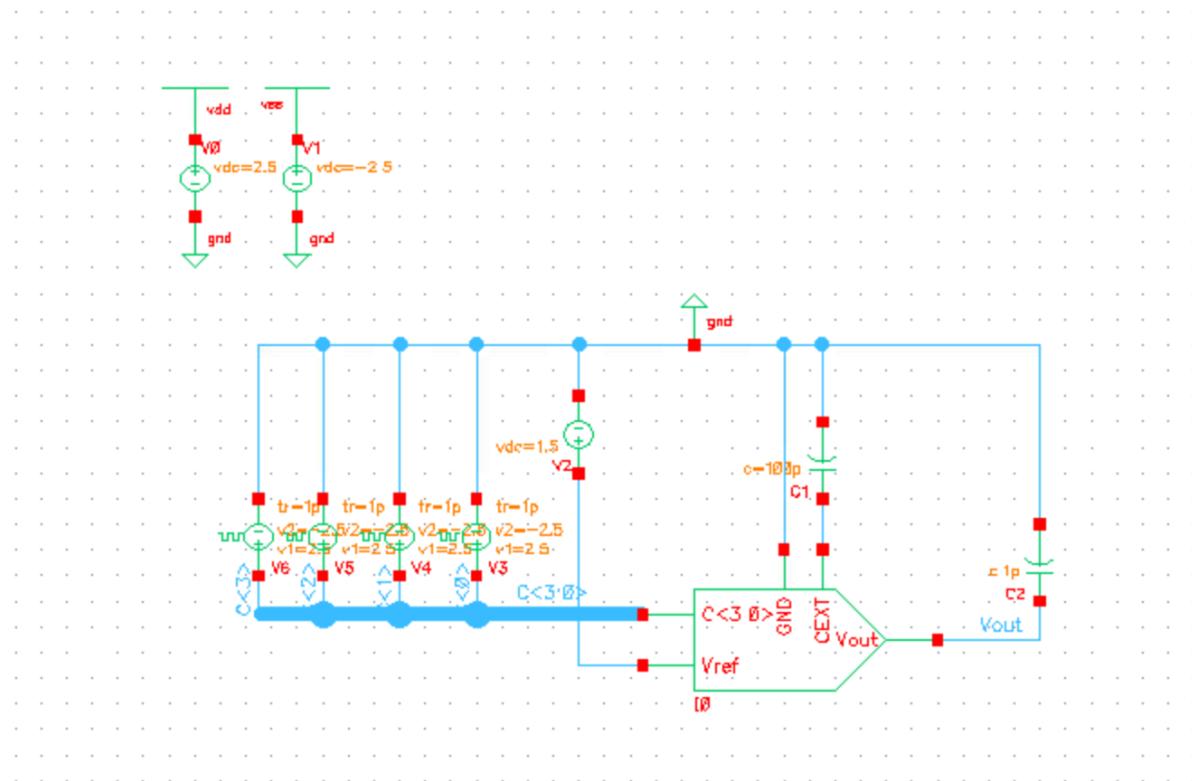


Figure 5.4: The Schematic of the Testbench

Note: Vref in here is 1.5V

Binary Input	Divider ratio	Output Voltage (V)
0000	0/15	0

0001	1/15	0.1
0010	2/15	0.2
0011	3/15	0.3
0100	4/15	0.4
0101	5/15	0.5
0110	6/15	0.6
0111	7/15	0.7
1000	8/15	0.8
1001	9/15	0.9
1010	10/15	1.0
1011	11/15	1.1
1100	12/15	1.2
1101	13/15	1.3
1110	14/15	1.4
1111	15/15	1.5

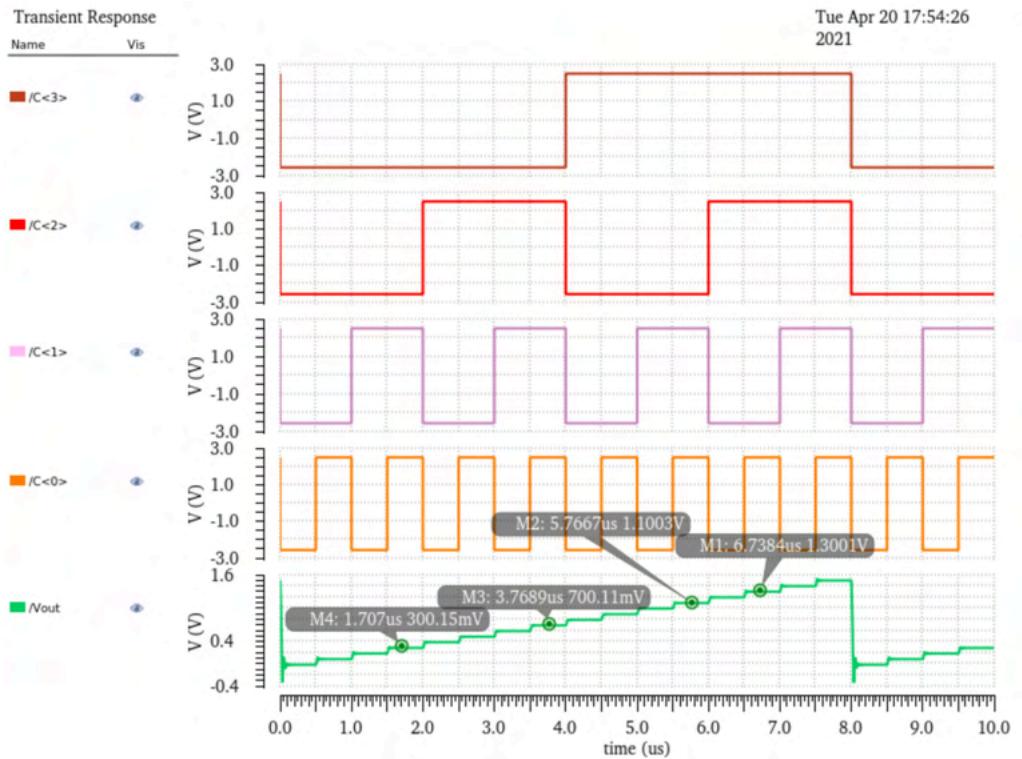


Figure 5.5.1: The Simulation result of the DAC with 1.5V Vref

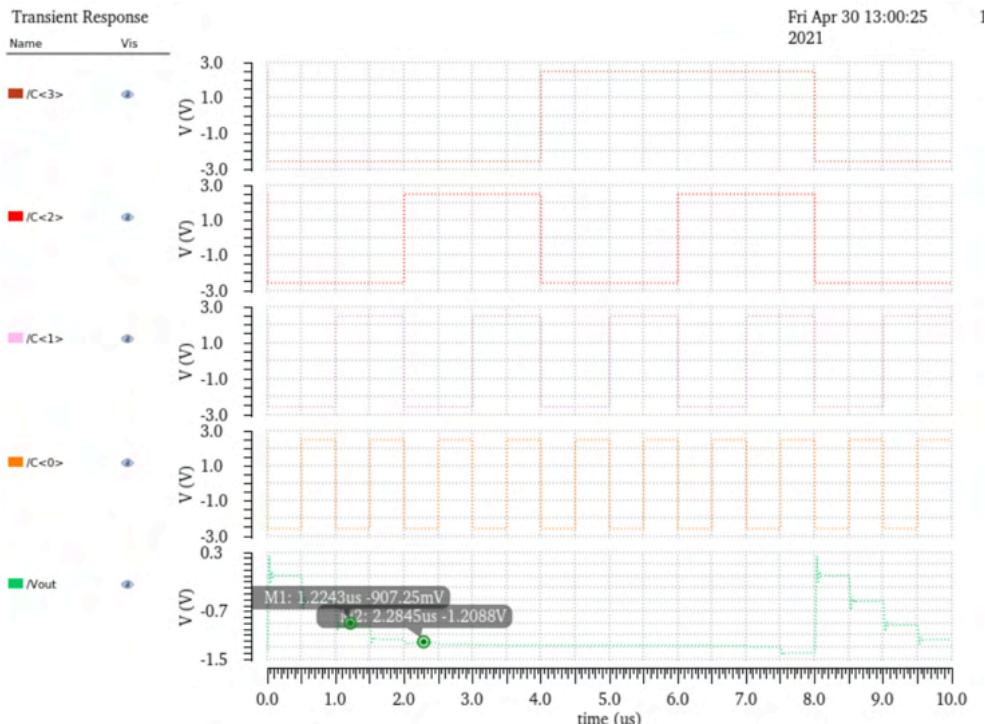


Figure 5.5.2: The Simulation result of the DAC with -1.5V Vref

By comparing the result between the Simulation and the Table, we found the Simulation result is a little bit off but accurate enough. The format of the DAC could then be made which was finished by the schematic. The layout (Figure 5.6) pass through both DRC and LVS assessments which is in the Appendix.

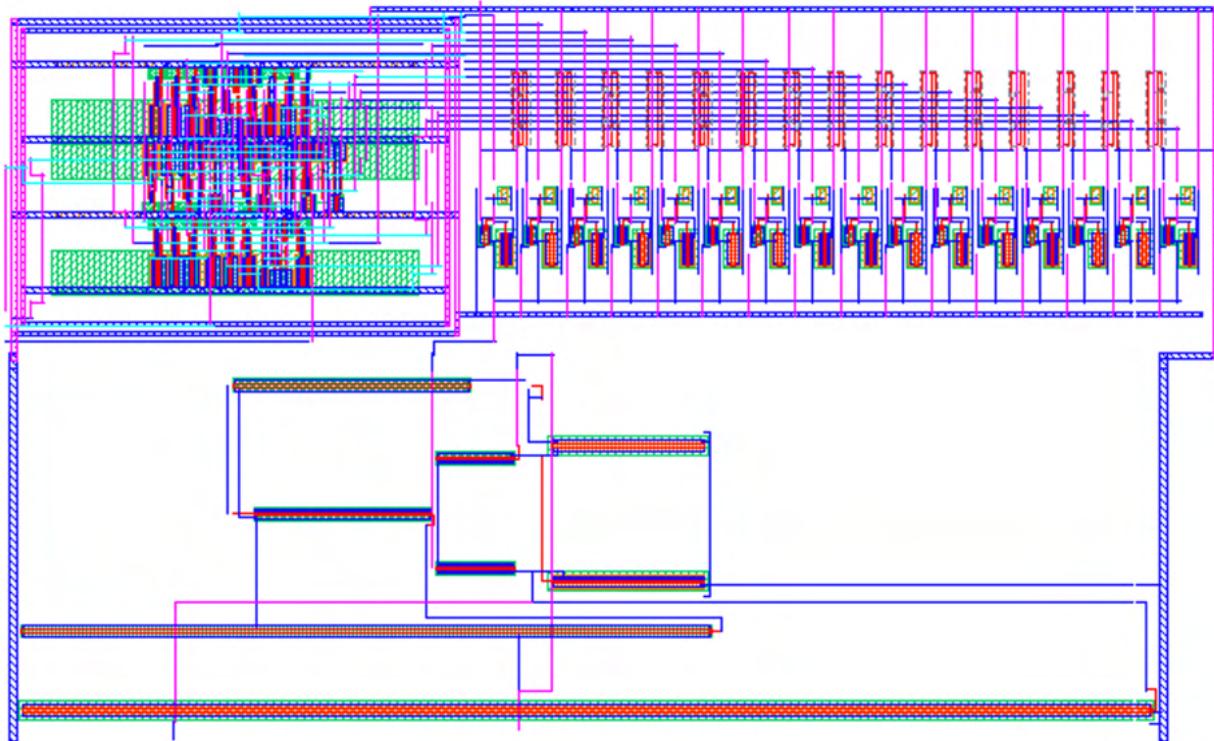


Figure 5.6: The layout of the DAC

6 Non - Inverting Amplifier

By using the Potentiometer and the operational amplifier, the inverting amplifier and Non inverting amplifier can be made (Figure 6.1). When setting up the gain of the non-inverting amplifier, the potentiometer can control the resistance and the resistance between the inverting pin of the op amp and ground. This results in a gain based on the ratio at the wiper. Then the symbol of the Non-Inverting Amplifier can was obtained. We can see the Table given below that could compare

with the result from the simulation, for each binary input we have different gain and resistor ratio.

Binary Input	Resistor Ratio	Gain
0000	0/75k	1
0001	5k/70k	1.071
0010	10k/65k	1.154
0011	15k/60k	1.25
0100	20k/55k	1.364
0101	25k/50k	1.5
0110	30k/45k	1.667
0111	35k/40k	1.875
1000	40k/35k	2.143
1001	45k/30k	2.5
1010	50k/25k	3
1011	55k/20k	3.75
1100	60k/15k	5
1101	65k/10k	7.5
1110	70k/5k	15
1111	75k/0	Infinity (in saturation region)

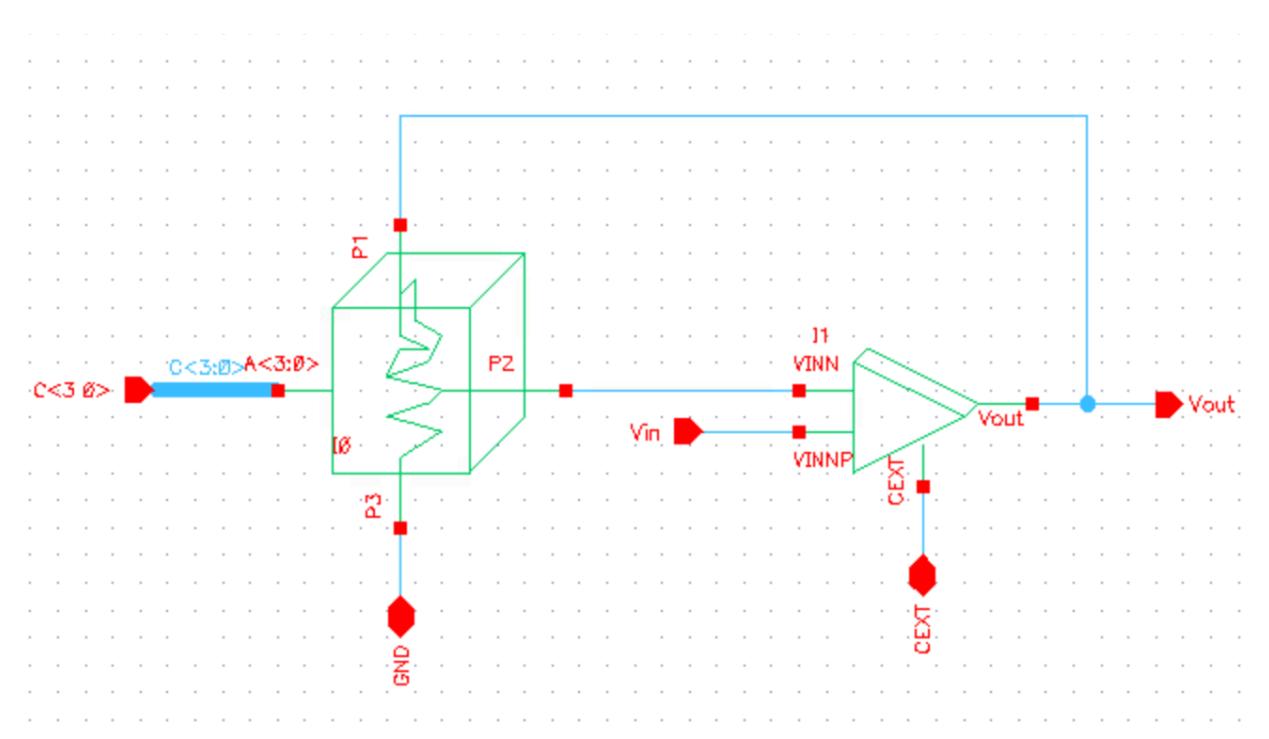


Figure 6.1: The Schematic of the Non-Inverting Amplifier

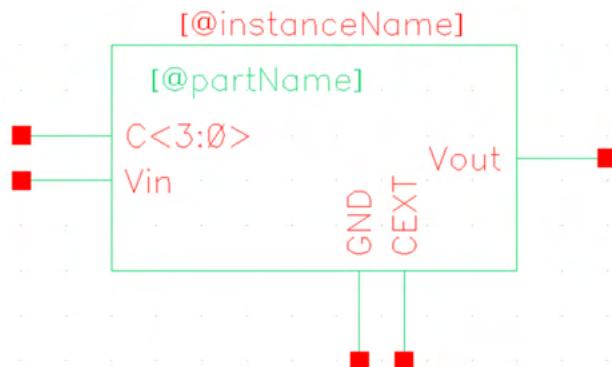


Figure 6.2: The symbol of the Non-inverting Amplifier

Then the testbench is created for the simulation (Figure 6.3). The 4 bit binary input sweep from 0000 to 1111 by using Vpulse. The first test is the DC voltage test, so we set the input as 100mV. By comparing the simulation result of the second clock (Figure 6.4.1) and the Table we can find they matched. There is an unknown issue happened here that is when we run the first clock there is a delay. We also tested

when we put a -100mV as an input the result also matched what we expected.

(Figure 6.4.2)

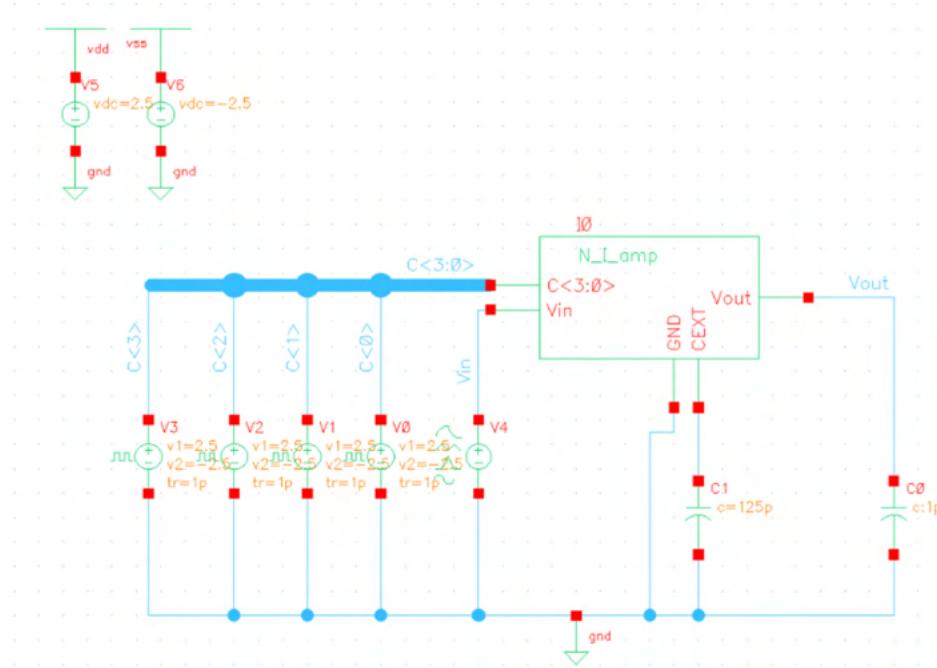


Figure 6.3: The Testbench of the Non-Inverting Amplifier

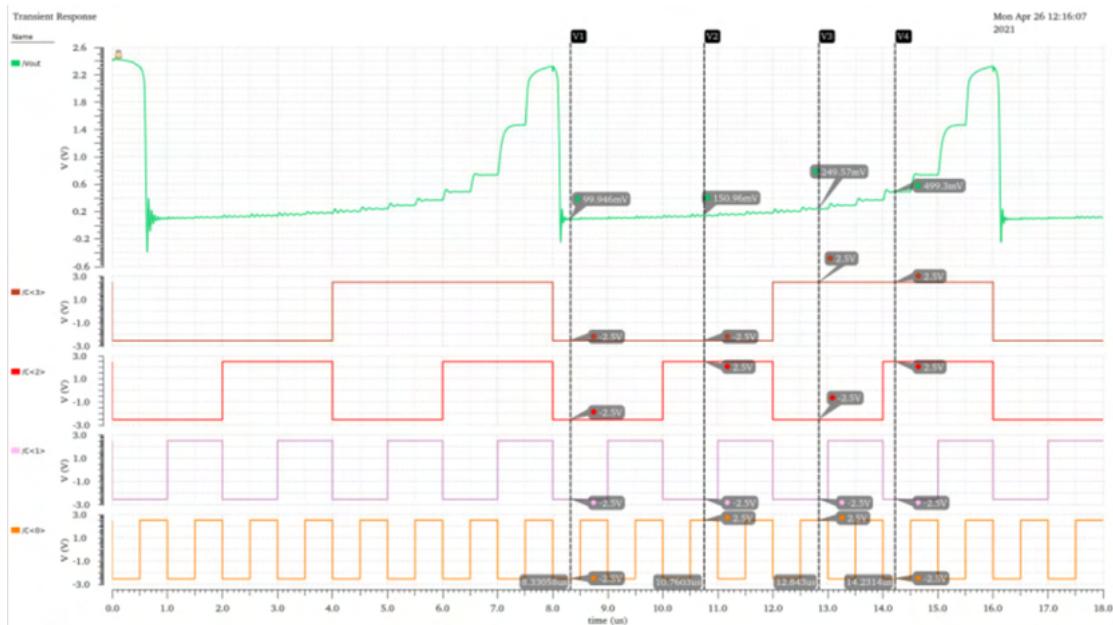


Figure 6.4.1: The simulation result of the non-Inverting amplifier (DC voltage input with 100mV)

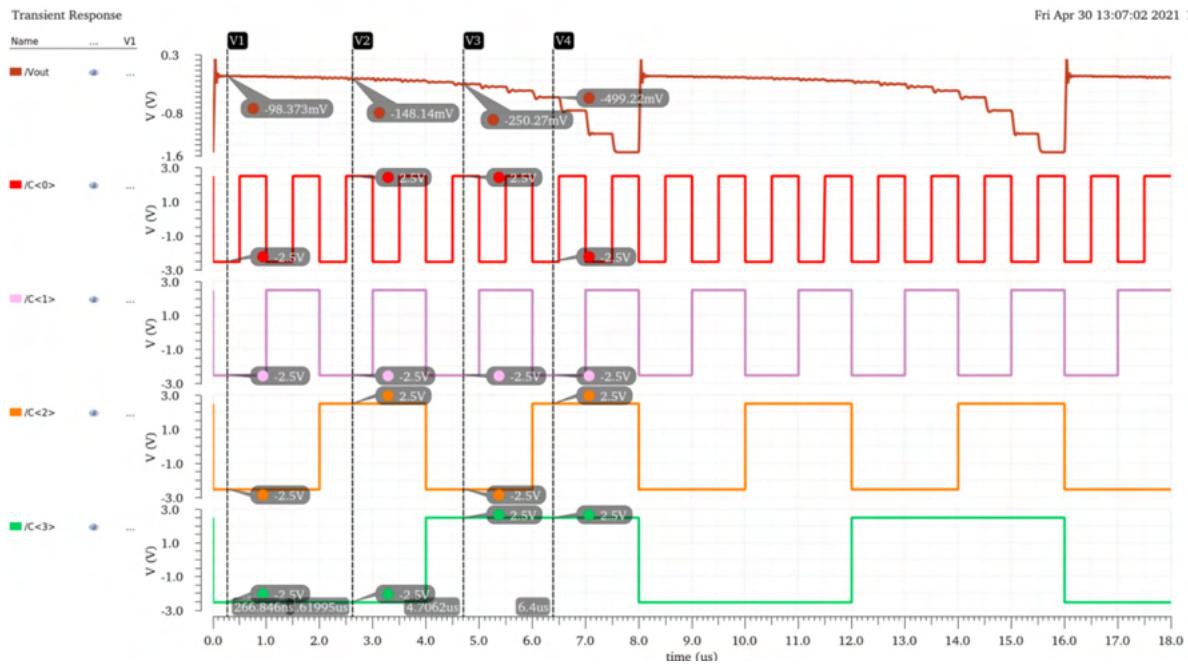


Figure 6.4.2: The simulation result of the non-Inverting amplifier (DC voltage input with -100mV)

Then we need to test the circuit when we use the AC sine wave as the input. Thus we set sine wave with a 4MHz frequency and 100mVpk amplitude. Then we can obtain the simulation (Figure 6.5). By comparing the V_{in} and V_{out} we can find that the circuit worked as we expected. (0101 is about 1.5 1001 is about 2.5 1100 is about 5.0)

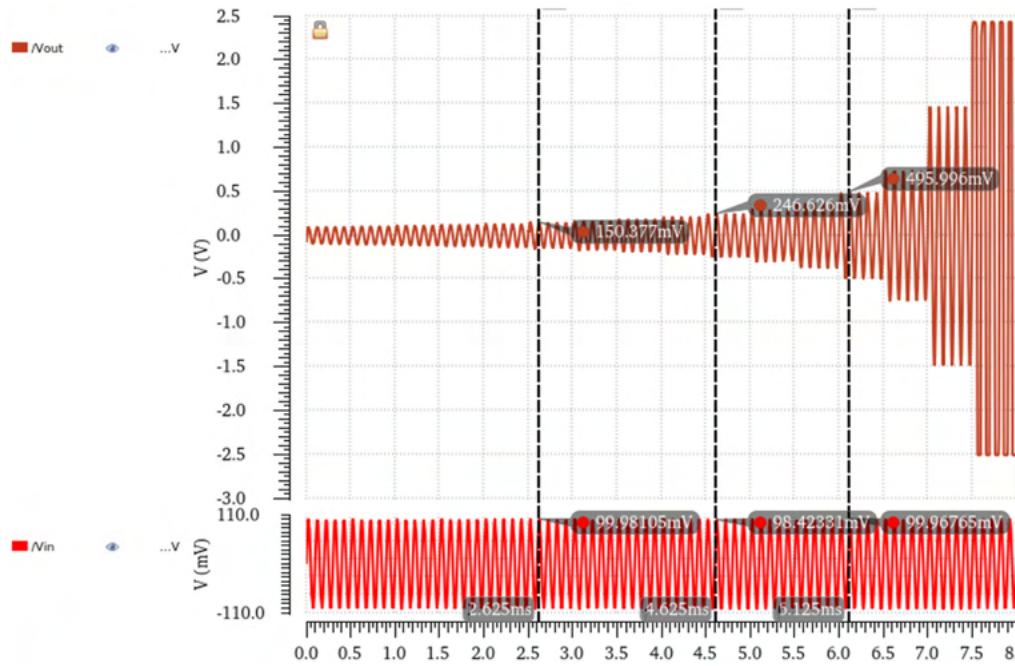


Figure 6.5: The simulation result of the non-Inverting amplifier (AC sine wave input)

After proofing the design is correct, the layout is created. Like what we did previously we put the potentiometer the and op-amps together. In Figure 6.6 shows the final layout for the non-inverting amplifier. The layout passed the DRC and LVS checks which is in the Appendix.

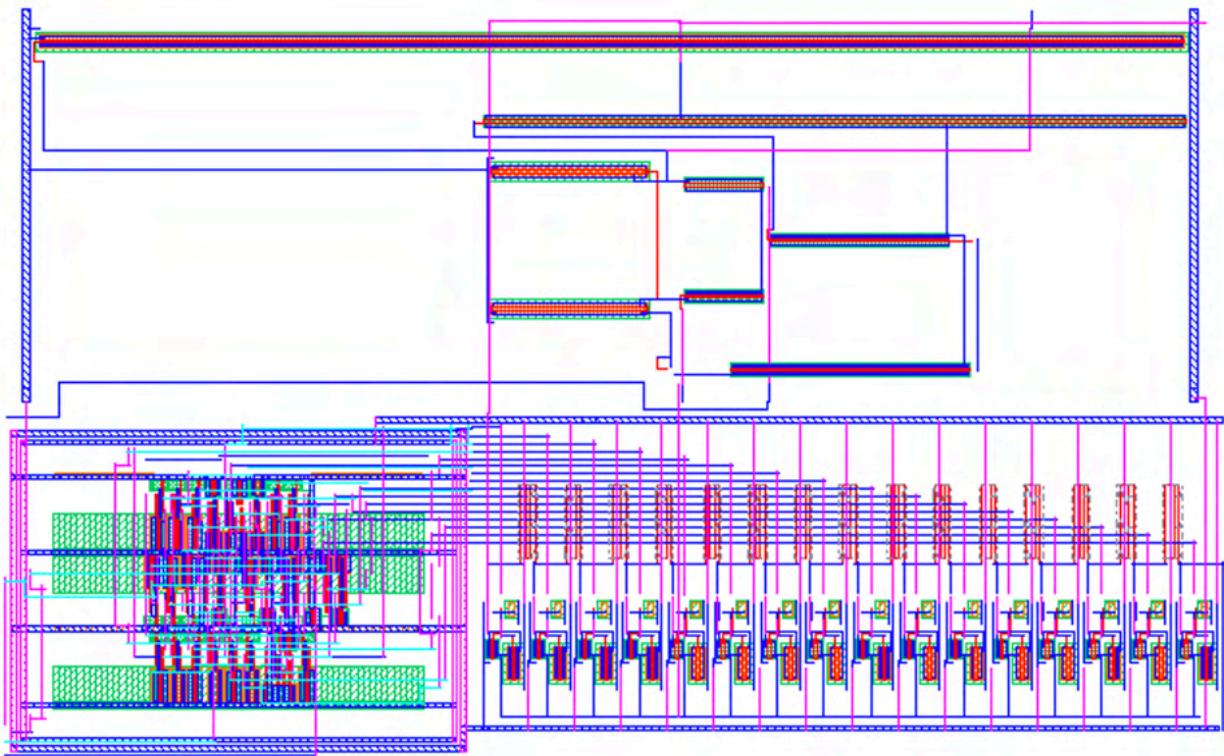


Figure 6.6: The Layout of the Non-Inverting amp

7 Inverting amp

For making the Inverting Amplifier, the means were about equivalent to the Non-reversing Amplifier. The Potentiometer controls the Gain, and Gain will be founded on the proportion of the Wiper (Figure 7.1). The input is connected to P3 of the potentiometer, the output to P1, and the inverting pin of the op amp to the wiper. Then the symbol also was created (Figure 7.2) The non-inverting pin is connected to ground. The table below will present the expected gain we will get.

Binary Input	Resistor Ratio	Gain
0000	0/75k	0
0001	5k/70k	-0.071

0010	10k/65k	-0.154
0011	15k/60k	-0.25
0100	20k/55k	-0.364
0101	25k/50k	-0.5
0110	30k/45k	-0.667
0111	35k/40k	-0.875
1000	40k/35k	-1.143
1001	45k/30k	-1.5
1010	50k/25k	-2
1011	55k/20k	-2.75
1100	60k/15k	-4
1101	65k/10k	-6.5
1110	70k/5k	-14
1111	75k/0	-Infinity (Sat region)

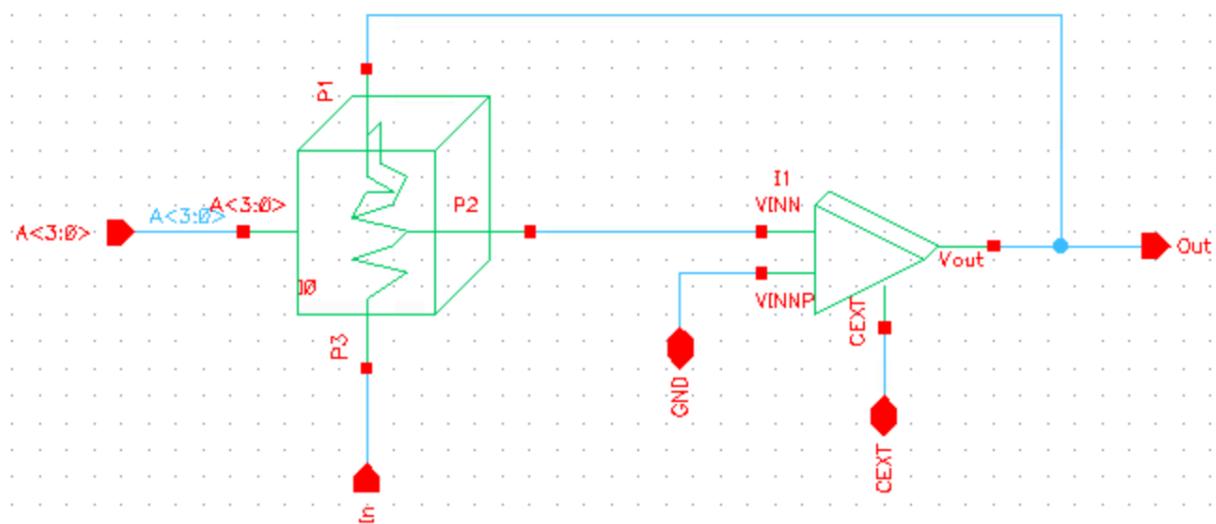


Figure 7.1 The Schematic of the Inverting Amplifier

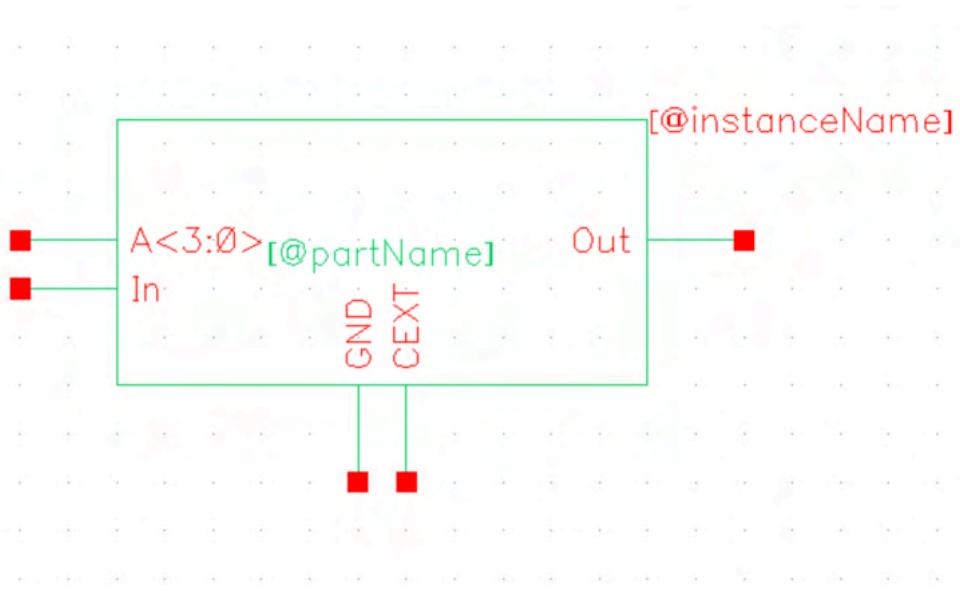


Figure 7.2 The Symbol of the Inverting Amplifier

Then we created the testbench to do the simulation (Figure 7.3). Like what we did in Non-Inverting Amplifier, The 4 bit binary input sweep from 0000 to 1111 by using Vpulse. The first test is the DC voltage test, so we set the input as 100mV. By comparing the simulation result of the second clock (Figure 7.4.1) and the Table we can find they matched. Then we also set the negative input -100mV which also matched what we expected. (Figure 7.4.1)

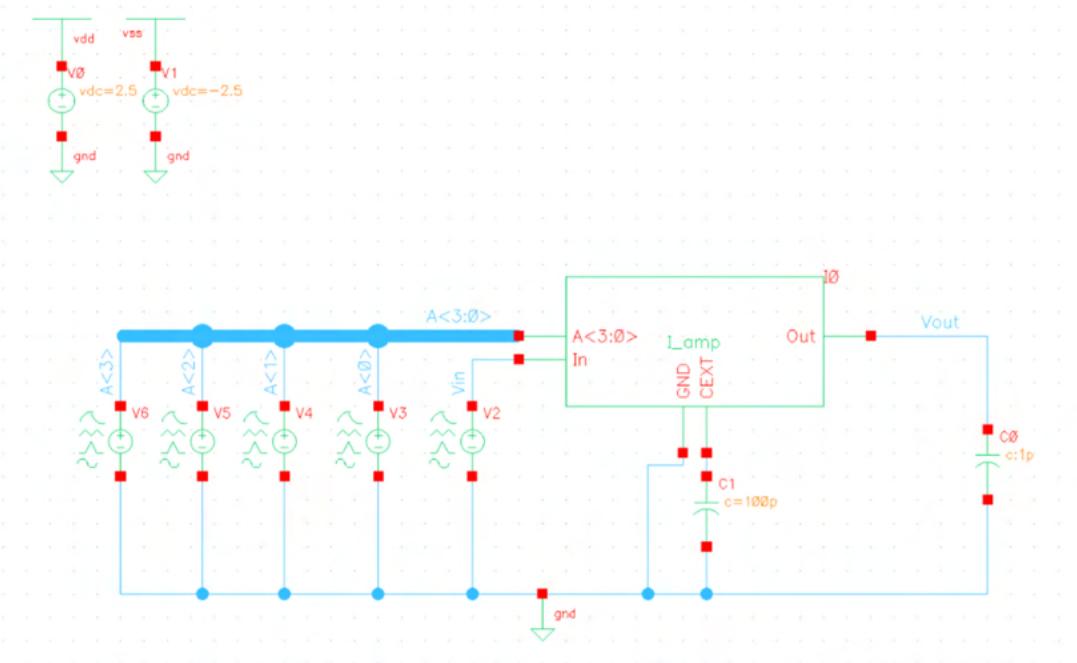


Figure 7.3: The Testbench of the Inverting Amplifier

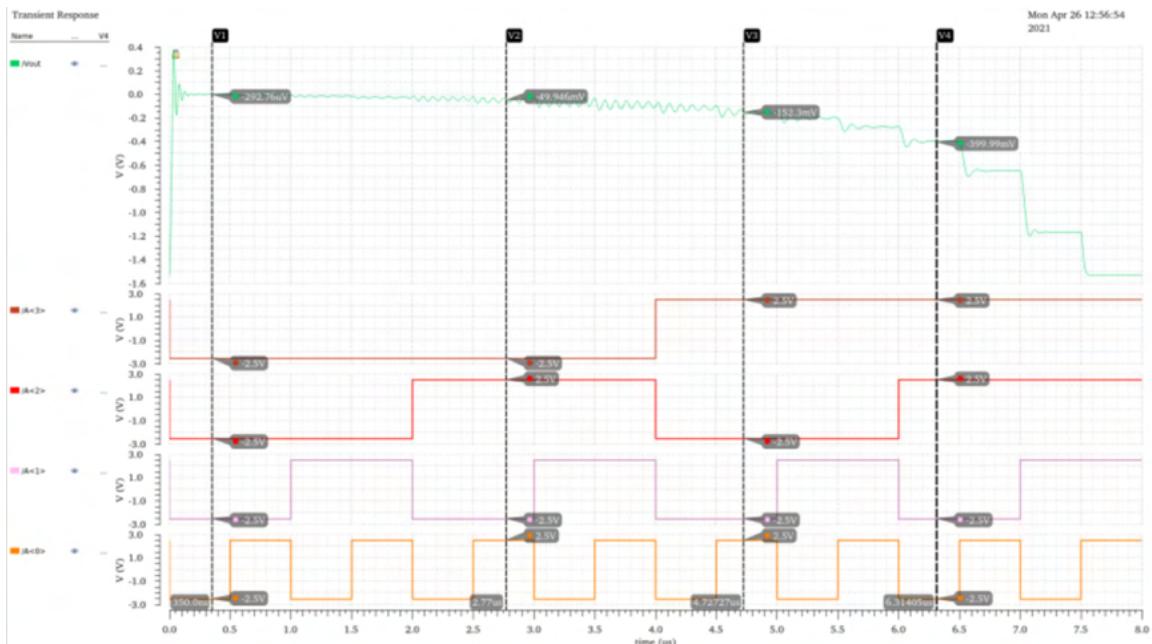


Figure 7.4.1: The simulation result of the Inverting amplifier (DC voltage input 100mV)

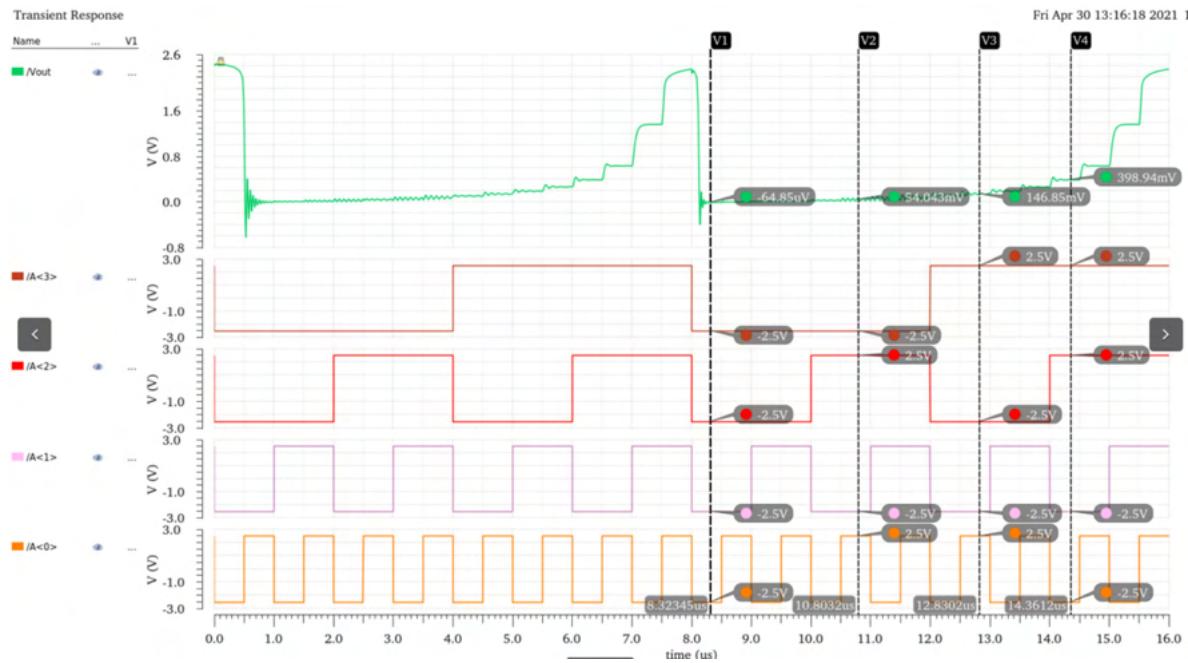


Figure 7.4.2: The simulation result of the Inverting amplifier (DC voltage input - 100mV)

Then like what we did for the Non-Inverting amplifier, we set AC input with frequency 4MHz and amplitude 100mVpk. We expected the gains to match the table given above. The simulation results for the AC simulation are shown in Figure 7.5. (0101 gain is about -0.5, 1001 gain is about -1.5 and 1100 gain is about -4.0). We can find that the simulation result matched the table above.

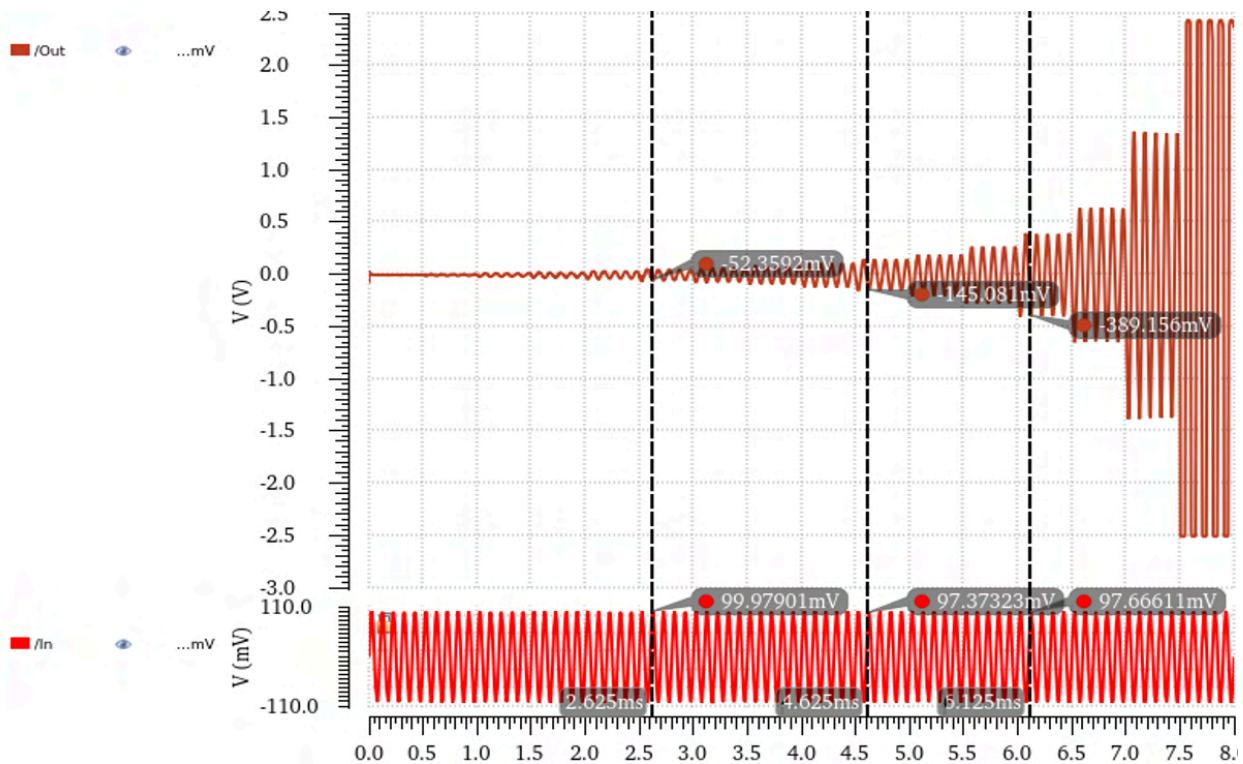


Figure 7.5: The simulation result of the Inverting amplifier (AC sine wave input)

After proofing the design is correct, the layout is created. Like what we did previously we put the potentiometer the and op-amps together. In Figure 7.6 shows the final layout for the non-inverting amplifier. The layout passed the DRC and LVS checks which is in the Appendix.

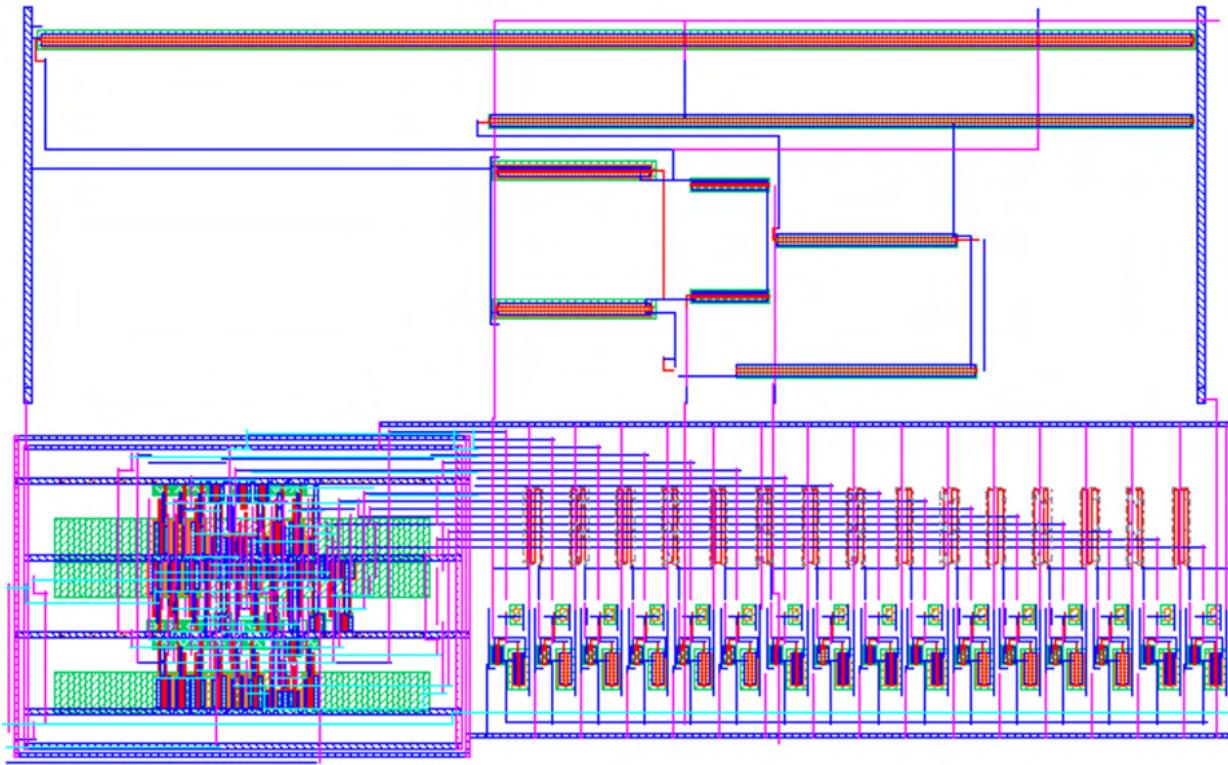


Figure 7.6: The layout of the Inverting amp

8 The final circuit

In this part, all of the components that was created will put them all together as the final project circuit. The non-inverting amplifier was associated with the In0, the inverting amplifier was connected to In1, the operational amplifier was connected to In2, and the DAC was associated to In3. Likewise, a piece of the circuit is the potentiometer that is an independent part. The client could choose to interface the potentiometer with a certain goal in mind, so the three pins are accessible for the client. The final circuit schematic and the symbol is given below (Figure 8.1 and

Figure 8.2) and the description for each PINs also is given below.

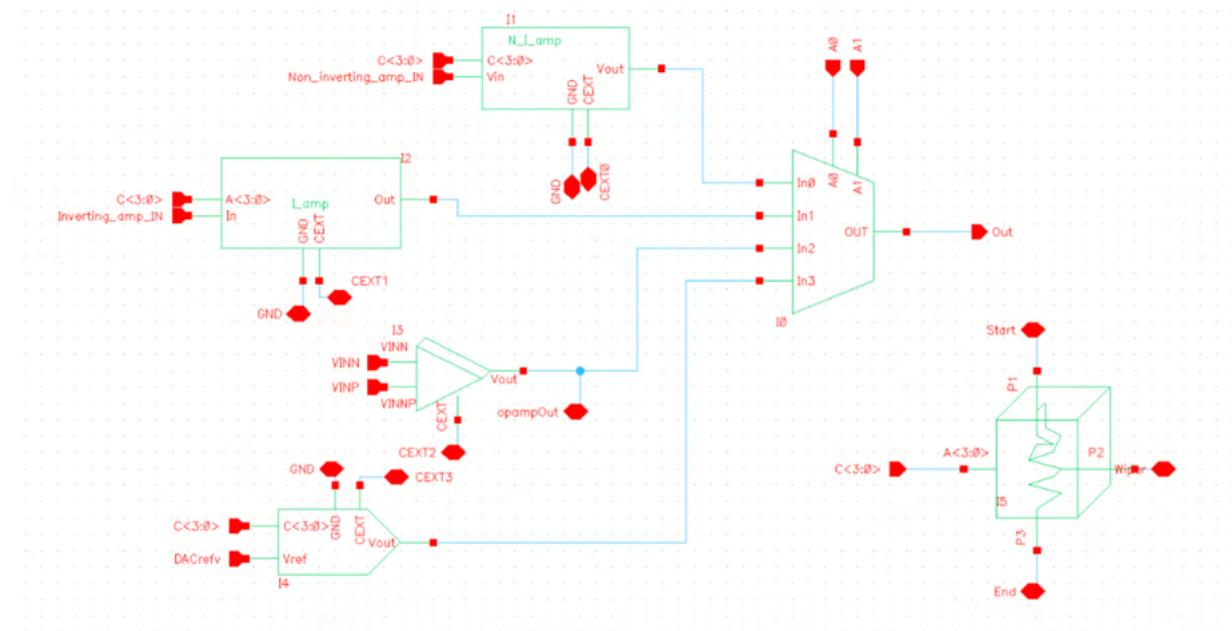


Figure 8.1: The Schematic of the Final circuit

Pin Name	Description
A0	MUX selector for the first bit.
A1	MUX selector for the second bit.
C<3:0>	The digital potentiometer 4 binary input (selects the resistance ratio at the wiper)
Non_inverting_amp_IN	Input to the non-inverting amplifier
Inverting_amp_IN	Input to the inverting amplifier
DACref	Input for the DAC reference voltage
VINN	Input to the inverting pin of the independent op amp
VINP	Input to the non-inverting pin of the independent op amp
opampOut	Output to the independent op amp
Out	Final result of the project circuit
Start	start the potentiometer

Wiper	wiper of the potentiometer
End	end of the potentiometer
GND	connect to ground
VDD	Upper power supply
VSS	Lower power supply
Cext1	Capacitor connection for the non-inverting amplifier
Cext2	Capacitor connection for the inverting amplifier
Cext3	Capacitor connection for the op amp
Cext4	Capacitor connection for the DAC

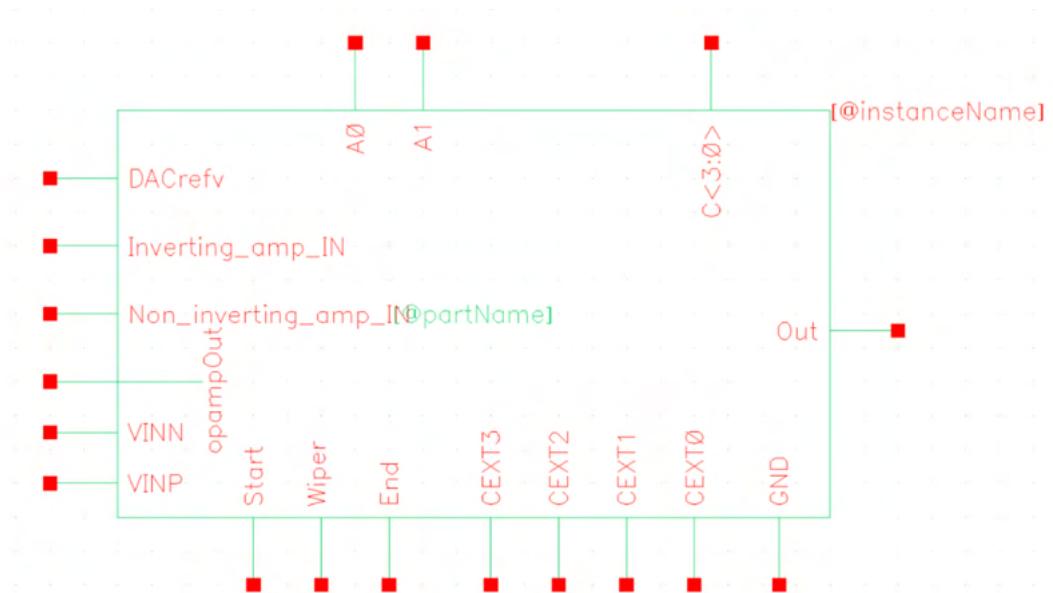


Figure 8.2: The symbol of the Final Circuit

The next step was to make a test bench that can test the whole design. Proofing that the circuit is correct , we set up every component to carry on as they did in their individual testing, so if the segment has about similar yield as its individual test, we would realize that that part acts accurately on the project circuit. We set the digital potentiometer's sweep from 0000 to 1111, also we set A0 and A1 to 00, 01,

10 and 11. DACREF shared with DAC and the amplifier inputs where it would include 100mV for the amplifier and 1.5V for the DAC, because in this way we can save some place on the symbol. The testbench for the circuit also is created (Figure 8.3). The simulation result of the whole circuit is also at below(Figure 8.4).

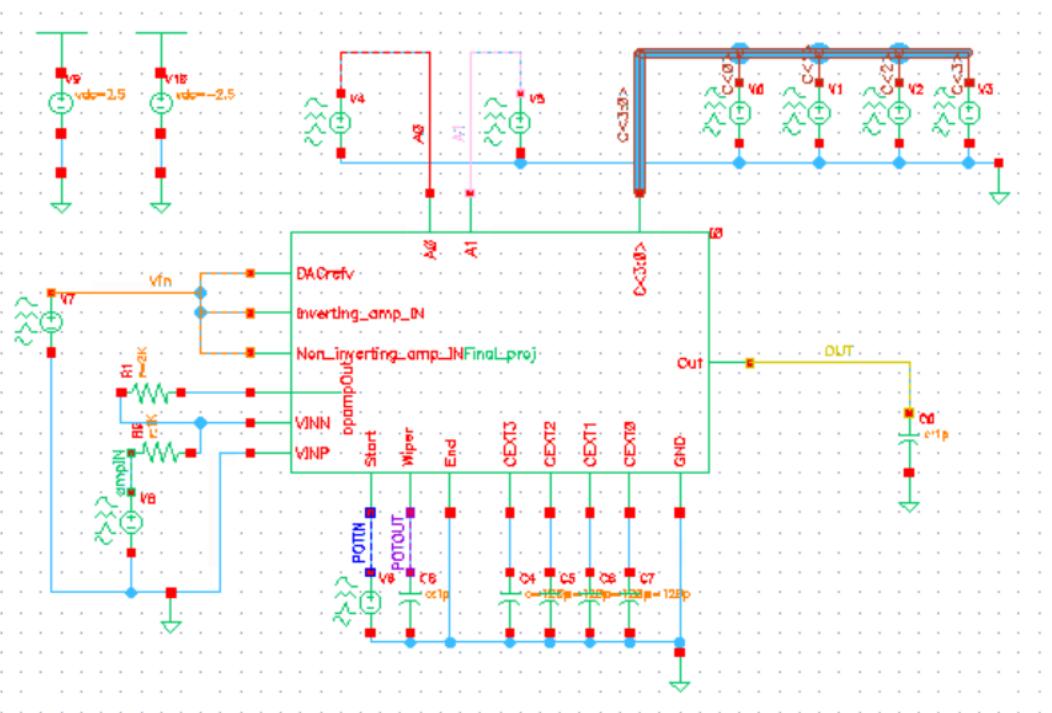


Figure 8.3: The testbench of the project circuit

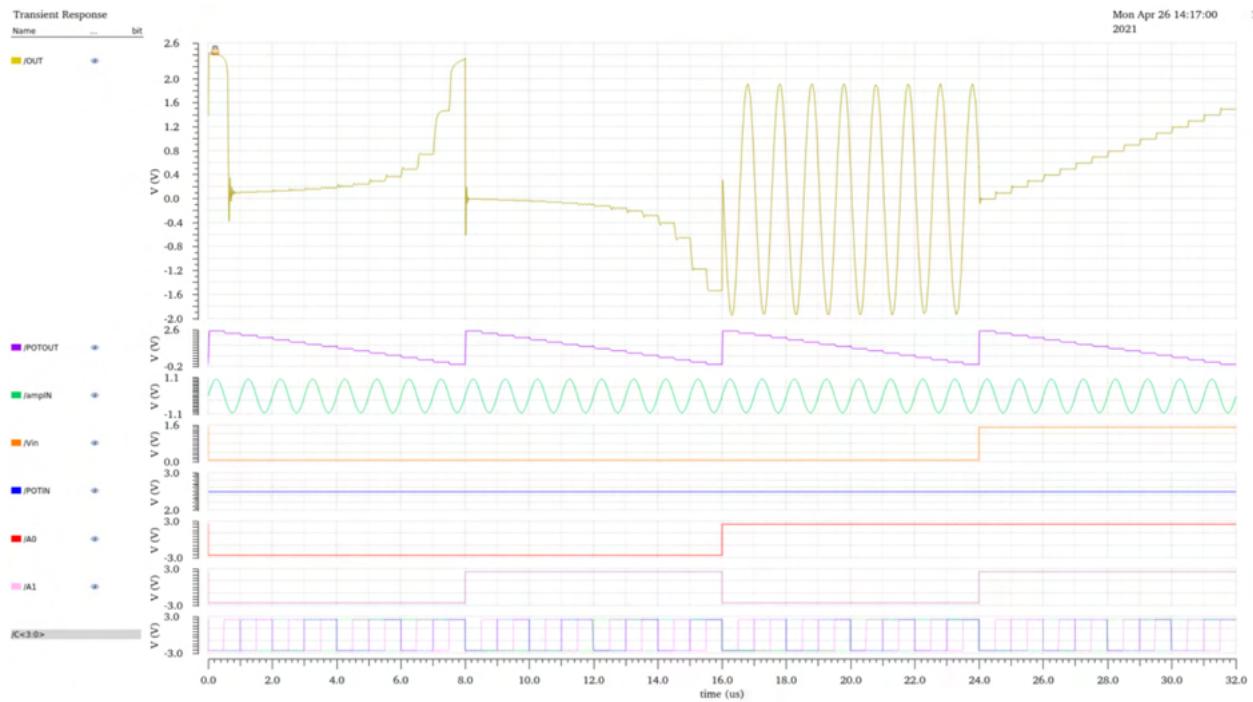


Figure 8.4: The simulation result of the Project circuit

Moreover, by comparing with the individual simulation result that we tested from the former steps. For the non-inverting amplifier, shown in Figure 8.5, for binary inputs 0101, 1001, and 1100. The results in a gain of 1.5182, 2.5098, and 4.9719 respectively and they are really close to the value that we expected.

For the inverting amplifier simulation result in Figure 8.6. For binary inputs 0101, 1001, and 1100. The results in a gain of -0.49362, -1.4169, and -4.0046 respectively and they are really close to the value that we expected.

For the op amp the simulation result in Figure 8.7, we can see the gain is about -2 which is the gain that we expected to get.

For the DAC, the simulation result in Figure 8.8. The DAC is receiving 1.5V at its Vref like in the individual test bench, and by comparing the values shown from the simulation and the table above we can see the result is correct.

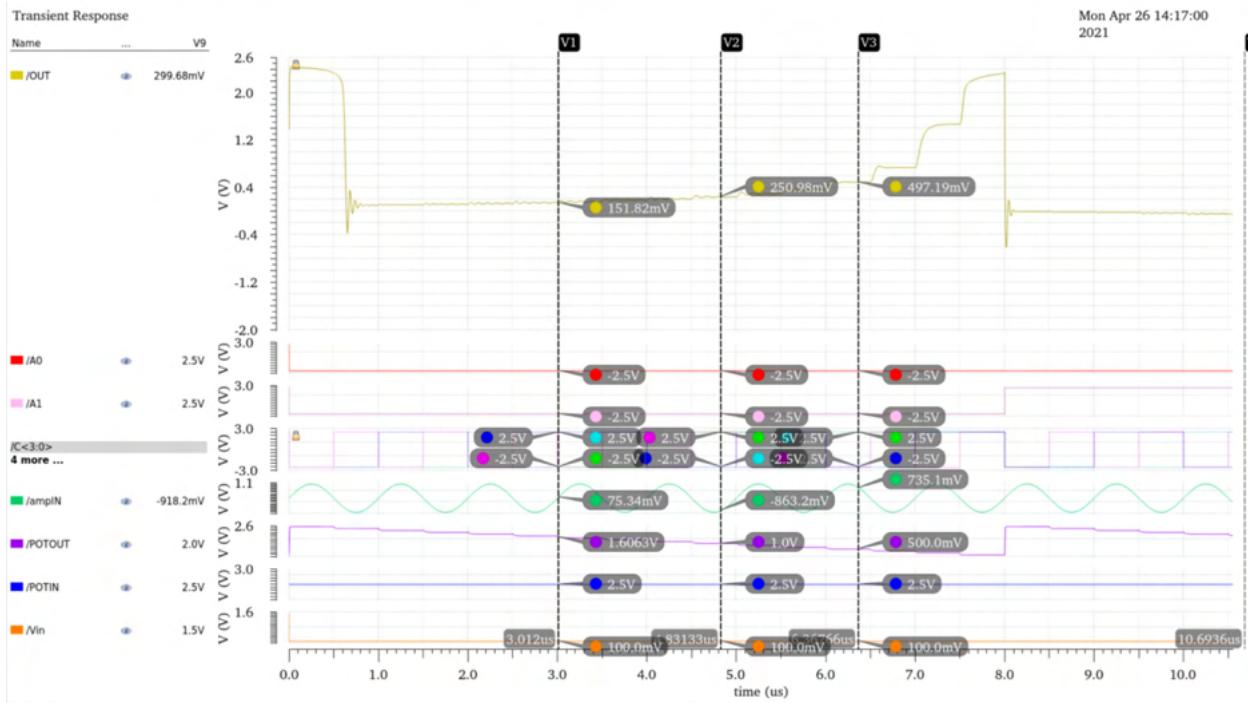


Figure 8.5: The Non-Inverting Amplifier Simulation

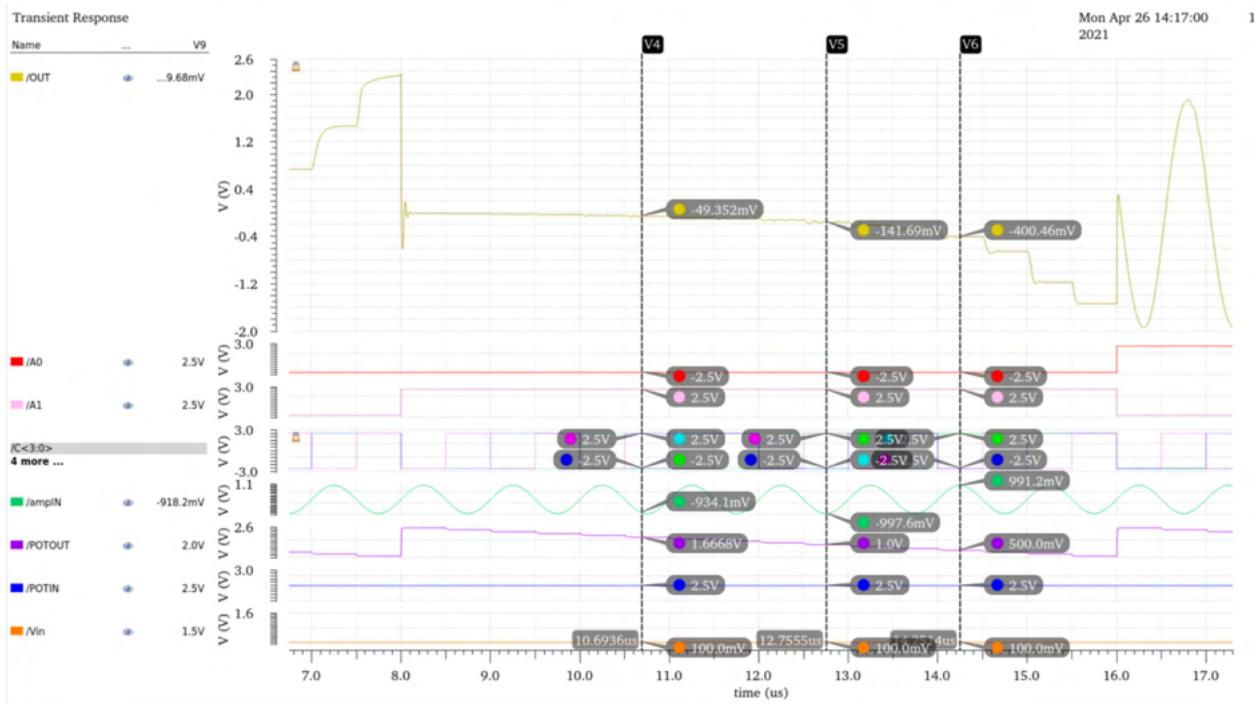


Figure 8.6 The Inverting Amplifier Simulation

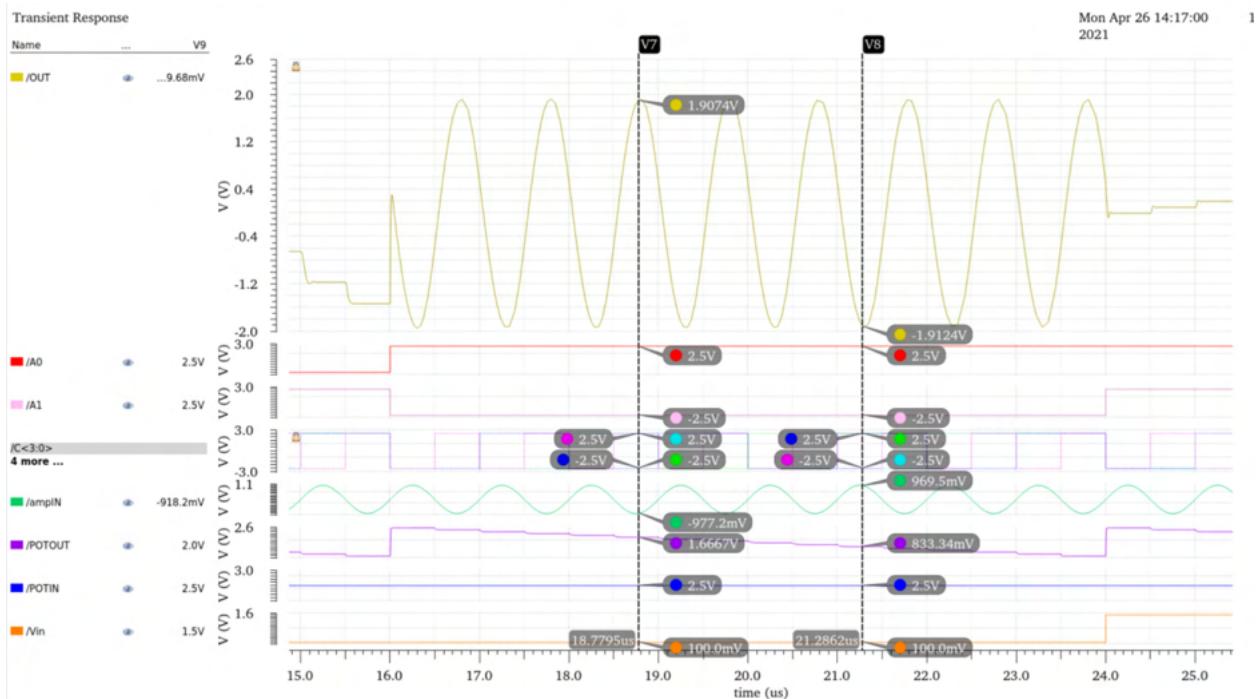


Figure 8.7 The OP-Amp simulation result

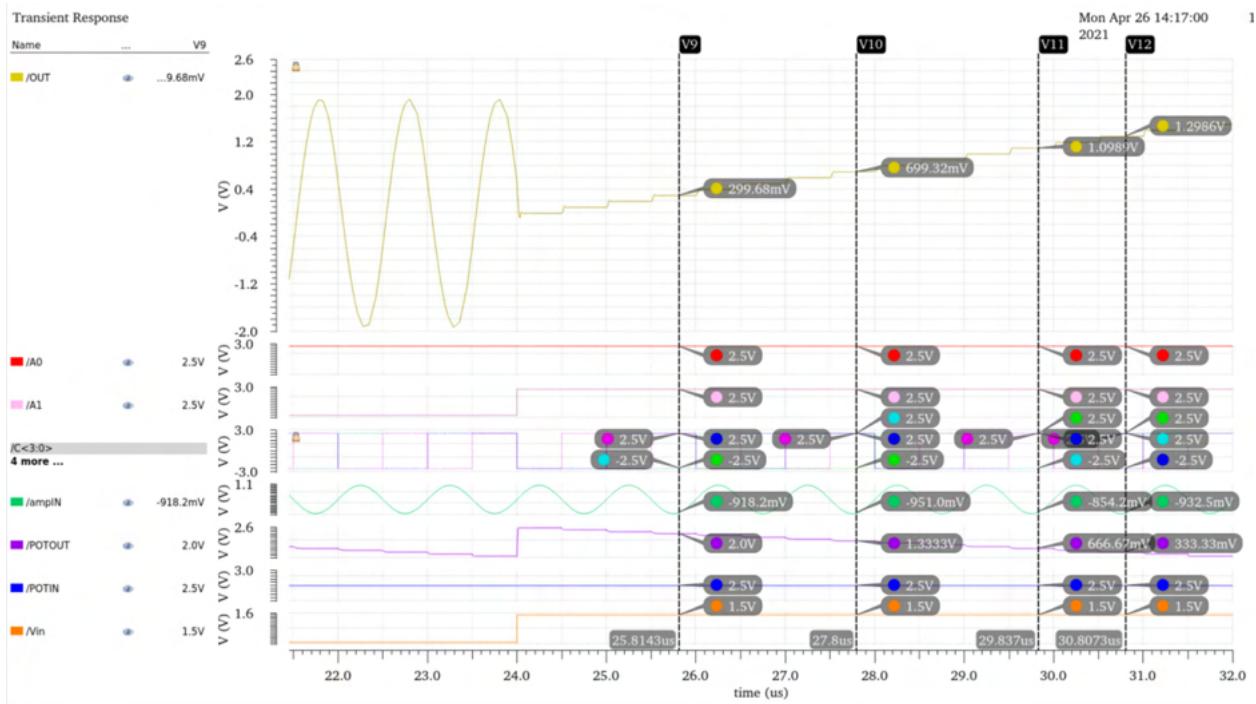


Figure 8.8 The DAC simulation result

Then we created the layout of the project circuit.(Figure 8.9) which passed the DRC and LVS check (Appendix)



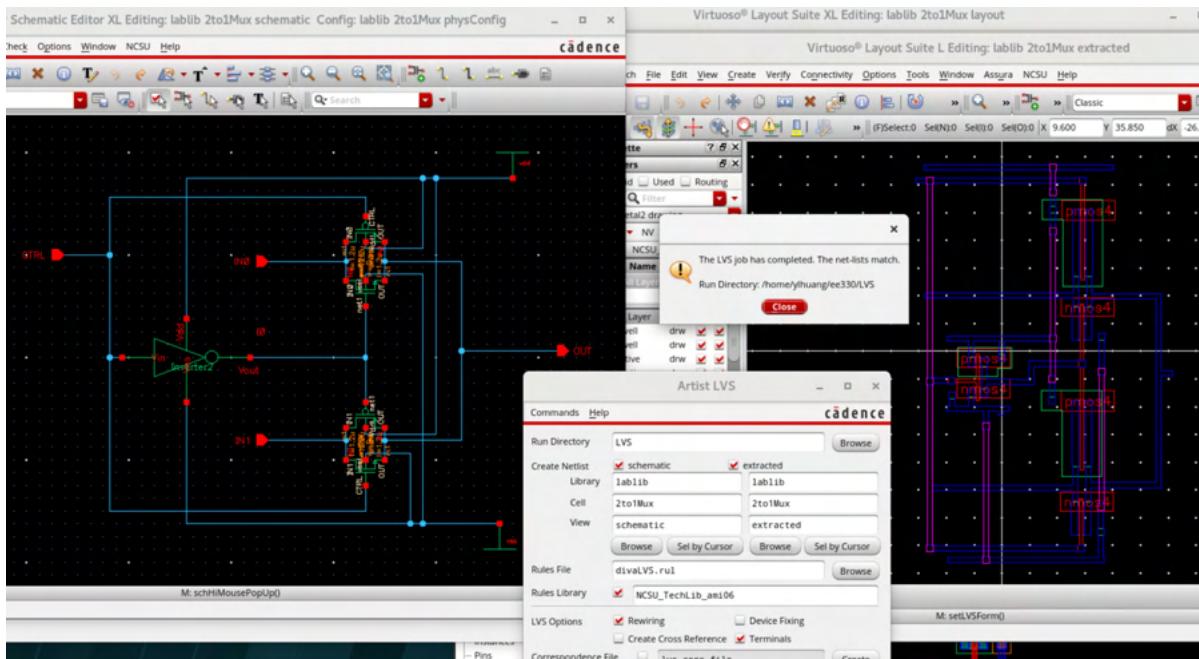
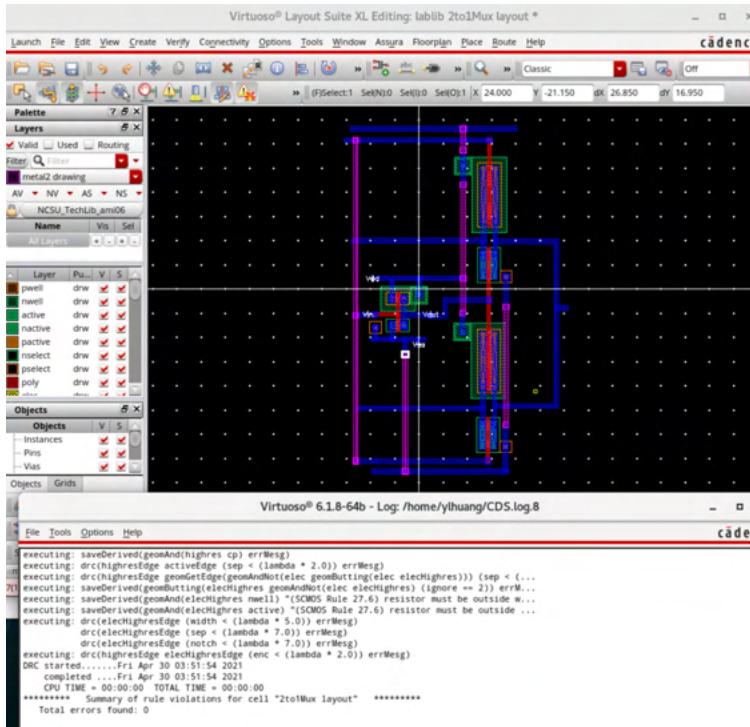
Figure 8.9: The Layout of the project circuit.

9 Conclusion

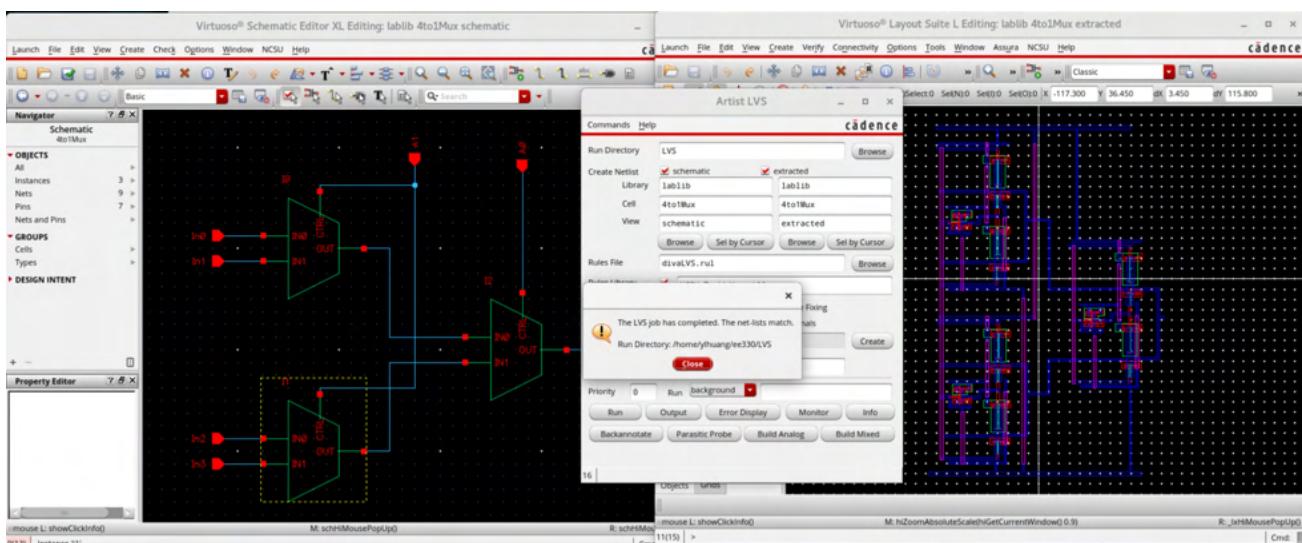
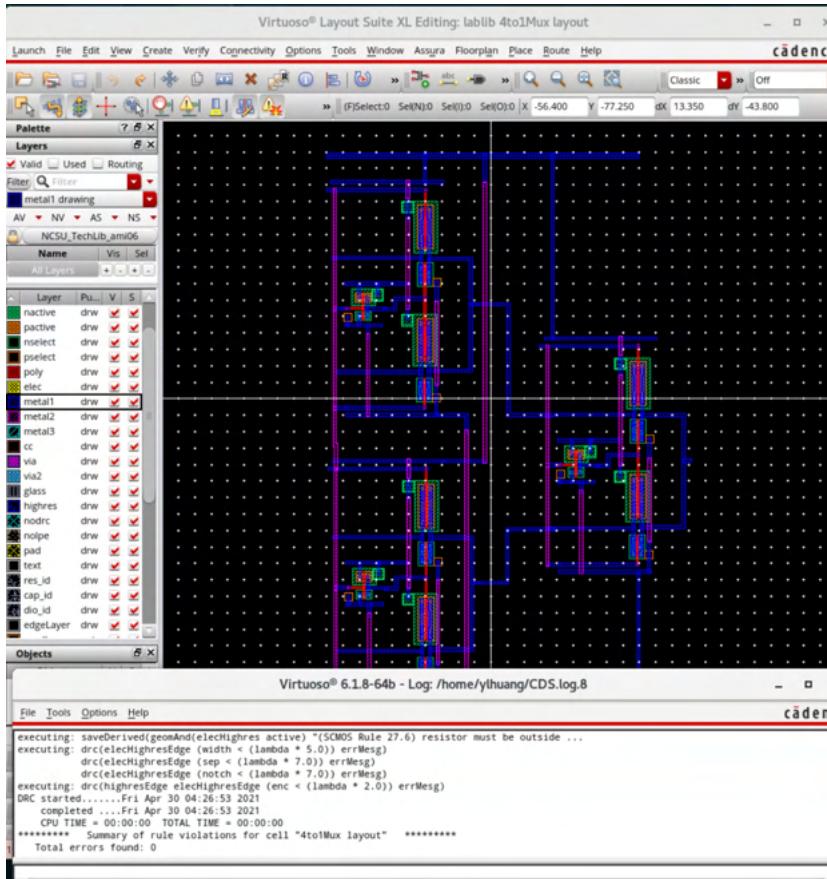
In this project, we made a digital potentiometer, operational amp, Inverting amp and non-Inverting amp, DAC, 2to1 MUX, 4to1 MUX, and we finally we put them together and consisted the Final Project circuit. We successfully made every individual component, and then we put them together also worked as we expected. Then we created the layout of each component and connected them together as the final project circuit design. From this project, we learned a lot of things and faced some realist issue. We found out about transmission gate when making the computerized potentiometer and MUX and how those can be utilized to control the association of the analog signal. We figured out how to make a digital potentiometer that has its wiper powered by the digital input. Also, we figured out how to make and measure the semiconductors for the operational amplifier. Moreover, we found out about DACs with consisted by the digital potentiometer and the op amps. By doing this project and taking this class let us learned some basic knowledge of the integrated circuit. Thus, we can get a better understanding and get ready for the next level of the integrated circuit classes in the future. Also, for this project we used 3 OP-amps which are really cost of power. To improve it, we can use only one OP-amps connect with Potentiometer by adding a selector to determine what function that we could be used. Moreover, we believe that we can build more complexed circuits with less cost and low power dissipation.

Appendix

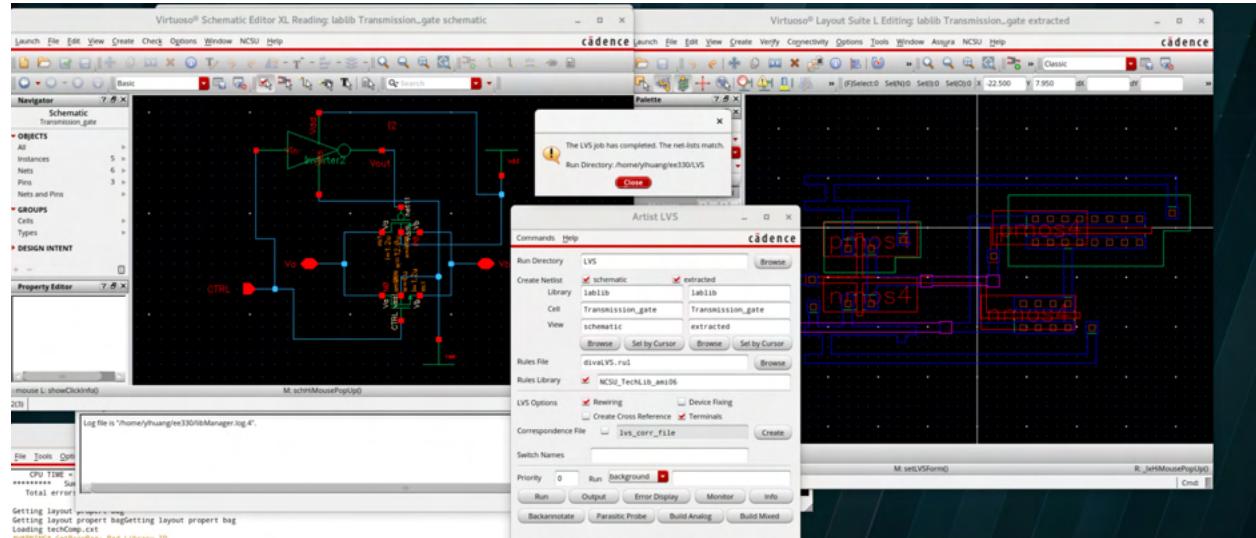
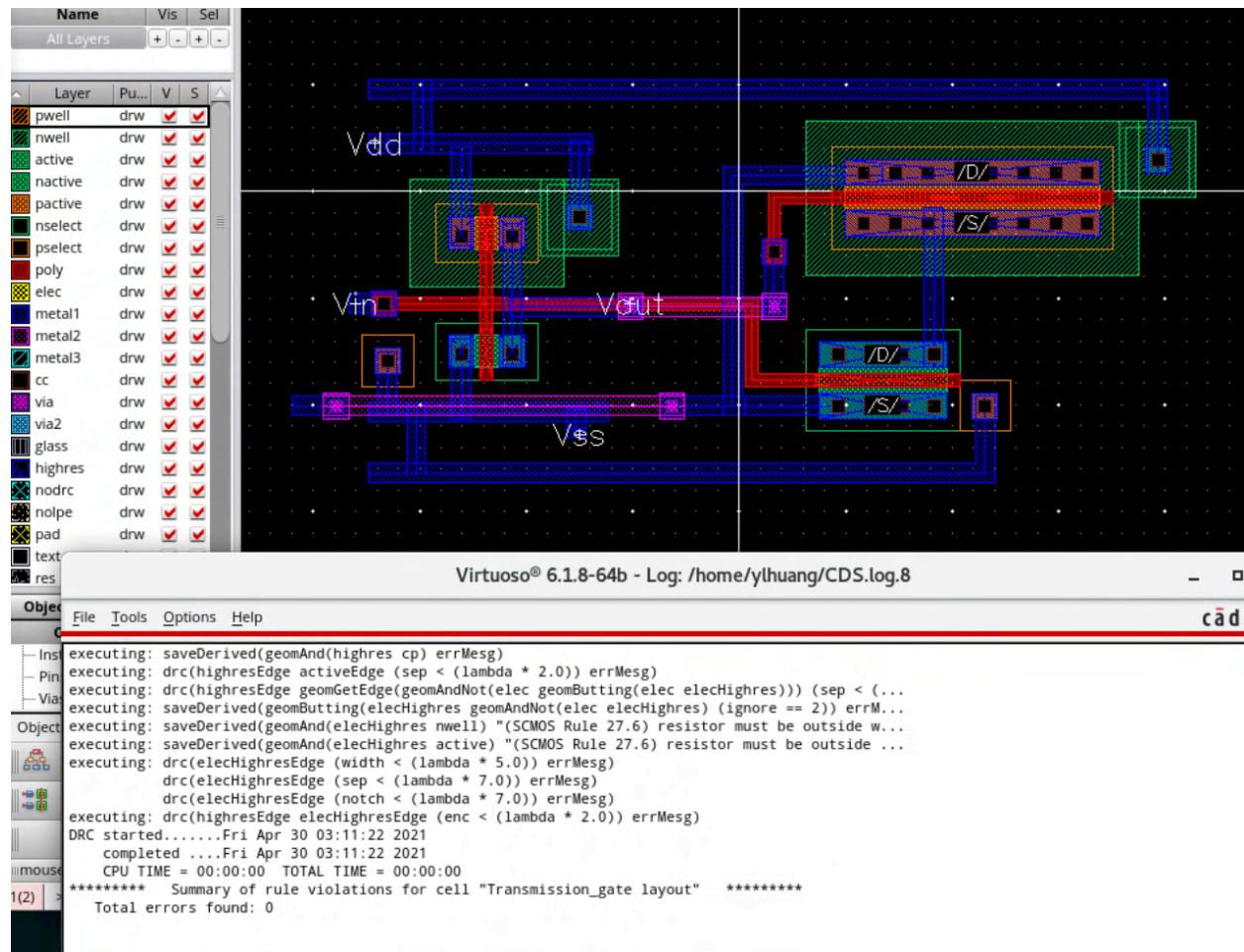
2-to-1 MUX (DRC and LVS)



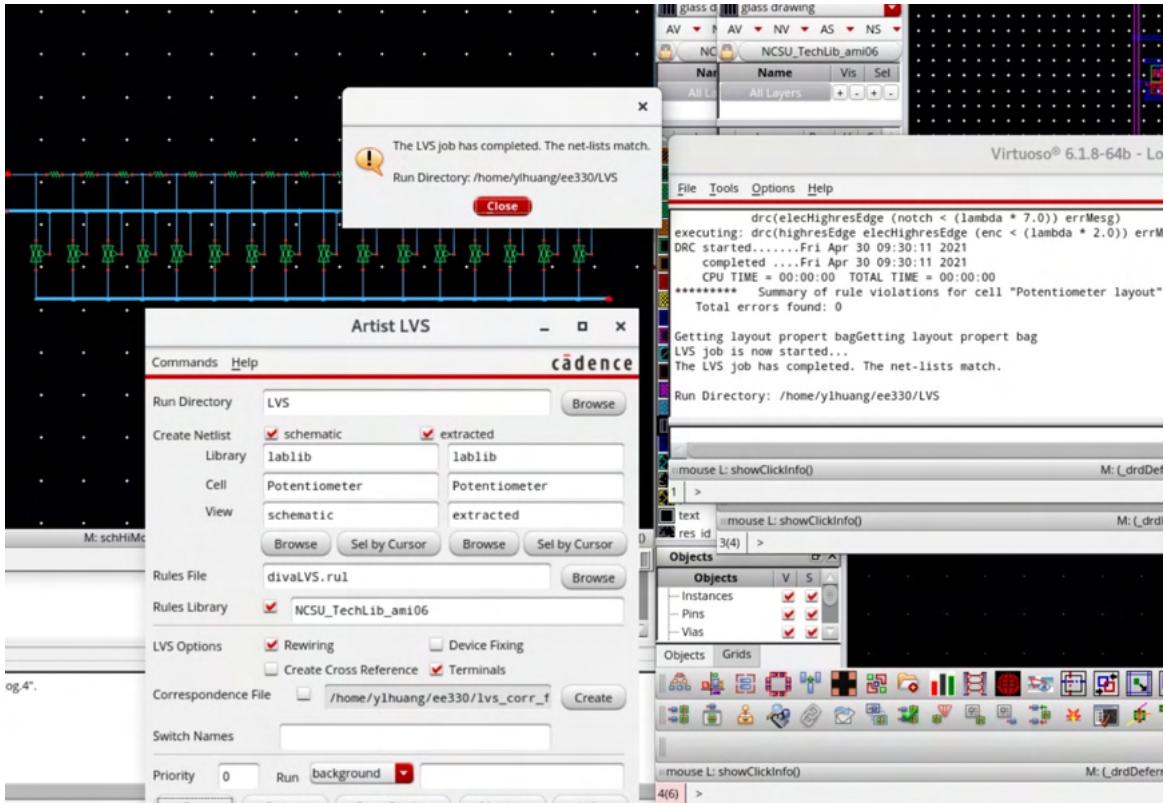
4-to-1 MUX (DRC and LVS)



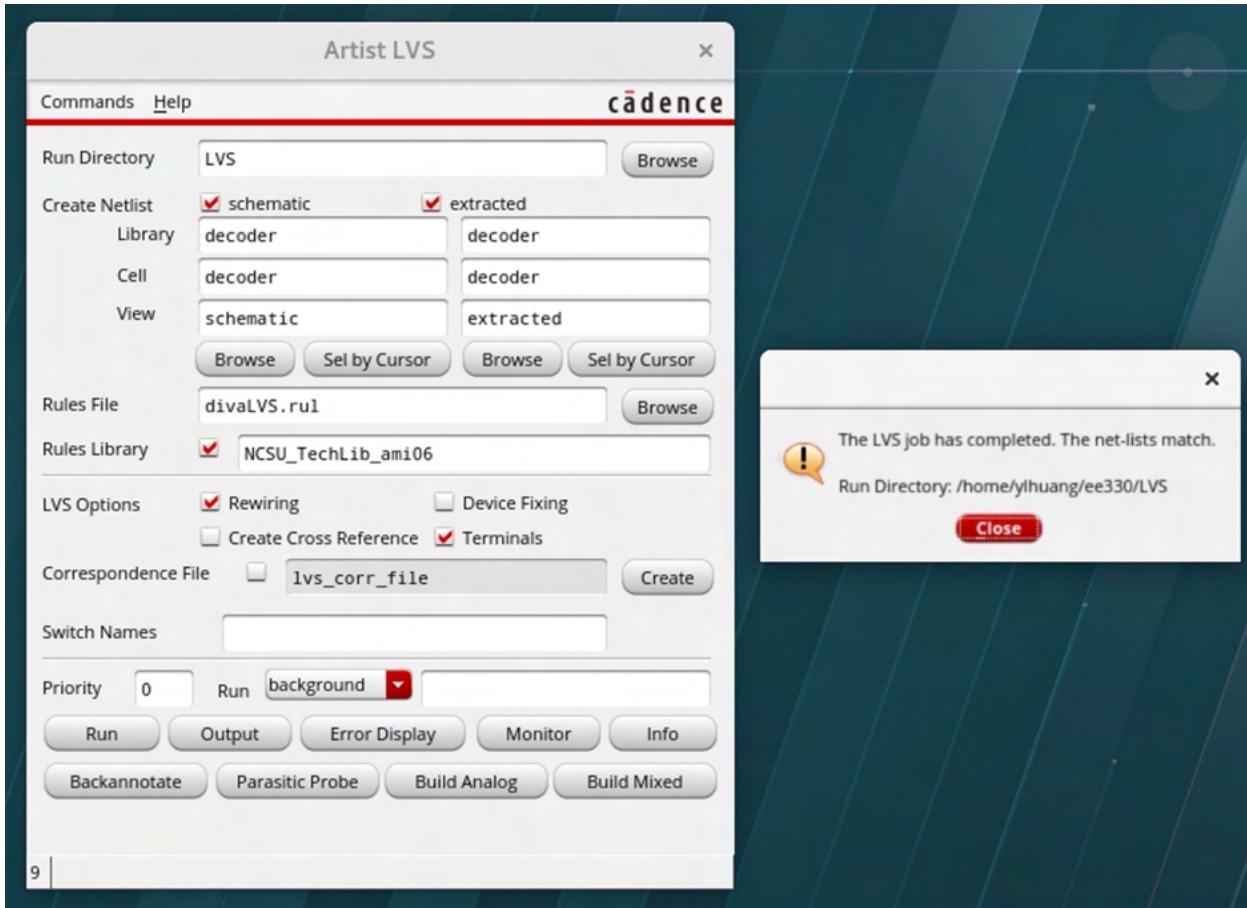
Transmission gate (DRC and LVS)



Potentiometer (DRC and LVS)



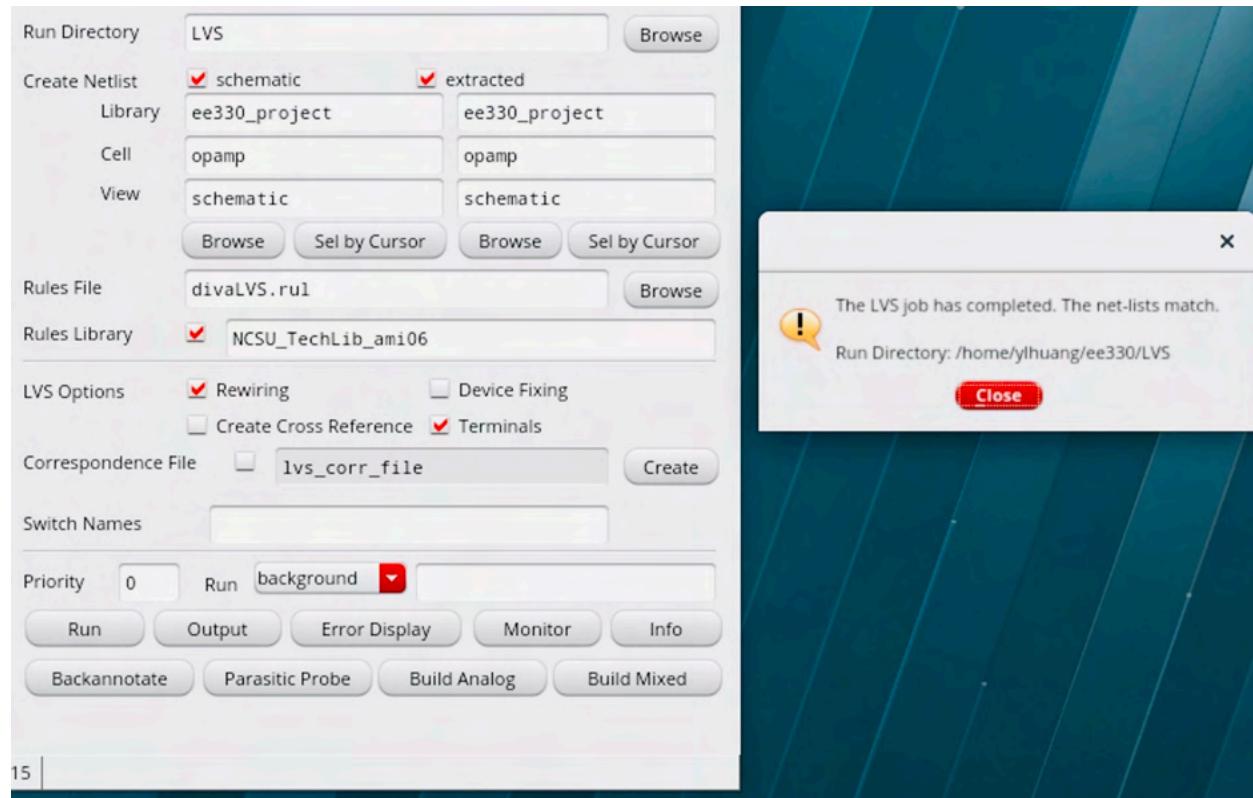
Decoder (DRC and LVS)



```
DRC started.....Fri Apr 30 07:41:55 2021
completed ....Fri Apr 30 07:41:55 2021
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "decoder layout" *****
Total errors found: 0
```

Getting layout propert bagGetting layout propert bag

OP-AMP (DRC and LVS)



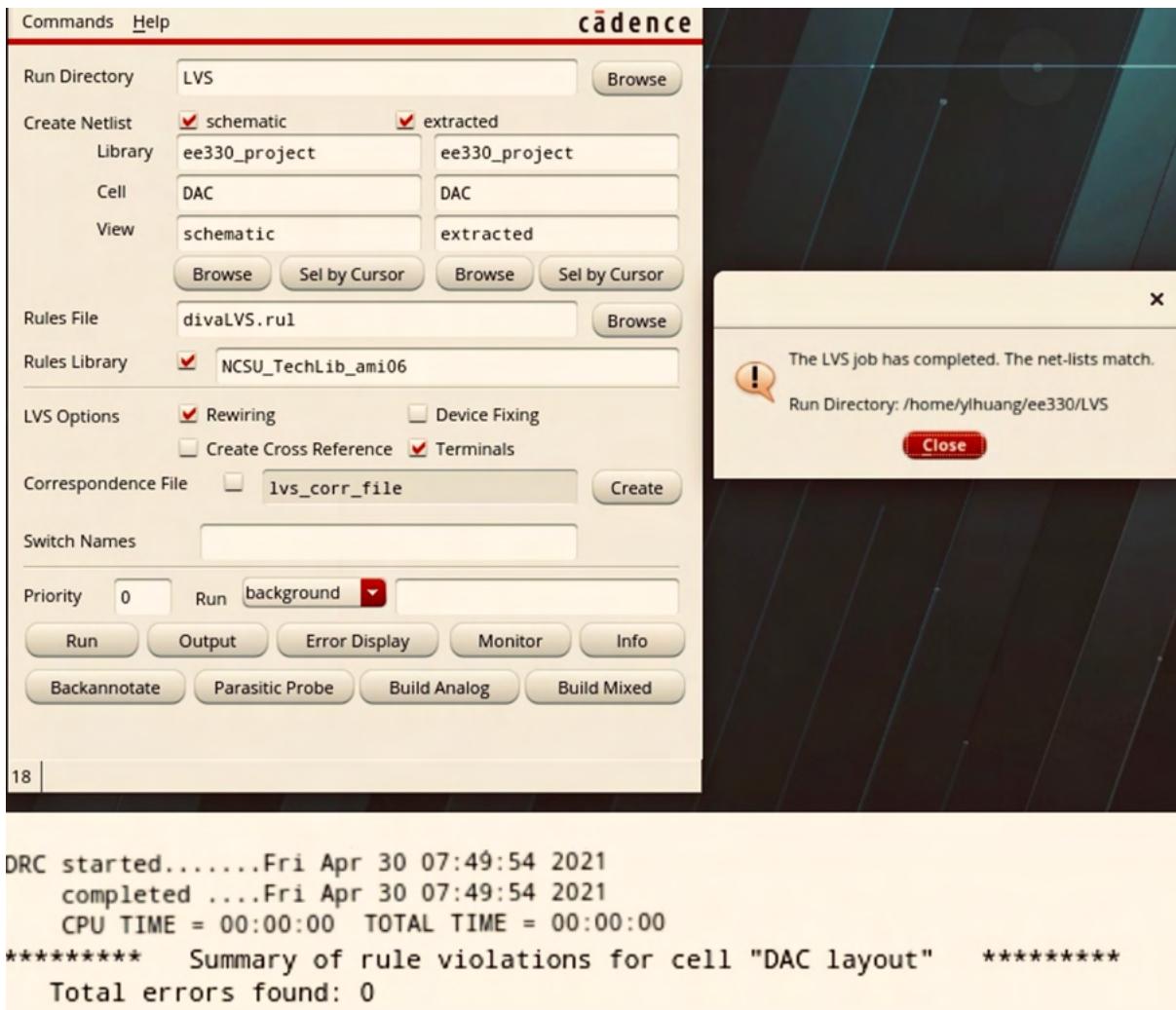
The screenshot shows the Cadence Virtuoso interface with the LVS setup dialog open. The dialog contains the following settings:

- Run Directory: LVS
- Create Netlist: schematic extracted
- Library: ee330_project
- Cell: opamp
- View: schematic
- Rules File: divaLVS.rul
- Rules Library: NCSU_TechLib_ami06
- LVS Options: Rewiring Device Fixing
 Create Cross Reference Terminals
- Correspondence File: lvs_corr_file
- Switch Names: (empty)
- Priority: 0
- Run: background
- Buttons: Run, Output, Error Display, Monitor, Info, Backannotate, Parasitic Probe, Build Analog, Build Mixed

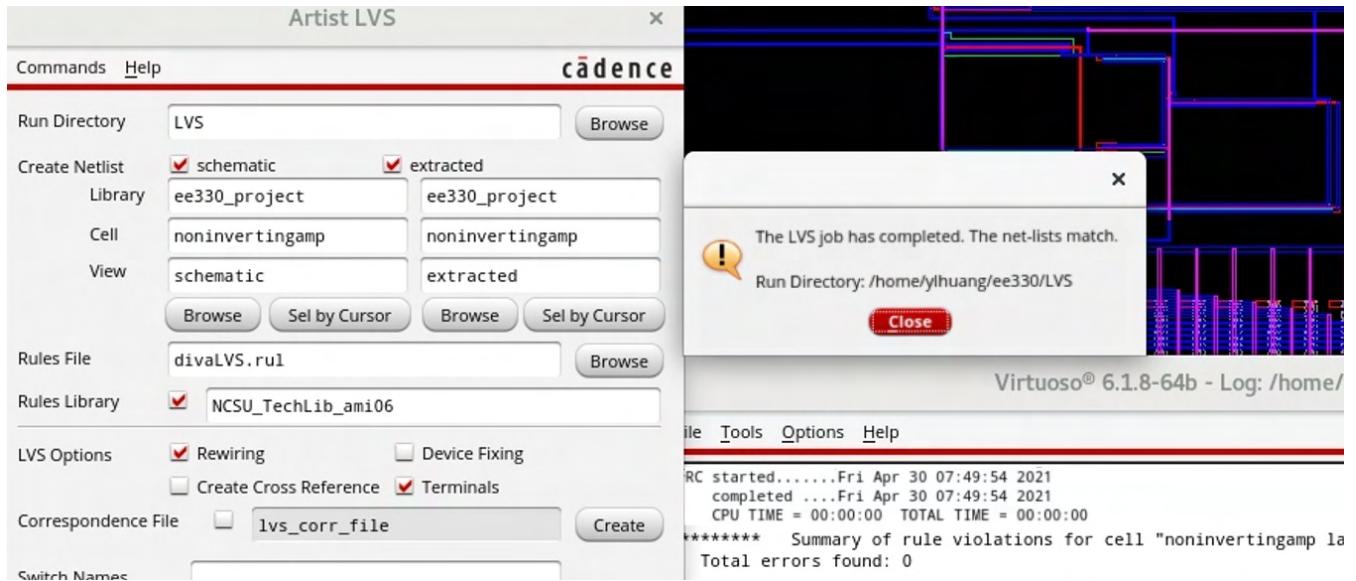
Below the dialog, a terminal window displays the following output:

```
15 |  
|>DRC started.....Fri Apr 30 07:45:59 2021  
| completed ....Fri Apr 30 07:45:59 2021  
| CPU TIME = 00:00:00 TOTAL TIME = 00:00:00  
***** Summary of rule violations for cell "opamp layout" *****  
Total errors found: 0
```

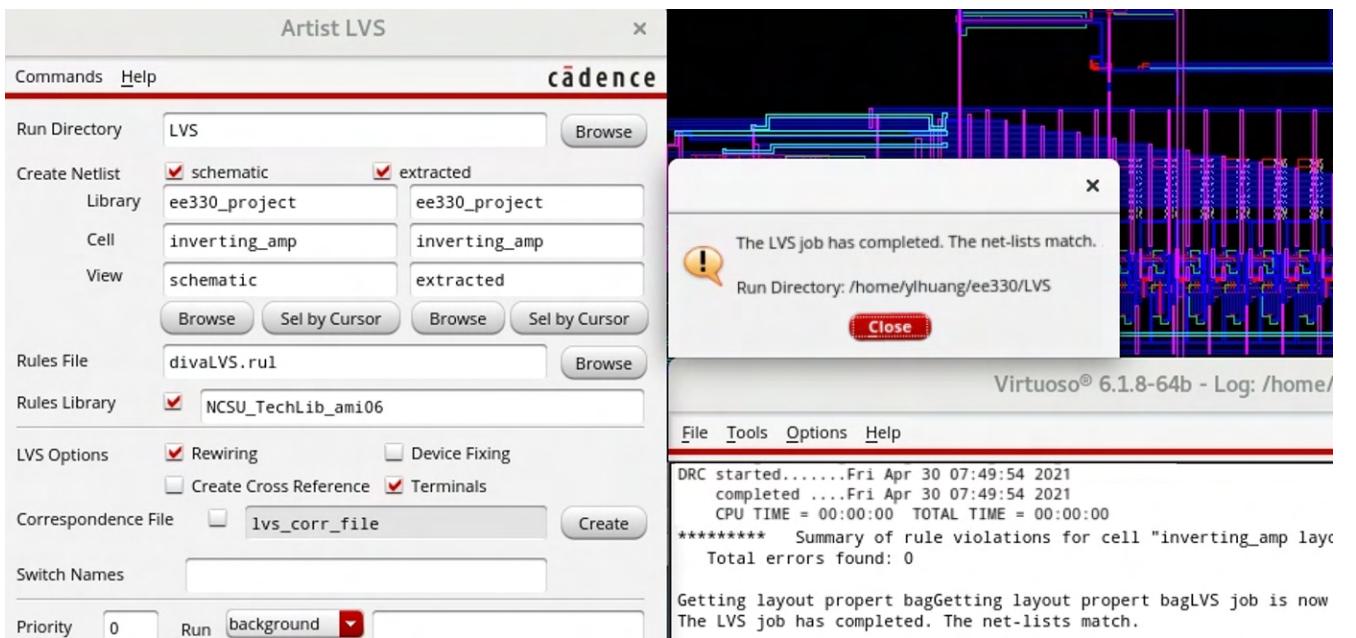
DAC (DRC and LVS)



Non-Inverting Amplifier (DRC and LVS)



Inverting Amplifier (DRC and LVS)



Project Circuit (DRC and LVS)

