Intan Technologies Rhythm version 1.4 release notes

26 February 2014

FPGA Verilog code:

Added the ability to control both the amplifier fast settle function and the auxiliary digital output pins **auxout** in near-real-time using selected TTL digital inputs as control signals. Added **ep44trigin** to transfer parameters related to real-time control of amplifier fast settle function. Added **ep44trigin** to transfer parameters related to real-time control of auxiliary digital output pins on RHD2000 chips. (See the Version 1.4 Rhythm documentation for more details on these new functions.)

C++ API:

Rhd2000EvalBoard class:

Added new functions **enableExternalFastSettle**, **setExternalFastSettleChannel**, **enableExternalDigOut**, and **setExternalDigOutChannel** to control the new functions described above. Also added function **getCableDelay** and modified function **setCableDelay**.

Modified functions **setCableLengthMeters** and **estimateCableLengthMeters** to improve cable length estimation based on detailed measurements of SPI interface cable properties.

Rhd2000Registers class:

Added function **createCommandListUpdateDigOut** to support real-time control of auxiliary digital output pin on chips.

Intan Technologies Rhythm version 1.3 release notes

10 December 2013

FPGA Verilog code:

Added eight low-latency digital threshold comparators and optional high-pass filters to the DAC output modules defined in **DAC_output_scalable.v**. Added hardware signed multiplier block with 18-bit inputs and 36-bit input (**multiplier_18x18.v**) to implement digital high-pass filter. Changed **ep1fwirein** to a multi-purpose input word, with **ep43trigin** used to trigger reading comparator threshold parameters using this input word and **ep44trigin** used to set high-pass filter parameters. The bit **ep00wirein[3]** now determines if the output signals of the eight threshold comparators are routed to Digital Outputs 0-7. (See the Version 1.3 Rhythm documentation for more details on these new functions.)

Defined four previously unused FPGA pins as digital inputs to set a “board mode” number that can be returned to the host computer.

C++ API:

Rhd2000EvalBoard class:

Added functions **setTtlMode**, **enableDacHighpassFilter**, **setDacHighpassFilter**, **setDacThreshold**, and **getBoardMode** to control the new functions described above.

Intan Technologies Rhythm version 1.2 release notes

20 September 2013

FPGA Verilog code:

No changes.

C++ API:

Rhd2000EvalBoard class:

Fixed unit conversion bug in **setCableLengthFeet** function. (Feet-to-meters conversion factor was off by a factor of ten.)

Rhd2000Registers class:

Updated registers to support 64-channel RHD2164 chip. Expanded number of amplifiers that can be powered up/down from 32 to 64; added support for registers 18-22. Changed command list in **createCommandListRegisterConfig** to program registers 18-22.

Intan Technologies Rhythm version 1.1 release notes

1 March 2013

FPGA Verilog code:

Fixed bug in **main.v** related to DAC output: In the main state machine in state **ms_wait**, changed "channel_MISO <= 2;" to "channel_MISO <= 33;"

Added variable gain and "audio noise slicing" capabilities to DAC outputs. Created new file, **DAC_output_scalable.v**, to define a new module **DAC_output_scalable**, which has two additional inputs: **gain[2:0]** and **noise_suppress[6:0]**. The **gain** variable scales the DAC signal in powers of two. The **noise_suppress** variable slices out a region of noise near zero to improve audibility of neural spikes. If both of these inputs are set to zero, the new DAC module behaves identically to the old module. The gain of all eight DACs is now controlled by **ep00wirein[15:13]** via the wire **DAC_gain**. The noise slicing region for the first two DACs (i.e., the DACs connected to the left and right audio line out jack on the evaluation board) is controlled by **ep00wirein[12:6]** via the wire **DAC_noise_suppress**.

C++ API:

Rhd2000EvalBoard class:

Fixed bugs in **disableDataStream** and **enableDataStream** functions.

Changed function **open** to return int (error code) instead of bool.

Added functions **setDacGain** and **setAudioNoiseSuppress** to control the new DAC functions described above.

Added function **fifoCapcityInWords** to return the maximum FIFO capacity.

Added functions **estimateCableLengthMeters** and **estimatedCableLengthFeet** to return a (very) rough estimate of cable length given a delay setting.

Added function **getSampleRateEnum** to return the per-channel sampling rate as an enumeration.

Removed function **disableDataStream** and replaced it with a modified **enableDataStream(int stream, bool enabled)** function.

Removed function **disableDac** and replaced it with a modified **enableDac(int stream, bool enabled)** function.

Removed function **clearDspSettle** and replaced it with a modified **setDspSettle(bool enabled)** function.

Increased value of **USB_BUFFER_SIZE**.

Rhd2000Registers class:

Fixed a bug that caused destructor problems in **Rhd2000Registers**: Changed **aPwr** to a **vector<int>** type.

Added functions **enableAux1**, **enableAux2**, and **enableAux3** to enable or disable ADC auxiliary inputs 1, 2, and 3.

Added function **setZcheckDacPower** to power up or down impedance testing DAC.

Removed functions **fastSettleOn** and **fastSettleOff** and replaced them with **setFastSettle(bool enabled)** function.

Removed function **disableDsp** and replaced it with a modified **enableDsp(bool enabled)** function.

Removed function **disableZCheck** and replaced it with a modified **enableZCheck(bool enabled)** function.

Removed functions **powerUpAmp** and **PowerDownAmp** and replaced them with **setAmpPowered(int channel, bool powered)** function.

Datasheet:

Added documentation for all new features listed above.

Added documentation for **Rhd2000EvalBoard::getNumEnabledDataStreams** function, which was included in version 1.0 API code but missing in version 1.0 documentation.