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Selective release of InP heterostructures from InP substrates

Tzu-Hsuan Chang, Wenjuan Fan, Dong Liu, Zhenyang Xia, and Zhenqiang Ma[a)]
Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 3445 Engineering Hall, Engineering Drive, Madison, Wisconsin 53706

Shihchia Liu, Laxmy Menon, Hongjun Yang, and Weidong Zhou[b)]
Department of Electrical Engineering, University of Texas at Arlington, 202A NanoFAB Center, 500 South Cooper Street, Arlington, Texas 76019

Jesper Berggren and Mattias Hammar
KTH-Royal Institute of Technology, School of Information and Communication Technology, Electrum 229, Kista 16440, Sweden

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The authors report here a method of protecting the sidewall for the selective release of InGaAsP quantum-well (QW) heterostructure from InP substrates. An intact sidewall secured by SiO_2 was demonstrated during the sacrificial layer selective etching, resulting in the suspended InGaAsP QW membranes which were later transferred to the Si substrate with polydimethylsiloxane stamp. The quality of the transferred InGaAsP QW membranes has been validated through photoluminescence and EL measurements. This approach could extend to arbitrary targeting substrate in numerous photonics and electronics applications. © *2016 American Vacuum Society*.
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I. INTRODUCTION

Crystalline semiconductor nanomembranes (NMs) have great potentials when integrated with optic and electronic applications due to their flexibility, thinness, and transferability.[1] Traditionally, they are fabricated via wafer bonding or direct growth. Wafer bonding as the most prevailing approach requires extrinsic force and excessively high temperature in order to achieve the surface bonding energy. On the other hand, lattice mismatch and incompatibility have limited the application of the direct growth method. Moreover, both wafer bonding and direct growth techniques face challenges such as scaling the wafer size and inefficient use of the substrate.

In the past decade, the epitaxial lift-off method has attracted great attention to facilitate the formation of single-crystal, defect-free high-quality semiconductor NMs.[2] In this approach, epitaxial thin film NMs are lifted off from the lattice-matched growth substrates by taking advantage of the high etching selectivity between the sacrificial layer and the functional membrane structure. In 1987, Yablonovitch *et al.* has successfully released AlGaAs film with AlAs as the sacrificial layer from lattice-matched GaAs substrates by using Apiezon black wax to protect the AlGaAs film and to facilitate peeling of the film after release from the substrate.[3,4] However, black wax is not applicable in the photolithography process because of limited flexibility. On the other hand, the transparent Mylar diaphragm as an intermediate transfer medium must be used for alignment, which further complicates the process.

An alternative approach is performed through the post-transfer process using standard lithography and etching technology. Recently, the utility of polydimethylsiloxane (PDMS) as the transfer medium was reported,[5] including demonstrations of flexible photodetectors, and high speed thin-film transistors and biosensors.[6–9] Significant progress has been made by our previous work on transfer printed membrane lasers, consisting of a transferred InGaAsP QW heterostructure membrane, sandwiched in between two single-layer crystalline silicon photonic crystal Fano resonance membrane reflectors on an SOI substrate.[10] The incorporation of InGaAsP QW membrane broadens the application of transferrable optical electronics that features a working wavelength at 1550 nm. However, InGaAsP QWs that are vulnerable to hydrofluoride solution can only be protected with black wax and transferred locally in a small area.

In this paper, we report experimental demonstration of sidewall protection processes for the selective release of InGaAsP QW heterostructures from InP substrates. The design protection structures were compatible with the standard PDMS printing process, and the large area of InGaAsP QW nanomembranes was successfully printed to the Si substrate.

II. EXPERIMENT

The standard InGaAsP QW heterostructure wafers were grown on (001) n-InP substrate by metal organic chemical vapor deposition. Table I shows the description of the InGaAsP QW structure and current existing etching tables of the relative etchant and protection layer. A 500 nm-thick InGaAs layer was first grown on an InP substrate followed by another 500 nm InP layer. The intrinsic active region consisting of eight strain-compensated InGaAsP quantum-wells (QWs) is sandwiched in between doped p- and n-InP claddings. Besides the economic consideration of reusable substrates, the undercut etch rate of InP is very small except for the (001) planes.[11] InGaAs with a less rigid requirement for the structural orientation and a high selectivity to InP is thus used as the sacrificial layer in this heterostructure. Layer 2 of

[a)]Electronic mail: mazq@engr.wisc.edu
[b)]Electronic mail: wzhou@uta.eduu

TABLE I. InGaAsP QW structure and etching tables of the relative etchant and protection layer.

Layer	Description	Material	Dopant	Thickness (nm)
7	Contact layer	InGaAs	Zn	80
6	Cladding layer	InP	Zn	88
5	Quantum wells (1 × 8)	InGaAsP	Undoped	127.5
4	Cladding layer	InP	Si	88
3	Contact layer	InGaAs	Si	80
2	Protect layer	InP	Si	500
1	Sacrificial layer	InGaAs	Si	500
0		InP substrate (n+)		

InP is used as a stop-and-protect layer during removal of the InGaAs sacrificial layer.

The process required to release and transfer InGaAsP QW nanomembranes is different from the current prevailing HF-based wet etching and releasing methods, which have been applied in releasing IV- and GaAs-based nanomembranes. For releasing IV group materials, such as Si, Ge, or SiGe, on SiO_2 as shown in Table II, no protection material is required during sacrificial layer etching due to the extremely high selectivity in HF solution. As for the GaAs-based nanomembrane release, photoresist has been used as a sidewall protection material to secure the AlInGaAs QW heterostructures during removal of the underlying $Al_{0.95}Ga_{0.05}As$ sacrificial layer from the GaAs substrate in HF solution.[12] AlInGaAs QW heterostructures are released from GaAs substrates and transferred to Si substrate with precise lithographic alignment and a low thermal budget, while also making efficient use of the III–V epitaxial material.[12] Different from releasing the AlInGaAs QWs, the InGaAsP QW structure has lower chemical resistivity to HF. Figure 1 demonstrates the etching results of the designed InGaAsP QW structures targeting at 1550 nm wavelength in $HF:H_2O_2:H_2O$ etch solution with a volume ratio of 1:1:10. As shown in Fig. 1(a), the high HF permeability bypasses the photoresist protection and attacks the vulnerable QW structures underneath. Also, the n contact InGaAs (layer 3) is also etched as seen in Fig. 1(b). So, it is concluded for the protection of the photoresist, the etch rate of each designed functional layer cannot be ignored and could significantly jeopardize the performance after transfer.

TABLE II. Sacrificial layer and etchant used for different material membranes lift-off.

Type	Membrane layer	Sacrificial layer	Etchant
(a) Direct etch	Si	SiO_2	HF
	Ge	SiO_2	HF
	SiGe	SiO_2	HF
(b) Photoresist protection	GaAs	AlGaAs	$HF:H_2O$
(c) Hard mask protection	InGaAsP/InP	InGaAs	$H_2SO_4:H_2O_2:H_2O/H_3PO_4:H_2O_2$
	InP	InGaAs	$H_2SO_4:H_2O_2:H_2O/H_3PO_4:H_2O_2$
	InGaAsP	InGaAs	$H_2SO_4:H_2O_2:H_2O/H_3PO_4:H_2O_2$

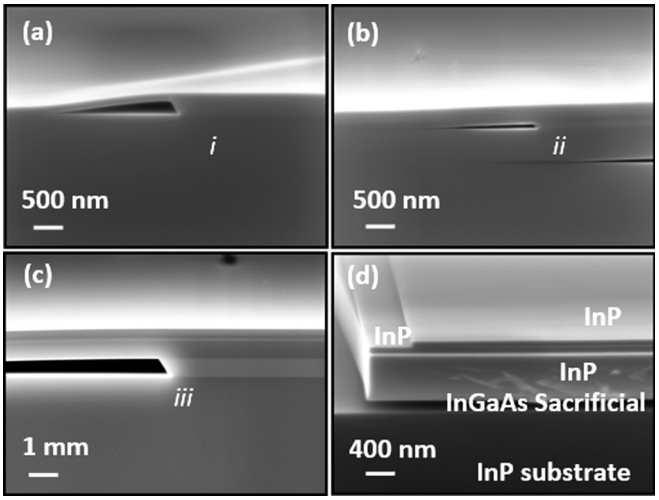

FIG. 1. Cross-section SEM images of the InGaAsP QWs after 3 h in $HF:H_2O_2:H_2O$ (1:1:10) solution with resist Shipley 1827 as sidewall protection. (d) All InGaAs(P) layers were etched, with zoom-in images in (a) layer 5 (127 nm intrinsic InGaAsP QWs), (b) layer 3 (80 nm n-InGaAs), and (c) layer 1 (500 nm n-InGaAs), with etching rates of 1.6 μm/3 h, 4.3 μm/3 h, and 11.3 μm/3 h, respectively.

To solve the strong infiltration issue of the HF wet etching method, we proposed a non-HF etching system using $H_3PO_4:H_2O_2$. By using a weaker acid like phosphoric acid, the protection layer could be introduced to protect the QWs. In Fig. 2, the transfer procedure of InGaAsP QW membranes with SiO_2 sidewall protection is demonstrated. SiO_2 is resistant to the $H_3PO_4:H_2O_2$ etching system and can be easily removed by CF_4 plasma etching or short time buffered oxide etchant (BOE) wet etching without attacking the InGaAsP QW heterostructures. The SiO_2 films grown by thermal oxidation, plasma-enhanced chemical vapor deposition (PECVD), and sputtering have been widely used in semiconductor device technology. The high temperature during the thermal oxidation process could damage the InGaAsP based QW structures. For PECVD SiO_2 deposition, temperature is within the acceptable range for III–V material around 200–400 °C. However, the temperature difference between deposition and cooldown causes the internal stress and the pinholes in the deposited film.[13] Consequently, the built-up stress will result in curving up of the released InGaAsP QWs membrane and the pinholes in the PECVD oxide create paths for the acid to penetrate into covered area during the long time undercut etching process. To avoid the high processing temperature, built-in strain, and pinhole problems from thermal oxidation and PECVD process, the sputtering process is thus chosen for our purpose due to the advantages of low-temperature, uniform and conformal coating, and good adhesion between the film and the substrate.

It is the first time that SiO_2 is used as a sidewall protection material in the InGaAsP epitaxial membrane lift-off process. The thickness of the SiO_2 has been optimized to secure the sidewall of the InGaAsP epitaxial membrane in a non-HF etching system. By properly controlling the volume ratio of $H_3PO_4:H_2O_2$, the InGaAs sacrificial layer can be selectively removed. Based on the transfer printing process, the

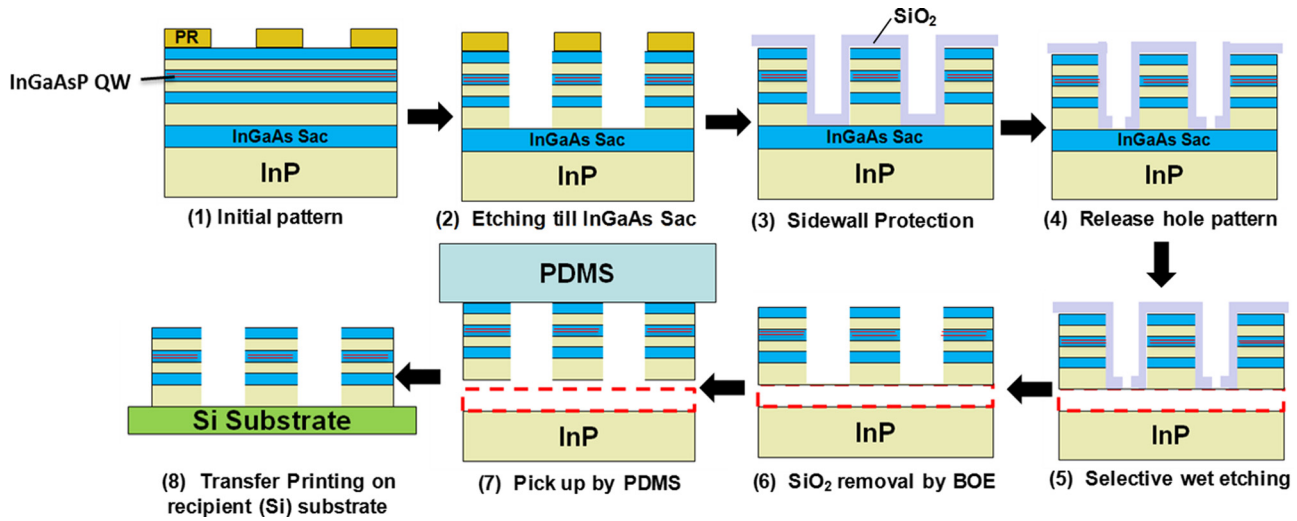

FIG. 2. (Color online) Schematic illustration of the procedure used to transfer InGaAsP QW membranes.

suspended InGaAsP epitaxial membrane is lifted off from the InP substrate. The strategy not only avoids the lattice mismatch and stringent surface requirement but also improves the reproducibility of III–V materials.

III. DEVICE FABRICATION AND RESULTS

The SiO_2 films were deposited by Denton Discovery 24 sputtering system, using a 3-in. diameter SiO_2 target in argon atmosphere at 20 mTorr with RF power of 540 W. The deposition was under vacuum of 2×10^{-6} mTorr with a deposition rate of 0.8 Å/s. As shown in Fig. 3(a), the SiO_2 film is uniformly coated on the edge of the heterostructure. Note that the steps were caused by underetching during the first release-hole structure wet etching. After coating the heterostructures with SiO_2, a second release-hole is patterned using optical lithography followed by reactive-ion etching to open the release holes. To generate membranes, the heterostructures were immersed in H_3PO_4:H_2O_2 (2:1) solution for 2 h, with its cross-sectional SEM image shown in Fig. 3(b). The InGaAs sacrificial layer is etched laterally under constant potential conditions, resulting in suspended InGaAsP QW membranes. Figures 3(c) and 3(d) show the zoomed-in optical images of the sidewall edge and center area between the release holes after undercut etching and printing on Si substrate, respectively. After release of the InGaAs sacrificial layer, SiO_2 can be easily etched away in BOE solution without attacking the III–V materials, leaving behind a high-quality, multilayer, and reusable InP substrate.

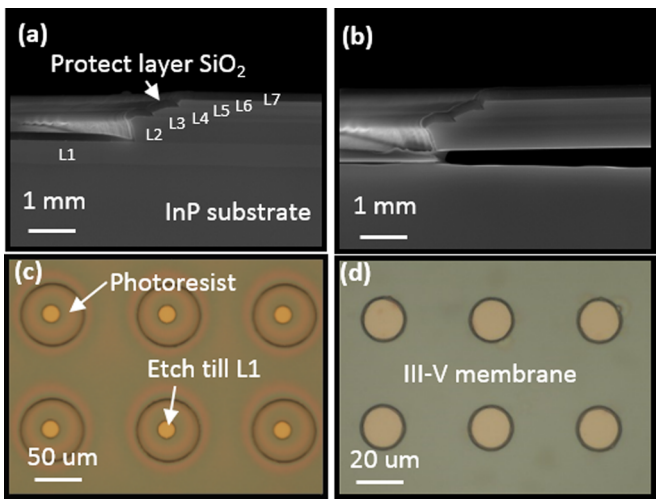

FIG. 3. (Color online) Cross-sectional SEM image of the seven-layer III–V membrane (a) before and (b) after release with sidewall protection. Optical image of III–V membrane (c) before and (d) after transfer onto Si.

To verify the quality of the InGaAsP QW membranes, we fabricated InGaAsP QWs photodiodes transferred on top of the Si substrate, as shown in Fig. 4(a), and compared the QWs membrane by both the PL and electroluminescence (EL). The PL results in Fig. 4(b) give the comparison between InP substrate (before transfer), InGaAsP QWs transferred on Si substrate with sidewall protection, and the one using the photoresist and HF transfer method. It is clearly seen that with SiO_2 protection transfer, the PL peak wavelength and intensity shows negligible differences with the epilayer structure, which indicates no degradation of the QWs. Instead, the PL of the QWs using the photoresist as a protection methods and HF as the etching acid shows degradation after the QWs membrane is transferred. As the permeability of HF solutions is significant, the QWs are partially etched during the releasing process.

Whereas the PL of the membrane with HF transfer methods showed a red-shift and reduction in intensity. To further compare the QW performance, Ohmic contact metal is placed on both sides of the contact layer. The DC and EL results are measured in Figs. 4(c) and 4(d). The diode shows a good static curve at DC bias from -2 to $+2$ V. No significant degrading of the QWs has been identified. The EL curve is measured under a forward current of 5 mA. The light emitting from the QW membrane on the Si substrate remains similar to the results on the InP substrate but slightly stronger. This may be due to the increased upward reflection from the Si substrate (refractive index n: 3.47) compared with the original InP substrate (n: 3.17). Overall, the performance of

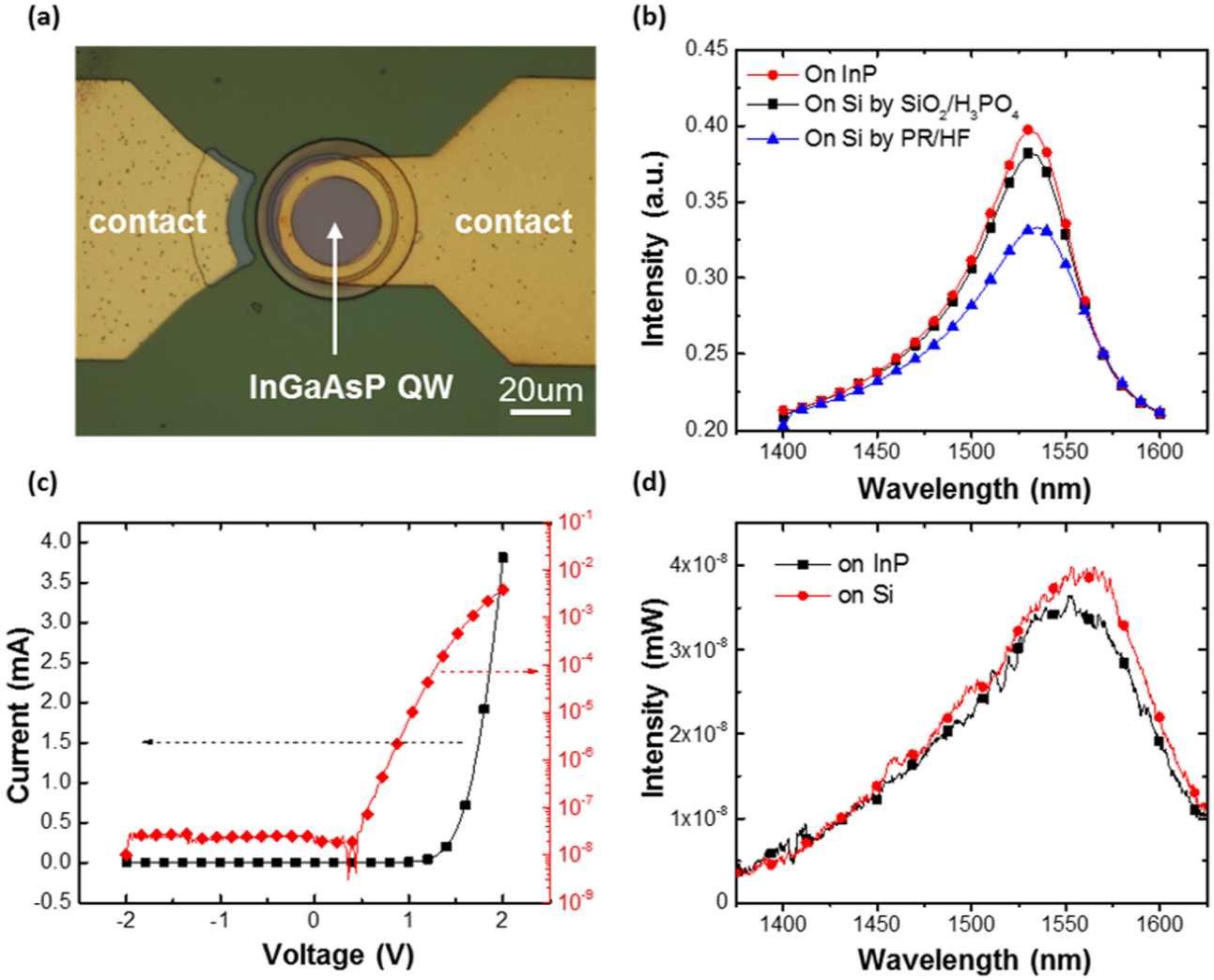

FIG. 4. (Color online) InP QW optical and electrical properties after side-wall protection transfer process. (a) Optical image of the fabricated InGaAsP QW photodiode embedded on Si substrate, (b) PL results of InP QWs on InP substrate, released onto Si substrate with sidewall protection, and released to Si substrate using photoresist/HF methods. (c) DC characteristic of the InP QWs after transferred onto Si substrate (d) EL results of InP QWs on InP substrate and released onto Si substrate at input current 5 mA.

the InGaAsP QW is well-maintained in the proposed transfer method.

IV. CONCLUSIONS

In conclusion, InGaAsP QWs heterostructures have been successfully released by SiO_2 sidewall protection in H_3PO_4:H_2O_2 solution. The technological processes are applicable in more material systems, which can open new possibilities for integrating III–V technology with arbitrary substrates, such as vertically stacked high-density photonic/electronic integration and high-performance flexible/conformal photonics.

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