Microelectronics Journal 42 (2011) 509–514

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

RF model of flexible microwave single-crystalline silicon nanomembrane PIN diodes on plastic substrate

Guoxuan Qin [a,b,*], Hao-Chih Yuan [b], George K. Celler [c], Weidong Zhou [d], Jianguo Ma [a], Zhenqiang Ma [b,**]

[a] Tianjin University, School of Electronic Information Engineering, Tianjin 300072, PR China
[b] University of Wisconsin-Madison, Department of Electrical and Computer Engineering, Madison, WI 53706, USA
[c] Soitec USA, 2 Centennial Drive, Peabody, MA 01960, USA
[d] University of Texas at Arlington, Department of Electrical Engineering, Arlington, TX 76019, USA

ARTICLE INFO

Article history:
Received 1 September 2010
Accepted 18 October 2010
Available online 11 November 2010

Keywords:
Flexible PIN diode
Microwave
Modeling
Nanomembrane
Plastic substrate
Radio frequency (RF)
Single-crystalline silicon

ABSTRACT

This paper reports the realization and RF modeling of flexible microwave P-type-Intrinsic-N-type (PIN) diodes using transferrable single-crystalline Si nanomembranes (SiNMs) that are monolithically integrated on low-cost, flexible plastic substrates. With high-energy, high-dose ion implantation and high-temperature annealing before nanomembrane release and transfer process, the parasitic parameters (i.e. resistance, inductance, etc.) are effectively reduced, and the flexible PIN diodes achieve good high-frequency response. With consideration of the flexible device fabrication, structure and layout configuration, a RF model of the microwave single-crystalline Si nanomembrane PIN diodes on plastic substrate is presented. The RF/microwave equivalent circuit model achieves good agreement with the experimental results of the single-crystalline SiNM PIN diodes with different diode areas, and reveals the most influential factors to flexible diode characteristics. The study provides guidelines for properly designing and using single-crystalline SiNMs for flexible RF/microwave diodes and demonstrates the great possibility of flexible monolithic microwave integrated systems.

1. Introduction

There has been increasing enthusiasm on high performance, large-area flexible electronics for the past few years, because of their unique advantages such as bendability, light weight, and conformally attachable to any shape of surfaces [1]. Various applications are now employing the flexible micro- and macro-electronics, including large-area displays, electronic textile/paper, biomedical sensors, etc. [2–6]. Amorphous silicon, organics and polymers, and polycrystalline silicon are the most commonly used materials for the low-speed flexible electronics [1,4,6]. However, due to their poor crystalline quality and carrier mobility, these materials are not suitable for applications that require high-speed and high frequency operations, e.g. RFIDs, portable Wi–Fi devices, flexible airborne/space-borne communication systems, and surveillance and remote sensing radars [1,7]. Recently developed transferrable and flexible single-crystalline Si nanomembrane (SiNM), lifted from silicon-on-insulator: SOI wafers, makes fast electronics possible. The high carrier mobility of SiNMs, which is as high as their rigid bulk wafer counterparts [8–11], makes them promising for very high-frequency applications.

To transform the superior carrier transport characteristics of SiNMs into high-speed thin-film transistors (TFTs), we have developed a unique combined high-temperature and low-temperature process for transferrable SiNMs [11]. This led to the realization of microwave TFTs on a plastic substrate [11,12]. Other than active transistors, in order to build the flexible monolithic microwave integrated circuits, passive components that can be operated at RF/microwave frequency are indispensable. Furthermore, to accurately and efficiently design the flexible microwave integrated circuits, RF/microwave model of the PIN diodes is essential. However, all the available models for PIN diodes are based on bulky rigid wafers, accurate modeling of the novel microwave PIN diodes using single-crystalline SiNMs on plastic substrate is not yet reported.

There are two kinds of models commonly used: physical model and equivalent circuit model. Although a physical model can precisely predict single device 2D or 3D characteristics, it requires abundant numerical complexity [13], thus it is not suitable for circuit designs. On the other hand, an equivalent circuit model can provide sufficiently accurate performance at the device or circuit level, with much fewer model parameters and less computation

* Corresponding author at: Tianjin University, School of Electronic Information Engineering, Tianjin 300072, PR China. Tel.: 86 22 27408761.
** Also Corresponding author. University of Wisconsin-Madison, Department of Electrical and Computer Engineering, Madison, WI 53706, USA.
Tel./fax: 1 608 261 1095.
E-mail addresses: gqin@tju.edu.cn, guoxuanqin@hotmail.com (G. Qin), mazq@engr.wisc.edu (Z. Ma).

0026-2692/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2010.10.012

time. In this paper, we develop an RF/microwave equivalent circuit model for the microwave PIN diodes using transferable SiNMs on plastic substrate. The model provides guidelines for designing and using PIN diodes in flexible MMICs based on single-crystalline Si nanomembranes on plastic substrates.

2. Device fabrication

For the goal of flexible monolithic microwave integrated circuits, the fabrication process of the PIN diodes using transferable SiNMs on plastic substrate is fully compatible with that used to fabricate active transistors (TFTs) [11]. This process allows simultaneous fabrication of the active TFTs and passive PIN diodes on the same plastic substrate.

The process flow is briefly illustrated as shown in Fig. 1. The fabrication process begins with a lightly-doped p-type Si (0 0 1) SOI substrate with a 200-nm Si top layer and 200-nm buried oxide (BOX) layer. Align marks and the lateral n- and p-type regions were formed by optical photolithography. The patterned SOI sample then received ion implantation of phosphorus ions and boron ions, respectively, to form heavily doped n- and p-type regions. The sample was annealed at 850 °C for 45 min in N_2 ambient in a furnace (Fig. 1(a)). The well-controlled high-energy, heavily dosed ion implantation, and high temperature furnace annealing enable low contact and sheet resistance and thus low parasitic effects, which are the critical process steps to fabricate RF/microwave active and passive devices.

The 200-nm Si template layer was then patterned into strips or membrane with array of holes, followed by a plasma dry etching (SF_6/O_2) down to the BOX layer (Fig. 1(b)). After stripping off the photoresist, the sample was put into diluted hydrofluoric acid (HF) to etch away the underlying BOX layer and release the SiNMs weakly bonded on the Si handling substrate wafer via van der Waals forces (Fig. 1(c)) [14].

Then the sample was rinsed thoroughly with DI water and was subsequently brought face-to-face and firmly contacted with a ~175 μm thick polyethylene terephthalate (PET) substrate that was spin-coated with a SU-8 epoxy layer. Since the bonding force between the SiNM and the epoxy is stronger than the Si-to-Si bonding, the SiNM can be lifted off from the SOI substrate (Fig. 1(d)) and flip-transferred onto the PET substrate (Fig. 1(e)). This flip transfer technique makes the displacement of patterned Si-strips as small as possible after they were transferred onto the plastic substrate [12,15]. A UV exposure step was then used to cure the SU-8.

SiNMs were then selectively dry etched into smaller active area regions to further enhance the device flexibility. Finally, metal contacts and interconnects were formed by evaporating and a lift-off process (Fig. 1(f)). The highest temperature applied to the plastic substrates was kept below 120 °C.

The lateral arrangement of the PIN structure in this study has two major advantages: firstly, it allows simultaneous photolithography patterning and n-/p-type ion implantation for active TFTs and passive PIN diodes. Secondly, the lateral structure is not compromising the thinness of the SiNMs and thus device flexibility. The width of the I-region is determined by the distance between the p+ and n+ regions during photolithography. An I-region width of 2 μm is used in this study in order to achieve high-frequency response while maintaining proper breakdown voltages for power handling. The diode cross-section area can be calculated by multiplying the width of the p+ (or n+) region by the thickness of the

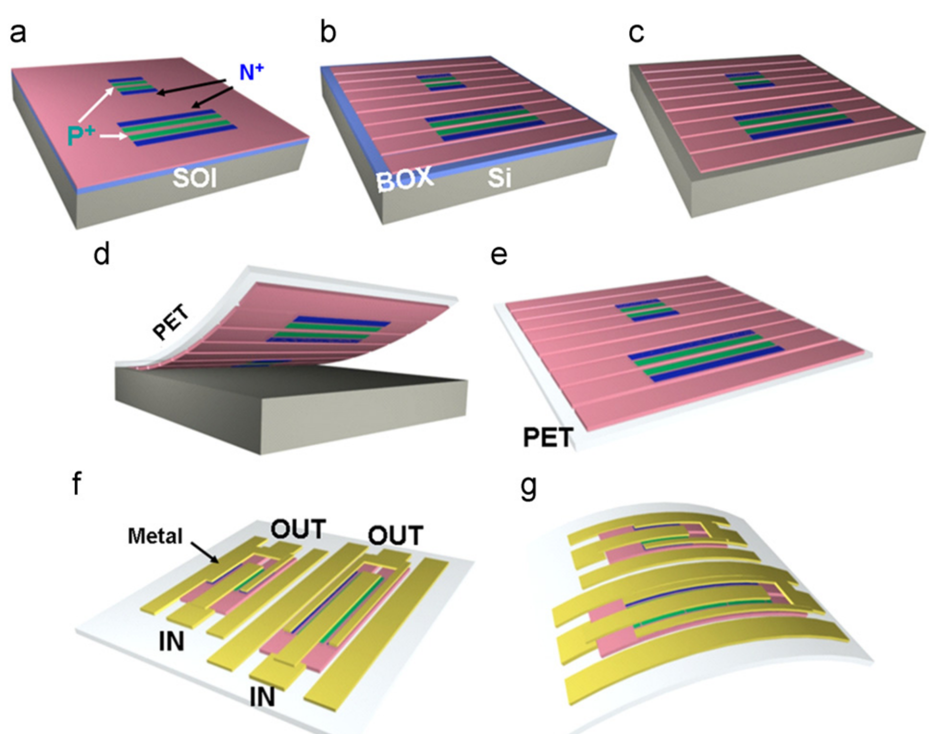


Fig. 1. Process schematic of fabricating flexible microwave single-crystalline Si nanomembrane PIN diode on plastic substrate (drawn not to scale). (a) SOI sample with heavily dosed n- and p-type regions by lithography patterning, ion implantation and high-temperature annealing. (b) 200 nm template Si layer is patterned into stripes and etched down to the buried oxide (BOX) layer by dry etching. (c) 200 nm single-crystalline Si nanostripes are released and attached on handling substrate wafer, by etching away the BOX layer in HF solution. (d) The Si nano-stripes (or SiNMs) are brought firmly contacted with PET plastic substrate with adhesive spinned SU-8 layer, and detached from the handling substrate. (e) The Si nano-stripes (or SiNMs) are flip-transferred onto the plastic substrate. (f) Finished flexible microwave PIN diode using transferable single-crystalline SiNMs on plastic substrate, after dry etching the SiNM active area and evaporating the metal connection and electrodes. (g) Illustration of the flexible single-crystalline SiNM PIN diodes under bending condition.

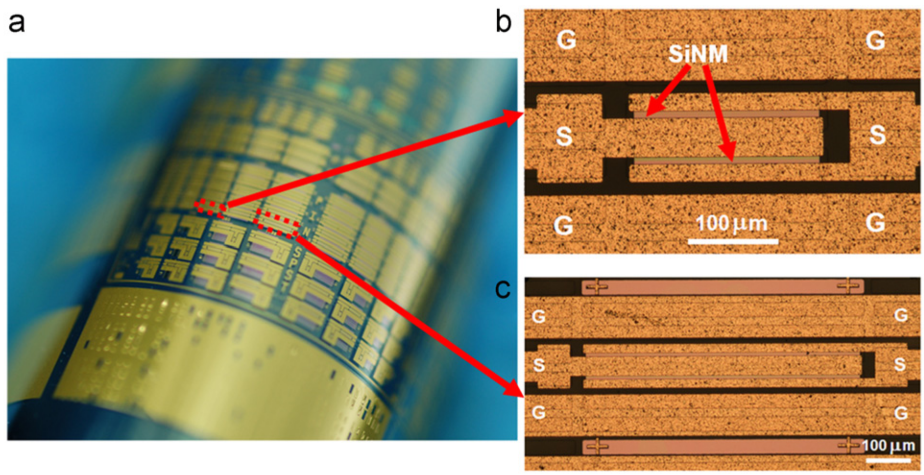


Fig. 2. (a) Optical image of the finished PIN diodes arrays on a bent PET substrate. (b) Microscopic image of the flexible microwave single-crystalline SiNM PIN diode on plastic substrate. Total diode width is 400 μm (two identical parallel diode channel, each channel has a width of 200 μm). Diode intrinsic region length is 2 μm. Total diode area is 80 μm^2. (c) Microscopic image of the 240 μm^2-PIN diode on plastic substrate. Total diode width is 1200 μm (two identical parallel diode channels, each channel has a width of 600 μm).

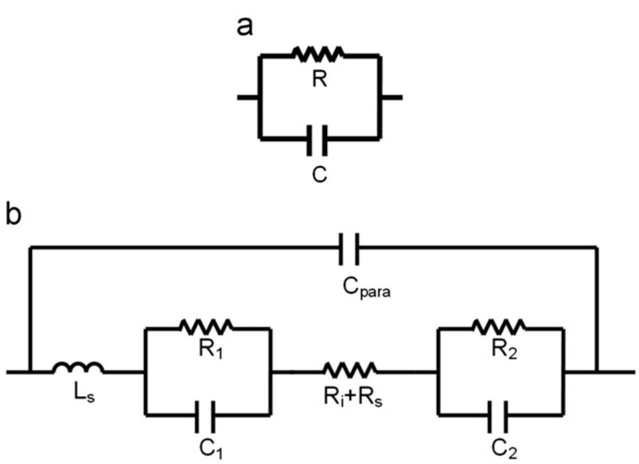


Fig. 3. (a) Equivalent circuit schematic of a p–n junction. (b) RF/microwave equivalent circuit model for microwave PIN diodes using transferable single-crystalline SiNMs on plastic substrate.

SiNM (200 nm). The fabricated diodes have various areas ranging from 80 μm^2 (total diode width is 400 μm) to 240 μm^2 (total diode width is 1200 μm). Fig. 2(a) shows an optical image of the flexible PIN diodes and switch arrays on PET substrate. Fig. 2(b) and (c) shows the optical-microscope images of finished lateral SiNM PIN diodes with an area of 80 and 240 μm^2, respectively.

3. RF model and experimental results

The RF/microwave equivalent circuit model of the microwave lateral PIN diode using single-crystalline SiNMs on plastic substrate is composed of three major parts according to the device structure and layout as depicted in Fig. 3.

1. Junctions
   The lateral PIN diode consists of two junctions: A p–n+ junction and a p+p- junction. Under forward mode condition, the equivalent circuit model for the p–n+ junction is shown in Fig. 3(a) [16]. The resistor value is small and can be expressed as shown in Eq. (1). The parallel capacitor is composed of space-charge region capacitance and diffusion capacitance, as expressed in Eqs. (2)–(9) [16]. When the PIN diode is zero or reversely biased, the resistor value is large and omitted as an open circuit for the simplicity without loosing the generality. The parallel capacitor is mainly space-charge region capacitance, as shown in Eq. (3), where reverse bias V_{Ar} is applied.

$$R = \frac{kT}{qAJ} \tag{1}$$

$$C = C_T + C_D \tag{2}$$

$$C_T = A\sqrt{\frac{\varepsilon q N_A}{2(V_{BJ}-V_A)}} \tag{3}$$

$$C_D = A\frac{q^2}{kT}L_n n_{p0}\exp\left(\frac{qV_A}{kT}\right) \tag{4}$$

$$V_{BJ} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{5}$$

$$V_A = \frac{kT}{q}\ln\left(\frac{J}{J_0}\right) \tag{6}$$

$$J_0 = \frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} \tag{7}$$

$$n_{p0} = \frac{n_i^2}{N_A}, \quad p_{n0} = \frac{n_i^2}{N_D} \tag{8}$$

$$L_p = \sqrt{\mu_p kT\tau_p}, \quad L_n = \sqrt{\mu_n kT\tau_n} \tag{9}$$

   The p+p- junction has the similar equivalent circuit topology as used for the p–n+ junction model, with only change to the built-in voltage expression and saturation current density, as shown in Eqs. (10) and (11).

$$V_{BJ2} = \frac{kT}{q}\ln\left(\frac{p_{p01}}{p_{p02}}\right) \tag{10}$$

$$J_{02} = \frac{qD_p p_{n0}}{L_p} \tag{11}$$

2. Intrinsic region
   The intrinsic region of the PIN diode can be modeled as a variable resistor, under forward and reverse bias conditions. The I-region resistance under forward-biased condition can be

expressed as

$$R_i = \frac{w_i^2}{I_f \tau(\mu_n + \mu_p)} \tag{12}$$

where w_i is the width of the I-region, I_f is the forward-biased current, and τ is the effective carrier lifetime. μ_n, μ_p are the mobilities of electrons and holes, respectively. The I-region resistance will be much larger at zero or reverse bias, because of the carrier fully depletion region.

3. Parasitics
For the microwave single-crystalline SiNM PIN diodes on plastic substrates, since novel nanoscale single-crystalline Si membrane is employed for fabricating PIN diodes and soft PET substrate is used, parasitic effects are more severe than those on rigid bulk Si substrates. Therefore parasitic parameters need to be carefully investigated and included in the RF equivalent circuit model. Series parasitic resistor and inductor are mainly induced by connection metals, electrode contact resistance, and thin SiNMs. According to the flexible device layout, parasitic capacitance between input and output is nonnegligible. As shown in the microscopic image (Fig. 2(b)), the parasitic capacitor is composed of two parallel plate capacitors between the input and output connection metal, and can be approximately expressed as Eq. (13). Where t is the connection metal thickness, w is the input and output metal overlap width (roughly diode width), and d is the spacing between input and output metal (roughly diode intrinsic region length). Therefore the parasitic capacitance is roughly proportional to the diode area, and reversely proportional to the diode intrinsic region length. The parasitic parameters are almost independent of the diode bias condition.

$$C_{para} \approx \frac{2\varepsilon\varepsilon_0 tw}{d} \tag{13}$$

With the three parts, the RF/microwave equivalent circuit model for flexible PIN diode on plastic substrate is shown in Fig. 3(b). Where intrinsic region resistor and series parasitic resistor are combined for simplicity. The model is put into Agilent Advanced Design System (ADS) to calculate the RF/microwave response of the flexible PIN diodes.

RF characteristics of the PIN diodes were measured with an Agilent E8364A performance network analyzer using 150-μm pitch Cascade Ground-Signal-Ground (GSG) probes. Calibration was conducted to the probe tip by Short-Open-Load-Thru (SOLT) method using impedance standard substrate from DC to 40 GHz. Small-signal scattering parameters (S-parameters) were measured for the SiNM PIN diodes under both ON (diode is forward biased, forward current I_f = 10 mA) and OFF (diode is zero biased) conditions. (DC and power handling capability of the flexible PIN diodes were also measured) [15,17]. Under this state, RF signal is transmitted from the IN port to the OUT port. The power ratio of the signal between the OUT port and the IN port through the diode under ON state is defined as insertion loss ($S21$, in dB). The measured RF signal power ratio between the OUT port and the IN port under OFF state is defined as isolation (also $S21$, in dB).

The experimental data for a 240-μm^2 SiNM PIN diode from DC to 20 GHz are shown in Fig. 4 (forward mode ON state) and Fig. 5 (reverse mode OFF state). The insertion loss of the 240-μm^2 SiNM PIN diode is less than 1.5 dB up to 20 GHz. Isolation of >11 dB is observed up to 5 GHz and degrades at higher frequencies. The flexible PIN diode using transferable single-crystalline SiNMs on plastic substrate demonstrates good frequency response at RF and microwave frequency regime, indicating great potential of monolithic integration of flexible active and passive devices on flexible substrates for RF/microwave applications. The fluctuations of the measured data are possibly due to the worse contact between the GSG probe and thin metal electrode on soft substrate.

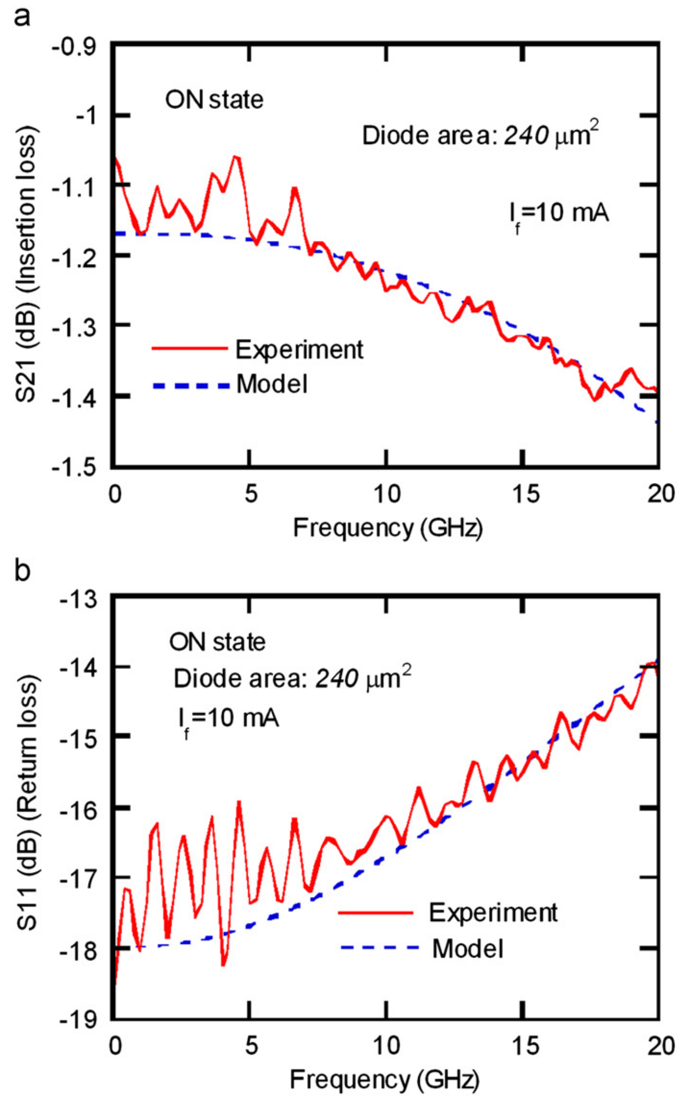


Fig. 4. Measured small-signal S-parameters (solid red curves) of the flexible microwave PIN diode (diode area = 240 μm) under ON state (forward mode), with comparison of the calculated results using developed RF model (dashed blue curves). (a) $S21$, insertion loss. (b) $S11$, return loss. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

The modeled results for ON and OFF states using the RF/microwave model are also shown in Figs. 4 and 5 for comparisons. Measurement and calculation results are further obtained and compared for an 80-μm^2 SiNM PIN diode for validating the developed model, as shown in Fig. 6 (ON state) and Fig. 7 (OFF state). Good agreements are achieved for both diodes under forward and reverse bias conditions. The discrepancy between experimental data and calculation is mainly because of the not perfect contact of the probes on soft substrates. Overall, Figs. 4–7 demonstrate good accuracy of the RF/microwave model for the microwave PIN diodes using single-crystalline SiNMs on plastic substrates.

4. Discussion

According to Figs. 4–7, it can be seen that flexible PIN diode with smaller diode area has worse insertion loss (more degradation)

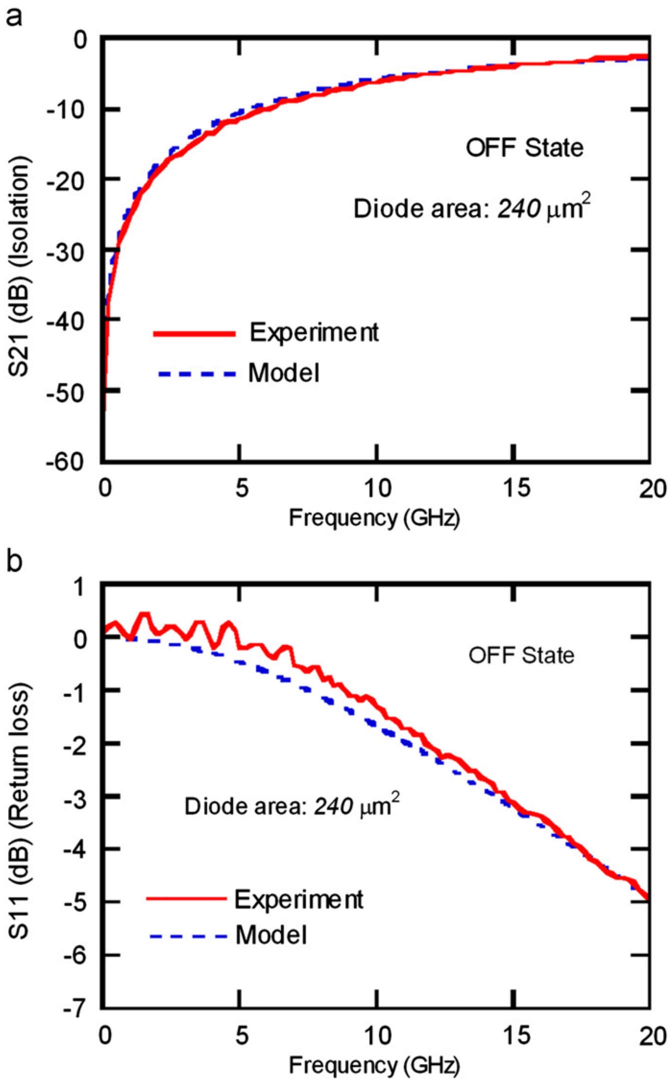


Fig. 5. Measured small-signal *S*-parameters (solid red curves) of the flexible microwave PIN diode (diode area = 240 μm) under OFF state, with comparison of the calculated results using developed RF model (dashed blue curves). (a) *S*21, isolation. (b) *S*11, forward mode return loss. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

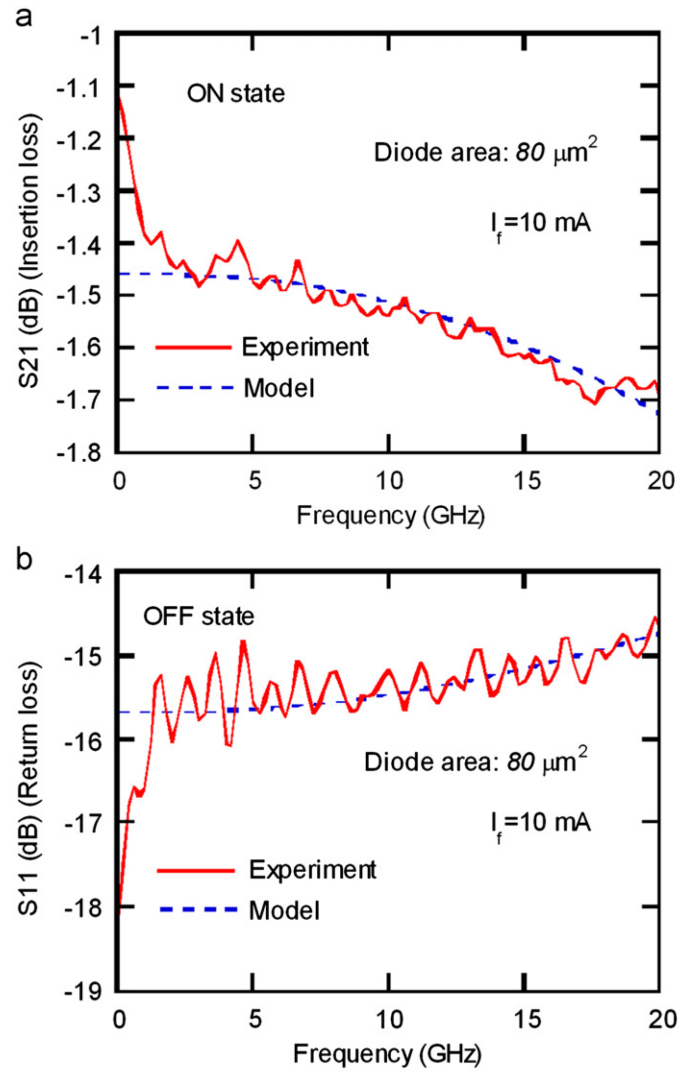
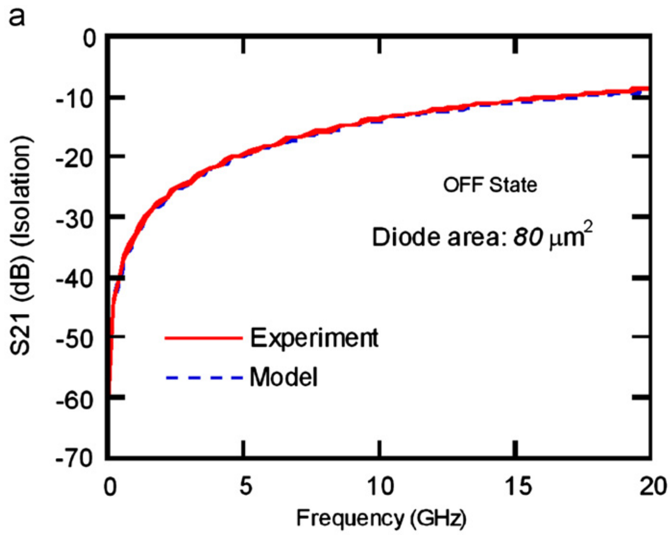


Fig. 6. Measured small-signal *S*-parameters (solid red curves) of the flexible microwave PIN diode (diode area = 80 μm) under ON state (forward mode), with comparison of the calculated results using developed RF model (dashed blue curves). (a) *S*21, insertion loss. (b) *S*11, forward mode return loss. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

at forward bias, but better isolation characteristic at reverse bias. With the RF/microwave model, underlying reason is analyzed. Under forward bias mode, the series resistance is 14.2 Ω and the parasitic inductance is 0.133 nH for the 240 μm PIN diode. When the diode area is decreasing to 80 μm, the series resistance increases to 19 Ω. The increasing is not proportional to the diode area change because that series resistance consists of intrinsic region resistance and parasitic resistance. When the diode area becomes smaller, intrinsic region resistance increases because of smaller diode width, while the parasitic resistance is reduced due to shorter connection metal length. The high series resistance is contributed from the thinness of the SiNMs and relatively large intrinsic region length for power handling capability. Smaller diode intrinsic region length is able to significantly reduce the series resistance. Different from the series resistance, the parasitic inductance is decreased from 0.133 to 0.126 nH for the PIN diode with 80 μm diode area, because of shorter connection metal length from input port to output port. Under reverse bias mode, series resistance of 240 μm PIN diode is 40.2 Ω while it increases to 120 Ω for the 80 μm PIN diode, approximately follows the reversely proportional increasement with diode area. This is because that under reverse bias condition, the intrinsic region resistance dominates the series resistance, therefore the diode shows series resistance reversely proportional to the diode area. Parasitic inductance shows similar change with that under forward mode, since parasitic inductance is much less sensitive to the diode width than resistance. In addition, all the capacitance (including junction capacitance and parasitic capacitance) shows proportional change with the PIN diode area. With good understanding of the device parameters based on RF/microwave model, higher series resistance is demonstrated to be the major factor for lower insertion loss and better isolation. The model shows a performance trade-off between forward mode insertion loss and reverse mode isolation with different flexible PIN diode structures. Furthermore, the model provides a guideline of designing and optimizing the flexible PIN diodes for RF/microwave applications.

5. Conclusion

Flexible microwave PIN diodes using transferrable single-crystal Si nanomembranes (SiNM) that are monolithically integrated on low-cost



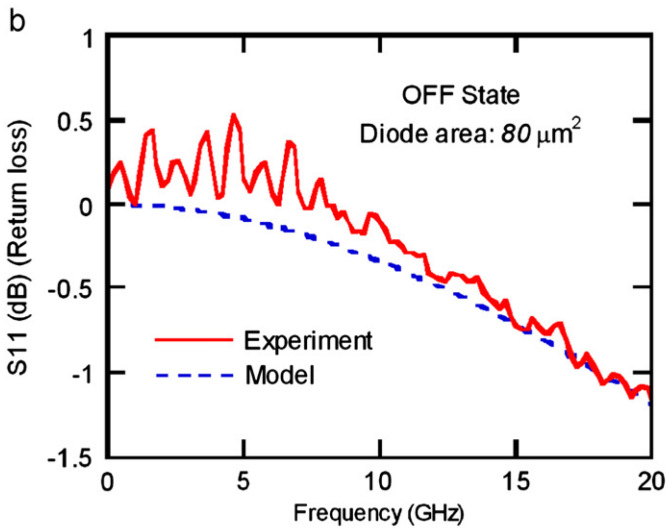


Fig. 7. Measured small-signal *S*-parameters (solid red curves) of the flexible microwave PIN diode (diode area = 80 μm) under OFF state (reverse mode), with comparison of the calculated results using developed RF model (dashed blue curves). (a) *S*21, insertion loss. (b) *S*11, reverse mode return loss. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

flexible plastic substrates are presented in this paper. With high-energy, high-dose ion implantation and high-temperature annealing before nanomembrane release and transfer process, the parasitic parameters are effectively reduced, and the flexible PIN diodes obtain good high-frequency response. Novel RF/microwave model of the microwave PIN diodes based on transferable single-crystalline Si nanomembrane on plastic substrate is reported, taking into account of the flexible device fabrication and layout. The RF/microwave equivalent circuit model achieves good agreement with the experimental results of the diodes with different diode areas, and reveals the most influential factors to the flexible PIN diode characteristics. The study provides guidelines for properly designing and using single-crystalline Si nanomembranes for flexible RF diodes and demonstrates the great possibility of flexible monolithic microwave integrated systems. RF/microwave modeling of the flexible single-crystalline Si PIN diodes under bending conditions is the future research direction.

Acknowledgements

This work was supported partly by AFOSR under Grant no. FA9550-06-1-0487 and NSF MRSEC under Grant DMR0520527. This work was also partially supported by National Natural Science Foundation of China (NSFC) under Grant no. 61006061 and Ministry of Education (MoE) of China.

References

[1] R.H. Reuss, B.R. Chalamala, A. Moussessian, M.G. Kane, A. Kumar, D.C. Zhang, J.A. Rogers, M. Hatalis, D. Temple, G. Moddel, B.J. Eliasson, M.J. Estes, J. Kunze, E.S. Handy, E.S. Harmon, D.B. Salzman, J.M. Woodall, M.A. Alam, J.Y. Murthy, S.C. Jacobsen, M. Olivier, D. Markus, P.M. Campbell, E. Snow, Macroelectronics: perspectives on technology and applications, Proceedings of IEEE 93 (2005) 1239–1256.

[2] H. Sirringhaus, T. Kawase, R.H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E.P. Woo, High-resolution inkjet printing of all-polymer transistor circuits, Science 290 (2000) 2123–2126.

[3] X. Lu, Y. Xia, Buckling down for flexible electronics, Nature Nanotechnology 1 (2006) 163–164.

[4] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gate, M. McCreary, Electronic paper: flexible active-matrix electronic ink display, Nature 423 (2003) 136.

[5] G.H. Gelinck, H.E.A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J.B.P.H. Van der Putten, T.C.T. Geuns, M. Beenhakkers, J.B. Giesbers, B.-H. Huisman, E.J. Meijer, E.M. Benito, F.J. Touwslager, A.W. Marsman, B.J.E. van Rens, D.M. de Leeuw, Flexible active-matrix displays and shift registers based on solution-processed organic transistors, Nature Materials 3 (2004) 106–110.

[6] T. Afentakis, M. Hatalis, A.T. Voutsas, J. Hartzell, Design and fabrication of high performance polycrystalline silicon thin-film transistor circuits on flexible steel foils, IEEE Transactions on Electron Devices 53 (2006) 815–822.

[7] P.F. Baude, D.A. Ender, M.A. Haase, T.W. Kelley, D.V. Muyres, S.D. Theiss, Pentacene-based radio-frequency identification circuitry, Applied Physics Letters 82 (2003) 3964–3966.

[8] E. Menard, K.J. Lee, D.-Y. Khang, R.G. Nuzzo, J.A. Rogers, A printable form of silicon for high performance thin film transistors on plastic substrates, Applied Physics Letters 84 (2004) 5398–5400.

[9] H.-C. Yuan, Z. Ma, M.M. Roberts, D.E. Savage, M.G. Lagally, High-speed strained single-crystal silicon thin-film transistors on flexible polymers, Journal of Applied Physics 100 (2006) 013708.

[10] J.-H. Ahn, H.-S. Kim, K.J. Lee, Z. Zhu, E. Menard, R.G. Nuzzo, J.A. Rogers, High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates, IEEE Electron Device Letters 27 (2006) 460–462.

[11] H.-C. Yuan, Z. Ma, Microwave thin-film transistors using Si nanomembranes on flexible polymer substrate, Applied Physics Letters 89 (2006) 212105.

[12] H.-C. Yuan, G.K. Celler, Z. Ma, 7.8-GHz flexible thin-film transistors on a low temperature plastic substrate, Journal of Applied Physics 102 (2007) 034501.

[13] G. Qin, H. Zhou, E.B. Ramayya, Z. Ma, I. Knezevic, Electron mobility in scaled silicon metal-oxide-semiconductor field-effect transistors on off-axis substrates, Applied Physics Letters 94 (2009) 073504.

[14] G.M. Cohen, P.M. Mooney, V.K. Paruchuri, H.J. Hovel, Dislocation-free strained silicon-on-silicon by in-place bonding, Applied Physics Letters 86 (2005) 251902.

[15] G. Qin, H.-C. Yuan, G.K. Celler, W. Zhou, Z. Ma, Flexible microwave PIN diodes and switches employing transferrable single-crystal Si nanomembranes on plastic substrates, Journal of Physics D: Applied Physics 42 (2009) 234006.

[16] S.M. Sze, Physics of Semiconductor Devices, third ed., Wiley,, 2006 Chapter 2.

[17] H.-C. Yuan, G. Qin, G.K. Celler, Z. Ma, Bendable high-frequency microwave switches formed with single-crystal silicon nanomembranes on plastic substrates, Applied Physics Letters 95 (2009) 043109.