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Capacitance-voltage characteristics of Si and Ge nanomembrane based flexible metal-oxide-semiconductor devices under bending conditions

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Metal-oxide-semiconductor (MOS) device is the basic building block for field effect transistors (FET). The majority of thin-film transistors (TFTs) are FETs. When MOSFET are mechanically bent, the MOS structure will be inevitably subject to mechanical strain. In this paper, flexible MOS devices using single crystalline Silicon (Si) and Germanium (Ge) nanomembranes (NM) with SiO_2, SiO, and Al_2O_3 dielectric layers are fabricated on a plastic substrate. The relationships between semiconductor nanomembranes and various oxide materials are carefully investigated under tensile/compressive strain. The flatband voltage, threshold voltage, and effective charge density in various MOS combinations revealed that Si NM−SiO_2 configuration shows the best interface charge behavior, while Ge NM−Al_2O_3 shows the worst. This investigation of flexible MOS devices can help us understand the impact of charges in the active region of the flexible TFTs and capacitance changes under the tensile/compressive strains on the change in electrical characteristics in flexible NM based TFTs. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4953458]

In recent years, with the development of transferrable single crystalline nanomembranes (NMs), a variety of NM based field-effect transistors have been demonstrated on flexible substrates.[1–3] Up to date, NM-based transistors have been evolving toward higher performance or more flexible/stretchable devices for wireless communication, military, and bioimplantable applications.[2–4] Although such NM based transistors have become more complicated in structure and configuration, these devices still have a metal-oxide-semiconductor (MOS) structure in the channel region. Basic theories about MOS devices on rigid semiconductor substrates are well developed. The behavior of the active material in MOS under mechanical bending has been well known. However, the study of the characteristics of the MOS stack uniaxial tensile/compressive strains has been limited. Some flexible MOS transistors and capacitor under mechanical bending have been studied systematically for the breakdown voltage, leakage current, and output transfer curves.[2,5] Previously, operational instabilities of flexible NM MOS due to interface changes that are induced by high uniaxial mechanical strain have been observed. However, a more systematic study of the MOS behavior under mechanical bending is needed in order to realize better performing flexible NM transistors with reliable operation.

In this paper, flexible MOS devices are fabricated with Si NMs and Ge NMs as semiconductor materials with various dielectric materials (SiO_2, SiO, and Al_2O_3) on flexible PET (polyethylene terephthalate) substrates and investigated in terms of the combination of materials that would lead to the best results by measuring capacitance−voltage (C−V) characteristics. We further measured the capacitance under different degrees of bending conditions to understand how oxide charges affect the electrical characteristics such as flatband voltage, threshold voltage, and charge density on the flexible MOS devices.

The flexible MOS devices were fabricated using a p-type silicon-on-insulator (SOI, from SOITEC) wafer with a 200 nm Si layer on top and a 145 nm buried oxide layer, and a p-type germanium-on-insulator (GeOI, from SOITEC) wafer with a 240 nm Ge top layer and a 400 nm buried oxide layer (Figure 1(a)). The cathode shaped Si NMs and Ge NMs were patterned and etched with a Reactive Ion Etcher (RIE, Unaxis 790), followed by immersion in concentrated Hydro fluoride (HF) to release the NMs (Figure 1(b)). The released Si NMs and Ge NMs then gently fell onto the handling substrate and bonded to it by weak van der Waals forces. The detailed undercut process can be found elsewhere.[6] Cathode metals (10 nm/150 nm of Ti/Au) were formed using an e-beam evaporator exactly on top of the Si NMs and Ge NMs, as shown in Figure 1(b). Then, the Si NMs and Ge NMs with the cathode metals were flip-transferred onto an adhesive coated (SU−8 2002, Microchem) PET substrate, and the adhesive layer was cured with UV exposure for complete bonding (Figure 1(c)). Note that the adhesion of SU-8 is stronger than a van der Waals bond, enabling transfer printing. The MOS structure was formed with the deposition of a 100 nm thick oxide layer and anode metal stacks (10 nm/150 nm of Ti/Au) by electron beam evaporation and dry etch (Figure 1(d)). Finally, NMs were patterned to form self-aligned MOS structure with a cathode metal partially exposed for contact (Figure 1(e)). During C−V measurement, the flexible MOS devices were fixed on convex or concave molds

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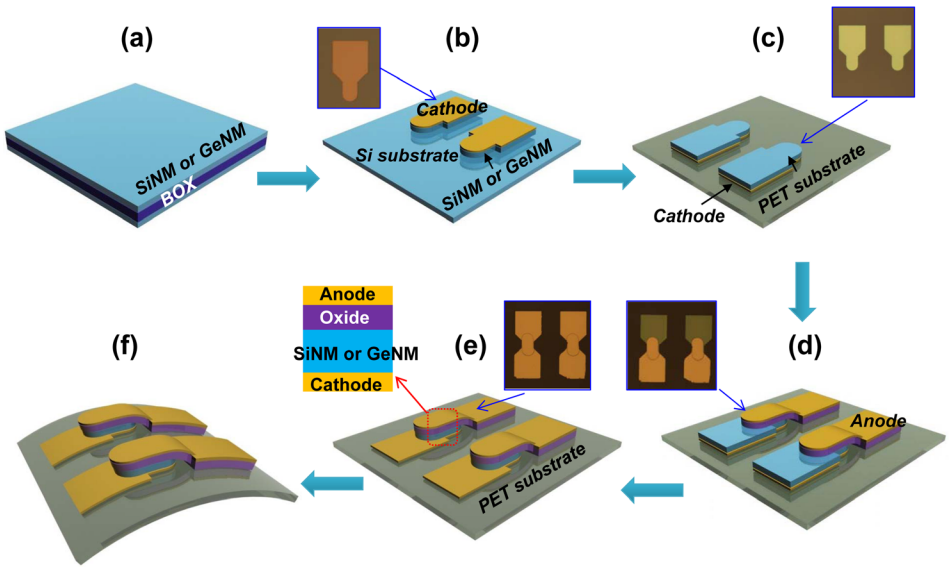

FIG. 1. Schematic illustrations of the fabrication process for flexible NM based MOS devices.

with different bending radii to control the type and amount of strain applied on the device (Figure 1(f)). C−V measurements were carried out by Agilent precision E4980 LCR meter at 1 MHz.

Flexible Si NM MOS devices show typical p-type MOS characteristics with clear accumulation and inversion regions. The inversion layer capacitance is defined by[7]

$$C_{inv} = \frac{1}{C_{ox}} + \frac{1}{C_{bulk}}, \tag{1}$$

where C_{inv} is the inversion layer capacitance, and C_{bulk} is the semiconductor capacitance. C_{bulk} depends on the depletion width in NMs. It should be noted that, when the NM is thin enough, the maximum depletion region may be limited by the thickness of NMs so that C_{inv} of Si NM MOS devices could be higher than C_{inv} of typical MOS capacitor on a bulk substrate.

Figures 2(a)–2(c) show the C−V characteristics of Si NM based flexible MOS devices with different dielectric materials (SiO_2, SiO, and Al_2O_3) under different bending curvatures: concave molds with bending radii of 110.5 mm and 85 mm, and convex molds with bending radii of 77.5 mm, 38.5 mm, 28.5 mm, 21 mm, and 15.5 mm. It should be noted that, as shown in Figure S3, I−V characteristics measured from reference metal-insulator-metal (MIM) structures with a SiO_2, Al_2O_3, or SiO dielectric layer indicate sufficiently high breakdown electric field (E_F) with very low leakage current.[22] The result agrees well with E_F values from other reports[20,21] and confirms that the interface between the oxide and electrode does not affect the performance of flexible MOS capacitors. Raman frequency shifts are observed for NMs with different bending radii, as shown in Figure S1,[22] and the corresponding strain values are calculated based on[8]

$$\Delta\omega = -b_{uni} \times \varepsilon_{xx}, \tag{2}$$

where $\Delta\omega$ is Raman frequency shift, b_{uni}, 337 for (100) Si in ⟨110⟩ direction and 202 for (100) Ge in ⟨110⟩ direction,[8] is proportion constant, and ε_{xx} is strain. For Si NMs, concave bending radii of 110.5 nm and 85 mm correspond to the compressive strain values, 0.16% and 0.32%, respectively, and convex bending radii of 77.5 mm, 38.5 mm, 28.5 mm, 21 mm, and 15.5 mm correspond to the tensile strain values, 0.16%, 0.32%, 0.48%, 0.63%, and 0.79%, respectively.

The flatband voltage (V_{FB}) for each strain condition was extracted using the corresponding flatband capacitance (C_{FB}) in the following equation and extracted from the measured C−V:[7]

$$C_{FB} = \frac{C_{\max}}{1 + \frac{(C_{\max}/C_{\min}) - 1}{2\sqrt{\ln(|N_A - N_D|/n_i)}}}, \tag{3}$$

where C_{max} is the maximum capacitance, C_{min} is the minimum capacitance, N_A is the acceptor concentration, N_D is the donor concentration, and n_i is the intrinsic carrier concentration. As seen in Figure 2(d), V_{FB} shifts toward positive voltages as the applied strain increases. This phenomenon is clear in convex bending with tensile strain. The factors which affect the V_{FB} shift can be analyzed by the following equation:[7]

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_{ox}}, \tag{4}$$

where ϕ_{ms} is the metal-semiconductor work function difference, Q_i is the effective trap charge, which is the sum of effective oxide and interface charges ($Q_i = Q_{ox} + Q_{it}$), and C_{ox} is the oxide capacitance. Based on Equation (2), the V_{FB} shift could be attributed to the change in effective trap charge or the change in the metal-semiconductor work function. The shift in V_{FB} is also related to the overall displacement of capacitance since V_{FB} is derived from C_{FB}. So far, the V_{FB} shift in the MOS device under strain has been explained by the following reasons: gate metal work function shift, the dielectrostriction effect, or a combination of band-edge shift and the modulation of band-edge-to-Fermi-level separation.[9–11] Huang *et al.* and Choi *et al.* assumed that the strain-induced variation in interfacial trap charges and fixed oxide charges do not change appreciably under strain on rigid substrates.[10,11] However, in addition to these factors, it is speculated that the V_{FB} shift in Si NM MOS devices can

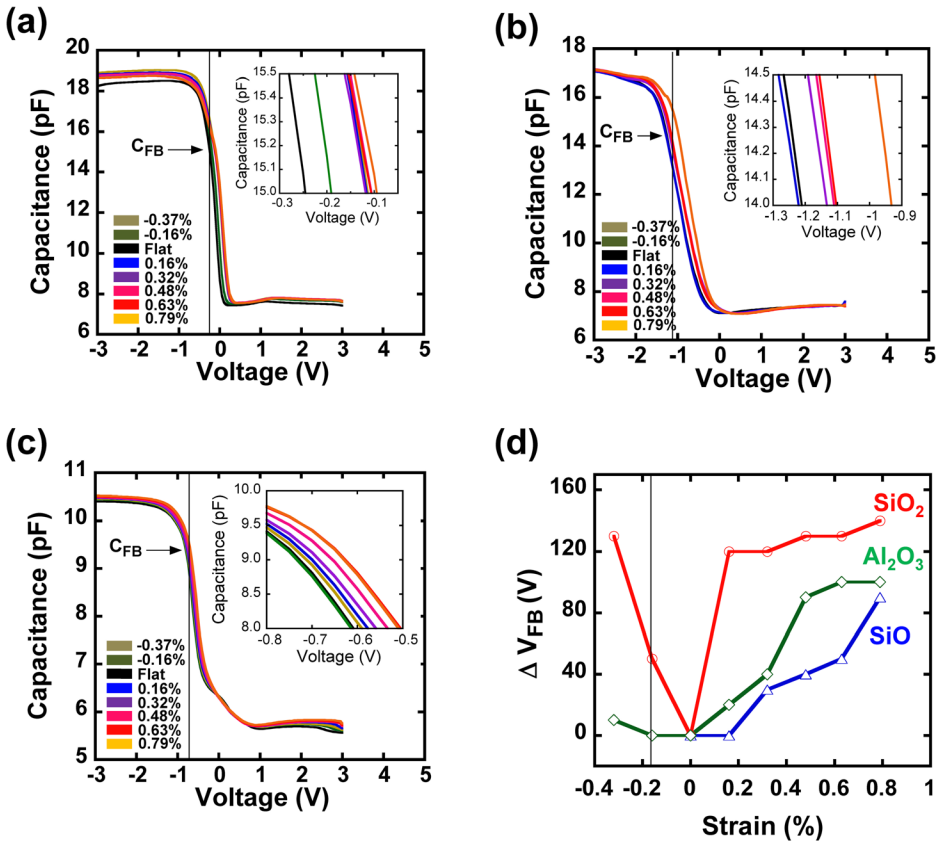

FIG. 2. C−V characteristics measured from Si NM based flexible MOS devices under different bending conditions: (a) Au/SiO_2/Si NM; (b) Au/SiO/Si NM; (c) Au/Al_2O_3/Si NM; and (d) ΔV_{FB} ($V_{FB.\text{bending}} - V_{FB.\text{nobending}}$) versus strain.

be specifically attributed to the strain-induced change in trap charge density for several reasons. First, the uniaxial strain applied to NM MOS devices (up to 0.9%) is higher than the strain typically applied to rigid MOS devices. Thus, the strain-related factors could be more dominant. Second, higher fixed trap charges and interface charges may exist due to a poor silicon-oxide interface and a high defect density in the dielectric layer caused by the evaporation method. The high C−V hysteresis shown in Figure S2 represents the high trap charge density in the evaporated dielectric layer.[12,22] Although it is reported that thermal annealing could reduce the trap charge density for typical rigid MOS devices, the low melting temperature of the plastic substrates in flexible MOS devices hinders further high temperature annealing.[13] Third, although we used the same anode metal for all devices, the different V_{FB} shifts in strain in each oxide indicates dependencies on the types of oxide used in our flexible MOS devices, as shown in Figure 2(d).[14] Figure 3 shows threshold voltage (V_{th}), effective charge (Q_{eff}), and effective charge density (N_{eff}) versus strain of SiNM MOS devices with different oxide materials, to compare the relationship between trap charge density and strain. In SiNM MOS devices, V_{th} is increased as more tensile strain is applied to three types of devices: SiO_2 device (0.17 V/%), SiO device (0.29 V/%), and Al_2O_3 (0.12 V/%). Both Q_{eff} and N_{eff} values are decreased as more tensile strain is applied: SiO_2 device (-1.33×10^{-8} C/%, $-8.31 \times 10^{10}\,\text{cm}^{-2}$/%), SiO device ($-2.09 \times 10^{-8}$ C/%, $-1.30 \times 10^{11}\,\text{cm}^{-2}$/%), and Al_2O_3 (-5.29×10^{-9} C, $-3.30 \times 10^{10}\,\text{cm}^{-2}$/%). Such decreases in

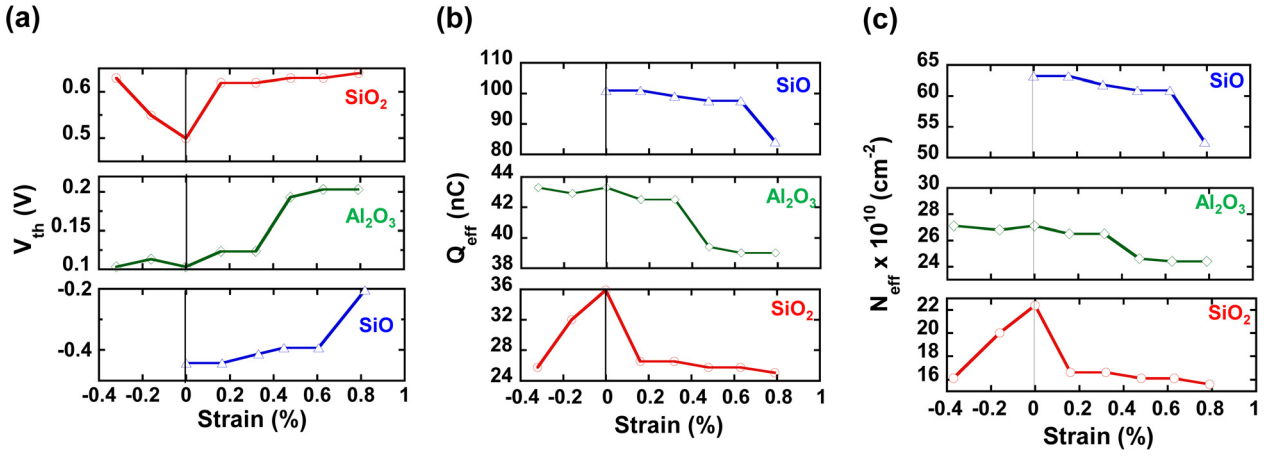

FIG. 3. Calculated values of (a) threshold voltage (V_{th}), (b) effective charge (Q_{eff}), and (c) effective charge density (N_{eff}) under different bending conditions for Si NM based flexible MOS devices.

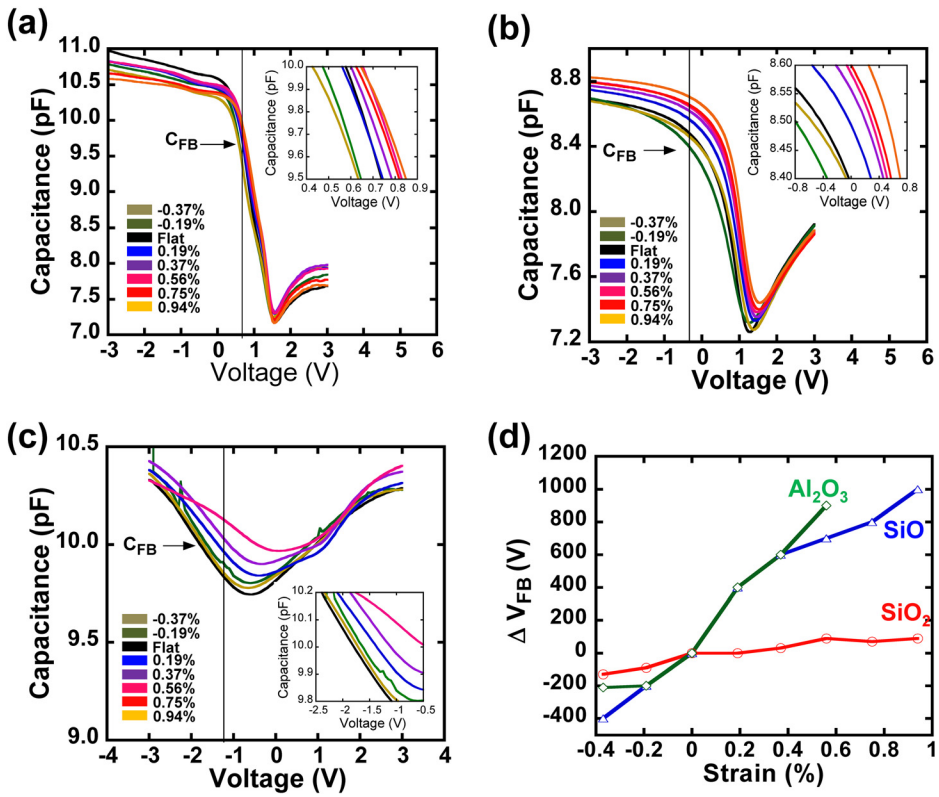

FIG. 4. C−V characteristics measured from Ge NM based flexible MOS devices under different bending conditions: (a) Au/SiO_2/Si NM; (b) Au/SiO/Si NM; (c) Au/Al_2O_3/Si NM; and (d) ΔV_{FB} ($V_{FB,\text{bending}} - V_{FB,\text{nobending}}$) versus strain.

Q_{eff} and N_{eff} values as more strain is applied could be related to increased electron trap density at the oxide/NM interface.

Figures 4(a)–4(c) show the C−V measurement results of flexible Ge NM MOS devices with different dielectric materials (SiO_2, SiO, and Al_2O_3) under various degrees of strain. For Ge NMs, concave bending radii of 110.5 nm and 85 mm correspond to the compressive strain values, 0.37% and 0.19%, respectively, and convex bending radii of 77.5 mm, 38.5 mm, 28.5 mm, 21 mm, and 15.5 mm correspond to tensile strains, 0.19%, 0.37%, 0.56%, 0.75%, and 0.94%, respectively.

The V_{FB} is shifted in the positive direction for Ge NM MOS devices as more tensile strain is applied: SiO_2 device (0.11 V/%), SiO device (1.22 V/%), and Al_2O_3 device (2.01 V/%) (Figure 4(d)). This trend is similar to that of flexible Si NM MOS devices but more pronounced. Under the flat condition, C−V curves in Ge NM MOS devices are shifted in the positive direction compared to those of Si NM MOS devices due to different doping concentrations: Si NM ($1 \times 10^{15}\,\text{cm}^{-3}$) and Ge NM ($1 \times 10^{16}\,\text{cm}^{-3}$). The accumulation capacitances of Ge NM MOS devices are different from those of Si NM MOS devices even though both devices have the same oxide materials and thickness. This difference could be attributed to a poor material interface between the evaporated oxide layers and the Ge NM.[15] Such a poor oxide quality also results in high hysteresis, as shown in Figure S2.[22] Another noticeable difference between the C−V curves of the Ge NM MOS devices and the Si NM MOS devices is the inversion capacitance. Ge NM MOS devices show obscure inversion capacitance characteristics, and the inversion capacitance values are larger than those of Si NM MOS with the same types of oxide and thickness. This is because of the smaller Ge bandgap as well as the poor oxide-Ge NM interface.[16] Therefore, evaporated oxide as a gate dielectric for Ge MOSFET with proper Ge surface passivation process is required.[17–19] Figure 5 shows V_{th}, Q_{eff}, and N_{eff} values of Ge NM MOS devices under different degrees of strain. Similar trends are observed in Ge NM MOS devices. V_{th} increases as more strain is applied: SiO_2 (0.09 V/%), SiO (1.22 V/%), and Al_2O_3 (2.01 V/%). Q_{eff} and N_{eff} values are comparable to those of Si NM MOS devices and show similar trends: SiO_2 device (-5.35×10^{-9} C/%, $-3.029 \times 10^{10}\,\text{cm}^{-2}$/%), SiO device ($-5.39 \times 10^{-8}$ C/%, $-3.36 \times 10^{11}\,\text{cm}^{-2}$/%), and Al_2O_3 device (-8.89×10^{-8} C/%, $-5.55 \times 10^{11}\,\text{cm}^{-2}$/%). In Ge NM MOS devices, the Al_2O_3 oxide layers were broken under tensile strain higher than 0.45% and we were unable to measure them further.

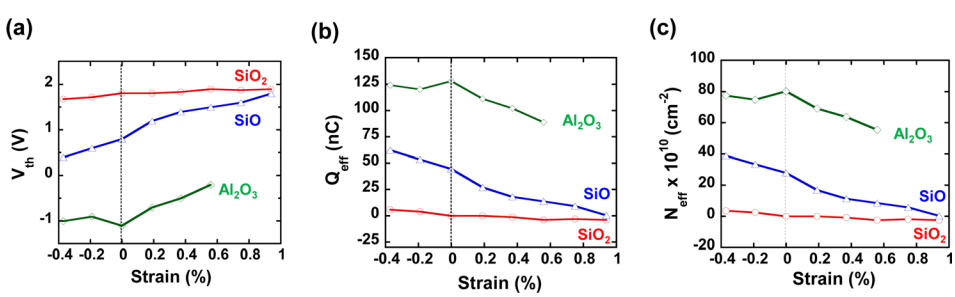

FIG. 5. Calculated values of (a) threshold voltage (V_{th}), (b) effective charge (Q_{eff}), and (c) effective charge density (N_{eff}) under different bending conditions for Ge NM based flexible MOS devices.

In summary, single crystalline flexible MOS capacitors using Si NM and Ge NM were fabricated on plastic substrates, and the C-V characteristics were measured under various degrees of tensile/compressive strain. A high uniaxial strain (up to 0.94%) was applied to the MOS capacitors. The examination of flatband voltage, threshold voltage, and effective charge density in various combinations of dielectric materials and semiconductor materials revealed that the Si NM−SiO_2 shows the best interface charge behavior, while the Ge NM−Al_2O_3 structure shows the worst. The investigations of flexible MOS capacitors can help explain the change in the electrical characteristics of flexible TFTs that are fabricated using flexible single crystalline semiconductor NMs.

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[1]Z.-T. Zhu, E. Menard, K. Hurley, R. G. Nuzzo, and J. A. Rogers, Appl. Phys. Lett. **86**, 133507 (2005).
[2]J.-H. Seo, T. Ling, S. Gong, W. Zhou, A. L. Ma, L. J. Guo, and Z. Ma, Sci. Rep. **6**, 24771 (2016).
[3]J. H. Seo, K. Zhang, M. Kim, D. Zhao, H. Yang, W. Zhou, and Z. Ma, Adv. Opt. Mater. **4**, 120–125 (2016).
[4]R. H. Reuss, B. R. Chalamala, A. Moussessian, M. G. Kane, A. Kumar, D. C. Zhang, J. A. Rogers, M. Hatalis, D. Temple, G. Moddel *et al.*, Proc. IEEE **93**(7), 1239–1256 (2005).
[5]M. T. Ghoneim, A. Kutbee, F. Ghodsi Nasseri, G. Bersuker, and M. M. Hussain, Appl. Phys. Lett. **104**, 234104 (2014).
[6]K. Zhang, J.-H. Seo, W. Zhou, and Z. Ma, J. Phys. D: Appl. Phys. **45**, 143001 (2012).
[7]S. P. Murarka, M. C. Peckerar, and S. Murarka, *Electronic Materials: Science and Technology* (Academic Press Orlando, FL, 1989).
[8]C.-Y. Peng, C.-F. Huang, Y.-C. Fu, Y.-H. Yang, C.-Y. Lai, S.-T. Chang, and C. W. Liu, J. Appl. Phys. **105**, 083537 (2009).
[9]P. Cheng-Yi, Y. Ying-Jhe, F. Yen-Chun, H. Ching-Fang, C. Shu-Tong, and L. Chee Wee, IEEE Trans. Electron Devices **56**(8), 1736–1745 (2009).
[10]J.-Q. Huang, Q.-A. Huang, M. Qin, W. Dong, and X. Chen, J. Microelectromech. Syst. **19**(6), 1521–1523 (2010).
[11]Y. S. Choi, T. Numata, T. Nishida, R. Harris, and S. E. Thompson, J. Appl. Phys. **103**(6), 064510 (2008).
[12]T. L. Tewksbury, L. Hae-Seung, and G. A. Miller, IEEE J. Solid-State Circuits **24**(2), 542–544 (1989).
[13]Z. A. Weinberg, D. R. Young, J. A. Calise, S. A. Cohen, J. C. Deluca, and V. R. Deline, Appl. Phys. Lett. **45**, 1204–1206 (1984).
[14]E. H. Nicollian, J. R. Brews, and E. H. Nicollian, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982).
[15]D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, IEEE Electron Device Lett. **29**(4), 328–330 (2008).
[16]R. S. Johnson, H. Niimi, and G. Lucovsky, J. Vac. Sci. Technol., A **18**(4), 1230 (2000).
[17]N. Taoka, M. Harada, Y. Yamashita, T. Yamamoto, N. Sugiyama, and S.-i. Takagi, Appl. Phys. Lett. **92**, 113511 (2008).
[18]K. Yamamoto, R. Ueno, T. Yamanaka, K. Hirayama, H. Yang, D. Wang, and H. Nakashima, Appl. Phys. Express **4**, 051301 (2011).
[19]C. H. Lee, T. Nishimura, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and A. Toriumi, paper presented at the 2010 IEEE International Electron Devices Meeting (IEDM), 2010.
[20]V. Mikhaelashvili, Y. Betzer, I. Prudnikov, M. Orenstein, D. Ritter, and G. Eisenstein, J. Appl. Phys. **84**, 6747 (1998).
[21]P. P. Budenstein and P. J. Hayes, J. Appl. Phys. **38**, 2837 (1967).
[22]See supplementary material at http://dx.doi.org/10.1063/1.4953458 for the detailed strain analysis by Raman spectroscopy and breakdown electric field of dielectric layer.