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Review

Transfer print techniques for heterogeneous integration of photonic components

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A B S T R A C T

The essential functionality of photonic and electronic devices is contained in thin surface layers leaving the substrate often to play primarily a mechanical role. Layer transfer of optimised devices or materials and their heterogeneous integration is thus a very attractive strategy to realise high performance, low-cost circuits for a wide variety of new applications. Additionally, new device configurations can be achieved that could not otherwise be realised. A range of layer transfer methods have been developed over the years including epitaxial lift-off and wafer bonding with substrate removal. Recently, a new technique called transfer printing has been introduced which allows manipulation of small and thin materials along with devices on a massively parallel scale with micron scale placement accuracies to a wide choice of substrates such as silicon, glass, ceramic, metal and polymer. Thus, the co-integration of electronics with photonic devices made from compound semiconductors, silicon, polymer and new 2D materials is now achievable in a practical and scalable method. This is leading to exciting possibilities in microassembly. We review some of the recent developments in layer transfer and particularly the use of the transfer print technology for enabling active photonic devices on rigid and flexible foreign substrates.

1. Introduction

Semiconductor photonic devices have made impressive progress in their performance with widespread use in multiple applications resulting in an annual €350 B market [1]. Nevertheless, the cost of photonic components remains too high for many other applications impeding their more widespread uptake. This cost is often associated with the diverse nature of the materials involved (e.g. GaAs, InP, GaN, Si, InAs, GaSb) and the associated process technology relying on careful handling for packaging and interfacing to the devices. Monolithic integration of different active and passive components into photonic integrated circuits (PICs) on native III-V substrates is possible but as the optimum device structure is different for different devices, the fabrication process is very challenging. Successful integration has been achieved on a number of material platforms and sophisticated circuits are used in specialised commercial products [2] but it is unlikely that such platforms will reach the cost level needed for widespread consumer use. An alternative approach using the direct growth of photonic device structures on foreign substrates (e.g. GaAs lasers on Si substrates) has been investigated for over 30 years and despite many successes in research labs, the technology has not reached commercial levels. Thus, it is increasingly difficult to envisage that photonics will thrive solely as a stand-alone technology. It will be necessary to integrate photonic components with the highly mature electronics industry by some form of co-packaging or

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heterogeneous integration. The highest functioning systems will involve a wide variety of active and passive photonic components and their intimate integration with other device platforms and substrates. Fortunately this is possible since, as with electronics, compound semiconductor based photonic devices rely on thin epilayers for their essential device function. These epilayers are at most 10 μm in thickness. The separation of the functioning epilayers from their growth substrate can be achieved by various techniques including by use of selective etchants which is made possible by the distinct chemical properties of the different semiconductor alloys involved in the epilayer structure. Such techniques have been extensively investigated for microelectromechanical (MEMS) systems [3]. It is essential that the separation and transfer methods do not introduce any defects into the fragile epilayer structure as the function of any active photonic device would be adversely affected.

This paper reviews some of the recent developments in epilayer transfer technology. We first discuss the wafer-scale transfer of compound semiconductor materials and the techniques used to separate the epilayers from their growth substrate. We then discuss device level transfer using the recently introduced transfer print technique which not only permits the efficient co-integration of photonic devices with different platforms but also allows the realisation of novel structures where lattice matching is not mandatory. We discuss the developments based on stiff and flexible substrates. We show examples of transferred devices based on GaAs, GaN, InP and Si materials.

2. Wafer-scale layer transfer

Perhaps the simplest approach to co-integration is to transfer the epilayers on a wafer scale to a new substrate followed by the removal of the native substrate. This is done providing that some particular advantages accrue. These might be the improved performance of thin devices, improved heat-sinking of active components, the access to the epilayers on the initial substrate side, the opportunity to reuse the substrate and reduce production costs, or the flexibility of the final devices.

Wafer bonding of epitaxial structures grown on III–V wafers to, for example, silicon wafers is one approach. This is constrained by a number of factors. A small difference in the thermal expansion coefficients between the different wafers to be bonded limits the temperature cycling that can be applied as is often needed to obtain a strong bond. This can be addressed by reducing the area to be bonded, by reducing the thickness of the III–V wafer or by pixellation of the III–V wafer. In addition, the III–V wafers often have different sizes, with varying degrees of roughness and different wafer bows making the bonding process specific to particular situations. Nevertheless, wafer scale bonding has been implemented commercially in quite a few applications. For example, wafer bonding of GaN epitaxial stacks to Ge, Cu or Si substrates in conjunction with laser lift-off of the sapphire substrate is being widely used for achieving the highest performing light-emitting diodes (LEDs) [4]. Often the attachment is formed by eutectic metal bonding providing a robust bond.

GaAs photovoltaic (PV) cells benefit from being thin for two principle reasons. The first is that a highly reflective metal contact can be deposited on one side allowing a thinner cell due to the double pass of sunlight while the reflection of internally generated emission allows for efficient photon recycling. Secondly, the substrate cost becomes significant as the production volume increases. A well-established method to separate the device epilayers from the substrate is to incorporate a thin (~20 nm) sacrificial lattice-matched AlAs, or high Al content $Al_xGa_{1-x}As$ layer beneath the cell layers during the growth of the structure. Highly selective etching of AlAs over GaAs is obtained with hydrofluoric acid (HF) based solutions [5] and, by using a peeling technique [6], the epilayers from full wafers can be separated from the GaAs substrate allowing for the recovery and re-use of the substrate. This technique has been used to realise thin PV cells with optimum photon management and has been the basis of the world record efficiency of 27.6% under 1 sun illumination for a single junction cell [7]. Substrate removed GaAs cell technology has been implemented commercially by a number of companies. To improve the surface quality of the GaAs wafer for subsequent for re-growth various additional layers (lattice matched $Ga_{0.5}In_{0.5}P$ in particular [8]) have been incorporated into the epitaxial structure. An alternative lattice-matched release layer for GaAs is $Al_{0.5}In_{0.5}P$ which can be etched using hydrochloric acid (HCl) with very high selectivity to GaAs as shown in Fig. 1. Epilayers as appropriate for a single junction photovoltaic cell were released from 50 mm diameter GaAs substrates and subsequently cells with 13.5% efficiency were demonstrated [9]. The HCl etch process results in the released GaAs surface being smoother than for the AlAs / HF based process. As a result the GaAs substrates require less preparation for re-growth.

Silicon photonics has emerged as a very promising for low-cost, universal (design rule based) integration of photonic components [11]. The technology operates at wavelengths longer than1 μm and to achieve its full potential it is necessary, at least, to integrate amplifying elements with the silicon on insulator (SOI) waveguide platform to provide the gain needed for integrated lasers. These gain elements are composed of layered quantum well structures grown primarily on 50–100 mm diameter InP substrates. Current integration strategies use an evanescent coupling between the silicon waveguide and adjacent gain providing layers which are energised by current through the III–V element. This close connection between the waveguides is obtained by wafer bonding [12]. Typically, small Section (1 cm^2) of the InP wafer are bonded to the SOI wafer using a very thin (< 200 nm) intermediate layer so as to enable high yield. A thin SiO_2 layer on each surface acts as an excellent bonding medium as it can be activated with an oxygen plasma to create a hydrophilic surface which provides a strong bond at relatively low temperatures (< 250 °C). Alternatively, a thin polymer such as BCB acts as a conformal interface layer. Such insulating layers prevent current transport across the interface requiring the electrical contacts to be on one side. Additionally they introduce a thermally resistive interface. Following bonding of the dies, the InP substrate is selectively removed in a HCl based etchant which stops at an InGaAs(P) layer incorporated in the structure. The devices can then be fabricated with lithographic alignment between the III–V and SOI structures.

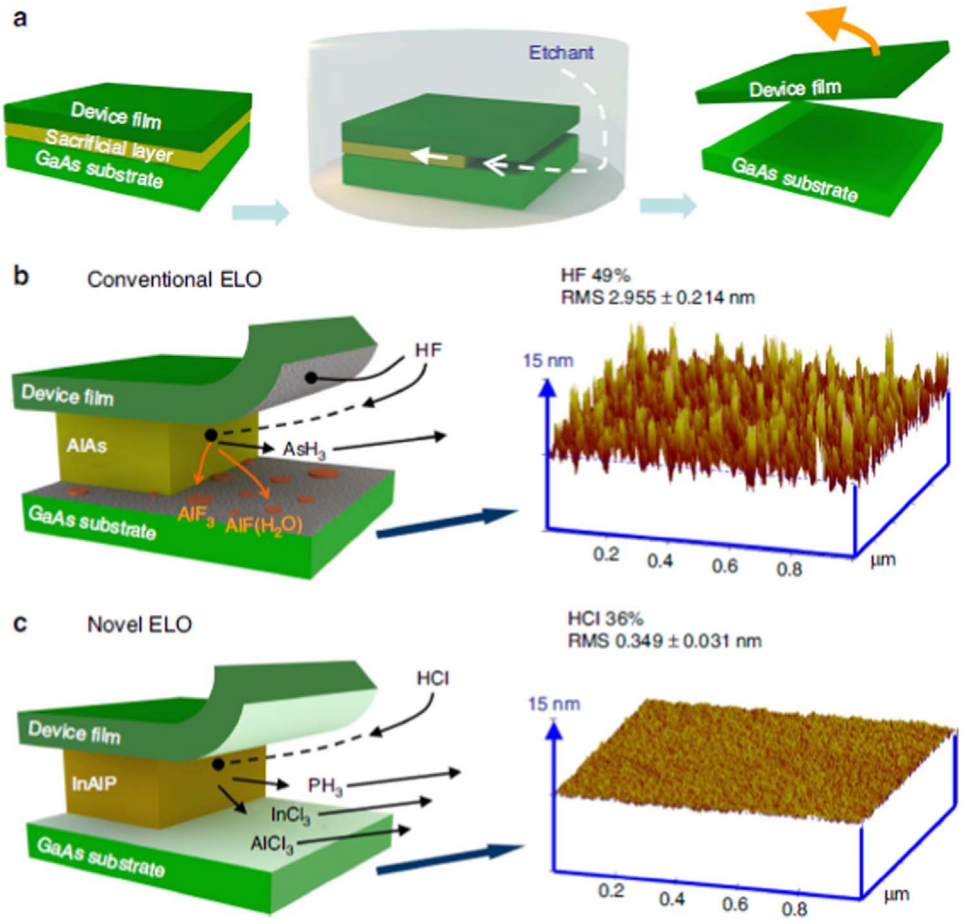

Fig. 1. Schematic epitaxial lift-off (ELO) process for wafer level release of epilayers from a GaAs substrate comparing selective etch layers of AlAs and AlInP and the resultant roughness as measured by atomic force microscopy (AFM). Reprinted from [9]. It is important to allow the etch gases to escape by maintaining a separation between the film being released and its substrate. This is achieved by a floating the released film [9] or by using an attached weight [10].

3. Device level transfer

The examples discussed so far have been wafer scale processes where the complete area of the epilayer contributes to the device function which is mostly stand-alone. There are many more applications where the need is for diverse devices to be co-integrated on a common platform. By using masking techniques it has long been possible to transfer III–V and II–VI materials or pre-fabricated devices from the growth substrate to a foreign substrate [13–17]. However, yield and placement accuracy remained an issue.

A major advance was made by the Rogers group at University of Illinois who introduced a technique where coupons of material could be transferred in a controllable, massively parallel manner with micron scale accuracy from a source wafer to a separate target substrate [18,19]. The only requirement on the receiving substrate is that it is locally flat. Suspended coupons of the required area are prepared on the source wafers by using an anchoring system in conjunction with an underlying layer which is selectively etched to release the coupons (Fig. 2). The technique utilises the viscoelastic properties of elastomeric materials, particularly polydimethylsiloxane (PDMS) rubber. A stamp is prepared using soft lithographic techniques with contacting posts corresponding to the desired arrangement of coupons to be transferred. Due to the soft nature of the PDMS it can handle fragile materials without damage. The basis of the transfer printing approach is the rate-dependence adhesion strength of the object to the elastomer stamp (Fig. 3). There is a temperature-dependent critical velocity between printing and pick up where the dominant adhesion switches from the substrate - object to the object – stamp interface. This critical velocity is dependent on the exact materials involved and the temperature [19,20]. The PDMS stamp is held on a transparent rigid support (glass) and is then brought in contact with the device coupons. A fast (> 10 cm/s) pulling motion is used to both break the tethers of the anchoring system at engineered locations picking up the selected coupons which are now adhered on the stamp posts. Using a mechanical motion the device coupons can be transferred and printed with the selected pitch/repetition to the target substrate and the stamp released by a slow (< 1 mm/s) action.

The stamp can be utilised repeatedly to consume all the devices/coupons from the source wafer. The coupons can be transferred multiple different target substrates. The protocols for efficient transfer of devices have been investigated for different situations on the receiving wafer and are reviewed in [21]. The relative adhesive strength between the stamp and the device should be less than

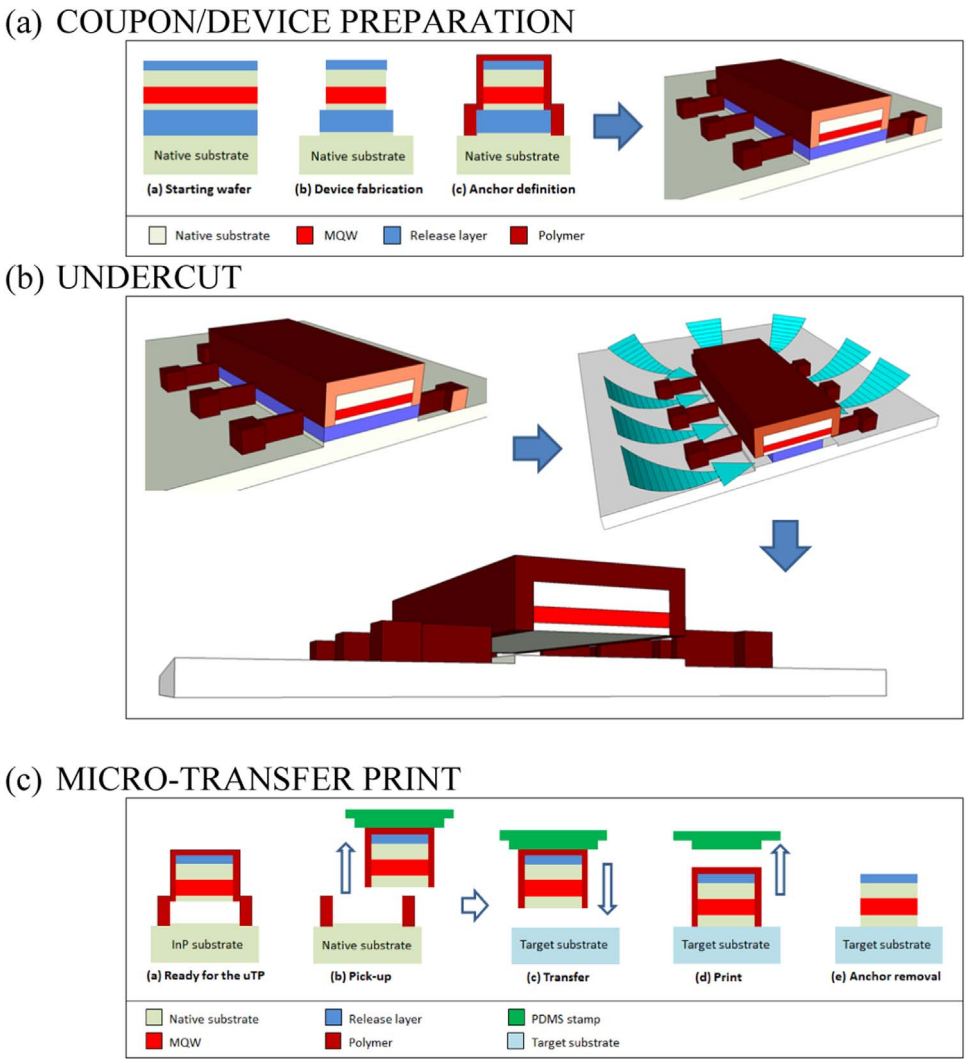

Fig. 2. Overview of the transfer print process: (a) preparation of mesas on the starting wafer to isolate coupons or devices of the desired footprint and pitch with (here) resist tethers between the coupons and the substrate, (b) Selective etching of the release layer while leaving the coupons suspended by resist tethers and held in place by anchors on the substrate, (c) use of a PDMS stamp to pick-up and transfer arrays of coupons to a new target substrate.

that between the device and the receiving location which can be achieved by, for example, introducing micro-tips as surface relief on the PDMS stamp to allow variable contact area or by using shear loading as a means to modulate the stamp adhesion. The bond to the receiving substrate can be a direct bond using van der Waals forces or can be enhanced by having a thin (< 1 μm) polymeric layer on the receiving substrate. The adhesion can be further improved by use of an oxygen plasma treatment. The adhesion layer should be as thin as possible to enable optical interconnect and avoid high thermal resistance. Generally, the adhesion layer is electrical non-conductive. Post-transfer there can be some limitation in the thermal steps. However, such restrictions can often be easily managed.

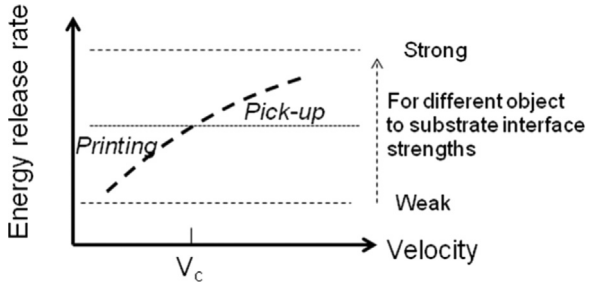

Fig. 3. Schematic illustrating stamp velocity dependent release. There is a switch between adhesion of the object to the stamp or to the substrate at a critical velocity, V_c, dependent on the actual interface adhesion strengths (adapted from [20]).

Micro-transfer printing tools have been developed specifically for the commercial production of transfer printed concentrator photovoltaic cells [22,23]. These tools are capable of transfer printing devices onto extremely large (400 mm x 500 mm) sized panels [24]. The tools use high-precision motion stages [25] and optics. The structured stamp is held on a rigid transparent plate. By utilising a machine vision system in conjunction with fiducial marks on both the device coupons and on the target substrate the automated positioning of high numbers of devices on the target substrate can be aligned with an accuracy of $\pm$ 1.5 μm at 3σ distribution with respect to the target location [26]. Sub-micron precision is also possible when individually placing devices [27]. If the device structure is processed post-transfer then it is then possible to obtain lithographic alignment of features between structures on the transferred coupon and on the target substrate. Multiple different components can be transferred in sequence such as needed for displays. Red, green and blue LEDs have been integrated onto single 'pixels' in a 100×100 display over 1 cm $\times$ 1 cm and 2 cm $\times$ 2 cm [42]. A polymer based bonding layer on the target substrate planarises minor roughness on the target substrate and improves the adhesion over direct van der Waals bonding. Direct bonding, however, provides the opportunity for an excellent thermal interface and potential current transport.

The transfer print technique can handle devices an order of magnitude smaller than is possible with conventional robotic pick and place tools, it can transfer as many devices as desired deterministically in each step. Transfer print makes very efficient use of the material on the source wafer effectively spreading the original wafer material over a wide area. It negates the impact of size mismatch between the source and receiving wafers. It allows the devices to be closely integrated with waveguides and thus has the potential to introduce massive savings on packaging costs. Novel device structures can be envisaged as the requirement of lattice matching is avoided. A particular advantage is that very small devices (micron scale) and very thin layers (monolayers) can now be transferred. The technique can accommodate minor particulates and individual devices can be replaced unlike wafer bonding. A vision for transfer print is that stocks of independently fabricated high performance standard components (materials or devices) are prepared. Functional photonic circuits are then built by the assembly of these components (Fig. 4). One can envisage that the devices are either pre-fabricated or subsequently fabricated on the new substrate. In any event, the interconnections are made on the new substrate in a common step. A review of some of the different devices that can be transfer printed is presented in [28].

3.1. Transfer print of GaAs based devices

There are a number of GaAs-based photonic structures that can benefit from transfer printing. Examples are photovoltaic (PV) devices, detectors, Vertical Cavity Surface Emitting Lasers (VCSELs) and edge-emitting lasers. As previously mentioned, GaAs structures can be released through the use of Al(Ga)As and AlInP sacrificial layers. Another potential approach is to use Ge which is closely lattice matched to GaAs. Ge can be selectively removed by spontaneous etching by gas phase XeF_2 where extremely high rates ($>$ 50 μm/min) have been demonstrated [29].

Concentrator photovoltaic cells need to consider heat sinking as, even with a 40% efficient cell, 60% of the energy is dissipated is heat which at a concentration of 1,000 suns is ~100 W/cm^2. An increase of the device temperature leads to a degradation in the performance of the cell. By using small device areas in conjunction with a low thermal resistance path to a metal substrate enabled by thin cells, the heat dissipation is distributed thereby avoiding the need for special heat sinking. Additionally, as the light is focussed on the individual cell it is necessary to separate the devices to maximise the use of the semiconductor material. The small and thin cells permit lightweight optics and thus lightweight panels. Dual-junction 600 μm sized cells with efficiencies of $>$ 30% at 1000 sun concentration have been realised [30] and cells with higher number of junctions used to develop commercial solar *modules* with record efficiencies of 35.5 percent [23].

The transfer print method allows for new efficient strategies in the growth of the materials. For example, by repeatedly depositing the layers for a device structure, each separated by a release layer, on a wafer during a single growth run it is possible to multiply the potential number of devices as illustrate schematically in Fig. 4 [31]. This approach has been applied to both PV cells and to detectors. Transfer print of PV cells made from each of three device layers was performed and the characteristics compared with good consistency shown. One issue which can arise during the repeated growth of *p-n* structures is the diffusion of Zn which is commonly used as the *p*-dopant. While C or Be can be used as an alternative *p*-dopants another approach is to use GaInP within the cell structure which leads to reduced Zn. The reported performance of transfer printed cells fabricated from each device layer in the system was nearly indistinguishable [32]. Thus, there are many routes to scaling, distributing and integrating PV cells on substrates of choice. (Fig. 5).

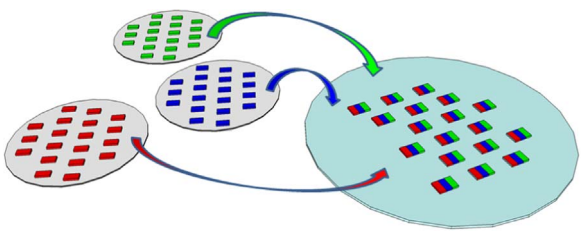

Fig. 4. Schematic diagram illustrating the co-integration of devices from different starting wafers onto a common substrate for obtaining both enhanced functionality and low cost sub-systems.

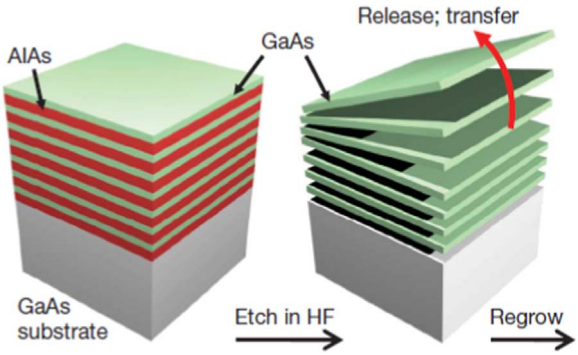

Fig. 5. Schematic illustrating the realisation of multi-levels of structures with a single growth stage thereby increasing the quantity of devices while also allowing for the reuse of the substrate. Reprinted with from Ref. [31].

Mechanical stacking of PV cells is one way to circumvent the lattice matching needed when growing multi-junction PV cells in a single step epitaxy. Using stacking it should be possible to reach overall cell efficiencies well in excess of 50%. The advantages for transfer print over conventional stacking are that it can handle the multiple material types and small cell dimensions (< 1 mm) as needed, provide an accurate alignment of the metal grids of the cells to minimise shading effects and it allows the use of thin film materials that minimise reflections between the cells. Sheng et al. [33] stacked a 3-junction cell on a Ge sub-cell to realise a 4-terminal PV cell with an efficiency of 43.9% at 1000 suns. A high refractive index As_2Se_3 interlayer was used to reduce the Fabry-Perot effect between the stacked cells. By replacing the bottom Ge cell with an InGaAs cell (bandgap of 0.8 eV) an efficiency of 44.1% at 690 suns was obtained [34].

Another advantage for PV cells is the ability to realise cells which are surrounded by low refractive material, ideally air, which leads to increased total internal reflection of the generated luminescence and thus photon recycling. This principle has been used to show that thin film GaAs coupons surrounded by air have a longer carrier lifetime and a resulting higher open circuit voltage [35].

850 nm emitting VCSELs are in widespread use especially in short reach optical interconnections with many companies reporting total sales in excess of 10^9 lasers. The device structure consists of a complex multilayer with total thickness of the grown layers being 5–10 μm. The active area of the device is typically 10 μm in dimension while the chip size is typically 250–300 μm. Thus, there is a great opportunity to increase the number of devices per unit area and to co-integrate VCSELs with the electronic drive and receive circuits to form compact transceivers. Accurate placement of individual thinned VCSELs with respect to driving circuits have been demonstrated [36]. Furthermore, the VCSEL is a very general low threshold laser source with many possible applications and many benefits from integration are evident. Kang et al. have transferred VCSEL arrays for opto-fluidic fluorescence excitation [37]. A specific $Al_{0.95}Ga_{0.05}As$ layer was incorporated in the layer structure. Thermal issues were found to be important when the devices were transferred to low thermal conductivity substrates such as glass or plastics. Operating the devices with 500 ns pulses was found to be a practical way to mitigate the thermal effects with comparable performance obtained on the native substrate as on the new glass substrate.

Edge-emitting lasers can provide high optical powers especially in a single spatial mode which is necessary for many applications. One example is in Heat Assisted Magnetic Recording (HAMR) where multiple milli-Watts of power coupled into a delivery waveguide are needed. Additionally, it is desirable that the laser be co-integrated with the other magnetic components suggesting that transfer print of thin lasers could be a good solution. To that end transfer print of edge-emitting lasers have been demonstrated on foreign substrates [38]. Coupons of the 824 nm emitting laser material were released and then transferred to Si substrates without using an adhesive layer. Due to the flexibility of the ~5 μm thin coupons with a footprint of 300 μm × 400 μm the bonding is remarkably strong. The lasers were then fabricated using etched-facets on the Si substrate allowing lithographic alignment with other features on the new substrate. Processing temperatures of at least 350 °C were possible. The intimate bond of the device to the substrate allowed the lasers to operate in continuous wave mode delivering > 5 mW at current of 100 mA for a substrate temperatures of 100 °C. The alternative approach where lasers are pre-fabricated and then transfer printed onto a Si substrate [39] was also demonstrated. In that case an HCl based etch of the $Al_{0.95}Ga_{0.05}As$ was found to be superior to a HF due to the presence of SiO_2 and Ti on the fabricated laser chip. When a polymeric adhesive layer was used for the bonding it was found that the lasers only operated in pulsed mode. Thermal simulations confirmed that the high thermal resistance was the cause. When the lasers were transfer printed onto an indium-silver (97% In/3% Ag) paste the laser was found to operate in continuous mode with comparable electro-optic performance to that achieved on the native substrate.

3.2. Transfer print of GaN devices

GaN materials are most widely used for visible (blue-green), UV emitting LEDs and edge emitting lasers emitting in the 380 nm to 520 nm range. The device structures are grown on a variety of substrates ranging from low-cost sapphire and Si to higher cost bulk GaN and SiC. GaN structures grown on $< 111 >$ oriented Si can be easily undercut by using aqueous potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) solutions. After the initial demonstration of thin ribbons of GaN released from Si [19], arrays of LEDs were fabricated, under-etched while held in place by thin GaN anchors, released and transferred to a range of

substrates followed by planarization and interconnection [40]. During the underetching with KOH the metal tracks on the LEDs needed to be protected by a layer of SiN. When the LEDs are operating at low current densities the interconnect tracks can dissipate the excess heat. For high current density operation it is necessary to use a high thermal conductivity substrate. Diamond with a thermal conductivity of 2200 W/m.K was used to show operation of the LED to a current density of 250 A/cm^2 [41]. It should be noted that GaN based LED structures can have a large amount of inbuilt strain which can result in deformation of the released coupons. Therefore, it is an advantage to releasing smaller dimensioned devices. Full colour displays based on micron scale transfer printed LEDs are now being developed. LEDs as small as 3 μm × 10 μm have been transfer printed and interconnected [42] on transparent substrates. Due to the small area occupied by the LEDs and interconnect, the display is mostly transparent when it is off. The concept of repair prints was also demonstrated [42].

Other than Si, the growth substrates for GaN devices are chemically inert thus requiring complicated techniques to effect release of the epilayers. Transfer of the wafer to a sacrificial substrate in conjunction with LLO is the most used method for lasers grown on sapphire substrates [43]. Photoelectrical chemical (PEC) etching of sacrificial InGaN superlattices can also be utilised to release coupons of GaN LED material [44].

3.3. Transfer print of InP devices

As discussed above, silicon photonics is emerging as a very scalable platform for integration of photonic components for use in communications and for sensing applications. Already, high performance photonic circuits are readily being achieved on large sized Si wafers with record precision. The first market opportunity for these circuits is likely to be in the emerging large sized data centres which will have a communication fabric based on single mode fibre at many links operating at 1300 nm/1550 nm wavelengths where Si is transparent. While Ge can be integrated in a straightforward manner to act as a photodetector, it is more complex to integrate a gain providing material as needed for lasers. The best materials to provide the amplification are based on InGaAs(P) quantum wells grown on InP substrates with the current solution using wafer bonding and substrate removal as described earlier. Transfer print potentially allows gain and detecting materials to be integrated easily on the full wafer scale (200 mm diameter), with requirement on flatness only local to the device location, very efficient use of the materials and the ability to integrate many different materials types for optimum function.

Recently, prefabricated 1550 nm emitting etched-facet lasers have been transfer printed to silicon substrates with and without a metal bonding layer [45]. A 1 μm thick buried InGaAs layer was used as the release layer. Ferric chloride ($FeCl_3$) at low temperature (~2 °C) was used to achieve highly selective (> 2000 with respect to InP) undercut etching. Continuous wave lasing was demonstrated and improved thermal sinking was obtained for devices printed onto a metal bonding layer. Fig. 6 shows the printing of 4 InP lasers on Si with the resist used for the anchoring still in place. A close up of the facet region is shown where the ridge waveguide and contact is evident. Finally, the adhered laser was a cross sectioned and the intimate contact between the III-V material (InP) and the Si substrate is seen.

The use of InP for silicon photonics is starting to develop and a first integration of the co-integration of 1550 nm emitting quantum well material with a Si waveguide (SOI) has been reported [46]. The device was optically pumped comparable performance to that of wafer bonded components.

3.4. Transfer print of SOI based devices

The SOI platform, itself formed by wafer bonding, is the basis for the realisation of advanced electronic circuits and photovoltaic devices. These devices can be readily transfer printed due to the high etch selectivity for the buried oxide with respect to Si when using HF solutions. Initially the transfer of thin film transistors was demonstrated. Subsequently, the large-scale transfer of foundry-processed CMOS circuits (dimensions of 167 μm × 50 μm × 8 μm) anchored with Si tethers was demonstrated with negligible impact on the electrical characteristics. The topography of the chip was not a problem. The circuits were used in the demonstration on an active matrix organic LED display with 10's of thousands of circuits printed with a 3σ positional accuracy of ± 1.5 μm [47].

SOI structures are of special interest for the metasurfaces that can be created by nanostructuring the high index contrast system of

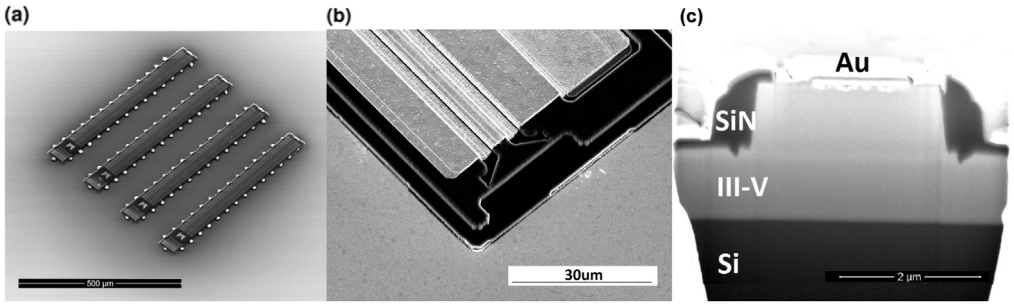

Fig. 6. SEM images of (a) an InP-based 1550 nm laser array transfer printed to Si with the resist anchors still in place, (b) close up of the etched facet region of the laser after resist removal and (c) cross-section of the ridge waveguide laser printed on Si.

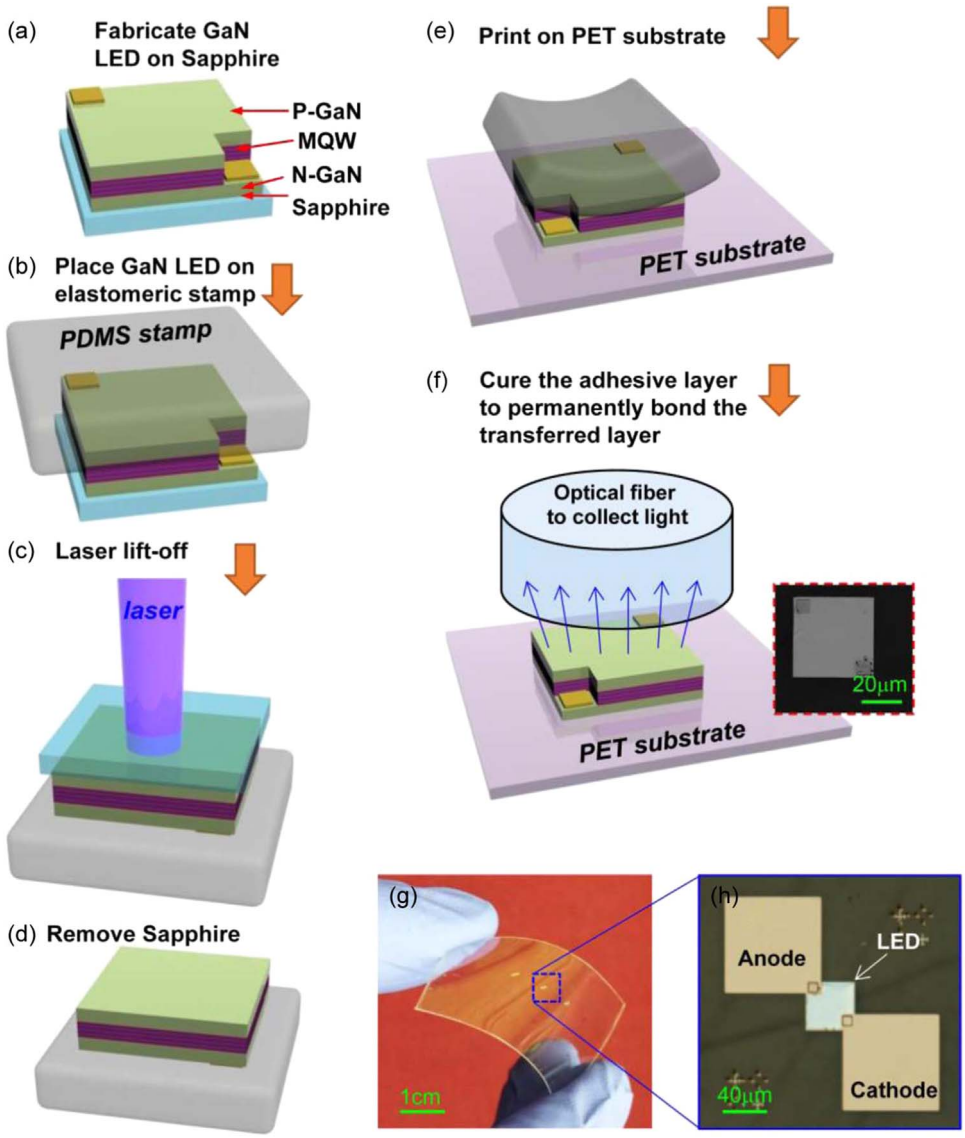

Fig. 7. Schematic of the fabrication process for GaN LEDs on a PET substrate using a laser lift-off (LLO) and transfer-printing method. (a) Fabrication of GaN LEDs on a sapphire substrate. (b) Place fabricated GaN LEDs on a PDMS elastomeric stamp. (c) Laser lift-off from the sapphire side. (d) Gentle removal of the sapphire substrate. (e) Transfer-print GaN LED layer onto the PET substrate. (f) Curing of the adhesive layer to permanently bond the transfer-printed GaN LED layer. An optical fiber is placed on top of the GaN layer for light collection. (g) Image of fabricated LED array on a bent PET substrate. (h) Zoomed-in image of an individual LED on PET (Reprinted from Ref. [50]).

Si and oxide. Particularly, photonic crystal cavities and high bandwidth, high reflection (> 99%) mirrors can be achieved using layers that are much less than 1 μm thick. These membrane reflectors can replace the multilayer quarter wave distributed Bragg reflector mirrors used in the VCSELs discussed above. As a result much thinner VCSELs can be realised. To demonstrate this, a compact VCSEL was created by stacking an InGaAsP quantum well structure and a released Si membrane reflector on a SOI membrane reflector [48]. Optically pumped lasing was demonstrated. The cavity thickness was less than 2 μm opening the possibility of simple integration with CMOS electronics. A wide variety of nanomembrane (NM) structures can be realised and used in novel ways [49].

4. Transfer print to flexible substrates

4.1. Flexible light emitting diodes

A simplified method to make flexible blue LED based on transfer printing is proposed by Seo [50]. For the growth of blue LED epilayers the GaN buffer layer on the sapphire substrate needs to be at least a few microns thick in order to achieve an acceptable GaN

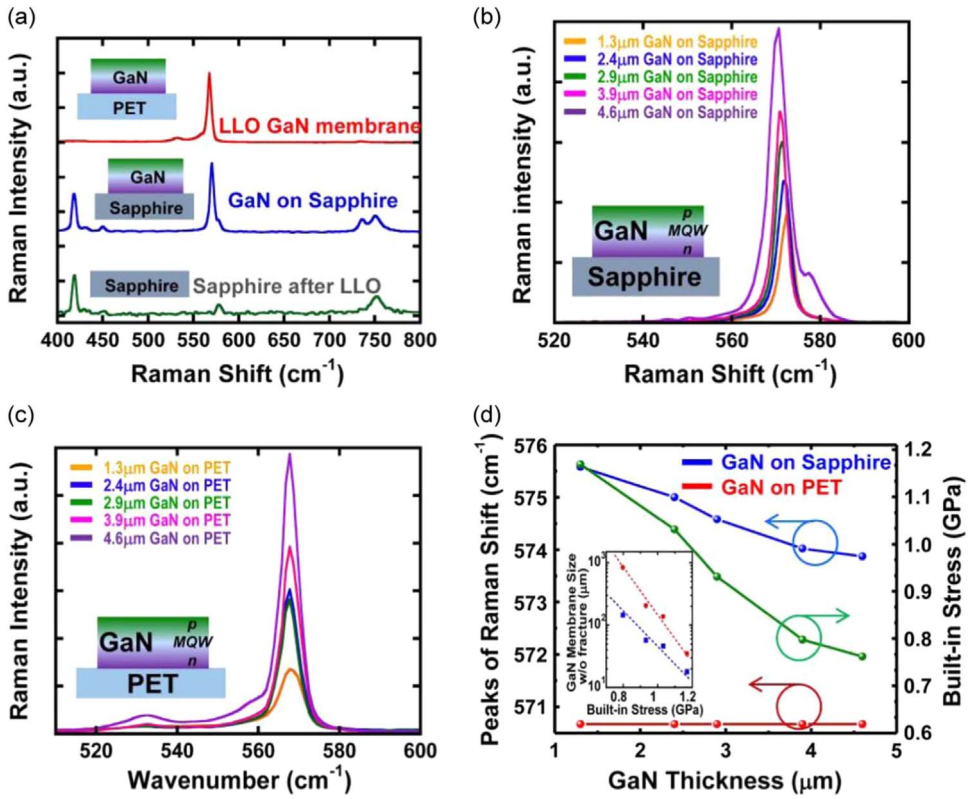

Fig. 8. (a) Raman spectra of the GaN LED structure on a sapphire substrate (blue), sapphire substrate after laser lift-off (green), and the LLO GaN layer on a PET substrate (red). (b) Comparison of Raman spectra of the GaN LED layers with various thicknesses grown on a sapphire substrate. (c) Comparison of Raman spectra of the LLO GaN LED layers with various thicknesses after transfer-printed on a PET substrate. (d) Raman peak and the calculated built-in stress as a function of the GaN layer thickness. Blue: Raman peak of the GaN layer grown on a sapphire substrate (i.e., before LLO); Red: Raman peak of the GaN layer transferred on a PET substrate after LLO. Green: Calculated built-in stress measured from the GaN layer grown on a sapphire substrate. The lines are used for guiding the view of the data points. The inset plots the dependence of the released GaN membrane size (Red: width; Blue: length.) versus built-in stress (Reprinted from Ref. [50]). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

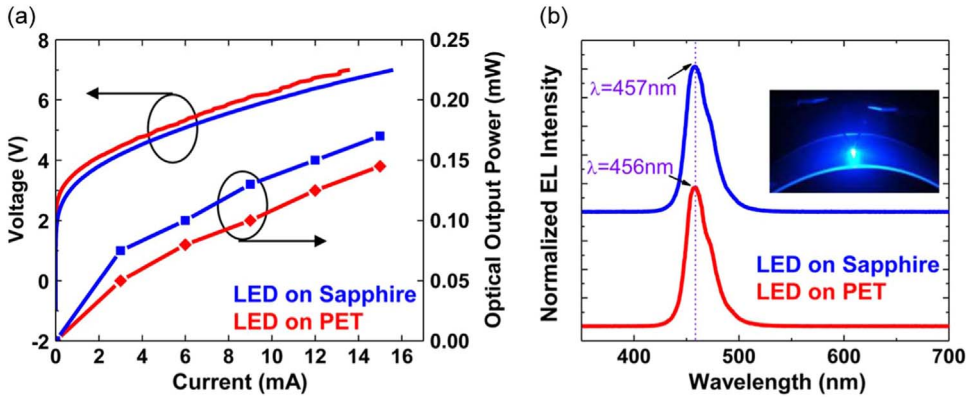

Fig. 9. (a) Light output power-current-voltage (L-I-V) characteristics and (b) electroluminescent light spectra of the GaN LEDs on sapphire substrate (before laser lift-off) and PET substrates (after transfer-printing). The insert in (b) shows the light emission images on a PET substrate (Reprinted from Ref. [50]).

crystal quality due to lattice mismatch. As a result, the built-in stress would induce fractures when LLO is applied to separate the InGaN/GaN QWs GaN structure from the sapphire substrate if not tightly bonded to a mechanically compatible substrate. While the mechanical rigidity of PDMS is controllable by varying the mixing ratio between PDMS solution and curing agent, the bonding strength between PDMS and GaN wafer is strong enough to sustain the stress, and the built- in stress is later relaxed during printing process on polyethylene terephthalate (PET) stretchable substrates (Fig. 7(e)). Compared with conventional LLO process, removal of bonding substrate is eliminated [51,52], thus reducing the process complexity and improving the transfer yield. Fig. 7 shows the main process flows and LED chip image on PET.

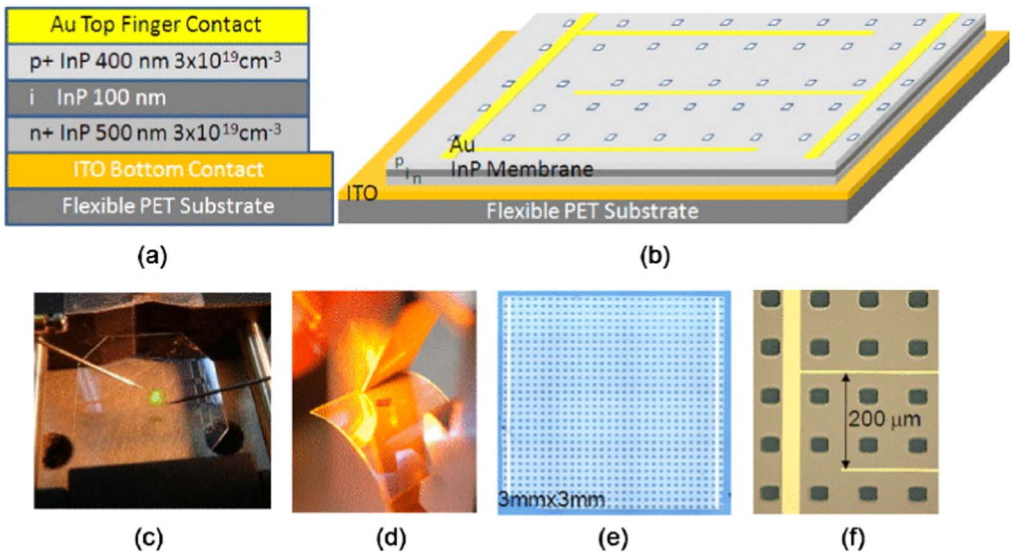

Fig. 10. (a) Cross-sectional, and (b) three-dimensional views of flexible InP p-i-n NM PD on ITO/PET substrate. (c) A micrograph of fabricated flexible InP PD under test. [(d)–(f)] Zoom-in views of a fabricated large area (3×3 mm^2) InP PD on flexible PET substrate (Reprinted from Ref. [57]).

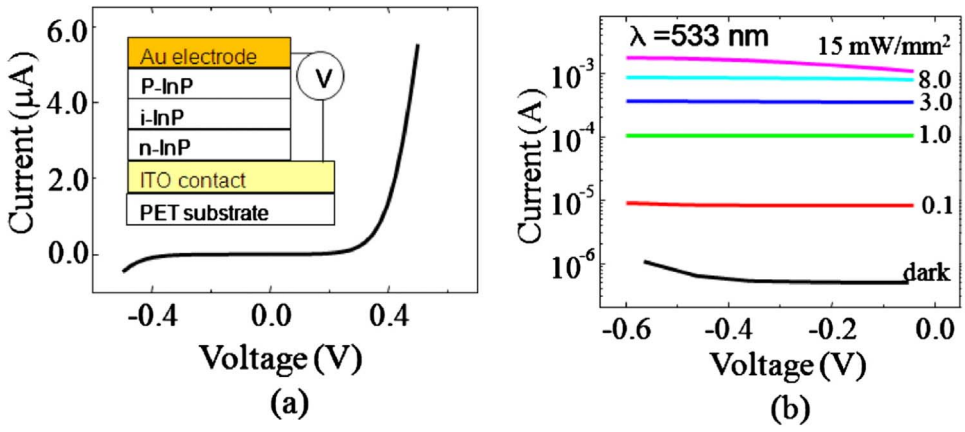

Fig. 11. Measured flexible InP p-i-n PD characteristics. (a) Measured dark current-voltage characteristics. (b) Measured photocurrents at different incident optical powers for a 533 nm wavelength light source (Reprinted from Ref. [57]).

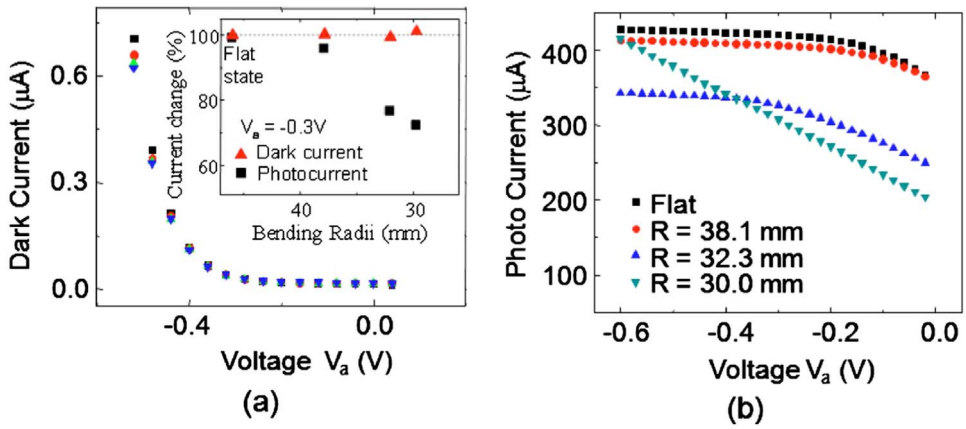

Fig. 12. Measured bending characteristics for a fabricated flexible InP PD at different bending radii, R. (a) Dark currents; and (b) photocurrents. The relative changes in measured dark and photocurrent are also shown in the inset of (a), at a bias voltage of -0.3 V (Reprinted from Ref. [57]).

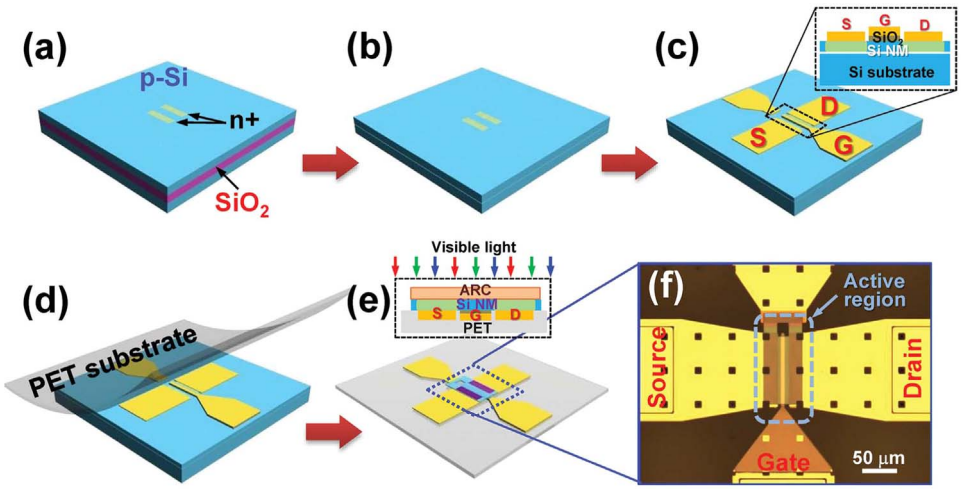

Fig. 13. Schematic illustration of the device fabrication process flow; (a) Beginning with forming n+ regions by ion implantation of source/drain regions to achieve an ohmic contact, (b) Releasing Si NM by selective etching of a buried oxide layer; (c) Metallization by e-beam evaporation to deposit source/drain electrodes, and a stack of gate/gate dielectric, d) Transfer printing fully fabricated devices to adhesive layer-coated PET substrate; (e) Spin-coating a protection layer on top of the surface, (f) Microscopic image of a finished flexible phototransistor. Insets in (c) and (e) depict the cross-sectional view of device (Reprinted from Ref. [62]).

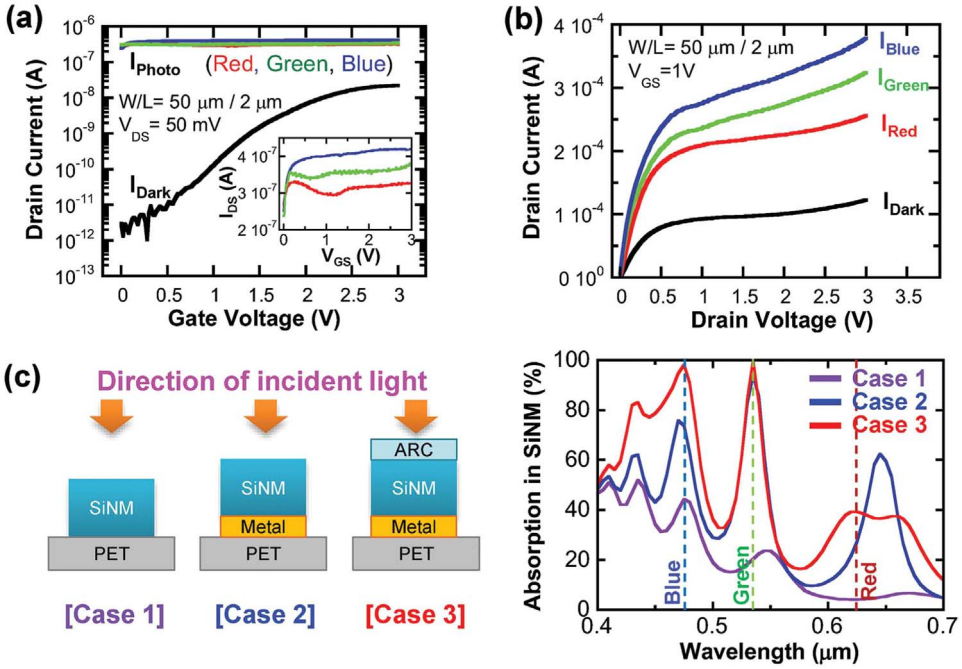

Fig. 14. (a) Drain current–gate voltage characteristics (I_{DS}–V_{GS}) at $V_{DS}=0$ V. Inset shows the magnified plot of photo currents. (b) Drain current–drain voltage characteristics (I_{DS}–V_{GS}) under dark and illumination with various light sources (red, green, and blue) onto flexible phototransistors. I_{DS}–V_{GS} curve under $V_{GS}=1$ V for photo-to-dark current ratio shows as high as $\approx 1\times 10^{5}$. (c) (left) Three layer structures used to simulate the light absorption of Si NM, (right) and their corresponding simulated absorption of Si NM i) without any layers, ii) with the metal reflector underneath the Si NM, iii) with the metal reflector underneath the Si NM and SU-8 ARC layer on the top of Si NM, respectively. Dashed line denotes blue (473 nm), green (532 nm), and red (632 nm) wavelengths (Reprinted from Ref. [62]). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Raman spectroscopy measurements are taken on the GaN LED on sapphire substrate and on the PET substrate to examine the built-in stress before and after the transfer, as in Fig. 8(a). Fig. 8(b) shows a red shift of the Raman peaks when the GaN layer is decreased from 4.6 μm to 1.3 μm, which indicates that the thicker GaN layer has reduced stress. On the PET substrate, the different GaN layer thickness show identical peaks and these are same as for the unstressed GaN, which indicated a full relaxation of the built-in stress of the GaN after transferring onto the PET. The Raman peaks shift and built-in stress comparisons between sapphire and PET substrate is plotted in Fig. 8(d) for different GaN thickness.

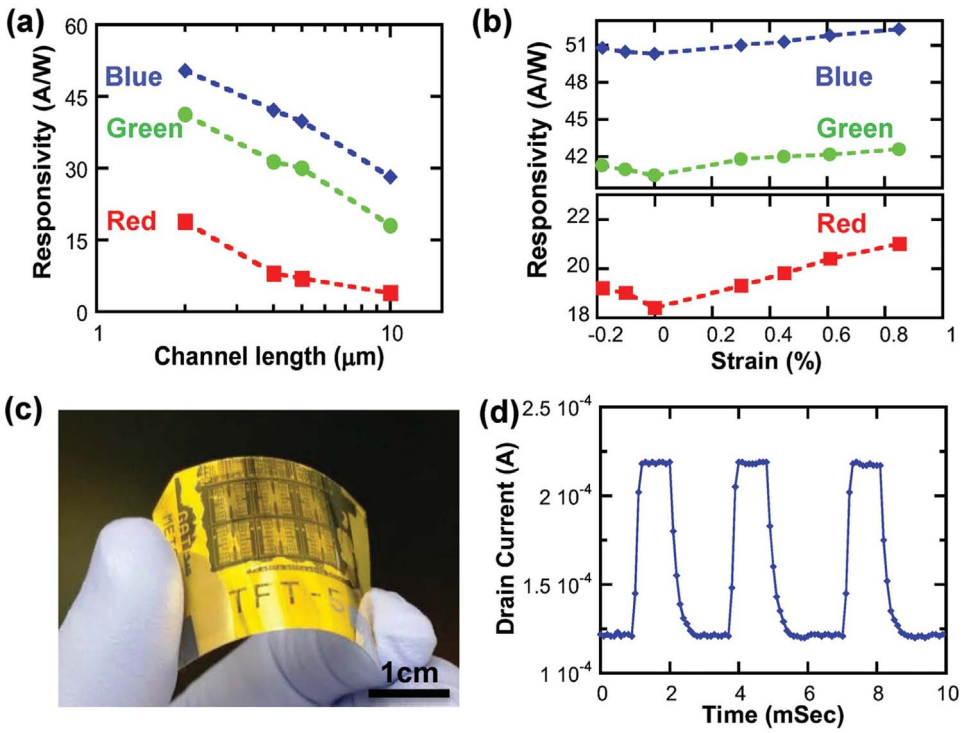

Fig. 15. (a) A trend of responsivity with respect to channel lengths from 2 to 10 μm. The channel width and bias point were fixed at 50 μm and at $V_{GS}=1$ V and $V_{DS}=3$ V. (b) Responsivity under bending condition measured at a fixed voltage bias point of $V_{GS}=1$ V and $V_{DS}=3$ V. (c) Optical image of the flexible Si NM phototransistor on a bent substrate. (d) Modulated photocurrent under pulsed 5 mW green laser measured at a fixed voltage bias of $V_{GS}=1$ V and $V_{DS}=3$ V (Reprinted from Ref. [62]). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

LED chips on sapphire and flexible PET substrate are measured and compared in regarding to both electrical and optical performances. From the current voltage (I–V) and light current (P-I) shown in Fig. 9(a), the LEDs on PET substrates have slightly smaller current at same voltage bias and less than 10% reduction in optical output power at the same current. This may be attributed to the heat dissipation issue induced by the lower thermal conductivity of PET when compared with sapphire. The optical spectra at 10 mA for the two cases (Fig. 9(b)) show that the peak is shifted from 457 nm to 455 nm after transfer printing on the PET substrate, which is speculated to originate from the relaxed stress and bandfilling effects [53–55]. This method of using PDMS as the LLO and transfer holder provides a simplified approach to fabricate GaN LEDs on any flexible substrate without performance degradation.

4.2. Large-area InP nanomembrane based flexible photodetectors

Flexible optoelectronic device has a variety of applications, such as flexible imaging, conformal photonic systems, and bio-photonics. Due to the rigidity and fragility of bulk crystalline semiconductor materials, conventional flexible devices are mostly based on organic or amorphous material. The transfer printing technique allows one to combine the advantages of high performance of inorganic crystalline material with mechanical flexibility of thin NM with nanometers scale [56]. For particularly fragile InP material, large-area release and transfer remains challenging. A frame-assisted membrane transfer (FAMT) process is proposed to deal with large-area and easy-to-break membrane material [57]. A 3×3 mm^2 InP NM is released from native substrate and transferred to PET substrate. The InP structure consists of p-i-n photodetecting diode and a InGaAs sacrificial layer underneath [58], which will be etched away during wet etching. Before the etch and release process, two frame finger-shaped metals are deposited on top of InP NMs, acting both as anode metal contact and mechanical support for the fragile large-area InP NM. As Fig. 10(a) and (b) depict, the InP NM is transferred onto an indium tin oxide (ITO)/PET substrate and ITO functions as a transparent cathode metal.

The photodetecting performances are measured, as shown in Fig. 11, the dark current is as low as 1 μA at reverse bias of -0.5 V. Light at 533 nm wavelength is incident on the devices and the photocurrent shows a near linear trend versus the incident light intensity (Fig. 11(b)). The responsivity for 533 nm is calculated to be 0.12 A/W and agrees with the calculation for the 1 μm thick InP with an absorption coefficient of 10^5 cm^{-1}.

To investigate the effect of bending to the device characteristics, the photo responsivities under different bending radii are compared under incident power density of 3 mW/mm^2 at 533 nm. No obvious degradation was noticed with bending radii up to 38.1 mm for both dark current and responsivity. If more bending is applied, the photocurrent began to decrease as shown in Fig. 12(b) and inset of Fig. 12(a), which may be attributed to the strain-induced absorption change of Si NM.

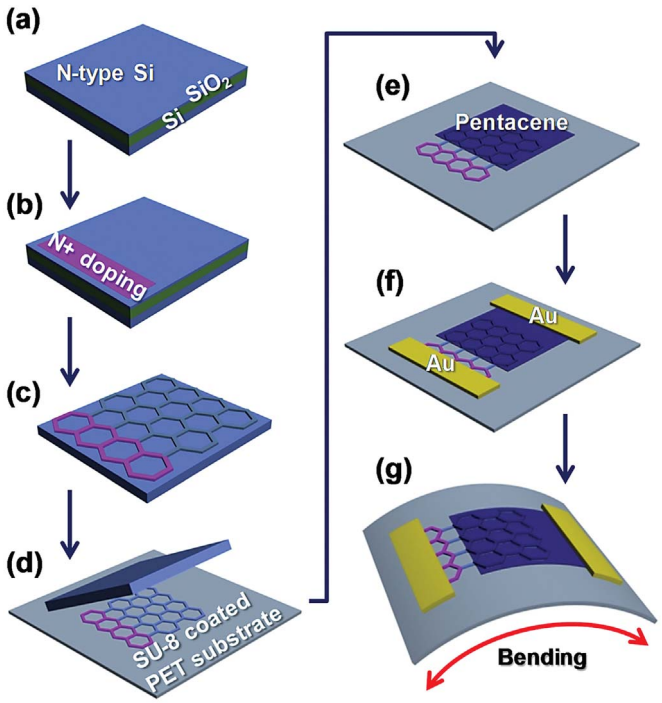

Fig. 16. Schematic illustration of the fabrication process flow. (a) Beginning with SOI (340 nm n-type top Si and 2000 nm buried oxide layer). (b) N+ region was selectively doped to create an ohmic contact area using spin-on dopant. (c) Patterning of active Si NM by RIE etching, followed by wet etching to undercut buried oxide layer. (d) Transfer printing released Si NM to adhesive layer coated PET substrate with a PDMS stamp. (e) Evaporation of pentacene on top of Si NM to form an organic-inorganic p-n junction. (f) Metallization with e-beam metal evaporation to complete the fabrication process. (g) The finished device is subject to bending (Reprinted from Ref. [63]).

4.3. Silicon nanomembrane based flexible phototransistors

The metal oxide semiconductor field-effect transistors (MOSFETs) have been reported to demonstrate outstanding characteristics in photosensitivity and responsivity [59–61]. Compared with the common p-n junction based photodetectors, Phototransistors possess exceptional photo-sensing capability in terms of quantum efficiency. Recently, we demonstrated a flexible phototransistor based on thin film single crystalline silicon NMs [62]. To maximize the exposure area to the light, the Si NM is flip-transferred on flexible substrate, thus the photo-sensing Si area is not limited by channel dimension, as the light is not blocked by the gate metal as in conventional phototransistors. On the other hand, the flip transfer benefits the phototransistor responsivity, as the gate electrode beneath the Si acts as a high reflection mirror, which increases the light absorption portion in the absorptive Si. As a result, the proposed structure not only takes advantage of the higher photo-sensing ability of phototransistors, but also further improves the light absorption induced by large exposure area and bottom metal mirror reflection.

As shown in Fig. 13(a), p type doped SOI substrate with 270 nm Si top layer is partially heavily doped to n^+ region by ion implantation, which are later deposited with metal to form ohmic contacts for source and drain, respectively (Fig. 13(c)). Before the metal e-beam evaporation, the oxide box layer is etched away to release the Si NM from the Si substrate, then the Si NM is picked up by PET substrate with an adhesive layer to assist the adhesion between PET and Si NM (Fig. 13(d)). Furthermore, to reduce the surface reflection, an anti-reflection layer (SU-8 2002) is coated on top of flipped Si NM. The finished phototransistor on flexible PET substrate is shown in microscopic image as Fig. 13(f).

Dark current and photocurrent with red (632 nm), green (532 nm) and blue (473 nm) laser illuminations are measured for the phototransistors with a 50 μm wide and 2 μm long gate channel. There are two operation conditions, one is under low bias to obtain high photo-to-dark current ratio, and the other is under normal operation voltage to achieve high responsivity. For the first operation condition, the phototransistor yields up to 10^5 of photo-to-dark ratio under 0.5 V of V_{GS} and 0.05 V of V_{DS}, while the responsivity only shows 0.04 AW^{-1} due to the very thin Si NM used for absorption gating layer. As gate bias increased to 1 V, the photo-to-dark ratio drops to 11, but the drain current increase significantly as shown in Fig. 14(b). The responsivity at voltage bias of $V_{GS}=1$ V and $V_{DS}=3$ V are calculated to be 51, 41, and 18 AW^{-1} under red, green, and blue light incident light, respectively.

The effects of metal reflector and anti-reflection coating on the light absorption enhancement is investigated as in Fig. 14(c), light absorptions for three cases are simulated in the 400–700 nm visible wavelength range, which shows that the average absorption percentage in Si NM with reflector and anti-reflection layer is increased more than twice from 20.2% to 48%, compared with Si NM directly on the PET substrate.

Furthermore, devices with different Si NM channel active area dimensions are also fabricated and measured under different tensile and compressive strain (Fig. 15(a) and (b)), it is found longer gate shows decreased photo responsivity, and under bending at

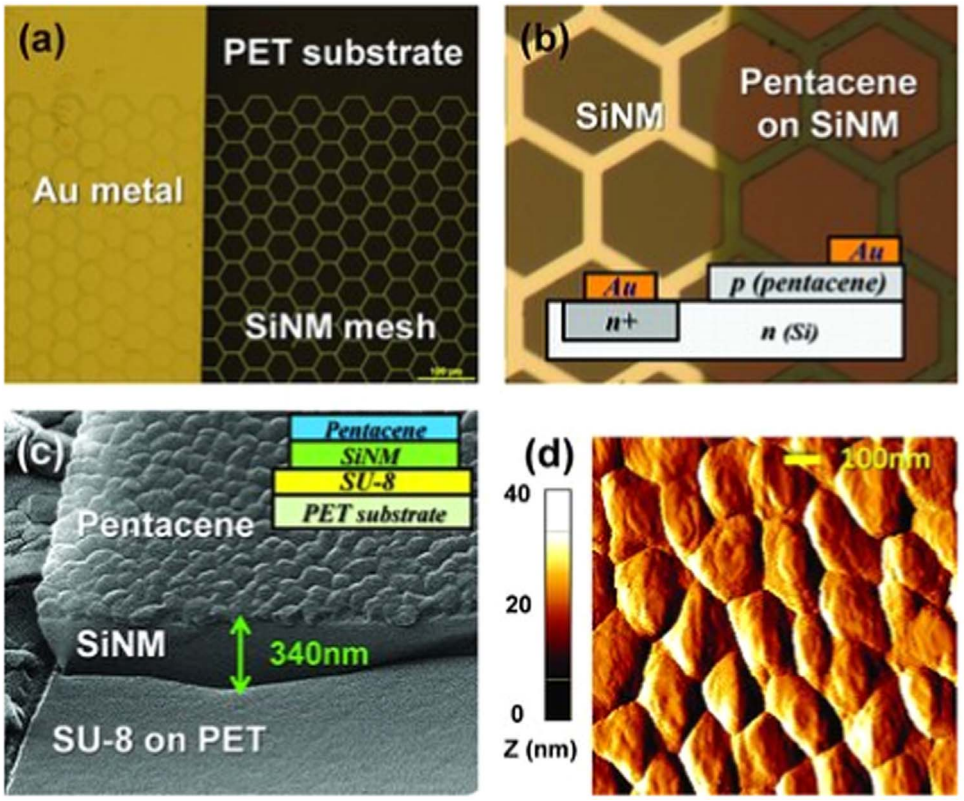

Fig. 17. (a) Microscopic image of transferred SiNM grid on PET substrate. (b) Microscopic images of SiNM (left)/pentacene (right) heterojunction. The inset shows the cross section of the heterostructure. (c) SEM image of SiNM and deposited pentacene layer sitting on SU-8 coated PET substrate. The inset shows the detailed layer structure. (d) AFM image of deposited pentacene on Si NM. The average pentacene grain size is 180 nm (Reprinted from Ref. [63]).

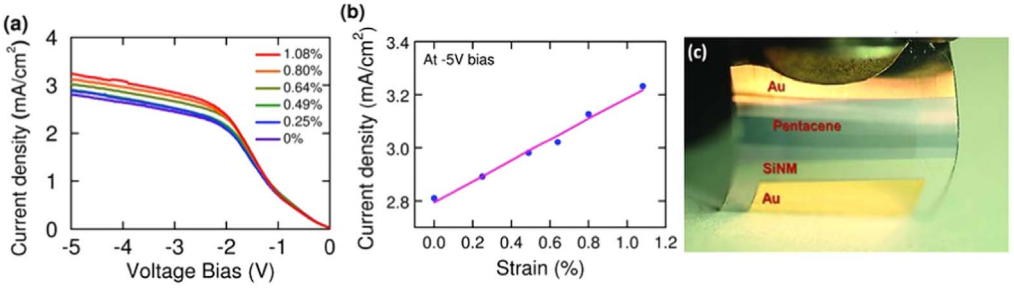

Fig. 18. Characteristics of Si NM-pentacene diode under mechanical bending. (a) Measured photocurrent of the diode under different bending strain. (b) Plot of photocurrent change as a function of strain. (c) An optical image of the diode under bending (Reprinted from Ref. [66]).

curvature radii of 15 mm, the device is proved to be stable in terms of responsivity (Fig. 15(b) and (c)), which provides great promises for flexible photodetecting applications.

4.4. Flexible photodetecting p-n diode between pentacene and Si nanomembrane

Heterogeneous *p-n* junctions between organic and inorganic material has also been demonstrated by transfer printing. It is reported in Ref. [63] that an *n* doped single crystal Si NM, which is transfer printed on a plastic substrate, forms a heterogeneous *p-n* diode with a *p* doped pentacene. Fig. 16 shows the schematic fabrication process flow. The SOI substrate with N type Si is partly heavily doped to from an ohmic contact region (Fig. 16(b)), and the 340 nm Si NM is etched to create the hexagonal shape for transparency and flexibility purposes (Fig. 16(c)). Then the Si NM is released and transferred on an SU-8 coated PET substrate (Fig. 16(d)), and pentacene is evaporated on top of SiNM, forming a heterojunction between inorganic Si and organic pentacene (Fig. 16(e)). For the last step, gold metal is deposited on n^+ Si area and pentacene as contacts (Fig. 16(f)).

Fig. 17(a) and (b) shows the microscopic picture of the SiNM with hexagonal meshed pattern on PET substrate under different magnifications. The vertical p-n diode structure can be clearly seen in the inset schematic drawing. The scanning electron microscopy

(SEM) image of the device is shown in Fig. 17(c) and atomic force microscopy (AFM) shows the pentacene surface with average grain size of 180 nm (Fig. 17(d)).

The photodetecting characteristics with different incident light wavelengths are measured, and the photo responsivity is 0.7 A/W for 532 nm illumination. The external quantum efficiency peak is 21.9% at 632 nm, over wavelength range from 473 nm to 905 nm. The effects of mechanical flexibility on device performances are also examined, Fig. 18 shows the *I-V* characteristics of the Si-pentacene diode under different bending strain from 0.25% to 1.08%, which indicates nearly no degradation. The photocurrent versus bending strain is depicted as well in Fig. 17 (b) that the external quantum efficiency increases by about 15% under bending strain of 1.08%. The photocurrent enhancement under bending condition could be explained by mobility improvement, given that tensile strain on crystal lattice could increase the carriers mobility of pentacene [64,65] and Si NM as well [66,67]. With thickness of only 340 nm and meshed hexagonal pattern, the Si NM and pentacene heterojunction structure on PET is highly transparent for visible light as Fig. 18(c) shows.

The demonstrated optically transparent, photosensitive and flexible heterogeneous *p-n* diode between organic pentacene and inorganic Si NM based on transfer printing, extends the boundaries of the transfer printing technique to an even broader choice of materials combinations.

5. Conclusions

It is clear that PDMS based transfer printing is a highly versatile technique for heterogeneous integration of photonic devices with other components and circuits on both rigid and flexible substrates. We have shown here that the technique can be applied to a wide variety of compound semiconductor and silicon devices through appropriate engineering of the layers within the material system. It can also be applied, for example, to passive devices such as dielectric mirrors, miniature optics and to monolayer-scale layers of InAs, and new materials such as graphene and dichalcogenides. As a result, the technique is likely to find widespread adoption enabling photonics to be integrated in a seamless manner into smart subsystems. Such systems can involve sensing, actuating and energy harvesting components each made from dissimilar materials. The interconnect wiring of the components can be performed using classical lithographic techniques or can be performed in combination with 3D printing for both the electrical and photonic wiring. From the scientific point the technique enables the realisation of completely new device configurations. Many of these concepts have yet to be explored.

The technology can lead to substantially reduced costs associated with photonic components especially due to the simplification of packaging by the co-integration. The use of flexible or biocompatible platforms will enable a wide range of new opportunities for photonics. The technology is at an early stage in its development and many advances can be expected from the realisation of circuits to the establishment of mature foundry-compatible processes with associated design rules and layout verification. The technique is likely to be developed for specific applications initially before becoming widely accessible through electronics and MEMS foundries.

Acknowledgements

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