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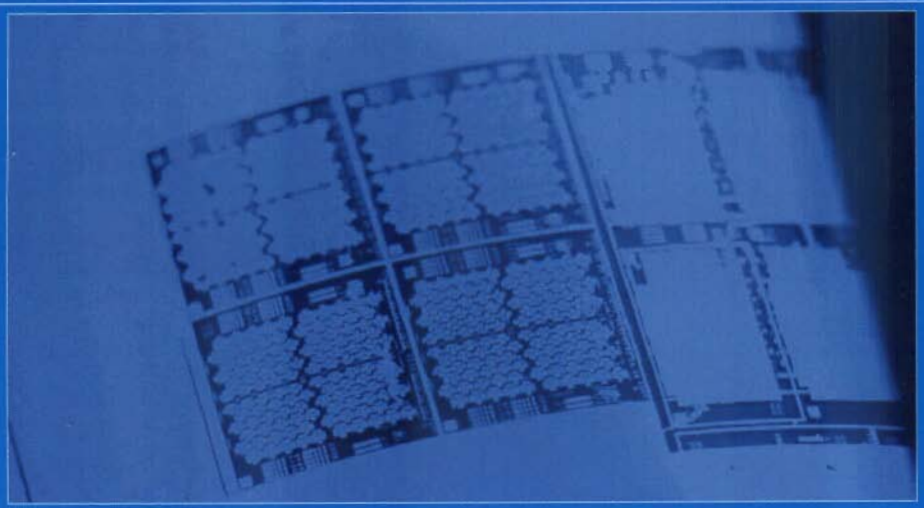

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High-performance flexible thin-film transistors fabricated using print-transferrable polycrystalline silicon membranes on a plastic substrate

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Abstract

Inexpensive polycrystalline Si (poly-Si) with large grain size is highly desirable for flexible electronics applications. However, it is very challenging to directly deposit high-quality poly-Si on plastic substrates due to processing constrictions, such as temperature tolerance and residual stress. In this paper, we present our study on poly-Si membranes that are stress free and most importantly, are transferrable to any substrate including a low-temperature polyethylene terephthalate (PET) substrate. We formed poly-Si-on-insulator by first depositing small-grain size poly-Si on an oxidized Si wafer. We then performed high-temperature annealing for recrystallization to obtain larger grain size. After selective doping on the poly-Si-on-insulator, buried oxide was etched away. By properly patterning the poly-Si layer, residual stress in the released poly-Si membranes was completely relaxed. The flat membrane topology allows the membranes to be print transferred to any substrates. High-performance TFTs were demonstrated on the transferred poly-Si membranes on a PET substrate.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Electronic circuits built on flexible substrates have great potential for a number of applications, including displays, solar cells, smart cards, RF tags, and implants compatible with biosystems [1–3]. Organic semiconductors and amorphous silicon (a-Si) [4] were traditionally used for these applications. Of the important advantages of using these two types of materials is that they can be directly applied to low-temperature plastic substrates. Recently single-crystal Si and GaAs were also made on plastic substrates for thin-film transistor (TFT) fabrication [5–7] via release and transfer processes. In comparison to single-crystal Si, polycrystalline Si (poly-Si) is much less expensive in terms of material cost. But, relatively high-performance TFTs can be made of poly-Si and the performance of poly-Si TFTs is much better than those made of organic semiconductors and a-Si. However, obtaining high-quality poly-Si requires the use of substrates with high temperature tolerance [8–11] and/or complicated crystallization techniques [12–16], both of which severely limit the use of poly-Si for flexible electronics. In addition, the residual stress in film was not easily relaxed in the prior demonstrated films. Residual stress often causes problems

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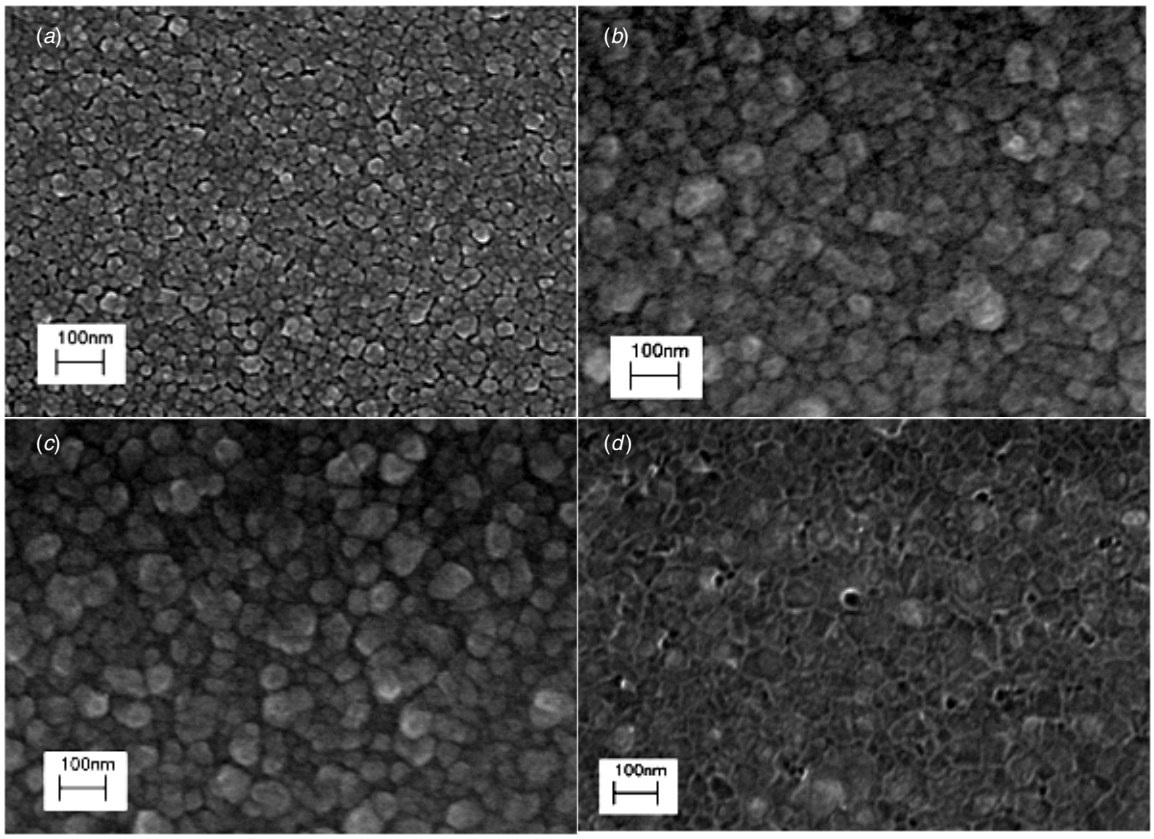

Figure 1. Planar SEM of a poly-Si-on-insulator under different conditions, indicating the grain size changes with the increase of annealing time. The scale bar is 100 nm for all conditions: (*a*) as-deposited, (*b*) 1 h annealing, (*c*) 2 h annealing, (*d*) 5 h annealing.

(such as warping) for very soft substrates. Here we present a simple and inexpensive approach to high-quality poly-Si that is transferrable to any substrate, including low-temperature plastic substrates. Although similar release and transfer techniques were used for the single-crystal Si membranes [7, 17], they cannot be easily applied to poly-Si without modifications. Before we can apply the release and transfer techniques, we first formed a poly-Si-on-insulator and performed the necessary high-temperature processing steps. By performing the high-temperature processes on the original host Si substrates for poly-Si, high-performance poly-Si TFTs can be made on plastic substrates without being restricted by the low temperature tolerance of plastic substrates.

2. Experiment

The process began with a Si wafer of some orientation. A thermal SiO_2 layer (∼230 nm) was grown on the Si wafer at 900 °C. Although thermal oxide was used here, plasma-enhanced chemical vapor deposition (PECVD) oxide deposited at elevated temperatures can also work in lieu of the thermal oxide. The oxide layer will serve as a sacrificial layer in the subsequent release process. The thickness of the oxide layer is chosen to be thin to allow in-place bonding (similar to our previous work for single-crystal Si [7, 17]) during the release of poly-Si (otherwise the release membrane will float up). Un-doped poly-Si was then deposited in a low pressure chemical vapor deposition (LPCVD) system at 600 °C for 14 min. The measured thickness of the poly-Si is ∼300 nm. The finished structure can be considered as a poly-Si-on-insulator (poly-SOI) and the grain size of the top poly-Si template is about 30 nm (figure 1(*a*)). To further improve the poly-Si quality, three pieces of identical poly-SOI samples were annealed at 850 °C for 1, 2 and 5 h, respectively. With the increase of annealing time, the grain size of the poly-Si was increased as indicated from the scanning electron micrographs (SEM) taken from the poly-Si surfaces (figures 1(*b*)–(*d*)). The annealing time for the poly-Si sample was further increased, but no further obvious improvement of the grain size was observed. An average grain size of ∼100 nm was obtained from the 5 h (figure 1(*d*)) annealing condition, the largest grain size obtained under furnace annealing conditions [18, 19]. This annealing condition also offers higher material mobility (based on simple measurements of the surface resistivity) than the other two conditions (∼40 and ∼50 nm grain sizes obtained for 1 h and 2 h annealing conditions, respectively). Since the as-deposited material is already poly-Si, crystal re-growth was difficult unless the annealing temperatures were very high. Overall, the grain size increase due to elongated annealing is not significant. We speculate that higher crystal quality would be obtained if a-Si was used as the starting material for the high-temperature recrystallization. The following processes for the poly-Si were based on the sample that was annealed for 5 h.

The top poly-Si layer of the poly-SOI was patterned with photolithography. Source and drain regions were defined by

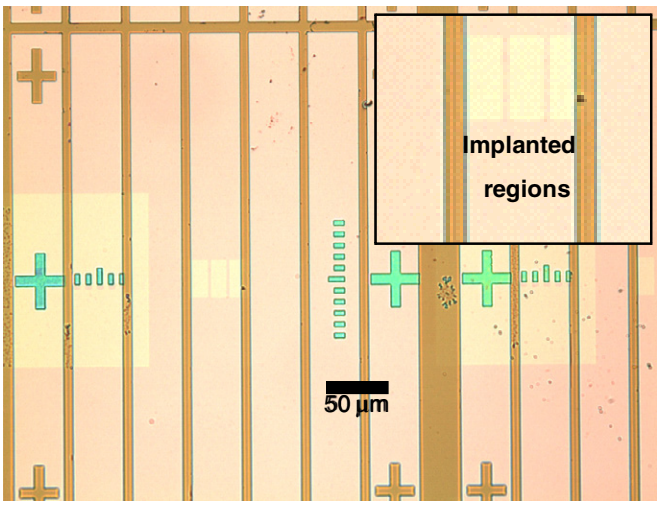

Figure 2. An optical-microscope image of patterned poly-Si stripes with ion implanted regions (also shown in the inset) before release.

selective phosphorus ion implantation with a dosage of 5×10^{14} cm^{-3} and 70 keV energy, followed by an annealing of 850 °C for 45 min (see figure 2 inset). This processing step is similar to what was used in the transferrable single-crystal Si membranes [17]. With this pre-release selective ion implantation, low-resistivity source/drain contacts were obtained by avoiding the use of high-temperature steps on plastic substrates. The poly-Si was then patterned into 450 μm long, 45 μm wide strips with 5 μm gaps in between (figure 2). The regions between the strips were then etched down to the oxide layer using reactive ion etching (RIE) and SF_6 gas. After stripping off the photoresist, the sample was immersed in aqueous concentrated HF (49% HF) for 25 min to fully etch away the sacrificial oxide layer in order to release the poly-Si membrane. During the sacrificial oxide removal process, the poly-Si layer fell down gradually and got attached to the handling Si substrate, as shown in figure 3. After the released poly-Si was removed, the handling Si substrate could be reused (recycled).

In figure 3 (right panel), it is observed that, quite different from the release of single-crystal Si [7, 17], which shows perfect flatness after release, significant rippling was shown on the released poly-Si strips. The ripples in the released poly-Si strips indicate that a significant amount of compressive residual stress was built in the poly-Si before it was released. As the oxide undercutting progressed, the strip edges attached to the substrate, inhibiting the further expansion of the strips, and the strips became buckled. The residual stress in (thin films and) poly-Si is very common [20, 21]. Large residual stress is one of the undesirable properties of poly-Si for flexible electronics applications [20, 21]. The non-flat topology of the released poly-Si membrane makes printing transfer impossible using the same transfer method as was used for the single-crystal Si [17], since only a very small area can be well attached to the destination substrate (e.g. plastic).

To flatten the poly-Si membrane after its release in order to be transferred, a modified patterning scheme was used. Instead of using long and narrow strips, a square-shape patterning with dimensions of 45 μm × 45 μm was used. The etching time in the aqueous concentrated HF was 20–25 min for the full release of the poly-Si membrane. Figure 3 (left panel) shows the released square-shape poly-Si in comparison with the long stripes on the same sample (side-by-side). It clearly indicates the effectiveness of relaxing the residual stress using the square-shape patterning (which is similar to road paving using cement: the cement needs to be cut into squares to allow expansion/contraction due to various weather conditions). It is also observed from figure 3 (left panel) that the width of the released square-shape poly-Si is slightly larger than the width of the long strips, indicating the full stress relaxation of the squares. The compressive strain released during the process is about 0.6% (estimated from figure 3).

The fully relaxed, flat poly-Si membrane can now be print transferred to any desired substrate for device fabrication using a similar method to that applied for the single-crystal Si membrane [5–7, 17]. Here the poly-Si membrane was transferred to a polyethylene terephthalate (PET) substrate using the dry flip transfer technique [7, 17]. The active regions were etched with RIE. Then the gate stack was evaporated at room temperature with an ∼300 nm SiO layer and ∼150 nm Ti/Au metal contacts. Source/drain contact metal (Ti/Au) was deposited by an e-beam metal evaporator. Figure 4 shows the process flow for transferring the poly-Si membrane and fabricating TFTs on plastic substrates.

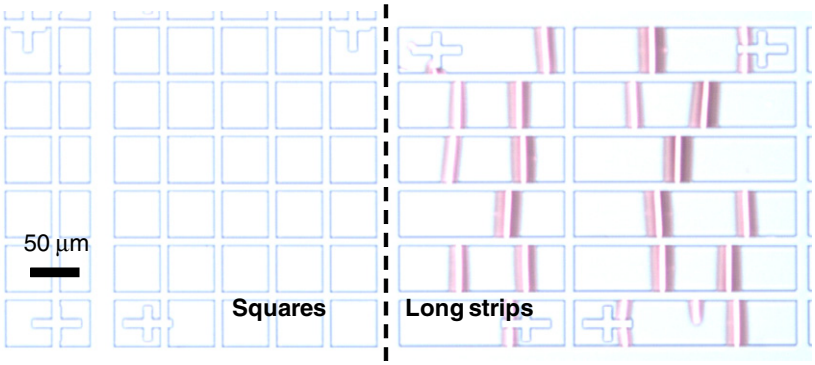

Figure 3. An optical-microscope image of poly-Si squares (left panel) and strips (right panel) on the same sample under removal of the sacrificial oxide layer. The dashed line was added to the single image. Significant buckling was formed for the long strips upon release. As a comparison, released poly-Si squares show flat topology.

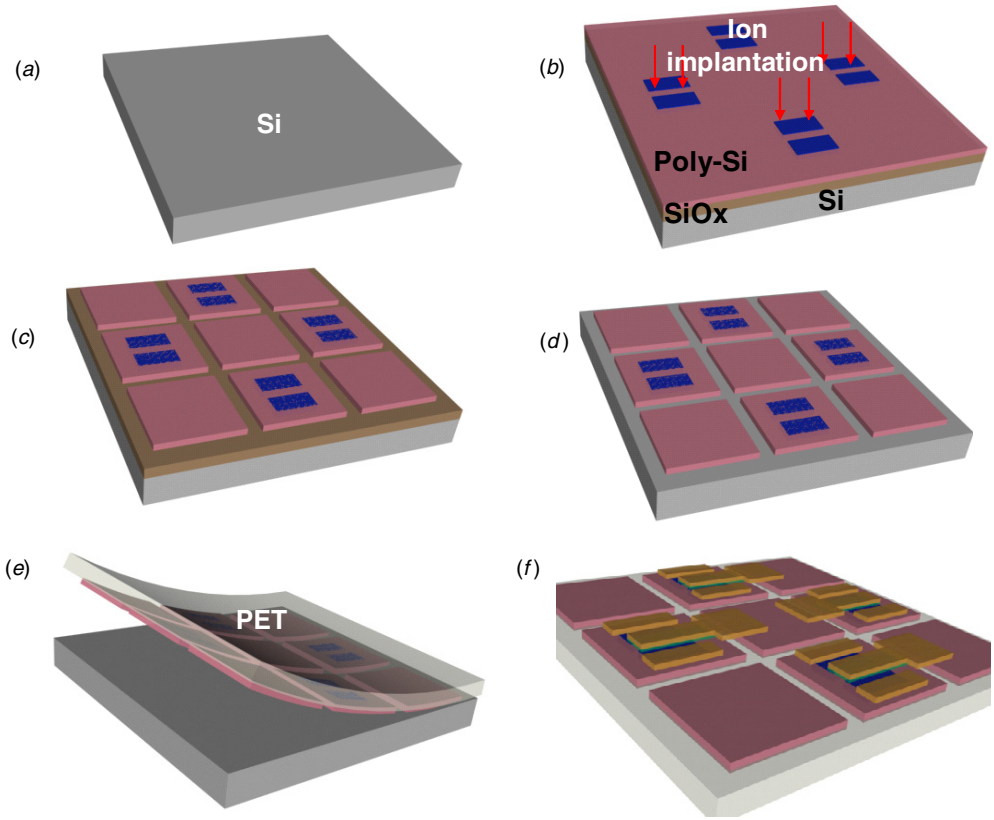

Figure 4. Process flow for the fabrication of poly-Si TFT on a plastic substrate (not drawn to scale). (*a*) Starting with the Si substrate, (*b*) grow thermal oxide and deposit poly-Si followed by annealing. Select ion implantation followed by another annealing used to define low-resistivity source/drain regions. (*c*) Pattern the poly-Si into square shapes. (*d*) Undercut oxide and release poly-Si membrane. (*e*) Apply SU-8 to PET and use the PET to pick up the poly-Si membrane. (*f*) Deposit gate stack and source/drain metal to finish the device fabrication.

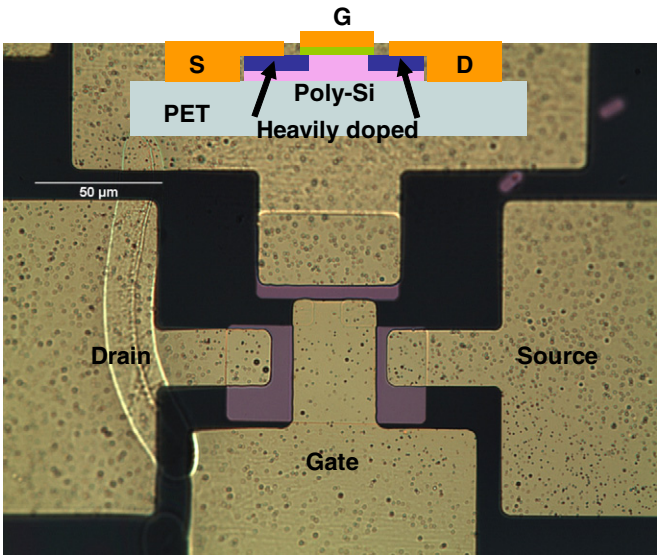

Figure 5. A microscopic image of a poly-Si TFT on a plastic substrate. The inset shows the cross section of the TFTs.

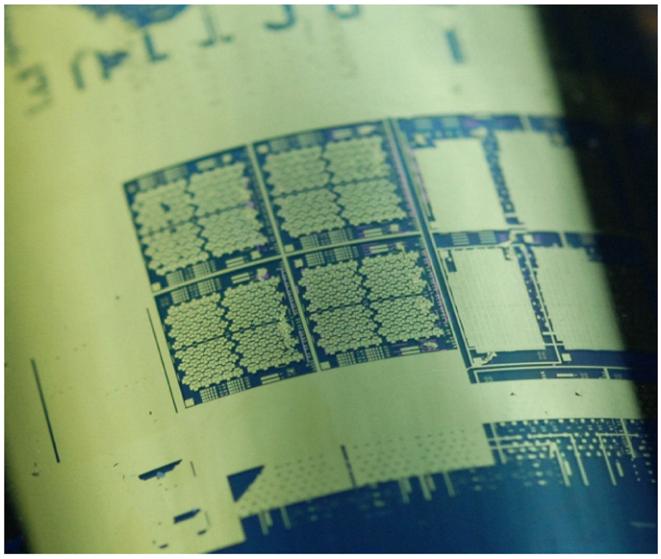

Figure 6. A bent flexible TFT array on PET.

3. Results

Figure 5 shows a microscopic image of a finished poly-Si TFT on a PET substrate. Figure 6 shows a bent array of flexible poly-Si TFTs. These TFTs have a gate length of ~38 μm and a gate width W_G of ~35 μm. The poly-Si TFTs on the plastic substrate were characterized, and figure 7 plots the representative output current–voltage (*I*–*V*) curves of the device. The linear region indicates the

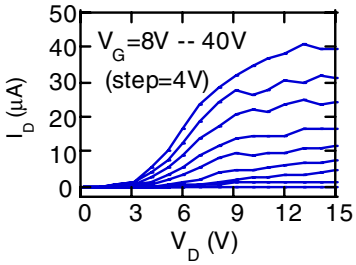

Figure 7. Representative output curves measured from the poly-Si TFT on plastic.

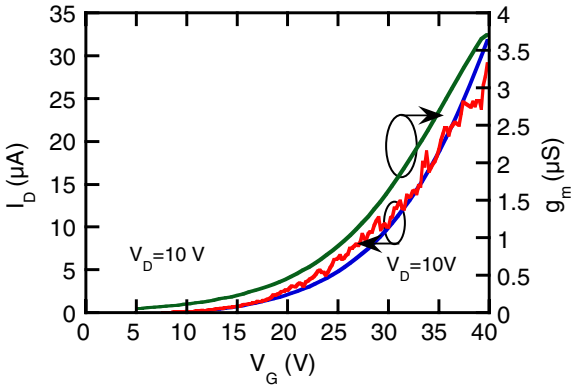

Figure 8. Measured transfer characteristics. The gate voltage V_G varies from −8 to 40 V in 4 V intervals. Transconductance g_m (calculated from the fitted smooth I_D curve) as a function of the gate bias for the poly-Si TFT on plastic. V_D is 10 V.

large parasitic resistance associated with the source and drain contacts, indicating the need for further ion implantation and annealing optimization in the future. Figure 8 shows the transfer characteristics of the TFT with a source–drain bias (V_D) of 10 V. The high voltages sustained by the devices are typical characteristics of poly-Si TFTs [8, 9, 11, 16]. The small drain current level obtained at high bias voltage makes direct extraction of the transconductance g_m difficult. In order to extract g_m, a smooth curve fitting (figure 8) was used for the measured drain current. The field-effect mobility (μ_{FE}) was extracted using the equation $\mu_{\mathrm{FE}} = L_G g_m/(W_G C_G V_D)$, where L_G and W_G are the physical dimensions of the gate length and width, respectively, $V_D = 10$ V, and the highest measured $g_m = 3.7$ μS. (Note that higher gate bias may be used to obtain even higher g_m, but it was limited by the bias limit of an Agilent 4155 semiconductor parameter analyzer.) The calculated field-effect mobility is ∼30 cm^2 V^{-1} s^{-1}, which is quite close to the limit of poly-Si mobility that can be obtained with furnace recrystallization [18, 19]. Furthermore, since the peak g_m was not reached due to bias limit, this mobility value may not be considered as the ultimate mobility of the poly-Si obtained in this process. Nevertheless, the mobility is much higher than that of a-Si that was deposited on plastic substrates. Even though the mobility is lower than excimer-laser-recrystallized poly-Si, the residual-stress-released flat poly-Si membrane can be transferred to any substrate, including paper and PET, which might not be accessible by other techniques.

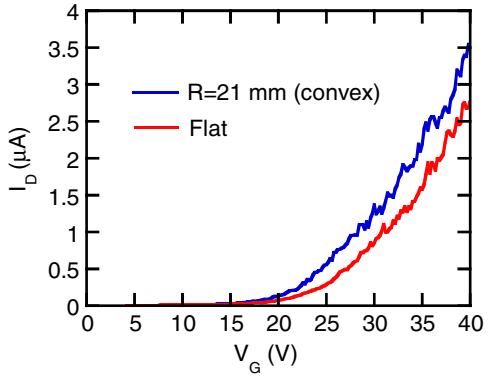

Figure 9. Measured drain current change under convex bending (tensile strain applied to the TFT channel).

The mechanical bending characteristics of the poly-Si TFTs were also characterized. The TFTs were bent along the device channel direction (tensile strain applied to the channel) using a fixed convex bender with a radius of 21 mm. As shown in figure 9, a significant increase in the drain current and the corresponding g_m (by 27%) was observed with a large tensile strain applied (21 mm bending radius: 0.31% tensile strain). The trend is consistent with those poly-Si TFTs that were made on stainless steel foil substrates [22].

4. Conclusions

We realized a simple and inexpensive approach to high-quality polycrystalline Si that is stress-free and, most importantly, transferrable to any substrate for flexible TFT fabrication. By performing high-temperature deposition, annealing and selective ion implantation processes on Si-wafers for LPCVD deposited poly-Si and employing stress-relaxed membrane patterning, release and printing transfer processes for the pre-doped poly-Si, high-performance poly-Si TFTs were made on plastic substrates. Further optimizations of the processes will lead to TFTs on any foreign substrates with comparable performance to those fabricated on high-temperature substrates (such as stainless steel). Other types of devices such as solar cells may also be made with this poly-Si approach.

Acknowledgments

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