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Citation: Appl. Phys. Lett. **106**, 262101 (2015); View online: https://doi.org/10.1063/1.4921077

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Microwave flexible transistors on cellulose nanofibrillated fiber substrates

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(Received 23 December 2014; accepted 24 February 2015; published online 30 June 2015)

In this paper, we demonstrate microwave flexible thin-film transistors (TFTs) on biodegradable substrates towards potential green portable devices. The combination of cellulose nanofibrillated fiber (CNF) substrate, which is a biobased and biodegradable platform, with transferrable single crystalline Si nanomembrane (Si NM), enables the realization of truly biodegradable, flexible, and high performance devices. Double-gate flexible Si NM TFTs built on a CNF substrate have shown an electron mobility of $160 \, \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$ and f_T and f_max of $4.9 \, \mathrm{GHz}$ and $10.6 \, \mathrm{GHz}$, respectively. This demonstration proves the microwave frequency capability and, considering today's wide spread use of wireless devices, thus indicates the much wider utility of CNF substrates than that has been demonstrated before. The demonstration may also pave the way toward portable green devices that would generate less persistent waste and save more valuable resources. © 2015 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4921077]

Personal electronic gadget users tend to upgrade their gadgets much more frequently nowadays as new technologies offering more functionality and more convenience become available. For example, cell phone users tend to buy new cellphones every 2 to 3 years. Thus, large quantities of working electronics are discarded constantly as new ones are available. In the U.S. alone, a report published by the U.S. Environmental Protection Agency in 2012 showed that 152 million of mobile devices were disposed in each year. Many more gadgets may be discarded daily, considering the larger quantities and more varieties being produced in the recent years. This will not only lead to a large amount of consumption of our limited natural resources but also generate a large amount of waste that could pollute our environment. The majority of the electronic components in portable gadgets are built on a Si wafer which is a highly purified, expensive, and rigid substrate. In fact, only a tiny proportion of the Si material is used in the electronics. A commercial standard 12 inch. Si wafer is 775 μ m thick, but only much less than 1 μ m on the top of the wafers used for electronic devices. The rest of the Si substrate is just used as a support for the devices and is eventually wasted when devices are discarded. Thus, it would be desirable to develop a technique for creating electronics using an alternative substrate that is inexpensive and biodegradable or even compostable while maintaining highperformance standards. This will not only drastically reduce the usage of Si but also reduce the accumulation of persistent waste. Since most personal gadgets operate at microwave frequencies (>1 GHz), demonstration of such electronics on the above alternate substrates are of important practical value. Previously, microwave thin-film transistors (TFTs) have been demonstrated on polyethylene terephthalate (PET) substrates. However, petroleum based PET substrates are not biodegradable. In addition, fabrication of TFTs on chemically stable PET substrates does not encounter solvent compatibility issues during wet processing.

In this paper, we demonstrate microwave flexible TFTs built on a cellulose nanofibrillated fiber (CNF) substrate by employing transferrable single crystalline Si nanomembranes (Si NMs). Recent studies have demonstrated that CNF substrates derived from wood^{2,3} have good mechanical properties, low thermal expansion, good flexibility, and good biodegradability⁴⁻⁷ and thus have the potential to serve as substrates for portable green electronics. Researchers have previously demonstrated the use of cellulose nanofibril composites as substrates for a variety of energy and electronic devices such as solar cells, 8-10 energy storage devices, 11 sensors, ¹² organic TFTs, ¹³ lighting devices, ¹⁴ and displays. ¹⁵ These demonstrations have mainly taken the advantages of transparency and decomposition/dissolution properties of CNF. As of today, the radio-frequency (RF) properties of CNF have been unknown or not explored. In order to realize microwave electronics on a CNF substrate, active materials with both high charge carrier mobility and flexibility are required. In the meantime, CNF needs to possess relatively low energy consumption loss at RF. High frequency operation of active devices on CNF can provide such insights of the RF suitability of CNF. Single crystalline Si NMs of a few hundred nanometers thick offer comparable electronic properties as their bulk counterparts yet with superior mechanical flexibility and durability. 18,19 Here, we explore the Si NM based microwave TFTs feasibility on CNF. However, CNF substrate itself is not stable under long exposure in certain processing chemicals such as acetone. As a result, the previously demonstrated Si NM TFT fabrication method,

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i.e., finishing high-temperature processing steps on rigid substrate and finishing the rest steps on PET substrate via additional photolithography, is not applicable to CNF substrates. An alternative TFT fabrication method is thus needed for the CNF substrates.

The complete device fabrication process flow is schematically shown in Figure 1(a). The fabrication starts with a SOI wafer (SOITEC) which has a 270 nm lightly p-type doped top Si layer and a 200 nm buried oxide layer. For the double gate configuration design used here, one drain (D) and two source (S) regions are needed, for a total of three n+ wells ($\sim 5 \times 10^{19} \, \text{cm}^{-3}$). These n+ wells are formed by using a spin-on-dopant (SOD, Honeywell P509) diffusion process carried out in a nitrogen/oxygen ambient furnace (N2 95% and O₂ 5% at 850 °C for 20 min) (Fig. 1(a-i)). After forming releasing holes, the top Si layer is released from the buried oxide layer by selective wet-etching in concentrated HF (49%). The released top Si NM gently falls down on the handling Si substrate (Fig. 1(a-ii)). After rinsing the sample, the Si NM is dried by N₂. Then, the Si NM is weakly bonded to the handling Si substrate. Gate electrodes of $0.8 \mu m$ in length and SiO₂ dielectric stacks (SiO₂/Ti/Au, 100 nm/10 nm/ 100 nm) are patterned using e-beam lithography and deposited with e-beam evaporation, followed by the deposition of the source/drain electrodes (Ti/Au, 10 nm/150 nm, Fig. 1(aiii)). After the completion of the metallization step, the entire device layers (electrodes and Si NM) are transfer to an adhesive layer (SU-8, Microchem) coated CNF substrate and cured to glue the devices onto the CNF substrate (Figs. 1(aiv) and 1(a-v)). After finishing the transfer step, the Si NM layer faces up and the electrodes become buried underneath the Si NM. The active layer is finally defined by the photoresist patterning and dry etching steps (Fig. 1(a-vi)). Shown in Fig. 1(b) is a micrograph of the fabricated double-gate TFT on a flat flexible CNF substrate. Figure 1(c) shows another micrograph with arrays of Si NM TFTs on a bent flexible CNF substrate, which is also optically transparent. Figures 1(d) and 1(e) present images of the degradation of the CNF substrate after exposure to *Postia placenta* (also known as brown-rot fungi)²⁰ for 3 weeks. Detailed descriptions on the transfer printing process²¹ and fabrication of the CNF substrate can be found elsewhere.²² Device I-V characteristics were measured using a semiconductor parameter analyzer (HP4155B) in the dark to avoid any light-induced photocurrents. RF characteristics were measured and extracted from scattering (S-) parameters using an Agilent E8364A performance network analyzer. A bias-tee was used to apply an external DC bias during RF measurement.

Figure 2(a) shows a cross-sectional view for the double gate Si NM TFT on a CNF substrate. A cross-sectional scanning electron-microscope image and a zoomed-in microscope image of the finished device on the CNF substrate are shown schematically in Figs. 2(b) and 2(c). The physical gate length, gate width $(W_{\rm g})$, and the effective gate (channel) length ($L_{\rm g}$) are 0.8 $\mu{\rm m}$, 20 $\mu{\rm m}$, and 0.5 $\mu{\rm m}$, respectively. The output characteristics of the TFTs under various gate biases from 0 V to 5 V measured on a flat surface and on a curvature (0.3% of strain, measured on the 38.5 mm mold radius) are shown in Figure 2(d). There is an approximately 8% of increment in drain current by bending, which is caused by lattice constant change in single crystal Si NM and agrees well with previous findings. 17,25 Excellent drain current saturation features indicate well-controlled drain current with e-beam lithographically defined submicron gate electrodes. Figure 2(e) shows the transfer characteristics under flat and bending conditions. The highest $g_{\rm m}$ was 11.5 μ S under a drain bias $(V_{\rm ds})$ of 100 mV. An on/off ratio of 10^6 and a well suppressed gate leakage current indicate effective SOD doping and the formation of high quality dielectric layers. The gate leakage current remained very low within all gate bias ranges. A 160 cm²/V·s of the field-effect mobility was measured based on the following equation: $\mu = (L_g \cdot g_m)/(W_g \cdot C_{ox} \cdot V_{ds})$, where C_{ox} is the oxide capacitance. This extracted fieldeffect mobility value is consistent with other Si NM-based TFTs. 16,17 Higher mobility should be possible by using a strained Si NM. 17 A threshold voltage (V_{th}) of 0.85 V and a

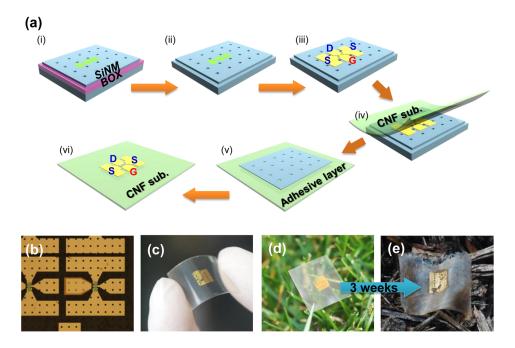


FIG. 1. (a) Illustration of the fabrication process flow for flexible Si NM TFTs built on CNF substrates. (b) Microscopic image of a finished device on the CNF substrate. (c) An optical image showing the transparency and flexibility of the CNF substrate. (d) An optical image and (e) an enlarged optical image showing the biodegradability of the array of devices built on the CNF substrate: (left) as-made and (right) after 3 weeks degradation.

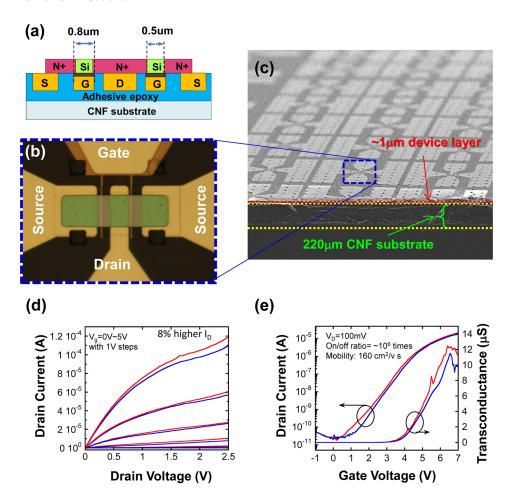


FIG. 2. (a) A schematic of the device cross-section with source/drain electrodes sandwiched in between the top Si NM active layer and the bottom CNF substrate due to the flip transfer printing process. (b) A microscope image of the active area of a finished flexible Si NM TFT on the CNF substrate. (c) A scanning microscope image of the cross-sectional view: showing only the top $1 \mu m$ is used for the device layer, while the other $220 \,\mu\mathrm{m}$ of CNF substrate comprise the supporting layer. (d) Drain current-voltage characteristics with different $V_{\rm g}$ values ranging from 0 V to 5 V with a 1 V step under flat (blue) and bending (red) conditions. (e) Drain current (I_D) and transconductance (g_m) curves with a drain bias of $100\,\mathrm{mV}$ and a V_{g} ranging from -1 V to 7 V, under flat (blue) and bending (red) conditions.

subthreshold swing of 550 mV/decade were also extracted from the transfer curve. High threshold voltage and subthreshold swing can be further improved by employing ion implantation to form well-defined n+ wells.

Figure 3(a) shows the measured current gain (h_{21}) and the Masons unilateral gain (U-gain) of Si NM TFTs on a CNF substrate under flat and bending conditions (0.3% of strain,

measured on the 38.5 mm mold radius) with a DC bias of $V_{\rm gs} = 5$ V and $V_{\rm ds} = 4$ V. Shown in Figs. 3(b) and 3(c) are the measured S-parameters from 45 MHz to 20 GHz on a linear scale and on a Smith chart. The measured $f_{\rm T}$ and $f_{\rm max}$, after de-embedding, were 4.9 and 10.6 GHz under flat conditions and 3.8 and 9.2 GHz under bending conditions, respectively. The slightly lower $f_{\rm T}$ and $f_{\rm max}$ values are attributed to the fact

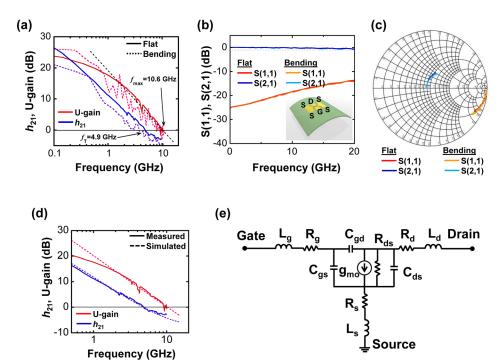


FIG. 3. (a) Current gain (h_{21}) and unilateral power gain (U-gain) as a function of frequency under flat (blue) and bending (red) conditions. (b) Measured S-parameters under the bias ($V_{\rm g} = 5 \, {\rm V}$, $V_{\rm ds} = 4$ V) under flat (blue) and bending (red) conditions. Inset shows the illustration of concave bending along the gate width direction. (c) Measured S(1,1) and S(2,1) on the Smith chart under bias $(V_g = 5 \text{ V}, V_{ds} = 4 \text{ V})$ under flat (blue) and bending (red) conditions. (d) Measured (solid) and simulated (dotted) frequency response characteristics of TFT under $V_{gs} = 5 \text{ V}$ and $V_{\rm ds} = 4 \, \rm V$. (e) The small-signal equivalent circuit model used for TFT parameter extraction.

TABLE I. Comparison of extracted device model parameters, FOM values between TFT on CNF substrate, and reference TFTs on PET substrate from Ref. 24. Reproduced with permission from J. Appl. Phys. **102**, 034501 (2007). Copyright 2015 AIP Publishing LLC.

	TFT of CNF	Ref-TFT ²⁴
L _{Gate} (μm)	0.8	2.5
$L_{eff}(\mu m)$	1	1.5
$g_{mo}(mS)$	0.95	1.18
τ (ps)	4	4.8
$R_g(\Omega)$	96	0.1
$R_{d}\left(\Omega\right)$	30	35
$R_{s}\left(\Omega\right)$	13.5	40
$L_{g}\left(nH\right)$	0.05	0.06
$L_{d}\left(nH\right)$	0.29	0.35
L_{s} (nH)	0.31	0
C_{gd} (fF)	9	40
C_{gs} (fF)	22	50
C_{ds} (fF)	2	3
$R_{ds}\left(\Omega \right)$	270	4500
$f_{\rm T}\left({\rm GHz}\right)$	4.9	2
f_{max} (GHz)	10.6	7.8

the concave bending is along the gate width direction. Under this condition, the Si channel experienced a compressive strain, thus lower electron mobility along the electron moving direction (from source to drain).²⁹ Comparing the f_T and f_{max} values with the other Si NM-based RF TFTs built on PET substrates, Si NM TFTs on CNF substrates show similarly high RF performances.²⁴ Considering other desirable mechanical, thermal, as well as dielectric properties possessed by CNF, the demonstration of its microwave capabilities further indicates its potential as alternative substrate contender for future broader bio-compatible and flexible electronic applications.^{6,7} We further analyzed the CNF-based TFT characteristics by employing a small-signal equivalent circuit model to extract the transistor parameter.²³ As shown in Fig. 3(b), Advanced Design System (ADS 2013) was used to generate a small-signal equivalent circuit model. The parameter extraction was then carefully performed from the measured Sparameters at the bias conditions, where the highest frequency responses were measured. Shown in Table I are the extracted figure-of-merit (FOM) values for TFTs on the CNF substrates reported here as well as the values for earlier reported TFTs on a PET substrate. Smaller $C_{\rm gs}$ and $C_{\rm gd}$ values were obtained for the TFTs on the CNF substrate reported here, mostly due to the small overlap between the gate and the source/drain, which was achieved by the precise alignment during e-beam lithography and can be attributed to the measured high RF characteristics.

In conclusion, we have demonstrated high performance Si NM flexible TFTs built on a CNF substrate that exhibit superior microwave-frequency operation capabilities. The demonstrations suggest that bio-based and bio-degradable CNF films can be readily used as alternative high performance flexible electronics substrates and, moreover, the semiconductor chips in future's portable devices/gadgets can be made biodegradable.

This work was supported by a PECASE award under Grant No. FA9550-09-1-0482. The program manager at AFOSR is Dr. Gernot Pomrenke.

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