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TOPICAL REVIEW

Fast flexible electronics using transferrable silicon nanomembranes

Kan Zhang[1,3], **Jung-Hun Seo**[1], **Weidong Zhou**[2] **and Zhenqiang Ma**[1,4]

[1] Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 1415 Engineering Drive, Madison, WI 53706, USA
[2] Department of Electrical Engineering, NanoFAB Center, University of Texas at Arlington, TX 76019, USA

E-mail: mazq@engr.wisc.edu

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Abstract

A systematic review, covering the aspects of material preparation, device fabrication and process integration, is provided for flexible electronics operating in high-frequency domain based on transferrable monocrystalline silicon (Si) nanomembranes (NM). Previously demonstrated methods of releasing Si NM from silicon-on-insulator source substrates and transferring it to flexible substrates are briefly described. Due to the processing temperature limitation of most flexible substrates, a pre-release NM selective doping scheme is used for Si NMs. With proper selections of ion implantation energy and dose, fully doped Si NMs across their entire thickness with very low sheet resistivity can be obtained, allowing flip transfer of the NMs for backside and even double side processing. A general conclusion of preferred low implantation energy for shallower depth ion implantation is identified. The evolvement of radio frequency (RF) flexible Si thin-film transistor (TFT) structures is described in detail. The continuous performance enhancement of TFTs owing to process and TFT structure innovations is analysed. Demonstrations of flexible Si RF switches and RF inductors and capacitors are also briefly reviewed as valuable components of the general flexible device family, some of which also benefit from the pre-release NM doping technique. With the proved feasibility of these basic RF elements and related processing techniques, more complicated flexible RF circuits can be expected. Future research directions are also discussed, including further enhancement of device performance, building more types of semiconductor devices on flexible substrates, and process integration for flexible circuits and systems.

(Some figures may appear in colour only in the online journal)

1. Introduction

Over the past decade, an enthusiastic pursuit for flexible electronics, employing both organic and inorganic semiconductor materials, with continuously improved performance has been observed. Intense research activities have been carried out in exploring the mechanical flexibility of electronics, while continuously revamping their performance metrics and expanding their applications [1–3]. Flexible electronics offer unique advantages of being lightweight, bendable/stretchable and conformal to uneven surfaces over their rigid counterparts. These merits have not only enabled some successful commercial products, such as flexible solar cell panels, organic light-emitting diode (OLED) displays and radio-frequency identification (RFID), but have also inspired tremendous efforts of research and development that are both academically and commercially valuable and attractive. Some of the examples include large-area flexible displays, wearable personal communication and computation devices, biomedical

[3] Now with Corning, Incorporated.
[4] Author to whom any correspondence should be addressed.

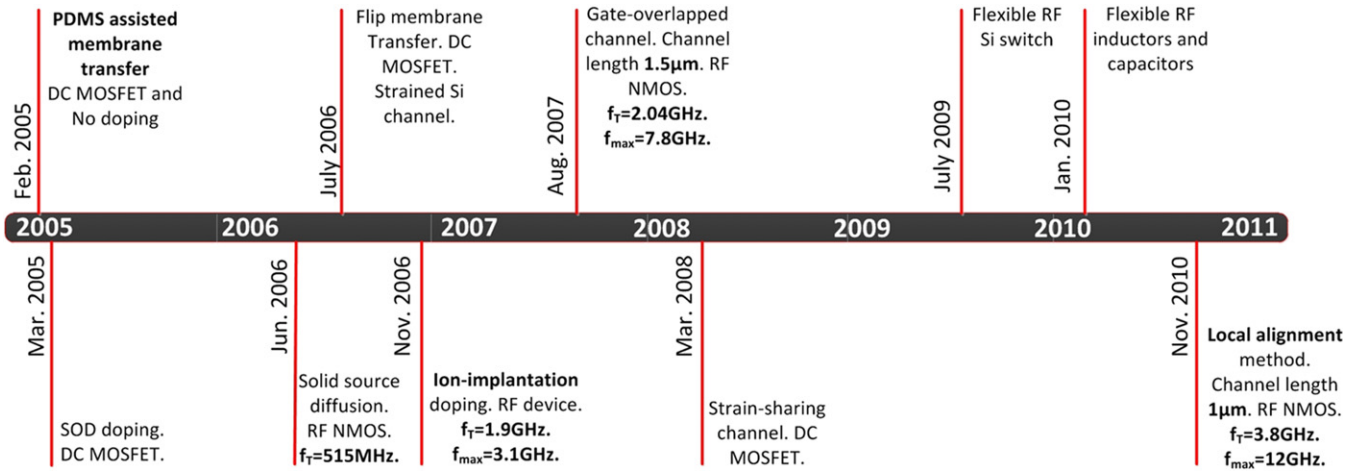

Figure 1. A short development history of flexible RF active devices (and related passive devices) on plastic substrates using transferrable Si NMs.

telemetry devices, foldable phased-array antennas, large-area radars for remote sensing, surveillance, etc [4–6]. Amorphous Si, polycrystalline Si and organic materials are traditional materials for flexible electronics due to their large area and availability at low cost [4, 7], and have demonstrated their dominance in low-speed applications such as flexible displays, electronic tags and low-cost integrated circuits [8–11]. However, for applications operating in higher frequency domain, the low carrier mobilities due to the poor crystalline quality of these materials indicate their incompetency.

High-speed flexible electronics, also known as fast flexible electronics, which uniquely enable wireless applications, impose specific requirements on both active materials and fabrication techniques to achieve comparable performance with their rigid counterparts. Suitable active materials should possess high carrier mobilities for high-speed operation, be readily integrable on flexible substrates, and be bendable without much sacrifice of performance. Within such criteria, monocrystalline semiconductor materials are the prevailing options, such as Si [12–15] and III–V materials [16–18]. Furthermore, monocrystalline Si nanomembrane (NM) released from silicon-on-insulator (SOI) emerges as one of the best choices due to its high carrier mobilities, commercial availability at relatively lower cost and mature fabrication techniques [19]. Specific considerations must also be taken in developing fabrication techniques so that they are compatible with flexible substrates, which usually have considerably worse physical and chemical stability than rigid semiconductor materials. Some processes, such as those involving high temperature or corrosive solutions, must be excluded on flexible substrates, leading to the requirement of sophisticated design of process flow [20]. In this paper, we review the development of the fabrication process for flexible RF active and passive devices on low-temperature plastic substrates, including flexible RF metal–oxide–semiconductor field-effect transistor (MOSFET) type thin-film transistors (TFT) and RF switches based on monocrystalline Si NM, and flexible inductors and capacitors. Future research directions on flexible electronics will also be discussed based on the review.

The relatively short development history of high-frequency flexible RF active devices (and the related passive devices) based on the monocrystalline Si NM transfer methods on plastic substrates is summarized in figure 1. Along the development timeline, some of the technical variations for the fabrication process flow, which made influential contribution to the improvement of the RF figure of merits (FOMs), are emphasized with bold font. These technical improvements will be analysed in detail as to what technical problems have been solved and how the FOMs were consequently enhanced. In this way, we hope to provide a clear understanding of how the technology for flexible Si RF devices has evolved, and further, to point out some potential future directions where the technology is heading.

2. Generic methods for Si NM transfer

Membranes that are formed with selective etching and are fixed on rigid substrates using SOI have existed for decades (also called diaphragms) [21]. Selective etching techniques of different materials also existed for decades, originating from the transferrable III–V devices [22, 23]. However, the key technique enabling today's intensive NM-related research and development activities is the transfer printing technique [24], i.e. completely releasing NMs and making them transferrable to a different substrate at will. The transfer printing technique is substantially different from the wafer bonding technique or the solution-based floating transfer technique. Transfer printing provides deterministic registration on destination hosts with much more flexibility than wafer bonding based material transfer methods. The first demonstration of Si NM transfer onto a flexible plastic substrate was performed with an elastomeric polydimethylsiloxane (PDMS) stamp, in which an effective method was also used to fully release Si NMs from SOI substrates [24]. This release and transfer method was so illuminating that most following research works adopted the essence of this method with certain improvements for better transfer yield and process simplicity considerations based on specific SOI material structures. Nevertheless, the generic process has been kept the same, as shown in

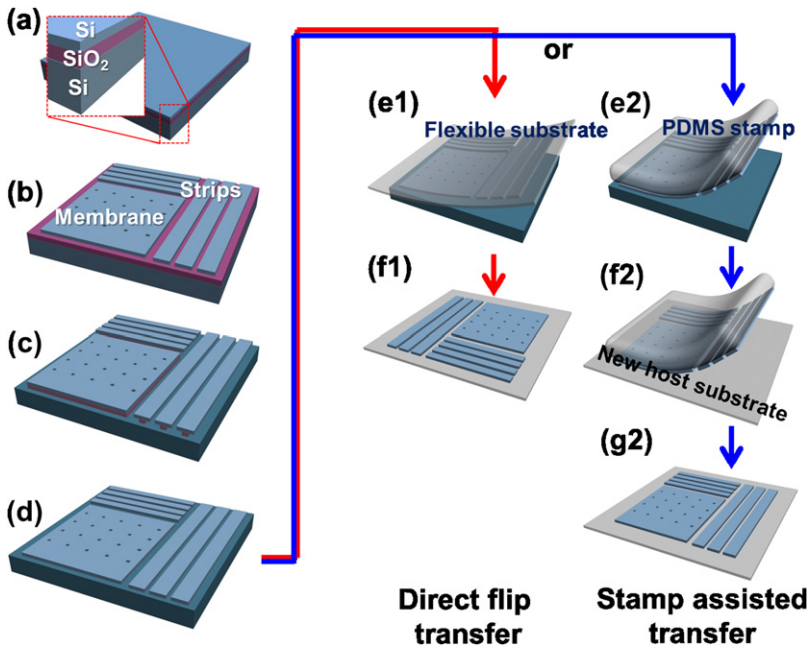

Figure 2. Generic process for Si NM release from SOI and transfer. (*a*) Use SOI as starting material; (*b*) pattern top Si template layer into strips or meshed NM and partially expose BOX; (*c*) immerse SOI into aqueous HF to undercut BOX; (*d*) Si template layer falls down as BOX is fully undercut and gets registered on the handling substrate. Two transfer routes exist: direct flip transfer (*e*1)–(*f* 1) and stamp-assisted transfer (*e*2)–(*g*2). (*e*1) Flexible substrate with adhesive coating is attached to Si NM. (*f* 1) Peel off the plastic substrate with NM transferred. (*e*2) Si NM is first picked up by the elastomeric stamp. (*f* 2) Bring the stamp into contact with (adhesive-coated) a new host substrate. (*g*2) The stamp is slowly peeled off, leaving NM being attached/transferred to the new host.

figure 2. The detailed process starts from an SOI material (figure 2(*a*)). Buried oxide (BOX) is partially exposed by patterning the top Si template layer into strips or mesh NM using photolithography and reactive-ion etching (RIE) (figure 2(*b*)). Then the sample is immersed in aqueous hydrogen fluoride (HF) solution to fully undercut the BOX. The top Si template layer consequently falls down and gets registered onto the Si handling substrate by van der Waals force (figures 2(*c*) and (*d*)) [25] as a standalone Si NM that is ready for the following manipulation of transferring to a foreign host [26]. In the case of a thicker BOX layer of SOI, e.g. thicker than 1–2 μm while the exact thickness is unknown due to limited commercially available BOX specifications, the fully released Si NMs may float in the HF solutions. In this case, special anchors need to be designed to hold the released NMs in place [27].

There are some technical considerations for the Si NM releasing process. They are decided by the following process requirements. The choice of using strip or mesh NM form during the release process depends on how much active area is needed for the device and whether subsequent alignment is needed between individual devices. With the strip form, misalignment is possible between neighbouring strips due to their possible random movement during undercutting and particularly the following transfer procedure [13]. In this sense, a mesh NM is generally preferred since no relative movement exists and usually a larger portion of Si NM can be preserved as active material instead of being etched away to expose the BOX underneath. But on the other hand it has been experimentally observed that BOX is easier to fully undercut in the case of strip pattern because of the larger portion of exposed BOX to react with HF. So using the mesh NM pattern, with all the benefits of larger useable material, needs more effort on undercut recipe tuning.

The key factors affecting successful Si NM releasing include complete removal of BOX without disturbing the Si template layer on top and good registration of NM with handling substrates. These factors therefore require well-defined Si/SiO_2 interfaces between the top Si template and BOX, as well as between BOX and the Si handling substrate. With this concern, SOI made by SmartCut® technology (obtainable from Soitec) is highly recommended because its technology guarantees a clearly defined Si/SiO_2 interface [28, 29], and high-quality, flat and uniform thickness NMs can be easily obtained. In contrast, SOI materials made by Separation by IMplantation of OXygen (SIMOX) technology is not suitable [30] and experiments show that the Si top template layer of SIMOX SOI may severely deform, e.g. curling, during BOX undercutting and the BOX is difficult to be thoroughly etched away.

After finishing the releasing procedure of SOI material, Si NM sitting on the handling substrate is ready for transfer. There are basically two routes of transfer: direct flip transfer and stamp-assisted transfer [31–33], as shown in figure 2, and with both methods one can achieve high transfer quality and high yield. Adhesive coating on flexible substrates may be necessary for both routes to facilitate transfer, and SU-8 (from Microchem Corp.), which is a UV-curable epoxy, has been commonly used as the adhesive by spin-coating. For the direct flip transfer method, the coated flexible substrate is attached directly to the prepared Si NM (figure 2(*e*1)) and then peeled off with Si NM adhered on the flexible substrate (figure 2(*f* 1)).

For the stamp-assisted transfer, the Si NM is first picked up by the elastomeric stamp (figure 2(*e*2)) and then adhered and transferred onto the flexible substrate (figures 2(*f*2) and (*g*2)). So stamp-assisted transfer is a non-flipped transfer method. After NM transfer with either method, SU-8 should be cured by exposure to UV light, so that the NM will be permanently bonded to the flexible substrate. It is noted that the backside of the NM is exposed using the direct flip transfer method. For NMs made from SmartCut® or wafer bonding SOIs, both their surfaces exhibit high crystal quality and flatness, and can suitably serve as device channels [28]. While there is no need to question the backside surface quality of flip transferred NMs, there is indeed one concern about the doping profile design between flipped and non-flipped NMs. The doping issues will be discussed in the next section.

It is also noted that under certain circumstances, particularly for transferring NMs to some rigid substrates, adhesive glues are not needed for temporarily attaching the transferrable NMs with the new substrates using the stamp-assisted transfer method [31]. Under the glue-free attachment situation, an ultra-clean interface will be obtained between the transferred NMs and the new host substrates. The cleanliness of the interface could be useful for future material integration and is thus considered as one of the most critical advantages of the stamp-assisted transfer method. Since the stamp-assisted transfer method does not involve any wet solutions during the transfer procedure, it is also sometimes called dry transfer.

3. Doping profile design

In the first report of flexible TFTs using transferrable Si NMs, there was no doping involved in the devices. Nevertheless, the direct current (dc) measurements of the TFTs clearly validate the high quality of the NMs as active device materials, indicating the great potential to achieve better device performance [24]. Among all the characteristics of the devices, the early work showed that the charge carrier mobility of transferrable Si NMs is equivalent to that of bulk Si. Following the first dc TFT demonstration, a spin-on dopant (SOD) was used to dope the Si NM and better dc NMOS TFT performance was reported, which further confirmed the feasibility of realizing high-speed devices [34]. High-frequency TFT was first explored using solid source diffusion as the doping method, and a cut-off frequency (f_T) of 515 MHz was reported, which was encouraging as a first step of flexible electronics towards the RF realm [12]. Although solid source diffusion is acceptable as pilot verification, the doping method may not be suitable for high-speed (e.g. microwave frequency) device applications for the following reasons. First, the thermal diffusion process typically works for devices with large critical feature sizes due to severe dopant spreading caused by elongated thermal treatment. Second, it is difficult to drive in the dopants into larger depth in NMs. Third, dopant concentration decreased rapidly with the doping depth, producing large sheet resistance in the NMs. For these reasons, ion implantation is a better option for NM doping and was soon adopted for flexible RF TFTs and better results were generated [15]. It should be mentioned that flexible substrates generally have much worse thermal stability than most rigid semiconductor substrates and cannot withstand high-temperature annealing processes. As a result, the high-temperature doping process, regardless of the method used, is performed on the rigid semiconductor substrate, which can be referred to as pre-release doping [12, 15, 34].

Since the ion-implantation procedure needs to be performed on SOI substrates, different requirements on doping profiles need to be applied for flipped and unflipped transferred NMs in order to achieve adequately heavy doping concentration near the final device surface for low contact resistance and low sheet resistance in source/drain (S/D) regions of MOSFET-type TFTs. Low parasitic resistance is the key towards high-speed TFTs. To be more specific, for the flip transfer method, a high doping concentration needs to be realized near the bottom side of the Si top template layer on the SOI substrate, while for unflipped transfer the top side of the Si template layer should have a high doping concentration. Regardless of unflipped or flipped NM doping, uniformly high doping concentration in Si template layer is generally favourable for both types of NMs in order to minimize S/D parasitic resistance and to realize better RF performance [35, 36].

A detailed study was conducted to guide the design of ion-implantation conditions. Since NMOS is the preferred type of TFTs for RF applications, phosphorous (P) ion implantation into SOI (lightly doped p-type with 270 nm Si template layer with 200 nm BOX is used as an example here) was investigated under similarly high dose but different energy to set the dopant concentration peak near either the top side or the bottom side of Si NMs. Secondary ion mass spectrometry (SIMS) was used to analyse the doping profiles under two implantation conditions: one has energy/dose of 12 keV/1×10^{16} cm^{-3}, and the other has 150 keV/4×10^{15} cm^{-3}, as shown in figure 3. Although different peak doping concentrations occur at different depths of the NMs, which are related to implantation energy (figures 3(*a*) and (*c*)), uniformly high doping concentration across the entire NM depth can be achieved as expected after finishing a furnace annealing at 950 °C for 45 min (figures 3(*b*) and (*d*)). However, further electrical characterizations using the transmission line model (TLM) reveal the difference between the two implantation conditions. Sheet resistance is lower in the case of low-energy implantation (18.63 Ω/□) than in the case of high-energy implantation (30.11 Ω/□). The difference is believed to be due to the damage caused by ion implantation that causes the crystalline quality to deteriorate. Lower energy implantation, which served as the recrystallization seed layer during annealing, leaves a thin layer of Si undamaged. On the other hand, the undamaged seed layer does not exist when high-energy implantation is used. Most likely, Si NMs with a large number of defects may be formed after thermal annealing in the high-energy implantation case. Based on these arguments, ion implantation may be designed with relatively low energy, depending on the Si template layer thickness. In addition, an adequate dose is always needed to amorphize the top portion of the Si template layer, easing the subsequent recrystallization during thermal anneal, and to realize the highest doping concentration.

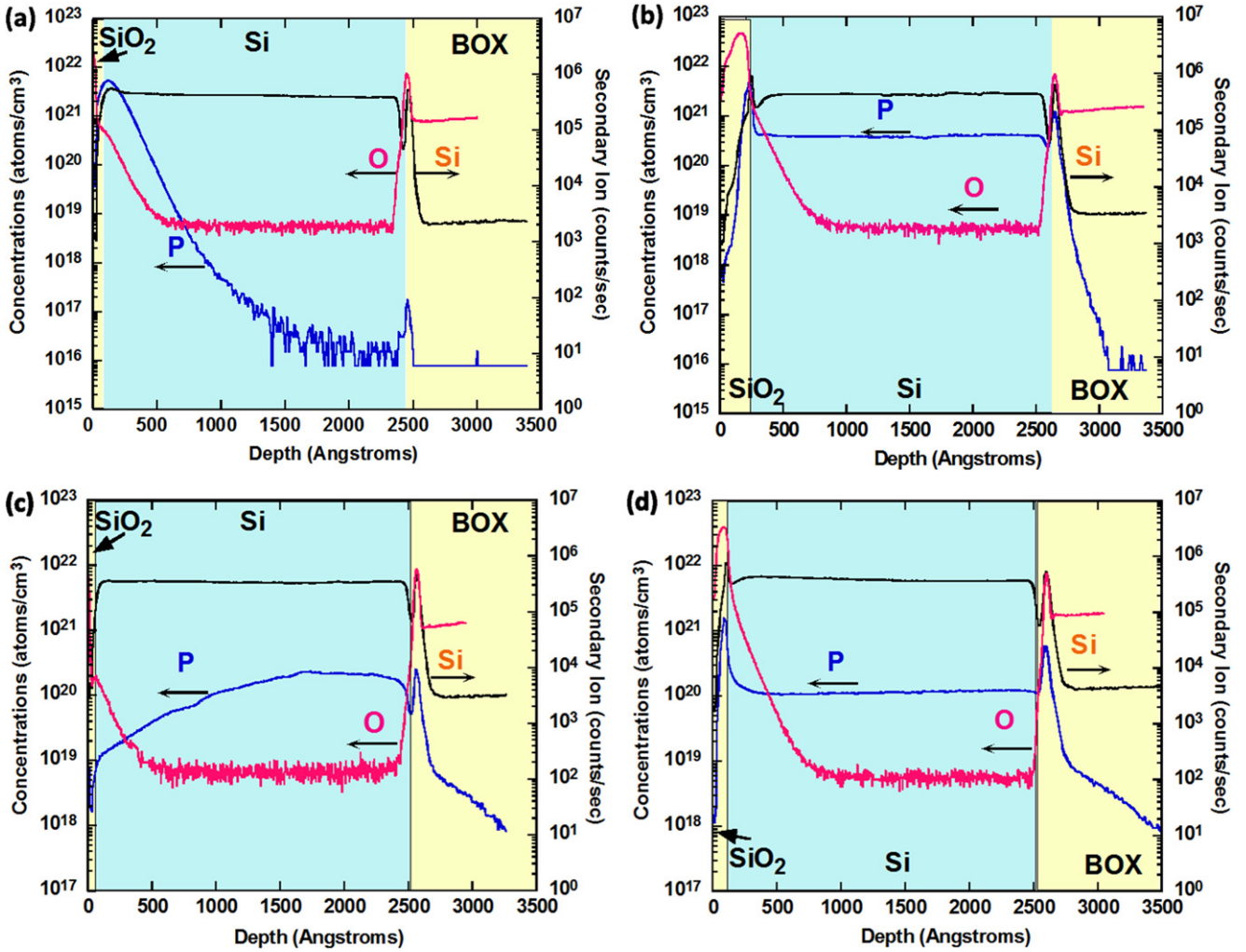

Figure 3. SIMS results of phosphorous doping profiles of two implantation conditions: 12 keV/1 × 10^{16} cm^{-3} (*a*) before and (*b*) after annealing; 150 keV/4 × 10^{15} cm^{-3} (*c*) before and (*d*) after annealing. A thin layer of screen oxide was grown before ion implantations. The nitrogen environment of the anneal furnace contains 5% oxygen, which caused further growth of top oxide layer, as indicated by the oxygen trace.

4. TFT design and performance

Using ion implantation as the pre-release doping method, a generic process flow using the flip transfer method and polyethylene terephthalate (PET) as the flexible substrate has been designed for fabricating flexible RF TFTs, as shown in figure 4. Due to the required use of the pre-release doping method for making TFTs on plastic substrates, the conventional self-aligned gate MOSFET process (i.e. 'S/D-after-gate') [37], which is effective in reducing gate-to-S/D capacitance, cannot be applied to flexible RF TFTs on these substrates. Instead, a 'gate-after-S/D' process is used for these flexible MOSFET TFT devices. Based on the process flow, several record-breaking devices have been reported. Due to the thermal instability of PET, which has varied softening point around 170 °C, the process temperature is tightly designed to accommodate the low substrate temperature. To meet the low-temperature requirement, gate stack and S/D metal are deposited by e-beam evaporation at room temperature. SiO is chosen as the gate dielectric due to its acceptable quality using e-beam evaporation and its higher dielectric constant than SiO_2 [38]. Many other high-*k* gate dielectric materials that can be deposited at PET tolerable temperatures can also be used to further and readily increase the device speed. The process starts from SOI material (figure 4(*a*)). Doping is introduced by phosphorous ion implantation (figure 4(*b*)) and annealed at a high temperature (typically 950 °C). With proper patterning of strip or mesh NMs, the sample is immersed in aqueous HF to undercut BOX (figure 4(*c*)). As BOX is fully removed (figure 4(*d*)), the top Si template layer is transferred to PET with the flip transfer method (figure 4(*e*)). A gate stack is formed consisting of SiO as the dielectric and Ti/Au as the gate metal (figure 4(*f*)) and then S/D metal of Ti/Au is patterned (figure 4(*g*)), concluding the process flow.

For the new TFT process, there are basically two design parameters in the generic process flow, as illustrated in figures 4 and 5. One is the separation or overlapping distance between the gate stack and S/D doping regions and the other is the gate length. It is noted that due to the use of non-self-aligned gate stacking, gate length and channel length do not refer to the same device dimension. Under the separated gate and S/D

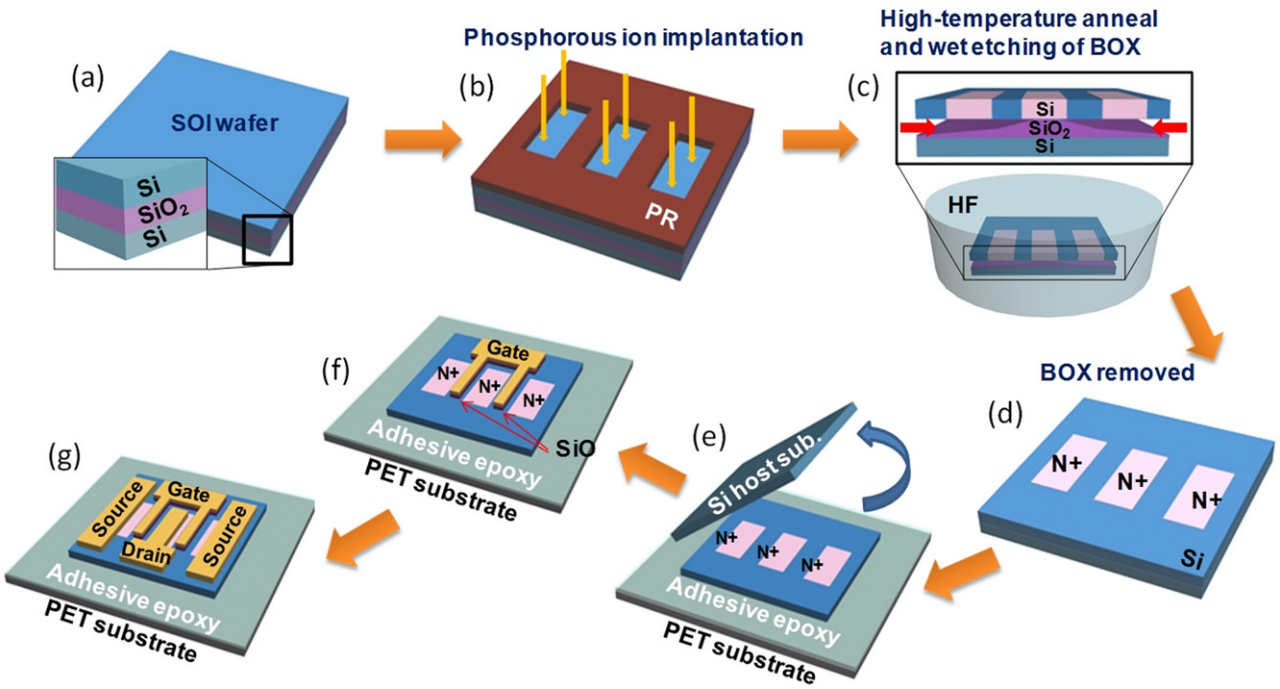

Figure 4. Generic process flow for fabricating flexible RF TFT using the flip transfer method. (*a*) The process starts from SOI material; (*b*) ion implantation for phosphorous doping; (*c*) sample is annealed to activate dopants and then immersed in aqueous HF to remove BOX; (*d*) after BOX removal, Si NM is ready for transfer; (*e*) Si NM is flip transferred onto PET with adhesive coating; (*f*) gate stack is formed using SiO as dielectric; (*g*) S/D metal contacts are formed.

condition, the channel length is larger than the gate length, and vice versa under the overlapped condition. Following the design of these two parameters, the structure evolvement of flexible RF TFTs are shown in figures 5(*a*)–(*c*). Figure 5(*d*) shows a microscopic image of a typical finished TFT with RF pads being connected. Corresponding to the three TFT designs shown in figures 5(*a*)–(*c*), the dc electrical characterization results of these devices are shown in figure 6(*a*). Clearly, the normalized drain current (per unit gate width) and thus the transconductance increase as the device structure is being improved. Along with the improvement of dc characteristics, the RF performance of the TFTs is also improved. A detailed analysis is given to explain how the improvement was achieved.

Following the demonstration of flexible TFTs using transferrable Si NMs with a cut-off frequency (f_T) of 515 MHz using solid source diffusion as the doping method [12], ion implantation was adopted to improve the doping of transferrable Si NMs. The first ion implanted RF TFT (TFT-1 in figure 5) has a relatively conservative design, where a non-overlapping gate-to-S/D structure with a 1 μm separation distance in between and a gate length of 2 μm is used. Its FOMs were reported as f_T of 1.9 GHz and maximum oscillation frequency (f_{max}) of 3.1 GHz (figure 6(*b*)) [15]. A refined design, as shown in figure 5 (TFT-2), changed the non-overlapping structure of TFT-1 to the overlapping gate-to-S/D structure with an overlapping distance of 0.5 μm. In addition, the gate length was shrunk down to 1.5 μm and the gate dielectric SiO thickness was reduced from 200 nm in TFT-1 to 100 nm in this device. The FOMs of TFT-2 were thus improved with a f_T of 2.04 GHz and particularly f_{max} of 7.8 GHz (figure 6(*c*)) [14]. A following design (TFT-3) kept the essence of channel length shrinking and the overlapping gate-to-S/D structure, and used 1 μm channel length. The FOMs of this device are increased to f_T of 3.8 GHz and f_{max} of 12 GHz (figure 6(*d*)) [13]. Along the evolvement from TFT-1 to TFT-3, drain current and transconductance (g_m) increase consistently (figure 6(*a*)).

$$f_{Ti} = \frac{g_{mo}}{2\pi (C_{gs} + C_{gd})} \tag{1}$$

$$f_{max} = \frac{f_{Ti}}{2\sqrt{(R_g + R_s) g_{ds} + 2\pi R_g C_{gd} f_{Ti}}}. \tag{2}$$

Reviewing the device structure evolvement and comparing them with the theoretical analysis of intrinsic cut-off frequency (f_{Ti}) and f_{max} in equations (1) and (2) provide clues about how the FOMs of the flexible TFTs have been improved and also a guideline for future design refinement [14]. In equations (1) and (2), g_{mo} is the intrinsic transconductance; C_{gs} and C_{gd} are the gate-to-S/D capacitance, respectively; R_g and R_s are the gate and source resistances, respectively; g_{ds} is the output conductance. By changing from the non-overlapping to the overlapping gate-to-S/D structure, R_s is significantly reduced while the gate-to-S/D capacitance, C_{gs} and C_{gd}, will increase. While f_{Ti} is compromised by changing the device structure from TFT-1 to TFT-2, the reduced R_s still benefits the improvement of f_{max}. Further shrinking the gate, and thus the channel length (TFT-3), directly improves both f_T and f_{max}. However, unlike device fabrication on rigid Si or other substrates, fabricating smaller feature sizes (<1–2 μm) poses severe challenges due to the soft nature of plastic substrates. The minimum temperature required by photolithography still

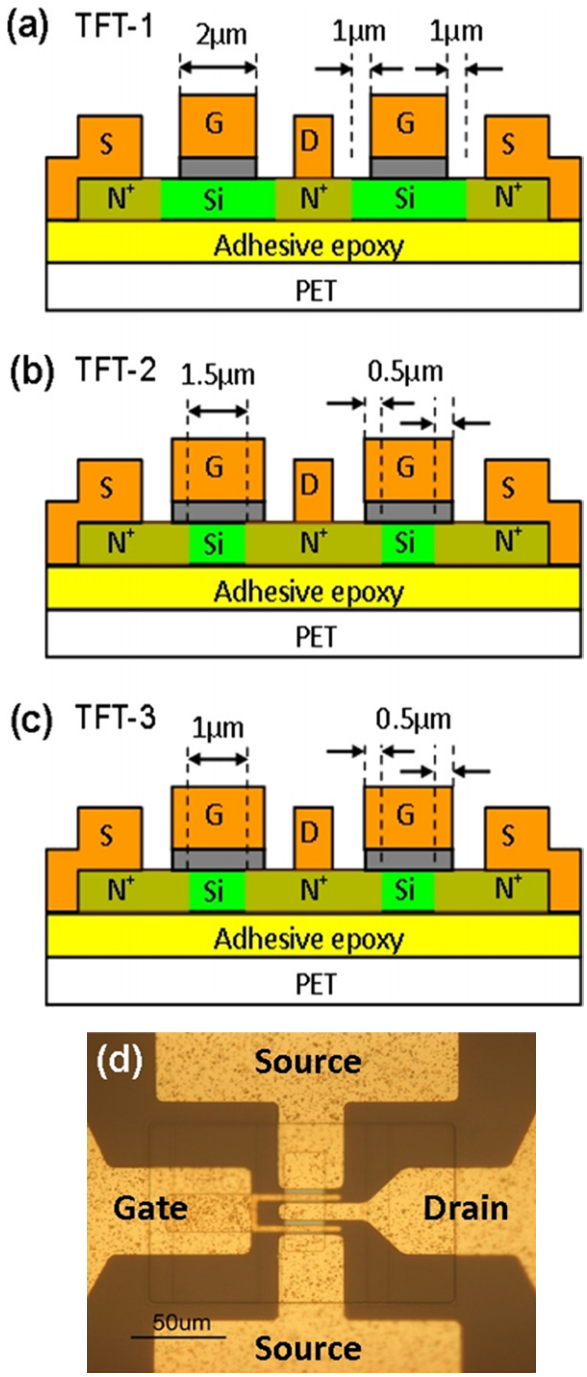

Figure 5. Evolvement of the structure of flexible RF TFT for better performance by reducing S/D resistance and channel length. (*a*) TFT-1 gate length/channel length = 2.0/3.0 μm; (*b*) TFT-2 gate length/channel length = 2.5/1.5 μm; (*c*) TFT-3 gate length/channel length = 2.0/1.0 μm. (*d*) Planar microscopic view of a typical TFT. Reprinted with permission from [13–15].

causes the substrate to have non-restorable deformation, making precise alignment with pre-doped regions of the transferred NMs on the soft substrates a difficult task. In TFT-3, a local alignment technique is used to overcome the misalignment caused by the softness of plastic substrates. The local alignment technique is conceptually similar to a stepper photolithography. Essentially, the alignment requirement on the soft plastic substrate is met by limiting the alignment area [13]. This issue will remain and become more challenging for even smaller channel lengths. In addition, reducing the gate oxide thickness will also contribute to better FOMs, but the gate leakage current sets a lower limit for the gate oxide thickness.

As the mechanical feature of flexible substrate indicates, the flexible devices are supposed to work under bending conditions which will introduce a strain in the active material. So acceptable performance variations under different bending conditions are essential for the flexibility to be treated as practical. The flexibility investigations are shown in figure 7. An optical image of a bent TFT array is shown in figure 7(*a*) and the electrical characterization under convex bending (tensile strain is induced along the channel width in this case) is also shown. The effective carrier mobility of electron, which is the carrier that is directly related to the performance of NMOS TFT, is extracted from the TFT linear operation regime under different bending conditions and normalized by its effective mobility with no bending [12]. As shown in figure 7(*b*) [12], only small variations are observed even when the bending is quite large with a radius of curvature as small as 3 mm. Although electron mobility, as a basic material parameter, will significantly influence the device performance, many other factors, such as the deformation of gate dielectric under bending conditions, can also affect device performance, particularly device reliability, with complicated mechanisms. An overall evaluation of the device frequency response performance is more meaningful to circuit implementation, as shown in figure 7(*c*) [13]. FOMs including f_T and f_{max} are extracted under different bending conditions of TFT-3. Small variations are observed based on the observation of electron mobility.

5. Demonstrations of other active and passive flexible RF devices

In addition to the active RF TFTs, other active and passive devices are also necessary for a functional flexible RF system. In this section, we review the demonstrations of flexible RF switches and flexible inductors and capacitors. These components are demonstrated such that their fabrication process is fully compatible with the flexible TFT process flow, paving the way towards future integration with the active devices for more complicated system implementation.

A microscope image of the fabricated flexible RF single-pole single-throw (SPST) switch, which consists of shunt and series P–intrinsic (I, unintentionally lightly p-type doped)–N (PIN) diodes, is shown in figure 8(*a*) (area of diodes: D1 = 240 μm^2 and D2 = 40 μm^2), with the inset showing its schematic layout. The mechanical flexibility of the switch is seen in the optical image where a finished switch array is bent (figure 8(*b*)). The inset in figure 8(*b*) shows the detailed bending direction relative to the switch's layout configuration. The fabrication process for the RF switch is almost identical to that for the TFTs, except that an additional step of ion implantation of boron is needed for P-type doping and that there is no gate stack needed, which actually simplifies the process flow on flexible substrate. A cross-sectional structure

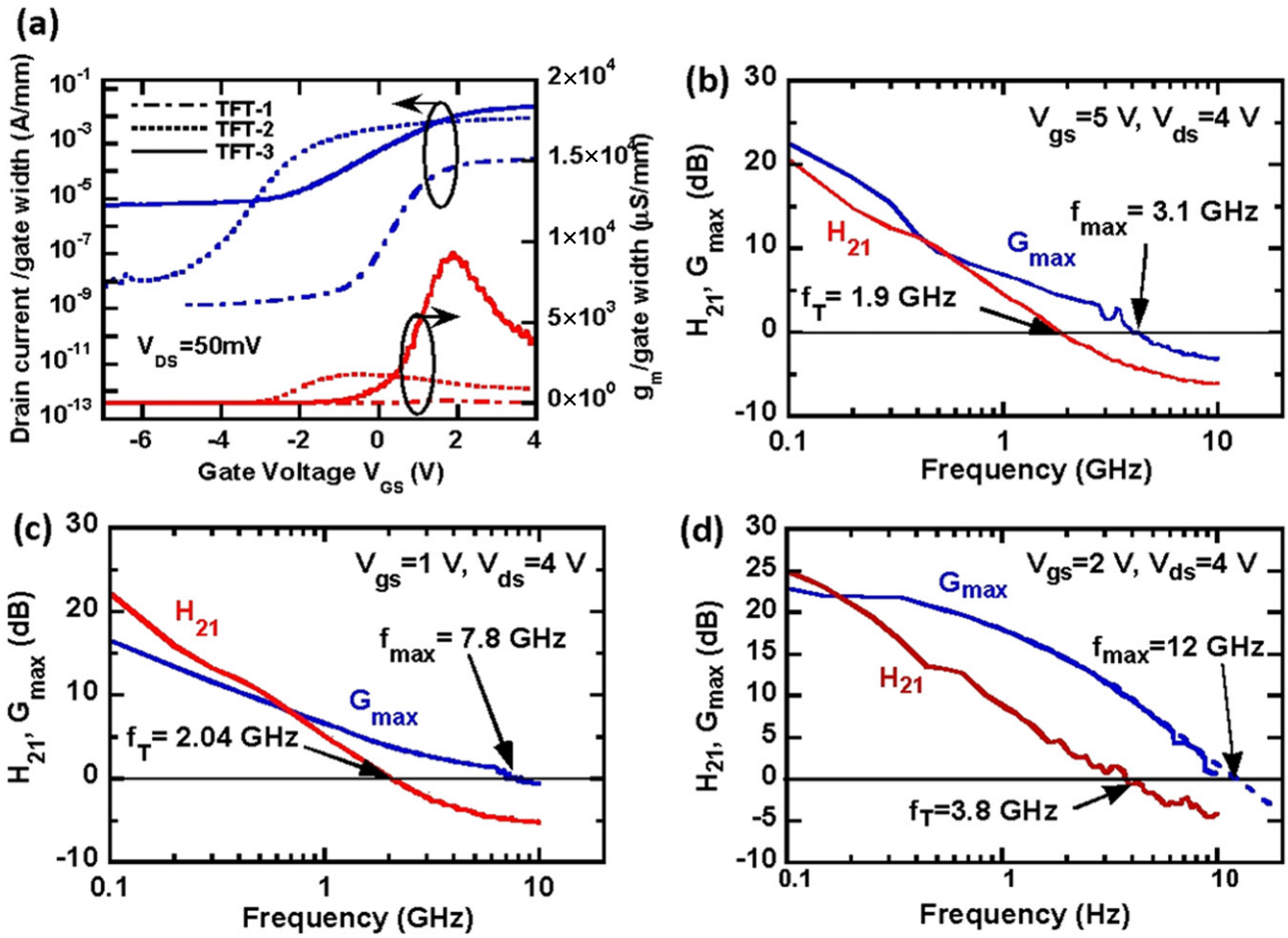

Figure 6. Electrical characteristics of three types of RF TFTs corresponding to figures 5(*a*)–(*c*). (*a*) Gate-width-normalized drain current and transconductance versus gate bias; (*b*)–(*d*) RF FOMs corresponding to device structures TFT-1 to TFT-3, respectively. Reprinted with permission from [13–15].

illustration is given in figure 8(*c*). Measured insertion loss in the ON state is as low as 0.93 dB and isolation is 6.9 dB at 20 GHz, as shown in figure 8(*d*), indicating high RF switch performance [39].

The RF characteristics of the switch under different uniaxial bending radii are shown in figures 8(*e*)–(*h*) [39]. The bending direction is shown in the inset of figure 8(*b*). Figure 8(*e*) shows the OFF state ($I_f = 0$ mA) performance of the RF switch (both diodes have an area of 40 μm^2) under different bending radii. Negligible changes of S21 were observed. Apparently, the strain has negligible effects on the resistance of D1. Since D1 also dominates S11 and S22 in the OFF state, no substantial changes in the measured S11 and S22 were observed, as shown in figure 8(*f*). Figure 8(*g*) shows the OFF state isolation and the return loss of the switch under bending when D2 was forward biased ($I_f = 0$ mA, $I_2 = 10$ mA). Again, no substantial changes were measured for S21 due to bending. In addition, S11 stayed unchanged by the bending. However, S22 was substantially improved due to the influence of the forward biased D2. Within the improved values, no strain-induced effects can be observed.

The ON-state ($I_f = 10$ mA, D2 zero biased) RF characteristics of the RF switch under bending are shown in figure 8(*h*). It can be seen that improved insertion loss (S21) and return loss (S11 and S22) were observed for the RF switch with the increase in the tensile strain. The observed changes in switch performance are ascribed to strain-induced mobility changes, which further cause the relevant resistance changes in the respective diodes. Detailed analyses of these relations can be found in previous publications [39, 40]. The flexible RF switches are also robust against repeated bending testing.

The demonstration of flexible RF switches not only contributes to enriching the flexible device family and supports the integration of more complicated RF system, but also further validates the incorporation of both N- and P-type doping, which is essential for comprehensive conversion of Si devices from a rigid substrate to a flexible substrate, such as complementary metal–oxide–semiconductor (CMOS) and bipolar junction transistor (BJT) devices.

Capacitors and inductors are indispensable components in RF circuits for providing proper dc bias and impedance match. These passive components have been demonstrated on flexible substrates with very high operation frequencies. The fabrication process flow for integrated capacitors and inductors is shown in figure 9 with well-controlled process temperatures so that this process is fully compatible with that used for flexible RF TFT fabrication and thus also compatible with the low-temperature PET substrates. The fabrication of capacitors and inductors on PET consists of patterning of three metal layers and related interlayer dielectric. The first metal

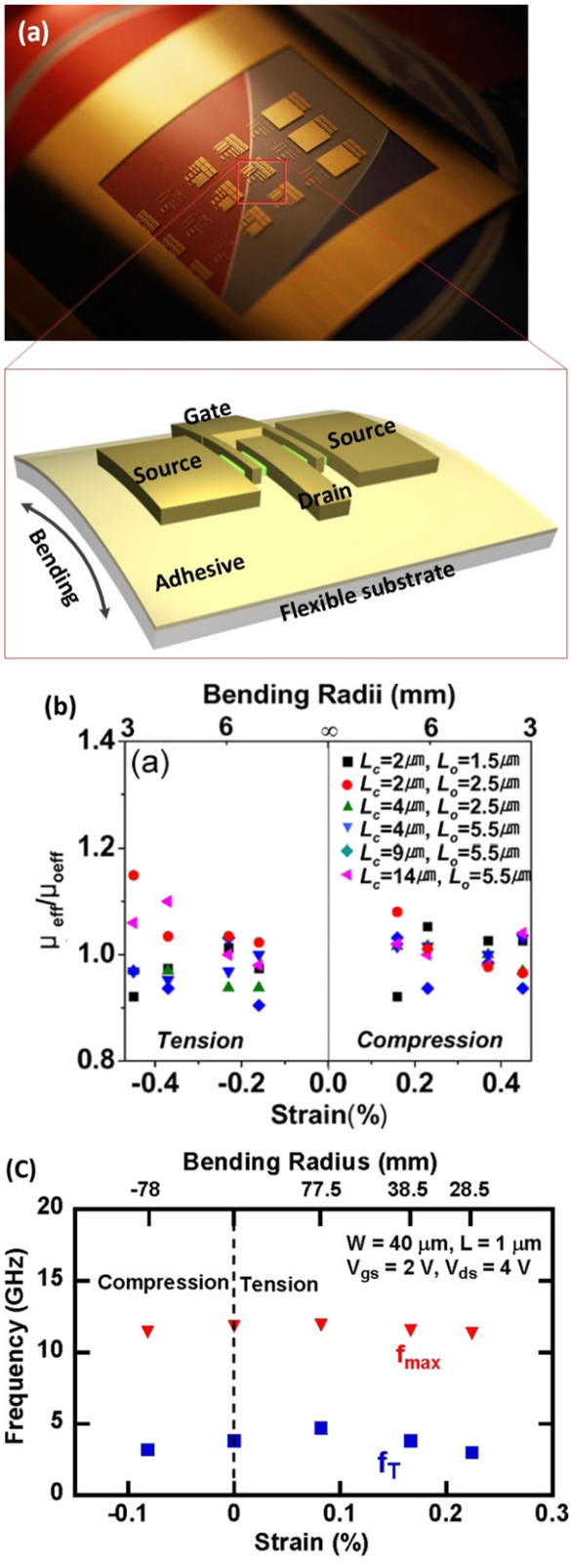

Figure 7. Demonstration of flexibility of RF TFT. (*a*) An optical image of a bent array of RF TFTs and schematic illustration of bending test; (*b*) normalized effective mobility ($\mu_{\text{eff}}/\mu_{0\text{eff}}$) as a function of bending-induced strain and bending radius from [12]; (*c*) operation frequency versus bending radius and strain for TFT-3. Reprinted with permission from [12, 13].

(M1) is patterned as the bottom electrode of metal–insulator–metal (MIM) capacitors and the centre lead metal of inductors (figure 9(*a*)). Then the photoresist lift-off method is used to pattern SiO as the capacitor high-*k* dielectric and metal as the top capacitor electrode simultaneously to form a self-aligned structure (figure 9(*b*)). The high *k* of SiO increases the capacitance value of the capacitors. SU-8 is spun and patterned with UV photolithography to form the open via holes, while the cured region works as the inter-metal low-*k* isolation layer (figure 9(*c*)). The low *k* of SU-8 reduces the parasitic capacitance of inductors and improves the operation/self-resonance frequency. Finally, the third metal (M3) is patterned as the spiral metal of inductors and interconnects to finish the entire process flow [41].

Microscope images of finished inductors and capacitors are shown in figures 10(*a*) and (*b*), respectively. The flexibility of these components is exhibited in a bent array of inductors and capacitors (figure 10(*c*)). High RF performance is also exhibited by these components. For a 4.5-turn inductor, a stable inductance (L) of about 6 nH was measured from 45 MHz up to about 5 GHz, with a resonant frequency (f_{res}) of 9.1 GHz (figure 10(*d*)) and a peak quality factor (Q) of 14.6 was achieved at 3.45 GHz (figure 10(*e*)). A capacitance of 0.45 pF was measured at 4 GHz, with a f_{res} of 13.5 GHz (figure 10(*f*)). The inductors and capacitors were also measured under bending conditions using fixtures with radii of curvature as small as 28.5 mm, and the performance variation was within the acceptable range [41]. The bending results are plotted in figures 10(*d*)–(*f*), along with the results obtained from the flat condition.

From a fabrication process point of view, the demonstrations of flexible capacitors and inductors are also feasibility validations of multiple interconnect metal layers on flexible substrates. Although most reported flexible devices are discrete, functional systems commonly consist of a large number of integrated devices with complicated interconnection. Multi-level metal interconnect may be needed for the complicated systems and, with the demonstrations, these circuits and systems can be expected within sight.

6. Outlook and future directions

Future research directions of fast flexible electronics can be summarized in the following three aspects: further improving the performance of existing flexible devices, converting more rigid active and passive devices to flexible ones and process integration towards more complicated systems.

As we have reviewed, mature and effective technologies in industry that have driven the development of traditional rigid semiconductor devices will also be potentially applicable to flexible devices. Although there are some technical issues that need to be addressed when fabricating devices on flexible substrates, channel length downscaling is the most readily available paradigm [37] that should be investigated. The evolvement of the current flexible RF TFTs has demonstrated the efficacy of downscaling to significantly improve the operation frequency. The smallest channel length of flexible

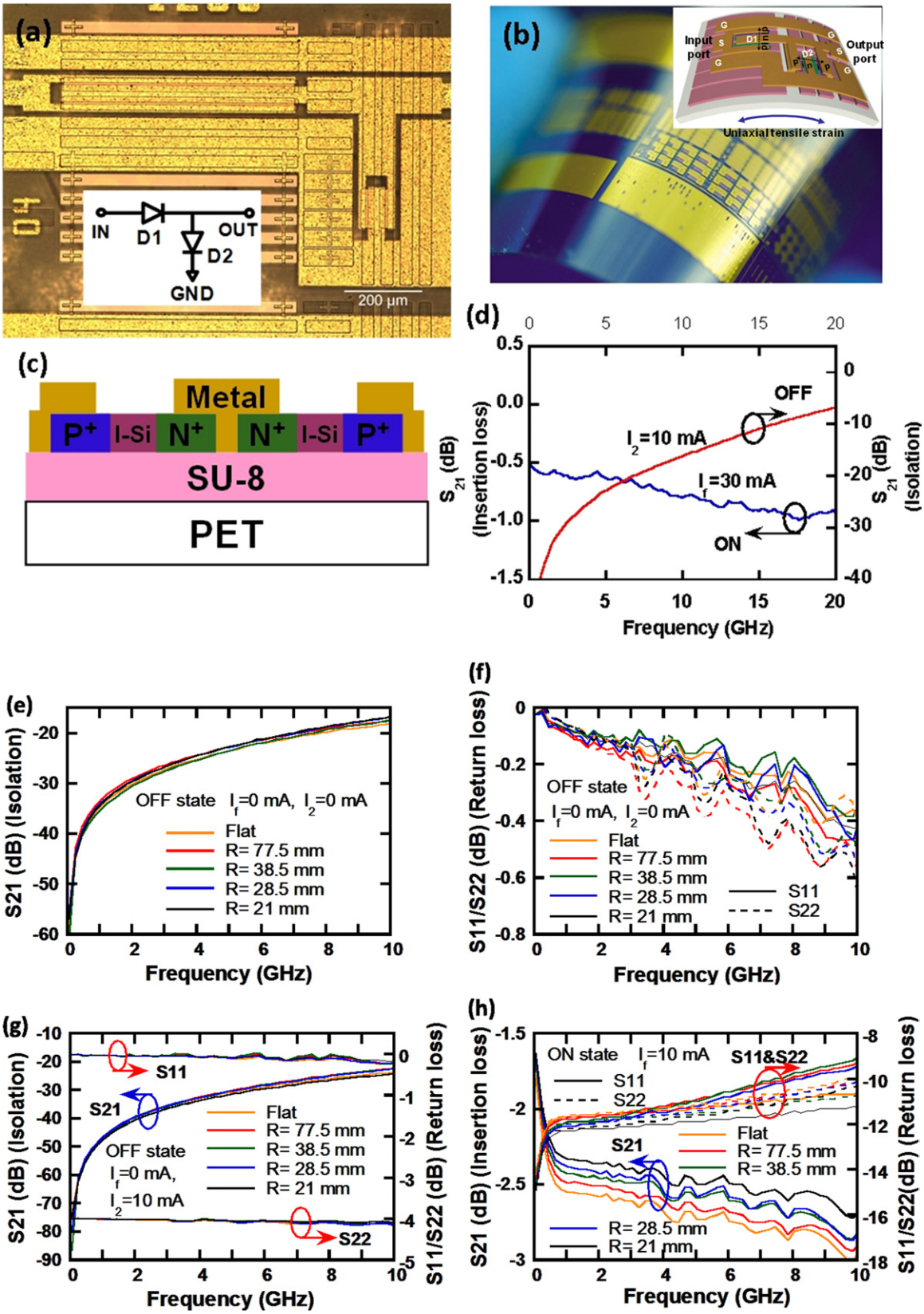

Figure 8. Demonstration of flexible RF switch and characterizations without bending and under uniaxial bending. (*a*) Microscope image of a shunt-series PIN diode SPST switch and its schematic circuit diagram; (*b*) optical image of a bent switch array with inset showing the detailed bending direction relative to the switch's layout; (*c*) cross-sectional illustration of the PIN diode; (*d*) measured insertion loss (ON state) and isolation (OFF state). The series and shunt PIN diodes have area of 240 μm^2 and 40 μm^2, respectively. The ON state is biased at I_f of 30 mA on D1. OFF state is biased at zero bias on D1 and I_2 of 10 mA on D2; the series and shunt PIN diodes both have area of 40 μm^2 for (*e*)–(*h*). (*e*) Measured S21 (isolation) and (*f*) S11 and S22 (return loss) of shunt-series SiNM PIN SPST switch in the OFF state $I_f = 0$ mA, $I_2 = 0$ mA. (*g*) Measured isolation and return loss under OFF state with bias $I_f = 0$ mA, $I_2 = 10$ mA. (*h*) Measured ON-state ($I_f = 10$ mA) insertion loss and return loss of the switch. Reprinted with permission from [39].

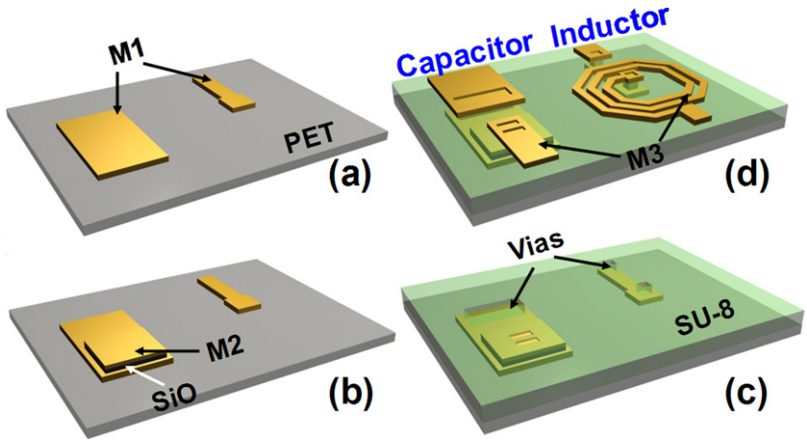

Figure 9. Process flow of flexible capacitors and inductors. (*a*) The first metal (M1) is patterned on the PET substrate as the bottom electrode of MIM capacitors and the centre lead metal of inductors. (*b*) SiO and the second metal (M2) are patterned by self-aligned lift-off as capacitor high-*k* dielectric and top electrode for capacitors. (*c*) SU-8 is spun and patterned with UV photolithography so that via holes are opened while the cured region works as the inter-metal low-*k* isolation layer. (*d*) The third metal (M3) is patterned as the spiral metal of inductors and interconnects. Reprinted with permission from [41].

TFTs that are directly fabricated on PET is only 1 μm [13]. This channel length, compared with today's deep-sub-micrometre industry capability, leaves plenty of room for further performance improvement on flexible substrates. As described earlier, alignment with pre-doped regions of the transferred NMs on soft substrates in the gate-after-S/D TFT process stands for a difficult task. While local alignment for 1 μm feature size [13] is proved to be cost effective, further reducing the size of the critical features will render the local alignment method cost ineffective. New fabrication techniques that allow rough tolerance of alignment, while maintaining the use of smaller critical feature sizes, are thus needed. Considering that 12 GHz has been realized on Si-based TFTs using only 1 μm channel length and that this critical dimension is considerably large from today's industrial point view, much better performance can be expected from flexible TFTs by using more advanced fabrication techniques.

An alternative approach to overcoming the misalignment issue on PET substrates at smaller feature sizes is to look for and use flexible substrates that have better thermal and mechanical properties than PET and the like. However, keeping the cost of the flexible substrates low should always be the major consideration in selecting a proper flexible substrate. For RF applications, RF loss at microwave frequencies of any new flexible substrate also needs to be considered. In addition to downscaling the critical dimensions of devices, gate dielectric engineering needs to be explored for low-temperature applications with a high dielectric constant in order to further increase the device speed. The current high-speed devices directly fabricated on PET employ evaporated gate dielectric materials. While the major advantage of using an evaporated dielectric is low temperature, the quality of the dielectric material is poorer than thermal oxide or other oxide deposited by atomic layer deposition. For this reason, high off-current, and thus low on/off ratio, was constantly observed from the flexible TFTs. In addition, with the reduced quality of the gate dielectric, a very thick layer often has to be used, which severely affects the device speed. In addition to NMOS for analogue/RF applications, complementary MOSFET TFTs also need to be developed for digital and switching applications on flexible substrates.

One way to circumvent the challenges associated with direct fabrication of small featured active devices on flexible substrates is to fully fabricate the active devices on their original host substrates and devise methods to release the fully fabricated devices and transfer them to flexible substrates [42]. For this method, releasing the devices with minimal degradation of the device performance and transfer printing them with high registration accuracy then become the key factors. Yet, using this alternative method large-area circuits and systems can be fabricated without using the same size masks, which has been considered as one of the major advantages of the transfer printing technique.

Channel material engineering is another route towards high-speed TFTs, which has been readily employed in industrial transistor technology for years. For Si-based TFTs, strained channel can be applied to improve the device speed, as indicated by the recent demonstration of strained Si TFTs on plastic substrates under dc condition [33]. Although flexible RF TFTs employing strained Si have not been reported and effectively minimizing the parasitic resistance for creating RF TFTs using the strained Si is still a challenge, the beneficial effect by increasing carrier mobilities using strain have become noticeable [33, 43]. Other semiconductors can also be further explored as active device materials, such as Ge and III–V materials [16–18, 44–46], to take advantage of their respective merits. For some of the non-Si-based semiconductor materials, other types of devices such as MESFET, HEMT, etc [47] may be used instead of MOSFET, for which large difference is not observed in the device fabrication methods with a rigid or a soft host. Although current flexible TFTs are essentially based on field effect transistors (FET), BJTs, which have a number of advantages over FETs, may also be used as TFTs (never demonstrated so far) and be fabricated on flexible substrates provided that low cost fabrication processes can be used on flexible substrates and the heat dissipation therein can be managed.

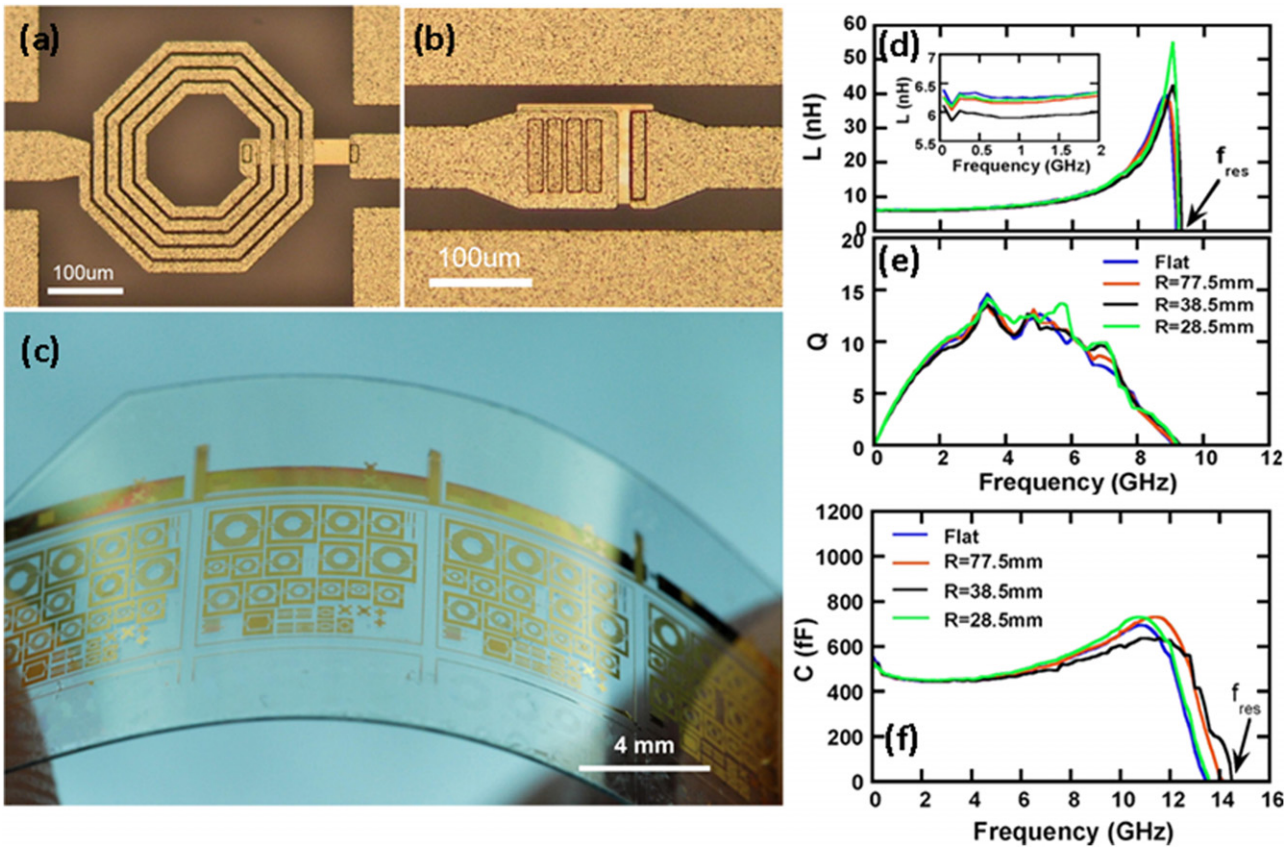

Figure 10. Demonstration of flexible capacitors and inductors. Microscope image of (*a*) a flexible inductor and (*b*) a flexible capacitor on a PET substrate. (*c*) Optical image of a bent array of flexible inductors and capacitors. Measured (*d*) L values and (*e*) Q values versus frequency of a 4.5-turn spiral inductor under flat and different bending conditions. (*f*) Measured C values versus frequency of a $40\times40\,\mu m^2$ MIM capacitor under flat and different bending conditions. Reprinted with permission from [41].

Lumped passive components [41] can generally fulfil the requirements of RF circuits operating at frequencies of a few gigahertz. Different from the fabrication of active devices where critical dimensions are the major challenge to overcome, passive elements generally do not require very small lateral features or high alignment accuracy. The major drawbacks of the current fabrication techniques for passives on flexible substrates, however, are still mask based, with little difference from the process used to fabricate passive components on rigid substrates except for the selection of inter-metal dielectric materials. The major limitation of mask-based fabrication is the size of the circuit to be fabricated. Since one of the major advantages of flexible electronics is to implement large-area circuits, non-mask-based passive element fabrication methods are needed. Furthermore, for low cost and large throughput reasons, roll-to-roll (R2R) fabrication of these elements is strongly desired. One fabrication option that can be used for R2R is the direct writing of the passive elements using inkjet printing [48]. To realize high-performance passive elements, high-conductivity inkjet materials and also often thicker conductive layers are generally needed, which could be of some challenge for the inkjet printing method. As the operation frequency goes higher towards millimetre wave frequencies, more advanced passives, other than lumped ones, are needed. For a few gigahertz microwave applications and even very high radio frequency applications, more challenges may exist for realizing high-performance passives than active devices on flexible substrates.

It has been shown that mechanical bending varies the performance of both active devices [12, 13, 16] and passive components [41]. In practical applications, the performance variation due to bending, particularly under the situation of continuous bending, may not be desired, besides complicating circuit design. To eliminate the bending effects on device/circuit performance variations, symmetrical packaging/lamination with the use of double flexible substrates, enabling a neutral plane, where active and passive components reside, may be one of the solutions to this problem. Previous demonstrations have proved the feasibility of this neutral plane approach [48].

Process integration for fast flexible electronics towards more complicated circuits and systems may be another challenging but essential issue to address in the future. Similar to the situation of rigid device based solid-state circuits, integration of a large number of different types of active devices can lead to complicated circuit functions with superior overall system performance. Taking Si (and SiGe) BiCMOS technology for example, mixed-signal systems can be more easily realized based on the single-chip integration of BJTs or heterojunction bipolar transistors (HBTs) with CMOS than based on only one type of the active devices. As a matter of fact, more integration flexibility exists using flexible substrates than

using rigid substrates due to the availability and versatility of the transfer printing techniques [49], while the conventional integration methods currently employed on rigid substrates limit the number of types of devices to be integrated together. However, fabricating multilevel metal interconnect with low loss at RF may be of a larger challenge on flexible substrates than on rigid substrates, considering the process complexity and the potential need of planarization procedure as in the rigid substrate case. Moreover, to fulfil the requirements of low cost of flexible electronics, R2R fabrication of high-frequency circuits on flexible substrates may create more interest and could also be the eventual, ideal goal of fabrication of fast flexible electronics. Nevertheless, a number of challenges to realizing R2R fabrication still lie ahead. Obviously, these challenges are worth further explorations to overcome.

7. Conclusion

In this paper, we reviewed some important issues related to the development and future directions of fast flexible electronics. Material preparation was described in detail as to how the Si NM can be released from a commercial SOI material and transferred onto a flexible substrate. Guidelines for ion implantation of dopants were provided to achieve minimum parasitic resistance in RF TFTs. The structure evolvement of flexible RF TFT with a pre-release doping method proves the favourable structure of overlapped gate-to-S/D and the effectiveness of channel length scaling down in improving the TFT RF performance. Due to the intrinsic similarity between flexible monocrystalline Si nanomembrane based devices and the commercial rigid Si devices, effectively adopting the mature techniques used in rigid semiconductor industry is promising to boost flexible active device performance in the future. With the demonstration of flexible PIN diodes and RF SPST switches as examples of RF components, and inductors and capacitors as passive components, not only is the flexible device family broadened, but it is also more influential from the viewpoint of process engineering that both n- and p-type of doping and interconnection with multiple metal layers for complicated systems are feasible on flexible substrates. Future research and exploration directions were outlined and projected. In the long term, an industrial transition of electronics from rigid substrate to flexible substrate, with lowered cost and enlarged form factors, for many applications can be expected.

Acknowledgments

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