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Layer	Name	Material	Thickness	Constant														
Layer	Top Overlay	IVIO COI IOI	111101111000	Constant	-													
	Top Solder	Solder Resist	0,025mm	4									75,1	OOmm—				
1	Layer1 Top		0,035mm															
	Dielectric1	PP-006	0,160mm	4.7					D								D D	
2	Layer2		0,035mm				"					000	_	0	0 0 0		п	
	Dielectric2	Core-039	1,130mm	4.74					_								J	
3	Layer3		0,035mm				444		0	0	0 0			_ °	0 0 0 0	о о	×	
	Dielectric3	PP-006	0,160mm	4.7			<u> </u>	1		0	0 (, .						
4	Layer4 Bottom		0,035mm]										
	Bottom Solder	Solder Resist	0,025mm	4				ļ									0 000	
	Bottom Overlay		L					,		р (-					_		
Total	board thickness:		1,640mm											п	□	0 0		
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Svmbo	Hit Count Fin	ished Hole Size	Plated Ho	ole Type I	Orill Layer Pair	1	44,							_ 0	0 0 0 0			
		00mm (7,87mil)			_ayer1 Top — Layer4 Bottom	1	I [1	0	0	0 0			_	_			
_ 7		00mm (31,50mil)	PTH Sk		_ayer1 Top — Layer4 Bottom		4 4	1								J	×	
		00mm (39,37mil)	1 1		_ayer1 Top — Layer4 Bottom		-	,										
Ħ		00mm (39,37mil)	PTH Sk		_ayer1 Top — Layer4 Bottom		-		1								D	
~ %		00mm (51,18mil)	1 1		_ayer1 Top — Layer4 Bottom				,								b	
		00mm (51,18mll) 00mm (102,36mil)	1 1															
)	4 2,6 492 Total	outiti (102,36mil)	FID K	ou 10 I	_ayer1 Top — Layer4 Bottom	4												
Clot da		th Lanath - Calaid	lated from to	al otart contr	re position to tool end centre	_ position												
SIOT GE	Hole Lengt	th = Routed Path	Length + To	ol Size = Sk	e position to tool end centre ot length as defined in the PC	B layout												
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Project:

Date:

12.05.2023

All drills (PTH and NPTH) should run in one work process

PCB Designer:

CSI2-ZCU106-EVK_Rev01.PcbDoc

File Name:

OFU

Layer Name:

Drill Drawing

SCALE: 1.00

Bare Board Number:



