ECEN 5014 Final Project - A 5-GHz 5.8-W Class-A GaN Power Amplifier

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***Abstract*—A 5.8-W 5-GHz Class-A GaN amplifier is designed on a 2.5-by-2.5mm die using the TriQuint 0.25um GaN 3MI Design Process. At an input power of 22dBm it is unconditionally stable and produces 37.54 dBm of output power, with a PAE of 52.98%.**

***Index Terms*—Power amplifiers, field effect transistors,**

I. Introduction

This paper documents the design of a 5.8-W 5-GHz Class-A GaN amplifier using the TriQuint 0.25um GaN 3MI Design Process.

Semiconductor foundries are generally classified into two groups: pure-play foundries and integrated device manufacturers. Pure-play foundries only fabricate ICs and do not do design in-house, mostly working on contract from semiconductor companies that do not own their own foundry. TSMC is a pure-play foundry that works in gallium nitride (GaN), and silicon germanium (SiGe); GlobalFoundries works in SiGe and silicon-on-insulator (SOI) among others. Fabless companies include Qualcomm (GaAs), GaN Systems (GaN), Nvidia (CMOS, SOI) and AMD (CMOS).

Integrated Device Manufacturers design and fabricate their own circuits. Peregrine/Murata work in Silicon-on-Sapphire (SOS) and SOI. Qorvo provides foundry services in GaAs and GaN. The library used in this design is from Qorvo.

II. Biasing the Nonlinear Model

The linear model provides a choice of V_{ds} from 15V to 40V in steps of 5V. The nonlinear model used is a 10-finger transistor with a gate length of 150 microns.To bias the nonlinear model to the same point as the linear model, the current density (i.e. 80mA/mm) is multipled by the gate periphery (number of fingers * gate width, $10 * .20mm = 2mm$). Locating this total current (80mA/mm*2mm=160mA) on the IV curve (Figure 1) will indicate which gate bias will provide that desired current – the design is thus biased at 30V at the drain and -2.7V at the gate. Simulation of the DC current verifies the desired bias voltage and current.

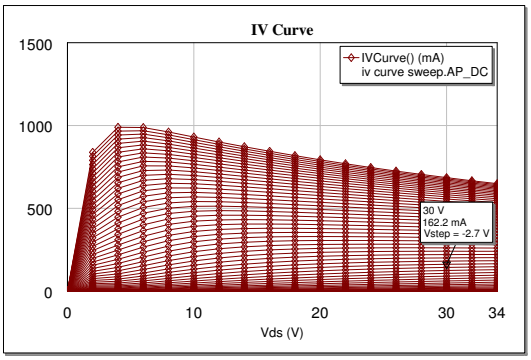

Fig. 1. Calculating the drain current will indicate the bias point that should be selected.

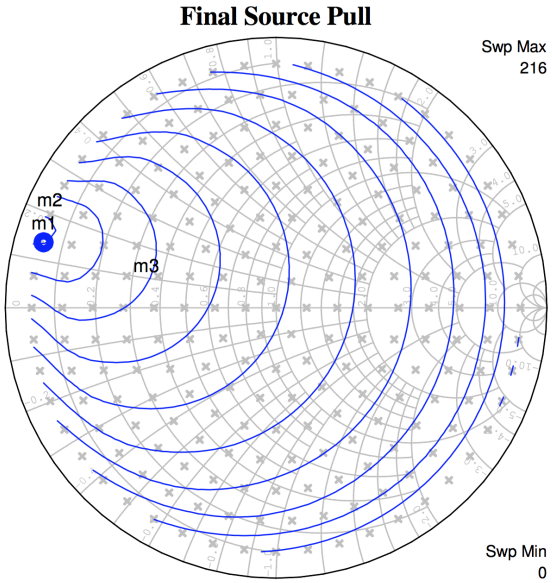

Fig. 2. The gate of the transistor should be presented with an impedance of $2.9094 + 6.8929j\Omega$.

III. Source and Load Pull

In order to maximize the total output power and power-added efficiency (PAE), source- and load-pull simulations are performed with 22dBm of input power to find the impedances that should be presented to the gate and drain, respectively. The results are shown in Figures 2 and 3. Figure 3 shows the load-pull curves for both total output power and power-added efficiency, which are not perfectly aligned but are fairly close. By maximizing load-pull there is a 7-point drop in PAE and by maximizing PAE 1.6dB of total power is sacrified. A load impedance between the two maxima was chosen, and the determined impedance with which to present the drain of the transistor is determined to be $18.1124 + 25.95j\Omega$.

Figure 4 uses ideal tuners to present the simulated load and source-pull values.

IV. Distributed Input and Output Matching Networks

The input and output matching networks consist of the bias tee and the matching network. The bias tee should be placed close to the transistor. Its function is to bias the transistor at the correct large-signal position on the IV curve and provide the small-signal voltage swing while preventing the RF and DC inputs from interfering with each other.

The input bias tee is implemented with a large DC blocking capacitor (8.323 pF) and a spiral inductor which acts as an RF open and a DC short. Inductors are prone to loss, but it is more important to avoid loss on the output side than on the input

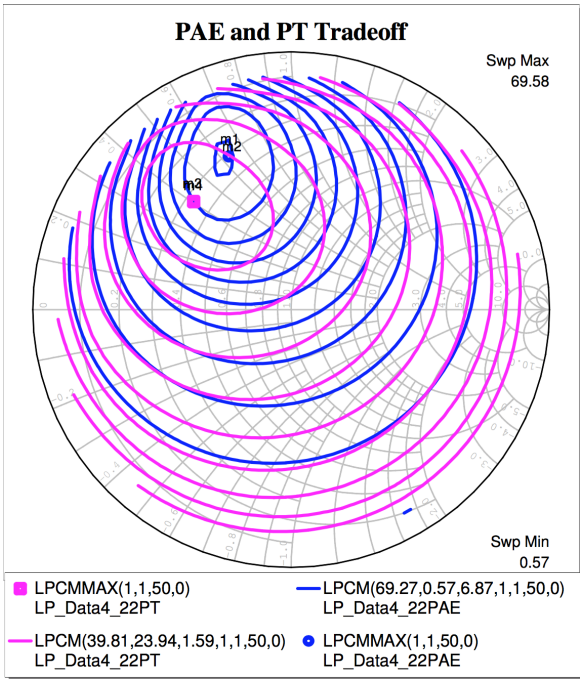

Fig. 3. The maximum of the PAE load-pull yields 38.22 dBm and a PAE of 69.27%. The maximum of the total output power load-pull yields 39.809 dBm and a PAE of 62.4%.

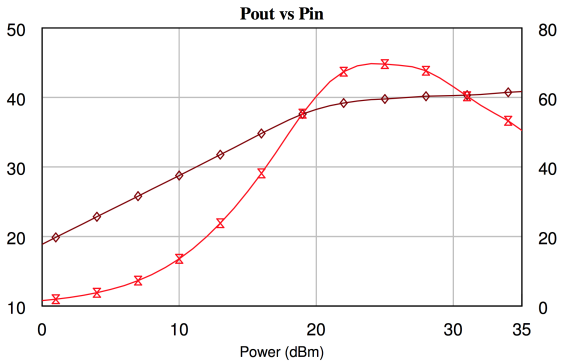

Fig. 4. With 22dBm of input power there is a total output power of 39.2 dBm with a PAE of 67.4%.

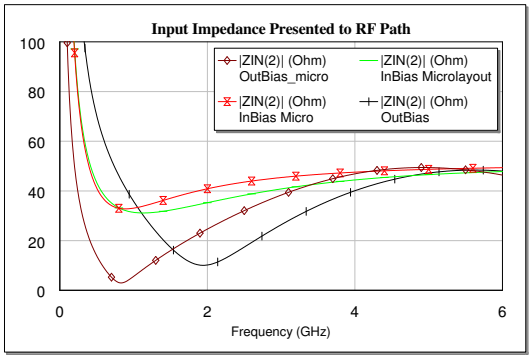

Fig. 5. The amplifier gate and drain both ”see” a high input impedance around 50 ohms.

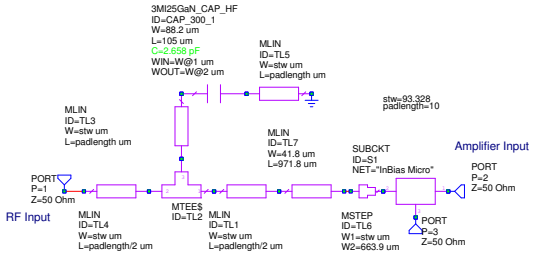

Fig. 6. The input matching network, designed to maximize output power while providing a good match across a wide bandwidth and conserving space.

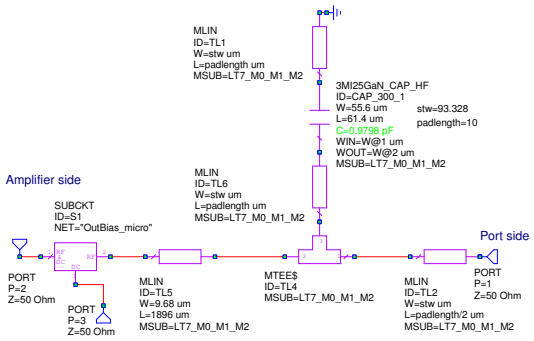

Fig. 7. The output matching network, designed to minimize loss and maximize output power.

side – furthermore the spiral inductor helps to conserve space on the die.

The output bias tee consists of a long line approximately a quarter-wavelength long with a high-density capacitor at the other end, meaning a short circuit at the RF frequency which becomes transformed to an open once it reaches the RF path of the tee. The high density capacitor has a value of 83.57 pF, which is very large but is only 285 by 253 microns as compared to the 17.94 pF DC blocking capacitor which occupies 250 square microns.

As shown in Figure 5, the bias tee should present close to 50 ohms of impedance to the RF path to avoid reflections of signal. The matching network is where the 50 ohm input/output ports are to be transformed to the optimal gate and drain impedances. An LC network is used for the tuning networks, in which a narrow transmission line and a lumped-element capacitor are selected. The lumped element capacitor increases the bandwidth of the match, but inductors are prone to loss and thus a narrow transmission line is chosen instead. In the case it is observed that adjusting the matching network is affecting the scattering parameters of the bias tee network, it is recommended to return to the bias tee design and ensure that

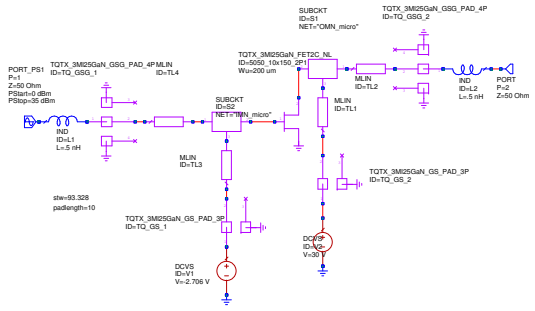

Fig. 8. The final amplifier in microstrip in simple geometry - modifications for bends and curves are not shown.

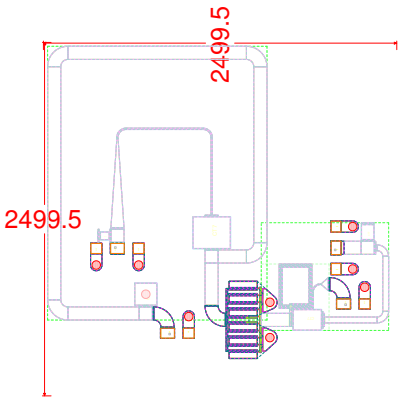

Fig. 9. The final amplifier layout.

the 50 ohm impedance is still being presented. Ultimately, port 2 in Figure 6 and port 2 in Figure 7 should see the impedances chosen from Figures 2 and 3.

V. Amplifier Layout

In reality, an amplifier in operation does not have an ideal port and there are a number of elements that can be added to try and approximate the non-idealities created by connecting power sources and measurement tools at input/output ports.

As shown in Figure 8, DC pads should be added to the biasing sources - each provides a via inductance of 0.032 nH and 0.02 Ω via resistance. The RF input and output of the amplifier are passed through a GSG pad and a .5nH inductance which represents a bondwire inductance. Furthermore, in order to pass the design rule check, curves and bends will have to be added to lines and element connections to avoid overlap of elements while fitting the amplifier onto the 2.5-by-2.5mm die. The added parasitic capacitances and resistances of the DC pads, bond wires, probe pads and lengths of layout line require that the bias tee and matching network be checked and readjusted to preserve performance.

VI. Performance of Final Design

Figure 9 shows the final layout of the amplifier. The wide, long length of line is due to the output bias tee and the long thin length of line is due to the input matching network. The design passes all rules in the AWRDE 12 default design rule check process.

Figure 10 shows the progression of amplifier output power and power-added efficiency across the stages of design. The final design of the amplifier in Figure 9 has an output power of 37.54 dBm and a power-added efficiency of 52.98%. As shown in Fig. 14, the output power is largely located at the fundamental frequency of operation. The power dissipated is defined as

$$P_D = P_{DC} + P_{RF,IN} - P_{RF,OUT}$$

where P_D is the total internal dissipated power. As seen in Figure 13, there is 5mW of power dissipated at an input power of 22dBm.

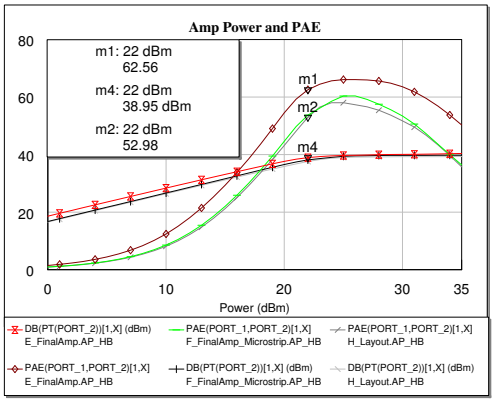

Fig. 10. Marker 1 indicates the performance of the amplifier with ideal lumped elements and transmission lines. The green line at marker 2 is the stage of design seen in Figure 8 and the gray line is final layout seen in Figure 9. PAE drops by 10 points after transitioning from ideal elements to microstrip, but the output power is only affected by about 1 dB.

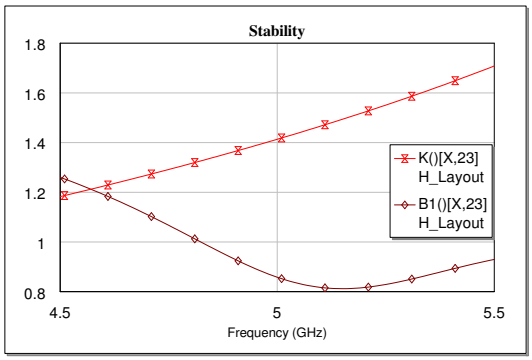

Fig. 11. The small-signal analysis shows that the amplifier is unconditionally stable across 20% bandwidth.

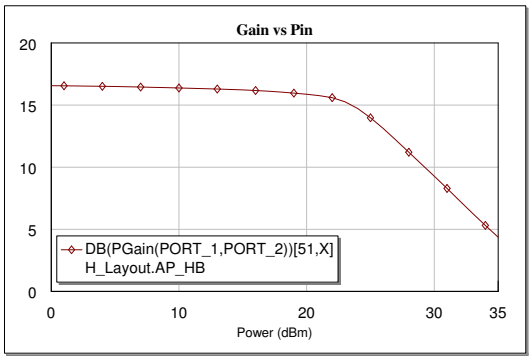

Fig. 12. At 22dBm of input power there is 15.6 dB of gain.

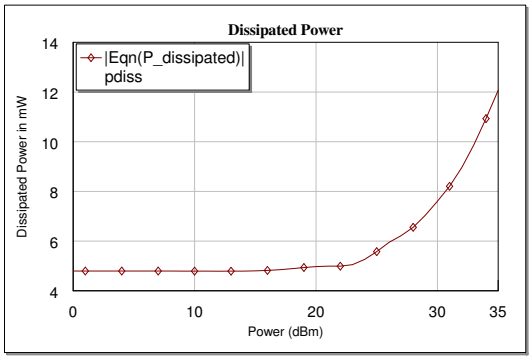

Fig. 13. Power dissipation is 4.99 mW at 22dBm of input power and begins to rise with input power after this point.

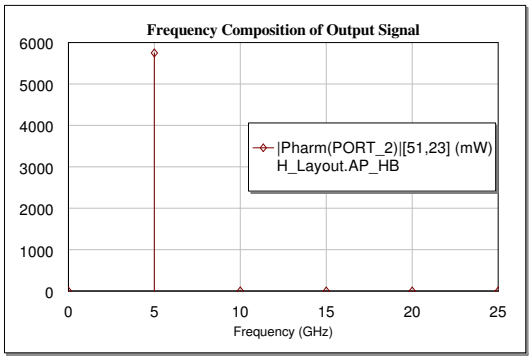

Fig. 14. 5.778 W is present at 5GHz and 3.183 mW in comparison at 10GHz.

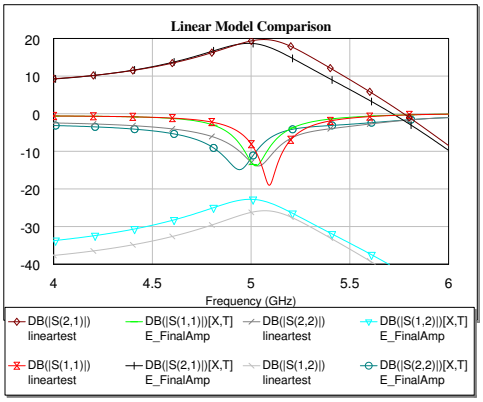

Fig. 15. The linear model can be used instead of the nonlinear model for small-signal analysis assuming that the region of operation is not saturation.

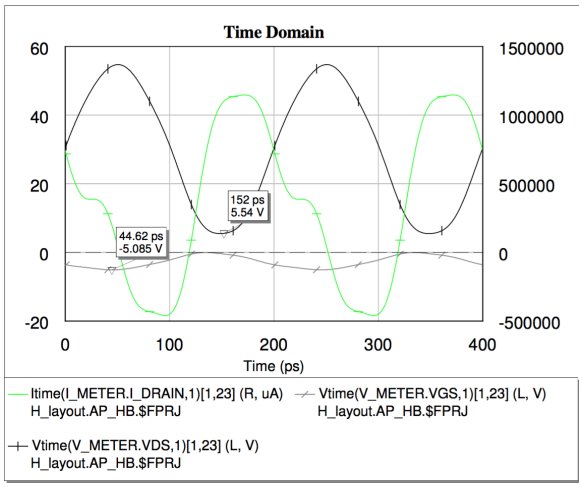

Fig. 16. The drain and gate voltage are expected values on an IV curve, but the drain current does not behave as expected.

VII. Discussion and Conclusion

Figure 15 is an investigation after the completed design of the suggestion in [1] that "it is sometimes advantageous to use linear models and load pull data to represent the transistor cells" to speed up the design process and allow faster investigation of various parameters. The small-signal behavior of the non-ideal amplifier design stays the same for an input power sweep of 0 to 35dBm. Although the points of resonance for S_{11} and S_{22} are shifted by 100 MHz or so between the two models, the general shape and magnitude of values are similar enough that the linear model indeed should be able to be used to represent the transistor cells.

Further investigation should be made into understanding the power and voltage handling of elements such as the capacitors and the spiral inductor air-bridge. [2] warns against use of high density capacitors due to poor voltage handling, so the effect of this on design has not yet been tested.

Another interesting result that appeared can be seen in Fig. 16. The gate voltage swings from 0 to -5V; at -5V, the transistor should enter pinchoff and have very minimal drain current. Instead, the drain current is negative for approximately

80 picoseconds of each cycle, implying that the transistor is consuming current. The author is hesitant to say that the simulation is wrong and yet extremely confused.

REFERENCES

[1] Campbell, C. 2013. Microwave Monolithic Power Amplifier Design. Wiley Encyclopedia of Electrical and Electronics Engineering. 000.
[2] M. Litchfield, 'MMIC Design Basics and Example', University of Colorado, Boulder, 2016.