Independent Study Final Report : GaAs MMIC Amplifier Design

Allison Duh

Supervised by Dr. Zoya Popović
Spring 2018

Contents

List of Figures

List of Tables

Chapter 1

Qorvo GaAs MMIC Process

The GaAs process used in this study was QP25GEN2, a process derived from TQP25. It has two primary metal layer interconnects which will be referred to in this work as BLMET and Me2, a top layer for capacitors, as well as two resistive layers named 'high-value resistor' and nickel chromium. Refer to Figure 1-1 for a diagram of the substrate file used in Keysight ADS.

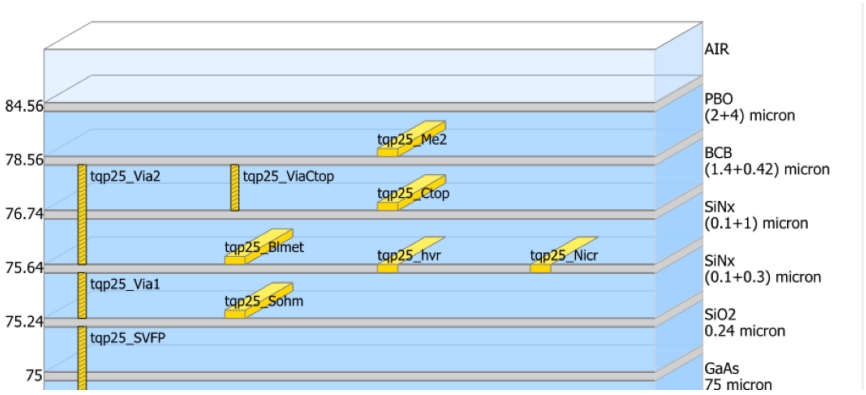


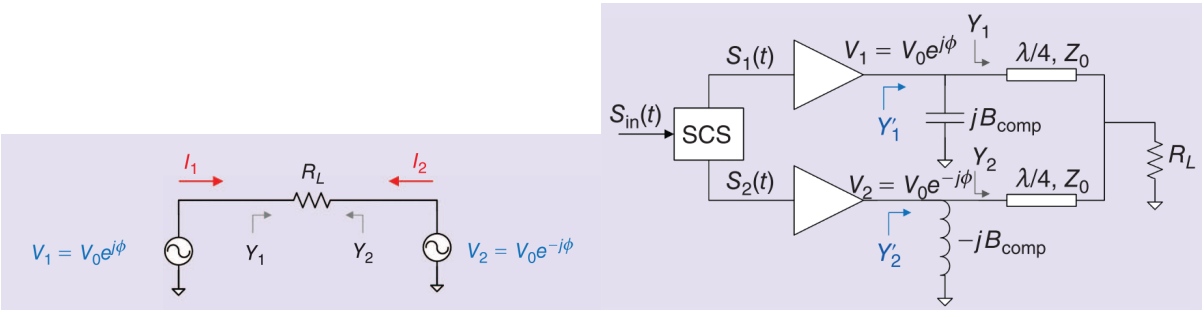
Figure 1-1: The QP25GEN2 process has a GaAs substrate of 75 microns, two metals, two resistive layers and a capacitive layer.

Chapter 2

Design Process

2.1 Design Topology Introduction

The load reconfigurable amplifier concept arises from the practice of active load-modulation commonly found in outphasing amplifiers [1]. Active load modulation requires at least two active devices which are able to "see" each other, *i.e.*, the devices directly load each other. Outphasing amplifiers operate the devices near saturation for higher efficiency, which also permits the active devices to be simplified into near-ideal voltage sources. The goal of outphasing amplification is to provide high output power at various levels of power back-off for data with high peak to average ratios.



(a) Bias tee scatter parameters.

(b) Bias tee input impedances presented at the fundamental frequency, and the second and third harmonics.

Figure 2-1: The outphasing topology as explained in [1]

The fundamental concept is illustrated in Fig. 2-1a. The quarter-wavelength lines in Fig.2-1b serve the purpose of transforming the differential output load to a single-ended load. As shown by the derivation in [1], the real load seen by each branch amplifier/voltage source varies from R/2 to infinity with outphasing angle. The imaginary component varies from 0 to 1/R, which can be normalized to a range of 0 to 1, and these conditions correspond to maximum outpower at $P_{out,norm} = 0$ and 1. To enable to amplifier to operate more efficiently within a smaller dynamic output power range, elements presenting complementary susceptances (plus minus G) can be added to each branch to move the points of intersection (Pout,norm) of the two reactive load curves (B=0) towards each other. If the susceptance values are not complementary, the intersection of the curves are moved off of the B=0 axis of the Smith Chart and shifted to intersect at a non-zero constant B plane.

Instead of applying it towards variable output power and transforming a fifty ohm load to various impedances that cause variable power output from the transistors, the LoRe amplifier uses active load-modulation essentially in reverse; a wide range of possible load values, with a range of real and imaginary components, are compressed so that the resulting range of impedances is smaller and are more favorable for higher effiency operation of the active devices. This concept has previously been successfully illustrated in [2]; the inductive and capacitive tuning values for each load-case was replaced and soldered by hand. Th ultimate aim of this project is to produce an amplifier that can match to a load that varies across a load centered at (-0.4,0) on a 50-Ω Smith Chart (20 Ohms) with a radius of 0.4, and using tuning elements that can be electronically controlled.

2.2 Bias Tee Design and Initial Load-Pull/Optimization

Using a manufacturer provided model of the six-finger $50 - um$ gate-width depletion-mode FET device, the following variables were optimized: drain bias, input power, gate resistor, fundamental source impedance, and fundamental, 2nd, and 3rd harmonic load impedances. The goal was a PAE of at least 45% at 10 GHz, with a gate resistor value of 7 Ohms. The resulting gate bias was -0.25 V and a drain bias of 5V for a quiescent bias of 59.7

mA. The results were double-checked with simulated load-pull, resulting in the following parameters:

	Fundamental	Second Harm.	Third Harm.
Source	$0.76\angle 127.8$	–	–
Load	$0.55\angle 75$	$0.9\angle 47$	$0.9\angle -22.3$

Table 2.1: Load-pull values found by optimizer

A bias tee was designed that also incorporated the second and third harmonic terminations. The schematic is shown in Figure 2-2, and the ultimate EM layout in Figure 3-1. The scattering parameters are shown in Figure 2-3. This subcircuit was run through DRC and cleaned before proceeding with the subsequent output matching network design.

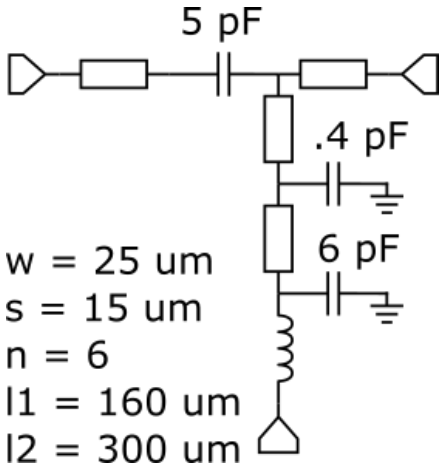
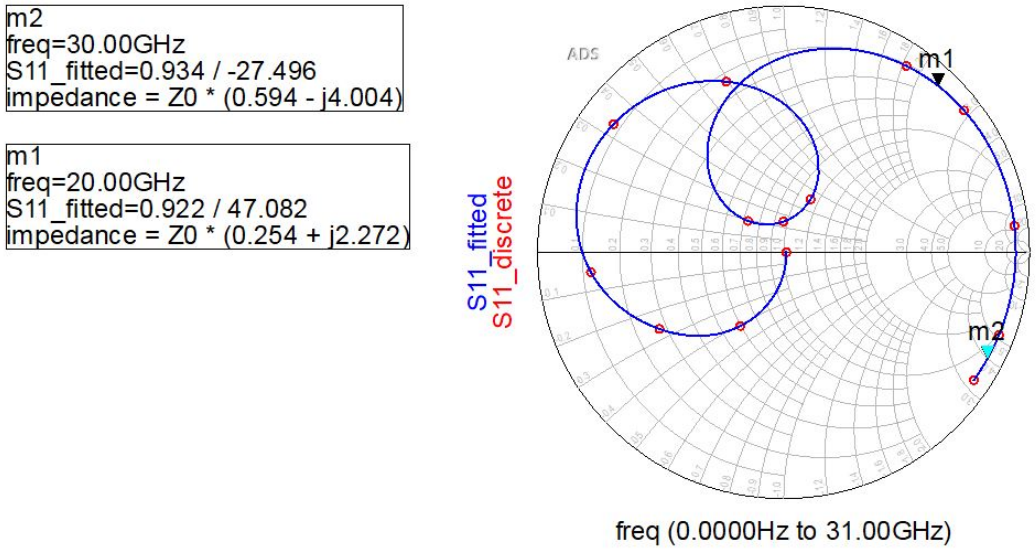
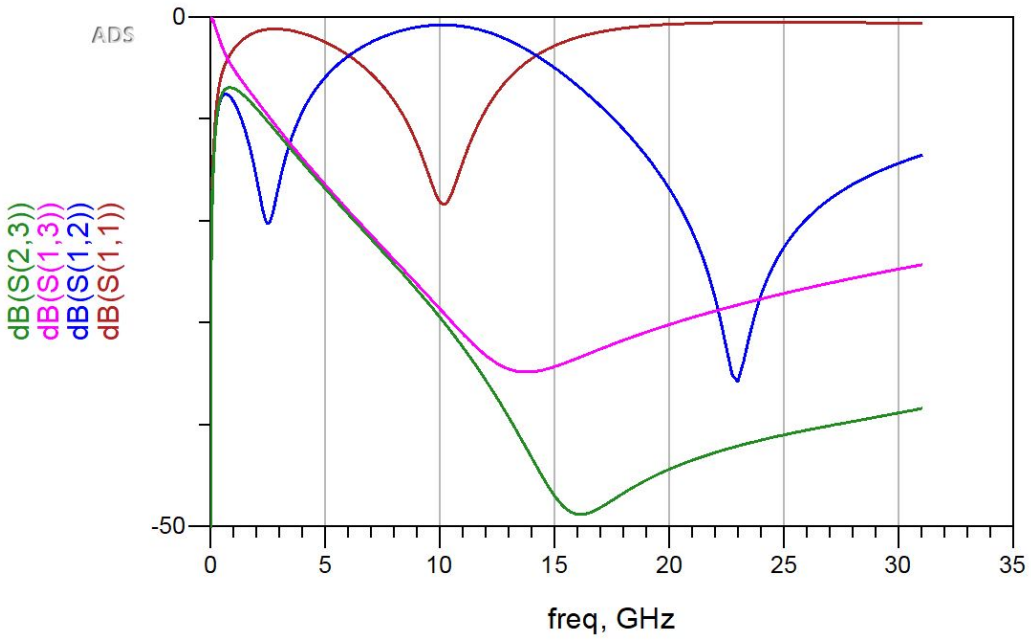


Figure 2-2: The second and third harmonic terminations are incorporated into the bias line. The inductor simply needs to be a high impedance to reflect any RF power that is not shunted to ground through the previous shunt capacitors.

The load-pull was taken at the output of the package drain. A block diagram of the entire output matching network is shown in Figure 2-4; as previously discussed, it borrows from the outphasing output matching network layout in that it has compensating reactive elements on each branch as well as quarter-wavelength lines on either side of a 50 Ohm load for impedance transformation. However, due to the size constraint imposed by the die, it is intended that the quarter-wavelength lines will be shortened where possible, and the compensating reactive elements will not be inverses of each other, as the bisecting line of the



(a) Bias tee input impedances presented at the fundamental frequency, and the second and third harmonics.



(b) Bias tee scatter parameters.

Figure 2-3: Bias tee input impedance and scattering parameters.

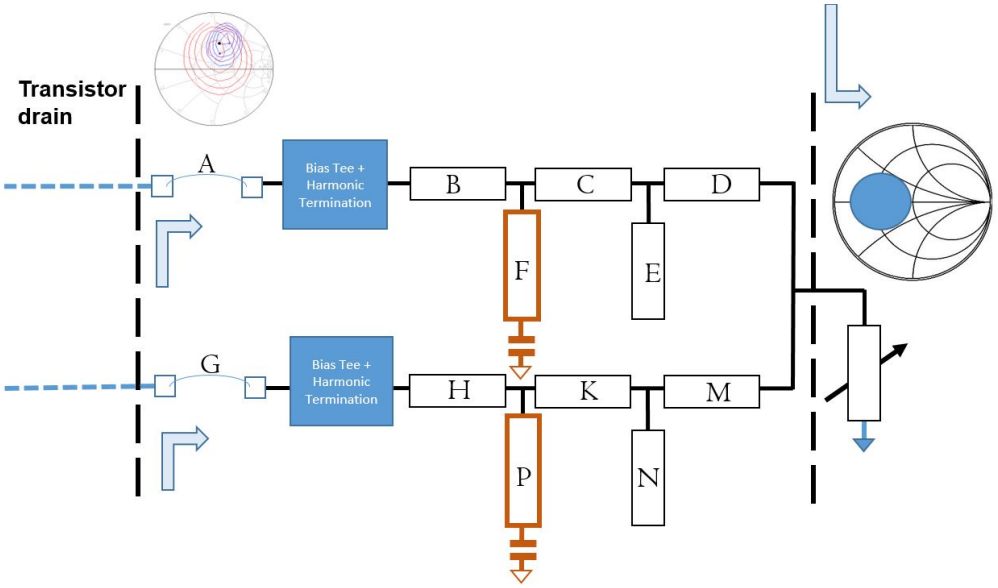


Figure 2-4: A block diagram of the output matching network along with the range of varying load values. The first plane of reference is at the drain terminals of the transistors. A bond wire bridges two RF pads at each drain output; before this bridge is made the output matching network can be probed separately as a static network.

outphasing curves is not intended to follow the $\beta = 0$ axis. With the bias tee and harmonic terminations already designed, the plane of reference for the desired impedance presented by the rest of the OMN can be shifted. The new target value for the load impedance is $16.6 + 33.5j$ and $12 + 28j$ for the source impedance.

Due to the complex nonlinear nature of the 3-port network, the values of the network topology are to be found through an optimization search. The variable length of the stubs is achieved through switched shunt capacitors, with the top metal plate of the capacitor incorporated into the length of the line, and the bottom metal plate connected to a single-pole, single-throw (SPST) switch to ground. The aim is for one line with three shunt capacitor-switch pairs to be able to act as three different lengths of line, depending on which switch to ground is turned on. This minimizes the amount of space taken up by the tunable lines.

2.3 Optimization Parameters

The optimization was run on four instances of the same amplifier large-signal simulation, in which each instance had a different swept load as shown in Figure 2-5. The length of stubs F and P varied for each load case are passed into each subcircuit for variation. Tables 2.2 and 2.3 show the values found for these goals, and Fig. 2-6 shows the PAE of 35-45% that is achieved in simulation with these switch cases.

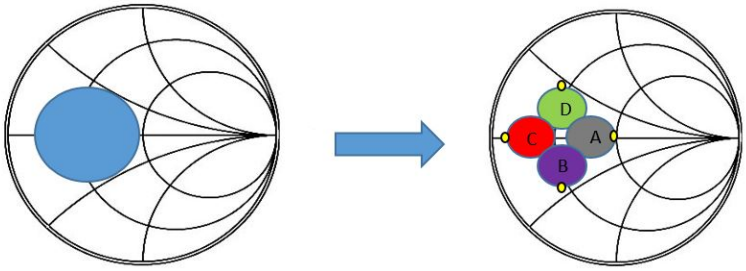


Figure 2-5: To create a load centered around 20 Ohms that varies from 10-50 ohms, four smaller load-cases are created. The amplifier's switch states are optimized to these load-cases.

	Z0	EL @ 10 GHz
B	41.46	55.47
C	41.46	12.88
D	41.46	41.07
E	51.7	56.23
F	56.5	varies
H	40	17.43
K	40	1
M	40	1
N	51.7	25.26
P	71.3	varies

Table 2.2: Result of optimization for lines shown in Fig. 2-4. Bondwires A and G are 300 microns in length with a diameter of 25 microns.

	EL of F	EL of P	Phase shift
Red /A	30.1	36.4	34.2
Blue / B	32.7	20.5	94.17
Green / C	66.45	67.9	45.54
Orange / D	40.95	70	14.95

Table 2.3: Result of optimization of stub lengths for various load areas.

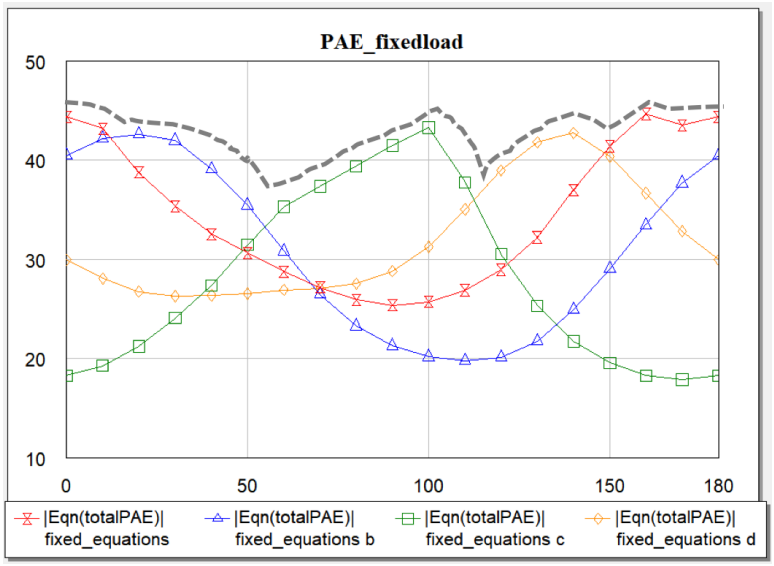


Figure 2-6: This configuration of switched stubs achieves a PAE of 35-45% across the total area indicated in Fig. 2-5. The x-axis label of 0-180 indicates the circumference of the potential load area.

2.4 Switch Model

A typical SPST switch model has two states: off and on. In the off state, the behavior is dominated by the off-capacitance of the switch and off-resistance is large relative to the system impedance and can thus be disregarded. In the on state, the resistance of the switch is called the on-resistance. A figure of merit for switches is derived from this:

$$FOM = \frac{1}{2\pi R_{on} C_{off}} \tag{2.1}$$

The SPST switch used in this design was one single-channel depletion-mode FET from the Qorvo process, with gate width of 490 microns to reduce R_{on}. The values seen in Tables 2.2 and 2.3 are found with an optimization that assumes the transistor has an infinite off-capacitance and can thus be seen as an open circuit when it is not connected. In reality, the SPST transistor has an R_{on} of 3.44 Ohm and a C_{off} value of 0.12 pF. As a result, whereas in the first iteration, each switch-state was simply represented by a stub of different length, the optimizer was re-run with cascaded stub lengths $F_{1,2,3}$ and $P_{1,2,3}$ altogether with each of the switches accordingly represented by an off-capacitance or on-resistance depending on its state for the load-case in question.

Ultimately, to save space on the die, the shunt capacitor is integrated in with the line so that the top plate of the capacitor is part of the stub metal, and the lower plate of the capacitor is connected to the drain of the FET switch. The capacitor is thus only connected to ground when the switch is closed. The shunt capacitances are all 5 pF. The topology of these cascaded stub-lengths and integrated shunt capacitors together are much more complex than the three disparate stub lengths found in the first iteration of optimization, and thus the lengths of the stubs will vary from the original values.

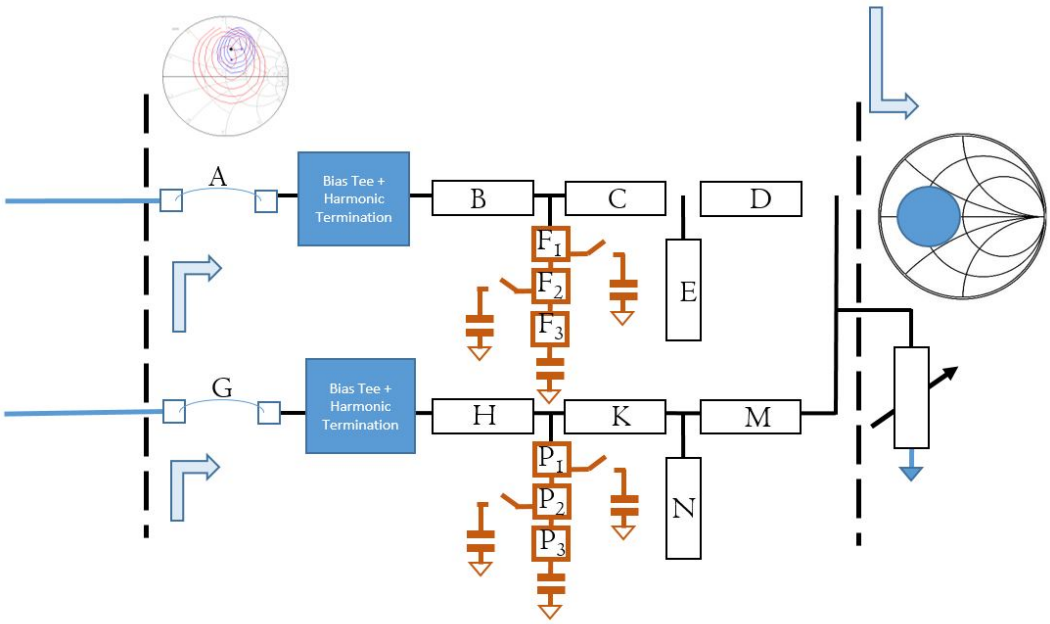


Figure 2-7: Block diagram updated with tunable stub design. The lengths F_n and P_n are connected or disconnected to RF ground depending on switch configuration to create a variable length stub.

Chapter 3

MMIC Layout

3.1 Layout

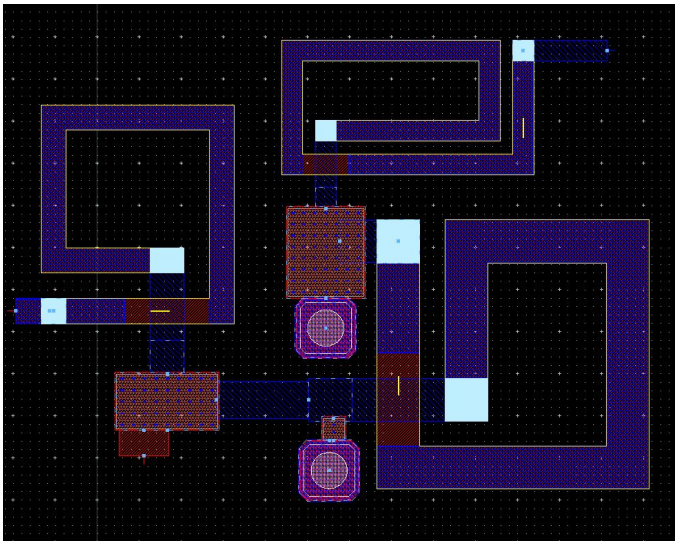


Figure 3-1: EM layout of the bias tee and harmonic termination subcircuit.

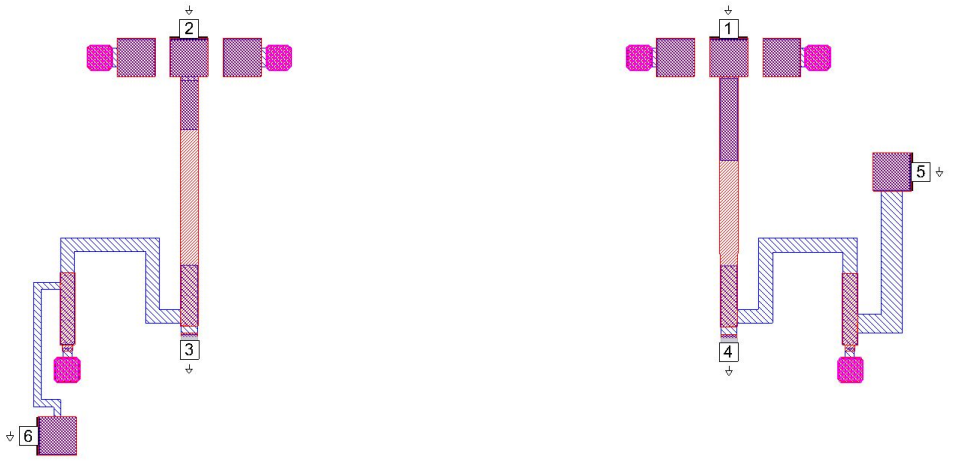


Figure 3-2: The input matching and bias network of the two transistors.

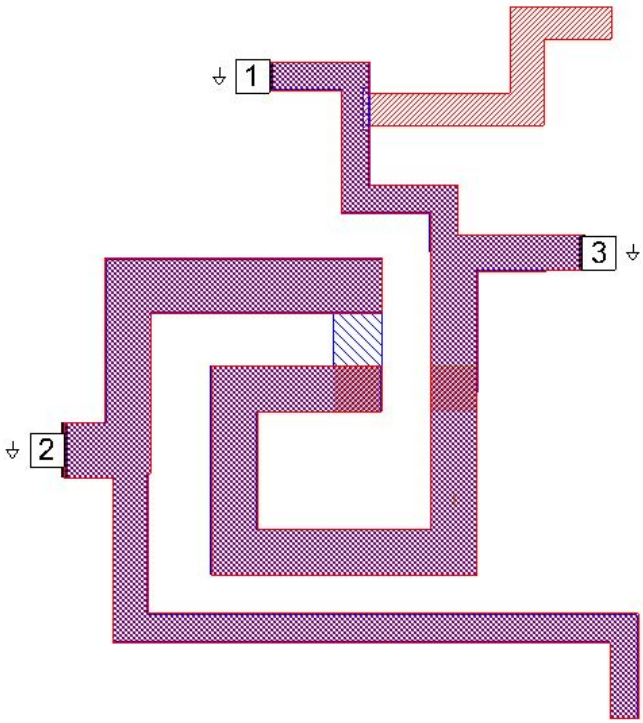


Figure 3-3: This is the combination of lines C, D, E and K, M, N, which are static lines and do not have switches in them.

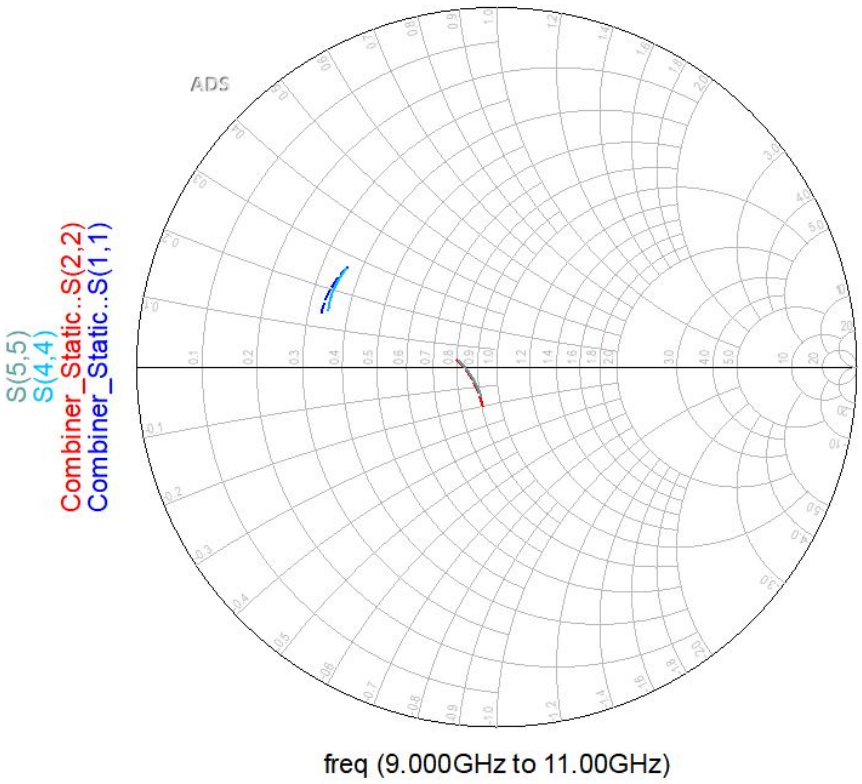


Figure 3-4: The input impedance presented by the EM layout (solid lines) from 9 to 11 GHz closely matches that of the intended schematic design ('Combiner_Static,' dashed).

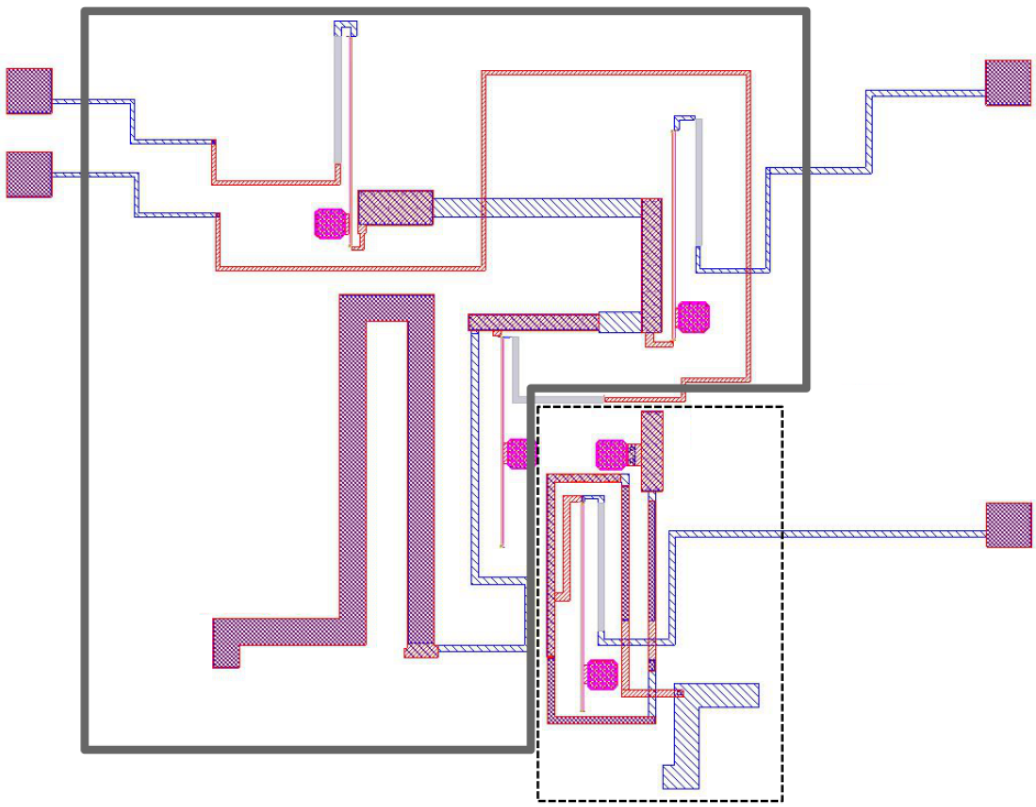


Figure 3-5: The two tuning stubs of the output matching network. The upper branch of Figure 2-7 is shown with a dashed border, while the lower branch is shown with a solid border.

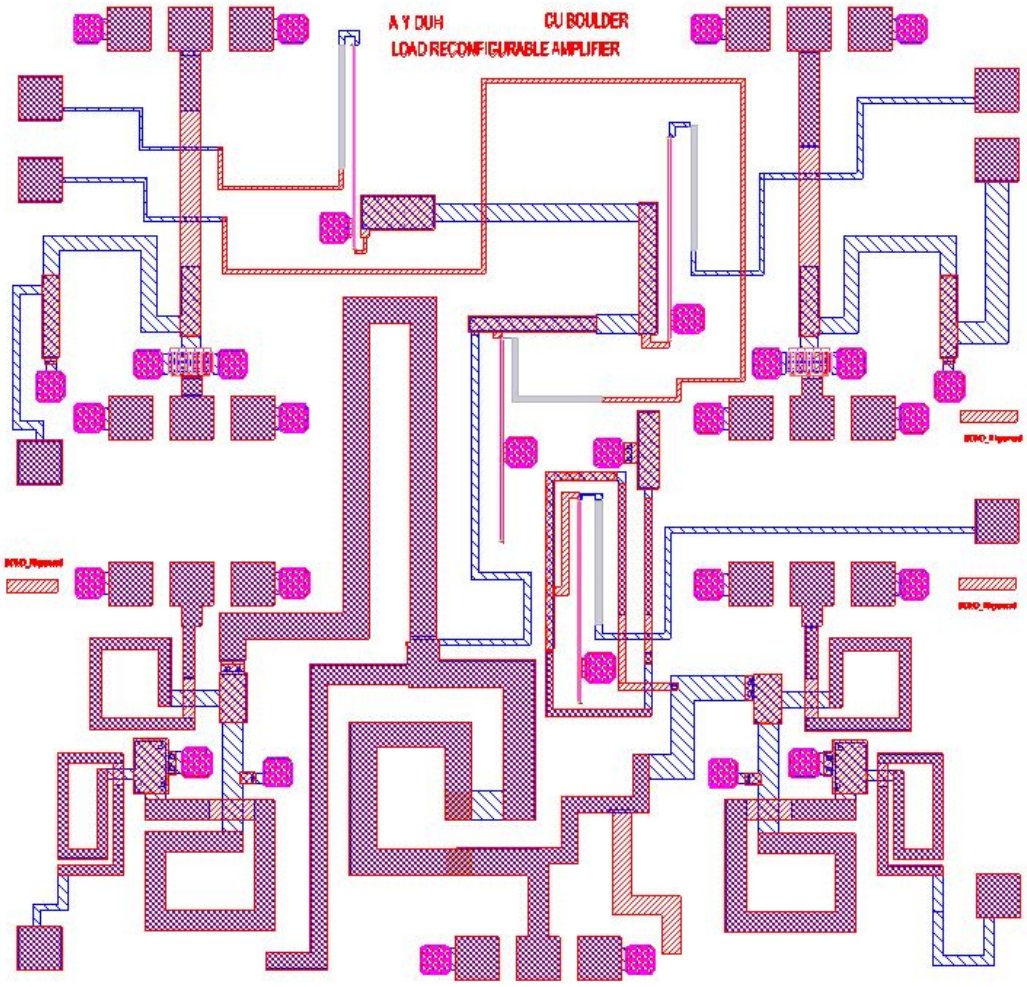


Figure 3-6: The layout of the entire MMIC, which fits within a 2.6 x 2.6 die space.

Chapter 4

MMIC Simulation Results

4.1 Mesh

The EM simulations are completed in AWR AXIEM. Care must be taken in creating the mesh, as the narrow lines connecting to the drains and gates can mesh incorrectly and fail to form a conducting connection.

The settings of the AXIEM mesh as differ from default are as follows:

- Uncheck 'No Edge Mesh for Thick Metal'
- Mesh Units: Absolute
- Min edge length: 5.1 um
- Max aspect ratio: 3

These values were found through trial-and-error until the High Aspect Ratio errors thrown by AWR were resolved.

4.2 Switch Behavior

The design has two switched variable stubs, one which has one switch and the other which has three switches. The input impedances presented by each switch are shown in Figs.

4-2 and 4-1, and are simulated with s2p files extracted from the off and on states of the Qorvo-provided nonlinear model, with 50 Ω ports.

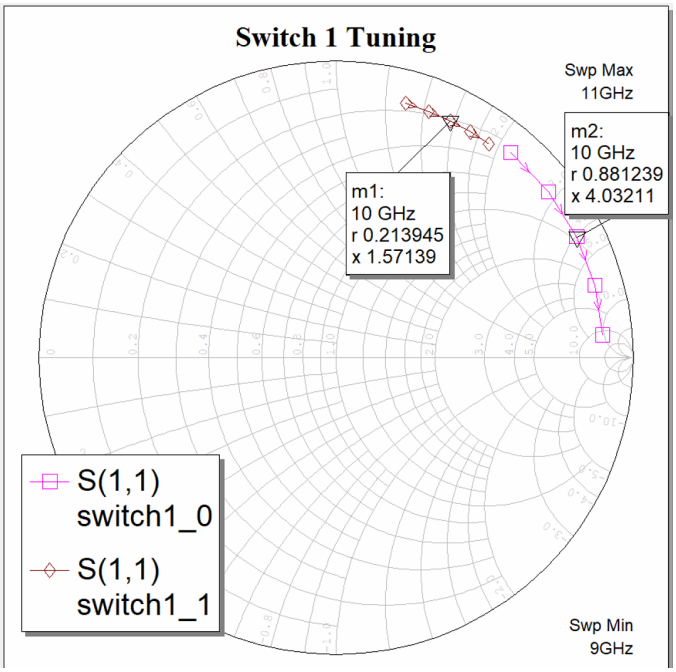


Figure 4-1: EM layout of the bias tee and harmonic termination subcircuit.

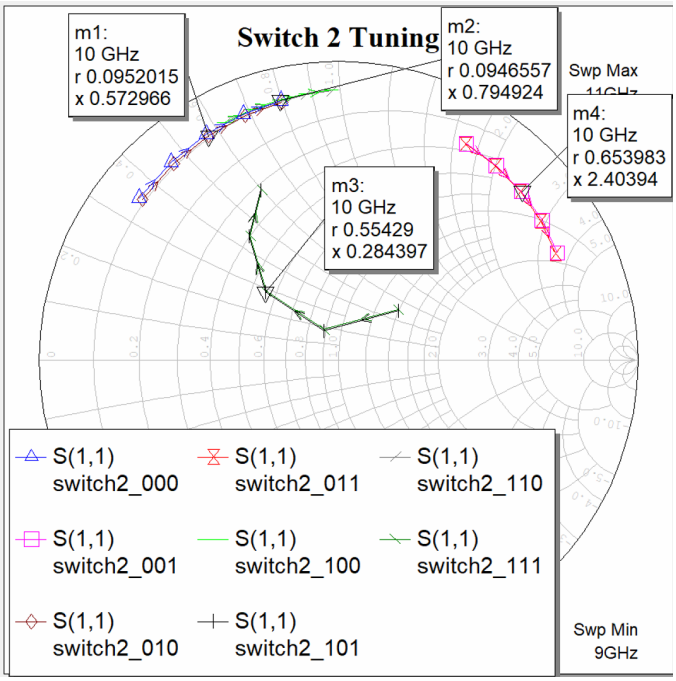


Figure 4-2: EM layout of the bias tee and harmonic termination subcircuit.

4.3 Output Matching Network Tuning Capabilities

The port impedances are defined as 21-j*20, which is the S_{22} impedance of the transistor when biased at the gate and drain with the 7 Ohm gate resistor. While the output impedance of the transistor will change with output power ($\Delta|\Gamma| = 0.1$ from $P_{in} = 11$ to $P_{in} = 14$), one value will be used as a general approximation for the calculation of Γ_{in}.

The output matching network is expected to present varying input impedances depending on input power level and relative input phase. Only one phase shift needs to be swept because it is the relative phase shift between the two inputs that matters; *e.g.* if phase 1 is shifted by 0 degrees and phase 2 by 60, the results will be the same as if phase 1 is shifted by 300 degrees and phase 2 by 0 degrees.

A schematic is set up in which the relative input phase is swept, as well as the real and imaginary components of the load attached to the output of the OMN. Fig. 4-3 shows the variation of the input impedances (defined as shown in 4-4 probed voltages and currents V/I), where the characteristic impedance of the smith chart is $Z_0 = 7 - 66j$, indicating that the impedance at the middle of the Smith chart denormalizes to 7 + 66j.

4.4 Amplifier Performance

Figures 4-5 to 4-9 show the PAE measured by the amplifier when presented by a broad sweep in loads; the x-axis of 1 to 171 indicates the rotation of a load around a 50-Ohm system to create a constant VSWR circle (e.g. to create a VSWR of 0.96, a 1 Ω load is rotated by a line varying in length from 1 to 171 degrees at 10 GHz). The switching states can be found in the legend of each trace; for example, xxx_0_110 indicates that the single switch in one tuning stub is off, and the first two switches closest to the RF path of the second stuning stub are on.

The poor PAE performance is likely due to reflective mismatch. The initial target load impedance intended in design is 16.6 + 33.5j. As shown in the previous section, the output matching network approximately matches to present 7 + 66j, and is thus much more re-

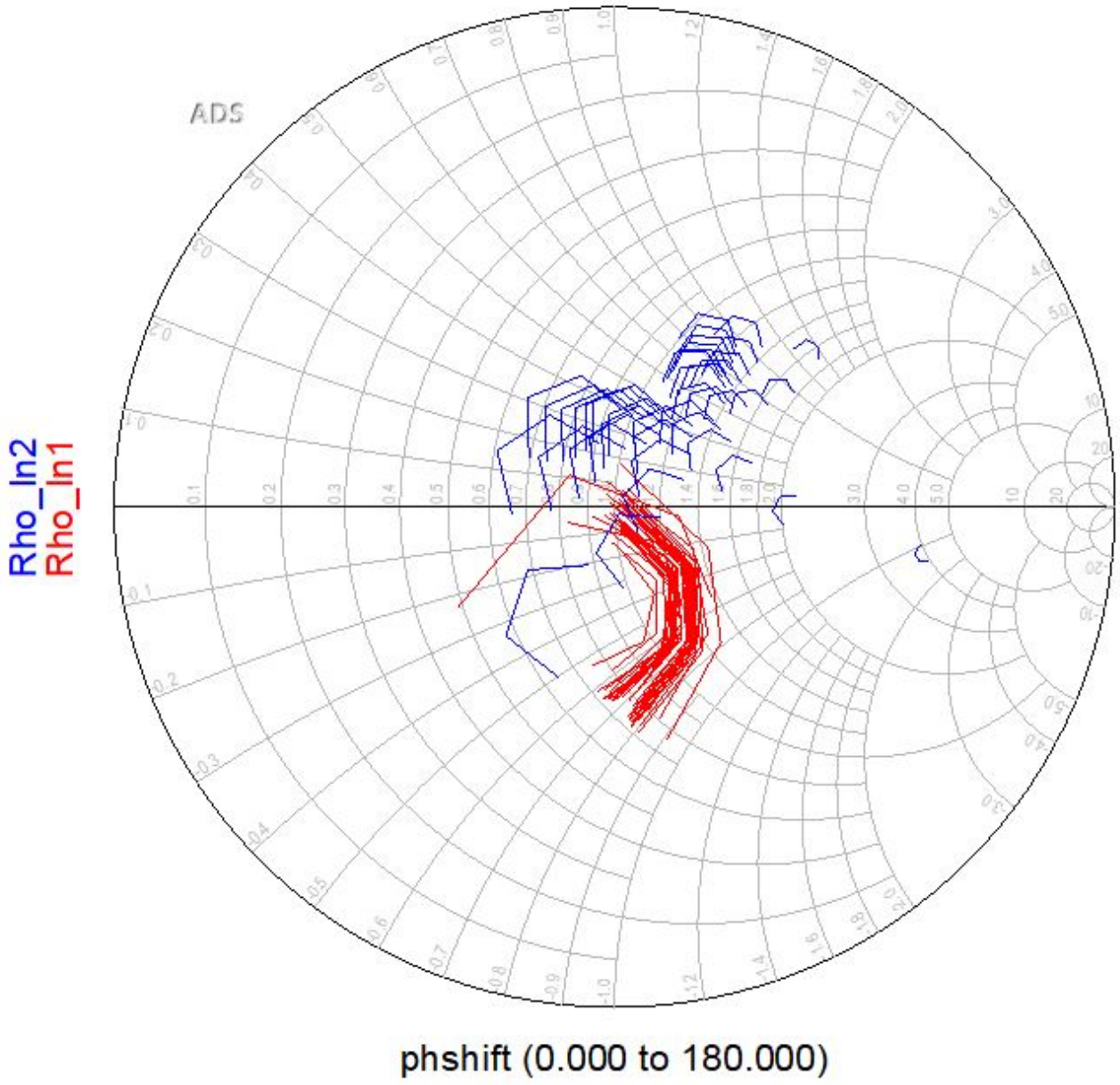


Figure 4-3: Reflection coefficients presented at the inputs to the output matching network; $Z_0 = 7 - 66j$.

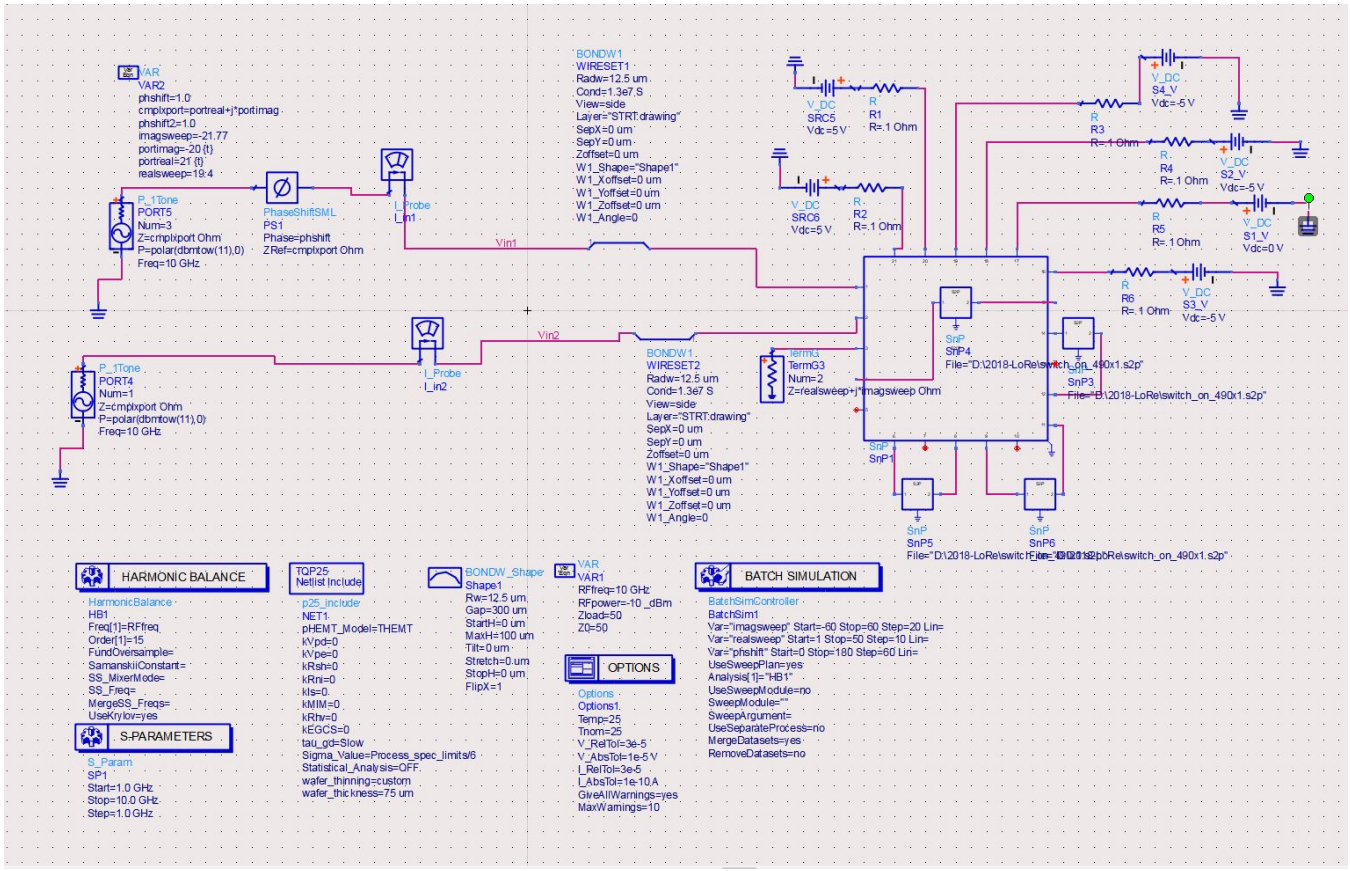
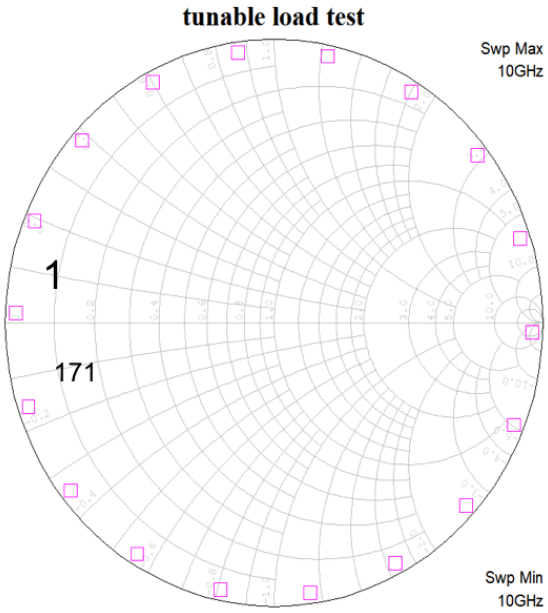
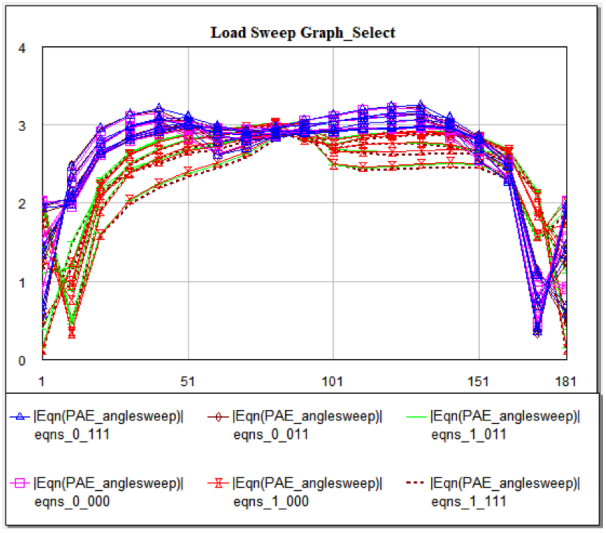


Figure 4-4: The schematic used to measure the impedance presented by the output matching network.

flective at the inputs. This leads to a large amount of reflection from impedance mismatch. Dissipative loss could also be a contributing factor, although the conventional definition of insertion loss cannot be applied in this instance due to the three-port nature of the network.

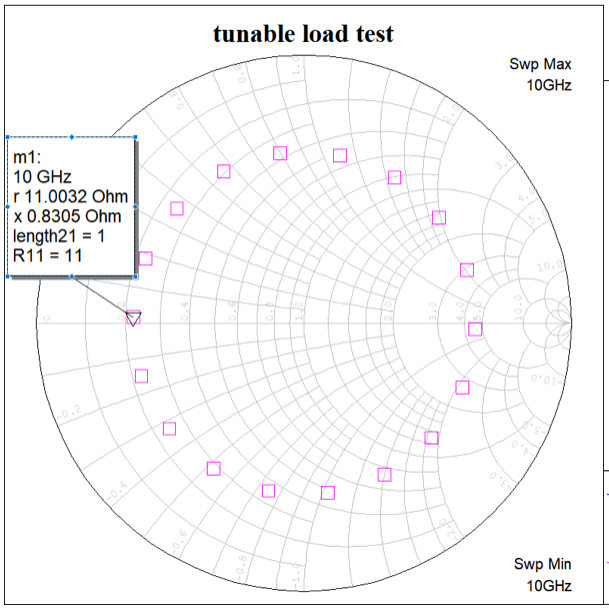


(a) The load presented to the amplifier.

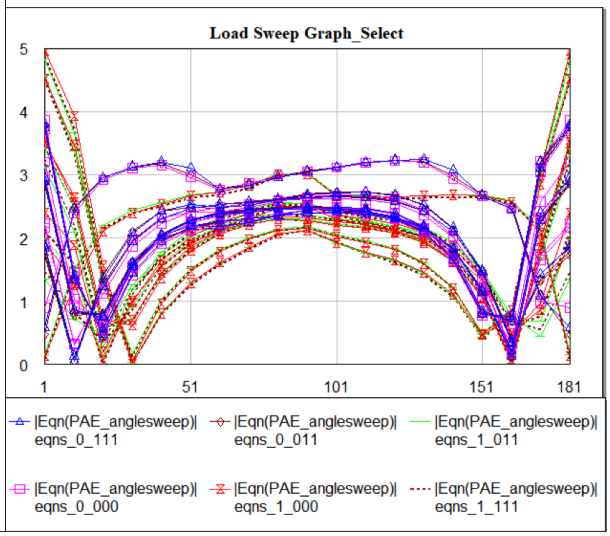


(b) PAE as it varies around sweep angle for various switch loading conditions.

Figure 4-5: Gamma = 0.96 with angle swept from 1 to 171

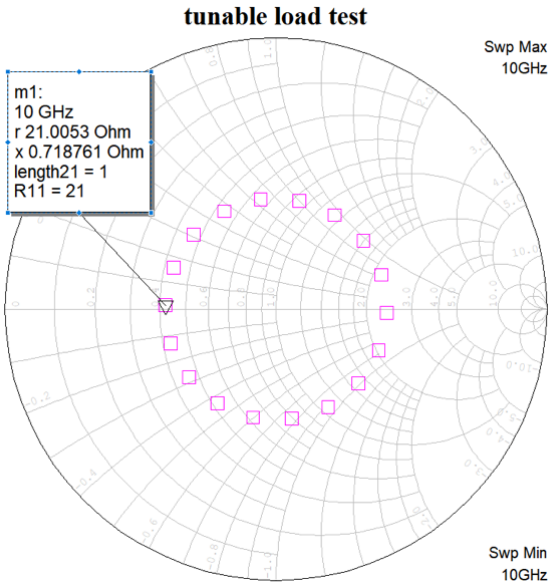


(a) The load presented to the amplifier.

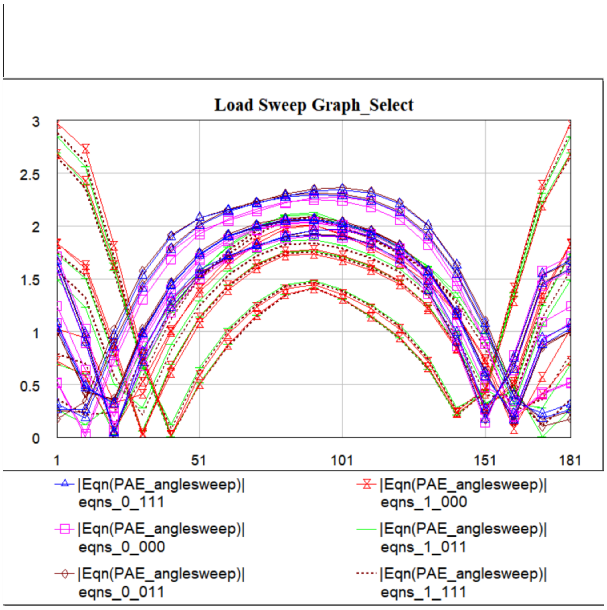


(b) PAE as it varies around sweep angle for various switch loading conditions.

Figure 4-6: Gamma = 0.64 with angle swept from 1 to 171

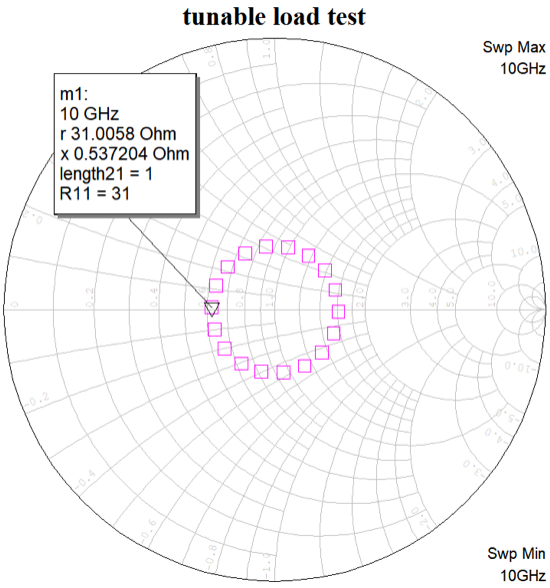


(a) The load presented to the amplifier.

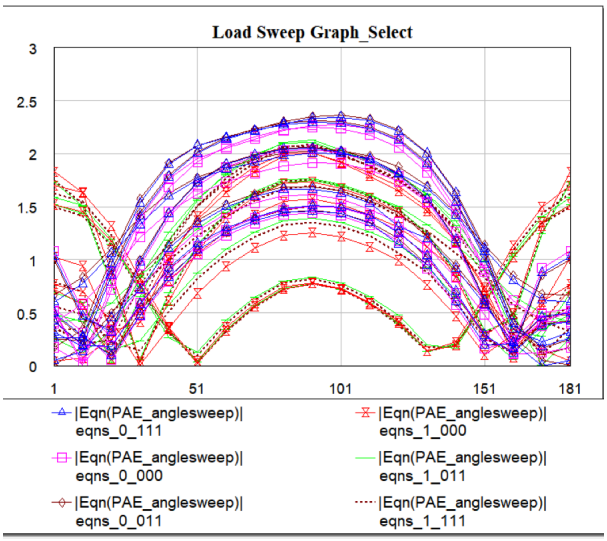


(b) PAE as it varies around sweep angle for various switch loading conditions.

Figure 4-7: Gamma = 0.41 with angle swept from 1 to 171

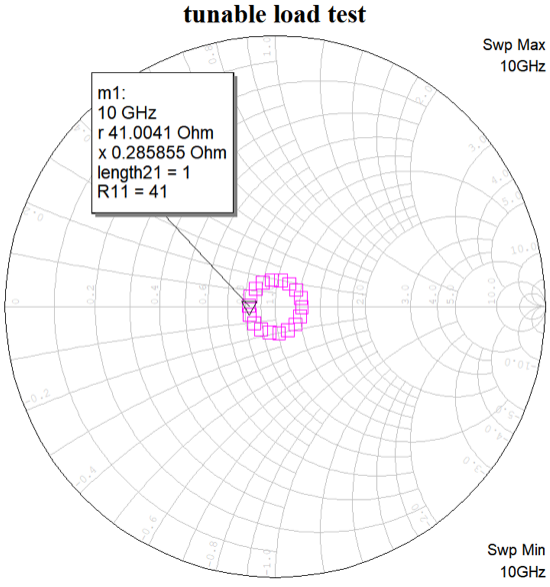


(a) The load presented to the amplifier.

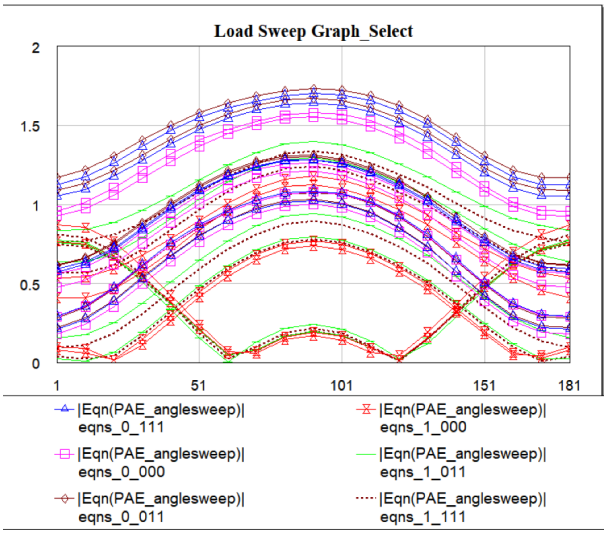


(b) PAE as it varies around sweep angle for various switch loading conditions.

Figure 4-8: Gamma = 0.23 with angle swept from 1 to 171



(a) The load presented to the amplifier.



(b) PAE as it varies around sweep angle for various switch loading conditions.

Figure 4-9: Gamma = 0.1 with angle swept from 1 to 171

Chapter 5

Conclusion

This concludes the exercise in MMIC study with a load-reconfigurable power amplifier.

The best performance by the 4 switches is 35-40% in the area where a simulated pre-matched loadpull claims 48%. There is a tradeoff between minimizing the number of switches and maximizing the area of the large variable load and its accompanying âĂIJborder." For future work, it may be more valuable to look into trying to improve over the pre-match condition at a higher PAE and a smaller area — e.g. increasing the area over which the PA can provide 60% efficiency rather than 48%. Future work must also include a quantity to indicate the amount of attenuating dissipative loss of the non-isolated three port network.

Bibliography

[1] Taylor Barton. Not Just a Phase: Outphasing Power Amplifiers. *IEEE Microwave Magazine*, 17(2):18–31, 2016.

[2] Cesar Sanchez-Perez, David Sardin, Michael Roberg, Jesus De Mingo, and Zoya Popovic. Tunable outphasing for power amplifier efficiency improvement under load mismatch. *IEEE MTT-S International Microwave Symposium Digest*, pages 31–33, 2012.