Design of a 5 GHz Harmonic Injection Power Amplifier for Linearity and Efficiency

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***Abstract*—This work documents the design of 5GHz power amplifier demonstrating 37.5dBm output power with a single tone input, and 33.71% PAE with a 5MHz spaced two-tone input signal and linearity of -13 dBc. Linearity and efficiency are achieved in simulation through active power injection at the second harmonic into the output of the main RF path transistor. The effect of injected power and phase on efficiency is investigated to determine the parameters of the passive terminating networks that connect the outputs of the main and injection path transistors.**

I. Introduction

In pursuing high efficiency and linearity in amplifier design, waveform shaping provides multiple avenues of design space that capitalize on active load-pull such as Doherty and outphasing amplifiers. [1] and [2] discuss the technique of harmonic injection, which begins with idealized waveforms and backs out the coefficients of the voltage and current equations that would yield the greatest efficiency. Ideal, class-B output waveforms with only two harmonics can be described with the following equations:

$$v(\theta) = V_{dc}[1 - x_1 sin\theta - x_2 cos(2\theta)] \quad (1)$$

and

$$i(\theta) = I_{max}[\frac{1}{\pi} + \frac{sin\theta}{2} + \sum_{n=2,4..}^{\infty} \frac{-2}{\pi[n^2-1]} cos(n\theta)] \quad (2)$$

As discussed in [2], coefficients of $x_1 = \sqrt{2}$ and $x_2 = 0.5$ allow some baseband ripple in exchange for an increased effect of the second harmonic amplitude on the overall efficiency. The maximum possible drain efficiency is 111% [1]. The necessary second harmonic load impedance to achieve this efficiency is $-R_f \cdot \frac{3\pi}{8\sqrt{2}}$, where $R_f = 2\sqrt{2}V_{dc}/I_{max}$, with the $\sqrt{2}$ factor being due to the increased swing in the fundamental voltage. A key goal of harmonic injection is to increase the fundamental voltage component without clipping the current.

Whereas passive terminating networks incur loss, limiting the magnitude of Γ that can be presented to the transistor, injecting power at the second harmonic enables reflection coefficients outside the Smith Chart to be synthesized. If more power is injected (a2 wave) than is produced by the main transistor (a1 wave) then it is possible to synthesize a Γ greater than 1.

II. Design and Simulation

The device used is the Qorvo TGF2952 7W GaN on SiC HEMT die. All simulation is completed using Keysight ADS, and microstrip is implemented on half-ounce 30-mil Rogers 4350B.

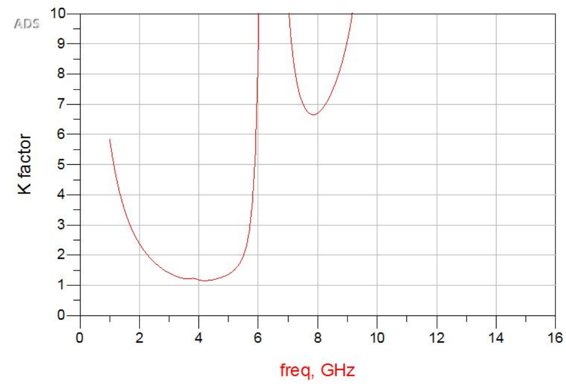

Fig. 1. The main path transistor is connected to port 1, the injection path is port 2 and the load is on port 3.

A. Stability

The device is stabilized with an RC parallel network comprised of a 13.3 Ω resistor (Vishay CRCW040213R3FKED) and a 22pF capacitor (ATC 600L220JT). With the transistor is biased in class B with an input matching network and stability network, it is desirable that the K factor be as close to 1 as possible at the fundamental frequency for maximum stable gain as shown in Figure 1. The input matching network presents an impedance of 2.8+2.52j, a result found through source pull with the stability network.

B. Main, Coupling, and Injecting Path Characteristics

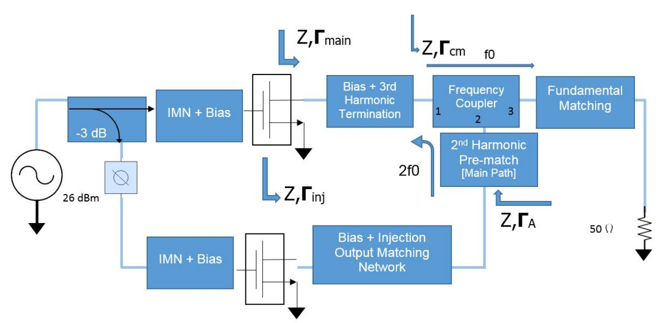

Fig. 2. The harmonic injection power amplifier with planes of reference.

The general layout of a harmonic injection amplifier can be seen in Figure 2. The injecting amplifier injects power at the second harmonic frequency into the drain terminal of the main transistor, which enables the synthesis of a variable second harmonic output impedance. Active power injection enables the impedance to reach $\Gamma > .9$, a region often unreachable by passive load terminations, and then to reach further beyond Γ=1. The component that interlinks the main and injecting paths must have the following qualities - it must admit the fundamental and second harmonic (S11), pass the second harmonic to port 2 (S21), and pass the fundamental to port 3 while simultaneously blocking the second harmonic (S31). The second harmonic must be admitted at port 2 (S22). This component has previously been called a diplexer, multiplexer, or simply combining network; as the former two are inaccurate descriptions and the latter imprecise, the network will be referred to in this work as a frequency coupler. The coupler is implemented with 50Ω line; as the output impedances of the amplifiers will most likely not be 50Ω, an impedance matching network must be implemented at the coupler output and at the output of the injection transistor.

C. Frequency Coupler Implementation

The frequency coupler (Figure 3) builds upon the basic structure presented in [1], with lengths tuned slightly to optimize for minimum loss at the fundamental frequency and maximum transmission between ports 1 and 2 of second harmonic power. It measures 585 by 407.5 mil and satisfies the scattering parameter requirements detailed in the previous section with an S21 of 0.552 at 10GHz (Figure 4).

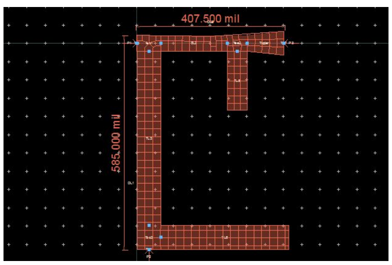

Fig. 3. The main path transistor is connected to port 1, the injection path is port 2 and the load is on port 3.

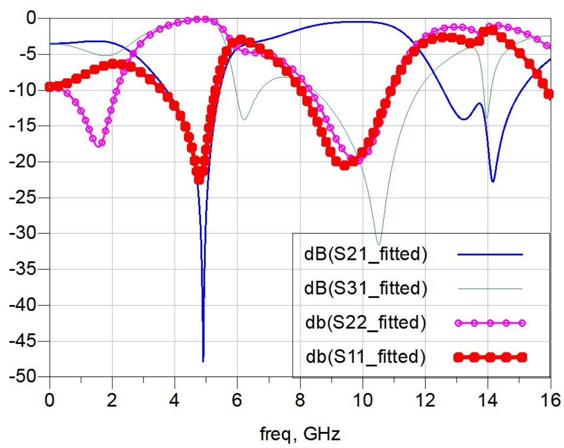

Fig. 4. Scattering parameters of the EM-simulated frequency coupler

D. Main Path Class B Amplifier

Load-pull is simulated at a gate bias of -3V and a drain bias of 32V. For harmonic generation and maximum PAE, ideally a load impedance is chosen at which there is approximately 3dB of compression and as high PAE as possible. However, a 23dBm input power limit is imposed on the main path, requiring a tradeoff between main path power and injection path power. A load of 51.35+50.23j is selected, with a gain compression of .81 dB and delivered load power of 37.791 with a PAE of 63.2%. Load-pull is iterated between the fundamental frequency, second, and third harmonics to find optimal load impedance and harmonic phase. These results are presented in Table I. Tthe third harmonic is terminated in a high-Gamma impedance with stubs at the output of the main transistor before the RF signal enters the frequency coupler. The frequency coupler enables the fundamental match and the 2nd harmonic pre-match to be tuned independently of each other. Load-pull with this impedance indicates that the device retains the same optimal phase for the second and third harmonic terminations.

TABLE I
IMPEDANCES FOR THE MAIN PATH AMPLIFIER

	Fund Gamma	2nd Harm Gamma	3rd Harm Gamma
Main Path	.435 $\angle 51$	1	1 $\angle 130$

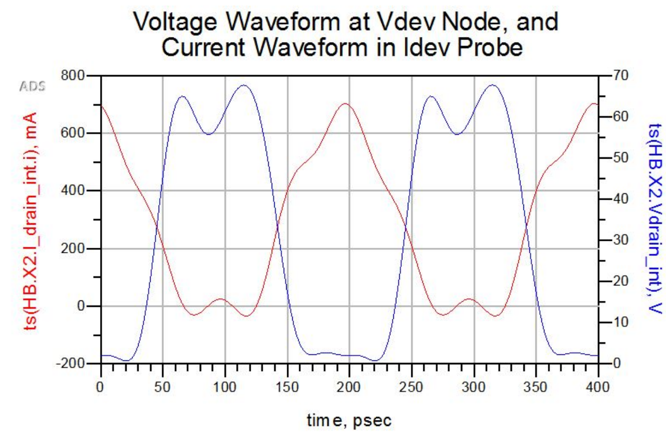

Fig. 5. Drain waveforms of a class B amplifier with the main path terminations presented in Table I

Figure 5 shows the waveforms at the intrinsic drain of the transistor when conjugate-matched for power at 23dBm input drive, with a load network that presents the terminations in Table I. This amplifier has a PAE of 64.3% and delivers output power of 37.84 dBm.

E. Second Harmonic Pre-match

With passive load-pull, pre-matching is performed when loss in the tuner threatens the ability of a passive load-tuner to present load with sufficiently high reflection to the circuit it is tuning. Prematching moves the constellation of presentable impedances to a chosen point closer to the desired load. With the second harmonic injection path, this constellation of presentable impedances is not limited to $\Gamma = 0.9$. Rather, assuming that one has infinite power to inject, the constellation is theoretically infinite in radius.

As infinite power is not available, it is of interest to characterize how the second harmonic pre-match can enable the injection of the least amount of power at the second harmonic to present an impedance to the main transistor that will shape the waveform and present the highest PAE. Also, it is expected that adjusting the second harmonic termination will not only change the optimal load impedance in some way, but also potentially affect where the optimum efficiency contours for the second harmonic lie.

The effect of the second harmonic pre-match is simulated by using the B amplifier and frequency coupler with the fundamental and third harmonic reflections previously described, and then various matching networks at port 2 of the coupler which are then connected to an ideal 50-ohm one tone source at 10GHz. The port 2 matching networks are designed so that when the ideal source is injected no power, a second harmonic short, 20 Ω, and 80 Ω are presented at the output of the main transistor package. The ideal source represents the output of the injection amplifier. Injected power and phase are then swept to see the range of PAE (Figure 6) with various prematch networks. The second harmonic short presents the highest PAE with the least injection power; however, the 20 ohm prematch surpasses this prematch condition with 30 dBm of injection power and can reach as high as 85 percent with 38 dBm of input power. Figure 7 shows the range of impedances presented to the main and injection transistors depending on the amount of injected power and phase; as expected, a negative impedance is presented to the main transistor at the second harmonic. In the case of the 20 ohm pre-match, a

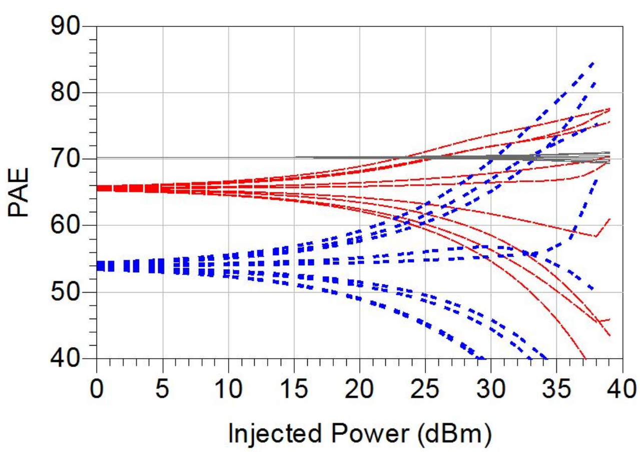

Fig. 6. The gray line is a high-gamma pre-match (1 ohm); the red is an 80 ohm pre-match and the blue is a 20 ohm pre-match.

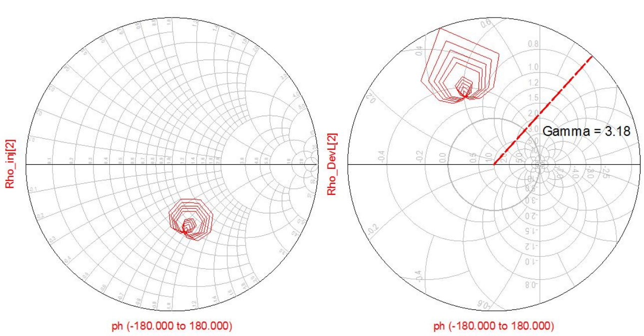

Fig. 7. The reflection coefficients presented at Γ_A (left) and Γ_{main} (right) when prematched to 20 ohms, with a full sweep of injection phase and injected power swept from 20 to 28 dBm.

phase of 60 presents the maximum PAE at any given injection

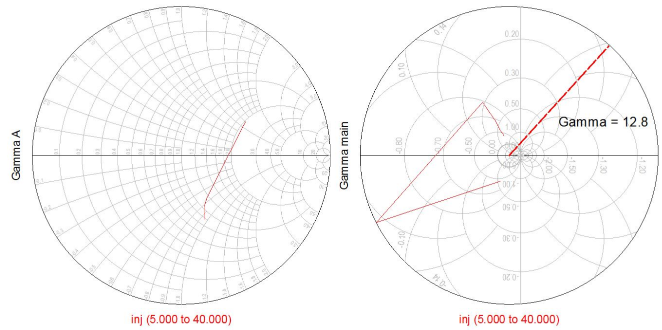

Fig. 8. Injected power is swept from 5 to 40 dBm with a fixed phase of 60 degrees to convey the trajectory of the reflection coefficient at Γ_A and Γ_{main} as defined in Fig. 2 ; realistically, 28 dBm is the upper limit of the injection path's output power at the second harmonic.

TABLE II
IMPEDANCES FOR INJECTION PATH AMPLIFIER

	Fund Gamma	2nd Harm Gamma	3rd Harm Gamma
Injection Path	.844 $\angle 72$	.7 $\angle 103.3$	.95 $\angle 100$

power. The reflection coefficient presented at Γ_A will be used in the design of the injection path. As expected, Fig 8 also suggests that the optimal second harmonic loads are no longer along the real axis as initial load-pull suggests.

F. Ideal Harmonic Injection Path Optimization

Load pull is performed at class B bias once more, but this time to find the load impedances at which output power at the second harmonic is maximized when driven with 23dBm at the fundamental frequency. The ideal maximum output power is 28.5 dBm, and the path efficiency is 9%, which is to be expected in using the transistor as a harmonic generator. Obtaining maximum output power which requires the fundamental termination and second harmonic load to present precise reflection coefficients presented in Table II. While the third harmonic can be terminated in a similar fashion as the main path amplifier, the fundamental load is relatively low in reflection magnitude, and thus by actively loading the second harmonic the optimal fundamental load presented will change simultaneously. This means that 28dBm of output power cannot be assured, but it will be used as a starting point for injection path designed.

G. Injection Path Implementation

Up to this point, the injection path in the harmonic injection amplifier has been represented by a 50 ohm ideal 10GHz source. To replace it while preserving equivalent behavior in the rest of the amplifier, the output network of the injection amplifier is designed not only to present harmonic and fundamental terminations and prematching, but also to transform the desired second harmonic pre-match (at the output of the injection transistor) to the reflection seen looking into the second harmonic matching network of the main amplifier. Using Fig. 8, Γ_A, which is the reflection seen at the junction between the second harmonic prematching network and the ideal source, is defined at 28dBm of injected power to be $0.356\angle-63.352$, which in a 50 ohm system is a load of 54.065 - 39.46j. This load is then transformed through the matching network to present the impedances seen in Table II. Now the paths can be combined together, beginning with a 26 dBm source that is split by a 3dB coupler into the two separate paths.

After implementing the output matching network of the injection path, the optimal phase shift must once again be found by sweeping a phase delay line at the coupled output of the input 3db coupler. Figure 9 shows a trade-off in third-order IMD and PAE with a two-tone measurement. A phase shift of 180 degrees at 5 GHz is chosen as a compromise between high PAE and low IMD3.

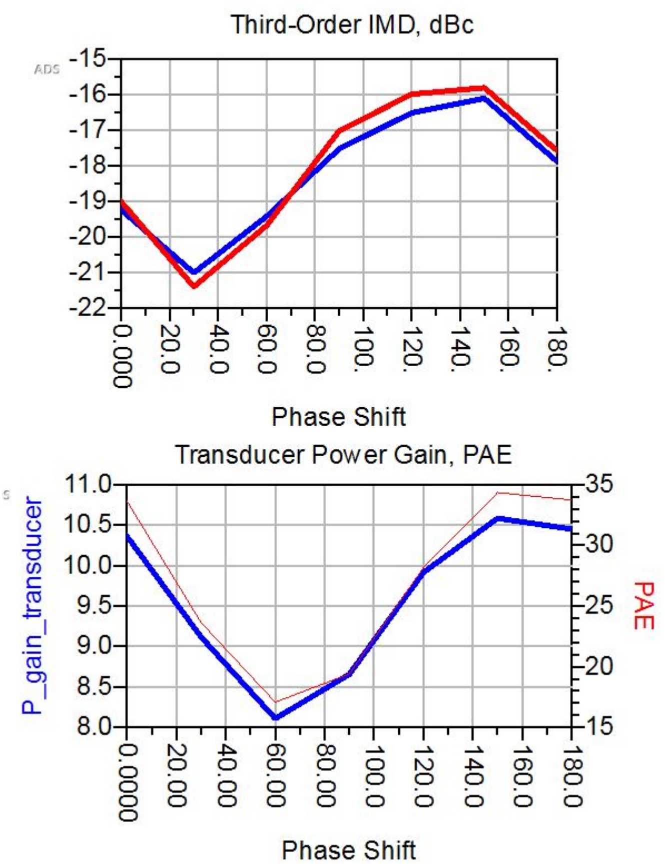

Fig. 9. The minimum and maximum in third-order IMD generally coincide with minimum and maximum in PAE

H. Simulated Performance

Under a one tone drive of 26dBm, the amplifier is able to deliver 37.5 dBm of power to the load. The waveforms seen in Figure 10 show a full voltage swing without current clipping. Without including the DC draw of the injection path amplifier, the power added efficiency is 68.64%. When the DC draw of the injection path amplifier is included, the efficiency drops to 36.496%. Furthermore, the fundamental load of the injection amplifier should be scaled from its class B optimal impedance by $\sqrt{2}$; however, changing the load impedance from the value in Table I only lowered the output power and efficiency [1]. Under a two tone drive with 5 MHz spacing,

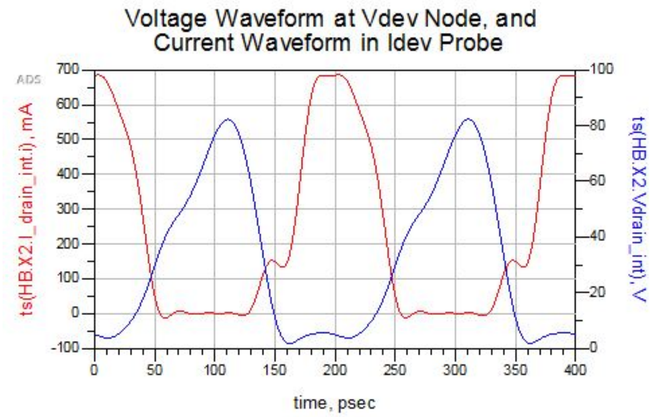

Fig. 10. Waveforms at the drain terminal of the die.

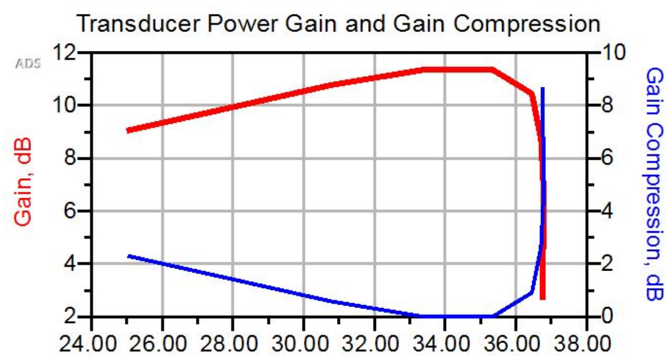

Fig. 11. Gain and gain compression as a function of input power drive, demonstrating hard compression around 37 dBm of input drive.

PAE is simulated to be 33.71% including injection path power draw when driven at 26 dBm with only .903 dB of gain compression and delivering 36.45 dBm. The IMD3 at 26dBm of input drive is -13dBc. The amplifier's 3dB compression input drive is at 29 dBm and rapidly compresses after this point. The best linearity performance is seen in Figure 13 when the amplifier is driven with only 22dBm of input power and uncompressed, delivering 33.3 dBm of output power. However Figure 12 reflects that backing off the power causes a drop in efficiency. The amplifier has a window from 32dBm to 36dBm output power in which its linearity stays under -25 dBm, and the PAE ranges from 15 to 30 %.

III. Future Work and Conclusion

The efficiency of the harmonic path impedes the efficiency of the overall harmonic injection amplifier; in future work, it would be of interest to investigate the use of a two-stage injection path and perhaps investigate the efficacy of using a diode as a frequency mixer in combination with an efficient amplifier at 10GHz. The injection power amplifier should also have a fundamental load that is scaled from its Class B optimal impedance by $\sqrt{2}$; this design did not fulfill that quality. Furthermore, the injection of the second harmonic is intended

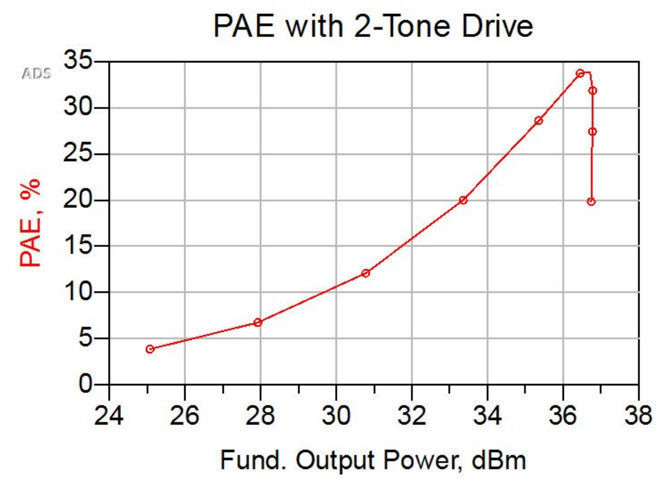

Fig. 12. Power added efficiency as a function of input power drive.

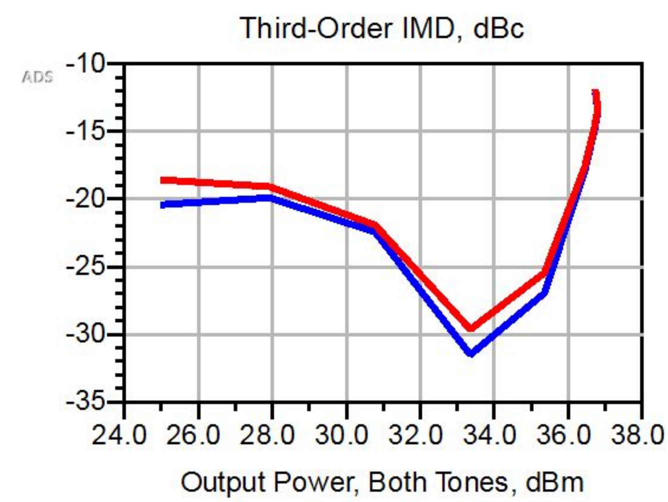

Fig. 13. IMD3 as a function of output power; optimum linearity is around 32-26 dBm of output power.

to reduce dissipated power and convert more DC power to RF power. The class B amplifier in Figure 5 has a greater output power without harmonic injection than the harmonic injection power amplifier, which indicates that the design can be further optimized to generate greater output power while also maintaining high efficiency.

References

[1] A. A. Almuhaisen, *A Novel Approach for Wide Band High-Efficiency Power Amplifier Design*. PhD thesis, Cardiff University, 5 2012.

[2] S. C. Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition (Artech House Microwave Library (Hardcover))*. Norwood, MA, USA: Artech House, Inc., 2006.