Allison Basore
Comp Arch HW#2
9/20/1028

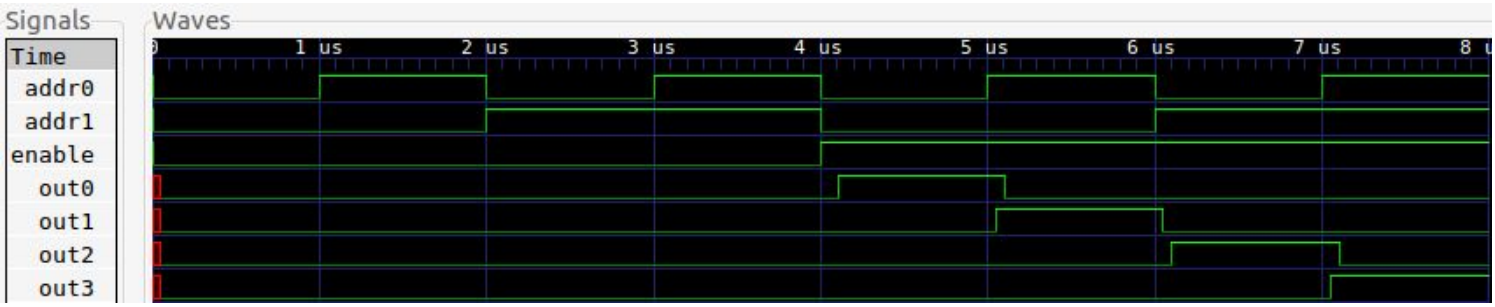
# HW 0b010: Verilog Building Blocks

**Decoder:**

Test Results for decoder showing enable, address 1, and address 2 combinations.

```
Decoder:
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```

Waveform for decoder showing each output high only when the right combination of address one and two are high and when enable is high.




**Multiplexer:**

Test results for multiplexer with all combinations of address 1 and address 2 with the four inputs.

```
Multiplexer:

A0 A1| O0 O1 O2 O3 | Output | Expected Output
0  0 | 1  0  0  0 | 1 | Same As 00
1  0 | 1  0  0  0 | 0 | Same As 01
1  1 | 1  0  0  0 | 0 | Same As 02
0  1 | 1  0  0  0 | 0 | Same As 03
-----------------------------------
0  0 | 0  1  0  0 | 0 | Same As 00
1  0 | 0  1  0  0 | 1 | Same As 01
0  1 | 0  1  0  0 | 0 | Same As 02
1  1 | 0  1  0  0 | 0 | Same As 03
-----------------------------------
0  0 | 0  0  1  0 | 0 | Same As 00
1  0 | 0  0  1  0 | 0 | Same As 01
0  1 | 0  0  1  0 | 1 | Same As 02
1  1 | 0  0  1  0 | 0 | Same As 03
-----------------------------------
0  0 | 0  0  0  1 | 0 | Same As 00
1  0 | 0  0  0  1 | 0 | Same As 01
0  1 | 0  0  0  1 | 0 | Same As 02
1  1 | 0  0  0  1 | 1 | Same As 03
```

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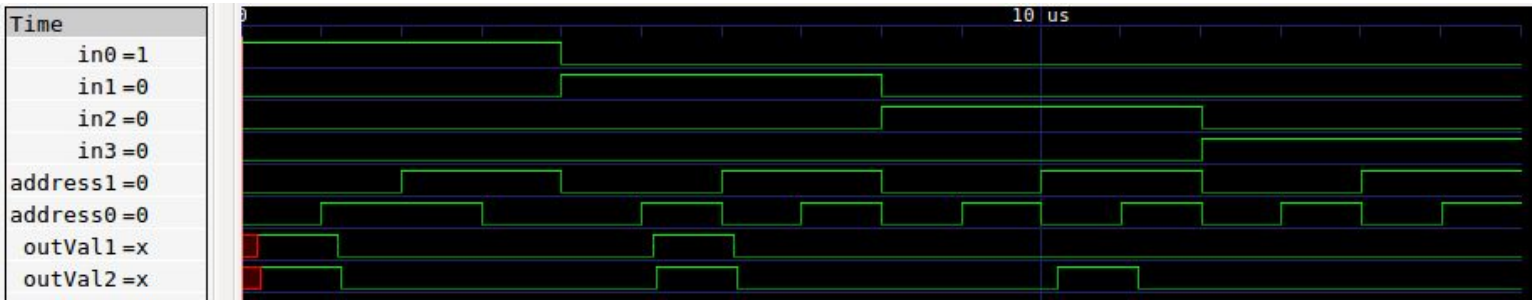
Waveform for the multiplexer showing the output with various combinations of address0 and address1 across each of the four inputs being high.




**Adder:**

Test results for an adder with combinations of A and B and CarryIn.

Adder:

| A | B | CarryIn | CarryOut | Carry Out Should Be | Sum | Sum Should Be |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | False | 0 | False |
| 0 | 0 | 1 | 0 | False | 1 | True |
| 0 | 1 | 0 | 0 | False | 1 | True |
| 0 | 1 | 1 | 1 | True | 0 | False |
| 1 | 0 | 0 | 0 | False | 1 | True |
| 1 | 0 | 1 | 1 | True | 0 | False |
| 1 | 1 | 0 | 1 | True | 0 | False |
| 1 | 1 | 1 | 1 | True | 1 | True |

Waveform for a full adder showing the carryOut and sum values for possible carryIn, A, and B values.