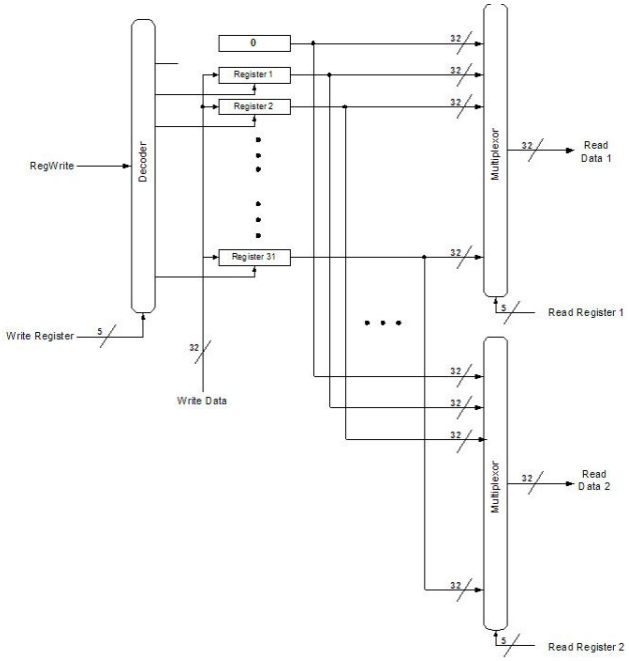
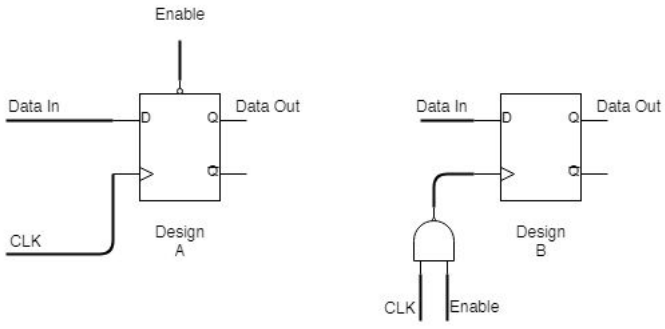
Allison Basore
10/10/2018
Comp-Arch: HW 4

For this assignment, I created a memory component, a register file, which will be reused in my CPU design. The register file was made according to the following design.



The following is a circuit diagram of showing the structural equivalent of two possible implementations of a register.



The following is a brief description of how the following Decoder behavioral Verilog works:

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```
module decoder1to32
(
output[31:0]  out,
input         enable,
input[4:0]    address
);
    assign out = enable<<address;
endmodule
```

The “assign out” line uses the left shift operator to shift the significant digit of enable to be in the right position according to the address. If enable is 1 (high), and the address is 0000, then we do not shift enable at all and the first output bit is 1 while the rest are zeros. If enable is 1 (high), and the address is 0011, then it will shift enable by 3 and the output will be 1 with three zeros behind it: 1000, which corresponds to that output index being set to high. The same pattern continues for all possible address values. If enable is 0 (low), then no matter what the address is, it will be all 0's.