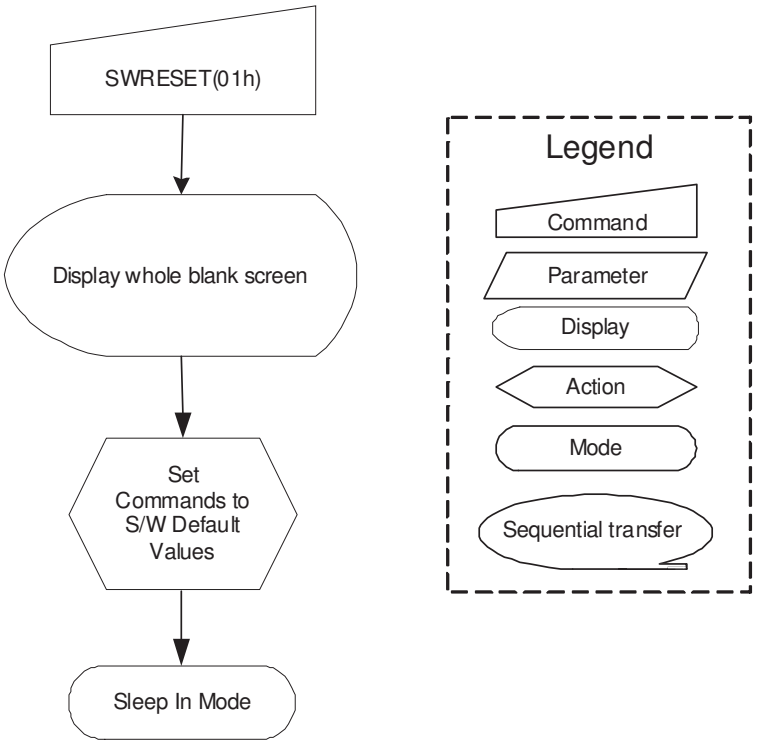
## 8.2. Description of Level 1 Command

### 8.2.1. NOP (00h)

<table>
<tr><th>00h</th><th colspan="12">NOP (No Operation)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter.</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.<br>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">None</td></tr>
</table>

## 8.2.2. Software Reset (01h)

| 01h | SWRESET | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |
| Parameter | No Parameter. | | | | | | | | | | | | |
| Description | When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)<br>Note: The Frame Memory contents are unaffected by this command<br>X = Don't care. | | | | | | | | | | | | |
| Restriction | It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence. | | | | | | | | | | | | |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Normal Mode On, Idle Mode On, Sleep Out — Yes<br>Partial Mode On, Idle Mode Off, Sleep Out — Yes<br>Partial Mode On, Idle Mode On, Sleep Out — Yes<br>Sleep In — Yes | | | | | | | | | | | | |
| Default | Status: Power On Sequence — Default Value: N/A<br>SW Reset — N/A<br>HW Reset — N/A | | | | | | | | | | | | |
| Flow Chart |  | | | | | | | | | | | | |

## 8.2.3. Read display identification information (04h)

| 04h | RDDIDIF (Read Display Identification Information) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | ID1 [7:0] | | | | | | | | XX |
| 3rd Parameter | 1 | ↑ | 1 | XX | ID2 [7:0] | | | | | | | | XX |
| 4th Parameter | 1 | ↑ | 1 | XX | ID3 [7:0] | | | | | | | | XX |
| Description | This read byte returns 24 bits display identification information.<br>The 1st parameter is dummy data.<br>The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID.<br>The 3rd parameter (ID2 [7:0]): LCD module/driver version ID.<br>The 4th parameter (ID3 [7:0]): LCD module/driver ID. | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

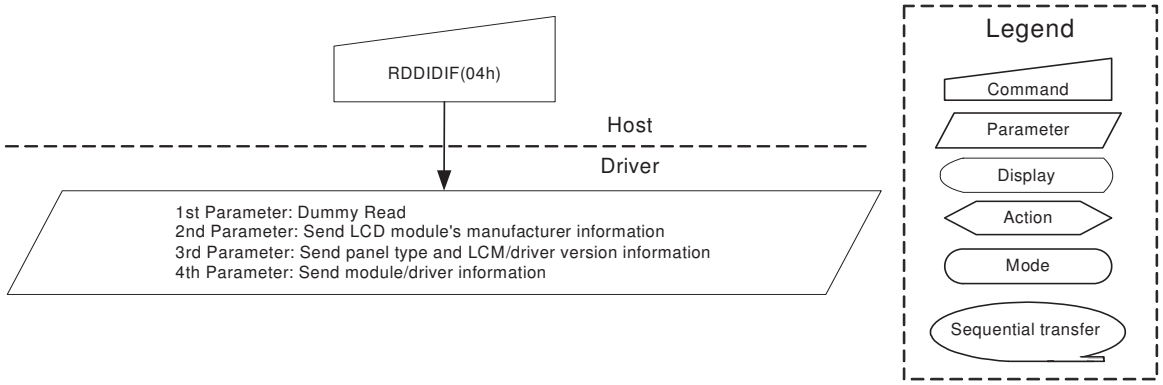
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | See description |
| SW Reset | See description |
| HW Reset | See description |

Flow Chart



## 8.2.4. Read Display Status (09h)

| 09h | RDDST (Read Display Status) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | D [31:25] | | | | | | | 0 | 00 |
| 3rdParameter | 1 | ↑ | 1 | XX | 0 | D [22:20] | | | D [19:16] | | | | 61 |
| 4thParameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | D [10:8] | | | 00 |
| 5thParameter | 1 | ↑ | 1 | XX | D [7:5] | | | 0 | 0 | 0 | 0 | 0 | 00 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value | Status |
|---|---|---|---|
| D31 | Booster voltage status | 0 | Booster OFF |
| | | 1 | Booster ON |
| D30 | Row address order | 0 | Top to Bottom (When MADCTL B7='0') |
| | | 1 | Bottom to Top (When MADCTL B7='1') |
| D29 | Column address order | 0 | Left to Right (When MADCTL B6='0'). |
| | | 1 | Right to Left (When MADCTL B6='1'). |
| D28 | Row/column exchange | 0 | Normal Mode (When MADCTL B5='0'). |
| | | 1 | Reverse Mode (When MADCTL B5='1'). |
| D27 | Vertical refresh | 0 | LCD Refresh Top to Bottom (When MADCTL B4='0') |
| | | 1 | LCD Refresh Bottom to Top (When MADCTL B4='1'). |
| D26 | RGB/BGR order | 0 | RGB (When MADCTL B3='0') |
| | | 1 | BGR (When MADCTL B3='1') |
| D25 | Horizontal refresh order | 0 | LCD Refresh Left to Right (When MADCTL B2='0') |
| | | 1 | LCD Refresh Right to Left (When MADCTL B2='1') |
| D24 | Not used | 0 | --- |
| D23 | Not used | 0 | --- |
| D22 | Interface color pixel format definition | 101 | 16-bit/pixel |
| D21 | | 110 | 18-bit/pixel |
| D20 | | | |
| D19 | Idle mode ON/OFF | 0 | Idle Mode OFF |
| | | 1 | Idle Mode ON |
| D18 | Partial mode ON/OFF | 0 | Partial Mode OFF |
| | | 1 | Partial Mode ON. |
| D17 | Sleep IN/OUT | 0 | Sleep IN Mode |
| | | 1 | Sleep OUT Mode. |
| D16 | Display normal mode ON/OFF | 0 | Display Normal Mode OFF. |
| | | 1 | Display Normal Mode ON. |
| D15 | Vertical scrolling status | 0 | Scroll OFF |
| D14 | Not used | 0 | --- |
| D13 | Inversion status | 0 | Not defined |
| D12 | All pixel ON | 0 | Not defined |
| D11 | All pixel OFF | 0 | Not defined |
| D10 | Display ON/OFF | 0 | Display is OFF |
| | | 1 | Display is ON |
| D9 | Tearing effect line ON/OFF | 0 | Tearing Effect Line OFF |
| | | 1 | Tearing Effect ON |
| D[8:6] | Gamma curve selection | 000 | GC0 |
| | | 001 | --- |
| | | 010 | --- |
| | | 011 | --- |
| | | other | Not defined |

| | | | | |
|---|---|---|---|---|
| | D5 | Tearing effect line mode | 0 | Mode 1, V-Blanking only |
| | | | 1 | Mode 2, both H-Blanking and V-Blanking. |
| | D4 | Not used | 0 | --- |
| | D3 | Not used | 0 | --- |
| | D2 | Not used | 0 | --- |
| | D1 | Not used | 0 | --- |
| | D0 | Not used | 0 | --- |

X = Don't care

Restriction

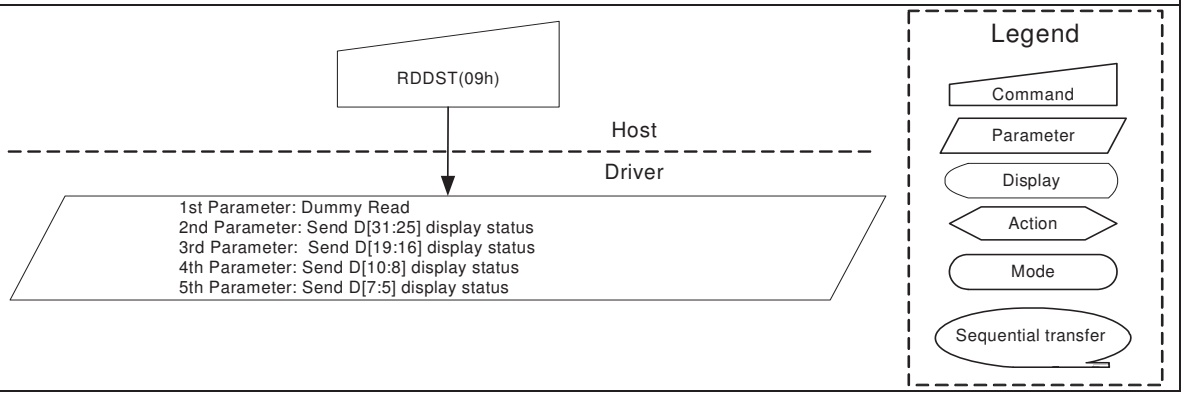
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 32'h00610000h |
| SW Reset | 32'h00610000h |
| HW Reset | 32'h00610000h |

Flow Chart



## 8.2.5. Read Display Power Mode (0Ah)

| 0Ah | RDDPM (Read Display Power Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0Ah |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 08 |

**Description**

This command indicates the current status of the display as described in the table below::

| Bit | Value | Description | Comment |
|---|---|---|---|
| D7 | 0 | Booster Off or has a fault. | --- |
| | 1 | Booster On and working OK | --- |
| D6 | 0 | Idle Mode Off. | --- |
| | 1 | Idle Mode On. | --- |
| D5 | 0 | Partial Mode Off. | --- |
| | 1 | Partial Mode On. | --- |
| D4 | 0 | Sleep In Mode | --- |
| | 1 | Sleep Out Mode | --- |
| D3 | 0 | Display Normal Mode Off. | --- |
| | 1 | Display Normal Mode On | --- |
| D2 | 0 | Display is Off. | --- |
| | 1 | Display is On | --- |
| D1 | -- | Not Defined | Set to '0' |
| D0 | -- | Not Defined | Set to '0' |

X = Don't care

**Restriction**

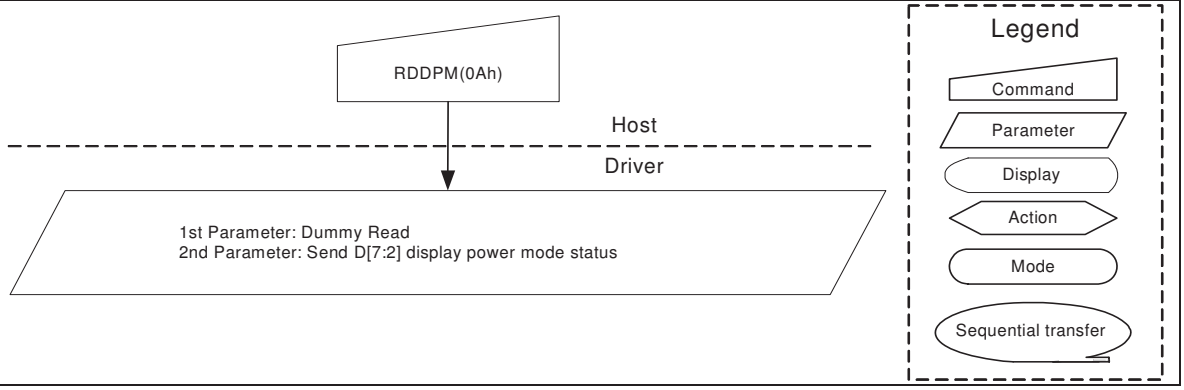
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 8'h08h |
| SW Reset | 8'h08h |
| HW Reset | 8'h08h |

**Flow Chart**



## 8.2.6. Read Display MADCTL (0Bh)

| 0Bh | RDDMADCTL (Read Display MADCTL) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0Bh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Value | Description | Comment |
|---|---|---|---|
| D7 | 0 | Top to Bottom (When MADCTL B7='0'). | --- |
| | 1 | Bottom to Top (When MADCTL B7='1'). | --- |
| D6 | 0 | Left to Right (When MADCTL B6='0') | --- |
| | 1 | Right to Left (When MADCTL B6='1') | --- |
| D5 | 0 | Normal Mode (When MADCTL B5='0'). | --- |
| | 1 | Reverse Mode (When MADCTL B5='1') | --- |
| D4 | 0 | LCD Refresh Top to Bottom (When MADCTL B4='0') | --- |
| | 1 | LCD Refresh Bottom to Top (When MADCTL B4='1'). | --- |
| D3 | 0 | RGB (When MADCTL B3='0') | --- |
| | 1 | BGR (When MADCTL B3='1'). | --- |
| D2 | 0 | LCD Refresh Left to Right (When MADCTL B2='0'). | --- |
| | 1 | LCD Refresh Right to Left (When MADCTL B2='1'). | --- |
| D1 | -- | Switching between Segment outputs and RAM | Set to '0' |
| D0 | -- | Switching between Segment outputs and RAM | Set to '0' |

X = Don't care

Restriction

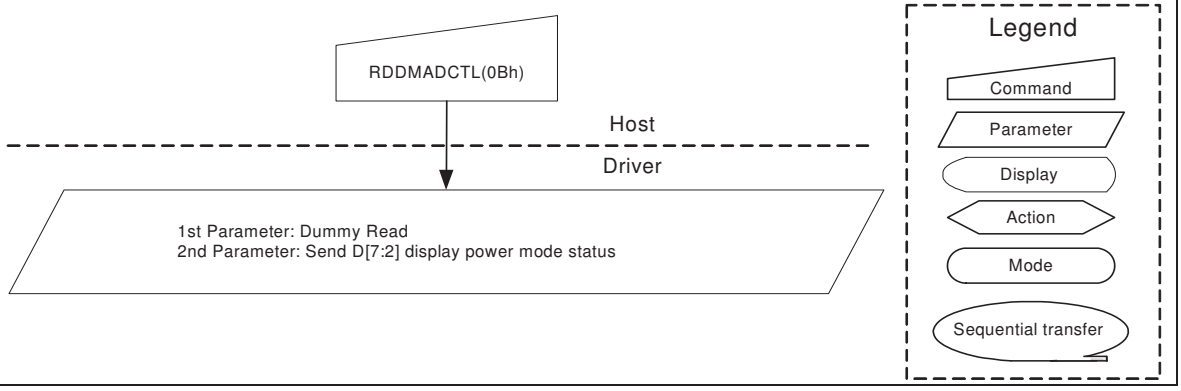
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 8'h00h |
| SW Reset | No Change |
| HW Reset | 8'h00h |

Flow Chart



## 8.2.7. Read Display Pixel Format (0Ch)

| 0Ch | RDDCOLMOD (Read Display Pixel Format) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0Ch |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | RIM | DPI [2:0] | | | 0 | DBI [2:0] | | | 06 |

**Description**

This command indicates the current status of the display as described in the table below:

| RIM | DPI [2:0] | | | RGB Interface Format |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 0 | Reserved |
| 0 | 0 | 1 | 1 | Reserved |
| 0 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 1 | 16 bits / pixel |
| 0 | 1 | 1 | 0 | 18 bits / pixel |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 1 | 16 bits / pixel (6-bit 3 times data transfer) |
| 1 | 1 | 1 | 0 | 18 bits / pixel (6-bit 3 times data transfer) |

| DBI [2:0] | | | MCU Interface Format |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 16 bits / pixel |
| 1 | 1 | 0 | 18 bits / pixel |
| 1 | 1 | 1 | Reserved |

X = Don't care

**Restriction**

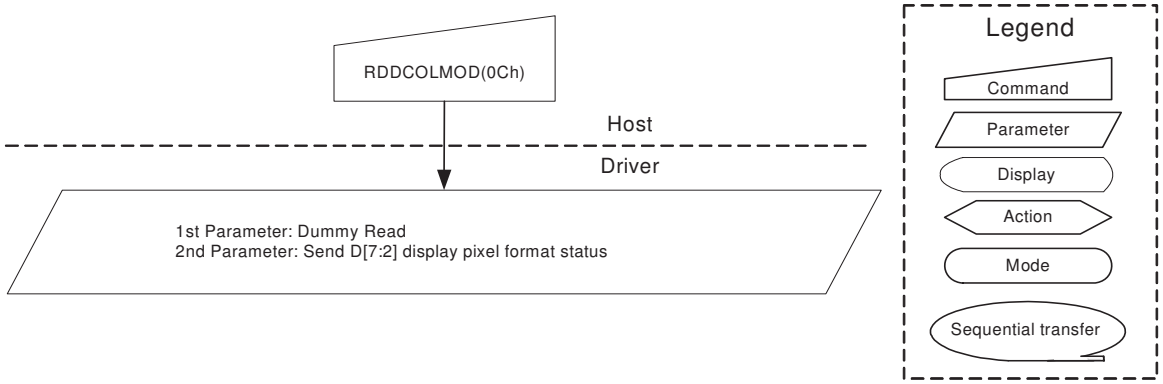
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | RIM | DPI [2:0] | DBI [2:0] |
| Power On Sequence | 1'b0 | 3'b000 | 3'b110 |
| SW Reset | No Chang | No Chang | No Chang |
| HW Reset | 1'b0 | 3'b000 | 3'b110 |

**Flow Chart**



## 8.2.8. Read Display Image Format (0Dh)

| 0Dh | RDDIM (Read Display Image Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0Dh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | D [2:0] | | | 00 |

**Description**

This command indicates the current status of the display as described in the table below:

| D [2:0] | Description |
|---|---|
| 000 | Gamma curve 1 (G2.2) |
| 001 | --- |
| 010 | --- |
| 011 | --- |
| Other | Not defined |

X = Don't care

**Restriction**

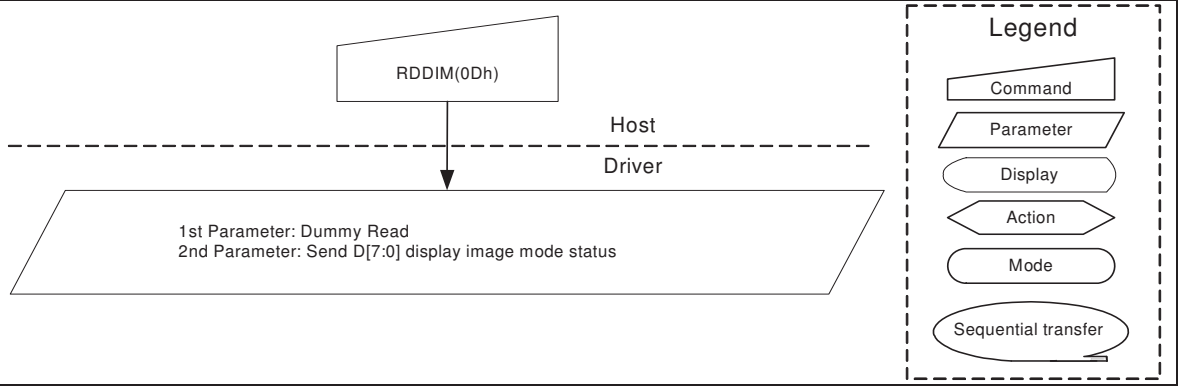
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 3'b000 |
| SW Reset | 3'b000 |
| HW Reset | 3'b000 |

**Flow Chart**



## 8.2.9. Read Display Signal Mode (0Eh)

| 0Eh | RDDSM (Read Display Signal Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0Eh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Value | Description |
|---|---|---|
| D7 | 0 | Tearing effect line OFF |
| | 1 | Tearing effect line ON |
| D6 | 0 | Tearing effect line mode 1 |
| | 1 | Tearing effect line mode 2 |
| D5 | 0 | Horizontal sync. (RGB interface) OFF |
| | 1 | Horizontal sync. (RGB interface) ON |
| D4 | 0 | Vertical sync. (RGB interface) OFF |
| | 1 | Vertical sync. (RGB interface) ON |
| D3 | 0 | Pixel clock (DOTCLK, RGB interface) OFF |
| | 1 | Pixel clock (DOTCLK, RGB interface) ON |
| D2 | 0 | Data enable (DE, RGB interface) OFF |
| | 1 | Data enable (DE, RGB interface) ON |
| D1 | 0 | Reserved |
| D0 | 0 | Reserved |

X = Don't care

**Restriction**

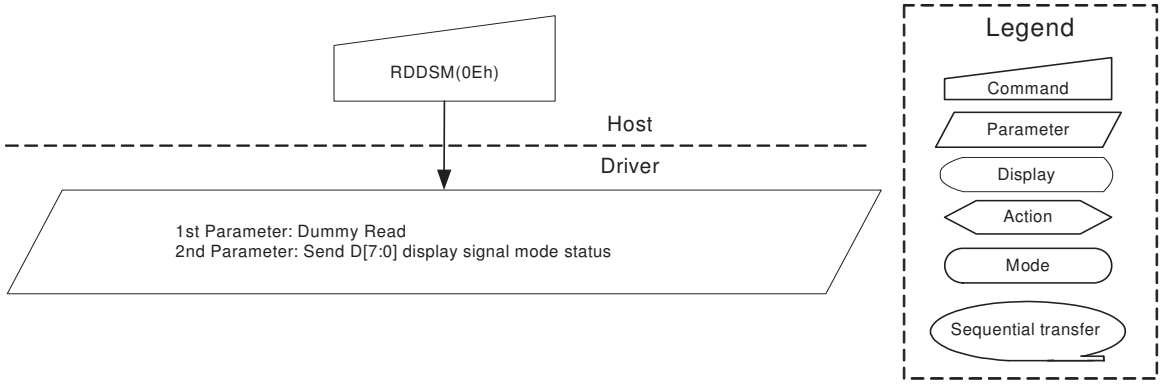
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 8'h00h |
| SW Reset | 8'h00h |
| HW Reset | 8'h00h |

**Flow Chart**



## 8.2.10. Read Display Self-Diagnostic Result (0Fh)

| 0Fh | RDDSDR (Read Display Self-Diagnostic Result) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0Fh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |

**Description**

| Bit | Description | Action |
|---|---|---|
| D7 | Register Loading Detection | Invert the D7 bit if register values loading work properly. |
| D6 | Functionality Detection | Invert the D6 bit if the display is functionality |
| D5 | Not Used | '0' |
| D4 | Not Used | '0' |
| D3 | Not Used | '0' |
| D2 | Not Used | '0' |
| D1 | Not Used | '0' |
| D0 | Not Used | '0' |

**Restriction**

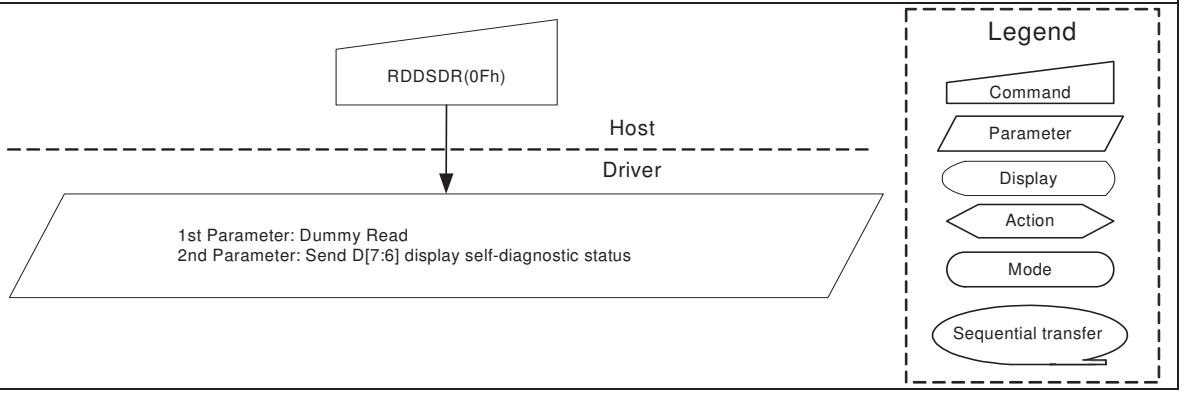
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 8'h00h |
| SW Reset | 8'h00h |
| HW Reset | 8'h00h |

**Flow Chart**



## 8.2.11. Enter Sleep Mode (10h)

| 10h | SPLIN (Enter Sleep Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10h |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.<br><br>MCU interface and memory are still working and the memory keeps its contents.<br>X = Don't care | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. | | | | | | | | | | | | |

Register Availability

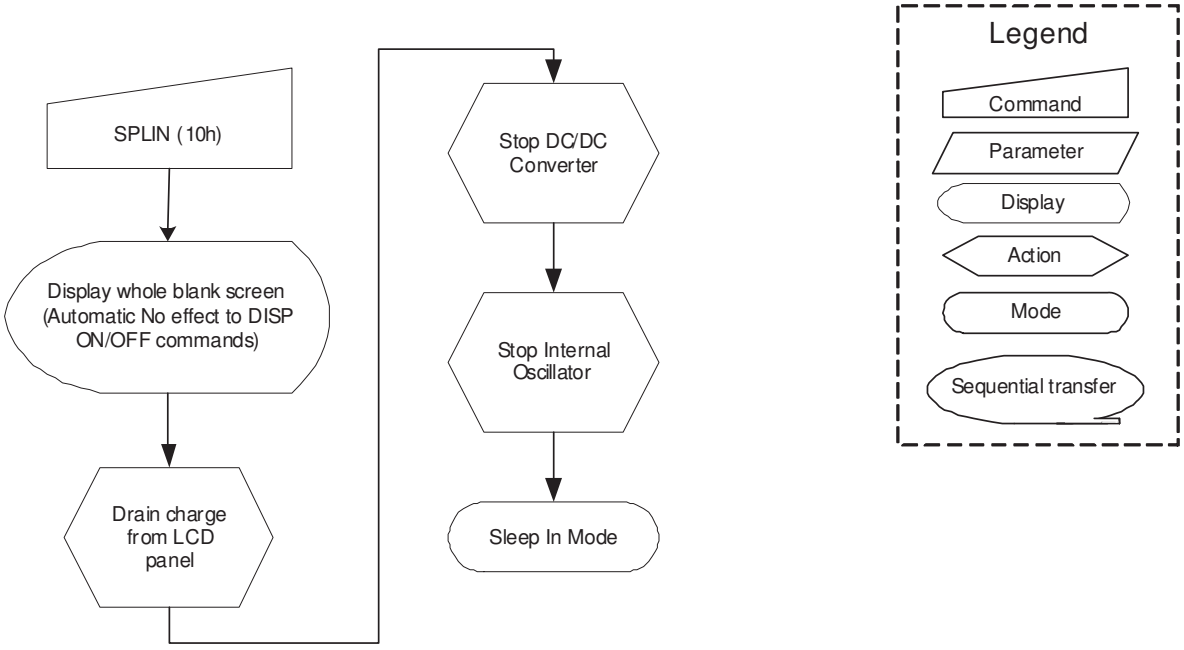
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Sleep IN Mode |
| SW Reset | Sleep IN Mode |
| HW Reset | Sleep IN Mode |

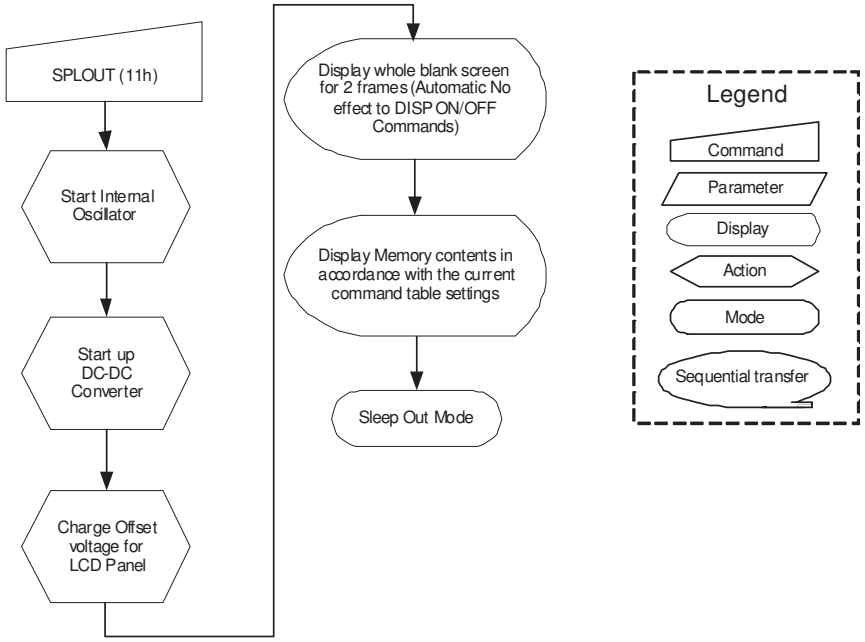
Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



## 8.2.12. Sleep Out (11h)

<table>
<tr><th>11h</th><th colspan="12">SLPOUT (Sleep Out)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.<br>In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.<br><br>X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">It takes 120msec to become Sleep Out mode after SLPOUT command issued.</td></tr>
</table>



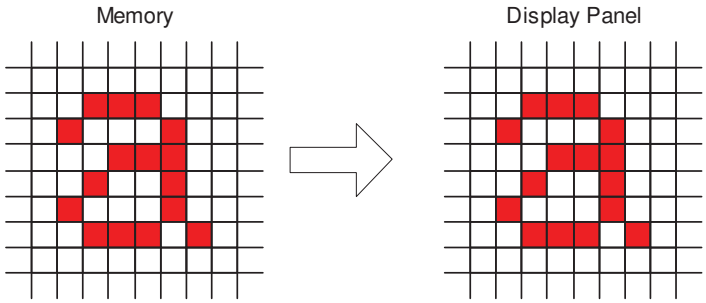
## 8.2.13. Partial Mode ON (12h)

<table>
<tr><th>12h</th><th colspan="12">PTLON (Partial Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.<br>X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

## 8.2.14. Normal Display Mode ON (13h)

<table>
<tr><th>13h</th><th colspan="13">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.<br>Normal display mode on means Partial mode off.<br>Exit from NORON by the Partial mode On command (12h)<br>X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

## 8.2.15. Display Inversion OFF (20h)

| 20h | DINVOFF (Display Inversion OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command is used to recover from display inversion mode.<br>This command makes no change of the content of frame memory.<br>This command doesn't change any other status.<br>  <br>X = Don't care | | | | | | | | | | | | |
| Restriction | This command has no effect when module already is inversion OFF mode. | | | | | | | | | | | | |

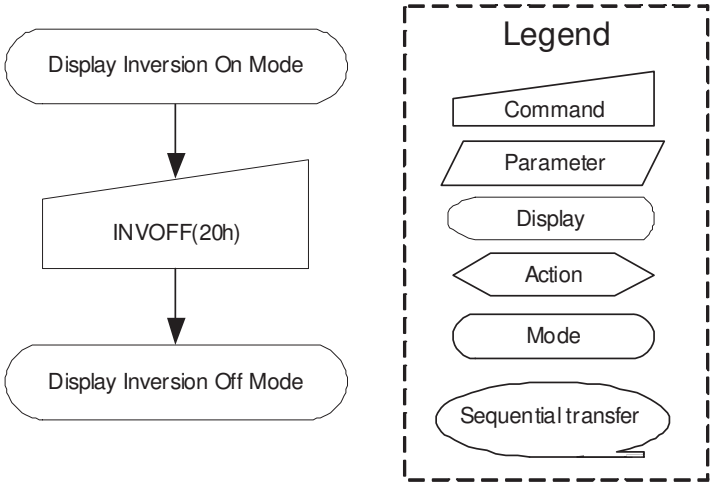
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion OFF |
| SW Reset | Display Inversion OFF |
| HW Reset | Display Inversion OFF |

Flow Chart



## 8.2.16. Display Inversion ON (21h)

| 21h | DINVON (Display Inversion ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h |
| Parameter | No Parameter | | | | | | | | | | | | |

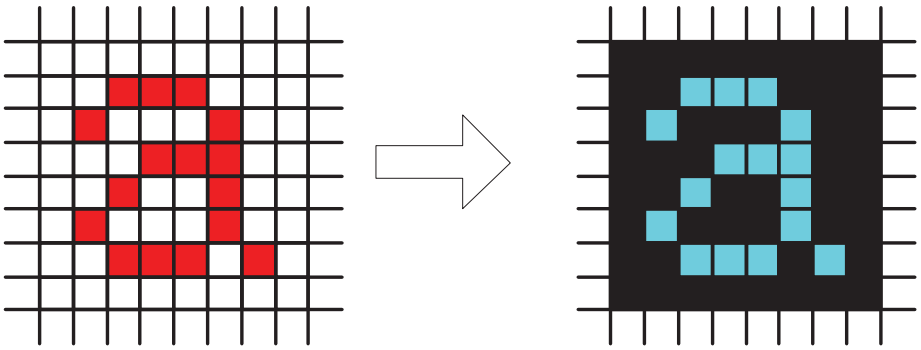
**Description**

This command is used to enter into display inversion mode.

This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.

This command doesn't change any other status.

To exit Display inversion mode, the Display inversion OFF command (20h) should be written.



X = Don't care

**Restriction**

This command has no effect when module already is inversion ON mode.

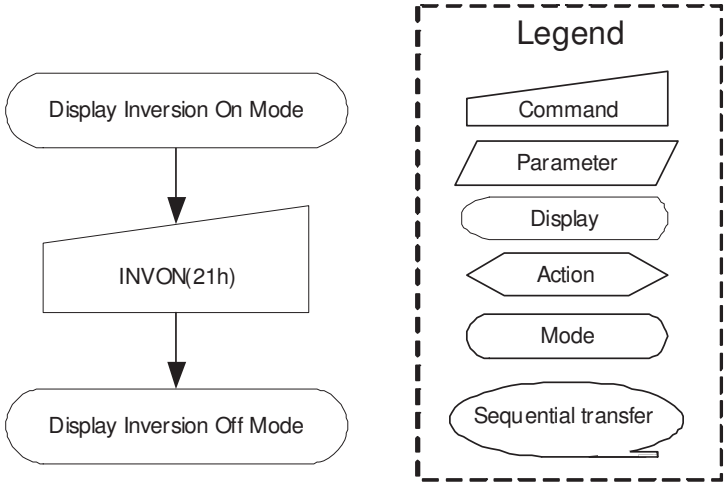
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion OFF |
| SW Reset | Display Inversion OFF |
| HW Reset | Display Inversion OFF |

**Flow Chart**



## 8.2.17. Gamma Set (26h)

| 26h | GAMSET (Gamma Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26h |
| Parameter | 1 | 1 | ↑ | XX | GC [7:0] | | | | | | | | 01 |

**Description**

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

| GC [7:0] | Curve Selected |
|---|---|
| 01h | Gamma curve 1 (G2.2) |
| 02h | --- |
| 04h | --- |
| 08h | --- |

Note: All other values are undefined.

X = Don't care

**Restriction**

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

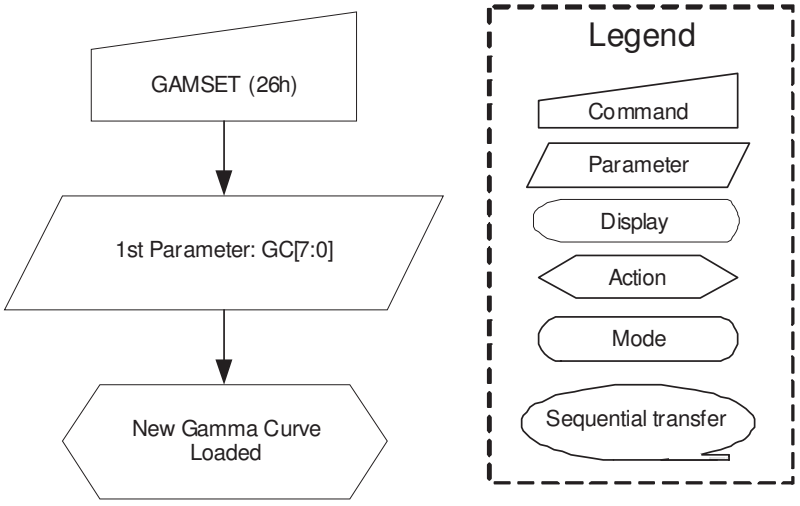
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 8'h01h |
| SW Reset | 8'h01h |
| HW Reset | 8'h01h |

**Flow Chart**



## 8.2.18. Display OFF (28h)

| 28h | DISPOFF (Display OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28h |
| Parameter | No Parameter | | | | | | | | | | | | |

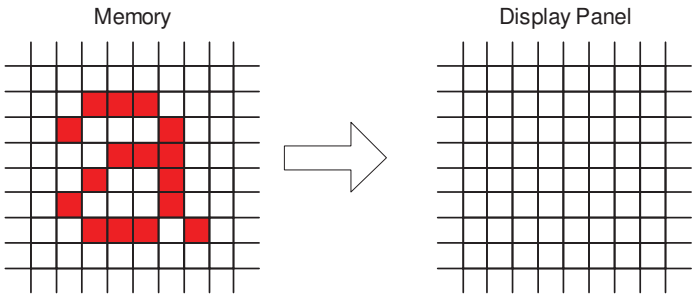
**Description**

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.

This command makes no change of contents of frame memory.

This command does not change any other status.

There will be no abnormal visible effect on the display.




X = Don't care.

**Restriction**

This command has no effect when module is already in display off mode.

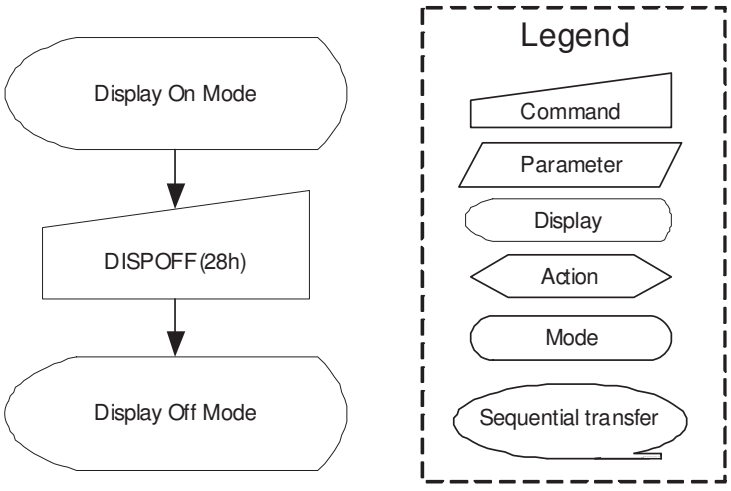
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

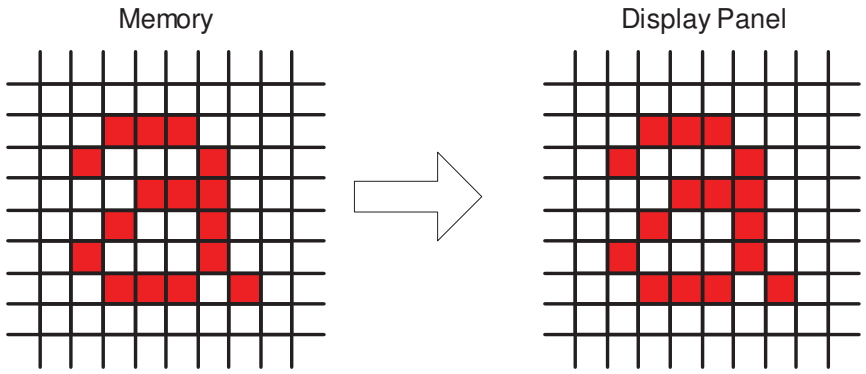
**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display OFF |
| SW Reset | Display OFF |
| HW Reset | Display OFF |

**Flow Chart**



## 8.2.19. Display ON (29h)

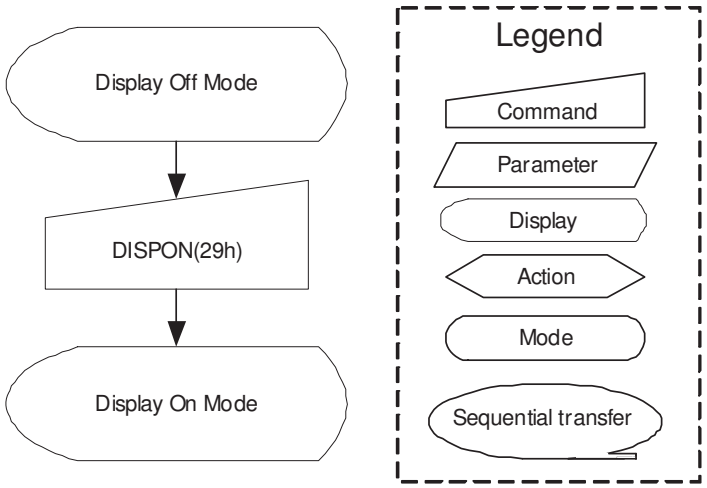
| 29h | DISPON (Display ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29h |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status<br>  <br>X = Don't care. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in display on mode. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display OFF |
| SW Reset | Display OFF |
| HW Reset | Display OFF |

Flow Chart

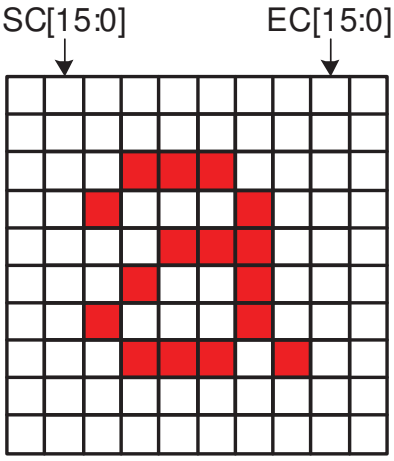


## 8.2.20. Column Address Set (2Ah)

| 2Ah | CASET (Column Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2Ah |
| 1st Parameter | 1 | 1 | ↑ | XX | SC15 | SC14 | SC13 | SC12 | SC11 | SC10 | SC9 | SC8 | Note1 |
| 2ndParameter | 1 | 1 | ↑ | XX | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | |
| 3rd Parameter | 1 | 1 | ↑ | XX | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 | Note1 |
| 4th Parameter | 1 | 1 | ↑ | XX | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | |

**Description**

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.




X = Don't care

**Restriction**

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored

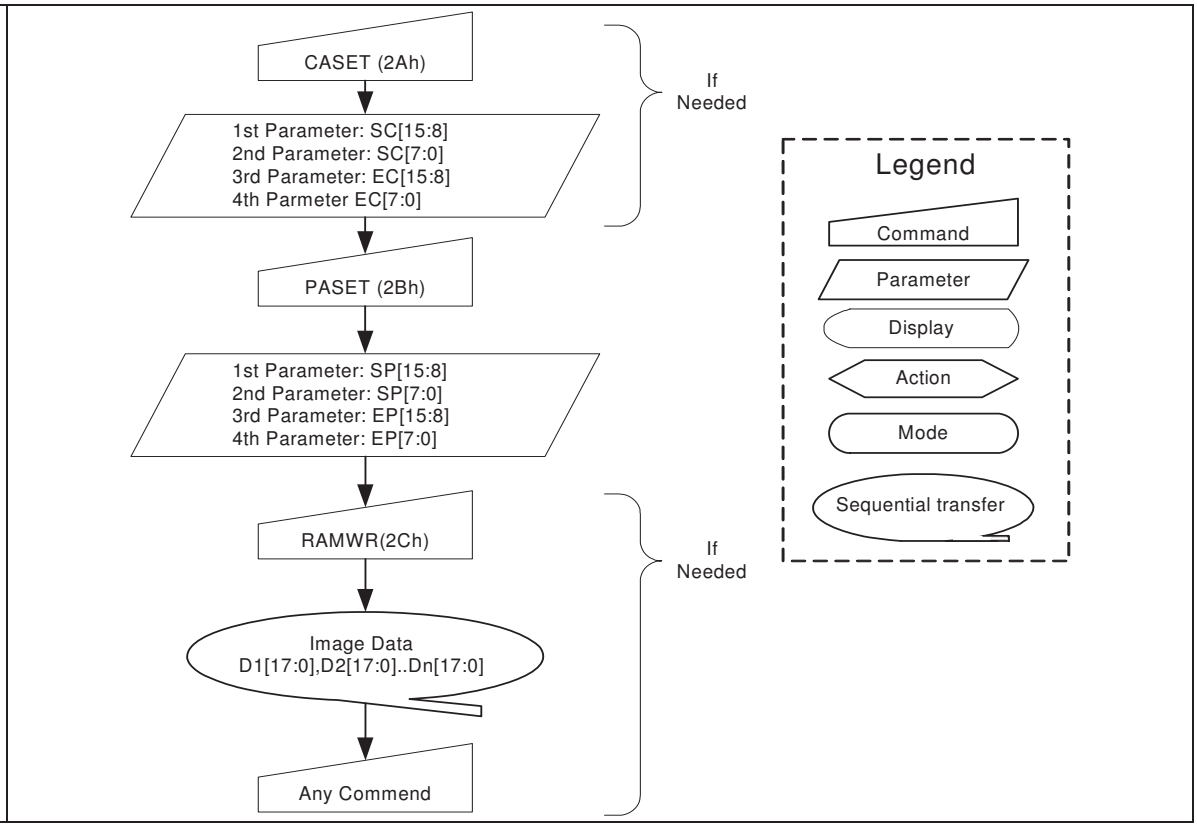
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| Power On Sequence | SC [15:0]=0000h | EC [15:0]=00EFh |
| SW Reset | SC [15:0]=0000h | If MADCTL's B5 = 0: EC [15:0]=00EFh<br>If MADCTL's B5 = 1: EC [15:0]=013Fh |
| HW Reset | SC [15:0]=0000h | EC [15:0]=00EFh |

Flow Chart

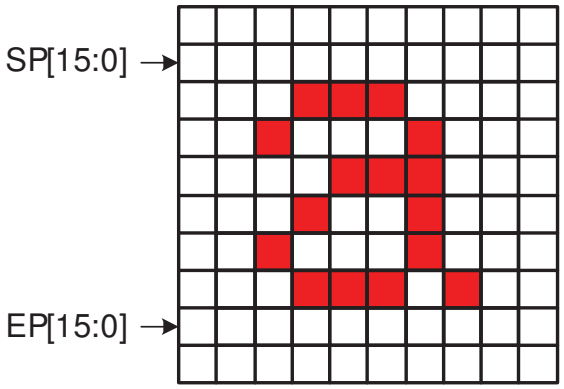


## 8.2.21. Page Address Set (2Bh)

| 2Bh | PASET (Page Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2Bh |
| 1st Parameter | 1 | 1 | ↑ | XX | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | Note1 |
| 2ndParameter | 1 | 1 | ↑ | XX | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | |
| 3rdParameter | 1 | 1 | ↑ | XX | EP15 | EP14 | EP13 | EP12 | EP11 | EP10 | EP9 | EP8 | Note1 |
| 4th Parameter | 1 | 1 | ↑ | XX | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 | |

**Description**

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.




X = Don't care

**Restriction**

SP [15:0] always must be equal to or less than EP [15:0]

Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.

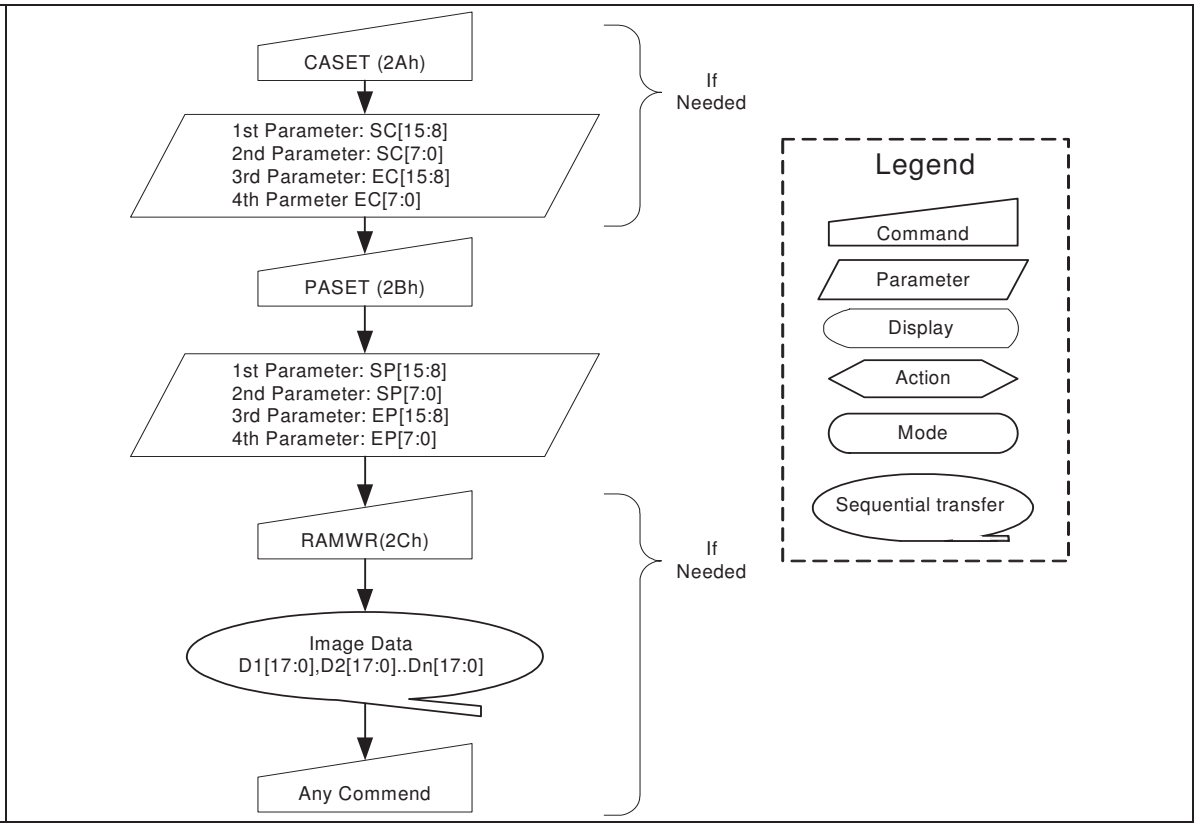
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| Power On Sequence | SP [15:0]=0000h | EP [15:0]=013Fh |
| SW Reset | SP [15:0]=0000h | If MADCTL's B5 = 0: EP [15:0]=013Fh<br>If MADCTL's B5 = 1: EP [15:0]=00EFh |
| HW Reset | SP [15:0]=0000h | EP [15:0]=013Fh |

Flow Chart



## 8.2.22. Memory Write (2Ch)

| 2Ch | RAMWR (Memory Write) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2Ch |
| 1st Parameter | 1 | 1 | ↑ | D1 [17:0] | | | | | | | | | XX |
| : | 1 | 1 | ↑ | Dx [17:0] | | | | | | | | | XX |
| Nth Parameter | 1 | 1 | ↑ | Dn [17:0] | | | | | | | | | XX |

**Description**

This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.

**Restriction**

In all color modes, there is no restriction on length of parameters.

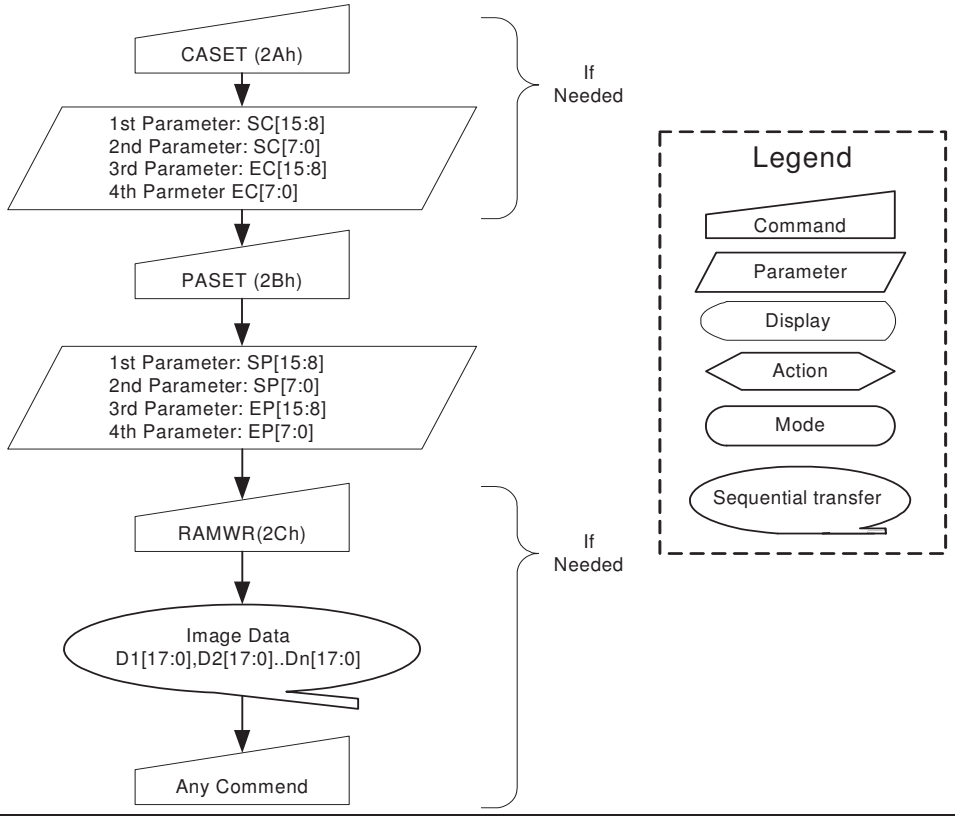
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| SW Reset | Contents of memory is not cleared |
| HW Reset | Contents of memory is not cleared |

**Flow Chart**



## 8.2.23. Color Set (2Dh)

| 2Dh | RGBSET (Color Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2Dh |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | R00 [5:0] | | | | | | XX |
| nth Parameter | 1 | 1 | ↑ | XX | 0 | 0 | Rnn [5:0] | | | | | | XX |
| 32ndParameter | 1 | 1 | ↑ | XX | 0 | 0 | R31 [5:0] | | | | | | XX |
| 33rdParameter | 1 | 1 | ↑ | XX | 0 | 0 | G00 [5:0] | | | | | | XX |
| nth Parameter | 1 | 1 | ↑ | XX | 0 | 0 | Gnn [5:0] | | | | | | XX |
| 96thParameter | 1 | 1 | ↑ | XX | 0 | 0 | G64 [5:0] | | | | | | XX |
| 97thParameter | 1 | 1 | ↑ | XX | 0 | 0 | B00 [5:0] | | | | | | XX |
| nth Parameter | 1 | 1 | ↑ | XX | 0 | 0 | Bnn [5:0] | | | | | | XX |
| 128thParameter | 1 | 1 | ↑ | XX | 0 | 0 | B31 [5:0] | | | | | | XX |

**Description**

This command is used to define the LUT for 16-bit to 18-bit color depth conversion.

128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.4 are referred.

This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.

**Restriction**

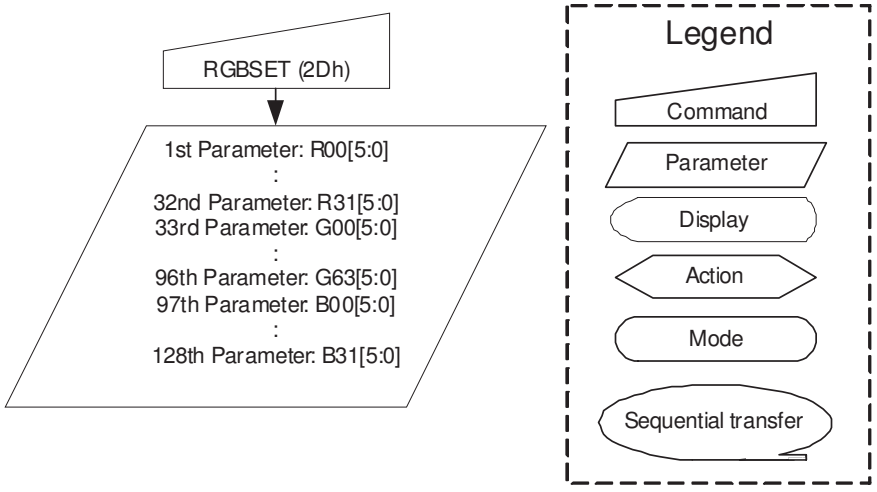
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Random values |
| SW Reset | Contents of LUT protected |
| HW Reset | Random values |

**Flow Chart**



## 8.2.24. Memory Read (2Eh)

| 2Eh | RAMRD (Memory Read) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2Eh |
| 1st Parameter | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | 1 | ↑ | D1 [17:0] | | | | | | | | | XX |
| : | 1 | 1 | ↑ | Dx [17:0] | | | | | | | | | XX |
| (N+1)th Parameter | 1 | 1 | ↑ | Dn [17:0] | | | | | | | | | XX |

**Description**

This command transfers image data from ILI9341's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

**Restriction**

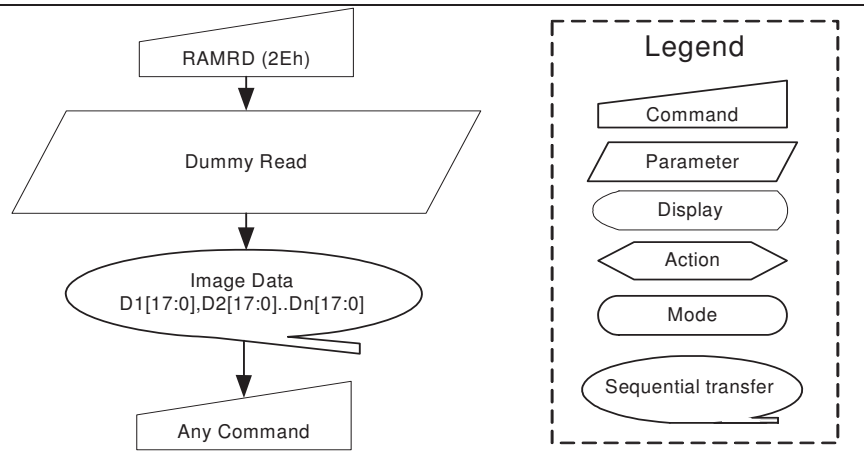
There is no restriction on length of parameters.

**Register Availability**

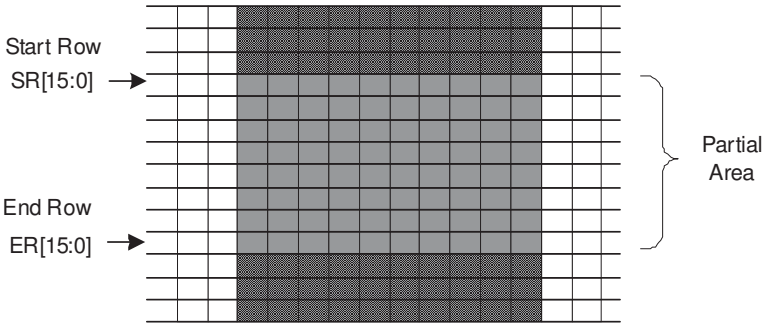
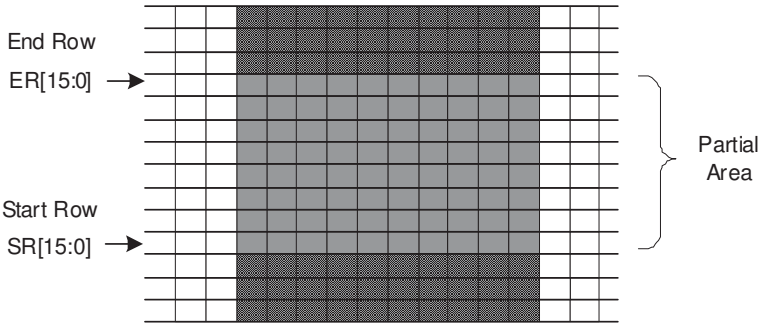
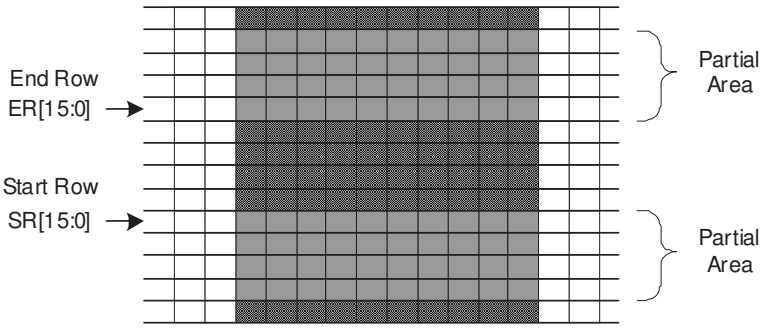
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| SW Reset | Contents of memory is set randomly |
| HW Reset | Contents of memory is set randomly |

| | |
|---|---|
| Flow Chart |  |

## 8.2.25. Partial Area (30h)

| 30h | PLTAR (Partial Area) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30h |
| 1st Parameter | 1 | 1 | ↑ | XX | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | 00 |
| 2ndParameter | 1 | 1 | ↑ | XX | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | 00 |
| 3rdParameter | 1 | 1 | ↑ | XX | ER15 | ER14 | ER13 | ER12 | ER11 | ER10 | ER9 | ER8 | 01 |
| 4th Parameter | 1 | 1 | ↑ | XX | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | 3F |
| Description | This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.<br>If End Row>Start Row when MADCTL B4=0:-<br>  <br><br>If End Row>Start Row when MADCTL B4=1:-<br>  <br><br>If End Row<Start Row when MADCTL B4=0:-<br>  <br><br>If End Row = Start Row then the Partial Area will be one row deep.<br>X = Don't care. | | | | | | | | | | | | |
| Restriction | SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh. | | | | | | | | | | | | |

**Register Availability**

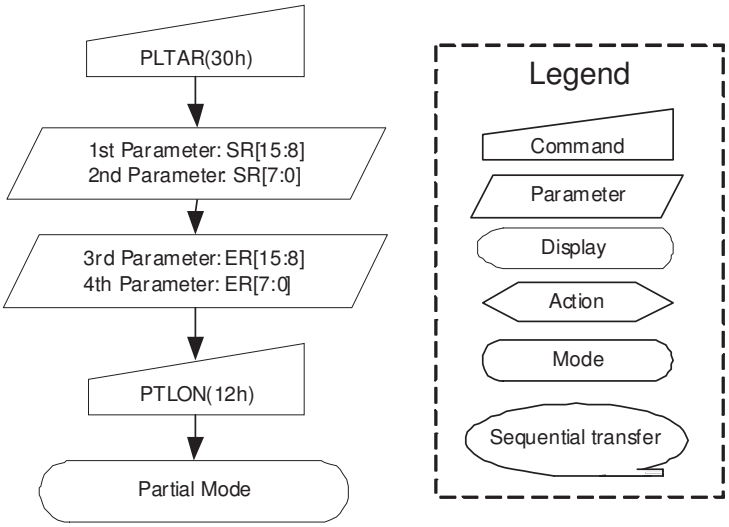
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

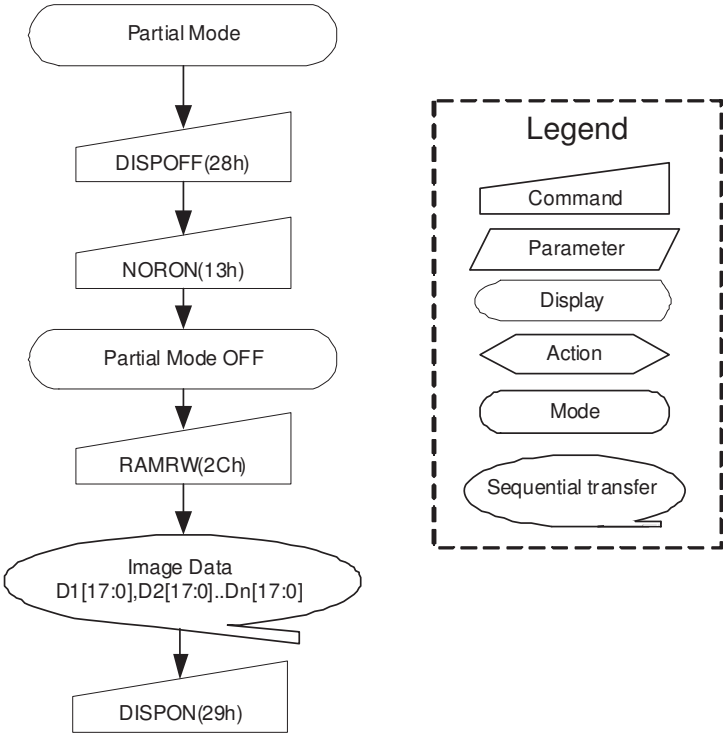
| Status | Default Value | |
|---|---|---|
| | SR [15:0] | ER [15:0] |
| Power On Sequence | 16'h0000h | 16'h013Fh |
| SW Reset | 16'h 0000h | 16'h 013Fh |
| HW Reset | 16'h 0000h | 16'h 013Fh |

**Flow Chart**

1. To Enter Partial Mode




2. To Leave Partial Mode



## 8.2.26. Vertical Scrolling Definition (33h)

| 33h | VSCRDEF (Vertical Scrolling Definition) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33h |
| 1st Parameter | 1 | ↑ | 1 | XX | TFA [15:8] | | | | | | | | 00 |
| 2nd Parameter | 1 | ↑ | 1 | XX | TFA [7:0] | | | | | | | | 00 |
| 3rd Parameter | 1 | ↑ | 1 | XX | VSA [15:8] | | | | | | | | 01 |
| 4th Parameter | 1 | ↑ | 1 | XX | VSA [7:0] | | | | | | | | 40 |
| 5th Parameter | 1 | ↑ | 1 | XX | BFA [15:8] | | | | | | | | 00 |
| 6th Parameter | 1 | ↑ | 1 | XX | BFA [7:0] | | | | | | | | 00 |

Description

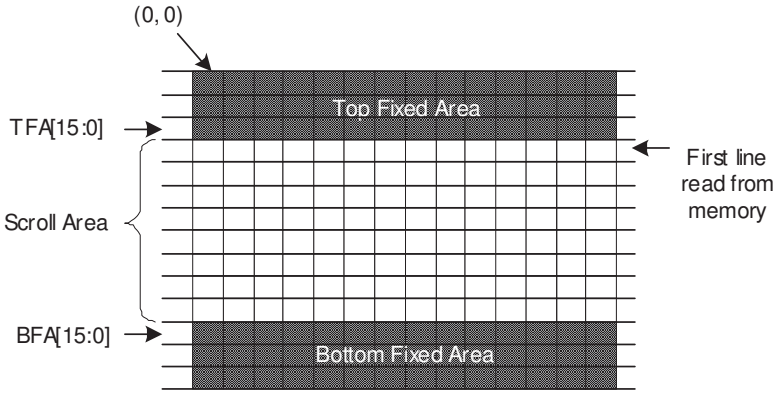
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

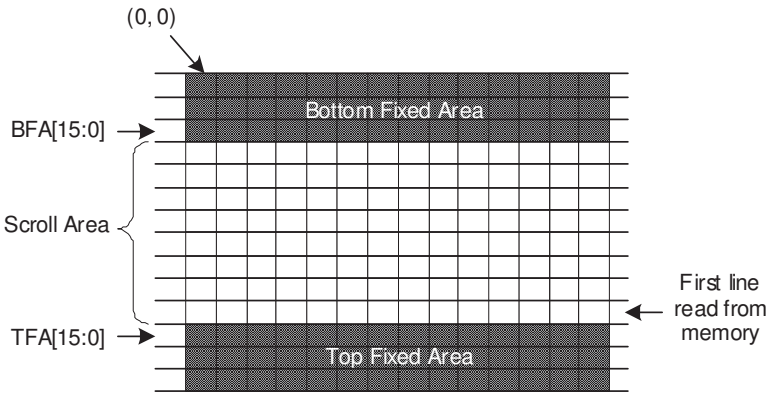



When MADCTL B4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).




X = Don't care

**Restriction**

**Register Availability**

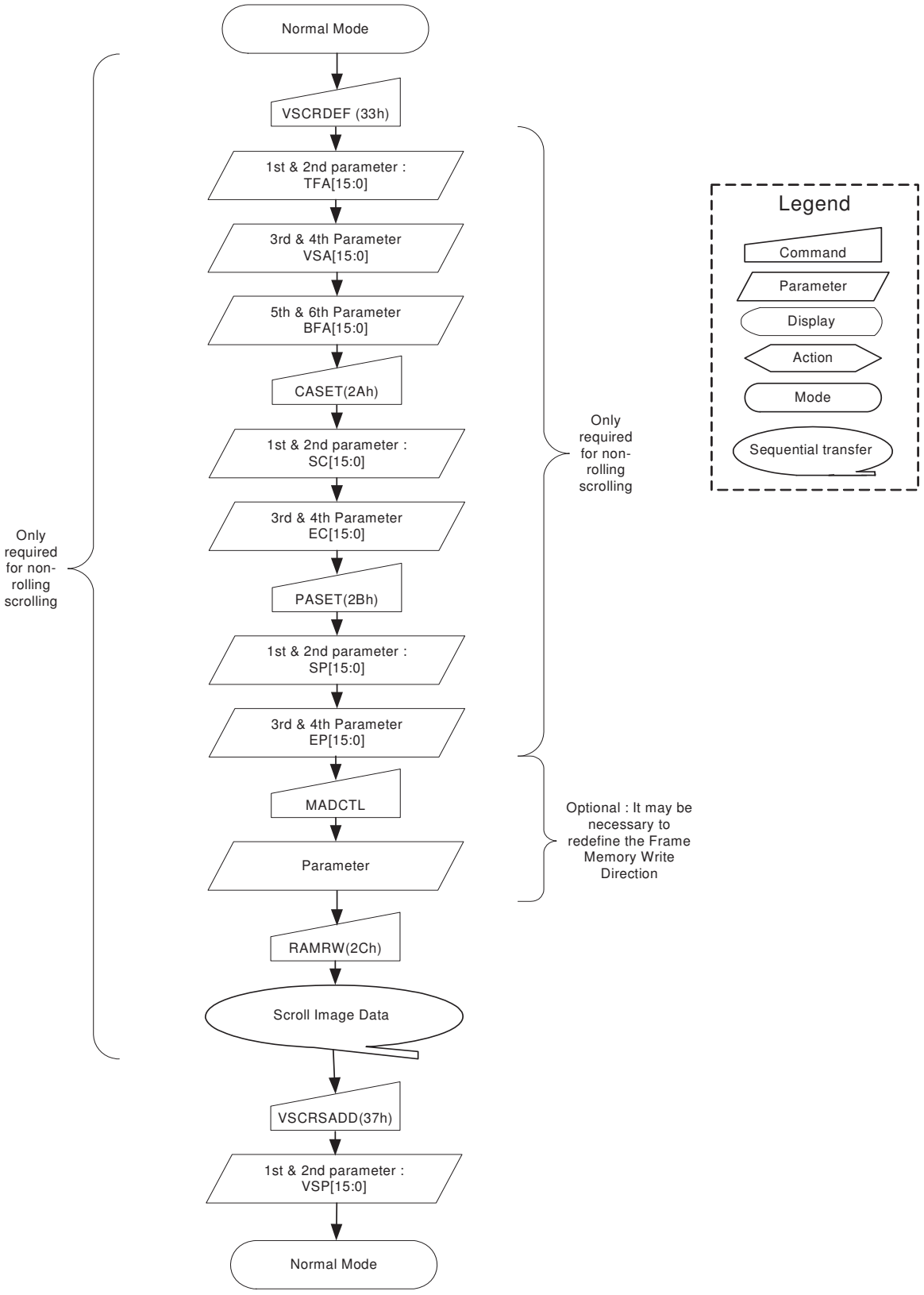
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | TFA [15:0] | VSA [15:0] | BFA [15:0] |
| Power On Sequence | 16'h0000h | 16'h0140h | 16'h0000h |
| SW Reset | 16'h0000h | 16'h0140h | 16'h0000h |
| HW Reset | 16'h0000h | 16'h0140h | 16'h0000h |

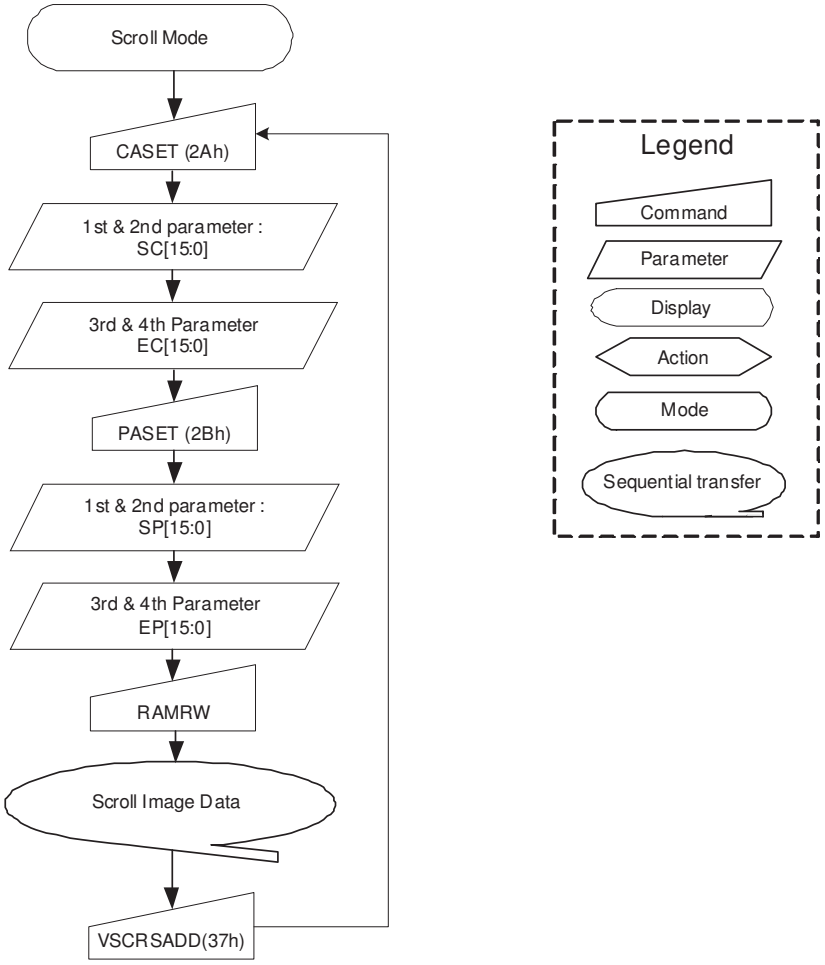
Flow Chart

1. To enter Vertical Scroll Mode :

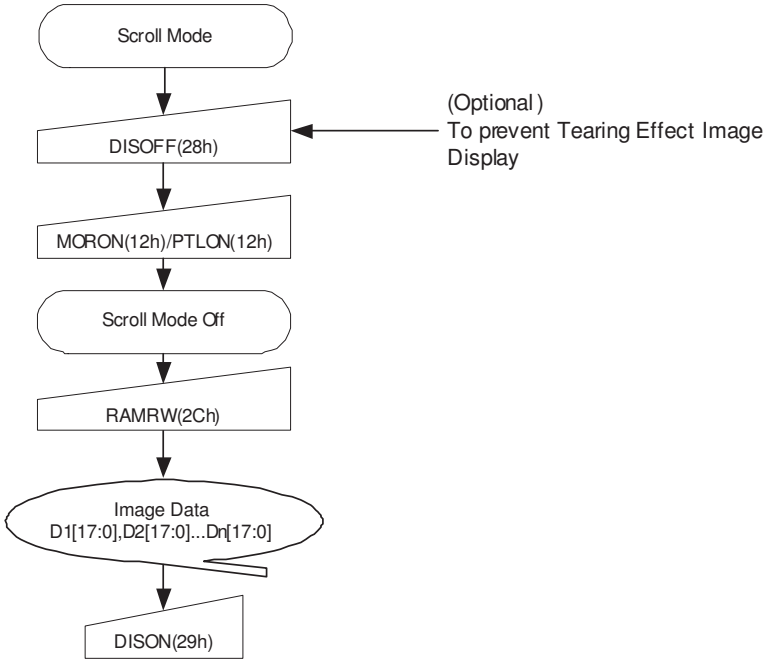



*Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.*

2. Continuous Scroll :




3.To Leave Vertical Scroll Mode:




*Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.*

## 8.2.27. Tearing Effect Line OFF (34h)

| 34h | TEOFF (Tearing Effect Line OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34h |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.<br>X = Don't care. | | | | | | | | | | | | |
| Restriction | This command has no effect when Tearing Effect output is already OFF. | | | | | | | | | | | | |

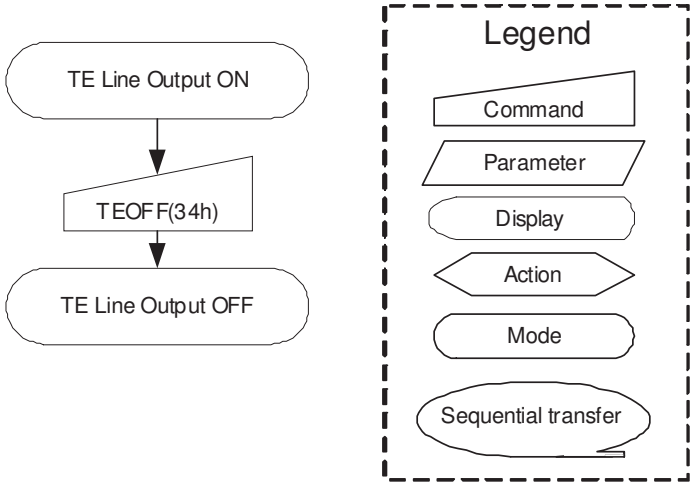
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | OFF |
| SW Reset | OFF |
| HW Reset | OFF |

Flow Chart



## 8.2.28. Tearing Effect Line ON (35h)

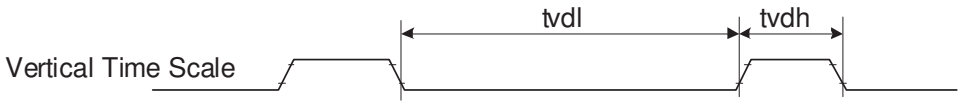
| 35h | TEON (Tearing Effect Line ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35h |
| Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M | 00 |

**Description**

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

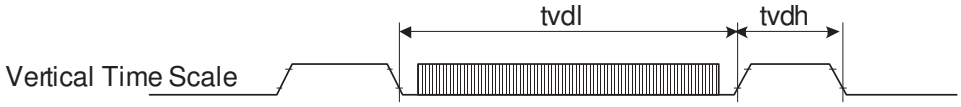
When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:




When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:




Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

**Restriction**

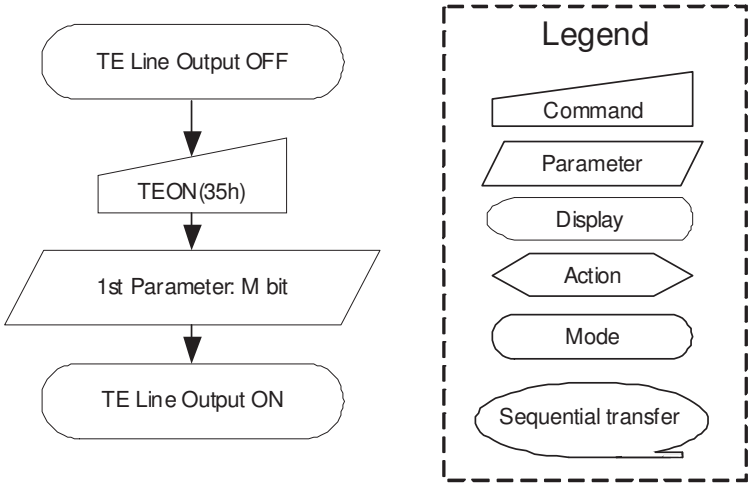
This command has no effect when Tearing Effect output is already ON

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | OFF |
| SW Reset | OFF |
| HW Reset | OFF |

| | |
|---|---|
| Flow Chart |  |

## 8.2.29. Memory Access Control (36h)

| 36h | MADCTL (Memory Access Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36h |
| Parameter | 1 | 1 | ↑ | XX | MY | MX | MV | ML | BGR | MH | 0 | 0 | 00 |

Description

This command defines read/write scanning direction of frame memory.

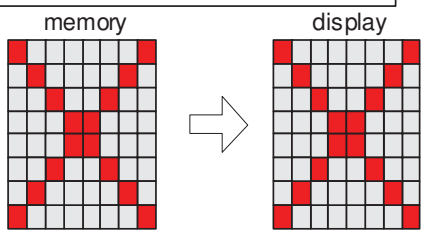
This command makes no change on the other driver status.

| Bit | Name | Description |
|---|---|---|
| MY | Row Address Order | These 3 bits control MCU to memory write/read direction. |
| MX | Column Address Order | |
| MV | Row / Column Exchange | |
| ML | Vertical Refresh Order | LCD vertical refresh direction control. |
| BGR | RGB-BGR Order | Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) |
| MH | Horizontal Refresh ORDER | LCD horizontal refreshing direction control. |

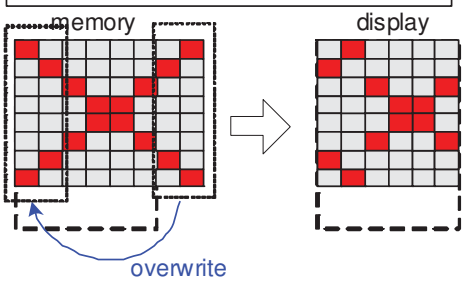
*Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.*

X = Don't care.

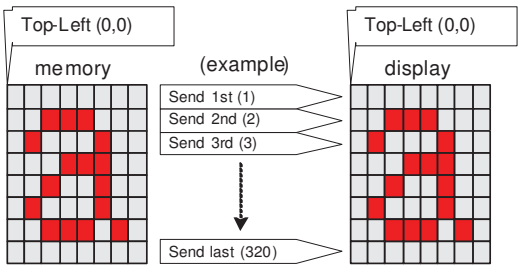
MV(Vertical refresh order bit)="0"



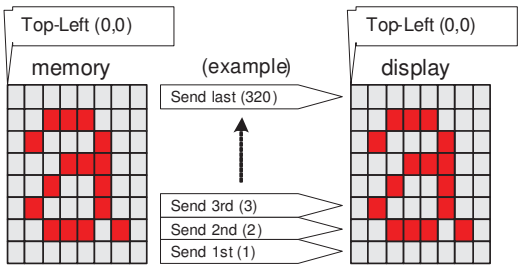

MV(Vertical refresh order bit)="1"



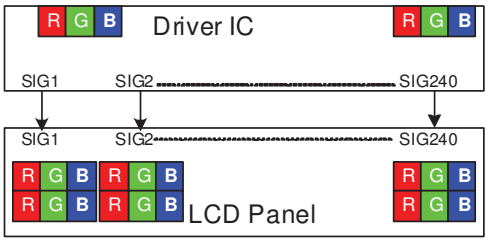

ML(Vertical refresh order bit)="0"



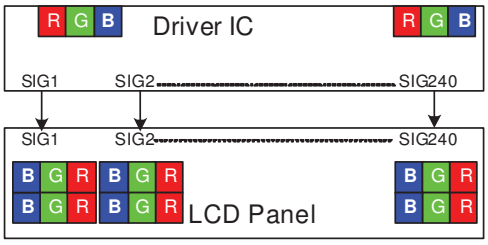

ML(Vertical refresh order bit)="1"

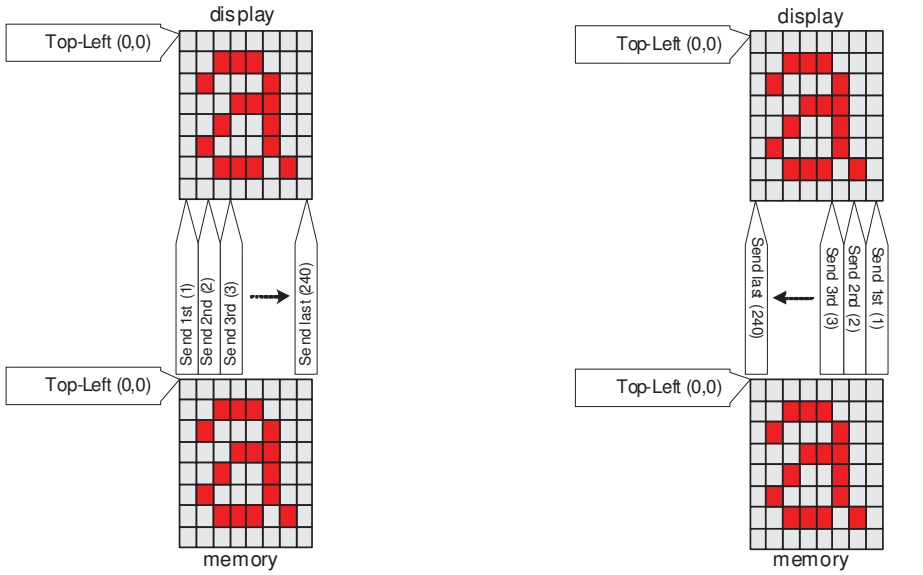
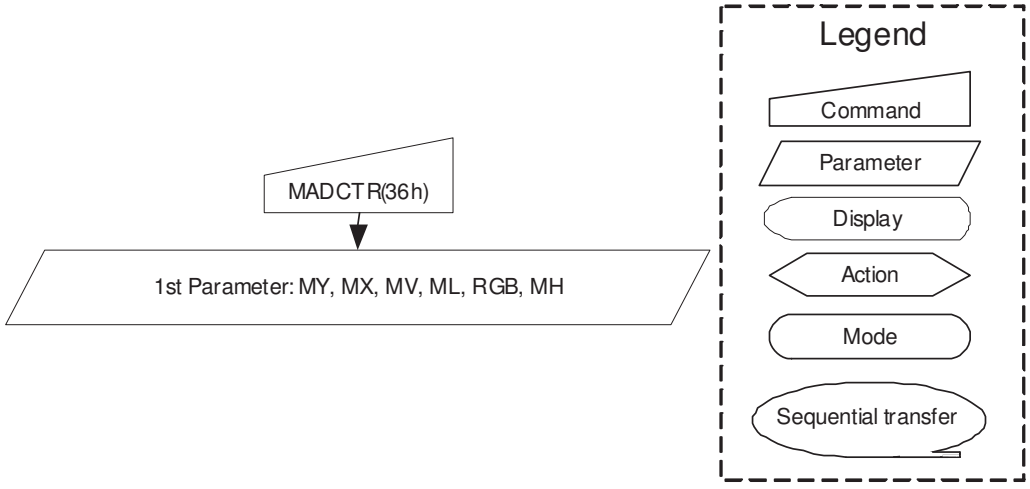



BGR(RGB-BGR Order control bit)="0"




BGR(RGB-BGR Order control bit)="1"



| | |
|---|---|
| | MH(Horizontal refresh order control bit)="0" / MH(Horizontal refresh order control bit)="1"<br>  <br><br>Note: Top-Left (0,0) means a physical memory location. |
| Restriction | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |
| Default | Status / Default Value<br>Power On Sequence / 8'h00h<br>SW Reset / No change<br>HW Reset / 8'h00h |
| Flow Chart |  <br> |

## 8.2.30. Vertical Scrolling Start Address (37h)

| 37h | VSCRSADD (Vertical Scrolling Start Address) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37h |
| 1st Parameter | 1 | ↑ | 1 | XX | VSP [15:8] | | | | | | | | 00 |
| 2nd Parameter | 1 | ↑ | 1 | XX | VSP [7:0] | | | | | | | | 00 |

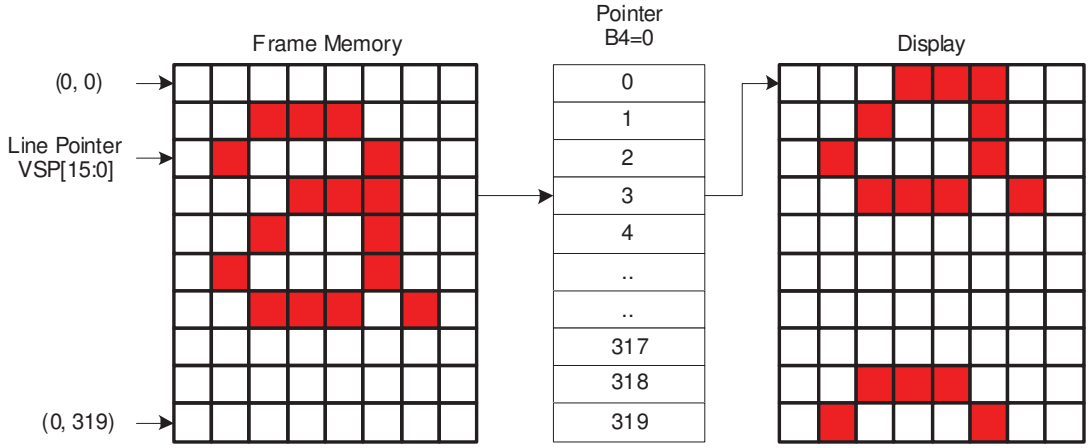
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

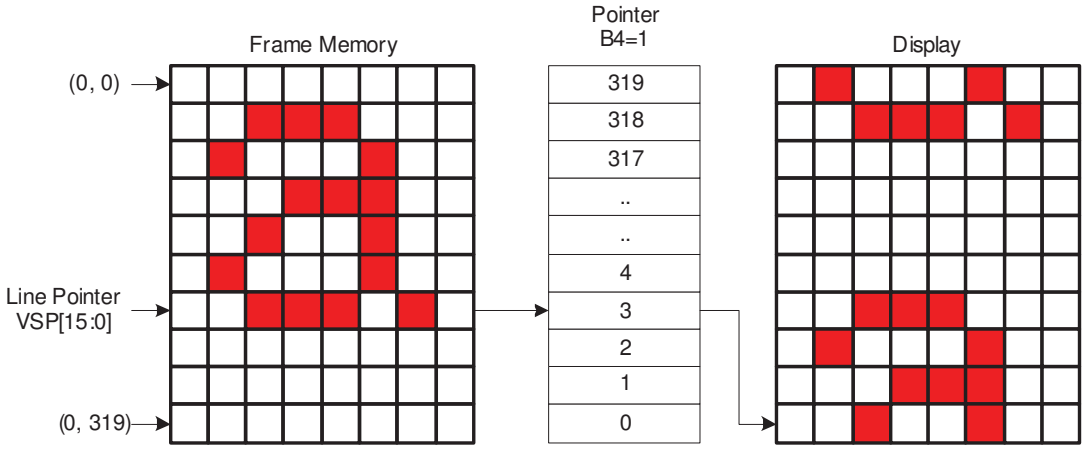
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.




When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.




*Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.*

*(2) This command is ignored when the ILI9341 enters Partial mode.*

X = Don't care

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register<br>Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

## 8.2.31. Idle Mode OFF (38h)

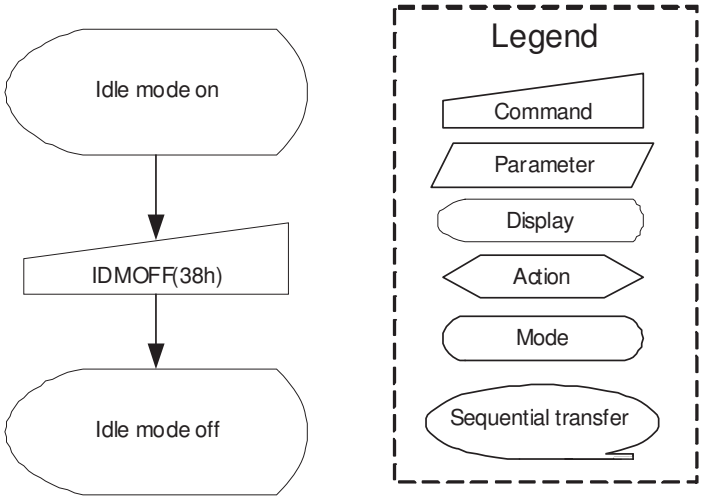
| 38h | IDMOFF (Idle Mode OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38h |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command is used to recover from Idle mode on.<br>In the idle off mode, LCD can display maximum 262,144 colors.<br>X = Don't care. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in idle off mode. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Idle mode OFF |
| SW Reset | Idle mode OFF |
| HW Reset | Idle mode OFF |

Flow Chart



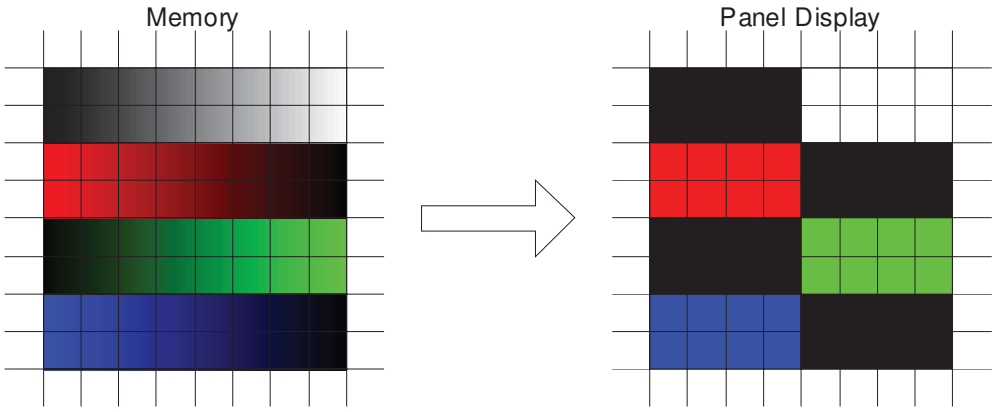
## 8.2.32. Idle Mode ON (39h)

| 39h | IDMON (Idle Mode ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39h |
| Parameter | No Parameter | | | | | | | | | | | | |

**Description**

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.




| Memory Contents vs. Display Color | | | |
|---|---|---|---|
| | $R_5\ R_4\ R_3\ R_2\ R_1\ R_0$ | $G_5\ G_4\ G_3\ G_2\ G_1\ G_0$ | $B_5\ B_4\ B_3\ B_2\ B_1\ B_0$ |
| Black | 0XXXXX | 0XXXXX | 0XXXXX |
| Blue | 0XXXXX | 0XXXXX | 1XXXXX |
| Red | 1XXXXX | 0XXXXX | 0XXXXX |
| Magenta | 1XXXXX | 0XXXXX | 1XXXXX |
| Green | 0XXXXX | 1XXXXX | 0XXXXX |
| Cyan | 0XXXXX | 1XXXXX | 1XXXXX |
| Yellow | 1XXXXX | 1XXXXX | 0XXXXX |
| White | 1XXXXX | 1XXXXX | 1XXXXX |

X = Don't care.

**Restriction**

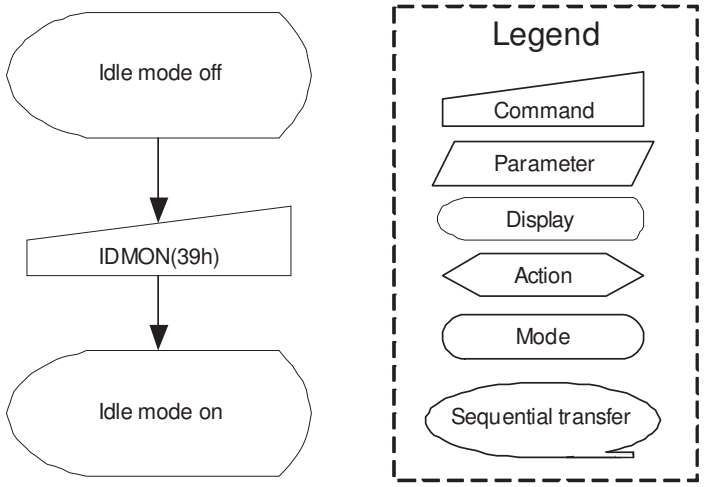
This command has no effect when module is already in idle off mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Idle mode OFF |
| SW Reset | Idle mode OFF |
| HW Reset | Idle mode OFF |

| | |
|---|---|
| Flow Chart |  |

## 8.2.33. COLMOD: Pixel Format Set (3Ah)

| 3Ah | PIXSET (Pixel Format Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3Ah |
| Parameter | 1 | 1 | ↑ | XX | 0 | DPI [2:0] | | | 0 | DBI [2:0] | | | 66 |

**Description**

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

| DPI [2:0] | | | RGB Interface Format |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 16 bits / pixel |
| 1 | 1 | 0 | 18 bits / pixel |
| 1 | 1 | 1 | Reserved |

| DBI [2:0] | | | MCU Interface Format |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 16 bits / pixel |
| 1 | 1 | 0 | 18 bits / pixel |
| 1 | 1 | 1 | Reserved |

If using RGB Interface must selection serial interface.

X = Don't care

**Restriction**

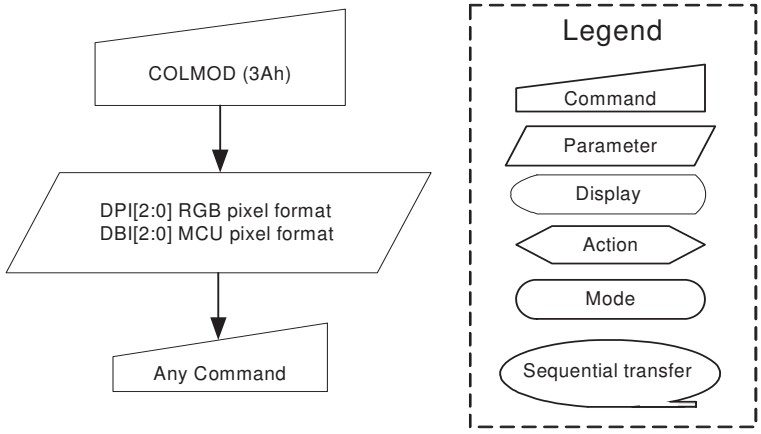
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | DPI [2:0] | DBI [2:0] |
| Power On Sequence | 3'b110 | 3'b110 |
| SW Reset | No Change | No Change |
| HW Reset | 3'b110 | 3'b110 |

**Flow Chart**



## 8.2.34. Write_Memory_Continue (3Ch)

| 3Ch | Write_Memory_Continue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3Ch |
| 1st Parameter | 1 | 1 | ↑ | D1 [17..8] | D1 [7] | D1 [6] | D1 [5] | D1 [4] | D1 [3] | D1 [2] | D1 [1] | D1 [0] | 000 3FF |
| Xth Parameter | 1 | 1 | ↑ | Dx [17..8] | Dx [7] | Dx [6] | Dx [5] | Dx [4] | Dx [3] | Dx [2] | Dx [1] | Dx [0] | 000 3FF |
| Nth Parameter | 1 | 1 | ↑ | Dn [17..8] | Dn [7] | Dn [6] | Dn [5] | Dn [4] | Dn [3] | Dn [2] | Dn [1] | Dn [0] | 000 3FF |

**Description**

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

**If set_address_mode B5 = 0:**

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

**If set_address_mode B5 = 1:**

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Sending any other command can stop frame Write.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=1

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

**Restriction**

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

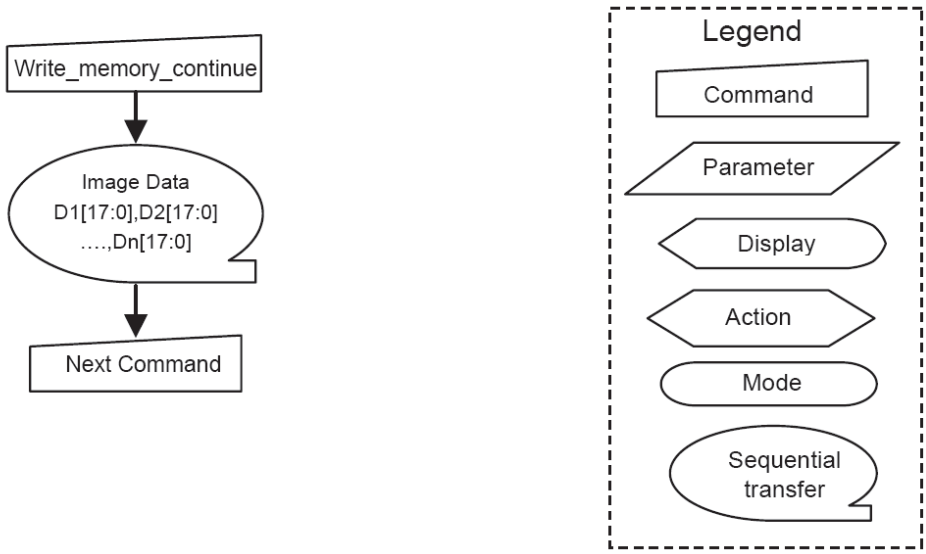
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | No |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Random value |
| SW Reset | No change |
| HW Reset | No change |

**Flow Chart**



## 8.2.35. Read_Memory_Continue (3Eh)

| 3Eh | Read_Memory_Continue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3Eh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | D1 [17..8] | D1 [7] | D1 [6] | D1 [5] | D1 [4] | D1 [3] | D1 [2] | D1 [1] | D1 [0] | 000 3FF |
| xst Parameter | 1 | ↑ | 1 | Dx [17..8] | Dx [7] | Dx [6] | Dx [5] | Dx [4] | Dx [3] | Dx [2] | Dx [1] | Dx [0] | 000 3FF |
| Nst Parameter | 1 | ↑ | 1 | Dn [17..8] | Dn [7] | Dn [6] | Dn [5] | Dn [4] | Dn [3] | Dn [2] | Dn [1] | Dn [0] | 000 3FF |

**Description**

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command.

If set_address_mode B5 = 0:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.

If set_address_mode B5 = 1:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.

This command makes no change to the other driver status.

**Restriction**

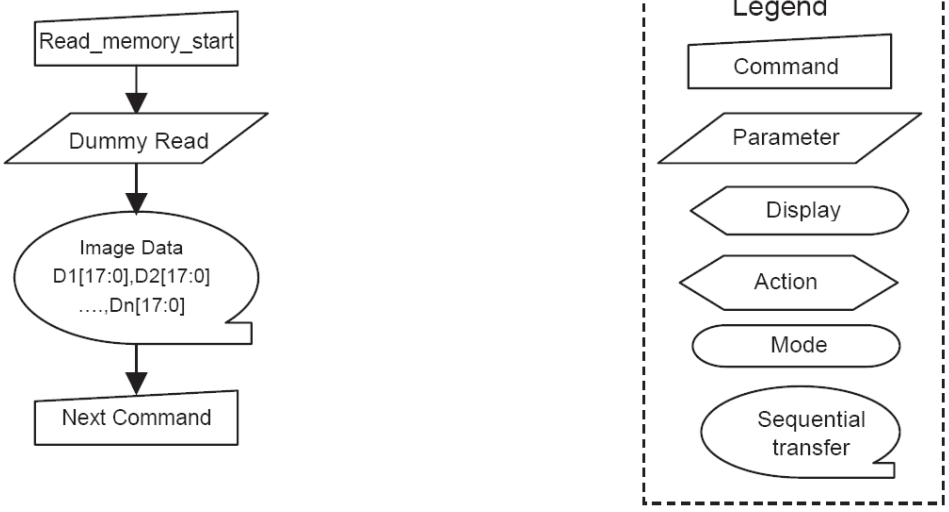
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Random data |
| SW Reset | No change |
| HW Reset | No change |

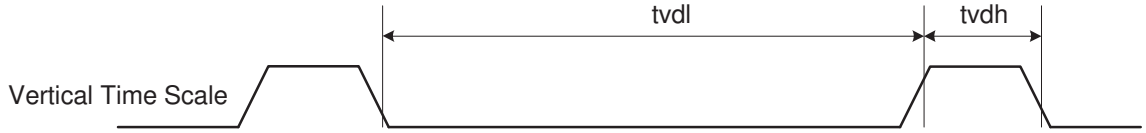
| | |
|---|---|
| Flow Chart |  |

## 8.2.36. Set_Tear_Scanline (44h)

| 44h | Set_Tear_Scanline | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STS [8] | 00 |
| 2nd Parameter | 1 | 1 | ↑ | XX | STS [7] | STS [6] | STS [5] | STS [4] | STS [3] | STS [2] | STS [1] | STS [0] | 00 |

**Description**

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.




Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

**Restriction**

-

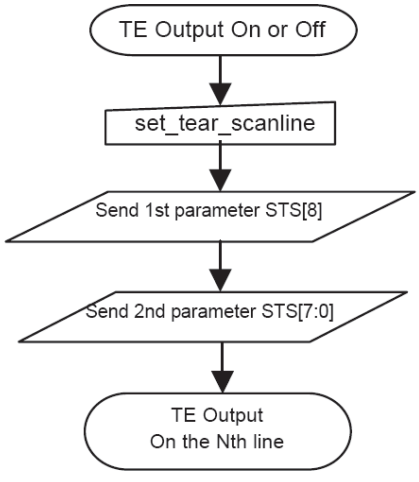
**Register Availability**

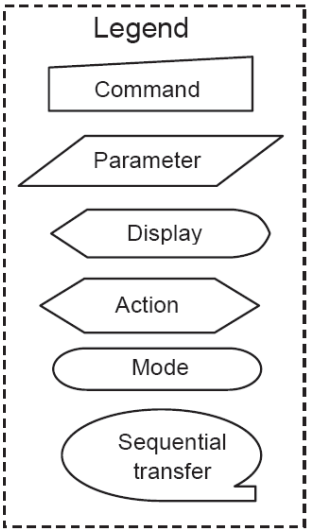
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | STS [8:0]=0000h |
| SW Reset | STS [8:0]=0000h |
| HW Reset | STS [8:0]=0000h |

**Flow Chart**



## 8.2.37. Get_Scanline (45h)

| 45h | Get_Scanline | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | GTS [9] | GTS [8] | 00 |
| 3rd Parameter | 1 | ↑ | 1 | XX | GTS [7] | GTS [6] | GTS [5] | GTS [4] | GTS [3] | GTS [2] | GTS [1] | GTS [0] | 00 |

**Description**

The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.

**Restriction**

None

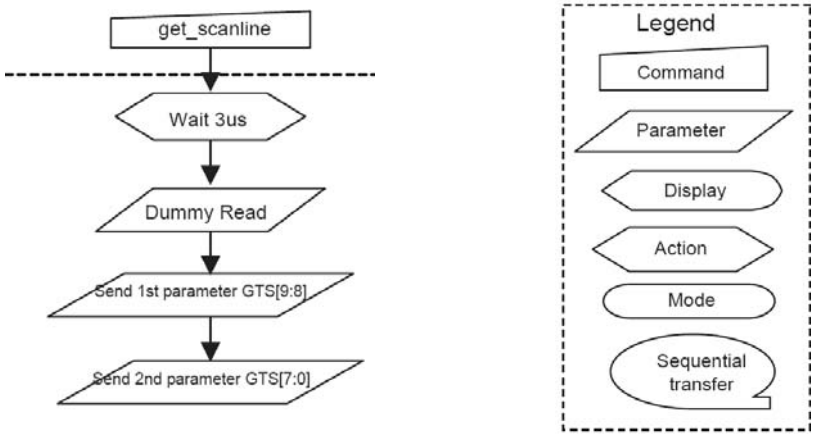
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | GTS [9:0] |
| Power On Sequence | GTS [9:0]=0000h |
| SW Reset | GTS [9:0]=0000h |
| HW Reset | GTS [9:0]=0000h |

**Flow Chart**



## 8.2.38. Write Display Brightness (51h)

| 51h | WRDISBV (Write Display Brightness) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51h |
| Parameter | 1 | 1 | ↑ | XX | DBV[7] | DBV[6] | DBV[5] | DBV[4] | DBV[3] | DBV[2] | DBV[1] | DBV[0] | 00 |
| Description | This command is used to adjust the brightness value of the display.<br>It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.<br>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. | | | | | | | | | | | | |
| Restriction | None | | | | | | | | | | | | |

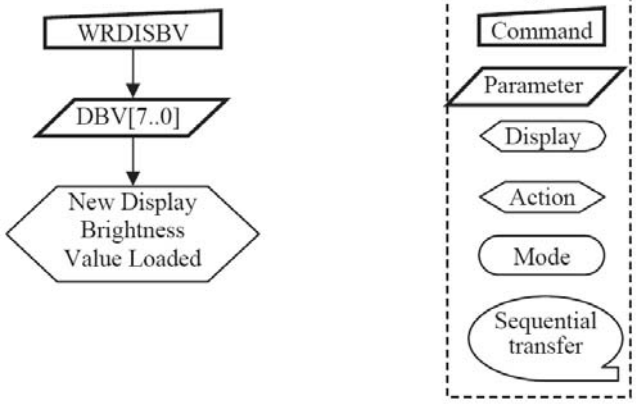
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| | DBV [7:0] |
| Power On Sequence | 8'h00h |
| SW Reset | 8'h00h |
| HW Reset | 8'h00h |

Flow Chart



## 8.2.39. Read Display Brightness (52h)

| 52h | RDDISBV (Read Display Brightness Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | DBV[7] | DBV[6] | DBV[5] | DBV[4] | DBV[3] | DBV[2] | DBV[1] | DBV[0] | 00 |

**Description**

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

**Restriction**

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

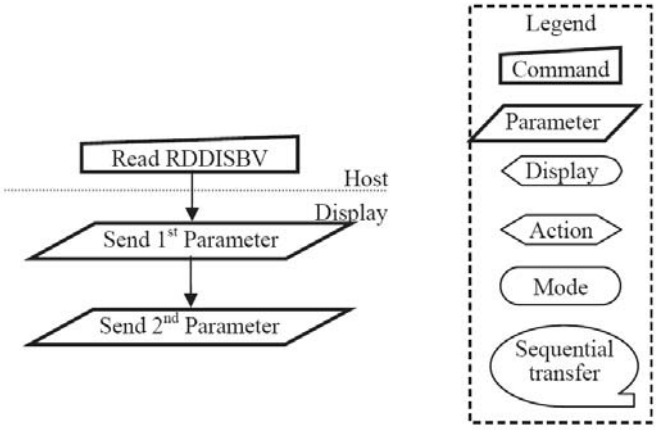
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | DBV [7:0] |
| Power On Sequence | 8'h00h |
| SW Reset | 8'h00h |
| HW Reset | 8'h00h |

**Flow Chart**



## 8.2.40. Write CTRL Display (53h)

| 53h | WRCTRLD (Write Control Display) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53h |
| Parameter | 1 | 1 | ↑ | XX | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | 00 |

**Description**

This command is used to control display brightness.

**BCTRL**: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off (Brightness registers are 00h, DBV[7..0])

1 = On (Brightness registers are active, according to the other parameters.)

**DD**: Display Dimming, only for manual brightness setting

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

**BL**: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low. )

1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1→ 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

**Restriction**

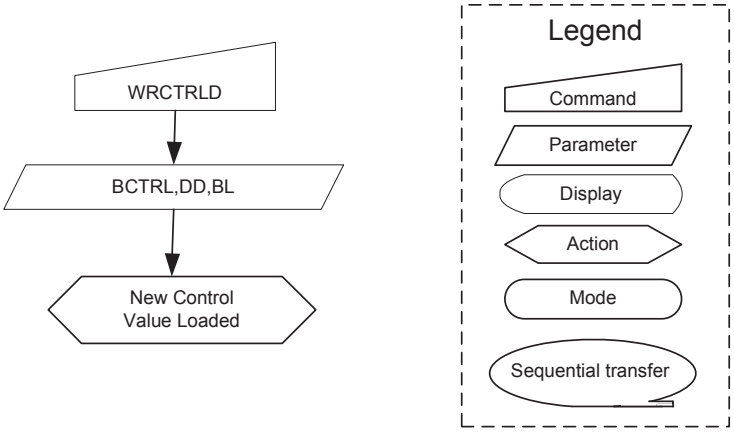
None

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | BCTRL | DD | BL |
| Power On Sequence | 1’b0 | 1’b0 | 1’b0 |
| SW Reset | 1’b0 | 1’b0 | 1’b0 |
| HW Reset | 1’b0 | 1’b0 | 1’b0 |

| | |
|---|---|
| Flow Chart |  |

## 8.2.41. Read CTRL Display (54h)

| 54h | RDCTRLD (Read Control Display) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| 2nd Parameter | 1 | ↑ | 1 | XX | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | 00 |

**Description**

This command is used to return brightness setting.

**BCTRL**: Brightness Control Block On/Off,

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)

**DD**: Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

**BL**: Backlight On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low. )

'1' = On

**Restriction**

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

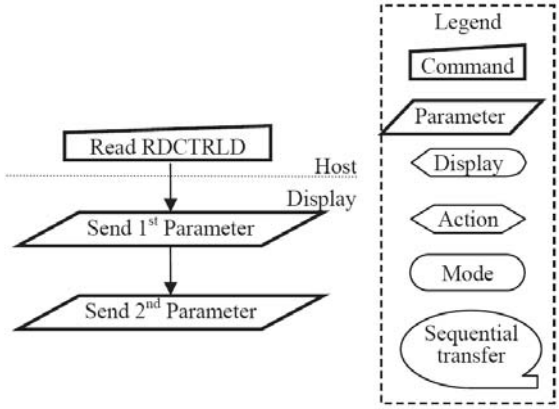
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | BCTRL | DD | BL |
| Power On Sequence | 1'b0 | 1'b0 | 1'b0 |
| SW Reset | 1'b0 | 1'b0 | 1'b0 |
| HW Reset | 1'b0 | 1'b0 | 1'b0 |

| | |
|---|---|
| Flow Chart |  |

## 8.2.42. Write Content Adaptive Brightness Control (55h)

| 55h | WRCABC (Write Content Adaptive Brightness Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55h |
| Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | C [1] | C [0] | 00 |

**Description**

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C [1:0] | Default Value |
|---|---|
| 2'b00 | Off |
| 2'b01 | User Interface Image |
| 2'b10 | Still Picture |
| 2'b11 | Moving Image |

**Restriction**

None

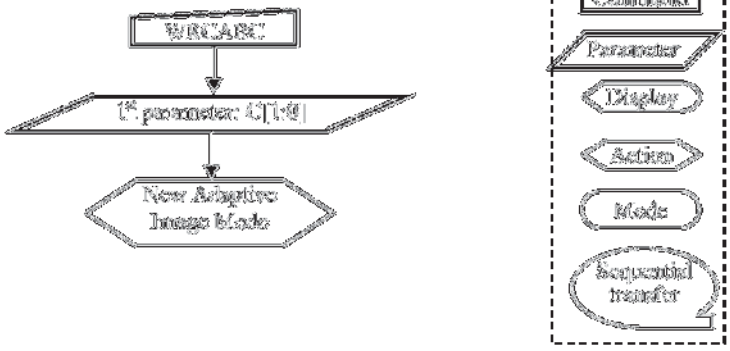
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | C [1:0]=00h |
| SW Reset | C [1:0]=00h |
| HW Reset | C [1:0]=00h |

**Flow Chart**



## 8.2.43. Read Content Adaptive Brightness Control (56h)

| 56h | RDCABC (Read Content Adaptive Brightness Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| 2nd Parameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | C [1] | C [0] | 00 |

**Description**

This command is used to read the settings for image content based adaptive brightness control functionality.

It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C [1:0] | Default Value |
|---|---|
| 2'b00 | Off |
| 2'b01 | User Interface Image |
| 2'b10 | Still Picture |
| 2'b11 | Moving Image |

**Restriction**

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

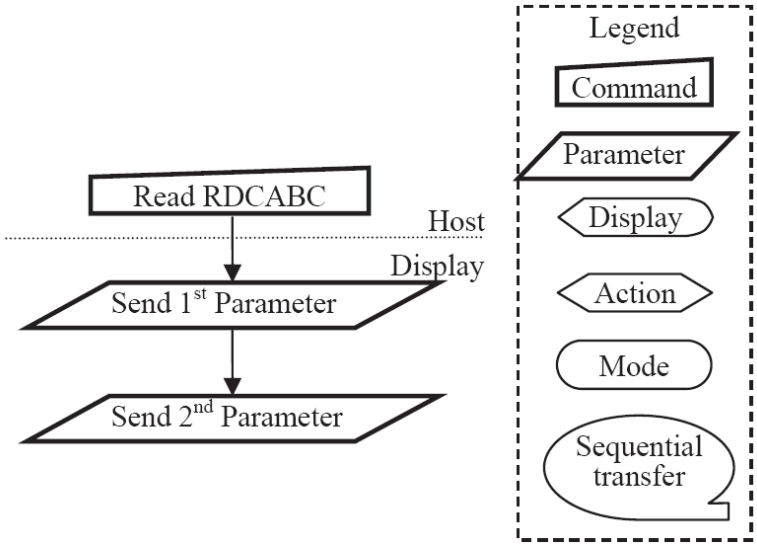
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | C [1:0]=00h |
| SW Reset | C [1:0]=00h |
| HW Reset | C [1:0]=00h |

**Flow Chart**



## 8.2.44. Write CABC Minimum Brightness (5Eh)

| 5Eh | Backlight Control 1 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5Eh |
| Parameter | 1 | 1 | ↑ | XX | CMB [7] | CMB [6] | CMB [5] | CMB [4] | CMB [3] | CMB [2] | CMB [1] | CMB [0] | 00 |

**Description**

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | CMB [7:0] |
| Power On Sequence | 8'h00h |
| SW Reset | No Change |
| HW Reset | 8'h00h |

## 8.2.45. Read CABC Minimum Brightness (5Fh)

| 5Fh | Backlight Control 1 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5Fh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | CMB [7] | CMB [6] | CMB [5] | CMB [4] | CMB [3] | CMB [2] | CMB [1] | CMB [0] | 00 |

**Description**

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | CMB [7:0] |
| Power On Sequence | 8'h00h |
| SW Reset | No Change |
| HW Reset | 8'h00h |

## 8.2.46. Read ID1 (DAh)

| DAh | RDID1 (Read ID1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DAh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | ID1 [7:0] | | | | | | | | XX |
| Description | This read byte identifies the LCD module's manufacturer ID and it is specified by User<br>The 1st parameter is dummy data.<br>The 2nd parameter is LCD module's manufacturer ID.<br>X = Don't care | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

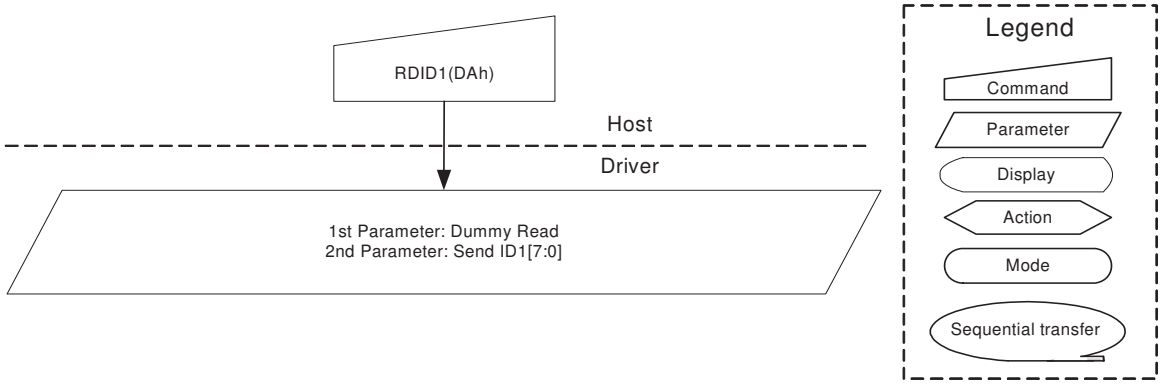
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value (Before MTP program) | Default Value (After MTP program) |
|---|---|---|
| Power On Sequence | 8'h00h | MTP value |
| SW Reset | 8'h00h | MTP value |
| HW Reset | 8'h00h | MTP value |

Flow Chart



## 8.2.47. Read ID2 (DBh)

| DBh | RDID2 (Read ID2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DBh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | 1 | ID2 [6:0] | | | | | | | XX |
| Description | This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.<br>The 1st parameter is dummy data.<br>The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.<br>The ID2 can be programmed by MTP function.<br>X = Don't care | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

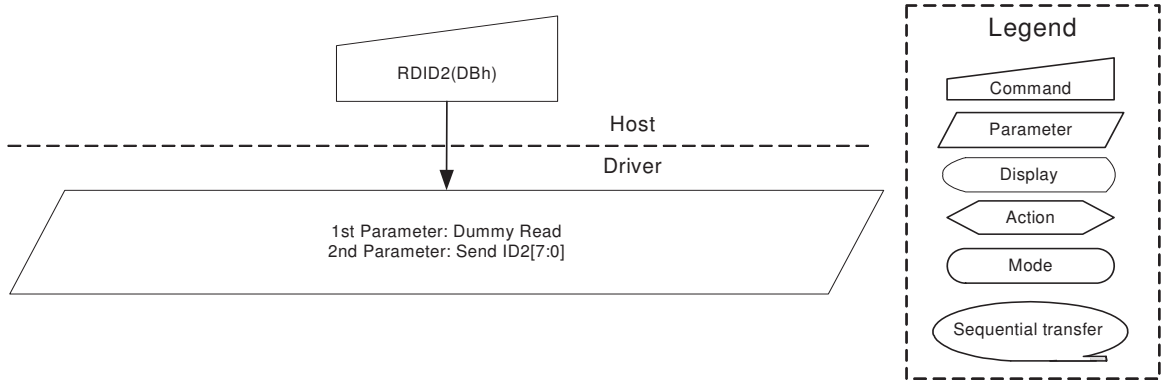
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value (Before MTP program) | Default Value (After MTP program) |
|---|---|---|
| Power On Sequence | 8'h80h | MTP value |
| SW Reset | 8'h80h | MTP value |
| HW Reset | 8'h80h | MTP value |

Flow Chart



## 8.2.48. Read ID3 (DCh)

| DCh | RDID3 (Read ID3) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DCh |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2nd Parameter | 1 | ↑ | 1 | XX | ID3 [7:0] | | | | | | | | XX |
| Description | This read byte identifies the LCD module/driver and It is specified by User.<br>The 1st parameter is dummy data.<br>The 2nd parameter is LCD module/driver ID.<br>The ID3 can be programmed by MTP function.<br>X = Don't care | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

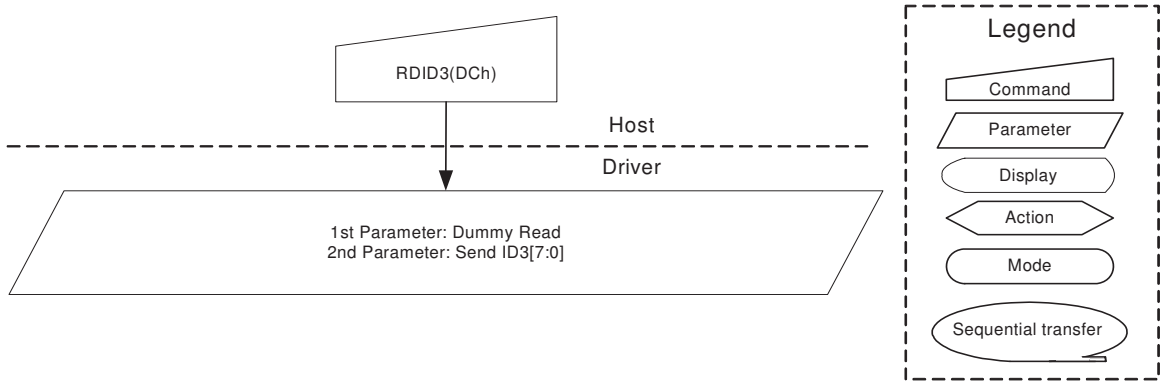
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value (Before MTP program) | Default Value (After MTP program) |
|---|---|---|
| Power On Sequence | 8'h00h | MTP value |
| SW Reset | 8'h00h | MTP value |
| HW Reset | 8'h00h | MTP value |

Flow Chart



# 8.3. Description of Level 2 Command

## 8.3.1. RGB Interface Signal Control (B0h)

| B0h | IFMODE (Interface Mode Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h |
| Parameter | 1 | 1 | ↑ | XX | ByPass_MODE | RCM [1] | RCM [0] | 0 | VSPL | HSPL | DPL | EPL | 40 |

**Description**

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

**EPL**: DE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface)

**DPL**: DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time)

**HSPL**: HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

**VSPL**: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

**RCM [1:0]:** RGB interface selection (refer to the RGB interface section).

**ByPass_MODE**: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.

| ByPass_MODE | Display Data Path |
|---|---|
| 0 | Direct to Shift Register (**default**) |
| 1 | Memory |

**Restriction**

EXTC should be high to enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

**Default**

| Status | Default Value | | | | | |
|---|---|---|---|---|---|---|
| | ByPass_MODE | RCM [1:0] | VSPL | HSPL | DPL | EPL |
| Power ON Sequence | 1'b0 | 2'b10 | 1'b0 | 1'b0 | 1'b0 | 1'b1 |
| SW Reset | 1'b0 | 2'b10 | 1'b0 | 1'b0 | 1'b0 | 1'b1 |
| HW Reset | 1'b0 | 2'b10 | 1'b0 | 1'b0 | 1'b0 | 1'b1 |

## 8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

| B1h | FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors)) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVA [1:0] | | 00 |
| 2nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNA [4:0] | | | | | 1B |

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc : internal oscillator frequency

Clocks per line : RTNA setting

Division ratio : DIVA setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

| RTNA [4:0] | | | | | Frame Rate (Hz) |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 119 |
| 1 | 0 | 0 | 0 | 1 | 112 |
| 1 | 0 | 0 | 1 | 0 | 106 |
| 1 | 0 | 0 | 1 | 1 | 100 |
| 1 | 0 | 1 | 0 | 0 | 95 |
| 1 | 0 | 1 | 0 | 1 | 90 |
| 1 | 0 | 1 | 1 | 0 | 86 |
| 1 | 0 | 1 | 1 | 1 | 83 |

| RTNA [4:0] | | | | | Frame Rate (Hz) |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 79 |
| 1 | 1 | 0 | 0 | 1 | 76 |
| 1 | 1 | 0 | 1 | 0 | 73 |
| 1 | 1 | 0 | 1 | 1 | 70(default) |
| 1 | 1 | 1 | 0 | 0 | 68 |
| 1 | 1 | 1 | 0 | 1 | 65 |
| 1 | 1 | 1 | 0 | 1 | 63 |
| 1 | 1 | 1 | 1 | 1 | 61 |

**DIVA [1:0]** : division ratio for internal clocks when Normal mode.

| DIVA [1:0] | | Division Ratio |
|---|---|---|
| 0 | 0 | fosc |
| 0 | 1 | fosc / 2 |
| 1 | 0 | fosc / 4 |
| 1 | 1 | fosc / 8 |

**RTNA [4:0]** : RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

| RTNA [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 1 | Setting prohibited |
| 0 | 0 | 0 | 1 | 0 | Setting prohibited |
| 0 | 0 | 0 | 1 | 1 | Setting prohibited |
| 0 | 0 | 1 | 0 | 0 | Setting prohibited |
| 0 | 0 | 1 | 0 | 1 | Setting prohibited |
| 0 | 0 | 1 | 1 | 0 | Setting prohibited |
| 0 | 0 | 1 | 1 | 1 | Setting prohibited |
| 0 | 1 | 0 | 0 | 0 | Setting prohibited |
| 0 | 1 | 0 | 0 | 1 | Setting prohibited |
| 0 | 1 | 0 | 1 | 0 | Setting prohibited |

| RTNA [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | Setting prohibited |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited |
| 0 | 1 | 1 | 0 | 1 | Setting prohibited |
| 0 | 1 | 1 | 1 | 0 | Setting prohibited |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited |
| 1 | 0 | 0 | 0 | 0 | 16 clocks |
| 1 | 0 | 0 | 0 | 1 | 17 clocks |
| 1 | 0 | 0 | 1 | 0 | 18 clocks |
| 1 | 0 | 0 | 1 | 1 | 19 clocks |
| 1 | 0 | 1 | 0 | 0 | 20 clocks |
| 1 | 0 | 1 | 0 | 1 | 21 clocks |

| RTNA [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 22 clocks |
| 1 | 0 | 1 | 1 | 1 | 23 clocks |
| 1 | 1 | 0 | 0 | 0 | 24 clocks |
| 1 | 1 | 0 | 0 | 1 | 25 clocks |
| 1 | 1 | 0 | 1 | 0 | 26 clocks |
| 1 | 1 | 0 | 1 | 1 | 27 clocks |
| 1 | 1 | 1 | 0 | 0 | 28 clocks |
| 1 | 1 | 1 | 0 | 1 | 29 clocks |
| 1 | 1 | 1 | 1 | 0 | 30 clocks |
| 1 | 1 | 1 | 1 | 1 | 31 clocks |

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register<br>Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIVA [1:0]</th><th>RTNA [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
</table>
</td></tr>
</table>

## 8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

| B2h | FRMCTR2 (Frame Rate Control (In Idle Mode / 8l colors)) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVB [1:0] | | 00 |
| 2ndParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNB [4:0] | | | | | 1B |

Description

Formula to calculate frame frequency

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Idle mode at MCU interface.

fosc : internal oscillator frequency

Clocks per line : RTNB setting

Division ratio : DIVB setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

| RTNB [4:0] | | | | | Frame Rate (Hz) |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 119 |
| 1 | 0 | 0 | 0 | 1 | 112 |
| 1 | 0 | 0 | 1 | 0 | 106 |
| 1 | 0 | 0 | 1 | 1 | 100 |
| 1 | 0 | 1 | 0 | 0 | 95 |
| 1 | 0 | 1 | 0 | 1 | 90 |
| 1 | 0 | 1 | 1 | 0 | 86 |
| 1 | 0 | 1 | 1 | 1 | 83 |

| RTNB [4:0] | | | | | Frame Rate (Hz) |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 79 |
| 1 | 1 | 0 | 0 | 1 | 76 |
| 1 | 1 | 0 | 1 | 0 | 73 |
| 1 | 1 | 0 | 1 | 1 | 70(default) |
| 1 | 1 | 1 | 0 | 0 | 68 |
| 1 | 1 | 1 | 0 | 1 | 65 |
| 1 | 1 | 1 | 0 | 1 | 63 |
| 1 | 1 | 1 | 1 | 1 | 61 |

**DIVB [1:0]**: division ratio for internal clocks when Idle mode.

| DIVB [1:0] | | Division Ratio |
|---|---|---|
| 0 | 0 | fosc |
| 0 | 1 | fosc / 2 |
| 1 | 0 | fosc / 4 |
| 1 | 1 | fosc / 8 |

**RTNB [4:0]**: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

| RTNB [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 1 | Setting prohibited |
| 0 | 0 | 0 | 1 | 0 | Setting prohibited |
| 0 | 0 | 0 | 1 | 1 | Setting prohibited |
| 0 | 0 | 1 | 0 | 0 | Setting prohibited |
| 0 | 0 | 1 | 0 | 1 | Setting prohibited |
| 0 | 0 | 1 | 1 | 0 | Setting prohibited |
| 0 | 0 | 1 | 1 | 1 | Setting prohibited |
| 0 | 1 | 0 | 0 | 0 | Setting prohibited |
| 0 | 1 | 0 | 0 | 1 | Setting prohibited |
| 0 | 1 | 0 | 1 | 0 | Setting prohibited |

| RTNB [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | Setting prohibited |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited |
| 0 | 1 | 1 | 0 | 1 | Setting prohibited |
| 0 | 1 | 1 | 1 | 0 | Setting prohibited |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited |
| 1 | 0 | 0 | 0 | 0 | 16 clocks |
| 1 | 0 | 0 | 0 | 1 | 17 clocks |
| 1 | 0 | 0 | 1 | 0 | 18 clocks |
| 1 | 0 | 0 | 1 | 1 | 19 clocks |
| 1 | 0 | 1 | 0 | 0 | 20 clocks |
| 1 | 0 | 1 | 0 | 1 | 21 clocks |

| RTNB [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 22 clocks |
| 1 | 0 | 1 | 1 | 1 | 23 clocks |
| 1 | 1 | 0 | 0 | 0 | 24 clocks |
| 1 | 1 | 0 | 0 | 1 | 25 clocks |
| 1 | 1 | 0 | 1 | 0 | 26 clocks |
| 1 | 1 | 0 | 1 | 1 | 27 clocks |
| 1 | 1 | 1 | 0 | 0 | 28 clocks |
| 1 | 1 | 1 | 0 | 1 | 29 clocks |
| 1 | 1 | 1 | 1 | 0 | 30 clocks |
| 1 | 1 | 1 | 1 | 1 | 31 clocks |

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register<br>Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIVB [1:0]</th><th>RTNB [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
</table>
</td></tr>
</table>

## 8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

| B3h | FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors)) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | DIVC [1:0] | | 00 |
| 2ndParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | RTNC [4:0] | | | | | 1B |

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

fosc : internal oscillator frequency

Clocks per line : RTNC setting

Division ratio : DIVC setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

| RTNC [4:0] | | | | | Frame Rate (Hz) |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 119 |
| 1 | 0 | 0 | 0 | 1 | 112 |
| 1 | 0 | 0 | 1 | 0 | 106 |
| 1 | 0 | 0 | 1 | 1 | 100 |
| 1 | 0 | 1 | 0 | 0 | 95 |
| 1 | 0 | 1 | 0 | 1 | 90 |
| 1 | 0 | 1 | 1 | 0 | 86 |
| 1 | 0 | 1 | 1 | 1 | 83 |

| RTNC [4:0] | | | | | Frame Rate (Hz) |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 79 |
| 1 | 1 | 0 | 0 | 1 | 76 |
| 1 | 1 | 0 | 1 | 0 | 73 |
| 1 | 1 | 0 | 1 | 1 | 70(default) |
| 1 | 1 | 1 | 0 | 0 | 68 |
| 1 | 1 | 1 | 0 | 1 | 65 |
| 1 | 1 | 1 | 0 | 1 | 63 |
| 1 | 1 | 1 | 1 | 1 | 61 |

**DIVC [1:0]**: division ratio for internal clocks when Partial mode.

| DIVC [1:0] | | Division Ratio |
|---|---|---|
| 0 | 0 | fosc |
| 0 | 1 | fosc / 2 |
| 1 | 0 | fosc / 4 |
| 1 | 1 | fosc / 8 |

**RTNC [4:0]**: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

| RTNC [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 1 | Setting prohibited |
| 0 | 0 | 0 | 1 | 0 | Setting prohibited |
| 0 | 0 | 0 | 1 | 1 | Setting prohibited |
| 0 | 0 | 1 | 0 | 0 | Setting prohibited |
| 0 | 0 | 1 | 0 | 1 | Setting prohibited |
| 0 | 0 | 1 | 1 | 0 | Setting prohibited |
| 0 | 0 | 1 | 1 | 1 | Setting prohibited |
| 0 | 1 | 0 | 0 | 0 | Setting prohibited |
| 0 | 1 | 0 | 0 | 1 | Setting prohibited |
| 0 | 1 | 0 | 1 | 0 | Setting prohibited |

| RTNC [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | Setting prohibited |
| 0 | 1 | 1 | 0 | 0 | Setting prohibited |
| 0 | 1 | 1 | 0 | 1 | Setting prohibited |
| 0 | 1 | 1 | 1 | 0 | Setting prohibited |
| 0 | 1 | 1 | 1 | 1 | Setting prohibited |
| 1 | 0 | 0 | 0 | 0 | 16 clocks |
| 1 | 0 | 0 | 0 | 1 | 17 clocks |
| 1 | 0 | 0 | 1 | 0 | 18 clocks |
| 1 | 0 | 0 | 1 | 1 | 19 clocks |
| 1 | 0 | 1 | 0 | 0 | 20 clocks |
| 1 | 0 | 1 | 0 | 1 | 21 clocks |

| RTNC [4:0] | | | | | Clock per Line |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 22 clocks |
| 1 | 0 | 1 | 1 | 1 | 23 clocks |
| 1 | 1 | 0 | 0 | 0 | 24 clocks |
| 1 | 1 | 0 | 0 | 1 | 25 clocks |
| 1 | 1 | 0 | 1 | 0 | 26 clocks |
| 1 | 1 | 0 | 1 | 1 | 27 clocks |
| 1 | 1 | 1 | 0 | 0 | 28 clocks |
| 1 | 1 | 1 | 0 | 1 | 29 clocks |
| 1 | 1 | 1 | 1 | 0 | 30 clocks |
| 1 | 1 | 1 | 1 | 1 | 31 clocks |

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register<br>Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIVC [1:0]</th><th>RTNC [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
</table>
</td></tr>
</table>

## 8.3.5. Display Inversion Control (B4h)

<table>
<tr><th>B4h</th><th colspan="13">INVTR (Display Inversion Control)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>B4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>NLA</td><td>NLB</td><td>NLC</td><td>02</td></tr>
<tr><td>Description</td><td colspan="13">Display inversion mode set<br>NLA: Inversion setting in full colors normal mode (Normal mode on)<br>NLB: Inversion setting in Idle mode (Idle mode on)<br>NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)<br><table><tr><th>NLA / NLB / NLC</th><th>Inversion</th></tr><tr><td>0</td><td>Line inversion</td></tr><tr><td>1</td><td>Frame inversion</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>NLA</th><th>NLB</th><th>NLC</th></tr><tr><td>Power ON Sequence</td><td>1’b0</td><td>1’b1</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>1’b1</td><td>1’b0</td></tr><tr><td>H/W Reset</td><td>1’b0</td><td>1’b1</td><td>1’b0</td></tr></table></td></tr>
</table>

## 8.3.6. Blanking Porch Control (B5h)

| B5h | PRCTR (Blanking Porch) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | VFP [6:0] | | | | | | | 02 |
| 2nd Parameter | 1 | 1 | ↑ | XX | 0 | VBP [6:0] | | | | | | | 02 |
| 3rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | HFP [4:0] | | | | | 0A |
| 4th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | HBP [4:0] | | | | | 14 |

Description

**VFP [6:0]** / **VBP [6:0]:** The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

| VFP [6:0] VBP [6:0] | Number of HSYNC of front/back porch | VFP [6:0] VBP [6:0] | Number of HSYNC of front/back porch |
|---|---|---|---|
| 0000000 | Setting inhibited | 1000000 | 64 |
| 0000001 | Setting inhibited | 1000001 | 65 |
| 0000010 | 2 | 1000010 | 66 |
| 0000011 | 3 | 1000011 | 67 |
| 0000100 | 4 | 1000100 | 68 |
| 0000101 | 5 | 1000101 | 69 |
| 0000110 | 6 | 1000110 | 70 |
| 0000111 | 7 | 1000111 | 71 |
| 0001000 | 8 | 1001000 | 72 |
| 0001001 | 9 | 1001001 | 73 |
| 0001010 | 10 | 1001010 | 74 |
| 0001011 | 11 | 1001011 | 75 |
| 0001100 | 12 | 1001100 | 76 |
| 0001101 | 13 | 1001101 | 77 |
| : : | : : | : : | : : |
| 0111101 | 61 | 1111101 | 125 |
| 0111110 | 62 | 1111110 | 126 |
| 0111111 | 63 | 1111111 | 127 |

*Note: VFP + VBP ≦ 254 HSYNC signals*

**HFP [4:0]** / **HBP [4:0]:** The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

| HFP [4:0] HBP [4:0] | Number of DOTCLK of the front/back porch | HFP [4:0] HBP [4:0] | Number of DOTCLK of front/back porch |
|---|---|---|---|
| 00000 | Setting prohibited | 10000 | 16 |
| 00001 | Setting prohibited | 10001 | 17 |
| 00010 | 2 | 10010 | 18 |
| 00011 | 3 | 10011 | 19 |
| 00100 | 4 | 10100 | 20 |
| 00101 | 5 | 10101 | 21 |
| 00110 | 6 | 10110 | 22 |
| 00111 | 7 | 10111 | 23 |
| 01000 | 8 | 11000 | 24 |
| 01001 | 9 | 11001 | 25 |
| 01010 | 10 | 11010 | 26 |
| 01011 | 11 | 11011 | 27 |
| 01100 | 12 | 11100 | 28 |
| 01101 | 13 | 11101 | 29 |
| 01110 | 14 | 11110 | 30 |
| 01111 | 15 | 11111 | 31 |

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register<br>Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HFP [4:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>SW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>HW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
</table>
</td></tr>
</table>

## 8.3.7. Display Function Control (B6h)

| B6h | DISCTRL (Display Function Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | PTG [1:0] | | PT [1:0] | | 0A |
| 2nd Parameter | 1 | 1 | ↑ | XX | REV | GS | SS | SM | ISC [3:0] | | | | 82 |
| 3rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | NL [5:0] | | | | | | 27 |
| 4th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | PCDIV [5:0] | | | | | | XX |

Description

**PTG [1:0]:** Set the scan mode in non-display area.

| PTG1 | PTG0 | Gate outputs in non-display area | Source outputs in non-display area | VCOM output |
|---|---|---|---|---|
| 0 | 0 | Normal scan | Set with the PT [2:0] bits | VCOMH/VCOML |
| 0 | 1 | Setting prohibited | --- | --- |
| 1 | 0 | Interval scan | Set with the PT [2:0] bits | |
| 1 | 1 | Setting prohibited | --- | --- |

**PT [1:0]:** Determine source/VCOM output in a non-display area in the partial display mode.

| PT [1:0] | | Source output on non-display area | | VCOM output on non-display area | |
|---|---|---|---|---|---|
| | | Positive polarity | Negative polarity | Positive polarity | Negative polarity |
| 0 | 0 | V63 | V0 | VCOML | VCOMH |
| 0 | 1 | V0 | V63 | VCOML | VCOMH |
| 1 | 0 | AGND | AGND | AGND | AGND |
| 1 | 1 | Hi-Z | Hi-Z | AGND | AGND |

**SS:** Select the shift direction of outputs from the source driver.

| SS | Source Output Scan Direction |
|---|---|
| 0 | S1 → S720 |
| 1 | S720 → S1 |

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

**REV:** Select whether the liquid crystal type is normally white type or normally black type.

| REV | Liquid crystal type |
|---|---|
| 0 | Normally black |
| 1 | Normally white |

**ISC [3:0]:** Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

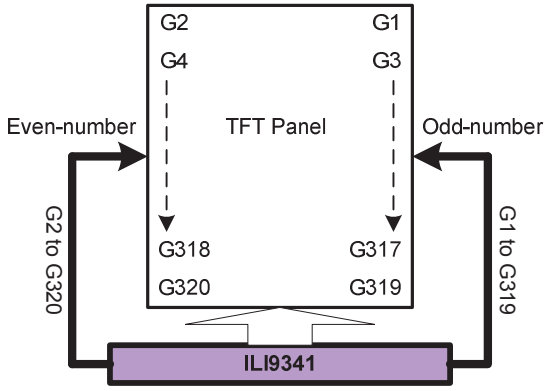
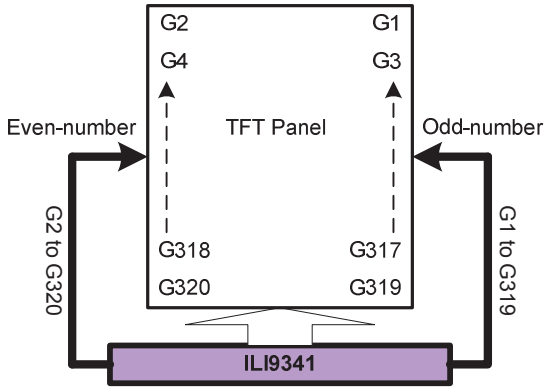
| ISC [3:0] | Scan Cycle | $f_{FLM}$ = 60Hz |
|---|---|---|
| 0000 | 1 frame | 17ms |
| 0001 | 3 frames | 51ms |
| 0010 | 5 frames | 85ms |
| 0011 | 7 frames | 119ms |
| 0100 | 9 frames | 153ms |
| 0101 | 11 frames | 187ms |
| 0110 | 13 frames | 221ms |
| 0111 | 15 frames | 255ms |

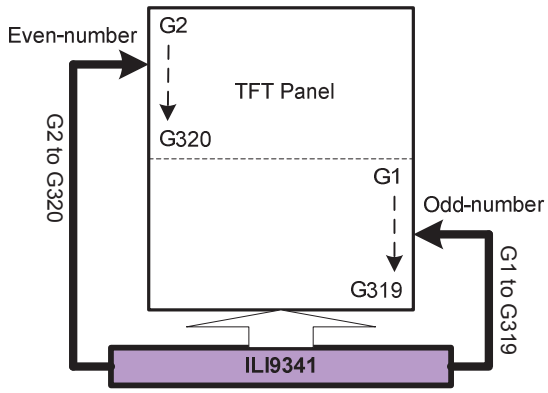
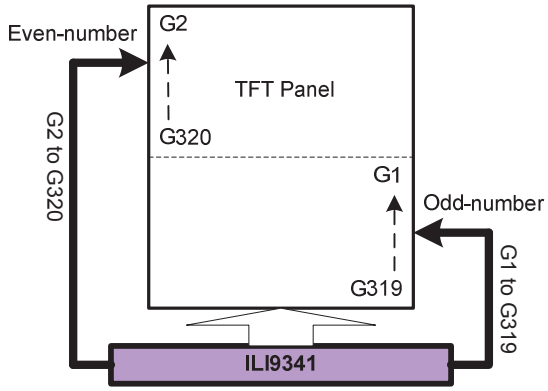
| | | |
|---|---|---|
| 1000 | 17 frames | 289ms |
| 1001 | 19 frames | 323ms |
| 1010 | 21 frames | 357ms |
| 1011 | 23 frames | 391ms |
| 1100 | 25 frames | 425ms |
| 1101 | 27 frames | 459ms |
| 1110 | 29 frames | 493ms |
| 1111 | 31 frames | 527ms |

**GS:** Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

| GS | Gate Output Scan Direction |
|---|---|
| 0 | G1 → G320 |
| 1 | G320 → G1 |

**SM:** Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

| SM | GS | Scan Direction | Gate Output Sequence |
|---|---|---|---|
| 0 | 0 |  | G1→G2→G3→G4→ ……<br>….→G317→G318→G319→G320 |
| 0 | 1 |  | G320→G319->G318→G317→……<br>…. →G4→G3→G2→G1 |

| | | | |
|---|---|---|---|
| 1 | 0 |  | G1→G3→…….→G317→G319→<br>G2→G4→……→G318→G320 |
| 1 | 1 |  | G320→G318→…….→G4→G2→<br>G319→G317→……→G3→G1 |

**NL [5:0]**: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

| NL [5:0] | | | | | | LCD Drive Line |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 0 | 1 | 16 lines |
| 0 | 0 | 0 | 0 | 1 | 0 | 24 lines |
| 0 | 0 | 0 | 0 | 1 | 1 | 32 lines |
| 0 | 0 | 0 | 1 | 0 | 0 | 40 lines |
| 0 | 0 | 0 | 1 | 0 | 1 | 48 lines |
| 0 | 0 | 0 | 1 | 1 | 0 | 56 lines |
| 0 | 0 | 0 | 1 | 1 | 1 | 64 lines |
| 0 | 0 | 1 | 0 | 0 | 0 | 72 lines |
| 0 | 0 | 1 | 0 | 0 | 1 | 80 lines |
| 0 | 0 | 1 | 0 | 1 | 0 | 88 lines |
| 0 | 0 | 1 | 0 | 1 | 1 | 96 lines |
| 0 | 0 | 1 | 1 | 0 | 0 | 104 lines |
| 0 | 0 | 1 | 1 | 0 | 1 | 112 lines |
| 0 | 0 | 1 | 1 | 1 | 0 | 120 lines |
| 0 | 0 | 1 | 1 | 1 | 1 | 128 lines |
| 0 | 1 | 0 | 0 | 0 | 0 | 136 lines |
| 0 | 1 | 0 | 0 | 0 | 1 | 144 lines |
| 0 | 1 | 0 | 0 | 1 | 0 | 152 lines |
| 0 | 1 | 0 | 0 | 1 | 1 | 160 lines |
| 0 | 1 | 0 | 1 | 0 | 0 | 168 lines |

| NL [5:0] | | | | | | LCD Driver Line |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 176 lines |
| 0 | 1 | 0 | 1 | 1 | 0 | 184 lines |
| 0 | 1 | 0 | 1 | 1 | 1 | 192 lines |
| 0 | 1 | 1 | 0 | 0 | 0 | 200 lines |
| 0 | 1 | 1 | 0 | 0 | 1 | 208 lines |
| 0 | 1 | 1 | 0 | 1 | 0 | 216 lines |
| 0 | 1 | 1 | 0 | 1 | 1 | 224 lines |
| 0 | 1 | 1 | 1 | 0 | 0 | 232 lines |
| 0 | 1 | 1 | 1 | 0 | 1 | 240 lines |
| 0 | 1 | 1 | 1 | 1 | 0 | 248 lines |
| 0 | 1 | 1 | 1 | 1 | 1 | 256 lines |
| 1 | 0 | 0 | 0 | 0 | 0 | 264 lines |
| 1 | 0 | 0 | 0 | 0 | 1 | 272 lines |
| 1 | 0 | 0 | 0 | 1 | 0 | 280 lines |
| 1 | 0 | 0 | 0 | 1 | 1 | 288 lines |
| 1 | 0 | 0 | 1 | 0 | 0 | 296 lines |
| 1 | 0 | 0 | 1 | 0 | 1 | 304 lines |
| 1 | 0 | 0 | 1 | 1 | 0 | 312 lines |
| 1 | 0 | 0 | 1 | 1 | 1 | 320 lines |
| Others | | | | | | Setting inhibited |

**PCDIV [5:0]:**

<table>
<tr><td></td><td>external fosc= $\frac{DOTCLK}{2\times(PCDIV+1)}$</td></tr>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register<br>Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="8">Default Value</th></tr>
<tr><th>PTG [1:0]</th><th>PT [1:0]</th><th>REV</th><th>GS</th><th>SS</th><th>SM</th><th>ISC [3:0]</th><th>NL [5:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b10</td><td>2’b10</td><td>1’b1</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>4’b0010</td><td>6’h27h</td></tr>
<tr><td>SW Reset</td><td>2’b10</td><td>2’b10</td><td>1’b1</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>4’b0010</td><td>6’h27h</td></tr>
<tr><td>HW Reset</td><td>2’b10</td><td>2’b10</td><td>1’b1</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>4’b0010</td><td>6’h27h</td></tr>
</table>
</td></tr>
</table>

## 8.3.8. Entry Mode Set (B7h)

| B7h | ETMOD (Entry Mode Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7h |
| Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | DSTB | GON | DTE | GAS | 06 |

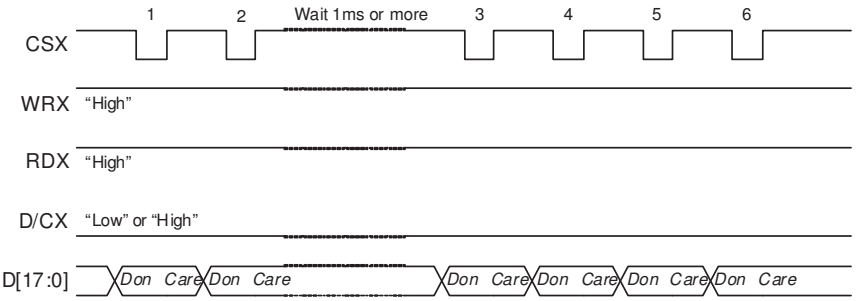
Description

**DSTB:** The ILI9341 driver enters the Deep Standby Mode when DSTB is set to high ("1"). In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.

*Note: ILI9341 provides two ways to exit the Deep Standby Mode:*

*(1) Exit Deep Standby Mode by pull down CSX to low ("0") 6 times.*

*(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.*




**GAS:** Low voltage detection control.

| GAS | Low voltage detection |
|---|---|
| 0 | Enable |
| 1 | Disable |

**GON/DTE:** Set the output level of gate driver G1 ~ G320 as follows

| GON | DTE | G1~G320 Gate Output |
|---|---|---|
| 0 | 0 | VGH |
| 0 | 1 | VGH |
| 1 | 0 | VGL |
| 1 | 1 | Normal display |

Restriction: EXTC should be high to enable this command

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value | | | |
|---|---|---|---|---|
| | DSTB | GON | DTE | GAS |
| Power ON Sequence | 1'b0 | 1'b1 | 1'b1 | 1'b0 |
| SW Reset | 1'b0 | 1'b1 | 1'b1 | 1'b0 |
| HW Reset | 1'b0 | 1'b1 | 1'b1 | 1'b0 |

## 8.3.9. Backlight Control 1 (B8h)

| B8h | Backlight Control 1 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | B8h |
| Parameter | | 1 | ↑ | XX | 0 | 0 | 0 | 0 | TH_UI [3] | TH_UI [2] | TH_UI [1] | TH_UI [0] | 0C |

Description

**TH_UI [3:0]**: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

| TH_UI [3:0] | Description |
|---|---|
| 4’0h | 99% |
| 4’1h | 98% |
| 4’2h | 96% |
| 4’3h | 94% |
| 4’4h | 92% |
| 4’5h | 90% |
| 4’6h | 88% |
| 4’7h | 86% |

| TH_UI [3:0] | Description |
|---|---|
| 4’8h | 84% |
| 4’9h | 82% |
| 4’Ah | 80% |
| 4’Bh | 78% |
| 4’Ch | 76% |
| 4’Dh | 74% |
| 4’Eh | 72% |
| 4’Fh | 70% |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| | TH_UI [3:0] |
| Power On Sequence | 4’b0110 |
| SW Reset | No change |
| HW Reset | 4’b0110 |

## 8.3.10. Backlight Control 2 (B9h)

| B9h | Backlight Control 2 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9h |
| Parameter | 1 | 1 | ↑ | XX | TH_MV [3] | TH_MV [2] | TH_MV [1] | TH_MV [0] | TH_ST [3] | TH_ST [2] | TH_ST [1] | TH_ST [0] | CC |

Description

**TH_ST [3:0]**: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

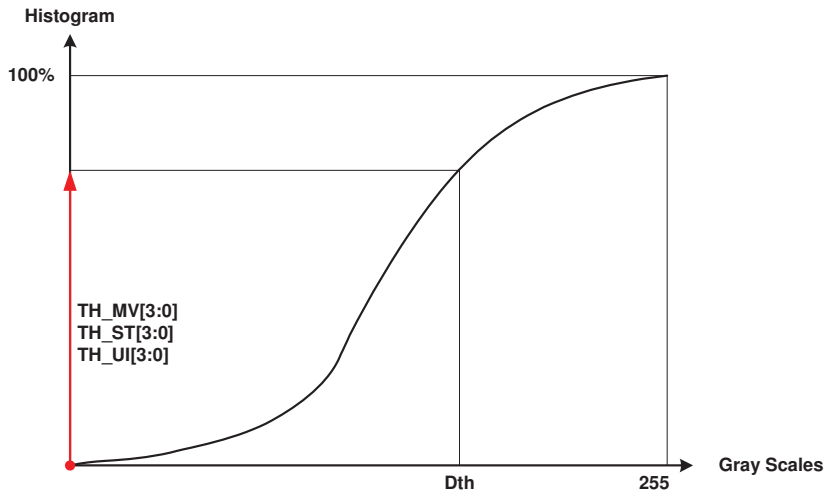
| TH_ST [3:0] | Description |
|---|---|
| 4’0h | 99% |
| 4’1h | 98% |
| 4’2h | 96% |
| 4’3h | 94% |
| 4’4h | 92% |
| 4’5h | 90% |
| 4’6h | 88% |
| 4’7h | 86% |

| TH_ST [3:0] | Description |
|---|---|
| 4’8h | 84% |
| 4’9h | 82% |
| 4’Ah | 80% |
| 4’Bh | 78% |
| 4’Ch | 76% |
| 4’Dh | 74% |
| 4’Eh | 72% |
| 4’Fh | 70% |

**TH_MV [3:0]**: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

| TH_MV [3:0] | Description |
|---|---|
| 4’0h | 99% |
| 4’1h | 98% |
| 4’2h | 96% |
| 4’3h | 94% |
| 4’4h | 92% |
| 4’5h | 90% |
| 4’6h | 88% |
| 4’7h | 86% |

| TH_MV [3:0] | Description |
|---|---|
| 4’8h | 84% |
| 4’9h | 82% |
| 4’Ah | 80% |
| 4’Bh | 78% |
| 4’Ch | 76% |
| 4’Dh | 74% |
| 4’Eh | 72% |
| 4’Fh | 70% |



<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>TH_MV [3:0]</th><th>TH_ST [3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’b1100</td><td>4’b1100</td></tr>
<tr><td>SW Reset</td><td>No change</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>4’b1100</td><td>4’b1100</td></tr>
</table>
</td></tr>
</table>

## 8.3.11. Backlight Control 3 (BAh)

| BAh | Backlight Control 3 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BAh |
| Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | DTH_UI [3] | DTH_UI [2] | DTH_UI [1] | DTH_UI [0] | 04 |

Description

**DTH_UI [3:0]**: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

| DTH_UI [3:0] | Description |
|---|---|
| 4'0h | 252 |
| 4'1h | 248 |
| 4'2h | 244 |
| 4'3h | 240 |
| 4'4h | 236 |
| 4'5h | 232 |
| 4'6h | 228 |
| 4'7h | 224 |

| DTH_UI [3:0] | Description |
|---|---|
| 4'8h | 220 |
| 4'9h | 216 |
| 4'Ah | 212 |
| 4'Bh | 208 |
| 4'Ch | 204 |
| 4'Dh | 200 |
| 4'Eh | 196 |
| 4'Fh | 192 |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| | DTH_UI [3:0] |
| Power On Sequence | 4'b0100 |
| SW Reset | No change |
| HW Reset | 4'b0100 |

## 8.3.12. Backlight Control 4 (BBh)

| BBh | Backlight Control 4 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | BBh |
| Parameter | 1 | 1 | ↑ | XX | DTH_MV [3] | DTH_MV [2] | DTH_MV [1] | DTH_MV [0] | DTH_ST [3] | DTH_ST [2] | DTH_ST [1] | DTH_ST [0] | 65 |

Description

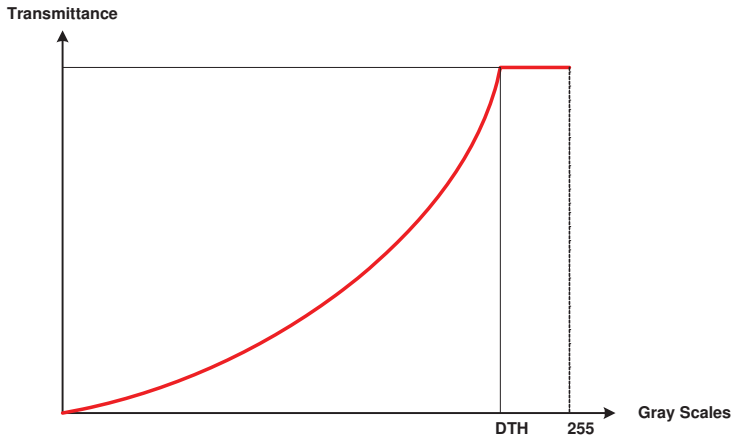
**DTH_ST [3:0]/DTH_MV [3:0]**: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

| DTH_ST [3:0] | Description |
|---|---|
| 4'0h | 224 |
| 4'1h | 220 |
| 4'2h | 216 |
| 4'3h | 212 |
| 4'4h | 208 |
| 4'5h | 204 |
| 4'6h | 200 |
| 4'7h | 196 |

| DTH_ST [3:0] | Description |
|---|---|
| 4'8h | 192 |
| 4'9h | 188 |
| 4'Ah | 184 |
| 4'Bh | 180 |
| 4'Ch | 176 |
| 4'Dh | 172 |
| 4'Eh | 168 |
| 4'Fh | 164 |

| DTH_MV [3:0] | Description |
|---|---|
| 4'0h | 224 |
| 4'1h | 220 |
| 4'2h | 216 |
| 4'3h | 212 |
| 4'4h | 208 |
| 4'5h | 204 |
| 4'6h | 200 |
| 4'7h | 196 |

| DTH_MV [3:0] | Description |
|---|---|
| 4'8h | 192 |
| 4'9h | 188 |
| 4'Ah | 184 |
| 4'Bh | 180 |
| 4'Ch | 176 |
| 4'Dh | 172 |
| 4'Eh | 168 |
| 4'Fh | 164 |




Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | DTH_MV [3:0] | DTH_ST [3:0] |
| Power On Sequence | 4'b0110 | 4'b0101 |
| SW Reset | No change | No change |
| HW Reset | 4'b0110 | 4'b0101 |

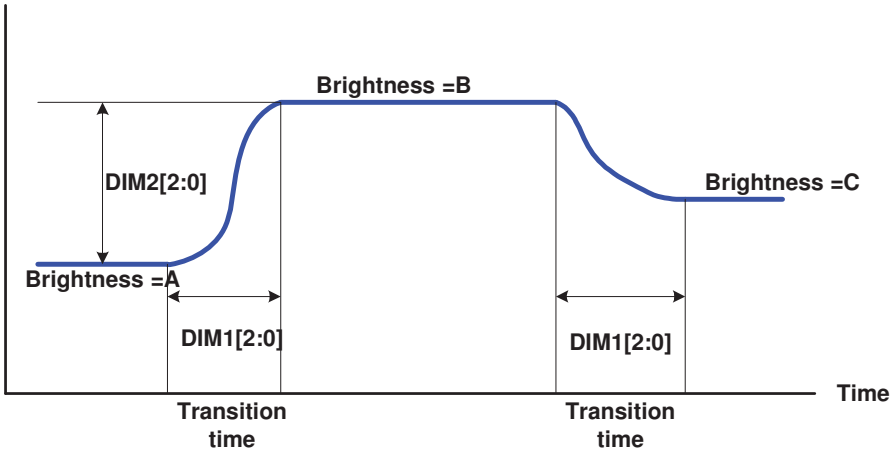
## 8.3.13. Backlight Control 5 (BCh)

| BCh | Backlight Control 5 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BCh |
| Parameter | 1 | 1 | ↑ | XX | DIM2 [3] | DIM2 [2] | DIM2 [1] | DIM2 [0] | 0 | DIM1 [2] | DIM1 [1] | DIM1 [0] | 44 |

Description

**DIM1 [2:0]**: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

| DIM1 [2:0] | Description |
|---|---|
| 3'0h | 1 frame |
| 3'1h | 1 frame |
| 3'2h | 2 frames |
| 3'3h | 4 frames |
| 3'4h | 8 frames |
| 3'5h | 16 frames |
| 3'6h | 32 frames |
| 3'7h | 64 frames |




**DIM2 [3:0]**: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.

For example:

If | brightness B – brightness A| < DIM2 [2:0], the brightness transition will be ignored and keep the brightness A.

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | DIM2 [3:0] | DIM1 [2:0] |
| Power On Sequence | 4'b0100 | 4'b0100 |
| SW Reset | No change | No change |
| HW Reset | 4'b0100 | 4'b0100 |

## 8.3.14. Backlight Control 7 (BEh)

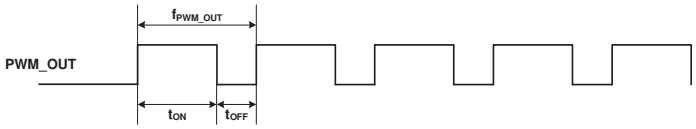
| BEh | Backlight Control 7 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BEh |
| Parameter | 1 | 1 | ↑ | XX | PWM_ DIV[7] | PWM_ DIV[6] | PWM_ DIV[5] | PWM_ DIV[4] | PWM_ DIV[3] | PWM_ DIV[2] | PWM_ DIV[1] | PWM_ DIV[0] | 0F |

Description

**PWM_DIV [7:0]**: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM\_OUT} = \frac{16MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

| PWM_DIV [7:0] | $f_{PWM\_OUT}$ |
|---|---|
| 8'h0 | 62.74 KHz |
| 8'h1 | 31.38 KHz |
| 8'h2 | 20.915KHz |
| 8'h3 | 15.686KHz |
| 8'h4 | 12.549 KHz |
| … | … |
| 8'hFB | 249Hz |
| 8'hFC | 248Hz |
| 8'hFD | 247Hz |
| 8'hFE | 246Hz |
| 8'hFF | 245Hz |




*Note: The output frequency tolerance of internal frequency divider in CABC is ±10%*

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | PWM_DIV [7:0]=0Fh |
| SW Reset | No change |
| HW Reset | PWM_DIV [7:0]=0Fh |

## 8.3.15. Backlight Control 8 (BFh)

| BFh | Backlight Control 2 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | BFh |
| Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | LEDONR | LEDONPOL | LEDPWMPOL | 00 |

Description

**LEDPWMPOL:** The bit is used to define polarity of LEDPWM signal.

| BL | LEDPWMPOL | LEDPWM pin |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | Original polarity of PWM signal |
| 1 | 1 | Inversed polarity of PWM signal |

**LEDONPOL:** This bit is used to control LEDON pin.

| BL | LEDONPOL | LEDON pin |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | LEDONR |
| 1 | 1 | Inversed LEDONR |

**LEDONR:** This bit is used to control LEDON pin.

| LEDONR | Description |
|---|---|
| 0 | Low |
| 1 | High |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | | |
|---|---|---|---|
| | LEDONR | LEDONPOL | LEDPWMPOL |
| Power On Sequence | 1'b0 | 1'b0 | 1'b0 |
| SW Reset | No change | No change | No change |
| HW Reset | 1'b0 | 1'b0 | 1'b0 |

## 8.3.16. Power Control 1 (C0h)

| C0h | PWCTRL 1 (Power Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | VRH [5:0] | | | | | | 21 |

Description

**VRH [5:0]:** Set the GVDD level, which is a reference level for the VCOM level and the grayscale voltage level.

| VRH [5:0] | | | | | | GVDD |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 0 | 1 | Setting prohibited |
| 0 | 0 | 0 | 0 | 1 | 0 | Setting prohibited |
| 0 | 0 | 0 | 0 | 1 | 1 | 3.00 V |
| 0 | 0 | 0 | 1 | 0 | 0 | 3.05 V |
| 0 | 0 | 0 | 1 | 0 | 1 | 3.10 V |
| 0 | 0 | 0 | 1 | 1 | 0 | 3.15 V |
| 0 | 0 | 0 | 1 | 1 | 1 | 3.20 V |
| 0 | 0 | 1 | 0 | 0 | 0 | 3.25 V |
| 0 | 0 | 1 | 0 | 0 | 1 | 3.30 V |
| 0 | 0 | 1 | 0 | 1 | 0 | 3.35 V |
| 0 | 0 | 1 | 0 | 1 | 1 | 3.40 V |
| 0 | 0 | 1 | 1 | 0 | 0 | 3.45 V |
| 0 | 0 | 1 | 1 | 0 | 1 | 3.50 V |
| 0 | 0 | 1 | 1 | 1 | 0 | 3.55 V |
| 0 | 0 | 1 | 1 | 1 | 1 | 3.60 V |
| 0 | 1 | 0 | 0 | 0 | 0 | 3.65 V |
| 0 | 1 | 0 | 0 | 0 | 1 | 3.70 V |
| 0 | 1 | 0 | 0 | 1 | 0 | 3.75 V |
| 0 | 1 | 0 | 0 | 1 | 1 | 3.80 V |
| 0 | 1 | 0 | 1 | 0 | 0 | 3.85 V |
| 0 | 1 | 0 | 1 | 0 | 1 | 3.90 V |
| 0 | 1 | 0 | 1 | 1 | 0 | 3.95 V |
| 0 | 1 | 0 | 1 | 1 | 1 | 4.00 V |
| 0 | 1 | 1 | 0 | 0 | 0 | 4.05 V |
| 0 | 1 | 1 | 0 | 0 | 1 | 4.10 V |
| 0 | 1 | 1 | 0 | 1 | 0 | 4.15 V |
| 0 | 1 | 1 | 0 | 1 | 1 | 4.20 V |
| 0 | 1 | 1 | 1 | 0 | 0 | 4.25 V |
| 0 | 1 | 1 | 1 | 0 | 1 | 4.30 V |
| 0 | 1 | 1 | 1 | 1 | 0 | 4.35 V |
| 0 | 1 | 1 | 1 | 1 | 1 | 4.40 V |

| VRH [5:0] | | | | | | GVDD |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 4.45 V |
| 1 | 0 | 0 | 0 | 0 | 1 | 4.50 V |
| 1 | 0 | 0 | 0 | 1 | 0 | 4.55 V |
| 1 | 0 | 0 | 0 | 1 | 1 | 4.60 V |
| 1 | 0 | 0 | 1 | 0 | 0 | 4.65 V |
| 1 | 0 | 0 | 1 | 0 | 1 | 4.70 V |
| 1 | 0 | 0 | 1 | 1 | 0 | 4.75 V |
| 1 | 0 | 0 | 1 | 1 | 1 | 4.80 V |
| 1 | 0 | 1 | 0 | 0 | 0 | 4.85 V |
| 1 | 0 | 1 | 0 | 0 | 1 | 4.90 V |
| 1 | 0 | 1 | 0 | 1 | 0 | 4.95 V |
| 1 | 0 | 1 | 0 | 1 | 1 | 5.00 V |
| 1 | 0 | 1 | 1 | 0 | 0 | 5.05 V |
| 1 | 0 | 1 | 1 | 0 | 1 | 5.10 V |
| 1 | 0 | 1 | 1 | 1 | 0 | 5.15 V |
| 1 | 0 | 1 | 1 | 1 | 1 | 5.20 V |
| 1 | 1 | 0 | 0 | 0 | 0 | 5.25 V |
| 1 | 1 | 0 | 0 | 0 | 1 | 5.30 V |
| 1 | 1 | 0 | 0 | 1 | 0 | 5.35 V |
| 1 | 1 | 0 | 0 | 1 | 1 | 5.40 V |
| 1 | 1 | 0 | 1 | 0 | 0 | 5.45 V |
| 1 | 1 | 0 | 1 | 0 | 1 | 5.50 V |
| 1 | 1 | 0 | 1 | 1 | 0 | 5.55 V |
| 1 | 1 | 0 | 1 | 1 | 1 | 5.60 V |
| 1 | 1 | 1 | 0 | 0 | 0 | 5.65 V |
| 1 | 1 | 1 | 0 | 0 | 1 | 5.70 V |
| 1 | 1 | 1 | 0 | 1 | 0 | 5.75 V |
| 1 | 1 | 1 | 0 | 1 | 1 | 5.80 V |
| 1 | 1 | 1 | 1 | 0 | 0 | 5.85 V |
| 1 | 1 | 1 | 1 | 0 | 1 | 5.90 V |
| 1 | 1 | 1 | 1 | 1 | 0 | 5.95 V |
| 1 | 1 | 1 | 1 | 1 | 1 | 6.00 V |

*Note1: Make sure that VC and VRH setting restriction: GVDD ≦ (AVDD - 0.5) V.*

Restriction: EXTC should be high to enable this command

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value |
|---|---|
| | VRH [5:0] |
| Power ON Sequence | 6'h21h |
| SW Reset | 6'h21h |
| HW Reset | 6'h21h |

## 8.3.17. Power Control 2 (C1h)

<table>
<tr><th>C1h</th><th colspan="13">PWCTRL 2 (Power Control 2)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td colspan="3">BT [2:0]</td><td>10</td></tr>
<tr><td>Description</td><td colspan="13">BT [2:0]: Sets the factor used in the step-up circuits.<br><br>Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.<br><br>
<table>
<tr><th colspan="3">BT [2:0]</th><th>AVDD</th><th>VGH</th><th>VGL</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="4">VCI x 2</td><td rowspan="2">VCI x 7</td><td>-VCI x 4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>-VCI x 3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td rowspan="2">VCI x 6</td><td>-VCI x 4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>-VCI x 3</td></tr>
</table>
<br>Note1: Make sure that AVDD setting restriction: AVDD ≦ 5.5 V.<br><br>2: Make sure that VGH and VGL setting restriction: VGH -VGL≦ 32 V.</td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>BT [2:0]</th></tr>
<tr><td>Power ON Sequence</td><td>3’b000</td></tr>
<tr><td>SW Reset</td><td>3’b000</td></tr>
<tr><td>HW Reset</td><td>3’b000</td></tr>
</table>
</td></tr>
</table>

## 8.3.18. VCOM Control 1(C5h)

| C5h | VMCTRL1 (VCOM Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | VMH [6:0] | | | | | | | 31 |
| 2ndParameter | 1 | 1 | ↑ | XX | 0 | VML [6:0] | | | | | | | 3C |

Description

**VMH [6:0] :** Set the VCOMH voltage.

| VMH [6:0] | VCOMH(V) | VMH [6:0] | VCOMH(V) | VMH [6:0] | VCOMH(V) | VMH [6:0] | VCOMH(V) |
|---|---|---|---|---|---|---|---|
| 0000000 | 2.700 | 0100000 | 3.500 | 1000000 | 4.300 | 1100000 | 5.100 |
| 0000001 | 2.725 | 0100001 | 3.525 | 1000001 | 4.325 | 1100001 | 5.125 |
| 0000010 | 2.750 | 0100010 | 3.550 | 1000010 | 4.350 | 1100010 | 5.150 |
| 0000011 | 2.775 | 0100011 | 3.575 | 1000011 | 4.375 | 1100011 | 5.175 |
| 0000100 | 2.800 | 0100100 | 3.600 | 1000100 | 4.400 | 1100100 | 5.200 |
| 0000101 | 2.825 | 0100101 | 3.625 | 1000101 | 4.425 | 1100101 | 5.225 |
| 0000110 | 2.850 | 0100110 | 3.650 | 1000110 | 4.450 | 1100110 | 5.250 |
| 0000111 | 2.875 | 0100111 | 3.675 | 1000111 | 4.475 | 1100111 | 5.275 |
| 0001000 | 2.900 | 0101000 | 3.700 | 1001000 | 4.500 | 1101000 | 5.300 |
| 0001001 | 2.925 | 0101001 | 3.725 | 1001001 | 4.525 | 1101001 | 5.325 |
| 0001010 | 2.950 | 0101010 | 3.750 | 1001010 | 4.550 | 1101010 | 5.350 |
| 0001011 | 2.975 | 0101011 | 3.775 | 1001011 | 4.575 | 1101011 | 5.375 |
| 0001100 | 3.000 | 0101100 | 3.800 | 1001100 | 4.600 | 1101100 | 5.400 |
| 0001101 | 3.025 | 0101101 | 3.825 | 1001101 | 4.625 | 1101101 | 5.425 |
| 0001110 | 3.050 | 0101110 | 3.850 | 1001110 | 4.650 | 1101110 | 5.450 |
| 0001111 | 3.075 | 0101111 | 3.875 | 1001111 | 4.675 | 1101111 | 5.475 |
| 0010000 | 3.100 | 0110000 | 3.900 | 1010000 | 4.700 | 1110000 | 5.500 |
| 0010001 | 3.125 | 0110001 | 3.925 | 1010001 | 4.725 | 1110001 | 5.525 |
| 0010010 | 3.150 | 0110010 | 3.950 | 1010010 | 4.750 | 1110010 | 5.550 |
| 0010011 | 3.175 | 0110011 | 3.975 | 1010011 | 4.775 | 1110011 | 5.575 |
| 0010100 | 3.200 | 0110100 | 4.000 | 1010100 | 4.800 | 1110100 | 5.600 |
| 0010101 | 3.225 | 0110101 | 4.025 | 1010101 | 4.825 | 1110101 | 5.625 |
| 0010110 | 3.250 | 0110110 | 4.050 | 1010110 | 4.850 | 1110110 | 5.650 |
| 0010111 | 3.275 | 0110111 | 4.075 | 1010111 | 4.875 | 1110111 | 5.675 |
| 0011000 | 3.300 | 0111000 | 4.100 | 1011000 | 4.900 | 1111000 | 5.700 |
| 0011001 | 3.325 | 0111001 | 4.125 | 1011001 | 4.925 | 1111001 | 5.725 |
| 0011010 | 3.350 | 0111010 | 4.150 | 1011010 | 4.950 | 1111010 | 5.750 |
| 0011011 | 3.375 | 0111011 | 4.175 | 1011011 | 4.975 | 1111011 | 5.775 |
| 0011100 | 3.400 | 0111100 | 4.200 | 1011100 | 5.000 | 1111100 | 5.800 |
| 0011101 | 3.425 | 0111101 | 4.225 | 1011101 | 5.025 | 1111101 | 5.825 |
| 0011110 | 3.450 | 0111110 | 4.250 | 1011110 | 5.050 | 1111110 | 5.850 |
| 0011111 | 3.475 | 0111111 | 4.275 | 1011111 | 5.075 | 1111111 | 5.875 |

**VML [6:0] :** Set the VCOML voltage

| VML [6:0] | VCOML(V) | VML [6:0] | VCOML(V) | VML [6:0] | VCOML(V) | VML [6:0] | VCOML(V) |
|---|---|---|---|---|---|---|---|
| 0000000 | -2.500 | 0100000 | -1.700 | 1000000 | -0.900 | 1100000 | -0.100 |
| 0000001 | -2.475 | 0100001 | -1.675 | 1000001 | -0.875 | 1100001 | -0.075 |
| 0000010 | -2.450 | 0100010 | -1.650 | 1000010 | -0.850 | 1100010 | -0.050 |
| 0000011 | -2.425 | 0100011 | -1.625 | 1000011 | -0.825 | 1100011 | -0.025 |
| 0000100 | -2.400 | 0100100 | -1.600 | 1000100 | -0.800 | 1100100 | 0 |
| 0000101 | -2.375 | 0100101 | -1.575 | 1000101 | -0.775 | 1100101 | Reserved |
| 0000110 | -2.350 | 0100110 | -1.550 | 1000110 | -0.750 | 1100110 | Reserved |
| 0000111 | -2.325 | 0100111 | -1.525 | 1000111 | -0.725 | 1100111 | Reserved |
| 0001000 | -2.300 | 0101000 | -1.500 | 1001000 | -0.700 | 1101000 | Reserved |
| 0001001 | -2.275 | 0101001 | -1.475 | 1001001 | -0.675 | 1101001 | Reserved |
| 0001010 | -2.250 | 0101010 | -1.450 | 1001010 | -0.650 | 1101010 | Reserved |
| 0001011 | -2.225 | 0101011 | -1.425 | 1001011 | -0.625 | 1101011 | Reserved |
| 0001100 | -2.200 | 0101100 | -1.400 | 1001100 | -0.600 | 1101100 | Reserved |
| 0001101 | -2.175 | 0101101 | -1.375 | 1001101 | -0.575 | 1101101 | Reserved |
| 0001110 | -2.150 | 0101110 | -1.350 | 1001110 | -0.550 | 1101110 | Reserved |
| 0001111 | -2.125 | 0101111 | -1.325 | 1001111 | -0.525 | 1101111 | Reserved |
| 0010000 | -2.100 | 0110000 | -1.300 | 1010000 | -0.500 | 1110000 | Reserved |
| 0010001 | -2.075 | 0110001 | -1.275 | 1010001 | -0.475 | 1110001 | Reserved |
| 0010010 | -2.050 | 0110010 | -1.250 | 1010010 | -0.450 | 1110010 | Reserved |
| 0010011 | -2.025 | 0110011 | -1.225 | 1010011 | -0.425 | 1110011 | Reserved |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0010100 | -2.000 | 0110100 | -1.200 | 1010100 | -0.400 | 1110100 | Reserved |
| | 0010101 | -1.975 | 0110101 | -1.175 | 1010101 | -0.375 | 1110101 | Reserved |
| | 0010110 | -1.950 | 0110110 | -1.150 | 1010110 | -0.350 | 1110110 | Reserved |
| | 0010111 | -1.925 | 0110111 | -1.125 | 1010111 | -0.325 | 1110111 | Reserved |
| | 0011000 | -1.900 | 0111000 | -1.100 | 1011000 | -0.300 | 1111000 | Reserved |
| | 0011001 | -1.875 | 0111001 | -1.075 | 1011001 | -0.275 | 1111001 | Reserved |
| | 0011010 | -1.850 | 0111010 | -1.050 | 1011010 | -0.250 | 1111010 | Reserved |
| | 0011011 | -1.825 | 0111011 | -1.025 | 1011011 | -0.225 | 1111011 | Reserved |
| | 0011100 | -1.800 | 0111100 | -1.000 | 1011100 | -0.200 | 1111100 | Reserved |
| | 0011101 | -1.775 | 0111101 | -0.975 | 1011101 | -0.175 | 1111101 | Reserved |
| | 0011110 | -1.750 | 0111110 | -0.950 | 1011110 | -0.150 | 1111110 | Reserved |
| | 0011111 | -1.725 | 0111111 | -0.925 | 1011111 | -0.125 | 1111111 | Reserved |

| | |
|---|---|
| Restriction | EXTC should be high to enable this command |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | VMH [6:0] | VML [6:0] |
| Power ON Sequence | 7'h31 | 7'h3C |
| SW Reset | 7'h31 | 7'h3C |
| HW Rest | 7'h31 | 7'h3C |

## 8.3.19. VCOM Control 2(C7h)

| C7h | VMCTRL1 (VCOM Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7h |
| Parameter | 1 | 1 | ↑ | XX | nVM | VMF [6:0] | | | | | | | C0 |

Description

**nVM:** nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.

**VMF [6:0]:** Set the VCOM offset voltage.

| VMF[6:0] | VCOMH | VCOML | VMF[6:0] | VCOMH | VCOML |
|---|---|---|---|---|---|
| 0000000 | VMH | VML | 1000000 | VMH | VML |
| 0000001 | VMH – 63 | VML – 63 | 1000001 | VMH + 1 | VML + 1 |
| 0000010 | VMH – 62 | VML – 62 | 1000010 | VMH + 2 | VML + 2 |
| 0000011 | VMH – 61 | VML – 61 | 1000011 | VMH + 3 | VML + 3 |
| 0000100 | VMH – 60 | VML – 60 | 1000100 | VMH + 4 | VML + 4 |
| 0000101 | VMH – 58 | VML – 58 | 1000101 | VMH + 5 | VML + 5 |
| 0000110 | VMH – 58 | VML – 58 | 1000110 | VMH + 6 | VML + 6 |
| 0000111 | VMH – 57 | VML – 57 | 1000111 | VMH + 7 | VML + 7 |
| 0001000 | VMH – 56 | VML – 56 | 1001000 | VMH + 8 | VML + 8 |
| 0001001 | VMH – 55 | VML – 55 | 1001001 | VMH + 9 | VML + 9 |
| 0001010 | VMH – 54 | VML – 54 | 1001010 | VMH + 10 | VML + 10 |
| 0001011 | VMH – 53 | VML – 53 | 1001011 | VMH + 11 | VML + 11 |
| 0001100 | VMH – 52 | VML – 52 | 1001100 | VMH + 12 | VML + 12 |
| 0001101 | VMH – 51 | VML -51 | 1001101 | VMH + 13 | VML + 13 |
| 0001110 | VMH – 50 | VML – 50 | 1001110 | VMH + 14 | VML + 14 |
| 0001111 | VMH – 49 | VML – 49 | 1001111 | VMH + 15 | VML + 15 |
| 0010000 | VMH – 48 | VML – 48 | 1010000 | VMH + 16 | VML + 16 |
| 0010001 | VMH – 47 | VML – 47 | 1010001 | VMH + 17 | VML + 17 |
| 0010010 | VMH – 46 | VML – 46 | 1010010 | VMH + 18 | VML + 18 |
| 0010011 | VMH – 45 | VML – 45 | 1010011 | VMH + 19 | VML + 19 |
| 0010100 | VMH – 44 | VML – 44 | 1010100 | VMH + 20 | VML + 20 |
| 0010101 | VMH – 43 | VML – 43 | 1010101 | VMH + 21 | VML + 21 |
| 0010110 | VMH – 42 | VML – 42 | 1010110 | VMH + 22 | VML + 22 |
| 0010111 | VMH – 41 | VML – 41 | 1010111 | VMH + 23 | VML + 23 |
| 0011000 | VMH – 40 | VML – 40 | 1011000 | VMH + 24 | VML + 24 |
| 0011001 | VMH – 39 | VML – 39 | 1011001 | VMH + 25 | VML + 25 |
| 0011010 | VMH – 38 | VML – 38 | 1011010 | VMH + 26 | VML + 26 |
| 0011011 | VMH – 37 | VML – 37 | 1011011 | VMH + 27 | VML + 27 |
| 0011100 | VMH – 36 | VML – 36 | 1011100 | VMH + 28 | VML + 28 |
| 0011101 | VMH – 35 | VML – 35 | 1011101 | VMH + 29 | VML + 29 |
| 0011110 | VMH – 34 | VML – 34 | 1011110 | VMH + 30 | VML + 30 |
| 0011111 | VMH – 33 | VML – 33 | 1011111 | VMH + 31 | VML + 31 |
| 0100000 | VMH – 32 | VML – 32 | 1100000 | VMH + 32 | VML + 32 |
| 0100001 | VMH – 31 | VML – 31 | 1100001 | VMH + 33 | VML + 33 |
| 0100010 | VMH – 30 | VML – 30 | 1100010 | VMH + 34 | VML + 34 |
| 0100011 | VMH – 29 | VML – 29 | 1100011 | VMH + 35 | VML + 35 |
| 0100100 | VMH – 28 | VML – 28 | 1100100 | VMH + 36 | VML + 36 |
| 0100101 | VMH – 27 | VML – 27 | 1100101 | VMH + 37 | VML + 37 |
| 0100110 | VMH – 26 | VML – 26 | 1100110 | VMH + 38 | VML + 38 |
| 0100111 | VMH – 25 | VML – 25 | 1100111 | VMH + 39 | VML + 39 |
| 0101000 | VMH – 24 | VML – 24 | 1101000 | VMH + 40 | VML + 40 |
| 0101001 | VMH – 23 | VML – 23 | 1101001 | VMH + 41 | VML + 41 |
| 0101010 | VMH – 22 | VML – 22 | 1101010 | VMH + 42 | VML + 42 |
| 0101011 | VMH – 21 | VML – 21 | 1101011 | VMH + 43 | VML + 43 |
| 0101100 | VMH – 20 | VML – 20 | 1101100 | VMH + 44 | VML + 44 |
| 0101101 | VMH – 19 | VML – 19 | 1101101 | VMH + 45 | VML + 45 |
| 0101110 | VMH – 18 | VML – 18 | 1101110 | VMH + 46 | VML + 46 |
| 0101111 | VMH – 17 | VML – 17 | 1101111 | VMH + 47 | VML + 47 |
| 0110000 | VMH – 16 | VML – 16 | 1110000 | VMH + 48 | VML + 48 |
| 0110001 | VMH – 15 | VML – 15 | 1110001 | VMH + 49 | VML + 49 |
| 0110010 | VMH – 14 | VML – 14 | 1110010 | VMH + 50 | VML + 50 |
| 0110011 | VMH – 13 | VML – 13 | 1110011 | VMH + 51 | VML + 51 |
| 0110100 | VMH – 12 | VML – 12 | 1110100 | VMH + 52 | VML + 52 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 0110101 | VMH – 11 | VML – 11 | | 1110101 | VMH + 53 | VML + 53 |
| | | 0110110 | VMH – 10 | VML – 10 | | 1110110 | VMH + 54 | VML + 54 |
| | | 0110111 | VMH – 9 | VML – 9 | | 1110111 | VMH + 55 | VML + 55 |
| | | 0111000 | VMH – 8 | VML – 8 | | 1111000 | VMH + 56 | VML + 56 |
| | | 0111001 | VMH – 7 | VML – 7 | | 1111001 | VMH + 57 | VML + 57 |
| | | 0111010 | VMH – 6 | VML – 6 | | 1111010 | VMH + 58 | VML + 58 |
| | | 0111011 | VMH – 5 | VML – 5 | | 1111011 | VMH + 59 | VML + 59 |
| | | 0111100 | VMH – 4 | VML – 4 | | 1111100 | VMH + 60 | VML + 60 |
| | | 0111101 | VMH – 3 | VML – 3 | | 1111101 | VMH + 61 | VML + 61 |
| | | 0111110 | VMH – 2 | VML – 2 | | 1111110 | VMH + 62 | VML + 62 |
| | | 0111111 | VMH – 1 | VML – 1 | | 1111111 | VMH + 63 | VML + 63 |
| Restriction | EXTC should be high to enable this command | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | nVM | VMF [6:0] |
| Power ON Sequence | 1'b1 | 7'h40h |
| SW Reset | 1'b1 | 7'h40h |
| HW Reset | 1'b1 | 7'h40h |

## 8.3.20. NV Memory Write (D0h)

| D0h | NVMWR (NV Memory Write) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | PGM_ADR [2:0] | | | 00 |
| 2ndParameter | 1 | 1 | ↑ | XX | PGM_DATA [7:0] | | | | | | | | XX |

**Description**

This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.

**PGM_ADR [2:0]**: The select bits of ID1, ID2, ID3 and VMF [6:0] programming.

| PGM_ADR [2:0] | | | Programmed NV Memory Selection |
|---|---|---|---|
| 0 | 0 | 0 | ID1 programming |
| 0 | 0 | 1 | ID2 programming |
| 0 | 1 | 0 | ID3 programming |
| 1 | 0 | 0 | VMF [6:0] programming |
| Others | | | Reserved |

**PGM_DATA [7:0]**: The programmed data.

**Restriction**

EXTC should be high to enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | PGM_ADR [2:0] | PGM_DATA [7:0] |
| Power ON Sequence | 3'b000 | MTP value |
| SW Reset | 3'b000 | MTP value |
| HW Reset | 3'b000 | MTP value |

## 8.3.21. NV Memory Protection Key (D1h)

| D1h | NVMPKEY (NV Memory Protection Key) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1h |
| 1st Parameter | 1 | 1 | ↑ | XX | KEY [23:16] | | | | | | | | 55h |
| 2nd Parameter | 1 | 1 | ↑ | XX | KEY [15:8] | | | | | | | | AAh |
| 3rd Parameter | 1 | 1 | ↑ | XX | KEY [7:0] | | | | | | | | 66h |
| Description | **KEY [23:0]:** NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted. | | | | | | | | | | | | |
| Restriction | EXTC should be high to enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value |
|---|---|
| Power ON Sequence | KEY [23:0]=55AA66h |
| SW Reset | KEY [23:0]=55AA66h |
| HW Reset | KEY [23:0]=55AA66h |

## 8.3.22. NV Memory Status Read (D2h)

<table>
<tr><th>D2h</th><th colspan="13">RDNVM (NV Memory Status Read)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>D2h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2ndParameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="3">ID2_CNT [2:0]</td><td>0</td><td colspan="3">ID1_CNT [2:0]</td><td>XX</td></tr>
<tr><td>3rdParameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>BUSY</td><td colspan="3">VMF_CNT [2:0]</td><td>0</td><td colspan="3">ID3_CNT [2:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">
ID1_CNT [2:0] / ID2_CNT [2:0] / ID3_CNT [2:0] / VMF_CNT [2:0]: NV memory program record. The bits will increase “+1” automatically after writing the PGM_DATA [7:0] to NV memory.
<table>
<tr><th colspan="3">ID1_CNT [2:0] / ID2_CNT [2:0]<br>ID3_CNT [2:0] / VMF_CNT [2:0]</th><th>Description</th></tr>
<tr><td colspan="3">Status</td><td>Availability</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No Programmed</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Programmed 1 time</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Programmed 2 times</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Programmed 3 times</td></tr>
</table>
BUSY: The status bit of NV memory programming.
<table>
<tr><th>BUSY</th><th>The Status of NV Memory</th></tr>
<tr><td>0</td><td>Idle</td></tr>
<tr><td>1</td><td>Busy</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="5">Default Value</th></tr>
<tr><th>ID3_CNT</th><th>ID2_CNT</th><th>ID1_CNT</th><th>VMF_CNT</th><th>BUSY</th></tr>
<tr><td>Power ON Sequence</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>SW Reset</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>HW Reset</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
</table>
</td></tr>
</table>

## 8.3.23. Read ID4 (D3h)

| D3h | RDID4 (Read ID4) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3h |
| 1st Parameter | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | X |
| 2ndParameter | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| 3rdParameter | 1 | ↑ | 1 | XX | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 93h |
| 4th Parameter | 1 | ↑ | 1 | XX | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41h |
| Description | Read IC device code.<br>The 1st parameter is dummy read period.<br>The 2nd parameter means the IC version.<br>The 3rd and 4th parameter mean the IC model name. | | | | | | | | | | | | |
| Restriction | EXTC should be high to enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value |
|---|---|
| Power ON Sequence | 24'h009341h |
| SW Reset | 24'h009341h |
| HW Reset | 24'h009341h |

## 8.3.24. Positive Gamma Correction (E0h)

| E0h | PGAMCTRL (Positive Gamma Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP63 [3:0] | | | | 08 |
| 2ndParameter | 1 | 1 | ↑ | XX | 0 | 0 | VP62 [5:0] | | | | | | |
| 3rdParameter | 1 | 1 | ↑ | XX | 0 | 0 | VP61 [5:0] | | | | | | |
| 4th Parameter | 1 | 1 | ↑ | X | 0 | 0 | 0 | 0 | VP59 [3:0] | | | | 05 |
| 5th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VP57 [4:0] | | | | | |
| 6th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP50 [3:0] | | | | 09 |
| 7th Parameter | 1 | 1 | ↑ | XX | 0 | VP43 [6:0] | | | | | | | |
| 8th Parameter | 1 | 1 | ↑ | XX | VP27 [3:0] | | | | VP36 [3:0] | | | | |
| 9th Parameter | 1 | 1 | ↑ | XX | 0 | VP20 [6:0] | | | | | | | |
| 10thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP13 [3:0] | | | | 0B |
| 11thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VP6 [4:0] | | | | | |
| 12thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP4 [3:0] | | | | 00 |
| 13thParameter | 1 | 1 | ↑ | XX | 0 | 0 | VP2 [5:0] | | | | | | |
| 14thParameter | 1 | 1 | ↑ | XX | 0 | 0 | VP1 [5:0] | | | | | | |
| 15thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VP0 [3:0] | | | | 00 |

| | |
|---|---|
| Description | Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. |
| Restriction | EXTC should be high to enable this command |
| Register Availability | |
| Default | |

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

## 8.3.25. Negative Gamma Correction (E1h)

| E1h | NGAMCTRL (Negative Gamma Correction) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1h |
| 1st Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN63 [3:0] | | | | 08 |
| 2ndParameter | 1 | 1 | ↑ | XX | 0 | 0 | VN62 [5:0] | | | | | | |
| 3rdParameter | 1 | 1 | ↑ | XX | 0 | 0 | VN61 [5:0] | | | | | | |
| 4th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN59 [3:0] | | | | 07 |
| 5th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VN57 [4:0] | | | | | |
| 6th Parameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN50 [3:0] | | | | 05 |
| 7th Parameter | 1 | 1 | ↑ | XX | 0 | VN43 [6:0] | | | | | | | |
| 8th Parameter | 1 | 1 | ↑ | XX | VN36 [3:0] | | | | VN27 [3:0] | | | | |
| 9th Parameter | 1 | 1 | ↑ | XX | 0 | VN20 [6:0] | | | | | | | |
| 10thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN13 [3:0] | | | | 04 |
| 11thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | VN6 [4:0] | | | | | |
| 12thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN4 [3:0] | | | | 0F |
| 13thParameter | 1 | 1 | ↑ | XX | 0 | 0 | VN2 [5:0] | | | | | | |
| 14thParameter | 1 | 1 | ↑ | XX | 0 | 0 | VN1 [5:0] | | | | | | |
| 15thParameter | 1 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | VN0 [3:0] | | | | 0F |

| | |
|---|---|
| Description | Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. |
| Restriction | EXTC should be high to enable this command |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

| | |
|---|---|
| Default | |

## 8.3.26. Digital Gamma Control 1 (E2h)

| E2h | DGAMCTRL (Digital Gamma Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2h |
| 1st Parameter | 1 | 1 | ↑ | XX | RCA0 [3:0] | | | | BCA0 [3:0] | | | | XX |
| : | 1 | 1 | ↑ | XX | RCAx [3:0] | | | | BCAx [3:0] | | | | XX |
| 16th Parameter | 1 | 1 | ↑ | XX | RCA15 [3:0] | | | | BCA15 [3:0] | | | | XX |
| Description | **RCAx [3:0]:** Gamma Macro-adjustment registers for red gamma curve.<br>**BCAx [3:0]:** Gamma Macro-adjustment registers for blue gamma curve. | | | | | | | | | | | | |
| Restriction | EXTC should be high to enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | RCAx [3:0] | BCAx [3:0] |
| Power ON Sequence | TBD | TBD |
| SW Reset | TBD | TBD |
| HW Reset | TBD | TBD |

## 8.3.27. Digital Gamma Control 2(E3h)

| E3h | DGAMCTRL (Digital Gamma Control 2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3h |
| 1st Parameter | 1 | 1 | ↑ | XX | RFA0 [3:0] | | | | BFA0 [3:0] | | | | XX |
| : | 1 | 1 | ↑ | XX | RFAx [3:0] | | | | BFAx [3:0] | | | | XX |
| 64rdParameter | 1 | 1 | ↑ | XX | RFA63 [3:0] | | | | BFA63 [3:0] | | | | XX |
| Description | **RFAx [3:0]:** Gamma Micro-adjustment register for red gamma curve.<br>**BFAx [3:0]:** Gamma Micro-adjustment register for blue gamma curve. | | | | | | | | | | | | |
| Restriction | EXTC should be high to enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | RFAx [3:0] | BFAx [3:0] |
| Power ON Sequence | TBD | TBD |
| SW Reset | TBD | TBD |
| HW Reset | TBD | TBD |

## 8.3.28. Interface Control (F6h)

| F6h | IFCTL (16bits Data Format Selection) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | F6h |
| 1st Parameter | 1 | 1 | ↑ | XX | MY_ EOR | MX_ EOR | MV_ EOR | 0 | BGR_ EOR | 0 | 0 | WE MODE | 01 |
| 2nd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | EPF [1] | EPF [0] | 0 | 0 | MDT [1] | MDT [0] | 00 |
| 3rd Parameter | 1 | 1 | ↑ | XX | 0 | 0 | ENDIAN | 0 | DM [1] | DM [0] | RM | RIM | 00 |

Description

**MY_EOR / MX_EOR / MV_EOR / BGR_EOR:**

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

**MDT [1:0]:** Select the method of display data transferring.

**WEMODE:** Memory write control

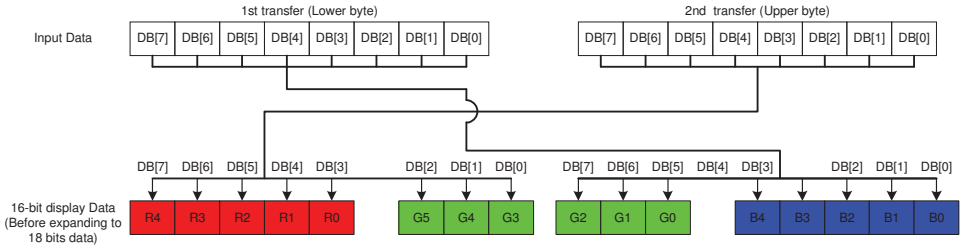
WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

**ENDIAN:** Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

| ENDIAN | Data transfer Mode |
|---|---|
| 0 | Normal (MSB first, default) |
| 1 | Little Endian (LSB first) |

*Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.*




**DM [1:0]:** Select the display operation mode.

| DM [1] | DM [0] | Display Operation Mode |
|---|---|---|
| 0 | 0 | Internal clock operation |
| 0 | 1 | RGB Interface Mode |
| 1 | 0 | VSYNC interface mode |
| 1 | 1 | Setting disabled |

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

**RM:** Select the interface to access the GRAM.

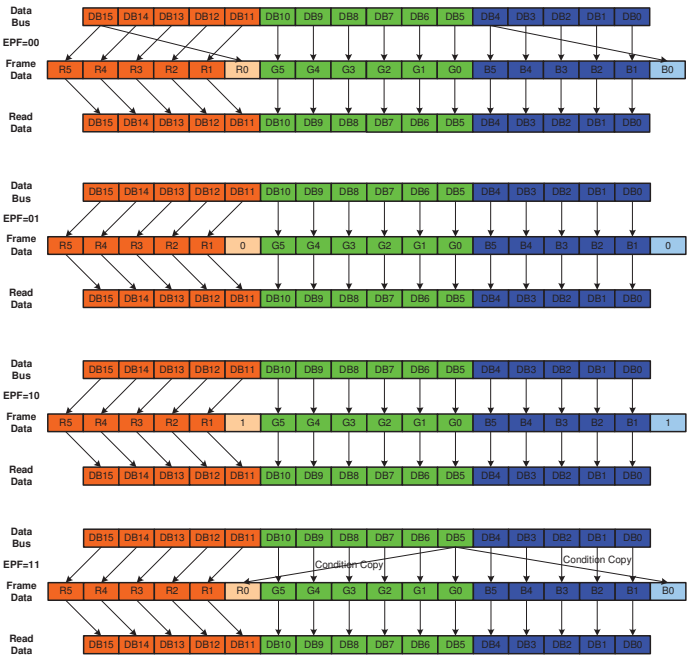
Set RM to "1" when writing display data by the RGB interface.

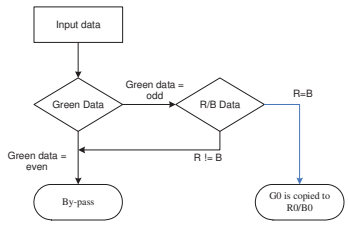
| RM | Interface for RAM Access |
|---|---|
| 0 | System interface/VSYNC interface |
| 1 | RGB interface |

**RIM:** Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

| RIM | COLMOD [6:4] | RGB Interface Mode |
|---|---|---|
| 0 | 110 (262K color) | 18- bit RGB interface (1 transfer/pixel) |
| | 101 (65K color) | 16- bit RGB interface (1 transfer/pixel) |
| 1 | 110 (262K color) | 6- bit RGB interface (3 transfer/pixel) |
| | 101 (65K color) | 6- bit RGB interface (3 transfer/pixel) |

**EPF [1:0]**: 65K color mode data format.




| EPF [1:0] | Expand 16 bbp (R,G,B) to 18bbp (R,G,B) |
|---|---|
| 00 | MSB is inputted to LSB<br>r [5:0] = {R [4:0], R [4]}<br>g [5:0] = {G [5:0]}<br>b [5:0] = {B [4:0], B [4]} |

| | | |
|---|---|---|
| | 01 | "0" is inputted to LSB<br>r [5:0] = {R [4:0], 0}<br>g [5:0] = {G [5:0]}<br>b [5:0] = {B [4:0], 0}<br><br>Exception:<br>R [4:0], B[4:0] = 5'h1F → r [5:0], b[5:0] = 6'h3F |
| | 10 | "1" is inputted to LSB<br>r [5:0] = {R [4:0], 1}<br>g [5:0] = {G [5:0]}<br>b [5:0] = {B [4:0], 1}<br><br>Exception:<br>R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00 |
| | 11 | Compare R [4:0], G [5:1], B [4:0] case:<br>Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}<br>Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]}<br>Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]}<br>Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} |

Restriction: EXTC should be high to enable this command

Register Availability

| Status | Availability |
|---|---|
| Normal Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Normal Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode OFF, Sleep OUT | Yes |
| Partial Mode ON, Idle Mode ON, Sleep OUT | Yes |
| Sleep IN | Yes |

Default

| Status | Default Value | | | | | | |
|---|---|---|---|---|---|---|---|
| | EPF [1:0] | MDT [1:0] | ENDIAN | WEMODE | DM [1:0] | RM | RIM |
| Power ON Sequence | 2'b00 | 2'b00 | 1'b0 | 1'b1 | 2'b00 | 1'b0 | 1'b0 |
| SW Reset | 2'b00 | 2'b00 | 1'b0 | 1'b1 | 2'b00 | 1'b0 | 1'b0 |
| HW Reset | 2'b00 | 2'b00 | 1'b0 | 1'b1 | 2'b00 | 1'b0 | 1'b0 |