PDS0101

Introduction to Digital Systems

Latches & Flip-flops II

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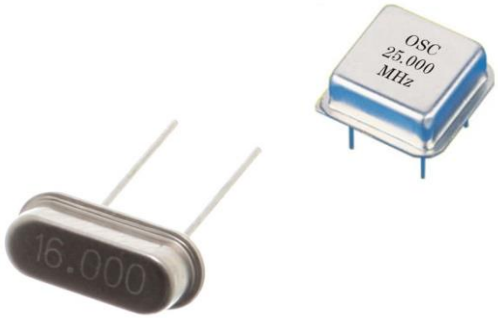
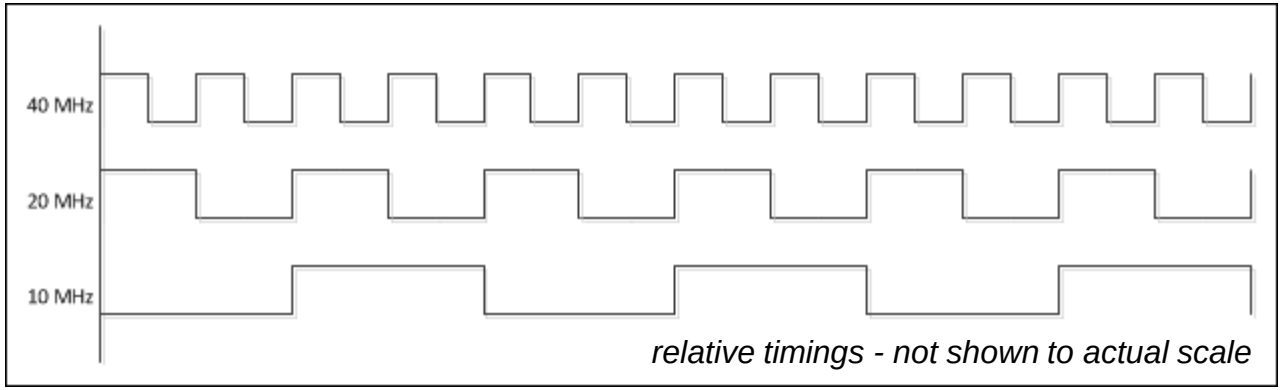
Lecture outcome

- By the end of today's lecture you should
  - learn to define the *clock*
  - be able to define edge-triggered flip-flops and its variants
  - learn the difference between latches and flip-flops
  - be able to identify logic symbols of different flip-flops
  - be able to compare and discuss the operations of S-R, D and J-K edge triggered flip-flops and explain differences using truth tables
  - be able to discuss asynchronous inputs of flip-flops

Clock signal

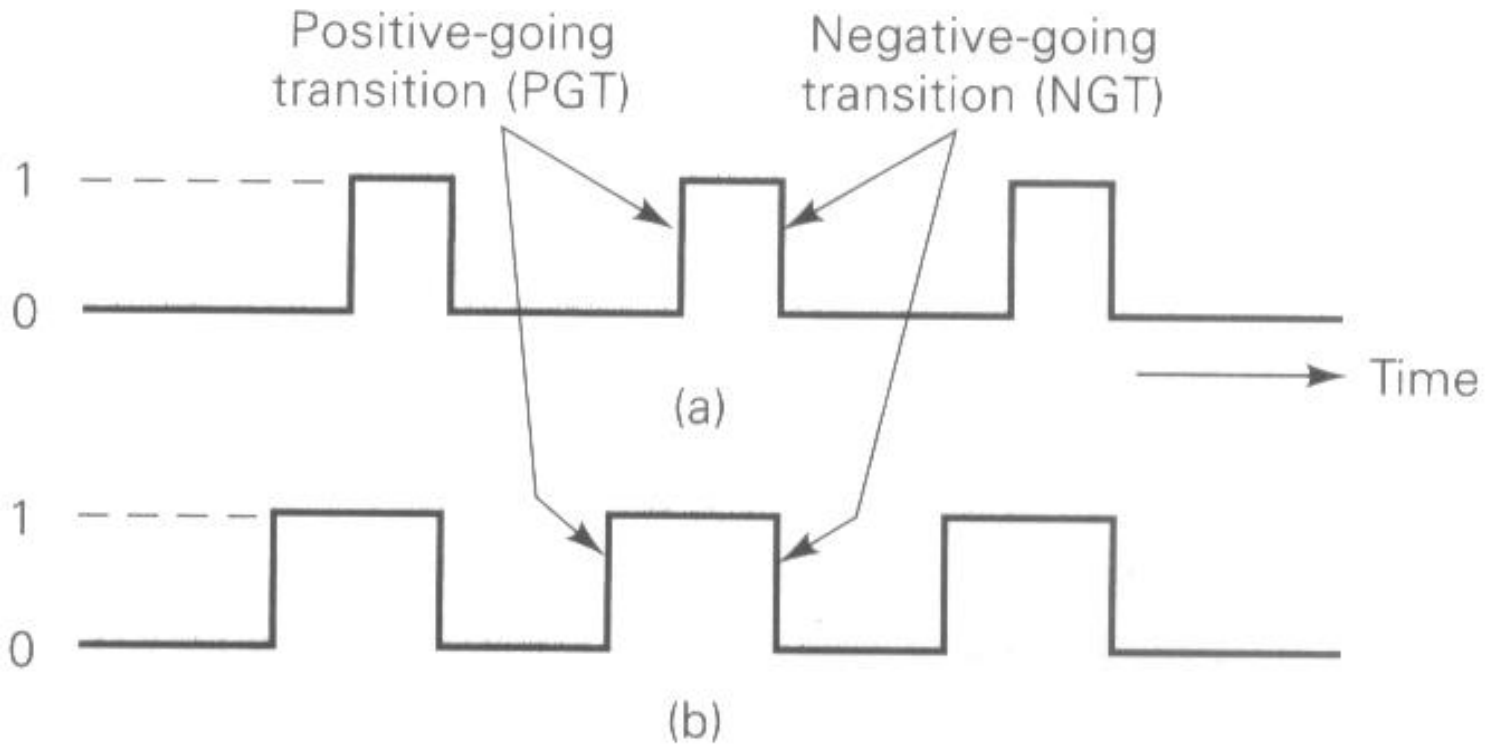
- The clock signal is a rectangular pulse train or square wave which periodic
  - In logic circuits, it is generated by a oscillator or clock generator





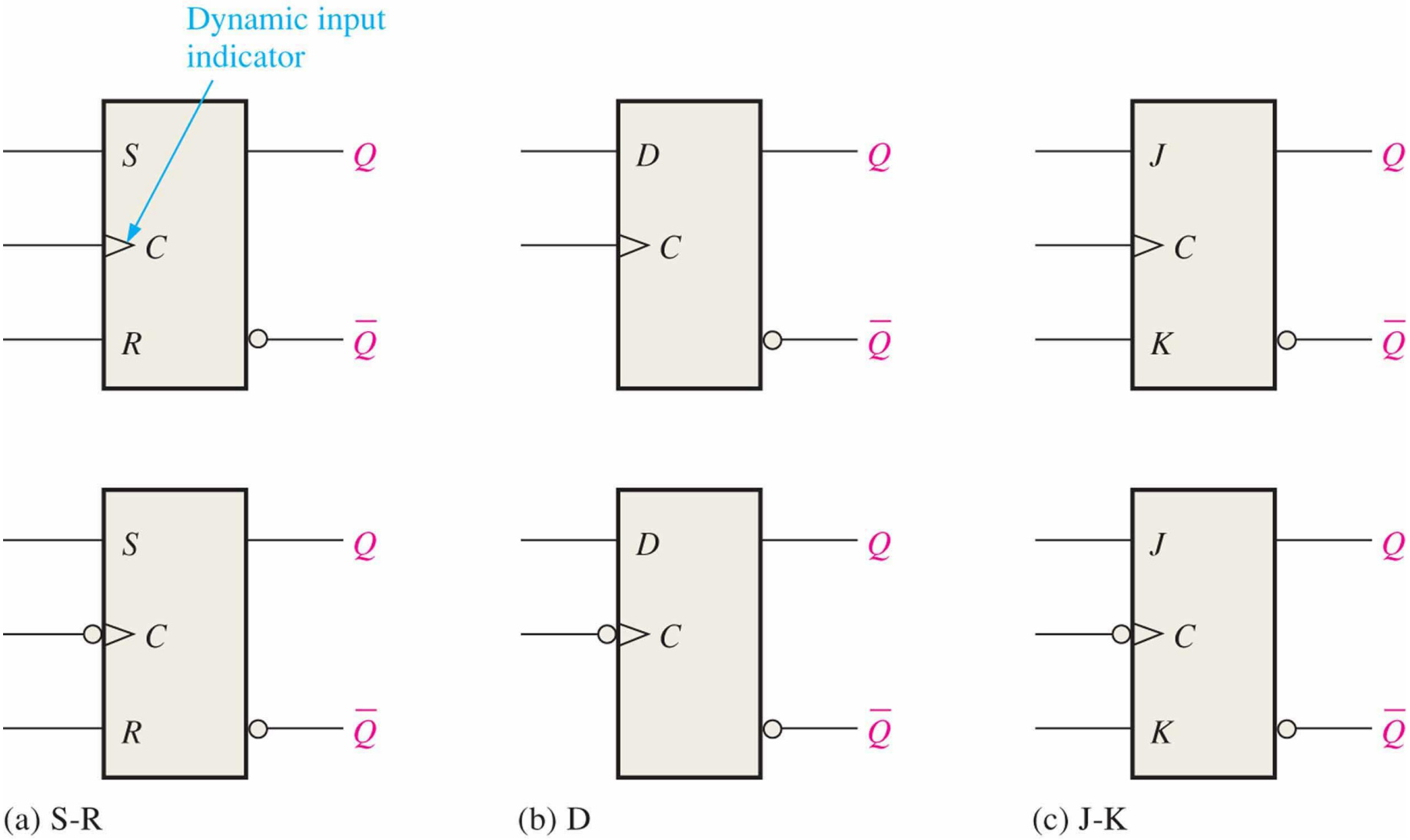
- Digital systems can operate either asynchronously or synchronously.
  - Asynchronous systems - outputs of logic circuit can change state any time one or more of the inputs change.
  - Synchronous systems - the exact time any output can change states are determined by the clock signal (i.e. state changes are dictated by the clock)

- Clock signals can trigger state changes based on their two transitions
  - positive-going transition – changes from 0 to 1 (i.e. rising edge)
  - negative-going transition – changes from 1 to 0 (falling)



Edge-triggered flip-flop

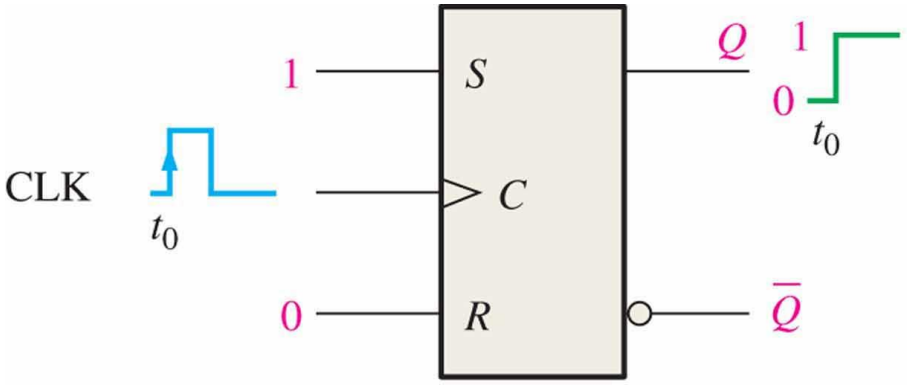
- A flip-flop differs from a latch in the manner of when it changes states
- A flip-flop is a clocked device, in which only the clock edge determines when a new bit is entered
- The edge-triggered (ET) flip-flop changes state either at the +ve or –ve edge of a clock pulse and reacts to its inputs only at this transition of the clock
- Three types of flip-flops are covered
  - ET S-R flip-flop
  - ET D flip-flop
  - ET J-K flip-flop
- All three types can be +ve/-ve triggered and depicted with bubble at the CLK
- The key to identifying a flip-flop by its logic symbol is the presence of a small triangle inside the block at the clock input – this is the dynamic input indicator ▷


Dynamic input indicator
S
C
R
Q
$\overline{Q}$
D
C
Q
$\overline{Q}$
J
C
K
Q
$\overline{Q}$
S
C
R
Q
$\overline{Q}$
D
C
Q
$\overline{Q}$
J
C
K
Q
$\overline{Q}$

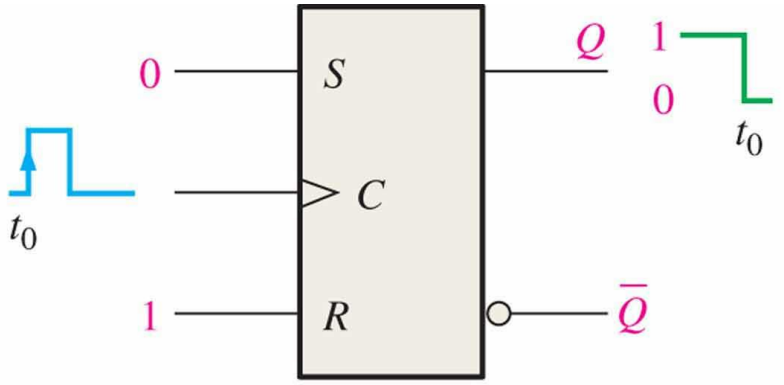
(a) S-R (b) D (c) J-K

ET S-R flip-flop

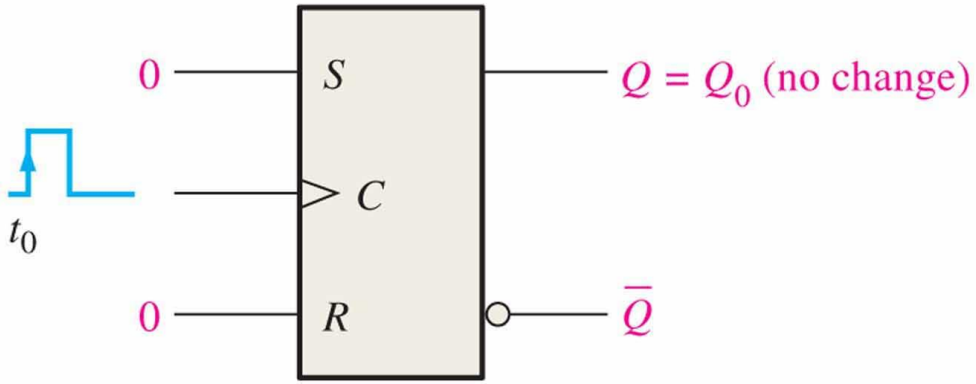
- ET S-R flip-flop is a conventional S-R latch with the EN input replaced with the clock
- The S-R inputs are called synchronous inputs because the data is only transferred to the flip-flop's output only on the triggering edge of the clock
  - The ET S-R flip-flop follows the S-R latch output states
  - If both S-R inputs are simultaneously switch HIGH, the next clock trigger will create an invalid condition



(a) $S = 1$, $R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



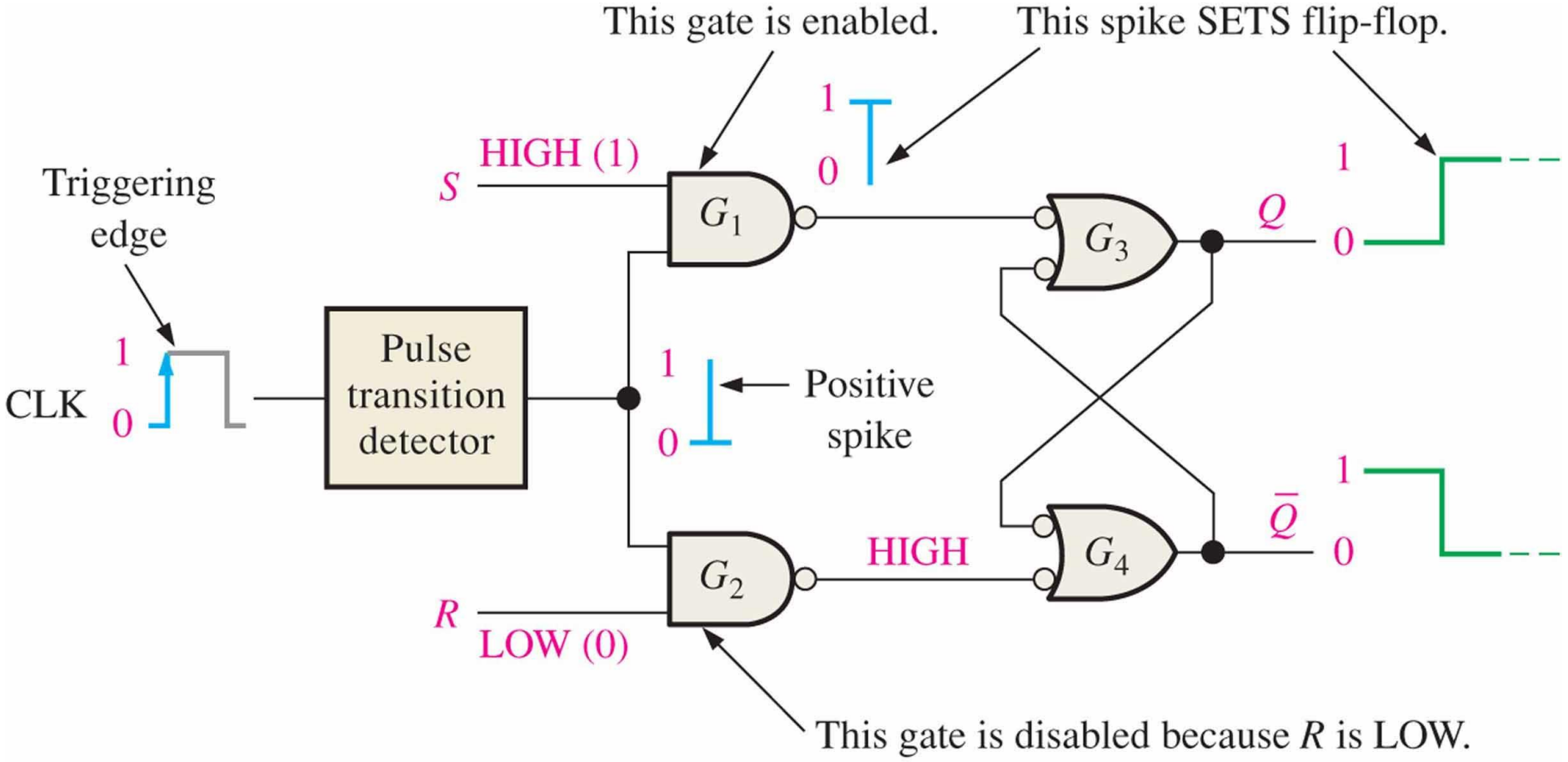
(b) $S = 0$, $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

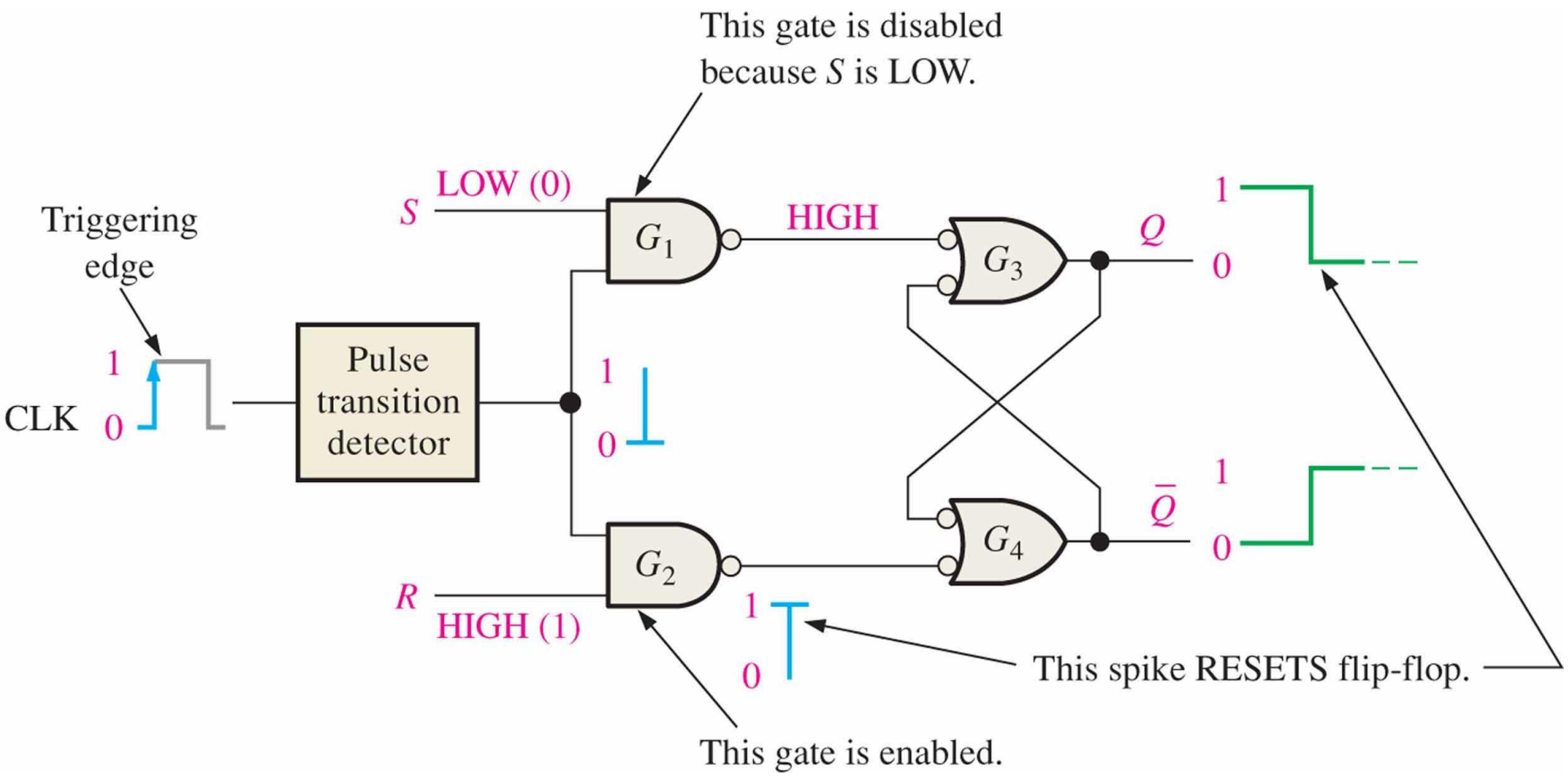
Setting the ET S-R flip-flop

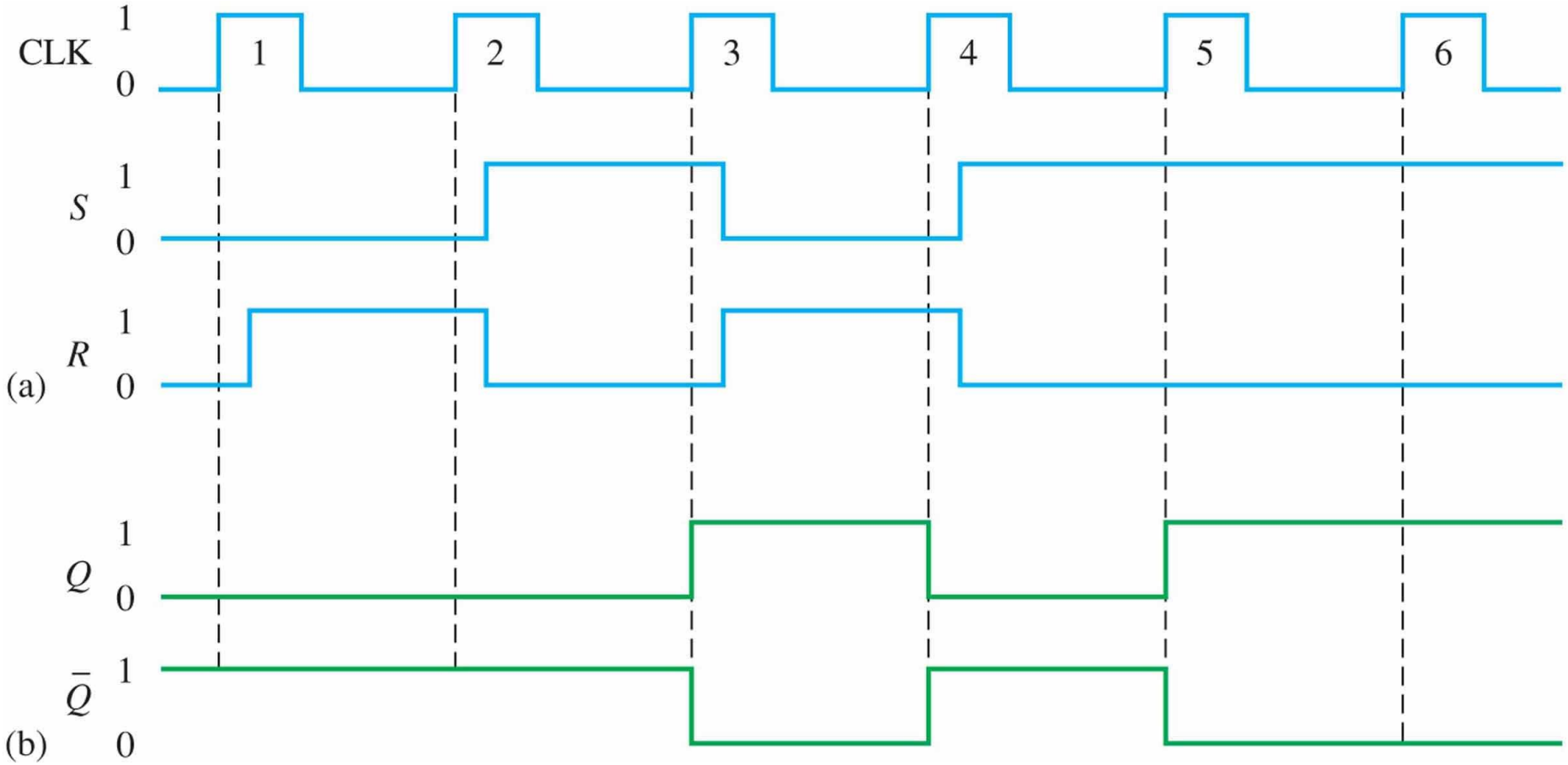
- To set the ET S-R flip-flop (assuming that it is currently in RESET state where Q=0 and S=R=C=0) the S input is made HIGH and apply a clock pulse CLK to generate a pulse
- Because of input S=1 and the clock pulse, the output of G1 does LOW for a short period and causes output Q at G3 to go HIGH (SET)
- Both inputs to G4 are then HIGH forcing Q'1 to be LOW
  - This LOW on Q' is fedback to input of G3 thus ensuring that the Q output remains at HIGH


This gate is enabled.
This spike SETS flip-flop.
Triggering edge
CLK
1
0
S
HIGH (1)
R
LOW (0)
Pulse transition detector
G_1
G_2
G_3
G_4
1
0
Positive spike
HIGH
Q
$\bar{Q}$
This gate is disabled because R is LOW.

Resetting the ET S-R flip-flop

- To reset the flip-flop the input to R is made HIGH and a clock pulse is applied thus inversing the SET actions



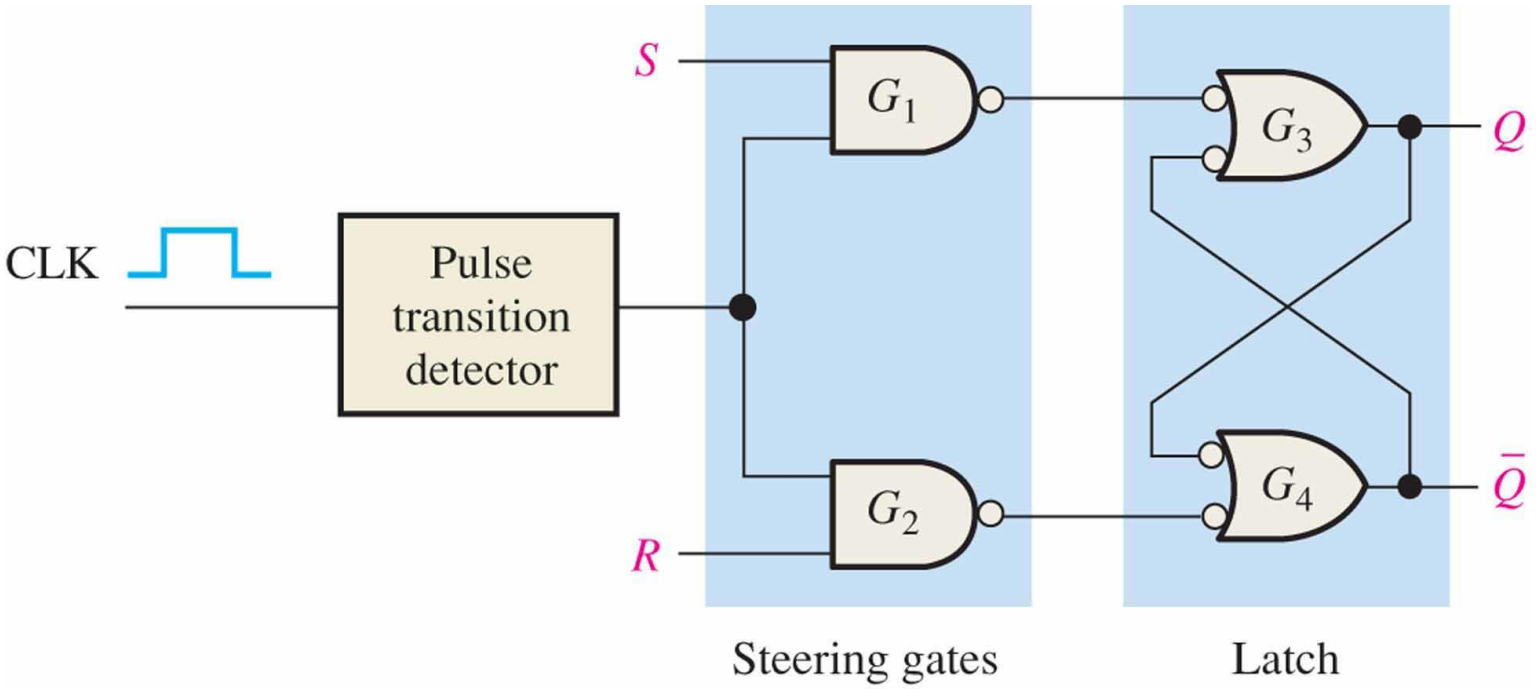

CLK
1
0
1
2
3
4
5
6
S
1
0
R
1
0
(a)
Q
1
0
$\bar{Q}$
1
0
(b)

Flip-flop logic – pulse detector

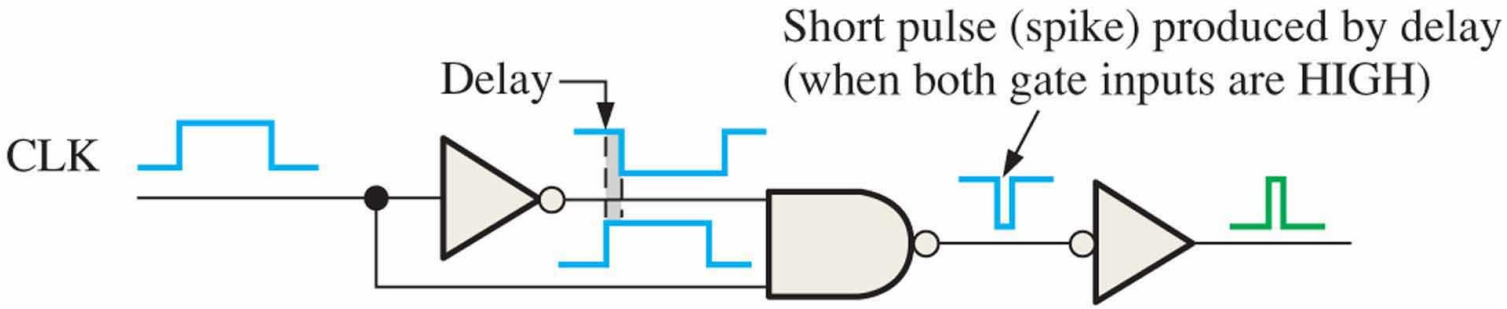
- A simplified logic circuit for the ET S-R flip-flop is shown in the next slide
- Notice that the clock controls the *pulse transition detector* which in turn produces a very short durationl spike on the +ve-going transition (rising edge) of the clock pulse → this is why the transitions only occur at the beginning of the clock pulse and not the entire duration of the pulse width

- A very basic pulse detector implements a delay towards a NAND gate so that the inverted signal arrives a few nanoseconds *after* the true clock pulse thus producing an output spike of only a few nanoseconds
  - in a –ve-edge triggered flip-flop, the clock pulse is inverted BEFORE input

- In the circuit, the first section (steering section) controls the clock spike to either inputs at G3 or G4 → to SET/RESET the latch section
- The second section (latch) functions like the normal S-R latch



(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

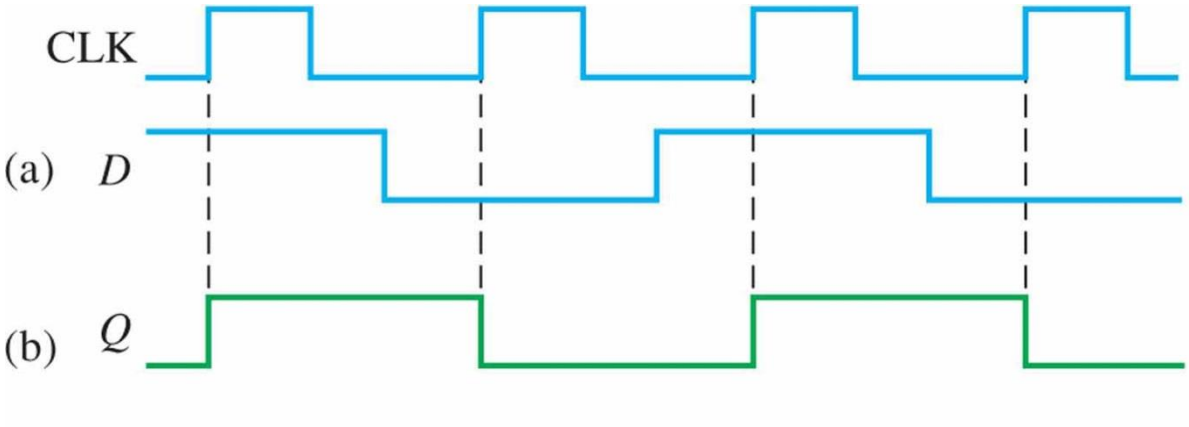


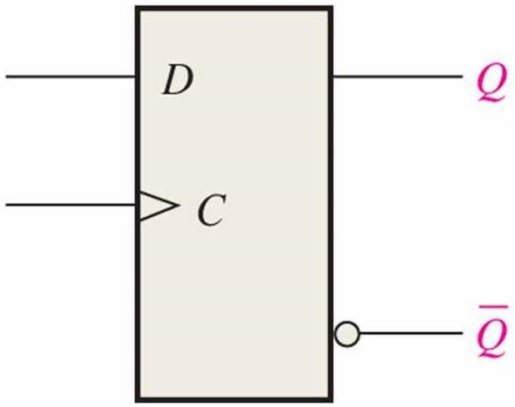
(b) A type of pulse transition detector

From this point onwards, the flip-flops shown are all to be edge-triggered and thus the reference to the words “edge-triggered” are assumed to be present but not shown

D flip-flop

- The D flip-flop only has one (1) input D for data in addition to the CLK
- If there is a HIGH on D when the clock pulse is applied the flip-flop will SET, else if there is a LOW then it will RESET.
- There is no invalid condition with the D flip-flop





D flip-flop truth tables

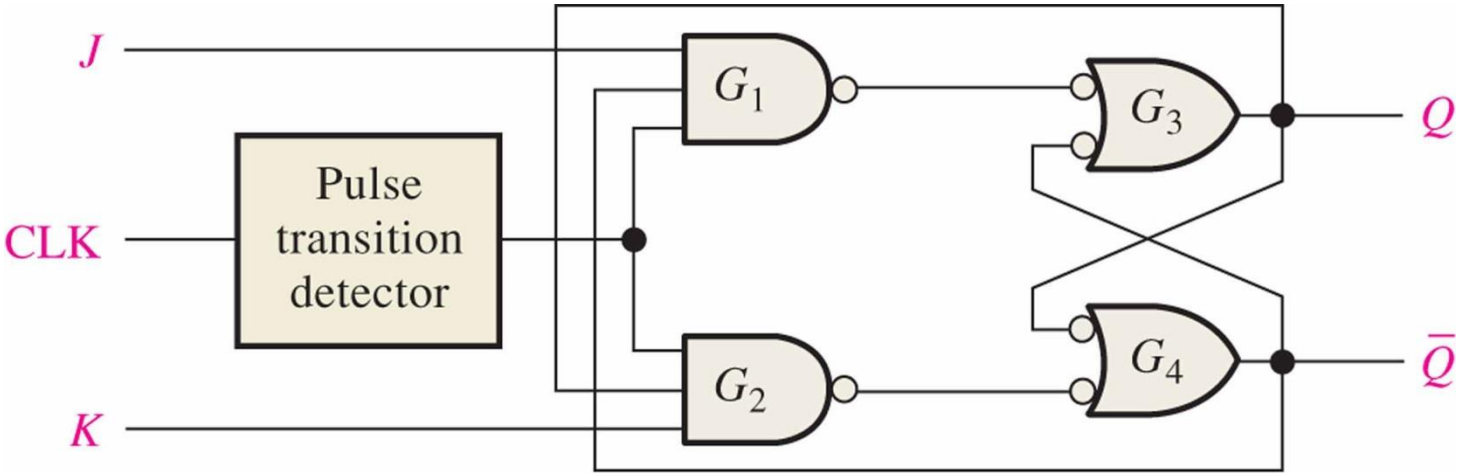
- The truth table for a positive-edge triggered D flip-flop shows an up arrow to remind you that it is sensitive to its D input only on the rising edge of the clock; otherwise it is latched.
- The truth table for a negative-edge triggered D flip-flop is identical except for the direction of the arrow.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↑	1	0	SET
0	↑	0	1	RESET

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↓	1	0	SET
0	↓	0	1	RESET

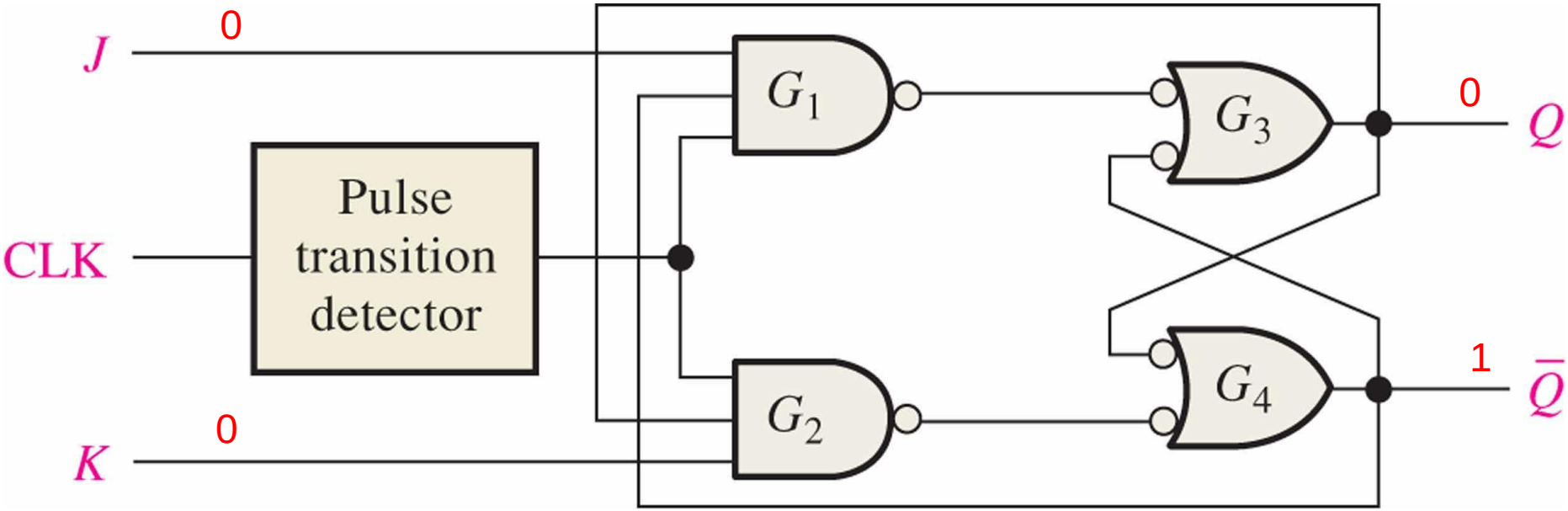
J-K flip-flop

- Latches/flip-flops with two inputs had to problem of having an invalid state if both inputs were simultaneously active
- To prevent this the J-K flip-flop was invented (by Jack Kilby hence the input alphabets) to ensure no invalid state can occur
  - The functioning of the J-K flip-flop is identical to the S-R flip-flop in all its SET, RESET and no-change operations.
  - If differs from the S-R flip-flop by having its Q and Q' outputs fedback to opposing gates at the steering section of the flip-flop and an additional 'condition' to the gates
- The diagram below shows a +ve ET J-K flip-flop

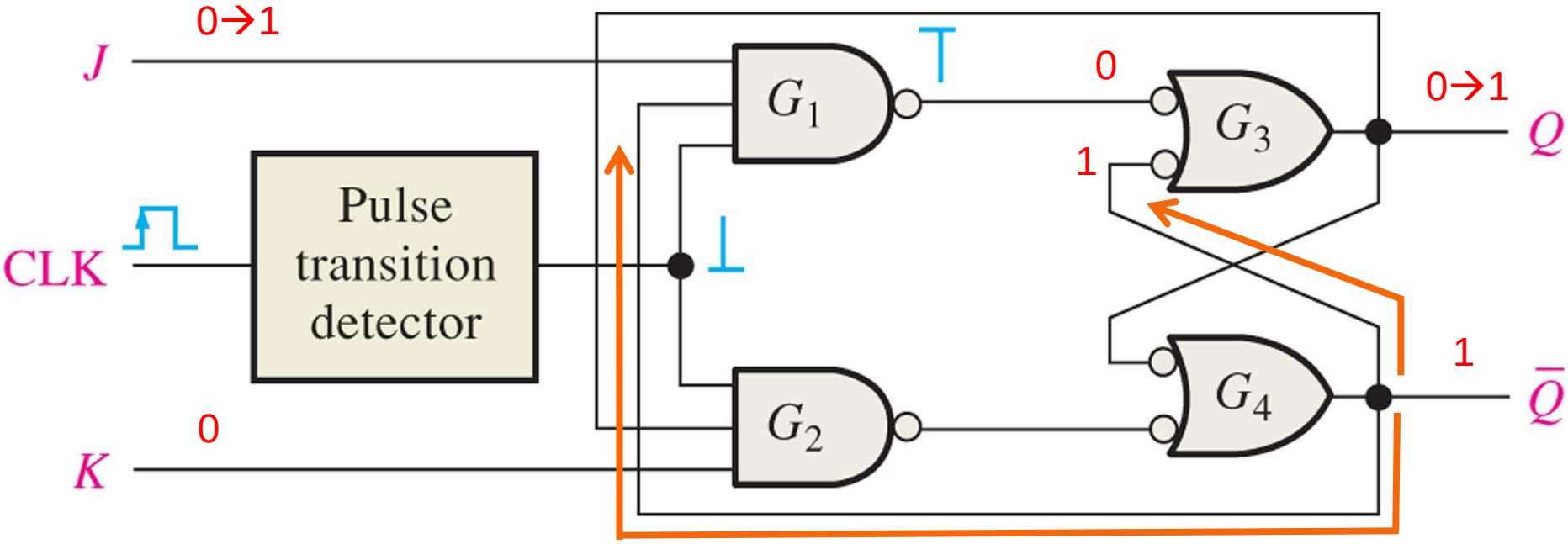


J-K flip-flop states

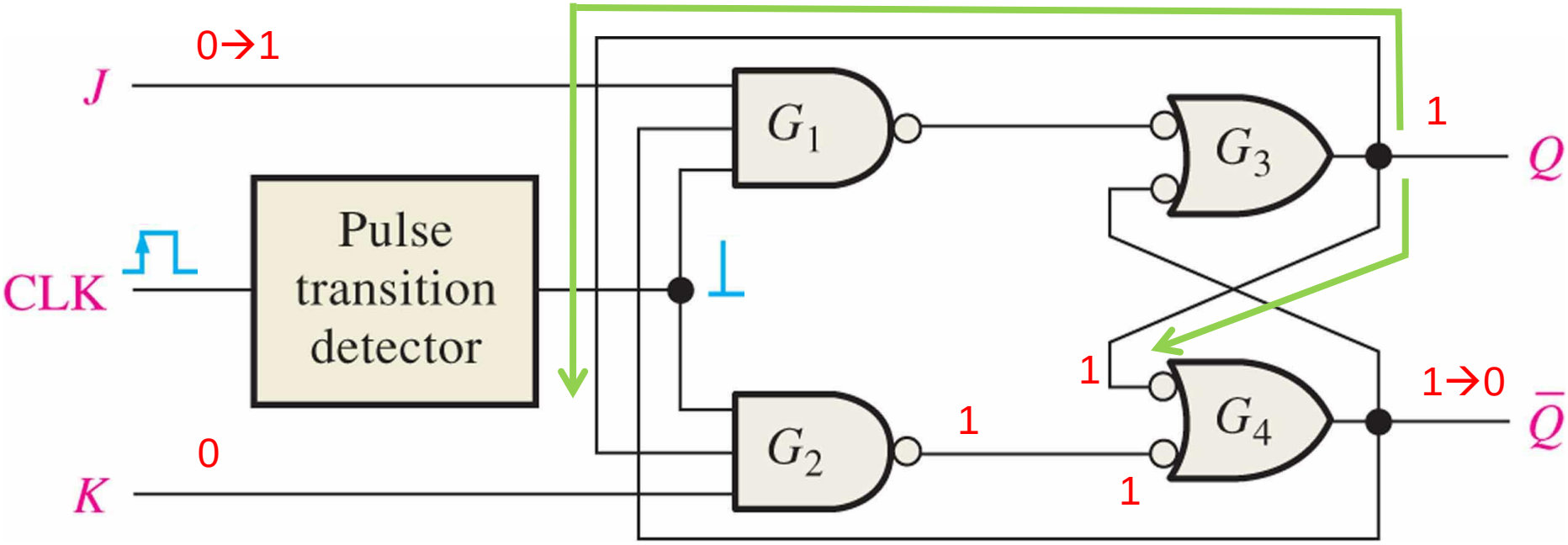
- Assume the flip-flop in the previous diagram is in RESET state with the following resting state



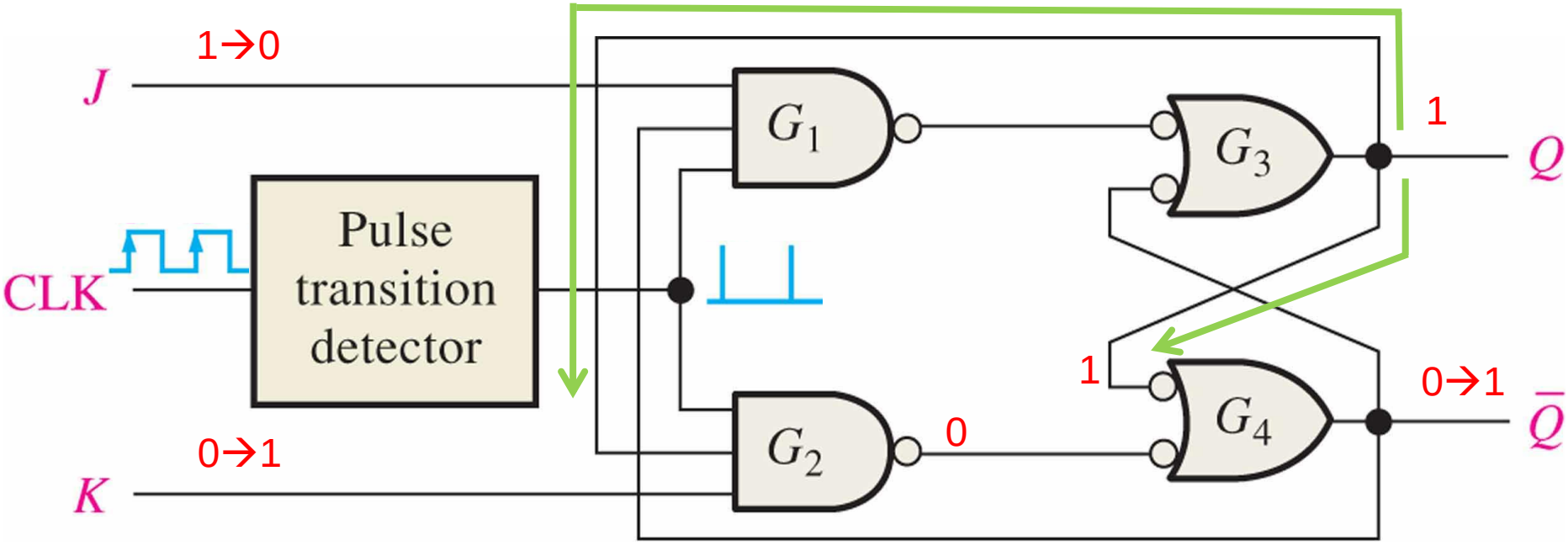
- To set the flip-flop, input J is made HIGH
- With the CLK, a spike at (1) passes through G1
  - Because Q'=1 and J=1 and CLK=1, G1=0 (NAND)
  - Output of G3 becomes Q=1



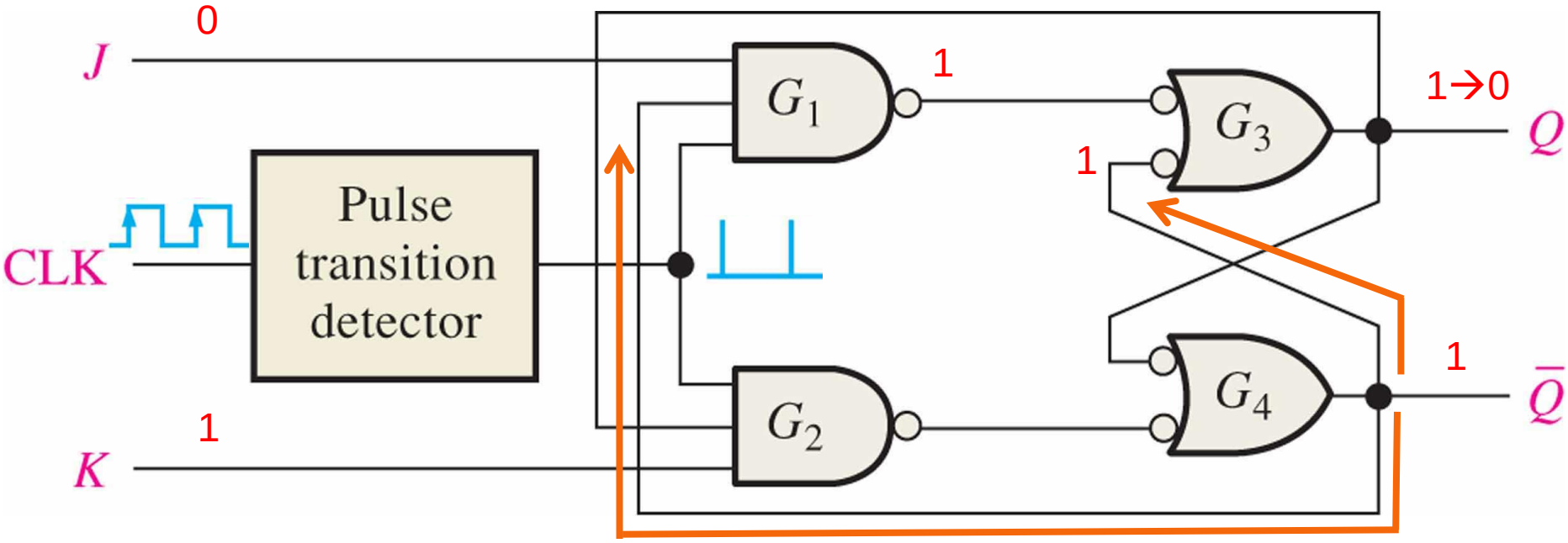
- When Q=1 this is fedback to G2 which outputs a HIGH towards the inputs of G4
- With both inputs to G4 (negative-OR) HIGH, the output of Q' switches to LOW thus the flip-flop is now SET



- If K is made HIGH (to reset), the next clock spike will pass through G2 in the steering section
- With all inputs to G2 at HIGH, the output is LOW thus making the inputs to G4 satisfy the condition to output Q'=1

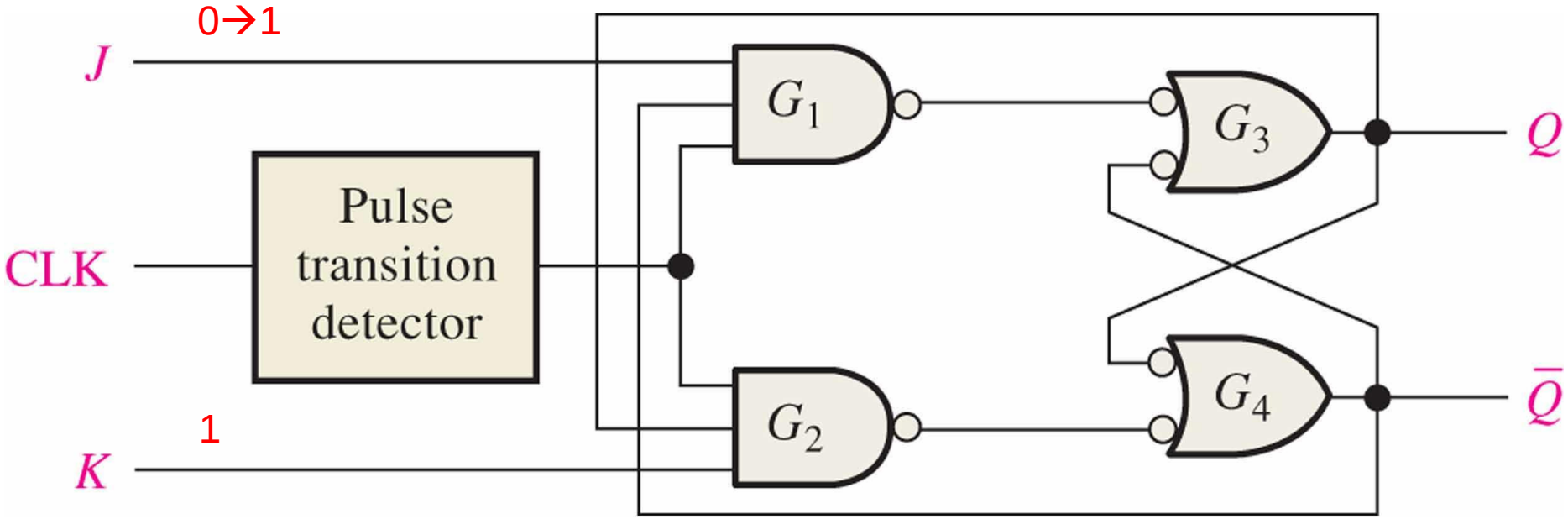


- With Q'=1, the inputs into G1 now create a HIGH output towards G3
- With both inputs to G3 high, the output Q now switches to LOW and thus RESETs the flip-flop

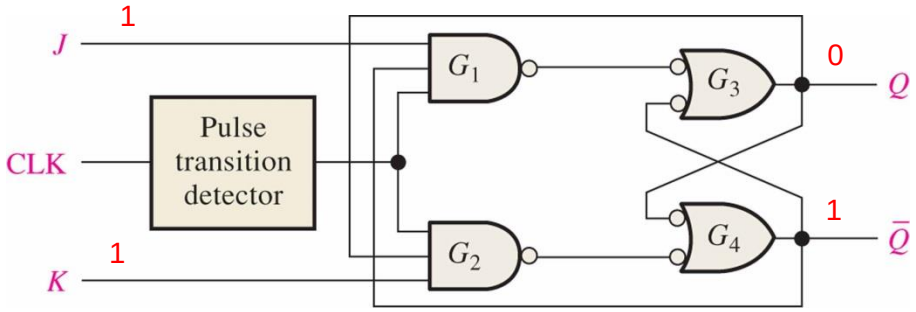


J-K flip-flop – invalid state?

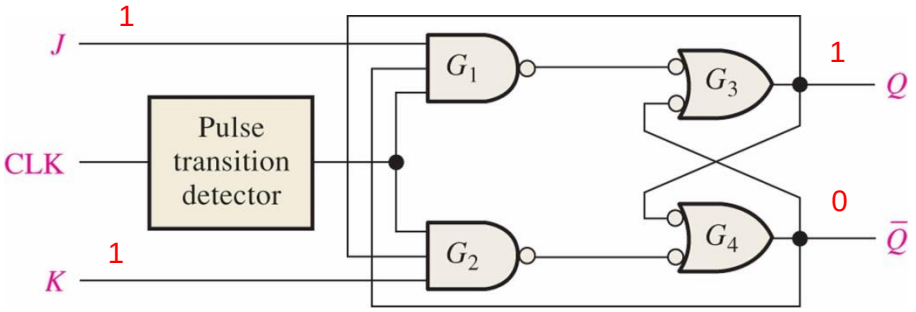
- If inputs J and K were both made LOW, the flip-flop would remain in whatever state is was in (i.e. no change)
- However when both J and K are made HIGH ? The following conditions occur depending on whether the flip-flop was in SET or RESET state



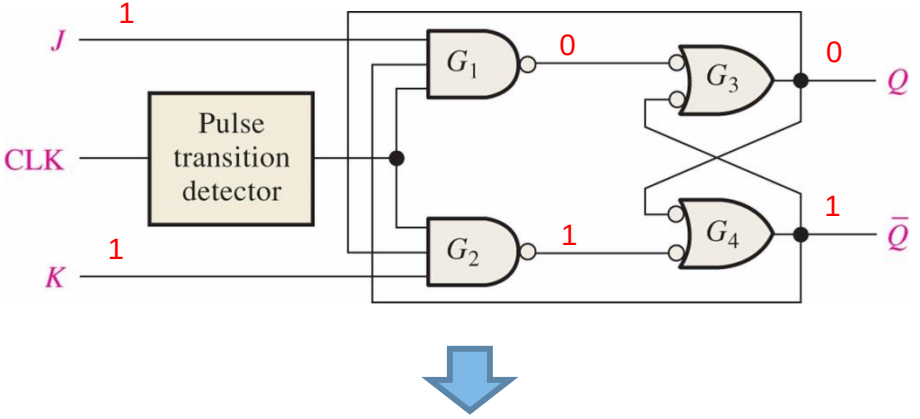
G1 inputs = 111



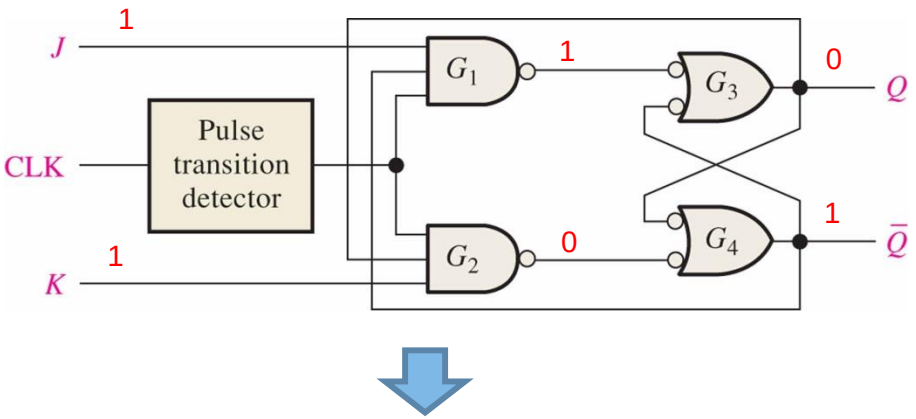
G1 inputs = 101

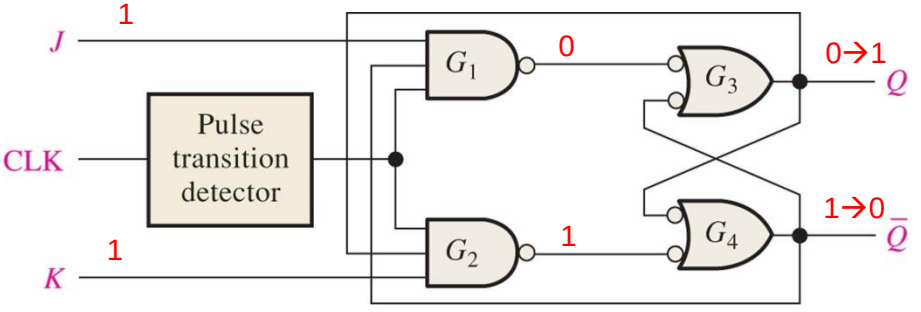


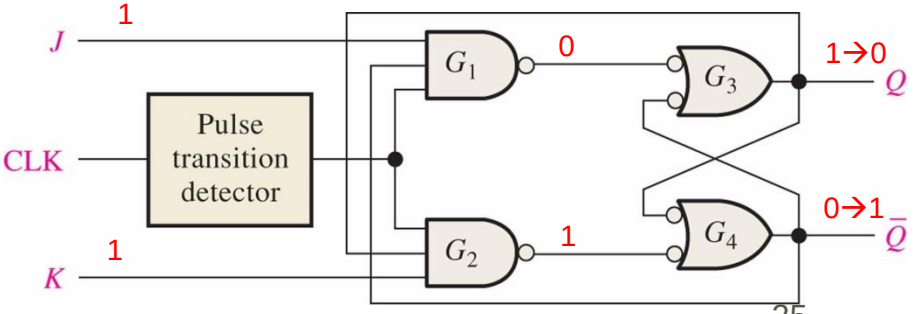
G2 inputs = 101



G2 inputs = 111



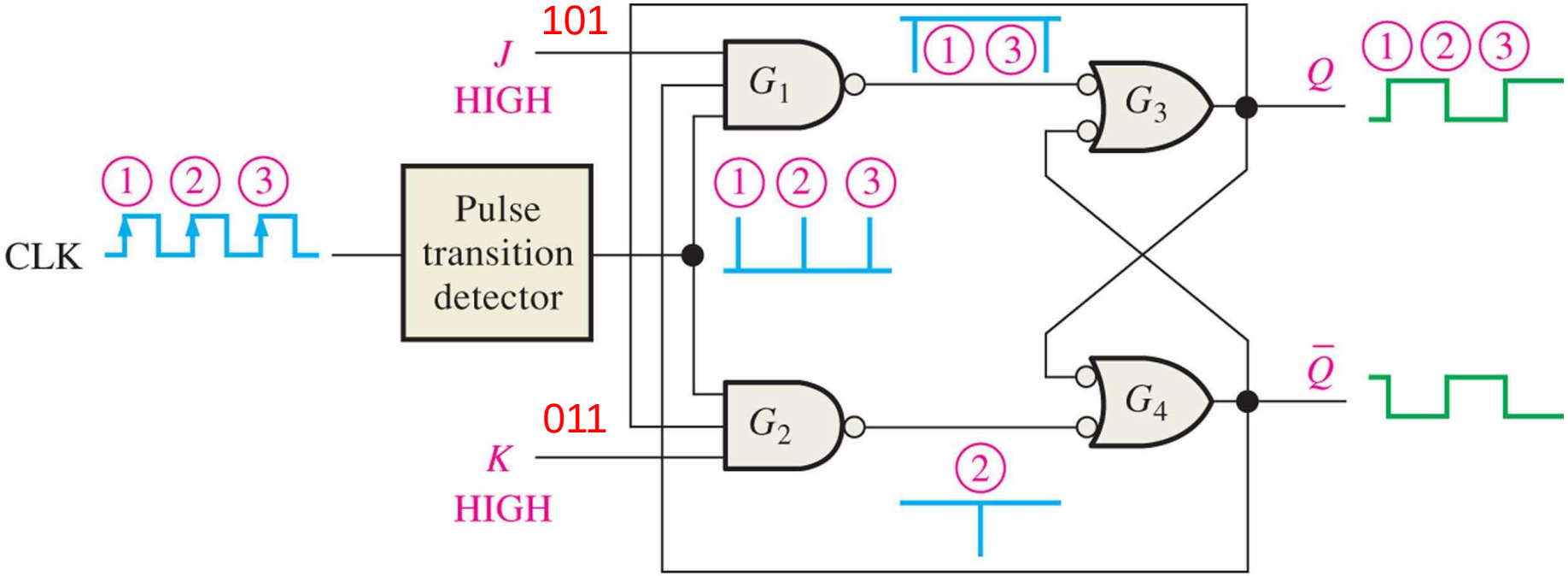




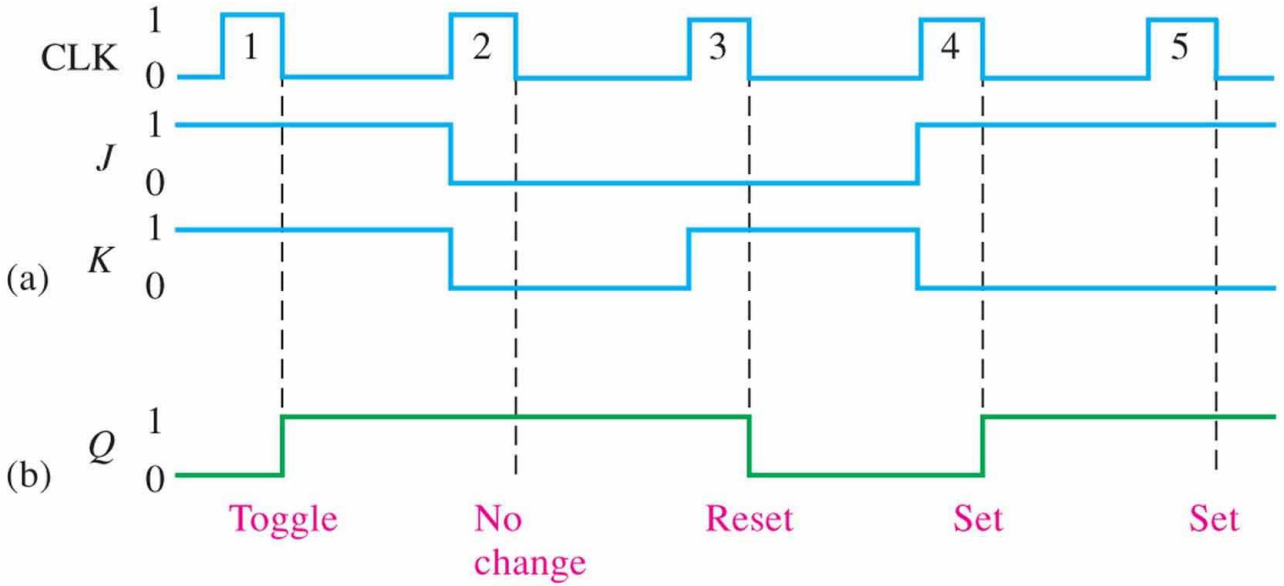
- With each clock pulse, when the J-K flip-flop encounters HIGH inputs simultaneously it changes the outputs to the opposite state
  - This mode is known as the toggle mode/operation

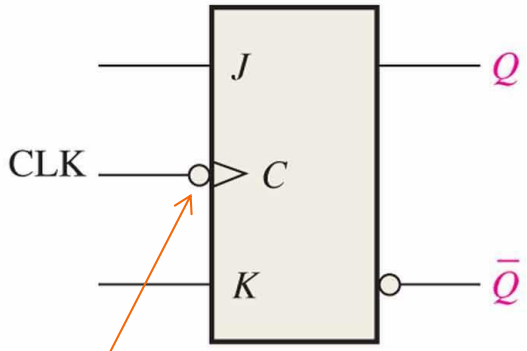
- The table below summarizes the logical operation of the J-K flip-flop (the –ve ET J-K is identical except triggered on falling edge)

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

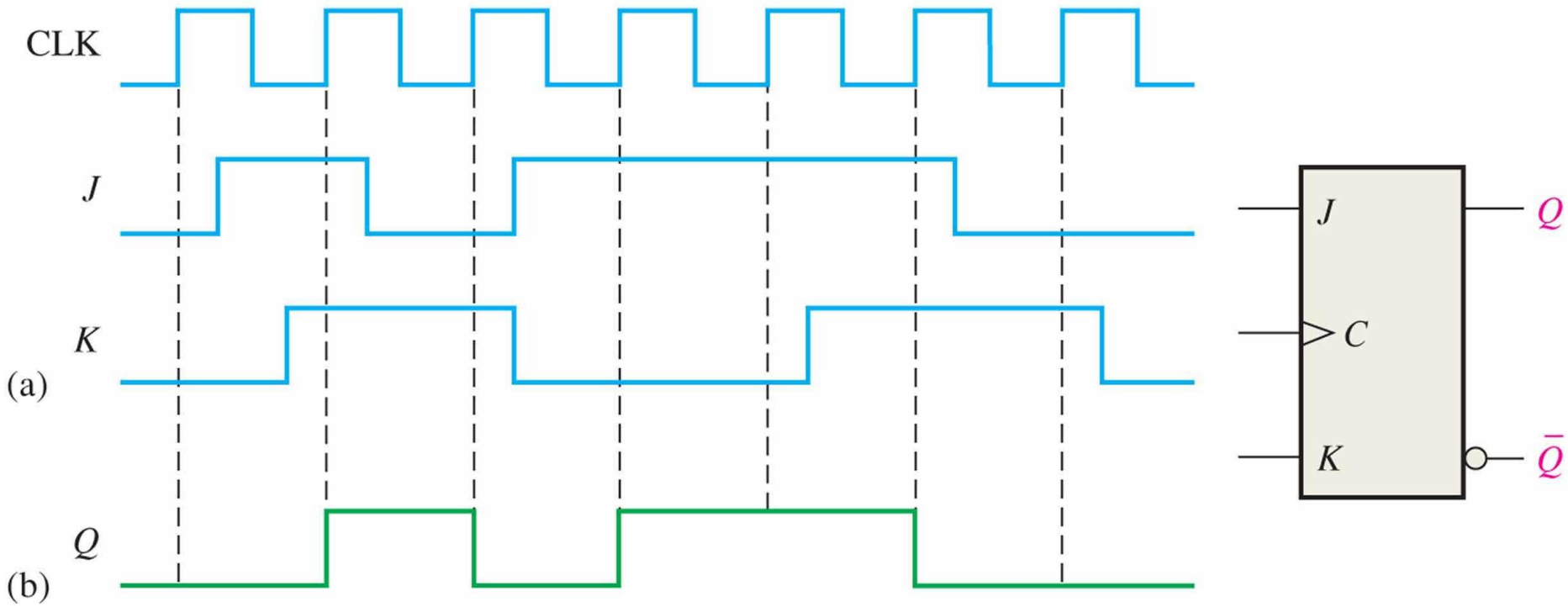

101
J
HIGH
CLK
1 2 3
Pulse transition detector
1 3
1 2 3
G_1
G_3
Q
1 2 3
G_2
G_4
$\bar{Q}$
011
K
HIGH
2

J-K flip-flop example





Note: this is a –ve ET J-K flip-flop and thus will trigger on falling edge


CLK
J
K
(a)
Q
(b)
J
C
K
Q
$\bar{Q}$

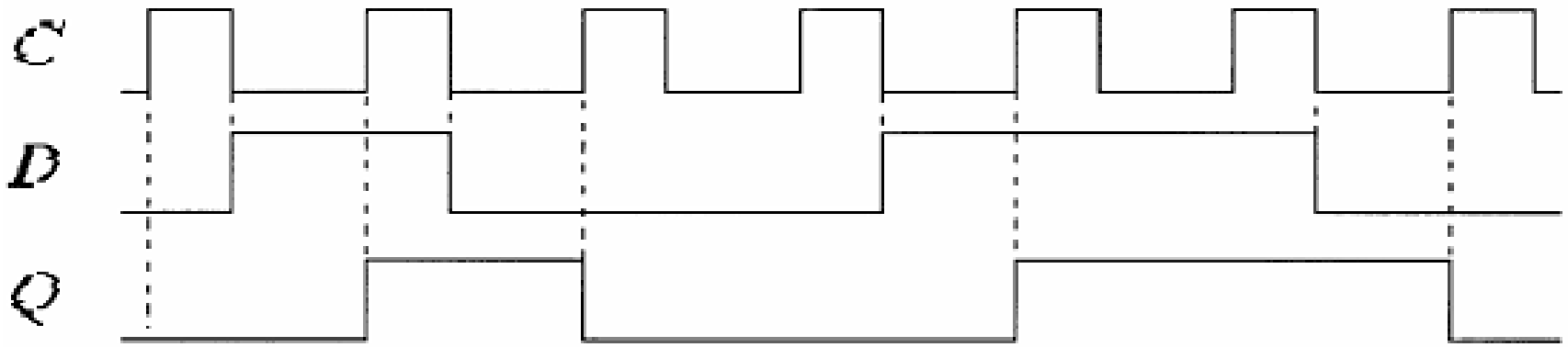
Application of flip-flops

- Edge-triggered (clocked) flip-flops can be used in a wide variety of applications, such as data storage, transferring data from one location to another, counting, etc.
- The most common use of flip-flops is for the storage of data or information by using groups of flip-flops called registers.
- To transfer data from one location to another, we need groups of flip-flops called shift register arranged in such a way so that the data in binary numbers form can be stored and shifted from one flip-flop to the next for every clock pulse.
- The application of flip-flops in counting is referred to as frequency division.
  - By using appropriate number of flip-flops, the circuit could divide a frequency by any power of 2.

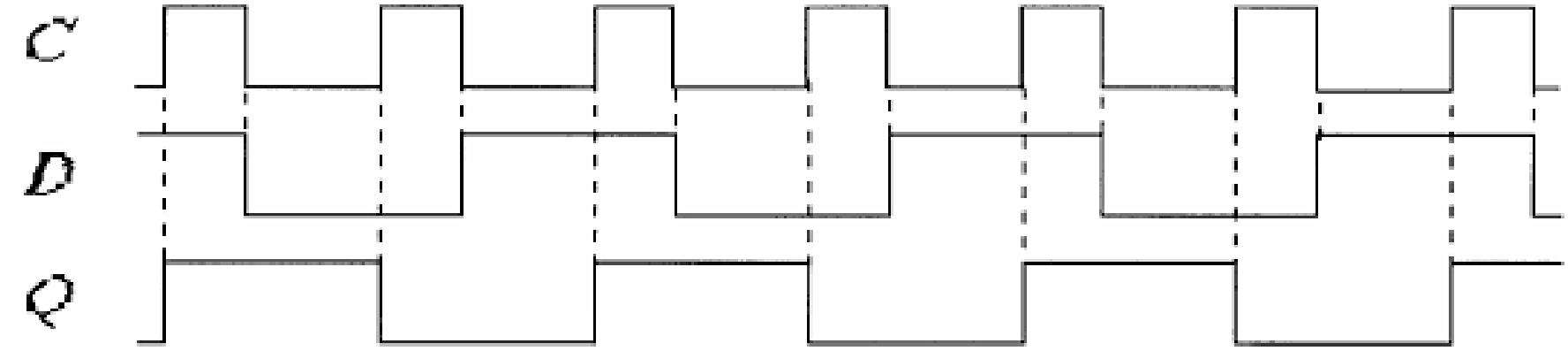
Exercise

- Draw the Q output relative to the CLK for a D flip-flop with the inputs as shown below (assume positive ET and Q is initially LOW)

(a)



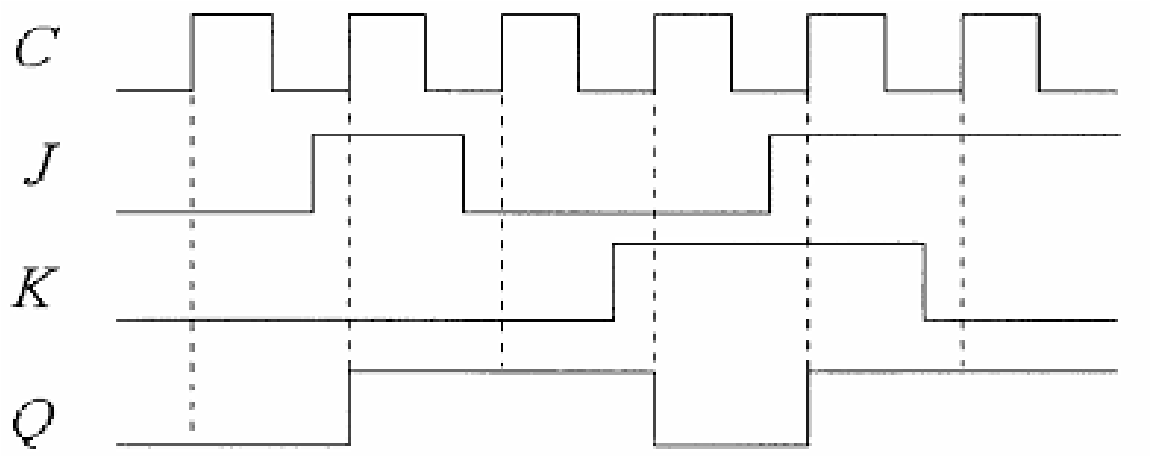
(b)



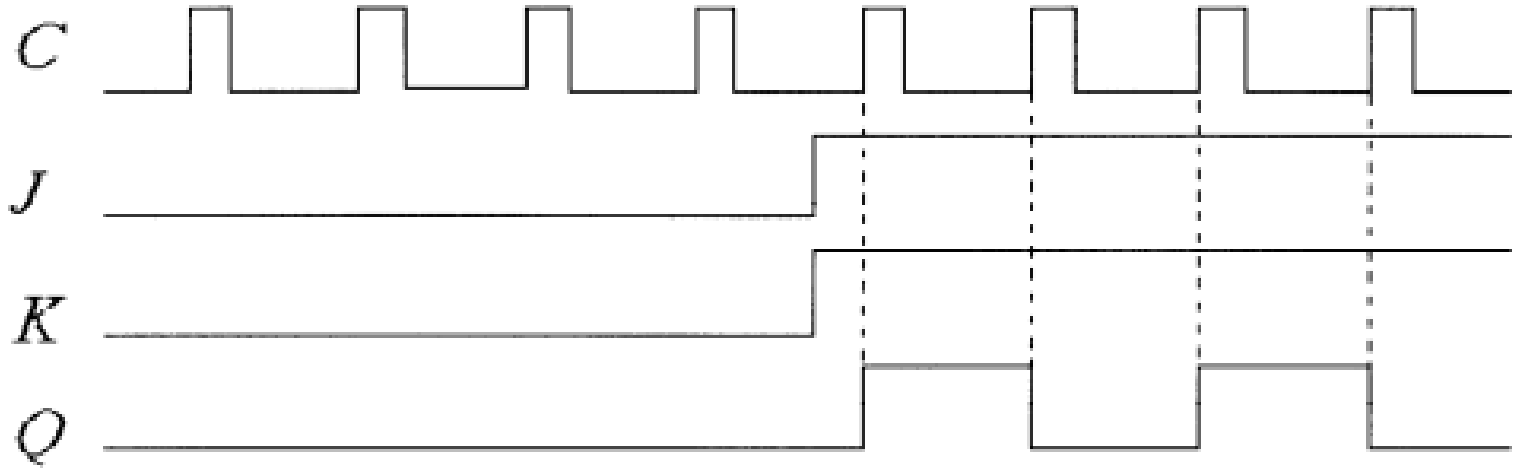
Exercise

- For a positve ET J-K flip-flop with inputs as shown, determine output Q in relation to CLK assuming at the flip-flop is initially RESET

(a)

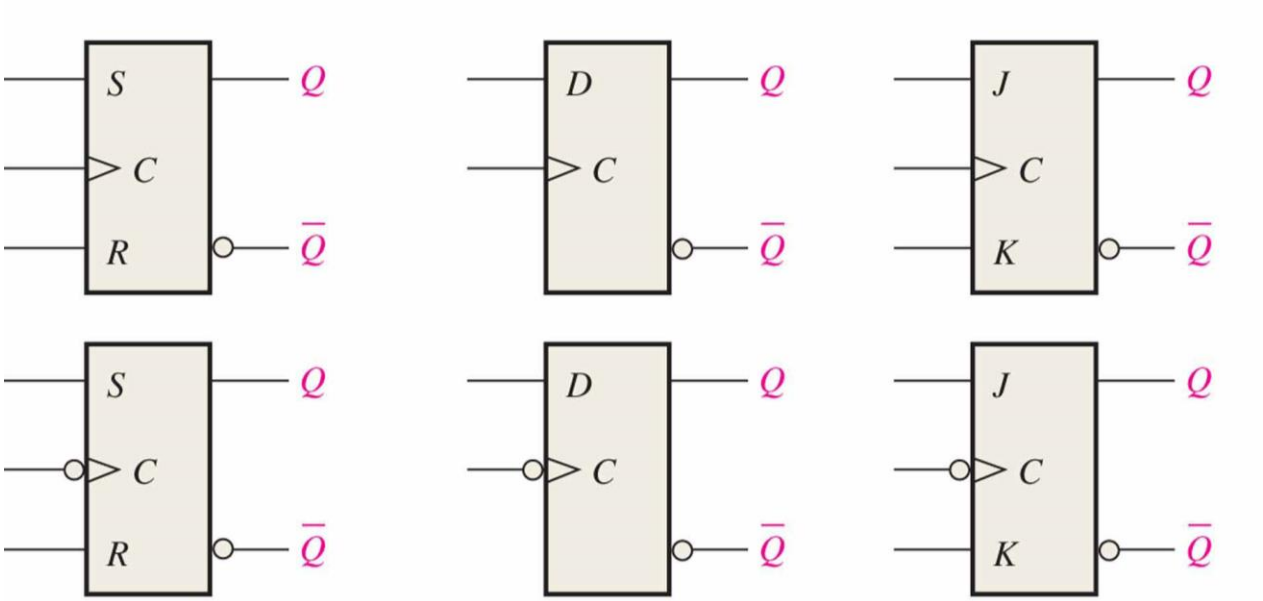


(b)



Summary

- Edge triggered flip-flops are bistable devices with synchronous inputs whose state depends on the inputs ONLY at the transition of a clock pulse
- J-K flip-flops avoid invalid states by checking the outputs at the steering section and switching to toggle mode if it occurs
- Logic symbols for all the flip-flops covered



(e) S-R edge-triggered flip-flops

(f) D edge-triggered flip-flops

(g) J-K edge-triggered flip-flops