PDS0101

Introduction to Digital Systems

Counters II

MMU
MULTIMEDIA UNIVERSITY

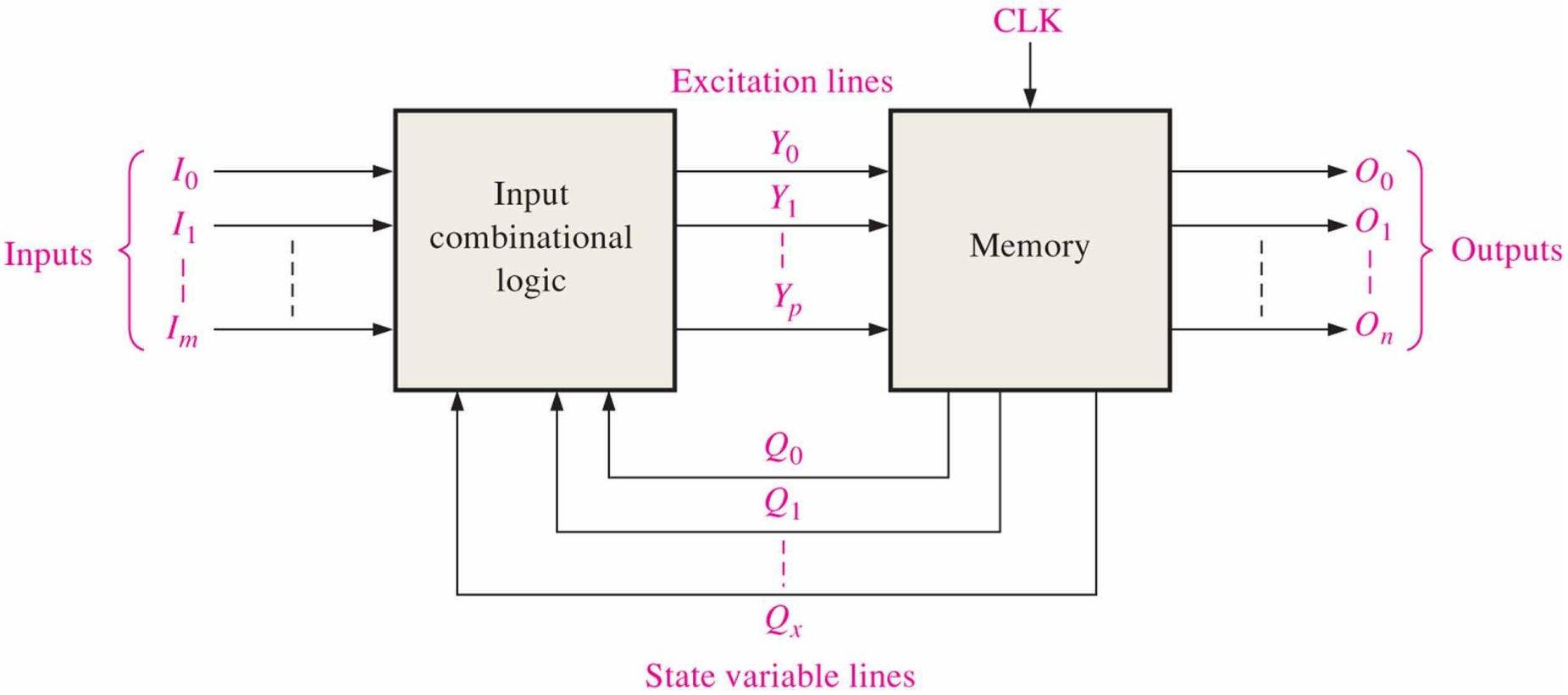
Lecture outcome

- By the end of today's lecture you should be able to
  - design your own synchronous counter that follows a specific pattern
  - implement the design as a logic circuit

- **NOTE**: contents in this set of slides are intentionally incomplete and content will be shown in class as examples of how they are derived

Synchronous Counter Design

- Most requirements for synchronous counters can be met with available ICs.
- In cases where a special sequence is needed, you can apply a step-by-step design process
- Basically, you start with the desired sequence and draw a state diagram and next-state table, simplify the states using algebra rules and/or k-map and complete the logic circuit
  - The resulting circuit will be a sequential circuit or state machine
- In general, a sequential circuit consists of a combinational logic section and a memory section (flip-flop)
- In the case of a clocked sequential circuit, a CLK input to the memory is added


CLK
Excitation lines
Inputs
I_0
I_1
I_m
Input combinational logic
Y_0
Y_1
Y_p
Memory
O_0
O_1
O_n
Outputs
Q_0
Q_1
Q_x
State variable lines

Synchronous Counter Design

Several methods are available that follow arbitrary sequence.

Here we will learn one common method using JK flip-Flops.

In synchronous counters all the FF's are clocked at the same time.

J-K Excitation Table

Before begin the designing we must know the operation of the J-K FF, let us analysis **Truth table for 74LS76 IC (JK flip-flop) and its** excitation table.

Truth table for 74LS76 IC (JK flip-flop)

$\overline{CLEAR}$	$\overline{PRESET}$	J	K	CLK	Qt	Qt’
0	0	0	0	x	1	1
		0	1	x	1	1
		1	0	x	1	1
		1	1	x	1	1
0	1	0	0	x	1	0
		0	1	x	1	0
		1	0	x	1	0
		1	1	x	1	0
1	0	0	0	x	0	1
		0	1	x	0	1
		1	0	x	0	1
		1	1	x	0	1
1	1	0	0	↓	Q_0	Q_0’
		0	1	↓	0	1
		1	0	↓	1	0
		1	1	↓	TOGGLE	TOGGLE

JK FF Excitation Table where $\overline{CLEAR}$ and $\overline{PRESET}$ are High (1)

PRESENT	**NEXT**	**J**	**K**
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

OUTPUT TRANSITIONS		FLIP-FLOP INPUTS	
Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J-K Excitation Table

TRANSITION AT OUTPUT		PRESENT STATE Q(N)	NEXT STATE Q(N+1)	J	K
0	0	0	0	0	X
0	1	0	1	1	X
1	0	1	0	X	1
1	1	1	1	X	0

0 → 0 TRANSITION; FF's Present status is 0 and it should remain in 0 when a clock pulse is applied. That can be either J=K=0 status or J=0,K=1.

That means J=0 and K=0 or 1

Resulted , J=0 and K=X(don't care)

Synchronous Counter Design

0 → 1 TRANSITION: The present state is 0 and it has to change to 1. This can happen either J=1 and K=0 or J=K=1.

That means J=1 and K=0 or1

Resulted , J=1 and K=X (don't care)

1 → 0 TRANSITION; The present state is 1 and it has to change to 0. This can happen either J=0 and K=1 or J=K=1.

That means K=1 and J=0 or1

Resulted , K=1 and J=X (don't care)

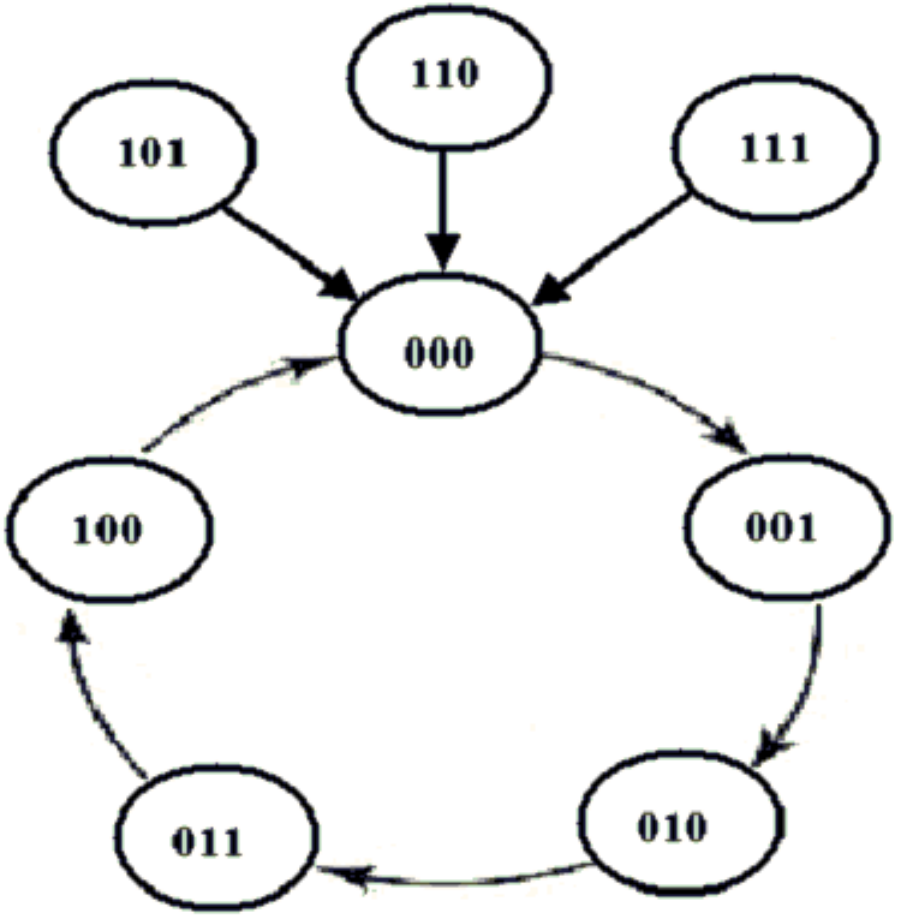
1 → 1 TRANSITION; The present state is 1 and it has to change to 1. This can happen either J=K=0 or J=1 and K=0.

That means K=0 and J can be 0 or 1

Resulted , K=0 and J=X (don't care)

STEP -1

Draw the state transition diagram showing all the possible states, including those that are not part of the desired counting sequence



Synchronous Counter Design / Example (1) ….cont.

STEP -2

Use the state transition diagram to set up a table that lists all **PRESENT** states and their **NEXT** states

	Present state			Next state		
	C	*B*	*A*	*C*	*B*	*A*
1	0	0	0	0	0	1
2	0	0	1	0	1	0
3	0	1	0	0	1	1
4	0	1	1	1	0	0
5	1	0	0	0	0	0
6	1	0	1	0	0	0
7	1	1	0	0	0	0
8	1	1	1	0	0	0

Undesired states transition to 000 here

STEP -3

Add a column to this table for each J and K input. For each **PRESENT** state, indicate the level required at each J and K input in order to produce the transition to the **NEXT** state.

OUTPUT TRANSITIONS		FLIP-FLOP INPUTS	
Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

	Present state			Next state								
	C	***B***	***A***	***C***	***B***	***A***	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	X	0	X	1	X
2	0	0	1	0	1	0	0	X	1	X	X	1
3	0	1	0	0	1	1	0	X	X	0	1	X
4	0	1	1	1	0	0	1	X	X	1	X	1
5	1	0	0	0	0	0	X	1	0	X	0	X
6	1	0	1	0	0	0	X	1	0	X	X	1
7	1	1	0	0	0	0	X	1	X	1	0	X
8	1	1	1	0	0	0	X	1	X	1	X	1

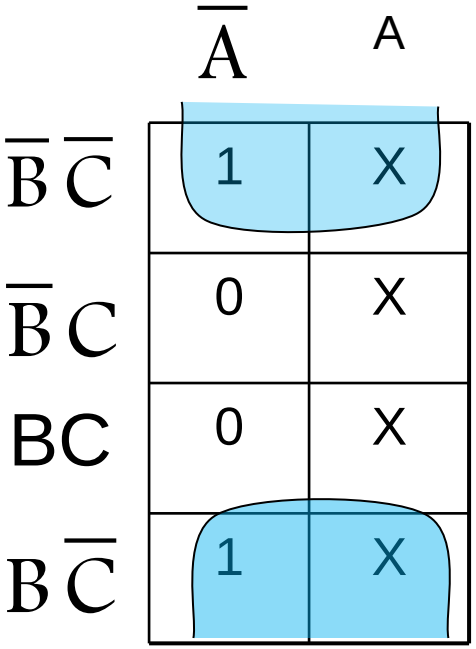
STEP 4 : K-MAP SIMPLIFICATIONS

- Determine the logic required for the J and K inputs of each FF in the counter using K-maps
  - There will be one K-map for the J input and another K-map for the K input of each FF
- From the J and K states in the transition table a 1, 0 or X is mapped onto each present-state cell on the K-maps depending on the transition of the Q output for a particular FF
- An example of this operation is shown on the following slide

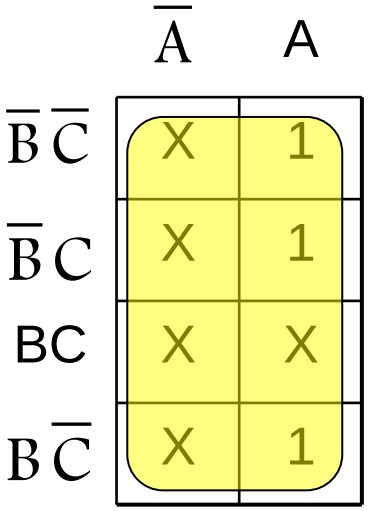
STEP- 4

Design the logic expression to generate the level required at each J and K, using K-maps.

Present state				
C	***B***	***A***	J_A	K_A
0	0	0	1	X
0	0	1	X	1
0	1	0	1	X
0	1	1	X	1
1	0	0	0	X
1	0	1	X	1
1	1	0	0	X
1	1	1	X	1



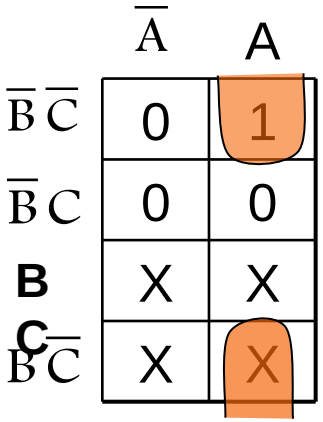
$J_A = \overline{C}$



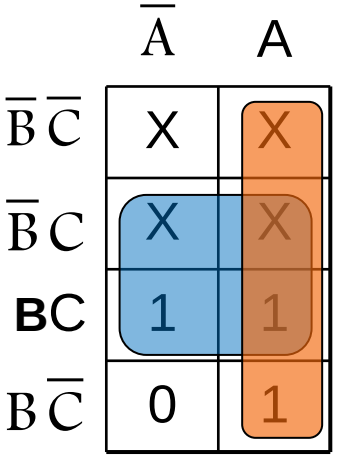
$K_A = 1$

STEP- 4 …..cont.

Present state				
C	***B***	***A***	J_B	K_B
0	0	0	0	X
0	0	1	1	X
0	1	0	X	0
0	1	1	X	1
1	0	0	X	X
1	0	1	X	X
1	1	0	X	1
1	1	1	X	1



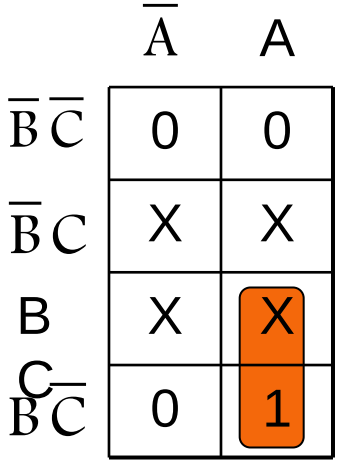
$J_B = A\,\overline{C}$



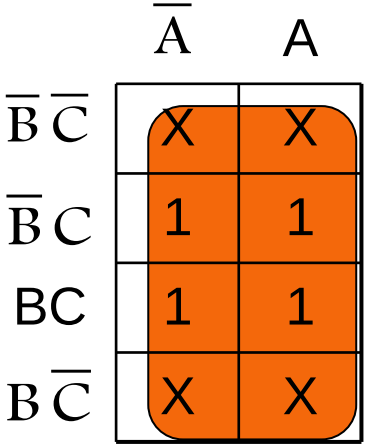
$K_B = A+C$

STEP- 4 …..cont

Present state				
C	***B***	***A***	***Jc***	***Kc***
0	0	0	0	X
0	0	1	0	X
0	1	0	0	X
0	1	1	1	X
1	0	0	0	1
1	0	1	X	1
1	1	0	0	1
1	1	1	X	1



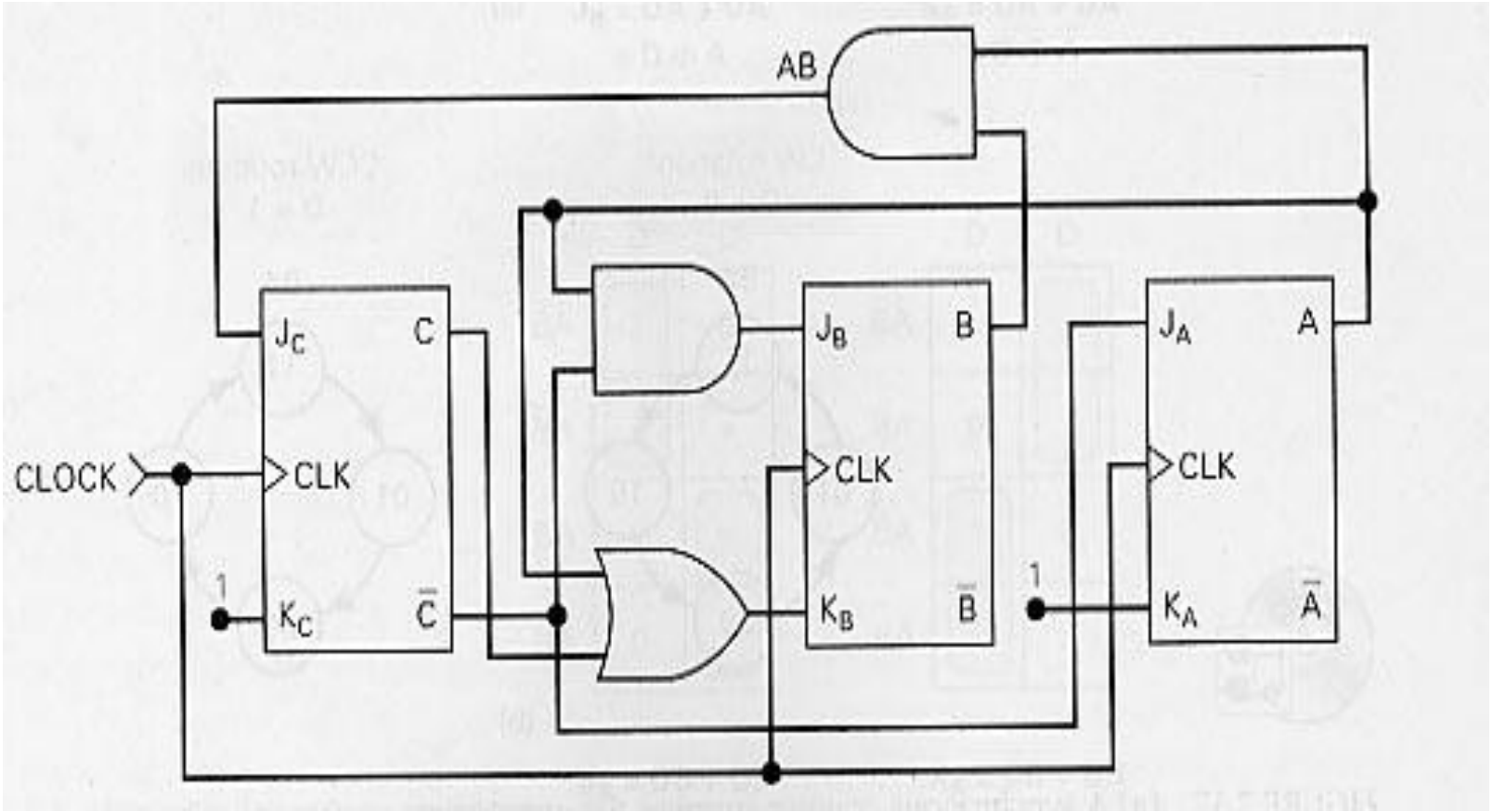
$J_C = AB$



$K_C = 1$

SETP -5

Finally to implement the final expressions.



$$J_c = AB \qquad J_B = A\bar{C} \qquad J_A = \bar{C}$$

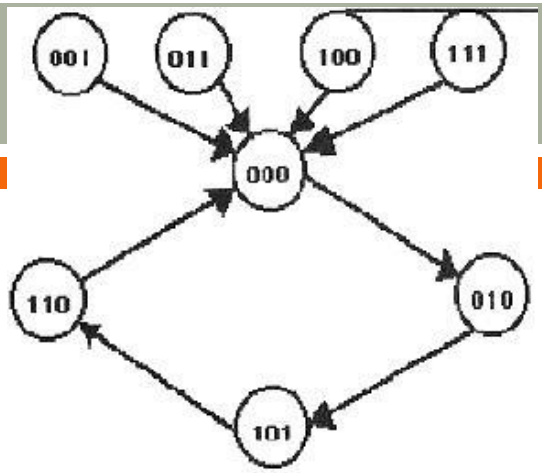
$$K_C = 1 \qquad K_B = A + C \qquad K_A = 1$$

Exercises

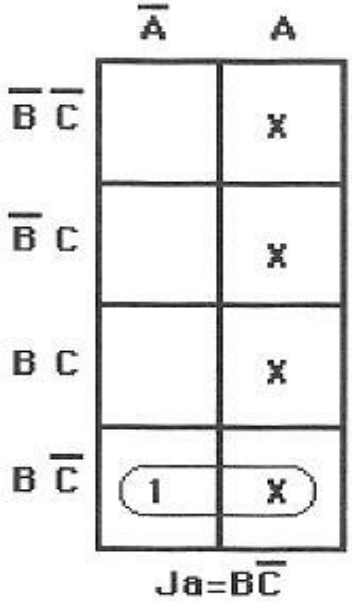
1. Design a JK synchronous counter that has follows the sequence 000,010,101,110 and repeats. The undesired states go to 000 on the next clock pulse

2. Design a JK synchronous counter that follows the sequence 000,010,101,110 and repeats. For undesired states their NEXT states can be DON'T CARES

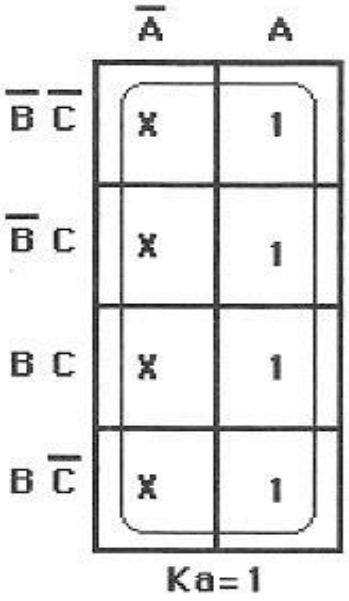
Answer 1



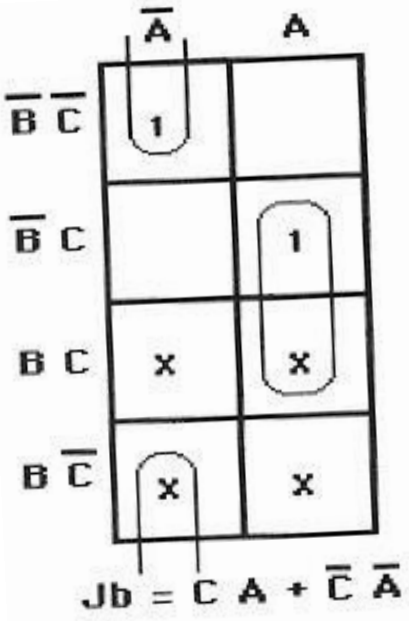
PRESENT STATE			NEXT STATE			FF2		FF1		FF0	
C	B	A	C	B	A	Jc	Kc	Jb	Kb	Ja	Ka
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	0	0	0	0	X	0	X	X	1
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1



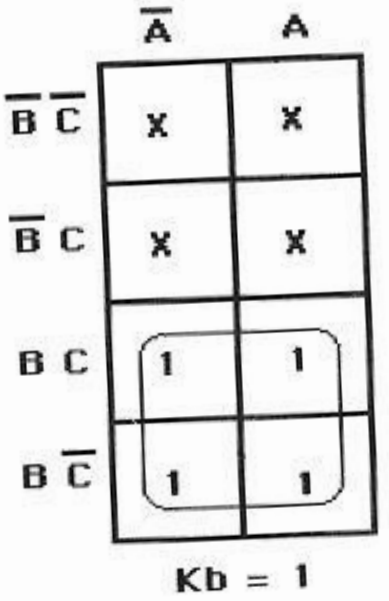
Ja=B$\overline{C}$



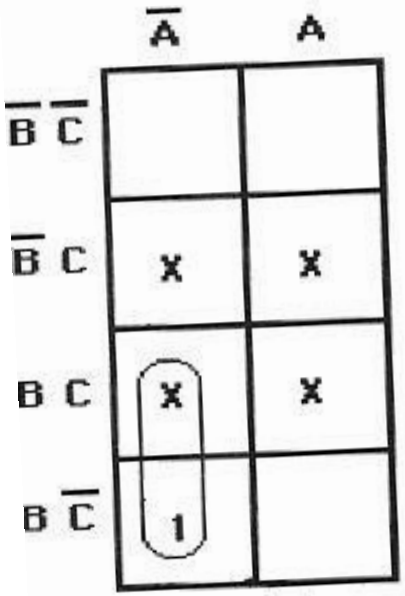
Ka=1



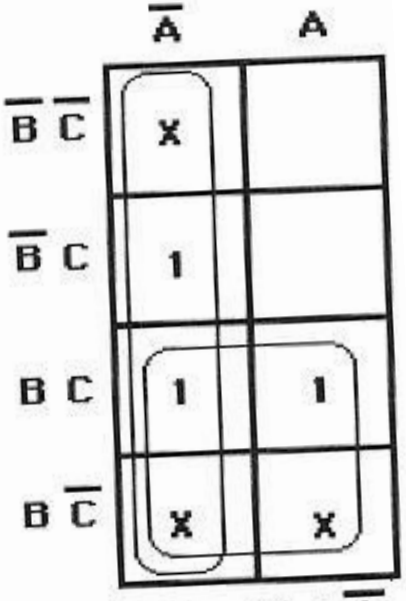
Jb = C A + $\overline{C}$ $\overline{A}$



Kb = 1

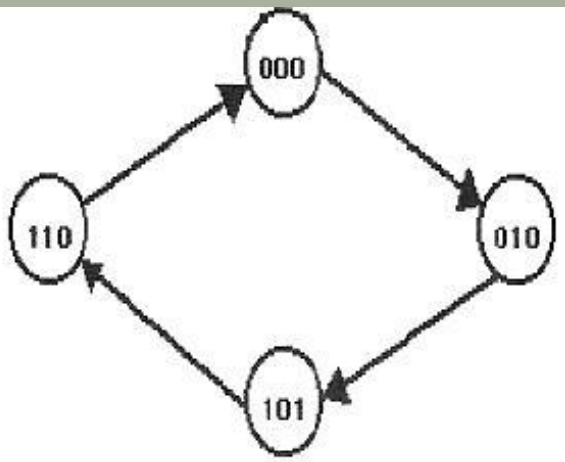


Jc = $\overline{A}$ B

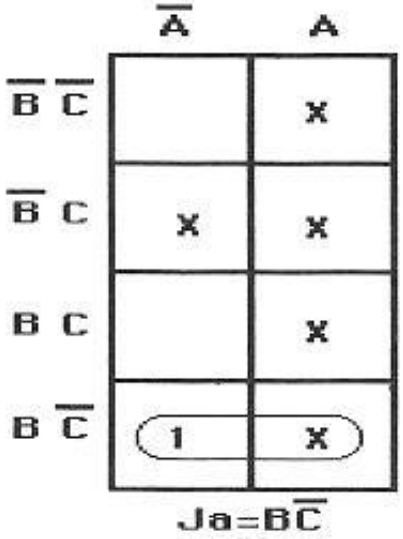


Kc = B + $\overline{A}$

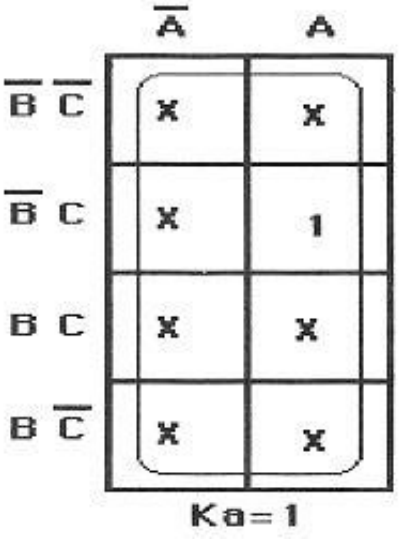
Answer 2



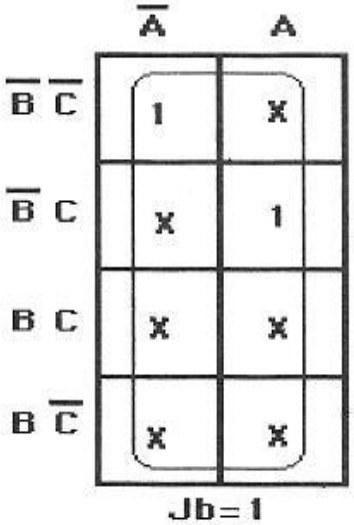
PRESENT STATE			NEXT STATE			FF2		FF1		FF0	
C	B	A	C	B	A	Jc	Kc	Jb	Kb	Ja	Ka
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X	X	X	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X



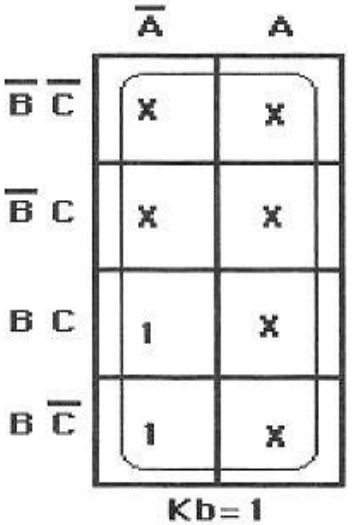
Ja=B$\overline{C}$



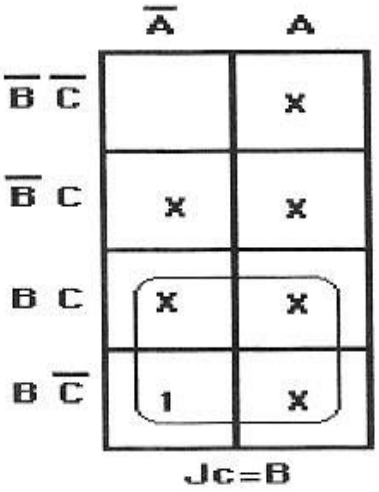
Ka=1



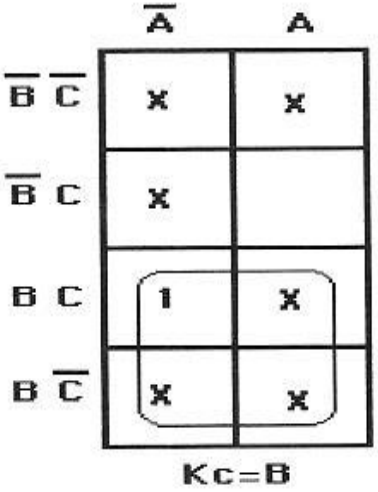
Jb=1



Kb=1



Jc=B



Kc=B

Summary

- These steps can be applied to any sequential circuit to create a counter
  - Specify the counter sequence and draw the state diagram
  - Derive the next-state table from the state diagram
  - Using the J-K FF transition/excitation table, develop the transition table showing the FF inputs required for each transition
  - Transfer J and K states to individual K-maps – there is a K-map for each input of each FF
  - Group K-map cells to simplifyand derive the logic expression for each FF input
  - Implement the expressions with combinational logic and combine with FF to create the counter