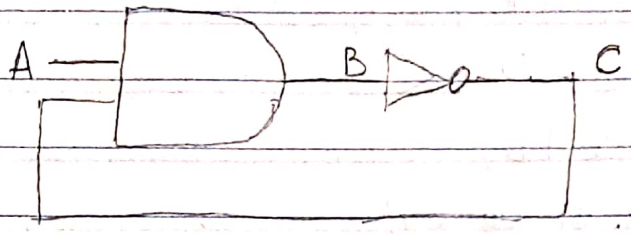
09/11/21

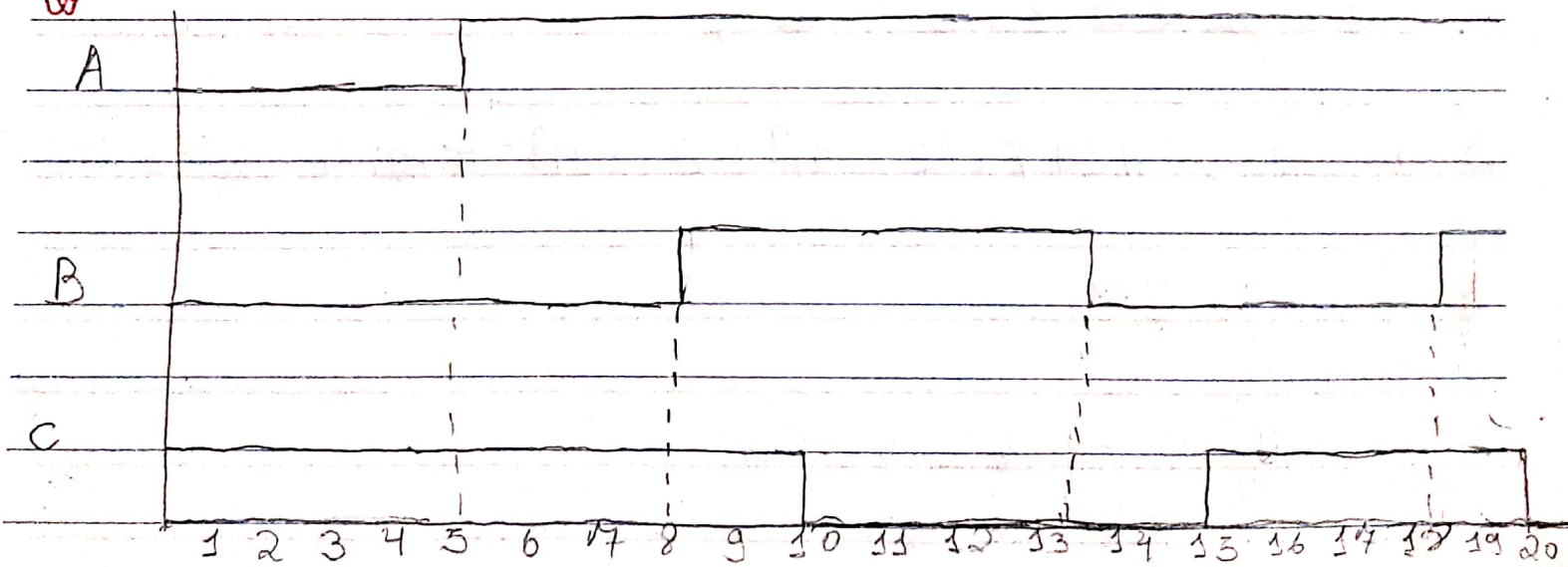
Aluno: Victor Luiz
Aluno: Fernanda Pascoal

Projeto 1 - SD
Respostas

1-a-



b-



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2- module Test(output wire Z, input wire A, B, C, D);

Wire var1, var2, var3;
Wire E, F;

assign #3 var1 = A & B & C;
assign #3 var2 = ~(B | C);

assign #3 E = var1 | D;
assign #3 F = ~(A & var2);
assign #2 var3 = ~F;

assign #3 Z = E ^ var3;

3-a- assign #10 F = (C == 0) ? ((D == 0) ? ~A : B) : ((D == 0) ? ~B : 0);

b- always @(*)
begin
if (C == 0 && D == 0)
#10 F = ~A;
else if (C == 0 && D == 1)
#10 F = B;
else if (C == 1 && D == 0)
#10 F = ~B;
else
#10 F = 0;
end

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c- always @(*)
begin case(
sel)
0: #10 F = ~A;
1: #10 F = B;
2: #10 F = ~B;
3: #10 F = 0;
endcase
end

4- a- module questao4(output reg A, input C, B1, B2, B3);

always @(C or B1 or B2 or B3)
begin
if(C == 1)
A <= B1;
else if(C == 2)
A <= B2;
else if(C == 3)
A <= B3;
else
A <= 0;
end
endmodule

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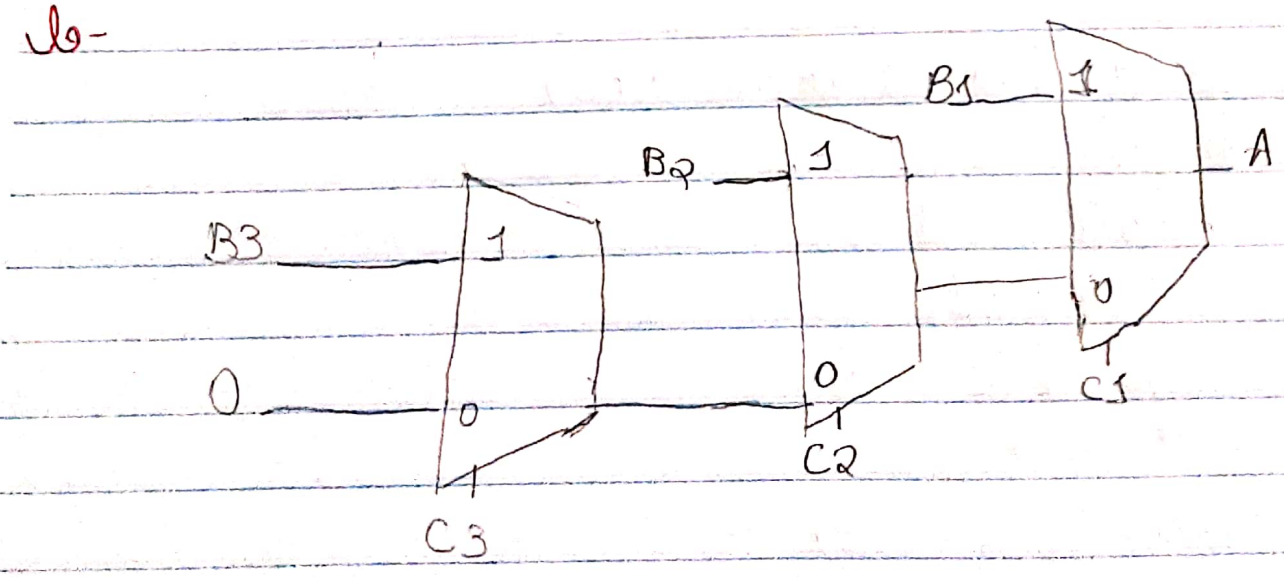
4a - Continuação

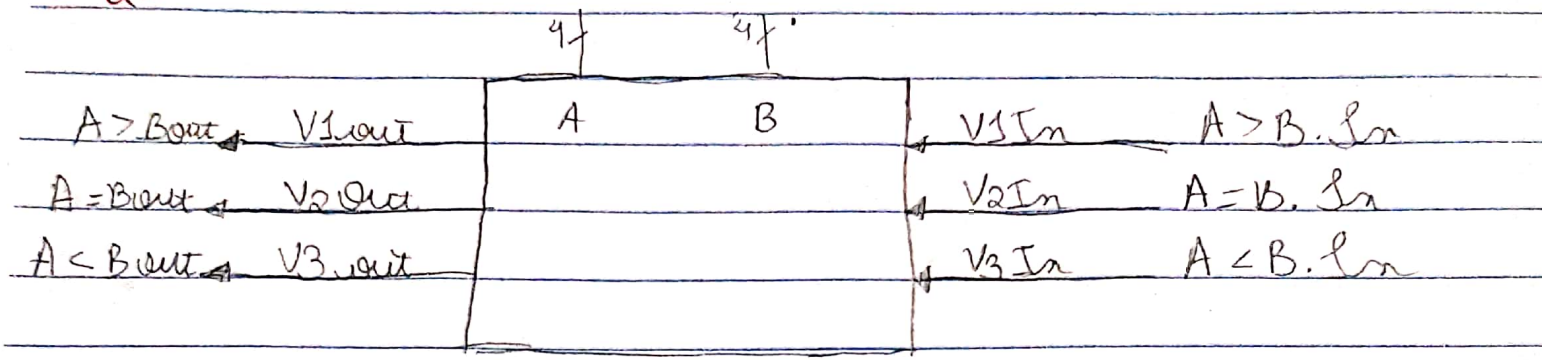
- module questao4_2(output reg A, input wire C, B1, B2, B3);

always @(C or B1 or B2 or B3)
case (C)
1: A = B1;
2: A = B2;
3: A = B3;
default: A = 0;
endcase
endmodule

4b -



5-a-



b-