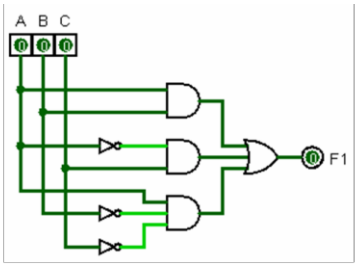
Designing a 4-bit binary Adder-Subtractor using Xilinx Vivado

Part I.

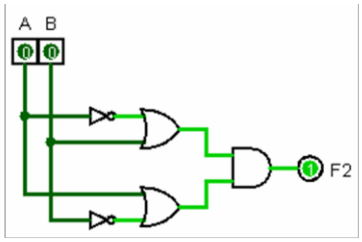
Part I requires students to work on developing two different digital circuits (Circuit 1 and Circuit 2) shown below using behavioral Verilog. For each design, students should develop separate behavioral Verilog modules and develop a simple testbench to verify each design.



$F_1(A,B,C) = A.B + A'.C + A.B'.C'$

row	A	B	C	F(A,B,C)
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

Figure 1. Circuit 1 and its corresponding truth table



$F_2(A,B,C) = (A'+B).(A+B')$

row	A	B	F(A,B,C)
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	1

Figure 2. Circuit 2 and its corresponding truth table

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Part II.

Using the knowledge learned from lab 1, you will be using Verilog programming to design a simple 4-bit adder/subtractor. As discussed in the previous lab, you must first develop the required 1-bit logical components using Verilog, and then construct the larger design by making the necessary instantiations. Lastly, you need to develop a testbench to verify your design using the simulation results and generated waveforms.

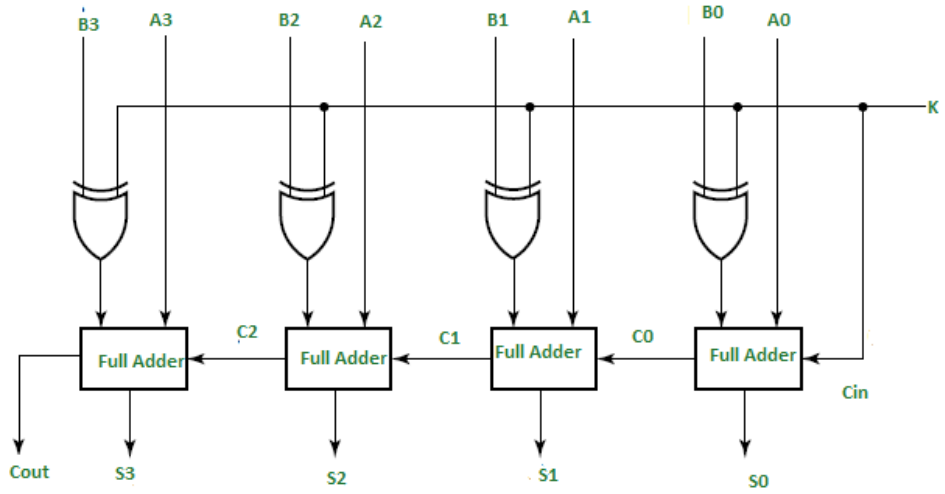

Figure 3. Schematic of an implementation of a 4-bit adder/subtractor.
Image taken from: https://www.geeksforgeeks.org/4-bit-binary-adder-subtractor/

Lab Deliverables

Submit a zipped file with the following syntax: Lab2_LastName1_LastName2.zip. The zipped file should include the following files:

- The **Part I** folder consisting of the project folder and files for Circuit 1 and Circuit 2 (folder containing all the files of your design including Xilinx generated files).
- The full **Lab 2-part II** project folder for the 4-bit adder-subtractor (folder containing all the files of your design including Xilinx generated files).
- A brief report describing your steps in developing your design. Also, include the snapshot of your top level RTL schematic for **Part II** and captured waveforms for **Parts I and II**.

In addition, you need to demonstrate your work and the completed steps in the class. Both group members should be present during the demo sessions. **The due date for in-class demonstration is Sep. 15th (9/15/2020).**

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