

# LABORATORY 5

Please print this sheet prior to coming to laboratory. Complete the pre-laboratory tasks in your lab notebook. Complete the lab tasks in **both** your lab notebook and this submission sheet.

## 1 Pre-laboratory Verification

3E -- 26	3E -- 27	3E -- 28
3E -- 29	3E -- 30	3E -- 31
3E -- 32	3E -- 33	

## 2 Laboratory Verification

3E -- 34	3E -- 35
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### 3 Deliverables

1. Copy the results table below (you may omit **0** values):

Inputs				Simulated Outputs							FPGA Dev. Board Outputs							Wired
A	B	C	D	F <sub>Kmap</sub>	F <sub>min</sub>	$\overline{ABCD}$	$\overline{ABCD}$	$\overline{ABCD}$	$\overline{ABCD}$	ABCD	F <sub>Kmap</sub>	F <sub>min</sub>	$\overline{ABCD}$	$\overline{ABCD}$	$\overline{ABCD}$	$\overline{ABCD}$	ABCD	Output
SW3	SW2	SW1	SW0	LD6	LD5	LD4	LD3	LD2	LD1	LD0	LD6	LD5	LD4	LD3	LD2	LD1	LD0	F <sub>Kmap</sub>
0	0	0	0															
0	0	0	1															
0	0	1	0															
0	0	1	1															
0	1	0	0															
0	1	0	1															
0	1	1	0															
0	1	1	1															
1	0	0	0															
1	0	0	1															
1	0	1	0															
1	0	1	1															
1	1	0	0															
1	1	0	1															
1	1	1	0															
1	1	1	1															

2. What do the **LEDR4..0** represent in the FPGA development board implementation?

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3. Why is row/column ordering in a Karnaugh map not in ascending binary order?

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