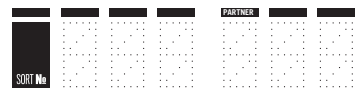


Kit No.   Date:   /   /

USE TEMPLATE  
01234  
56789  
MISFILL -1 PT



# LABORATORY 5

Please print this sheet prior to coming to laboratory. Complete the pre-laboratory tasks in your lab notebook. Complete the lab tasks in **both** your lab notebook and this submission sheet.

## 1 Pre-laboratory Verification

|                               |                               |                               |
|-------------------------------|-------------------------------|-------------------------------|
| <input type="text"/> 4E .. 26 | <input type="text"/> 4E .. 27 | <input type="text"/> 4E .. 28 |
| <input type="text"/> 4E .. 29 | <input type="text"/> 4E .. 30 | <input type="text"/> 4E .. 31 |
| <input type="text"/> 4E .. 32 | <input type="text"/> 4E .. 33 |                               |

## 2 Laboratory Verification

|                               |                               |
|-------------------------------|-------------------------------|
| <input type="text"/> 4E .. 34 | <input type="text"/> 4E .. 35 |
|-------------------------------|-------------------------------|

### 3 Deliverables

1. Copy the results table below (you may omit **0** values):

| Inputs |     |     |     | Simulated Outputs |                  |                   |                   |                   |                   |      | FPGA Dev. Board Outputs |                  |                   |                   |                   |                   |      | Wired             |
|--------|-----|-----|-----|-------------------|------------------|-------------------|-------------------|-------------------|-------------------|------|-------------------------|------------------|-------------------|-------------------|-------------------|-------------------|------|-------------------|
| A      | B   | C   | D   | F <sub>Kmap</sub> | F <sub>min</sub> | $\overline{ABCD}$ | $\overline{ABCD}$ | $\overline{ABCD}$ | $\overline{ABCD}$ | ABCD | F <sub>Kmap</sub>       | F <sub>min</sub> | $\overline{ABCD}$ | $\overline{ABCD}$ | $\overline{ABCD}$ | $\overline{ABCD}$ | ABCD | Output            |
| SW3    | SW2 | SW1 | SW0 | LD6               | LD5              | LD4               | LD3               | LD2               | LD1               | LD0  | LD6                     | LD5              | LD4               | LD3               | LD2               | LD1               | LD0  | F <sub>Kmap</sub> |
| 0      | 0   | 0   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 0   | 0   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 0   | 1   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 0   | 1   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 1   | 0   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 1   | 0   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 1   | 1   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 0      | 1   | 1   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 0   | 0   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 0   | 0   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 0   | 1   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 0   | 1   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 1   | 0   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 1   | 0   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 1   | 1   | 0   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |
| 1      | 1   | 1   | 1   |                   |                  |                   |                   |                   |                   |      |                         |                  |                   |                   |                   |                   |      |                   |

2. What do the **LEDR4..0** represent in the FPGA development board implementation?

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3. Why is row/column ordering in a Karnaugh map not in ascending binary order?

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