LABORATORY 3

Please print this sheet prior to coming to laboratory. Complete the pre-laboratory tasks in your lab notebook. Complete the lab tasks in **both** your lab notebook and this submission sheet.

1 Pre-laboratory Verification

3E .. 14	3E .. 15	3E .. 16
3E .. 17	3E .. 18	

2 Laboratory Verification

3E .. 19	3E .. 20

3 Deliverables

1. Copy the results table below (you may omit **0** values):

Inputs			Predicted					74XX					Simulated					FPGA				
			Intermediate					Intermediate					Intermediate					Intermediate				
A	B	C	net3	net2	net1	net0	F	net3	net2	net1	net0	F	net3	net2	net1	net0	F	net3	net2	net1	net0	F
0	0	0																				
0	0	1																				
0	1	0																				
0	1	1																				
1	0	0																				
1	0	1																				
1	1	0																				
1	1	1																				

2. Compare circuit output results between predictions, 74XX (IC) implementation, Quartus simulation, and FPGA hardware. Are the results identical? **Explain why or why not.**

3. Interpret the laboratory data in the context of the circuit. Does the behavior of the output make sense, given the components used? **Explain.**