Kit No. Date: / /

USE TEMPLATE
MISFILL –1 PT
SORT No
PARTNER

LABORATORY 5

Please print this sheet prior to coming to laboratory. Complete the pre-laboratory tasks in your lab notebook. Complete the lab tasks in **both** your lab notebook and this submission sheet.

1 Pre-laboratory Verification

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2 Laboratory Verification

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3 Deliverables

1. Copy the results table below (you may omit **0** values):

Inputs				**Simulated Outputs**							**FPGA Dev. Board Outputs**							**Wired**
A	B	C	D	F_{Kmap}	F_{min}	$\bar{A}BCD$	$A\bar{B}CD$	$AB\bar{C}D$	$ABC\bar{D}$	ABCD	F_{Kmap}	F_{min}	$\bar{A}BCD$	$A\bar{B}CD$	$AB\bar{C}D$	$ABC\bar{D}$	ABCD	**Output**
SW3	**SW2**	**SW1**	**SW0**	**LD6**	**LD5**	**LD4**	**LD3**	**LD2**	**LD1**	**LD0**	**LD6**	**LD5**	**LD4**	**LD3**	**LD2**	**LD1**	**LD0**	F_{Kmap}
0	**0**	**0**	**0**															
0	**0**	**0**	**1**															
0	**0**	**1**	**0**															
0	**0**	**1**	**1**															
0	**1**	**0**	**0**															
0	**1**	**0**	**1**															
0	**1**	**1**	**0**															
0	**1**	**1**	**1**															
1	**0**	**0**	**0**															
1	**0**	**0**	**1**															
1	**0**	**1**	**0**															
1	**0**	**1**	**1**															
1	**1**	**0**	**0**															
1	**1**	**0**	**1**															
1	**1**	**1**	**0**															
1	**1**	**1**	**1**															

2. What do the **LEDR4..0** represent in the FPGA development board implementation?

3. Why is row/column ordering in a Karnaugh map not in ascending binary order?