

Kit No.   Date:   /   /

USE TEMPLATE  
01234  
56789  
MISFILL -1 PT



# LABORATORY 3

Please print this sheet prior to coming to laboratory. Complete the pre-laboratory tasks in your lab notebook. Complete the lab tasks in **both** your lab notebook and this submission sheet.

## 1 Pre-laboratory Verification

4E -- 14	4E -- 15	4E -- 16	4E -- 17	4E -- 18
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## 2 Laboratory Verification

4E -- 19	4E -- 20
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### 3 Deliverables

1. Copy the results table below (you may omit **0** values):

Inputs			Predicted					74XX					Simulated					FPGA				
			Intermediate				F	Intermediate				F	Intermediate				F	Intermediate				F
A	B	C	net3	net2	net1	net0		net3	net2	net1	net0		net3	net2	net1	net0		net3	net2	net1	net0	
0	0	0																				
0	0	1																				
0	1	0																				
0	1	1																				
1	0	0																				
1	0	1																				
1	1	0																				
1	1	1																				

2. Compare circuit output results between predictions, 74XX (IC) implementation, Quartus simulation, and FPGA hardware. Are the results identical? **Explain why or why not.**

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3. Interpret the laboratory data in the context of the circuit. Does the behavior of the output make sense, given the components used? **Explain.**

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