

Kit No. Date: / /

USE TEMPLATE
01234
56789
MISFILL -1 PT



LABORATORY 5

Please print this sheet prior to coming to laboratory. Complete the pre-laboratory tasks in your lab notebook. Complete the lab tasks in **both** your lab notebook and this submission sheet.

1 Pre-laboratory Verification

4E -- 26	4E -- 27	4E -- 28	4E -- 29

4E -- 30	4E -- 31	4E -- 32	4E -- 33

2 Laboratory Verification

4E -- 34	4E -- 35

3 Deliverables

1. Copy the results table below (you may omit **0** values):

Inputs				Simulated Outputs							FPGA Dev. Board Outputs							Wired
A	B	C	D	F _{Kmap}	F _{min}	$\overline{A}BCD$	$A\overline{B}CD$	$AB\overline{C}D$	$ABCD$	$\overline{A}BCD$	F _{Kmap}	F _{min}	$\overline{A}BCD$	$A\overline{B}CD$	$AB\overline{C}D$	$ABCD$	Wired	
SW3	SW2	SW1	SW0	LD6	LD5	LD4	LD3	LD2	LD1	LD0	LD6	LD5	LD4	LD3	LD2	LD1	LD0	F _{Kmap}
0	0	0	0															
0	0	0	1															
0	0	1	0															
0	0	1	1															
0	1	0	0															
0	1	0	1															
0	1	1	0															
0	1	1	1															
1	0	0	0															
1	0	0	1															
1	0	1	0															
1	0	1	1															
1	1	0	0															
1	1	0	1															
1	1	1	0															
1	1	1	1															

2. What do the **LEDR4..0** represent in the FPGA development board implementation?

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3. Why is row/column ordering in a Karnaugh map not in ascending binary order?

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