Assignment 4 – Extra

Q1. Modify the testbenches for the **priority encoder** and the **ALU** in assignment 1 adding assertions making sure that all outputs are correct in all cases instead of using a task for checking the output (remove the task). Generate code coverage and make sure to get 100% code and assertion coverage.

Q2. Write SVA properties for an arbiter design for the following specs:

1- Upon rising of the signal “request” by a master, the arbiter should raise the “grant” within 2 to 5 clock cycles.
2- Once the “grant” is raised, the master should acknowledge acceptance in the same clock cycle by lowering the "frame" and "irdy" signals after they were high in the previous cycle.
3- Once the master completes the transaction it raises the "frame" and "irdy" signals, followed by that, the arbiter should lower the "grant" signal on the next clock cycle after it was high.

Q3. Suppose you are a design engineer and would like to write assertions to the internals of your design that has an FSM, write down the following SVA properties as per the following specs:

1- Current state internal signal “cs” will always stay one-hot irrespective of the input conditions.
2- If the current state “cs” is "IDLE" and if "get_data" input is raised, then the state is "GEN_BLK_ADDR" the following cycle and 64 cycles later the state should change to "WAITO."