Dalian Good Display Co.,Ltd.

GDE021A1

Dalian Good Display Co., Ltd.

Tel: +86-411-84619565
Fax: +86-411-84619585
WebSite: http://www.good-display.com

Rev.	Issued Date	Revised Contents
1.0	Jul. 1,2011	Preliminary
1.1	SEP.4.2011	1. Modify Mechanical Drawing of EPD module 2. Delete 7-3-1-2) MUC Parallel 6800-series Interface 3. Delete7-3-1-3) MUC Parallel 8080-series Interface 4. Delete7-3-2) Timing Characteristics of 6800-Series MCU Parallel Interface 5. Delete 7-3-3)Timing Characteristics of 8080-Series MCU Parallel Interface 6. Figure . 7-6 (1) Modify 41 pin conector to 24 pin connector

TECHNICAL SPECIFICATION

CONTENTS

1. Over View

The display is a TFT active matrix electrophoretic display , with interface and a reference system design.

The 2.04" active area contains 172×72 pixels, and has 1-bit and 2-bit full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM. LUT ,VCOM, and border are supplied with each panel.

2. Features

◆High contrast

◆High reflectance

◆Ultra wide viewing angle

◆Ultra low power consumption

◆Pure reflective mode

◆Bi-stable

◆Commercial temperature range

◆Landscape, portrait mode

◆Antiglare hard-coated front-surface

◆Low current deep sleep mode

◆On chip display RAM

◆Waveform stored in On-chip OTP

◆Serial peripheral interface available

◆On-chip oscillator

◆On-chip booster and regulator control for generating VCOM, Gate and source driving voltage .

◆I^{2}C Signal Master Interface to read external temperature sensor

◆Available in COG package IC thickness 250um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.04	Inch	
Display Resolution	172(H)×72(V)	Pixel	Dpi:95
Active Area	20.16(H)×48.16(V)	Mm	
Pixel Pitch	0.280×0.280	Mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.20(H×59.20(V) ×1.18(D)	Mm	
Weight	4±0.5	g	

4. Mechanical Drawing of EPD module

http://www.good-display.com

5. Input/Output Terminals

5-1) Pin out List

Pin #	Type	Single	Description	Remark
1		NC	Do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I^2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I^2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 5-5
9	O	BUSY	Busy state output pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command control pin	Note 5-2
12	I	CS #	Chip Select input pin	Note 5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	C	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW in parallel interface. When CS# is not in use, please connect to VCI or VSS.

http://www.good-display.com

Note 5-2: This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at [7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be interpreted as command.

Note 5-3: This pin is reset signal input.
Active Low.

Note 5-4:This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. e.g., The chip would put Busy pin High when
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5:

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

http://www.good-display.com

6. Command Table

D/C# =0, R/W# (WR#) =0, E（RD# =1）unless specific setting is stated.

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
1	0 -		0	0	0	0	0	A2	A1	A0	Status Read	Read Drive Status on *A2:BUSY flag *A1,A0:Chip ID(01 as default)
0	-	010	0	0	0	0	0	0	0	A0	Deep Sleep mode	Deep Sleep mode Control
0	1 -		0	0	0	0	0	0	0	A0	-	A[0] / Description 0 [POR] 1 Enter Deep Sleep Mode
0	0	20	0	0	1	0	0 0		0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrup t this o peration to avoid corruption of panel images
0	0	21	0	0	1	0	0	0	0	1	Display Update	Option for Display Update
0	1 -		A7	0	A5	A4	A3	A2	A1	A0	Control 1	Bypass Option Used for Pattern Display, which is used for display the RAM content into the Display. OLD RAM Bypass option A[7] 1 Enable bypass 0 Disable bypass [POR] A[5 : 4] valve will be used as for bypass 00 [POR] A[3 : 0] Initial Update Optio n-Source Control

	GSC A[3 : 2]	GSD A [1 : 0]
0000	GS0	GS0
0001	GS0	GS1
0010	GS0	GS2
0011 [POR]	GS0	GS3

													0100	GS1	GS0
													0101	GS1	GS1
													0110	GS1	GS2
													0111	GS1	GS3
													1000	GS2	GS0
													1001	GS2	GS1
													1010	GS2	GS2
													1011	GS2	GS3
													1100	GS3	GS0
													1101	GS3	GS1
													1110	GS3	GS2
													1111	GS3	GS3
0	0	22	0	0	1	0	0 0		1	0	Display Update	Display Update Sequence Option			
0	1 -		A7	A6	A5	A4	A3	A2	A1	A0	Control 2	Enable the stage for Master Activation			

Parameter (in Hex)

Enable Clock Single
Then Enable CP
Then   lo ad Temperature Value
Then Load LUT   FF
The INIITIAL DISPLAY   [POR]
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC
Enable Clock Single
Then Enable CP
Then Load Temperature value
Then Load LUT   F7
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC
To Enable Clock Single
(CLKEN =1)   80
To Enable Clock Single
Then Enable CP   C0
(CLKEN =1,CPEN =1)
To INITIAL
DIALAY+PATTEN
DISLAY   0C
To INITIAL DISPLAY   08

													Description
													To DISPLAY PATTEN 04 To Disable CP then Disable Clock Single (CLKEN =1) 01 Remark: CLKEN=1 If CLS = VDDIO then Enable OSC If CLS = VSS then Enable External Clock CLKEN=0 If CLS = VD DIO then Disable OSC AND INTERNAL CLOCK Single = VSS
0	0	24	0	0	1	0	0 1		0	0		Write RAM	After this command, data entries will be written into the RAM un til another command is written . Address pointers will advance accordingly.
0	0	3C	0	0	1	1	1 1		0	0		Border Waveform	Select border waveform for VBD
0	1 -			A7	A6	A5	A4	A3	A2	A1	A0	Control	A [7] Follow Source at initial Update Display A [7] = 0: [POR] A [7] = 1: Follow Source at initial Update Display for VBD A [6] setting are being overridden at Initial Display STAGE A[6] Select GS Transition/ Fix Level for VBD A[6] = 0: Select GS Transition A[3:0] for VBD A[6] = 0: Select Fix level Setting A[5:4] for VBD [POR] A[5:4] Fix Level Setting for VBD

	VBD
00	VSS
0	VSH
10	VSL

11[POR]	HiZ

A[3:0] GS tran sition setting f or VBD (Select waveform like data A[3:2] to data A[1:0])

	GSA	GSB
0000	GS0	GS0
0001	GS0	GS1
0010	GS0	GS2
001 [POR]	GS0	GS3
0100	GS1	GS0
0101	GS1	GS1
0110	GS1	GS2
0111	GS1	GS3
1000	GS2	GS0
1001	GS2	GS1
1010	GS2	GS2
1011	GS2	GS3
1100	GS3	GS0
1101	GS3	GS1
1110	GS3	GS2
1111	GS3	GS3

0	0	44	0	1	0	0	0 1		0	0	Set RAM X — address Start / End position	Specify the start / end positions of th e window address in the X directio n by an address unit. A[7 :0] :X Start ,POR = 00h B[7 :0] :X End, POR = 1Fh
0	1 -		0	0	0	A4	A3	A2	A1	A0		
0	1 -		0	0	0	B4	B3	B2	B1	B0		
0	0	4E	0	1	0	0	1 1		1	0	Set RAM X address counter	Make initial setting for the RAM X address in the address counter (AC) POR is 0
0	1 -		0	0	0	A4	A	A2	A1	A0		
0	0	4F	0	1	0	0	1 1		1	1	Set RAM Y address counter	Make initial setting for the RAM Y address in the address counter (AC) POR is 0
0	1 -		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	F0	1	1	1	1	0 0		0	0	Booster Feedback Selection	Set Booster Feedback Selection 0×1F=Internal Feedback is used POR is 0×3F
0	1 -		A7	A6	A5	A4	A3	A2	A1	A0		

7. Electrical Characteristics

7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.5 to +3.6	V
Logic Input Voltage	V_{IN}	-0.5 to VCI +0.5	V
Logic Output Voltage	V_{OUT}	-0.5 to VCI +0.5	V
Operating Temp. range	T_{OPR}	0 to +50	℃
Storage Temp. range	T_{STG}	-25 to +70	℃

7-2) Panel DC Characteristics
The following specifications apply for : VSS = 0V, VCI = 3.0V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.4	3.0	3.3	V
High level input voltage	VIH	-	0.8VCI	-	-	V
Low level input voltage	VIL	-	-	-	0.2VCI	V
High level output voltage	VOH	IOH= -100uA	0.9VCI	-	-	V
Low level output voltage	VOL	IOH= 100uA		-	0.1VCI	V
Maximum power panel	P_{MAX}	--	-	-	3.610	mW
Standby power panel	T_{STBY}	-	-	-	TBD	mW
Typical power panel	P_{TYP}	-	-	0.657	-	mW
Operating temperature	-	-	0	-	50	℃
Storage temperature	-	-	-25	-	70	℃
Maximum image update Time at 25℃	-	- -		1000	-	ms
Deep sleep mode current	VCI	DC/DC off No clock No input load Ram data not retain	-	2	5	uA
Sleep mode current	VCI	DC/DC off No clock No input load Ram data retain	-	35	50	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern.(Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED

Ver 1.1   **SEP.04.2011**   **12 / 26**

- Vcom is recommended to be set in the range of assigned value $\pm$ 0.1V.

Note 7-1

The Typical power consumption
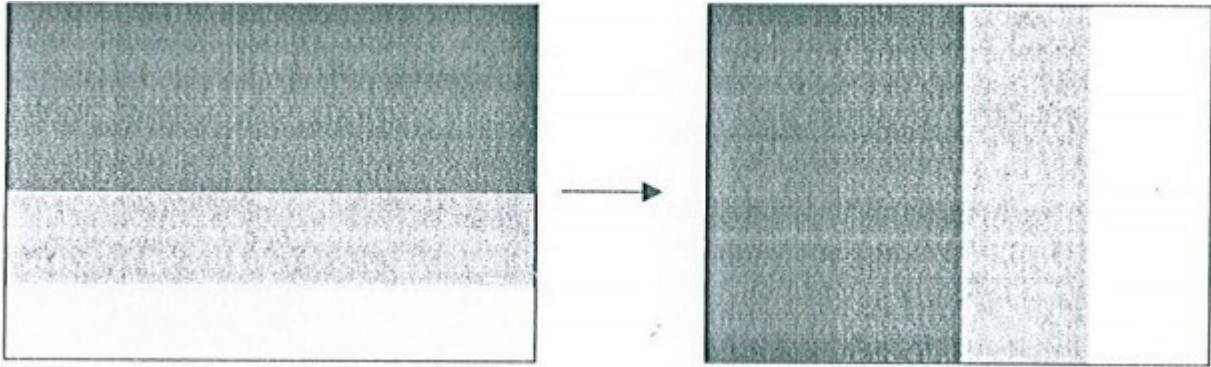
7-3) Panel AC Characteristics

The following specifications apply for : VSS = 0V, VCI = 3.0V, T$_A$ = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.4 to 3.3V	0.95	1	1.05	MHz

7-3-1) MCU Interface

Note 7-2 : L is connected to VSS

Note 7-3 : H is connected to VCI

7-3-1-1) MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins .The pin assignment at different interface mode is summarized in Table 7-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports spi4 or spi3 interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDin	SCLK	CS#	D/C#	RES#
SPI3	SDin	SCLK	CS#	L	RES#

MCU interface assignment under different bus interface mode

7-3-1-2) MCU Serial Interface (4-wire SPI)

The serial interface consists of serial cl ock SCLK, seri al data SDIN, D/C# , CS#.   In SPI   mode ,D0 acts a s SCLK, D1 acts as SDIN .

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Control pins of Serial interface

Note 7-9 : ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in order of D7,D6, D0.D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM(RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 7-5 : Write procedure in SPI mode
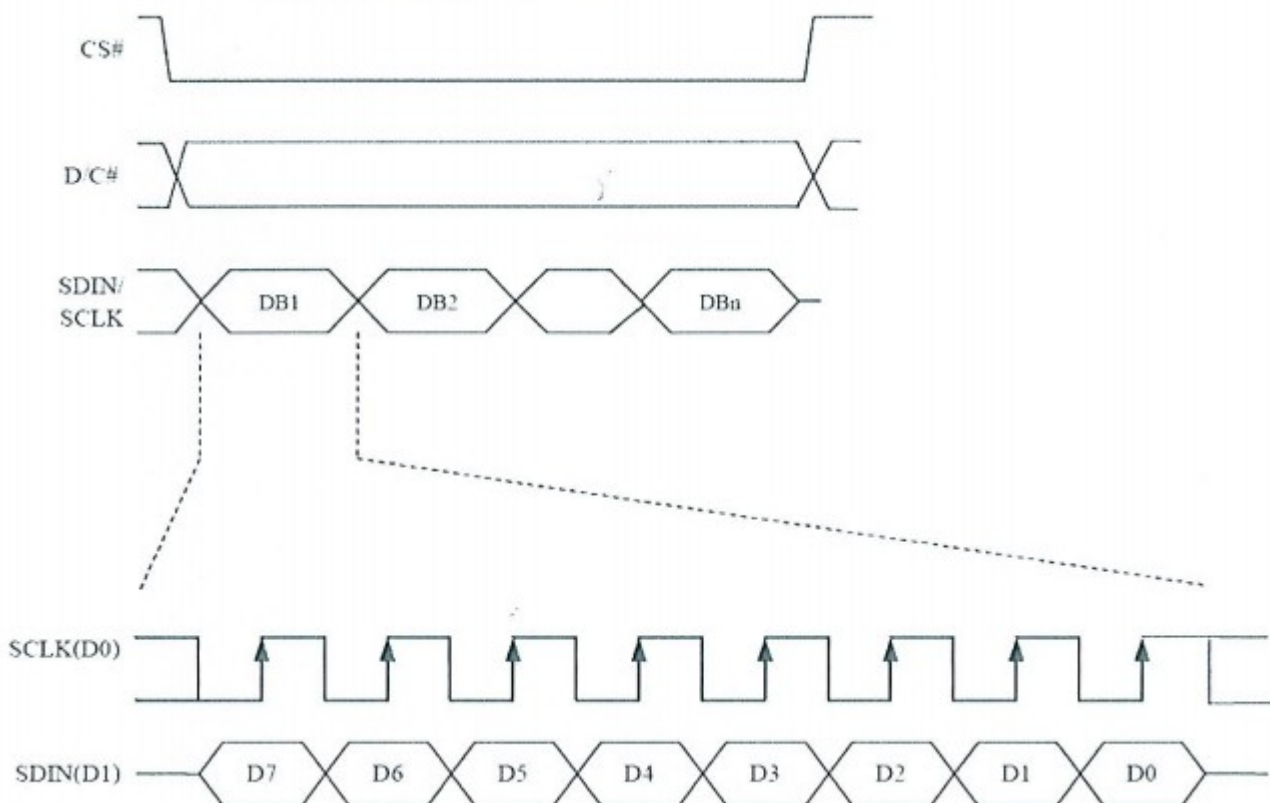
7-3-1-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode,D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence : D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode ,only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Control pins of 3-wire Serial interface

Note 7-10 : ↑ stands for rising edge of signal

Figure 7-6 : Write procedure in 3-wire Serial interface mode
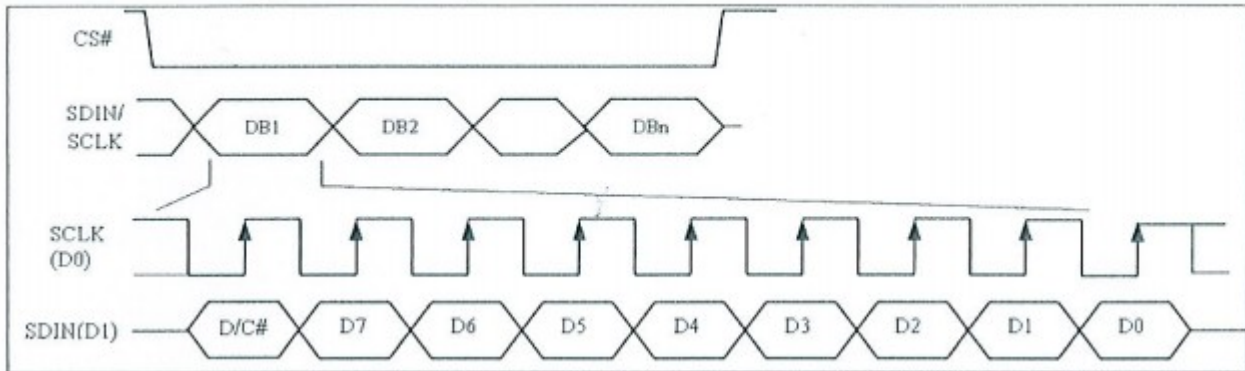
7-3-2) Timing Characteristics of Series Interface

◆ Series Interface Timing Characteristics

(VCI - VSS = 1.8 V to 2.0 v , $T_A = 25°C$, $C_L = 20$ pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20%~80%]	-	-	15	ns
t_F	Fall Time [20%~80%]	-	-	15	ns

◆ Series interface characteristics
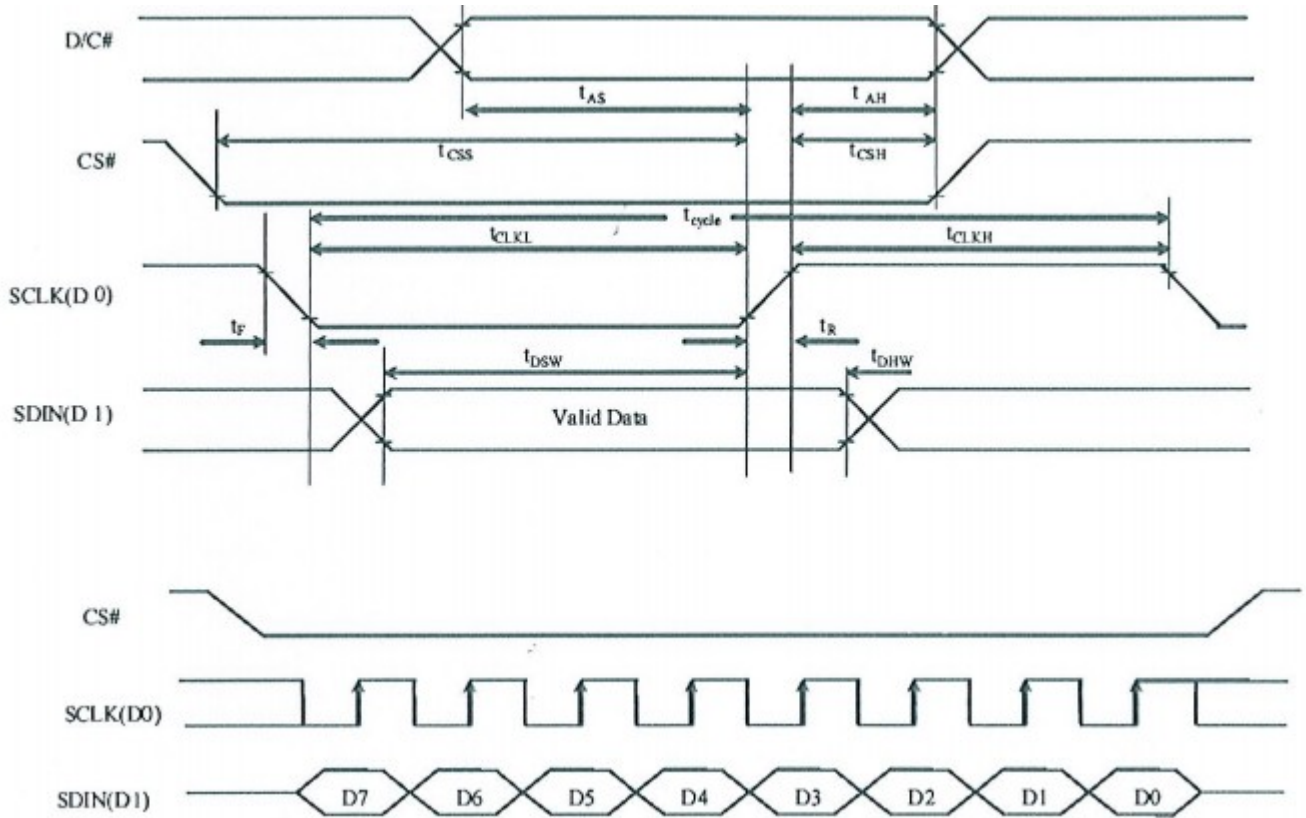
7-4) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	-	0.657	3.610	mW	-
Power consumption in standby mode	-	-	-	TBD	mW	-

7-5) Reference Circuit
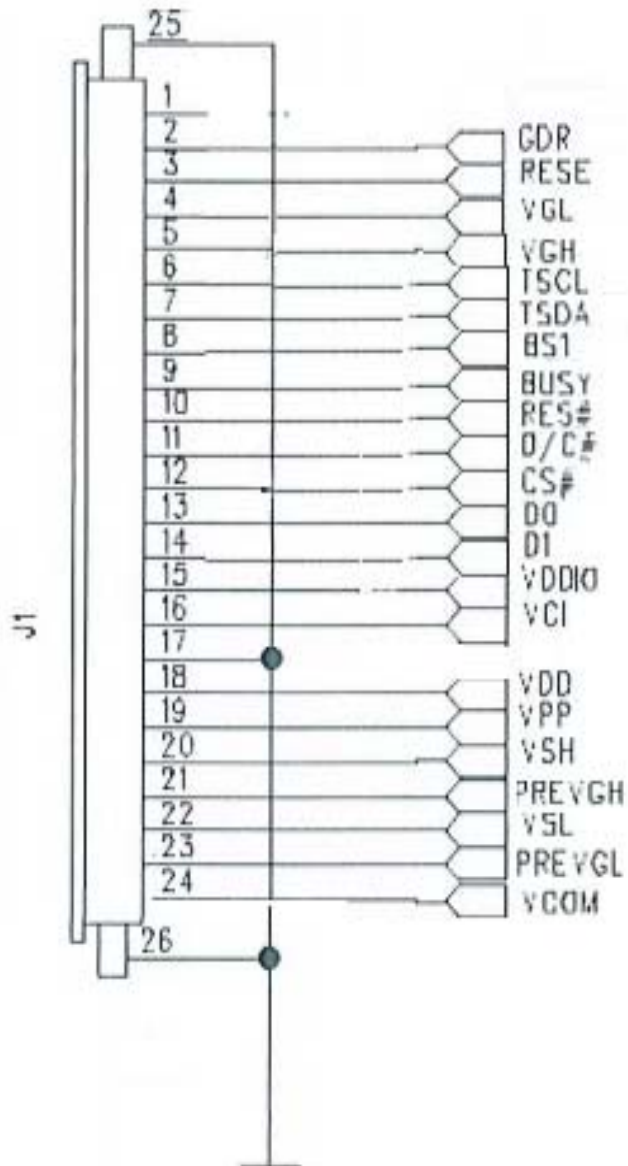
■

Figure . 7-5 (1)

VCDM VSL VSH VDD VCI VGH VGL

| C1 | C3 | C5 | C6 | C7 | C9 | C10 |
| 1uF/6V | 1uF/25V | 1uF/25V | 1uF/6V | 1uF/6V | 1uF/25V | 1uF/25V |

Figure . 7-5 (2)

TSDA
TSCL

R1 2.2K
R2 2.2K

LM75A

U1

4 GND
3 OS
2 SCL
1 SDA

VCC 8
A0 7
A1 6
A2 5

C8
0.1uF/6V

VCI

Figure . 7-5 (3)

Figure . 7-5 (4)

http://www.good-display.com
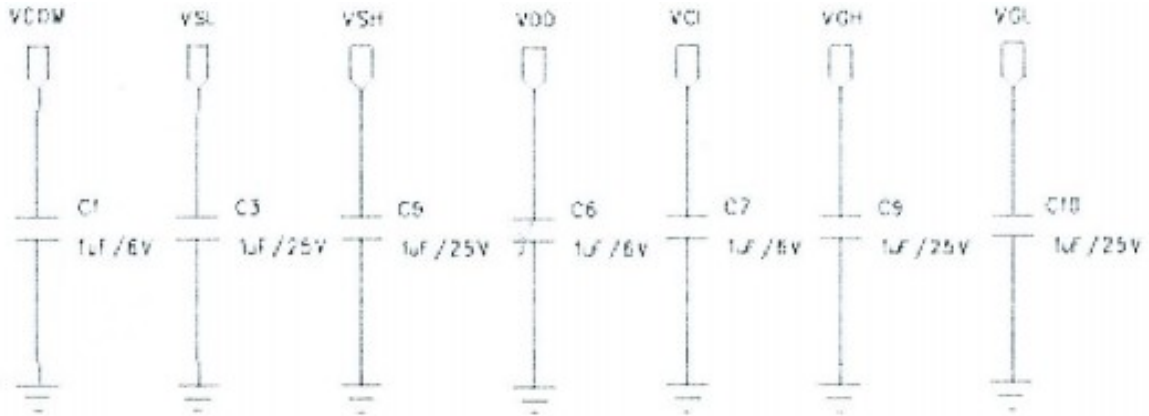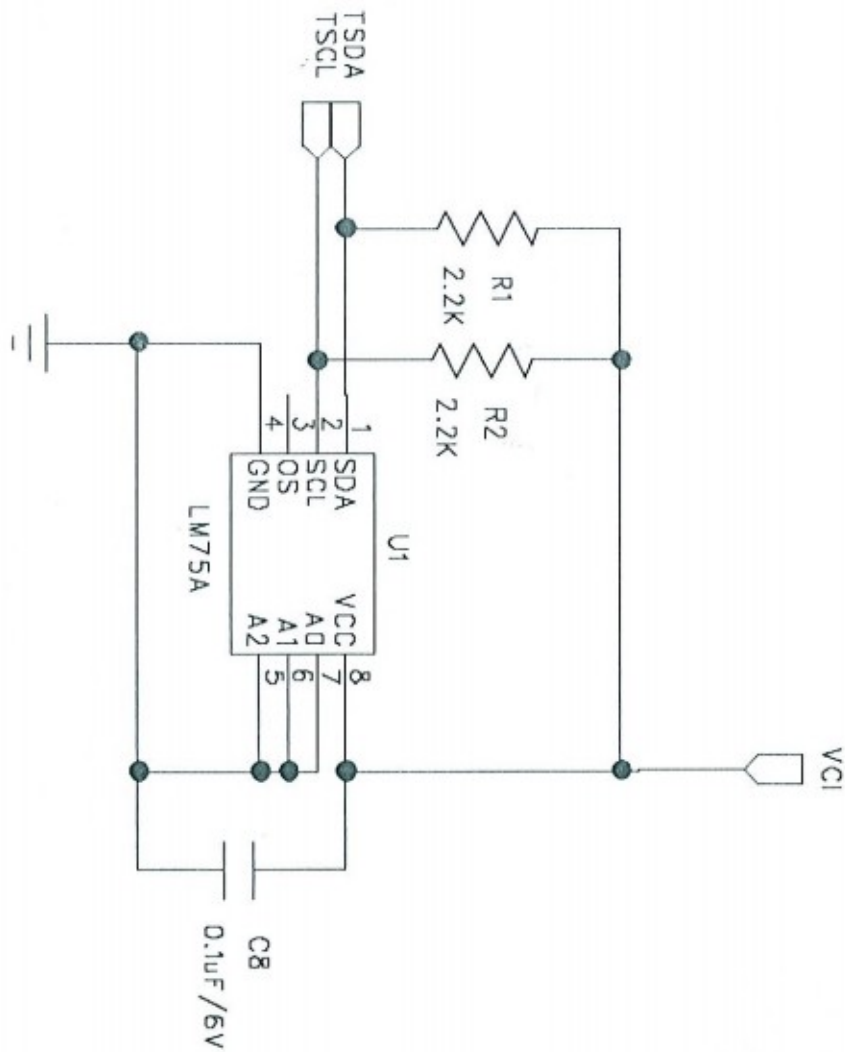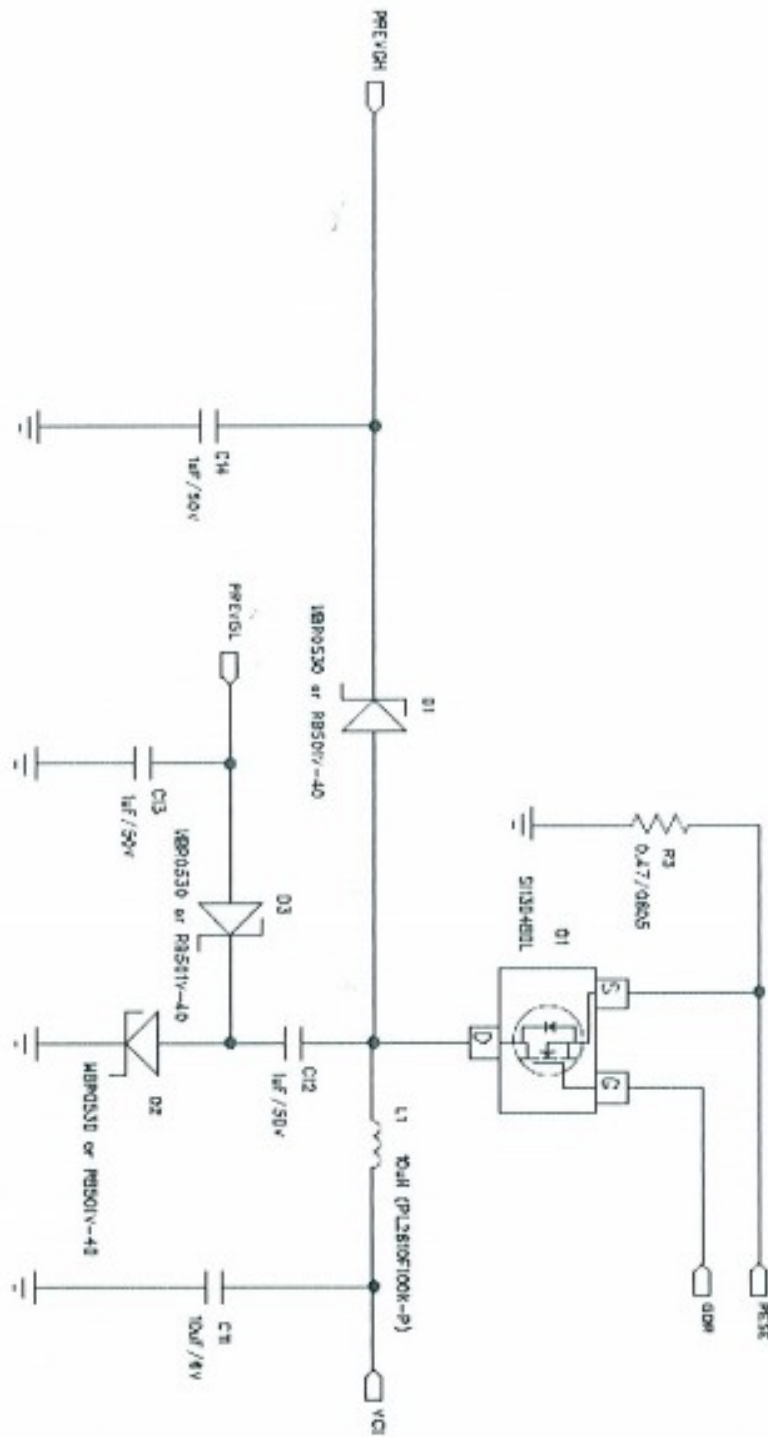
8. Typical Operating Sequence

Initialize display :

```
Command 21H
    ↓
Data 8FH
    ↓
Command 03
    ↓
Data 00H
    ↓
Command 24H
    ↓
Deliver 5760 times of
data FFH
    ↓
Data F8H
    ↓
Command 20H
```
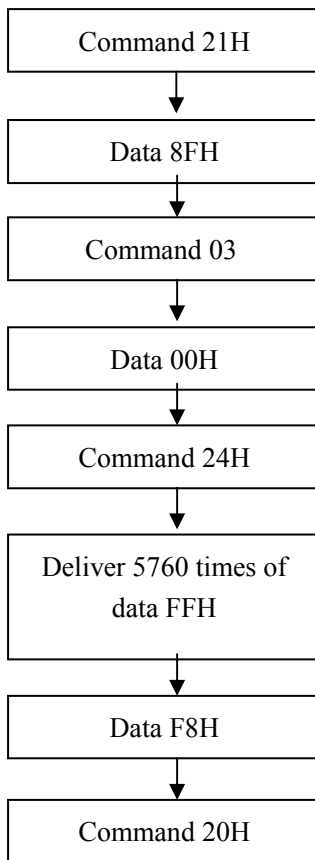
Close charge pump (shut down) :

```
Command 22H
    ↓
Data 1FH
    ↓
Command 20H
```

Open charge pump :

```
Command F0H
    ↓
Data 83H
    ↓
Command 22H
    ↓
Data C0H
    ↓
Command 20H
```

http://www.good-display.com
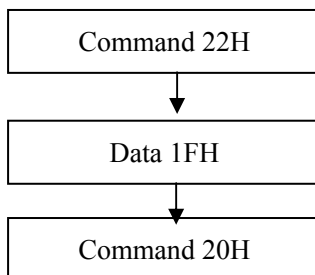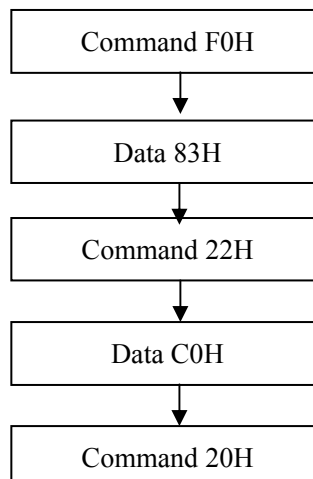
Normal display sequence :

Image resolution : 72×172

Image type   : 24-bit.   Note : 1

Flowchart (left column):

- Command F0H
- Data 1FH
- Command 22H
- Data C0H
- Command 20H
- Command 44H
- Data 00H
- Data 12H

Flowchart (right column):

- Command 4EH
- Data 00H
- Command 4FH
- Data 00H
- Command 24H
- Transmit image byte data (Note 1)
- Command 21H
- Data 0FH
- Command 22H
- Data F4H
- Command 20H
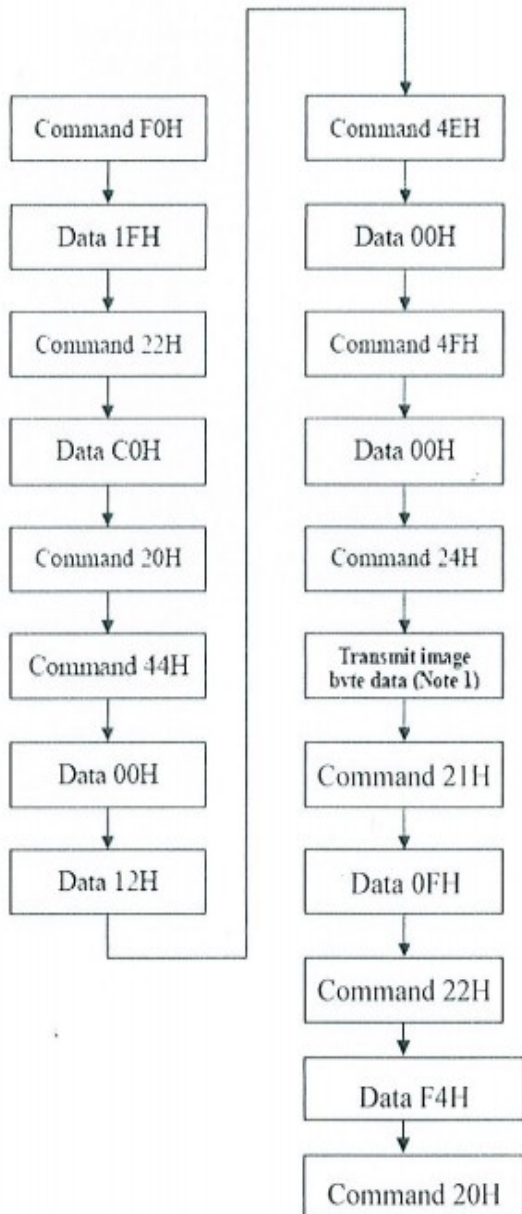
Change image format :

Original image data	00H~3FH	40H~7FH	80H~BFH	C0H~FFH
Send data to ic	00B	01B	10B	11B

Ex :

11B   11B   11B   11B → 11111111B (combine)

→ Send 11111111B to ic

01B   10B   01B   10B → 01100110B (combine)

→ Send 01100110B to ic

9. Optical characteristics

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	YPY	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS) xn (m−1)	-	L* -	
CR	Contrast Ratio	-	6		-	- -	
T_{update}	Update time	2~4-bit mode	-	-		sec	-

WS : White state, DS : Dark state

Gray state from Dark to White : DS、G1、G2 ••、 Gn ••、 Gm-2、WS
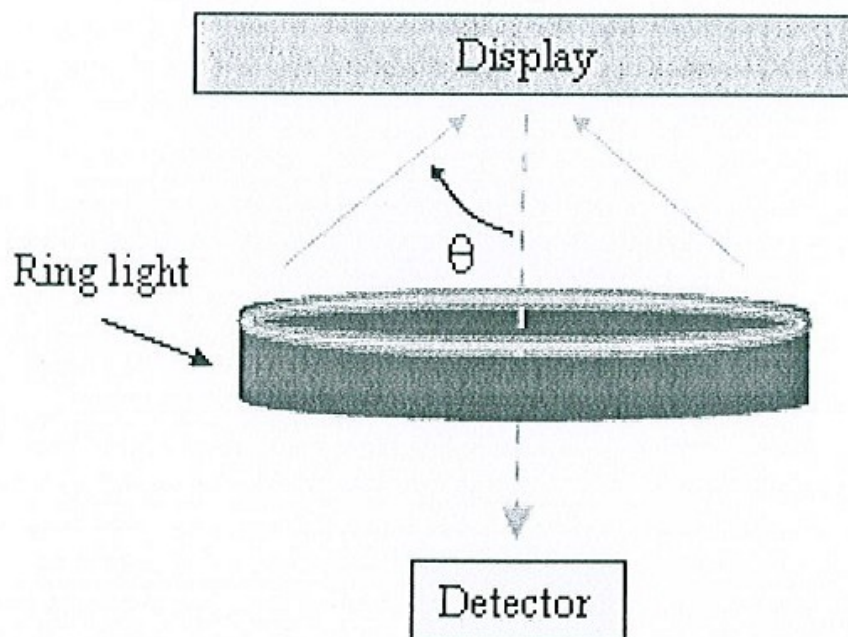
m : 4, when 2 bits mode

Note 9-1 : Luminance meter : Eye – One Pro Spectrophotometer

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

CR = R1/Rd

9-3) Reflection Ratio

The reflection ratio is expressed as :

http://www.good-display.com

R = Reflectance Factor $_{\text{white board}}$ x (L $_{\text{center}}$ / L $_{\text{white board}}$)

L $_{\text{center}}$ is the luminance measured at center in a white area (R=G =B=1) . L $_{\text{white board}}$ is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .
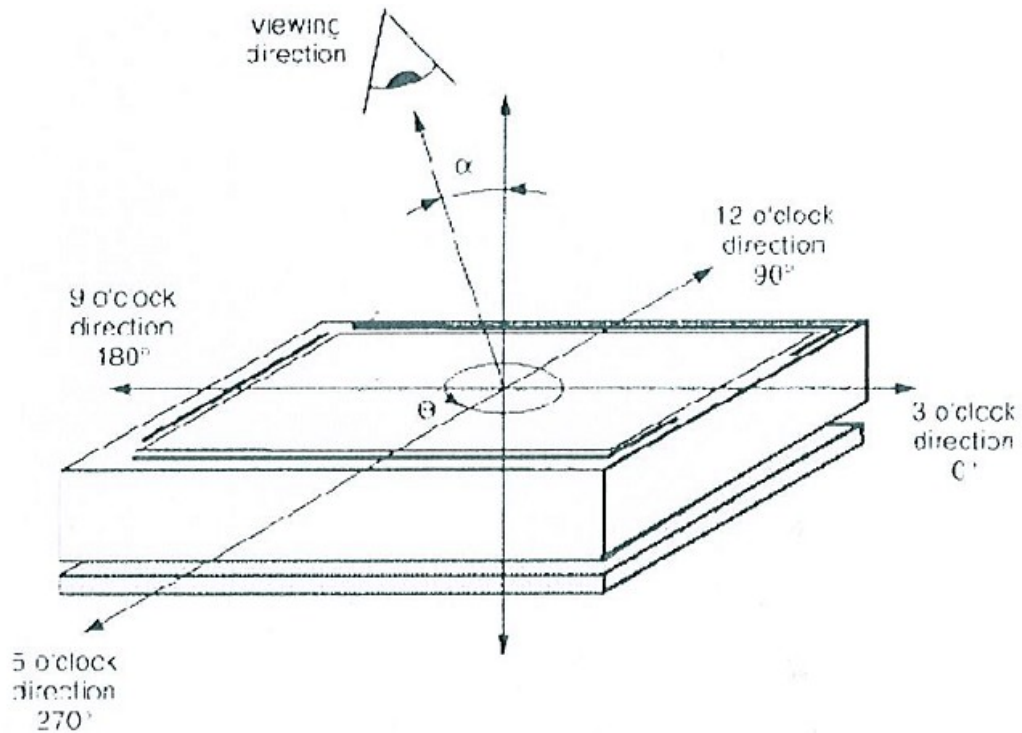
10. HANDLING，SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface . Handle with care.
Should the display break, do not touch the electrophoretic material . In case of contact with electrophoretic material , wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases , such as acid and alkali gases , which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components . The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied . Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given , it is advisory and dose not form part of the specification.	

11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 50℃,30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70℃, 23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40℃,RH=90%for168hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+60℃,RH=80%for240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→ +70℃,100 cycles 30mins 30mins Test in white pattern	IEC 60 068-2-14	
8	UV exposure Resistance	765 W/m^2 for 1688 hrs,40℃	IEC 60 068-2-5 Sa	
9	Electrostatic Effect (non-operating)	Machine mode +/- 250V, 0Ω ,200pF	IEC62179, IEC62180	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
12	Altitude test Operation	700hPa (=3000 m),48Hr		
13	Altitude test Storage	260hPa (=10000 m),48Hr Test in white pattern		

Actual EMC level to be measured on customer application.

Note : The protective film must be removed before temperature test.

http://www.good-display.com

12. Block Diagram

http://www.good-display.com