CS2610: Computer Organization and Architecture Lab

Lab-7: Virtual Memory Management

21^{st} April 2025

In modern computer systems, virtual memory is a critical feature that enables efficient use of physical memory while providing process isolation and flexibility. In the RISC-V architecture, this is achieved through a hierarchical page table structure and the Supervisor Address Translation and Protection (SATP) mechanism. In this assignment, you will delve into the workings of virtual memory by creating and configuring page tables, enabling paging, and verifying address translations. This hands-on experience will help you understand the foundational concepts of memory management and privilege modes in RISC-V, preparing you to design and debug systems that rely on virtual memory.

The following is the description of what you are supposed to do.

- ***Step-1:*** Switch execution from Machine Mode to Supervisor Mode.
- ***Step-2:*** Initialise the page table, i.e. fill in the page table entries at appropriate the memory locations (refer to Fig.1). Keep in mind, we are doing *Sv39*-paging.

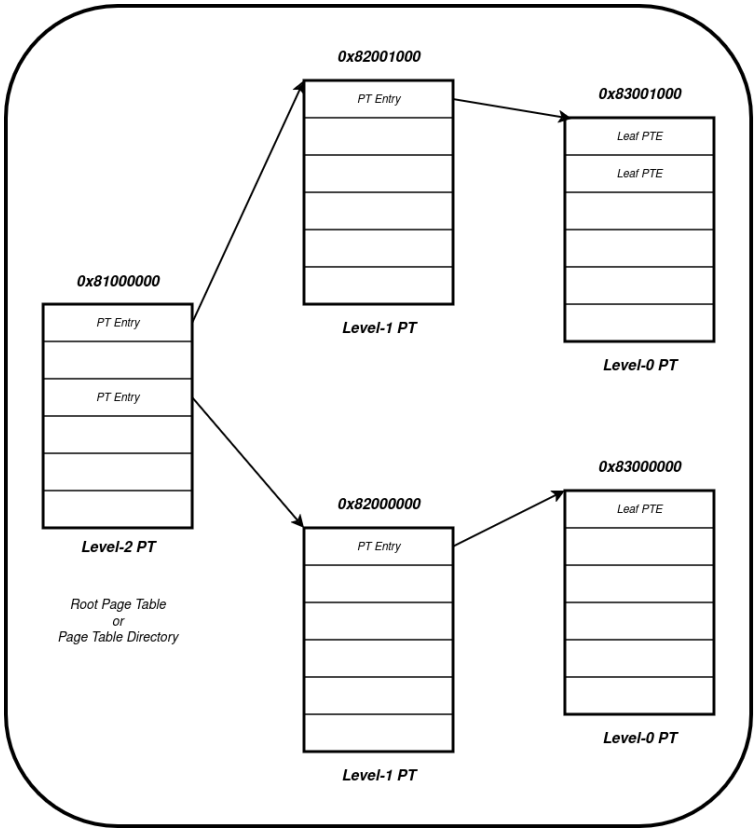

Figure 1: Page Table Structure for Sv39

- ***Step-3:*** Set the appropriate value at to the ***satp*** register by assigning a value to ***satp_config***

- ***Step-4:*** Switch execution from Supervisor Mode to User Mode.
- ***Step-5:*** Do you see that your physical addresses (the ones see in your *dump*-file) was replaced with their virtual addresses (when executing in spike)?

**** Keep in mind to align all the different components properly ****

- In case you forgot what your aim is, refer Fig.2.
- In case you forgot what these registers do, how does the page translation occur, and what values do you set to the registers, go to *References.*

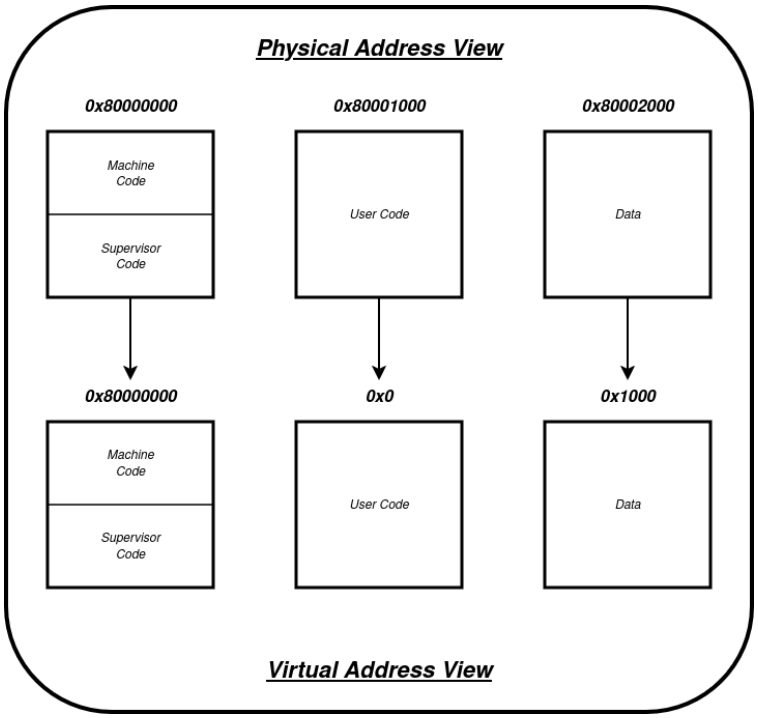

Figure 2: Pictorial view of the aim of the assignment

References:

- The OG Document: RISC-V ISA Manual: Volume II (Privileged Architecture)
- The Lecture slides: Virtual Memory, Privileges and Interrupts
- Important parts in the OG Document:
  - Section 3.1.6: Machine Status Registers (mstatus)
  - Section 7.1.11: Supervisor Address Translation and Protection (satp) Register
  - Section 7.3.2 Virtual Address Translation Process
  - Section 7.4: Sv39: Page-Based 39-bit Virtual-Memory System
- Where to start? - The self-evident code template (va_template.S)
- How to switch between privilege modes? - Refer to your own code from the previous labs

- How to compile and create a dump file?

```
$ riscv64-unknown-elf-gcc -nostartfiles -T linker.ld va_template.S
$ riscv64-unknown-elf-objdump -D a.out > dump
```

- More doubts? - Ask your smart, funny, kind, caring and helpful TAs :)

As you step into the academic realm, recall the wisdom of the wise man: ***"In the grand symphony of learning, let laughter be your melody!"*** Embrace the joy of discovery, the camaraderie of exploration, and the whimsicality of knowledge. May your journey be filled with mirth and enlightenment. Onward, with a merry heart!