Low-Harmonic-Input Three-Phase Rectifier With Passive Auxiliary Circuit: Comparison and Design Consideration

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***Abstract*—A novel passive correction approach to improve the input currents of a conventional three-phase rectifier with dc-side C filter is studied in this paper. By adding an inductor and capacitor passive auxiliary circuit to the ac side of the rectifier, good mains behavior would be achieved. A family of low-harmonic-input three-phase rectifiers with passive auxiliary circuit is derived. From the comparative analytical results in operation principle, auxiliary circuit design, characteristic discussion, and simulation results, some important conclusions are drawn. Experimental results from the prototypes built in the laboratory with different specifications are shown to confirm the validity of the analysis and the feasibility of the proposed approach.**

***Index Terms*—Auxiliary circuit, harmonics, low harmonic input, three-phase rectifier.**

I. Introduction

CONVENTIONAL three-phase rectifiers with dc-side C filters are widely used as interface circuits between the grid and power electronic equipment for their simplicity and reliability. Because of the nonlinear characteristic of diodes, a large amount of harmonics are drawn from the grid, leading to severely distorted input currents and low power factors [1].

Reducing the input-current harmonics by modifying the rectifier itself mainly includes the following techniques. Pulsewidth modulation rectifiers could improve the input currents effectively, but the shortcomings of high cost, large switching loss, and unsatisfactory efficiency limit their application, particularly in the high-power application situation [2], [3], Multiple-pulse rectifiers could achieve acceptable input currents in relatively low cost and good electromagnetic interference (EMI), but the achievement of satisfactory input current usually accompanies the increase of pulse number, leading to larger bulk and heavier weight of the equipment [4], [5]. Rectifiers applying current injection contribute to the reduction of the input current by injecting third-order current harmonics, which could be stimulated by the inherent third-order fluctuation of a conventional rectifier into the input terminal of the rectifier. Distortion of the input current could be suppressed, but the method does not get widely used [6], [7]. Some novel rectifiers, such as rectifiers with near-sinusoidal input currents (RNSICs), are proposed in recent years. An RNSIC converter, which is composed of input inductors, a three-phase diode rectifier, and commutation capacitors connected with the diodes, could effectively improve the input currents and power factors [8]–[11]. RNSIC converters have caught increasing attention for their simple fabrication and high reliability, but research on them is inadequate and unsystematic.

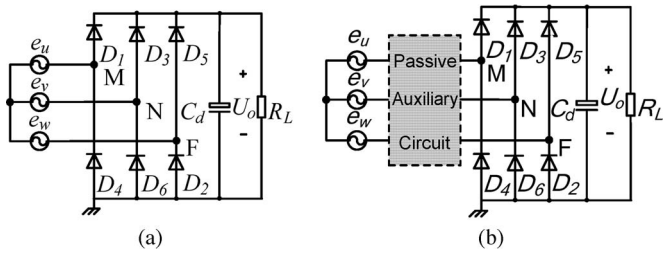

Fig. 1. Three-phase rectifiers with dc-side C filter. (a) Conventional uncontrollable three-phase rectifier. (b) Proposed rectifier with passive auxiliary circuit.

Based on the former research, a novel passive correction approach is proposed in this paper. By adding an inductor–capacitor auxiliary circuit to the input terminal of the diode bridge rectifier, a family of low-harmonic-input three-phase rectifiers is derived. They are only composed of passive components that suit to work in high-power application with high-EMI requirement. Some important conclusions are drawn from the comparative analytical results of three typical rectifiers in operation principle, auxiliary circuit design, and characteristic discussion. Meanwhile, simulation results of RNSIC converters under more generalized operation conditions are given. Finally, by using the design method proposed in this paper, seven prototypes are built in the laboratory. Experimental results are shown to confirm the validity of the analysis and the feasibility of the proposed design method.

II. Topologies of Low-Harmonic-Input Three-Phase Rectifier With Passive Auxiliary Circuit

By adding a passive auxiliary circuit to the input terminal of a conventional uncontrolled rectifier (as Fig. 1(a) shows), a novel low-harmonic-input three-phase rectifier (as Fig. 1(b) shows) is obtained.

The basic inductor and capacitor auxiliary circuit is shown in Fig. 2(a). This type of LC second-order circuit is widely

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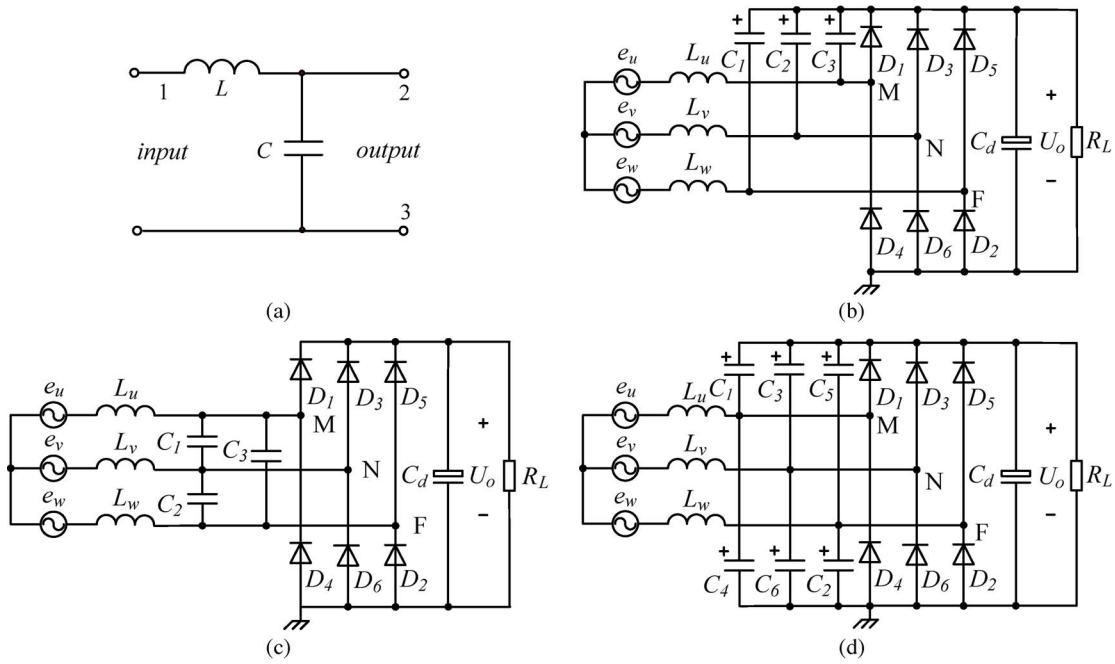

Fig. 2. Family of low-harmonic-input three-phase rectifiers with passive auxiliary circuit. (a) LC second-order auxiliary circuit. (b) Topology 1. (c) Topology 2. (d) Topology 3.

used in switching power converter application as the output and input filters [12]–[14]. By adding this kind of auxiliary circuit to the input terminal of the diode bridge rectifier, a family of low-harmonic-input three-phase rectifiers with auxiliary circuit is derived. By connecting the neuter point of commutation capacitors to the dc bus, topology 1 is derived (as Fig. 2(b) shows) [11]; changing the Y-connection commutation capacitors to be Δ-connection, topology 2 is derived (as Fig. 2(c) shows) [10]; and replacing the upper commutation capacitor by symmetrical capacitors, topology 3 is derived (as Fig. 2(d) shows) [8], [9].

Meanwhile, topologies 1, 2, and 3 are named as RNSIC-3, RNSIC-2, and RNSIC-1, respectively.

These three topologies are comparatively investigated and analyzed in operation principle, auxiliary circuit optimal design, and characteristic discussion to reveal some general rules of this family of low-harmonic-input rectifiers.

III. Comparison of Operation Principle

As Fig. 2 shows, RNSIC converters are composed of three series inductors $L_u, L_v,$ and L_w of equal inductance values L's and commutation capacitors of equal capacitance values C's. The commutation capacitors are C_1–C_6 in RNSIC-1 but C_1–C_3 in RNSIC-2 and RNSIC-3.

For the sake of simplicity, the following simplifications are performed. The mains currents are purely sinusoidal, and there is no phase displacement between voltages and current

$$e_u = U_m \sin \omega t \quad i_u = I_m \sin \omega t \tag{1}$$

$$e_v = U_m \sin\left(\omega t - \frac{2}{3}\pi\right) \quad i_v = I_m \sin\left(\omega t - \frac{2}{3}\pi\right) \tag{2}$$

$$e_w = U_m \sin\left(\omega t + \frac{2}{3}\pi\right) \quad i_w = I_m \sin\left(\omega t + \frac{2}{3}\pi\right) \tag{3}$$

TABLE I
Startand End Time of the Currents Discharging C_1

Converter	Operation Mode	Start time	End time (t_1)
RNSIC-1 RNSIC-3	Large Current	0	$[0, \pi/(3\omega)]$
	Medium Current		$[\pi/(3\omega), 2\pi/(3\omega)]$
	Small Current		$[2\pi/(3\omega), \pi/(\omega)]$
RNSIC-2	Large Current		$[0, \pi/(3\omega)]$
	Medium Current	$[0, \pi/(6\omega)]$	$[\pi/(3\omega), \pi/(2\omega)]$
	Small Current	$\pi/(6\omega)$	$[\pi/(2\omega), 5\pi/(6\omega)]$

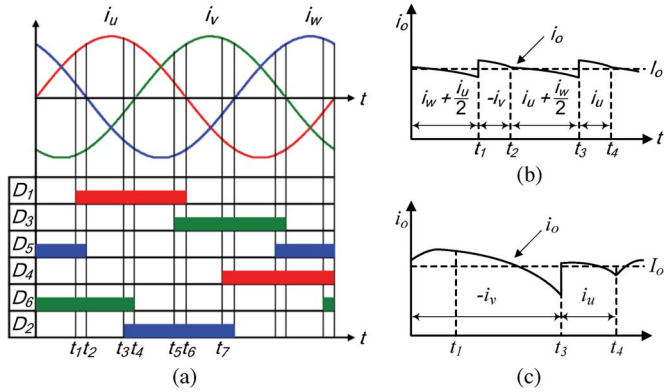

Fig. 3. Key waveforms of RNSIC converters working in large-current mode. (a) Diodes' conducting sequence in three topologies. (b) DC-link current i_o of RNSIC-1 and RNSIC-2. (c) DC-link current i_o of RNSIC-3.

where U_m is the amplitude of the phase voltage and I_m is the amplitude of the input currents.

Zero time point $(t = 0)$ is defined as the moment when current i_u crosses zero from negative to positive, and t_1 is defined as the moment when capacitor C_1 finishes discharging. In RNSIC converters, the start and end times of the currents discharging C_1 are given in Table I, from which we can see the duration that the charging or discharging of commutation

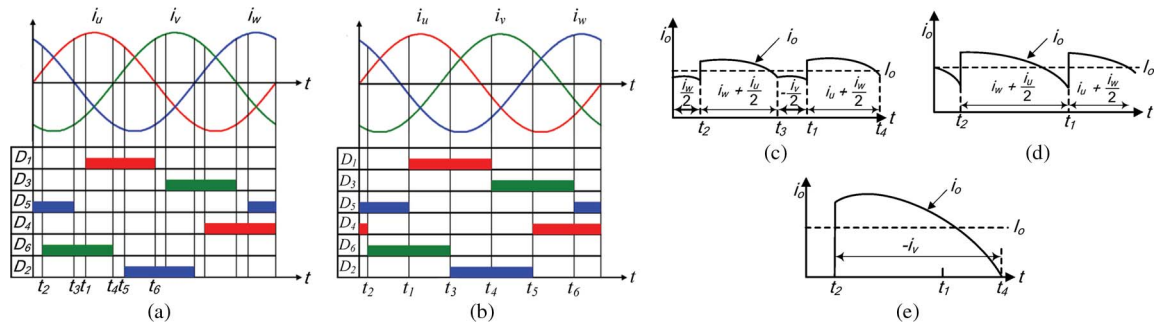

Fig. 4. Key waveforms of RNSIC converters working in medium-current mode. (a) Diodes' conducting sequence in RNSIC-1 and RNSIC-3. (b) Diodes' conducting sequence in RNSIC-2. (c) DC-link current i_o of RNSIC-1. (d) DC-link current i_o of RNSIC-2. (e) DC-link current i_o of RNSIC-3.

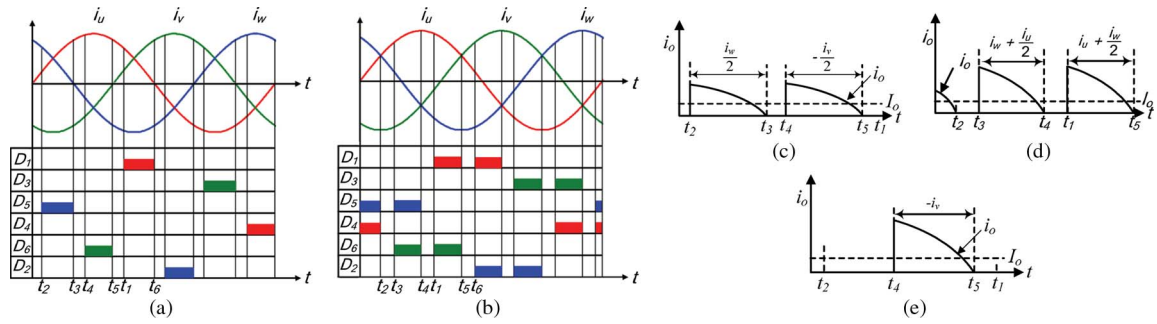

Fig. 5. Key waveforms of RNSIC converters working in small-current mode. (a) Diodes' conducting sequence in RNSIC-1 and RNSIC-3. (b) Diodes' conducting sequence in RNSIC-2. (c) DC-link current i_o of RNSIC-1. (d) DC-link current i_o of RNSIC-2. (e) DC-link current i_o of RNSIC-3.

capacitors varies with the load. The key waveforms of RNSIC converters working in large-, medium-, and small-current modes are shown in Figs. 3–5, respectively.

A. Large-Current Mode

For large-current mode, t_1 varies in the interval $[0, \pi/(3\omega)]$ (ω denotes the mains angular frequency).

The diodes of three RNSIC converters conduct in the same sequence (as Fig. 3(a) shows). Every one-sixth of the mains period $T = 2\pi/\omega$ composed of two distinct operation stages is the basic time cell of an RNSIC converter. For example, in RNSIC-1, in the first stage $(0 - t_1)$, diodes D_5 and D_6 are conducting, C_1 is discharging, while C_4 is charging. Then, in the second stage (t_1–t_2), three diodes D_1, D_5, and D_6 are conducting. Hereafter, the one-sixth period repeats over and over.

The dc-side current i_o is a 12-pulse waveform (as Fig. 3(b) shows) in RNSIC-1 and RNSIC-2, while it is a six-pulse waveform (as Fig. 3(c) shows) in RNSIC-3.

I_o, the mean value of dc-link current i_o in RNSIC-1 and RNSIC-2, could be expressed as follows:

$$I_o = \frac{3}{\pi}\left[\int_0^{\omega t_1}\left(I_m \sin\left(\omega t + \frac{2}{3}\pi\right) + \frac{1}{2} I_m \sin \omega t\right) d\omega t + \int_{\omega t_1}^{\frac{\pi}{3}} -I_m \sin\left(\omega t - \frac{2}{3}\pi\right) d\omega t\right] = \frac{3}{2\pi} I_m (1 + \cos \omega t_1). \quad (4)$$

Expressions of I_o in RNSIC converters are given in Table II.

TABLE II
EXPRESSIONS OF I_O IN RNSIC CONVERTERS

Converter	Operation Mode	Expressions of I_o
RNSIC-1 RNSIC-3	Large Current	$I_o = \frac{3}{2\pi} I_m (1 + \cos \omega t_1)$
	Medium Current	
	Small Current	
RNSIC-2	Large Current	
	Medium Current	$I_o = \frac{3\sqrt{3}}{2\pi} I_m \cos(\omega t_1 - \frac{\pi}{6})$
	Small Current	$I_o = \frac{3\sqrt{3}}{2\pi} I_m (1 + \cos(\omega t_1 + \frac{\pi}{6}))$

B. Medium-Current Mode

As Fig. 4 shows, in RNSIC-1 and RNSIC-3, diodes conduct in the same sequence, and the basic time cell one-sixth period is composed of two distinct operation stages in which one or two diodes conduct. In RNSIC-2, two diodes conduct at any time. In addition, RNSIC-3 has the largest dc-link current ripple, while RNSIC-1 has the best output-current behavior.

C. Small-Current Mode

In RNSIC-1 and RNSIC-3 working in small-current mode, diodes conduct in the same sequence, as shown in Fig. 5. The basic time cell one-sixth period is composed of two distinct operation stages in which none or one diode conducts, while in RNSIC-2, two distinct stages in which none or two diodes conduct exist. Additionally, the dc-link current i_o in three RNSIC converters becomes discontinuous.

From the aforementioned analysis, we could draw the following conclusions: RNSIC-3 could be seen equivalent with

RNSIC-1, and it has simpler configuration but with larger dc current ripple. RNSIC-2 and RNSIC-1 become equivalent in large-current mode.

IV. Auxiliary Circuit Optimal Design

A. Auxiliary Circuit Selection

The first issue that needs to be solved in rectifier design is to select a suitable RNSIC converter topology and to determine its operation mode, according to the requirement of application field (the input voltage, output voltage, and output power).

The input and output powers are given as

$$P_{\text{in}} = 3\frac{U_m}{\sqrt{2}}\frac{I_m}{\sqrt{2}} = 3\frac{U_m I_m}{2} \tag{5}$$

$$P_o = U_o I_o \tag{6}$$

where U_o is the output voltage, neglecting the voltage ripple.

Neglecting the power losses of the converter, substituting (5) and (6) into (4), and the solution for ωt_1 lead to

$$\omega t_1 = \arccos\left(\frac{\pi U_m}{U_o} - 1\right). \tag{7}$$

Note that the expression of ωt_1 is the function of U_m and U_o in RNSIC-1 and RNSIC-3. Similarly, the expression of ωt_1 in RNSIC-2 can be found as follows:

$$\omega t_1 = \begin{cases} \arccos\left(\frac{\pi U_m}{U_o} - 1\right), & \text{large-current mode} \\ \arccos\frac{\pi U_m}{\sqrt{3}U_o} + \frac{\pi}{6}, & \text{medium-current mode} \\ \arccos\left(\frac{\pi U_m}{\sqrt{3}U_o} - 1\right) - \frac{\pi}{6}, & \text{small-current mode.} \end{cases} \tag{8}$$

The variation of ωt_1 in RNSIC converters is shown in Fig. 6, in which the values of output voltage U_o are adopted as 300, 400, 500, and 600 V. From Fig. 9, we could find that RNSIC converters should be designed to work in small-current mode for the application with low input voltage and high output voltage, whereas the large-current mode is more preferable for the application with high input voltage and relatively low output voltage. Fig. 6 gives a criterion for us to determine the topology and operation mode of RNSIC converters.

B. Optimal Parameter Design Based on the Time-Weighted Averaging Method

As mentioned before, one-sixth of the mains period comprising two operation stages is the basic time cell of RNSIC, and the auxiliary circuit could be designed as follows.

Step 1) By using the (7), (8), and Fig. 6, we can determinate the auxiliary circuit type and operation mode according to the different input and output voltages.

Step 2) According to the operation mode of an RNSIC converter, choose one one-sixth period, and calculate the parameter value of the auxiliary circuit in two operation stages.

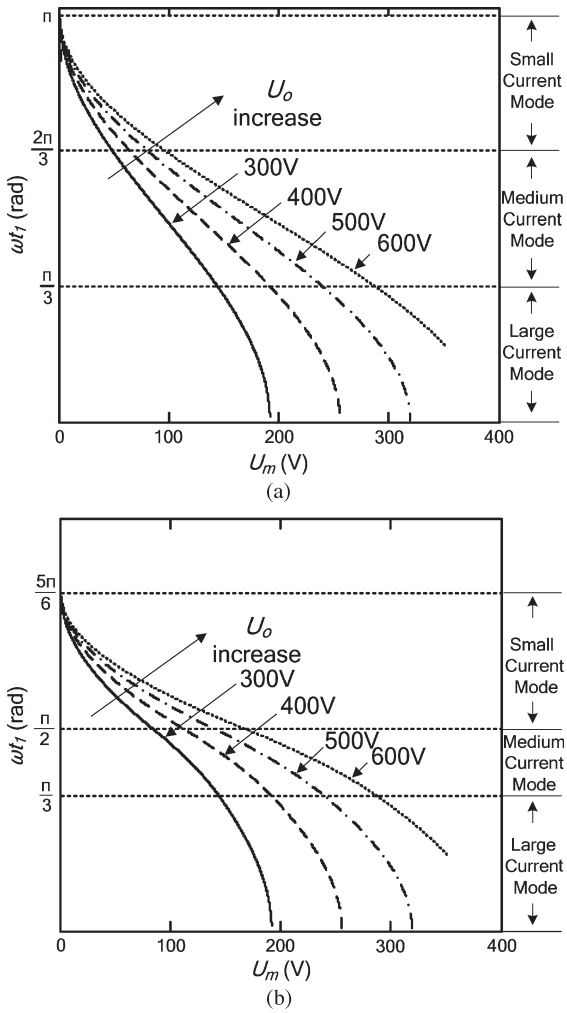

Fig. 6. Variations of ωt_1 as a function of U_m and U_o in RNSIC converters. (a) RNSIC-1 and RNSIC-3. (b) RNSIC-2.

Step 3) Use the time-weighted averaging method. The optimal parameter value is derived by weighted-averaging the two values derived previously.

Note that when RNSIC-2 works in medium-current mode, only a single operation stage exits in one time cell, and it should be designed separately.

C. Design Example

As an example, the input voltage U_m is 150 V, the desired output voltage U_o is 500 V, and the output power P_o is 6.55 kW. Now, let us consider the design of an RNSIC converter, and it is going to be optimized at the operating point.

Using (7), the value of ωt_1 is calculated as 0.518π, which means that the RNISC-1 working in medium-current mode can be selected to fulfill the requirement from Fig. 6(a). If (8) is used for calculation, the value of ωt_1 will be 0.484π. As shown in Fig. 6(b), the RNISC-2 working in medium-current mode can be selected as well. Here, typical RNSIC-1 is adopted to demonstrate the design procedure, and its equivalent circuit for one-sixth of the mains period is shown in Fig. 7.

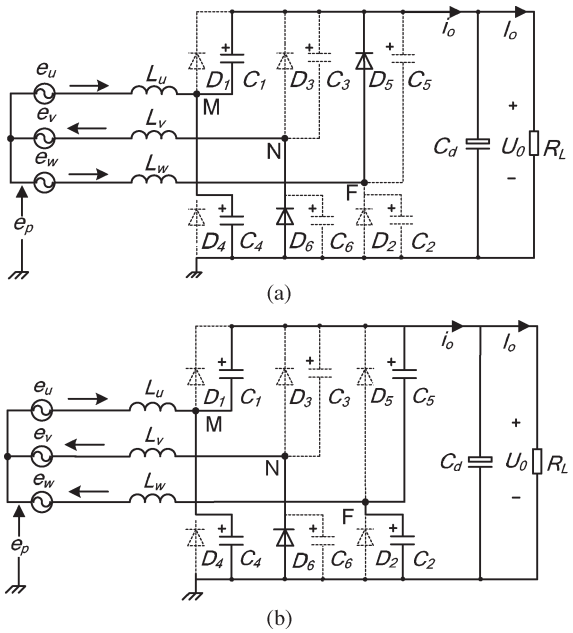

Fig. 7. Equivalent circuit of the RNSIC-1 working in medium-current mode for one-sixth of the mains period. (a) t_2–t_3. (b) $t_3 - t_1$.

The relationship between the ac-side voltage and current of rectifiers could be represented by employing Kirchhoff's voltage law as

$$e_p + e_u = L\frac{di_u}{dt} + u_M \tag{9}$$

$$e_p + e_v = L\frac{di_v}{dt} + u_N \tag{10}$$

$$e_p + e_w = L\frac{di_w}{dt} + u_F. \tag{11}$$

Considering the symmetric of three-phase voltage, the voltage of neuter point e_p can be found to be

$$e_p = \frac{u_M + u_N + u_F}{3}. \tag{12}$$

1) Value of Operation Stage $[t_2, t_3]$*:* At time point t_2, diode D_6 starts conducting (as Fig. 4(a) shows). Meanwhile, diode D_5 keeps conducting, and input current i_u keeps charging C_4 and discharging C_1 from zero time point. Thus, the voltage of point M, N, F could be expressed as follows:

$$u_M = u_{c4} = \frac{1}{C}\int_0^t \frac{1}{2} I_m \sin\omega t dt = \frac{I_m}{2C\omega}(1 - \cos\omega t) \tag{13}$$

$$u_N = 0 \tag{14}$$

$$u_F = U_o. \tag{15}$$

Substituting (13) for u_M, (14) for u_N, and (15) for u_F into (12) gives

$$e_p = \left[\frac{I_m}{2C\omega}(1 - \cos\omega t) + 0 + U_o\right]/3. \tag{16}$$

Subtracting (11) from (10) gives

$$e_v - e_w = L\left(\frac{di_v}{dt} - \frac{di_w}{dt}\right) + (u_N - u_F). \tag{17}$$

Substituting (2) for i_v, (3) for i_w, (14) for u_N, and (15) for u_F into (17) leads to

$$e_v - e_w = L\left[d\left(I_M \sin\left(\omega t - \frac{2\pi}{3}\right)\right)/dt - d\left(I_M \sin\left(\omega t + \frac{2\pi}{3}\right)\right)/dt\right] + (0 - U_o). \tag{18}$$

Integrating both sides of (18) on the angular interval $[\omega t_2, \omega t_3]$ and simplifying give the value L_1 of inductance as follows:

$$L_1 = \frac{\int_{\omega t_1 - \frac{\pi}{3}}^{\frac{\pi}{3}} (e_w - e_v - U_o) d\omega t}{I_m \omega \left[-\sin\left(\omega t_1 + \frac{\pi}{3}\right) - \sin\omega t_1 + \frac{\sqrt{3}}{2}\right]} = 27.3 \text{ mH}. \tag{19}$$

Here, ωt_2 corresponds to $\omega t_1 - \pi/3$, while ωt_3 corresponds to $\pi/3$.

Using the inductance value L_1 and substituting (2) for i_v, (14) for u_N, and (16) for e_p into (10) give

$$\left[\frac{I_m}{6C\omega}(1 - \cos\omega t) + \frac{U_o}{3}\right] + e_v = L_1\frac{di_v}{dt} + 0. \tag{20}$$

Integrating both sides of (20) on the angular internal $[\omega t_2, \omega t_3]$ and simplifying give the value C_1 of capacitance

$$C_1 = \int_{\omega t_1 - \frac{\pi}{3}}^{\frac{\pi}{3}} I_m(1 - \cos\omega t) d\omega t / 6\omega \left[L_1 \omega I_m \left(\sin\omega t_1 - \frac{\sqrt{3}}{2}\right) - \frac{U_o}{3}\left(-\omega t_1 + \frac{2\pi}{3}\right) - \int_{\omega t_1 - \frac{\pi}{3}}^{\frac{\pi}{3}} e_v d\omega t\right] = 103.3\ \mu\text{F}. \tag{21}$$

2) Value of Operation Stage $[t_3, t_1]$*:* At time point t_3, diode D_5 stops conducting, input current i_w starts charging C_5 and discharging C_2, input current i_u keeps charging C_4 and discharging C_1, and diode D_6 keeps conducting. Therefore, u_M and u_N have the same expression as that in the last stage, and u_F could be expressed as follows:

$$u_F = u_{c2} = u_{c2}|_{t=t_3} + \frac{1}{C}\int_{t_3}^{t} \frac{1}{2} I_m \left(\sin\omega t + \frac{2}{3}\pi\right) dt = U_o - \frac{I_m}{2C\omega}\left(1 + \cos\left(\omega t + \frac{2\pi}{3}\right)\right). \tag{22}$$

Using the aforementioned similar method as in $[t_2, t_3]$, the value L_2 of inductance and C_2 of capacitance in the stage of $[t_3, t_1]$ could be derived and expressed as follows:

$$L_2 = \left\{ \int_{\frac{\pi}{3}}^{\omega t_1} (e_v - e_w + U_o) d\omega t - \int_{\frac{\pi}{3}}^{\omega t_1} \frac{3\left[1+\cos\left(\omega t + \frac{2\pi}{3}\right)\right]}{\sin\omega t_1 + \sin\left(\omega t + \frac{2\pi}{3}\right) - \frac{\sqrt{3}}{2}} \cdot \left[U_m \left(\frac{1}{2} - \cos\left(\omega t_1 - \frac{2\pi}{3}\right)\right) + \frac{U_o}{3}\left(\omega t_1 - \frac{\pi}{3}\right)\right] d\omega t \right\} / \left\{ I_m \omega \left[\sin\left(\omega t_1 - \frac{2\pi}{3}\right) - \sin\left(\omega t_1 + \frac{2\pi}{3}\right) + \frac{\sqrt{3}}{2}\right] - \int_{\frac{\pi}{3}}^{\omega t_1} \frac{3 I_m \omega \left[1+\cos\left(\omega t + \frac{2\pi}{3}\right)\right]}{\sin\omega t_1 + \sin\left(\omega t + \frac{2\pi}{3}\right) - \frac{\sqrt{3}}{2}} \cdot \left[\sin\left(\omega t_1 - \frac{2\pi}{3}\right) + \frac{\sqrt{3}}{2}\right] d\omega t \right\}$$

$$= 28.32 \text{ mH} \quad (23)$$

$$C_2 = \frac{\int_{\frac{\pi}{3}}^{\omega t_1} I_m \left[1+\cos\left(\omega t + \frac{2\pi}{3}\right)\right] d\omega t}{3\omega \left[\int_{\frac{\pi}{3}}^{\omega t_1} \left(\frac{2U_o}{3} + e_v\right) d\omega t + I_m L_1 \omega \sin\left(\omega t_1 - \frac{2\pi}{3}\right)\right]}$$

$$= 94.8\ \mu\text{F}. \quad (24)$$

3) Optimal Value: Finally, the conclusive optimal values of inductance and capacitance are derived by using the time-weighted averaging method as follows:

$$L = \frac{L_1\left(\frac{2\pi}{3} - \omega t_1\right) + L_2\left(\omega t_1 - \frac{\pi}{3}\right)}{\frac{\pi}{3}} = 27.7 \text{ mH} \quad (25)$$

$$C = \frac{C_1\left(\frac{2\pi}{3} - \omega t_1\right) + C_2\left(\omega t_1 - \frac{\pi}{3}\right)}{\frac{\pi}{3}} = 98.6\ \mu\text{F}. \quad (26)$$

D. Graphical Description

Fig. 8 shows the variation of optimal capacitance value C as a function of input voltage U_m. The values of P_o and U_o are adopted as 300 and 500 V, respectively. Three RNSIC converters have similar characteristic of optimal capacitance value: It will decrease as the input voltage increases, while it will increase as the output power increases. The optimal capacitance value of RNSIC-3 is largest and nearly twice as that of RNSIC-1, while the value of RNSIC-2 is smallest.

Fig. 9 shows the variation of optimal inductance value L as a function of input voltage U_m and output power P_o. The values of U_o are adopted as 500 V, and the values of P_o are adopted as 300 and 1 000 W, respectively. From this diagram, we could find that three RNSIC converters have similar values and trend of optimal inductances: First, as U_m increases from the lower value to the higher one, L will increase, but it will decrease again after RNSIC rectifiers enter into large-current mode; second, as P_o increases, the optimal inductance will decrease.

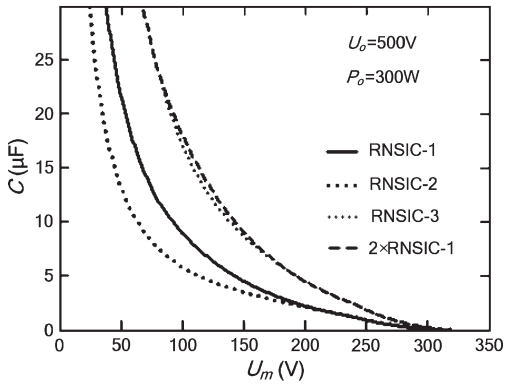

Fig. 8. Variations of C as a function of U_m in RNSIC converters.

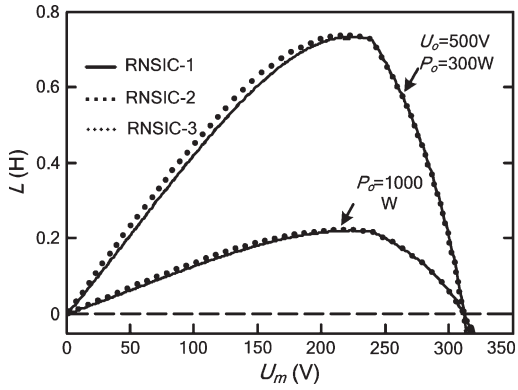

Fig. 9. Variations of L as a function of U_m in RNSIC converters.

TABLE III
SPECIFICATIONS OF FIVE SIMULATION EXAMPLES

Example	U_m	U_o/V	P_o/ kW	L/mH	C/μF
1	311V / 50Hz	600	100	2.6	167
2	311V / 50Hz	475	150	2.6	167
3	311V / 50Hz	668	150	2.6	385
4	Phase *u*: 350V / 50Hz Phase *v* & *w*: 311V / 50Hz	600	100	2.6	167
5	311V / 50Hz +50V / 150Hz	600	100	2.6	167

V. Simulation Results and Discussion

All the aforementioned results are drawn under ideal operation condition, and simulation results of RNSIC-1 under load variation, mains voltage imbalance, and mains voltage distortion are given in this section. The detailed specifications of these simulation examples are given in Table III.

A. Load Variation

The simulation waveforms of examples 1, 2, and 3 are shown in Fig. 10(a), from which we could find that

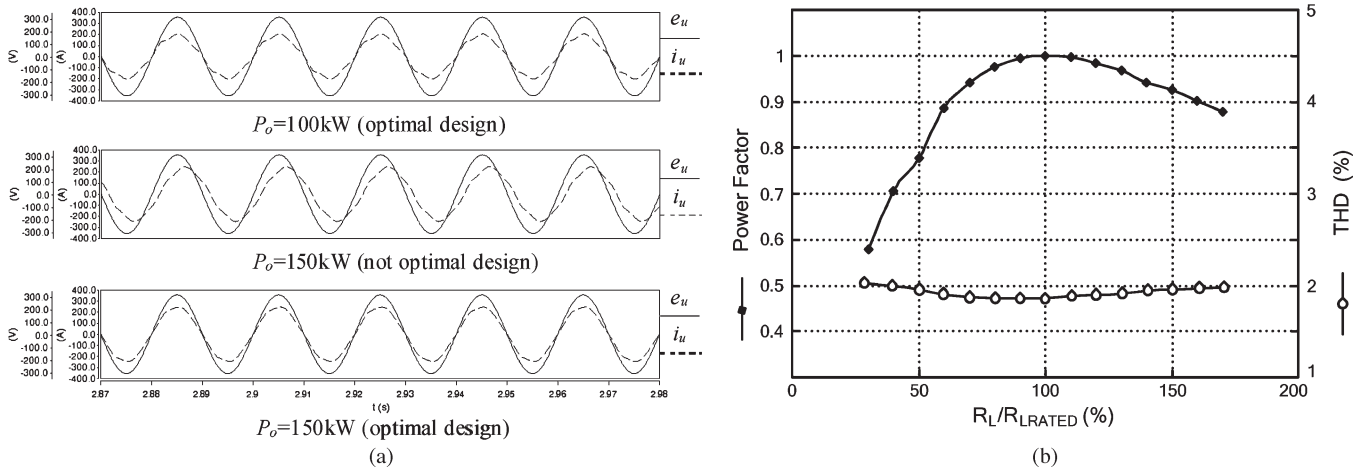

Fig. 10. Simulation waveforms under load variation. (a) Mains voltage and input current. (b) Power factor and input-current THD.

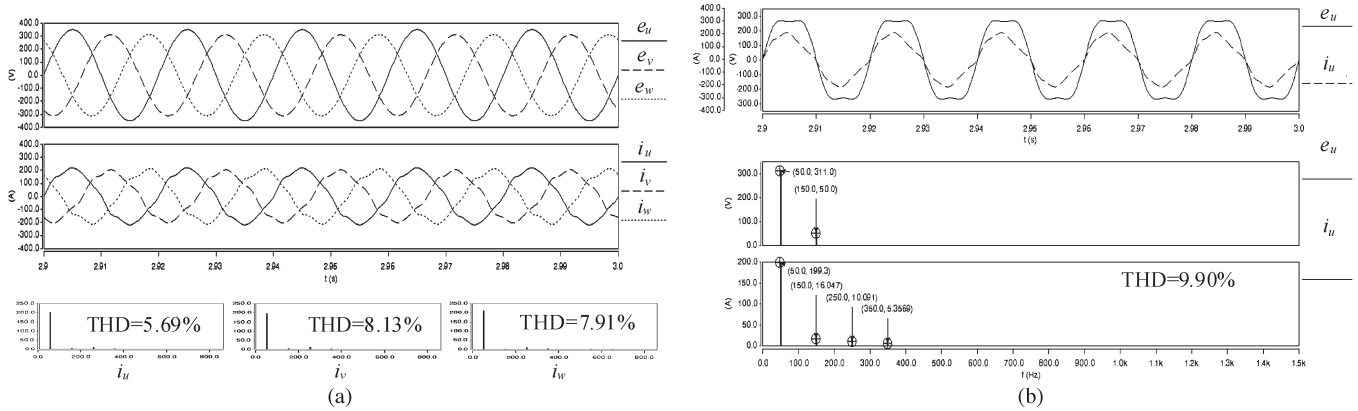

Fig. 11. Simulation waveforms under nonideal mains voltage. (a) Mains voltage imbalance. (b) Mains voltage distortion.

near-sinusoidal input currents are drawn from the mains. When the output power increases from 100 (example 1) to 150 kW, a visible phase displacement exists between voltage and current without any change of the passive components (example 2), but it will disappear after optimal selection of capacitances (example 3).

More simulation results under load variation condition are shown in Fig. 10(b). Load resistors are selected from 0.3 to 1.7 of the normalized value. From this diagram, we can draw the following conclusions: First, the input-current total harmonic distortion (THD) is influenced by the load resistor slightly, all below 3%; second, the input power factor is strongly influenced by the load resistor. When the converter deviates the operation point, the power factor will decrease drastically.

B. Mains Voltage Imbalance and Distortion

Fig. 11(a) shows the simulation waveforms of example 4, in which the mains voltage is imbalanced. Although THDs in distinctive phases are different, they all keep in a low level.

When a third-order (150-Hz) voltage harmonic corresponding to 50 V appears in the mains voltage, the THDs of the input currents under distorted voltage are 9.90% from Fig. 11(b) showing the simulation waveforms of example 5.

TABLE IV
SPECIFICATIONS OF SEVEN RNSIC PROTOTYPES

Prototype	U_m /V	U_o / V	P_o / kW	L / mH	C / μF
1	250	500	7.18	27.7	22.46
2	150	500	6.55	27.7	98.7
3	55	500	2.52	27.7	159.2
4	250	500	4.79	41.5	14.92
5	250	515	7.95	27.7	27.7
6	250	500	7.18	27.7	22.46
7	250	500	7.18	27.7	44.88

VI. EXPERIMENTAL VERIFICATION

In order to verify the feasibility of the analysis derived earlier and the validity of the proposed design method, seven RNSIC prototypes are built in the laboratory. The detailed specifications are given in Table IV. The topologies of prototypes 1–5 are RNSIC-1, while the topologies of prototypes 6 and 7 are RNSIC-2 and RNSIC-3, respectively. Prototypes 1, 4, 6, and 7 all work in large-current mode, with the same design value of ωt_1 corresponding to 0.307π. Prototypes 2 and 3 work in medium- and small-current modes, with the same design value of ωt_1 corresponding to 0.518π and 0.741π, respectively.

Fig. 12(a)–(g) shows the experimental waveforms of i_u and e_u in seven prototypes. The input currents are nearly sinusoidal, and the displacement factors are all near unity. From the input-current spectrum of prototype 1 (as Fig. 12(h) shows), the

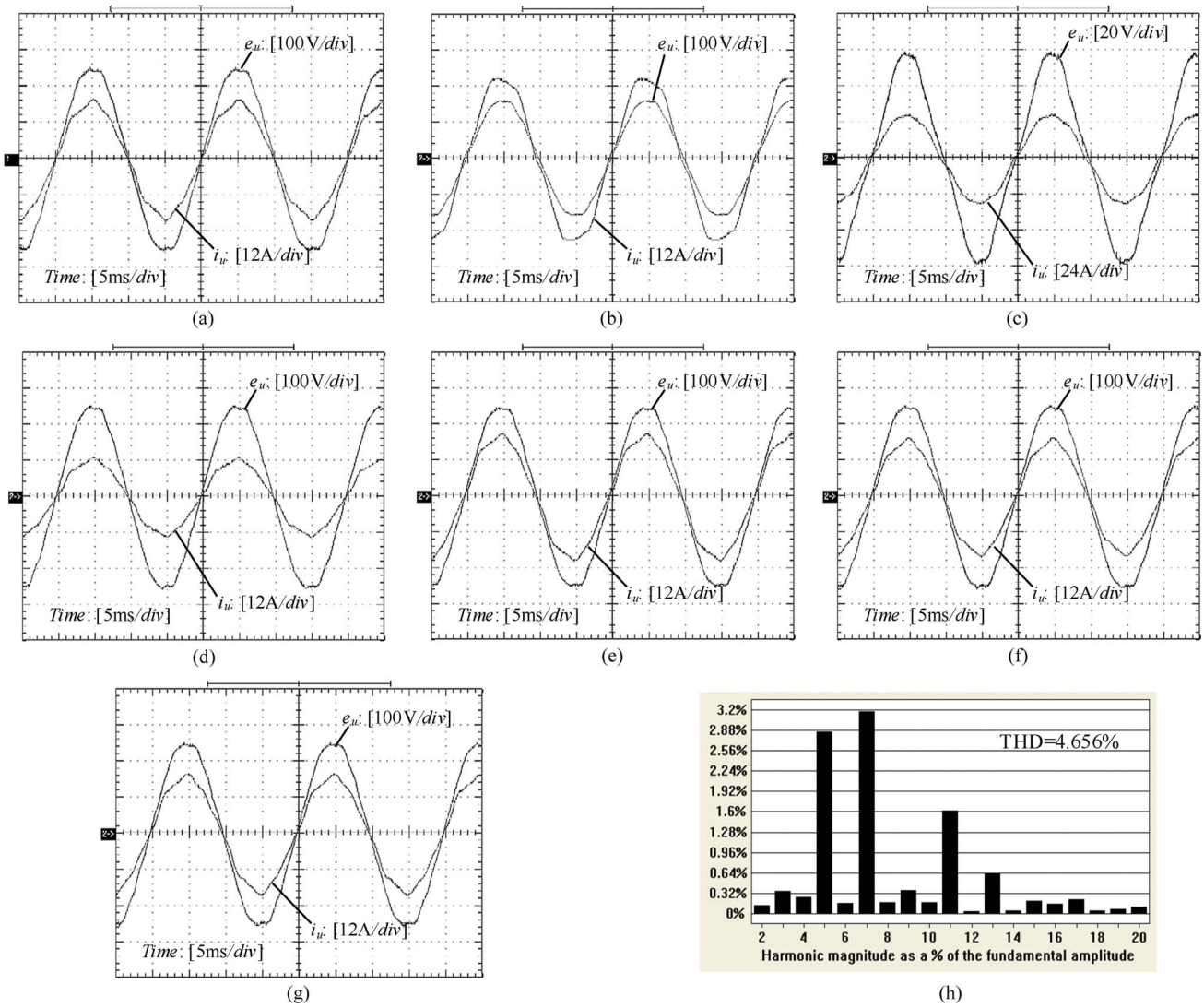

Fig. 12. Experimental waveforms of RNSIC prototypes. (a) Prototype 1. (b) Prototype 2. (c) Prototype 3. (d) Prototype 4. (e) Prototype 5. (f) Prototype 6. (g) Prototype 7. (h) Input-current spectrum of the prototype.

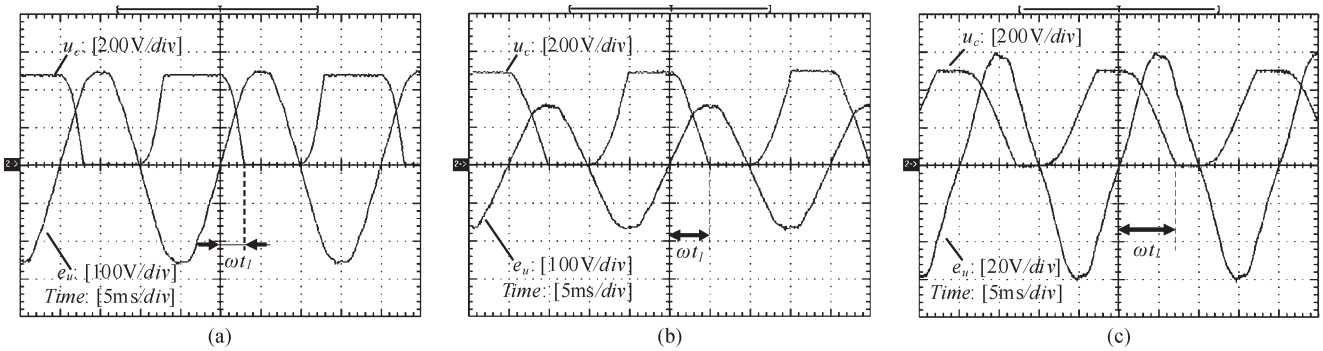

Fig. 13. Experimental waveforms of u_c in RNSIC prototypes. (a) Prototype 1. (b) Prototype 2. (c) Prototype 3.

THD of the input currents is 4.656%, and the THDs of other prototypes are all below 6%, which are not shown in Fig. 12. Additionally, the input power factors of the seven prototypes are all higher than 0.99.

From the comparison between prototypes 1 and 4, good mains behavior (as Fig. 12(d) shows) could be achieved by increasing the inductance from 27.7 to 41.5 mH and reducing the capacitance from 22.46 to 14.92 μF, when the output power decreases from 7.18 to 4.79 kW. From the comparison between prototypes 1 and 5, good mains behavior in a load variation condition could also be obtained by changing only the capacitors at the expense of output-voltage fluctuation.

Fig. 13 shows the experimental waveform of u_c voltage on the commutation capacitors in prototypes 1, 2, and 3. In

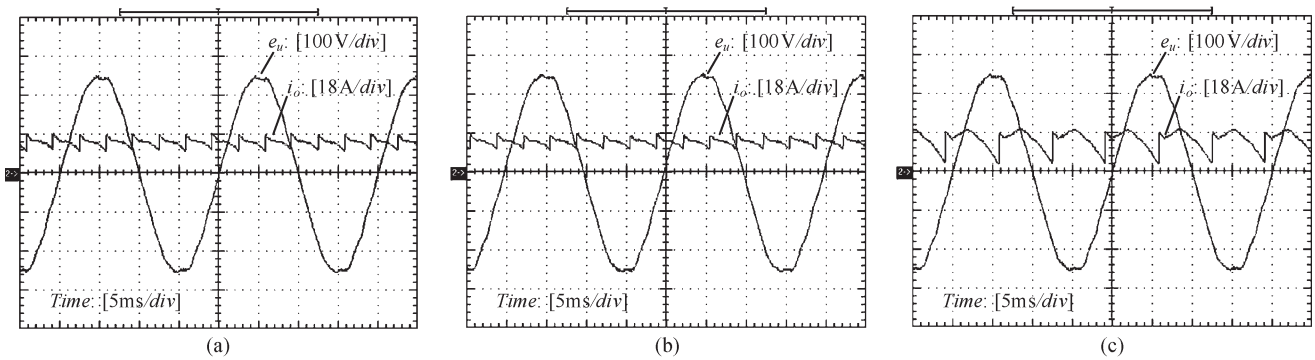

Fig. 14. Experimental waveforms of i_o in RNSIC prototypes. (a) Prototype 1. (b) Prototype 6. (c) Prototype 7.

RNSIC-1, the commutation capacitors start charging or discharging when the input current (phase voltage in Fig. 13) crosses zero. The observed values of ωt_1 in the three prototypes are about 0.3π, 0.5π, and 0.7π, coinciding well with the design values.

Fig. 14 shows the experimental waveform of dc-link current i_o in prototypes 1, 6, and 7; it is the same 12-pulse waveform in RNSIC-1 and RNSIC-2, but it is a six-pulse waveform with large ripple in RNSIC-3, agreeing well with the previous analysis. Note that, although the input inductors have the same value in prototypes 1, 6, and 7, the value of commutation capacitors in RNSIC-3 is twice as that of the other two RNSIC converters, as Table IV demonstrates.

VII. Conclusion

A family of low-harmonic-input three-phase rectifiers with passive LC auxiliary circuit has comparatively been studied. A design method optimized at the operating point, including the selection of auxiliary circuit and the determination of passive components, has been proposed. Both simulation and experimental results show that this family of rectifiers with simple fabrication could effectively suppress the input-current harmonics.

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