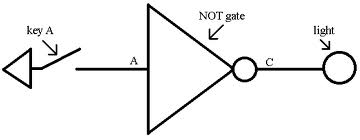
* Not Gate  
  
* AND Gate
* OR Gate
* XOR Gate

|  |  |  |
| --- | --- | --- |
| * A | * B | * X |
| * 0 | * 0 | * 0 |
| * 0 | * 1 | * 1 |
| * 1 | * 0 | * 1 |
| * 1 | * 1 | * 0 |

* + XOR is called Exclusive OR
* NAND Gate

|  |  |  |
| --- | --- | --- |
| * + A | * + B | * + X |
| * + 0 | * + 0 | * + 1 |
| * + 0 | * + 1 | * + 1 |
| * + 1 | * + 0 | * + 1 |
| * + 1 | * + 1 | * + 0 |

* + X = (A \* B) '
* NOR Gate

|  |  |  |
| --- | --- | --- |
| * + A | * + B | * + X |
| * + 0 | * + 0 | * + 1 |
| * + 0 | * + 1 | * + 0 |
| * + 1 | * + 0 | * + 0 |
| * + 1 | * + 1 | * + 0 |

* + Expression: X = (A + B)'
* Review of Gate Processing
  + NOT gate inverts its signal input
  + AND gate produces 1 if both input values are 1
  + OR gate produces 0 if both input values are 0
  + XOR gate produces 0 if input values are the same
  + NAND gate produces 0 if both inputs are 1
  + NOR gate produces a 1 if both inputs are 0
* Example
  + if NOT ((A>B) AND (C =D ) OR (G F))
* Gates and be designed to take three or more inputs

|  |  |  |  |
| --- | --- | --- | --- |
| * + A | * + B | * + C | * + X |
| * + 0 | * + 0 | * + 0 | * + 0 |
| * + 0 | * + 0 | * + 1 | * + 0 |
| * + 0 | * + 1 | * + 0 | * + 0 |
| * + 0 | * + 1 | * + 1 | * + 0 |
| * + 1 | * + 0 | * + 0 | * + 0 |
| * + 1 | * + 0 | * + 1 | * + 0 |
| * + 1 | * + 1 | * + 0 | * + 0 |
| * + 1 | * + 1 | * + 1 | * + 1 |

* Transistor
  + a device that acts either as a wire that conducts electricity or as a resistor that blocks the flow of electricity, depending on the voltage level of an input signal
  + Has no moving parts, yet acts like switch
  + Made of a semiconductor material, which is neither a particularly good conductor of electricity nor a particularly good insulator
  + Started use in generation 2
  + Terminals
    - source
    - Base
    - Ground (emitter)
  + Easiest gates to create are the NOT, NAND, and NOR gates
* Combinational circuit
  + Input values explicitly determine the output
* Sequential circuit
  + The output is a function of the input values and the existing state of the circuit
* Example

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| * + A | * + B | * + C | * + D | * + e | * + x |
| * + 1 | * + 0 | * + 1 | * + 1 | * + 0 | * + 1 |
| * + 0 | * + 1 | * + 1 | * + 0 | * + 0 | * + 0 |
|  |  |  |  |  |  |