**Flashcards Answers:**

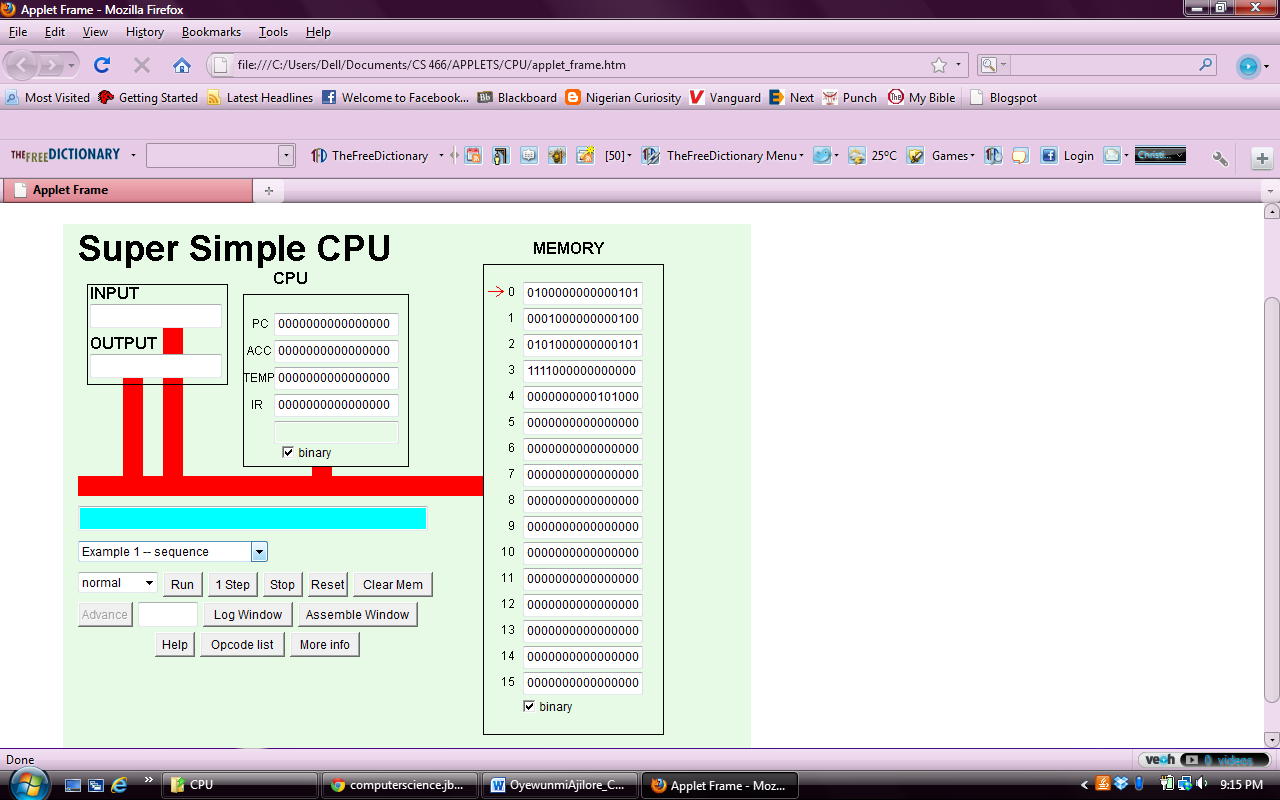
1. Addressability
2. Seek time
3. Block
4. Cylinder
5. Control Unit
6. Sector
7. Track
8. Auxiliary storage device
9. Shared memory
10. Instruction register
11. Access time
12. Input unit
13. Transfer rate
14. Input/output devices
15. Input
16. Motherboard
17. Synchronous processing
18. Latency
19. Allocate
20. Bus
21. Fetch-execute cycle
22. Arithmetic/logic unit
23. Output unit
24. Pipelining processing
25. CPU
26. Program Counter
27. Register

**Exercises Answers:**

1. B
2. A
3. C
4. D
5. H
6. G
7. E
8. F
9. G
10. G
11. E
12. D
13. A
14. I
15. E
16. I
17. F
18. B
19. C
20. E
21. B
22. G
23. D
24. It means that memory is pulsing 133million times per second.
25. A. 536 870 912 B. 2 147 483 648
26. RPM helps determine the access time on computer hard disk drives which is the measurement of how many complete revolutions a computer’s hard disk drive makes in a single minute. The higher the RPM, the faster data will be accessed.
27. It’s a principle on the realization that data and instructions to manipulate the data were logically the same and could be stored in the same place.
28. It entails the stored-program principle.
29. Control Unity, Arithmetic/logic unit, Memory Unit, Input/output Unit, the Bus
30. 8-bit
31. It performs arithmetic operations and logical operations.
32. Control Unit
33. Paper tapes could not hold much data and to access data in the middle of the tape, all the data before the piece you want must be accessed and discarded.
34. The register that contains the Instruction currently being executed
35. The register that contains the address of the next instruction to be executed
36. Fetch next instruction, decode instruction, get data if needed, execute instruction
37. The next instruction is fetched from the memory address that is currently stored in the Program Counter, and stored in the Instruction register. At the end of the fetch operation, the PC points to the next instruction that will be read at the next cycle.
38. The decoder interprets the instruction. During this cycle the instruction inside the IR (instruction register) gets decoded.
39. The CU passes the decoded information as a sequence of control signals to the relevant function units of the CPU to perform the actions required by the instruction such as reading values from registers, passing them to the ALU to perform mathematical or logic functions on them, and writing the result back to a register. If the ALU is involved, it sends a condition signal back to the CU. The result generated by the operation is stored in the main memory, or sent to an output device. Based on the condition of any feedback from the ALU, Program Counter may be updated to a different address from which the next instruction will be fetched.
40. Both the RAM and ROM are memory units in the CPU. The ROM is a memory in which each location can be accessed but not changed, making it not volatile; while, the RAM is memory in which each location can be accessed and changed, making it volatile.

**Lab Answers:**

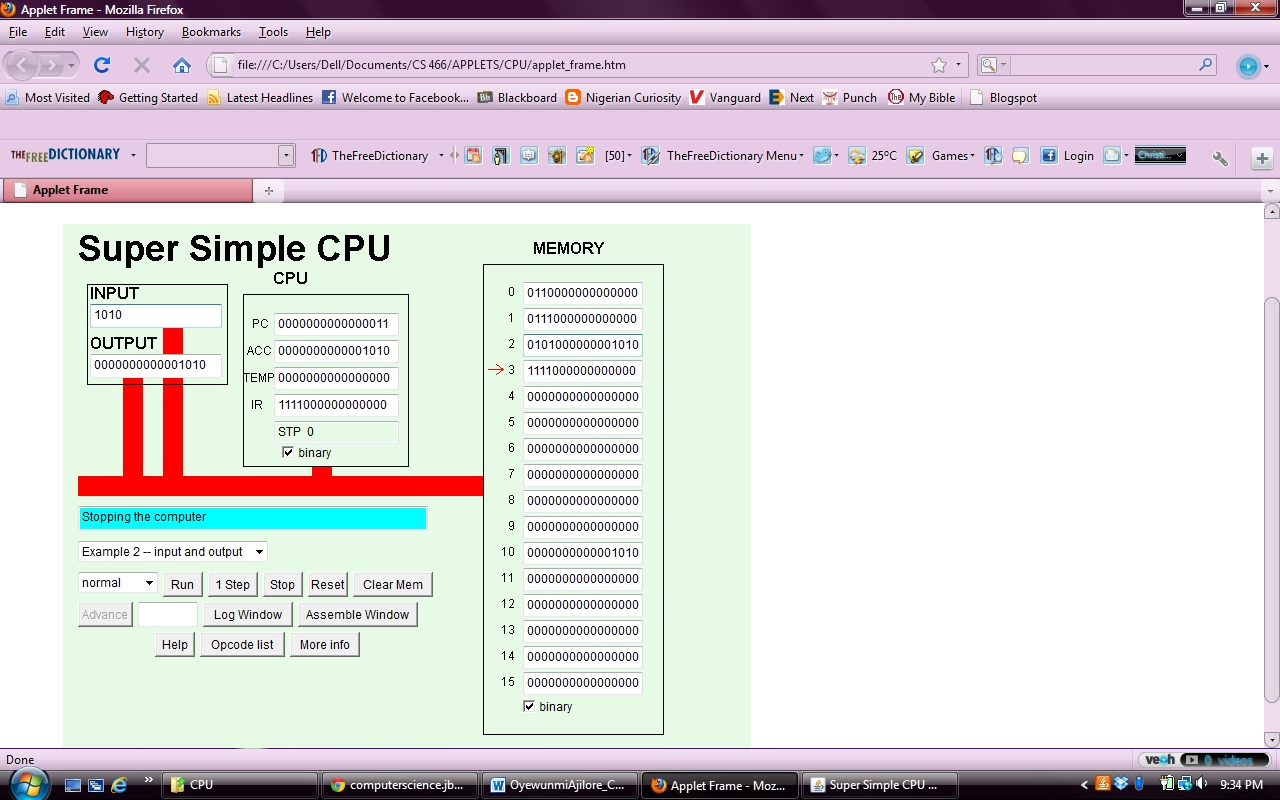
*Exercise 1*



Mnemonics: LDI, ADD, STO, STP

It runs 4 Fetch-Execute cycles.

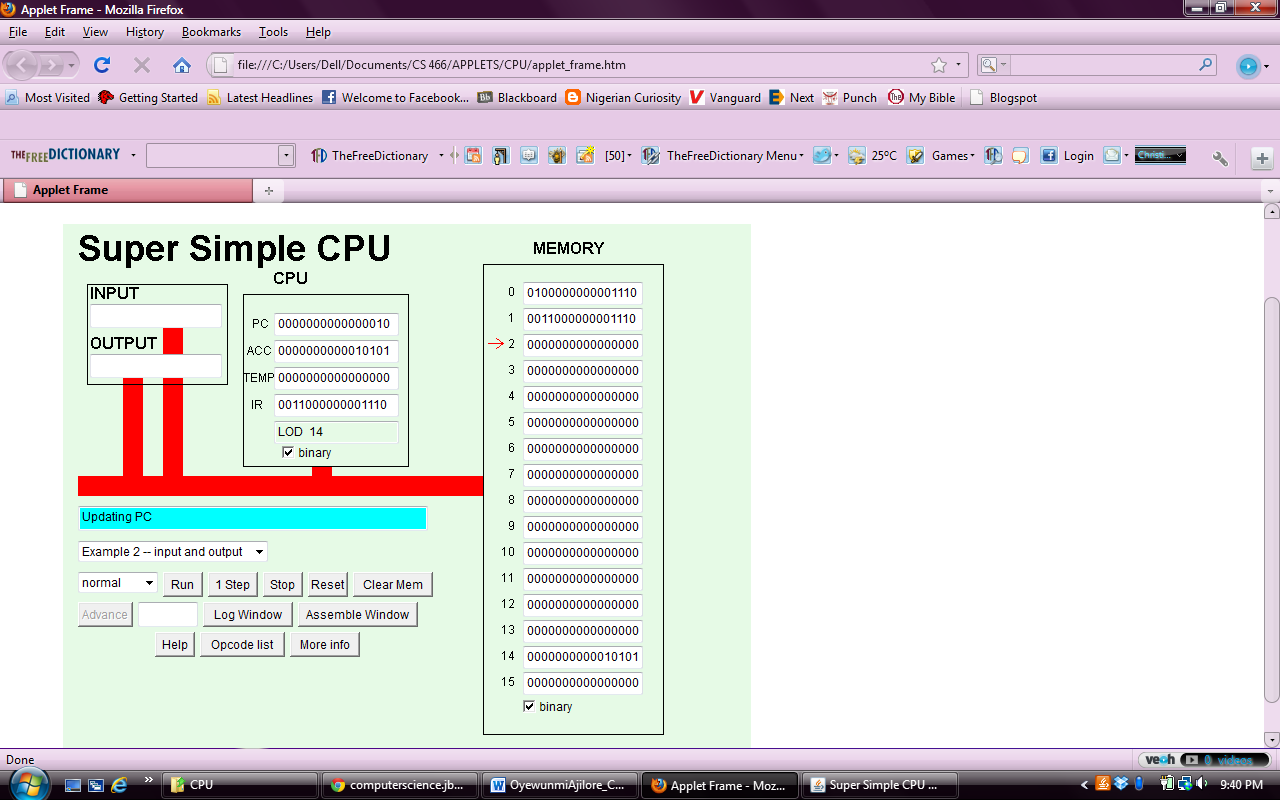
*Exercise 2*



*Exercise 3*

0011 LOD

0101 STO



LOD –loads memory cell into accumulator ie, fetch number from memory and store it in accumulator replacing old value

STO –stores the accumulators value in memory at the indicated location

7. By specifying the specific cell you want it to be stored in.