

ECE429-L02

**Final Project: *Case Study for 32-bit
Pipelined CPU design with New ALU
Architecture***

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Introduction:

The objective of the final project for ECE429 is to understand 32-bit Pipelined Central Processing Unit (CPU). Pipelined means that the circuit can handle more than one 32-bit word at a time. We will use the techniques from the past 9 labs and the introduced software to implement the circuit design. This requires revisiting past labs.

The lab is broken into two Case Studies. In Case Study-1 we investigate different types of adders in our CPU and examine the path delay associated with each adder over a variety of operations. In Case Study-2 we redesign the Arithmetic Logic unit (ALU) as a 32-bit comparator.

Pre-Lab/Theory:

Our designed CPU consists of a 32x32 Memory File, Arithmetic Logic Unit (ALU) and several 2-1 MUXes along with the inputs and various encoders. The below block diagram from the lab manual shows the relationships between the signals and components in the lab.

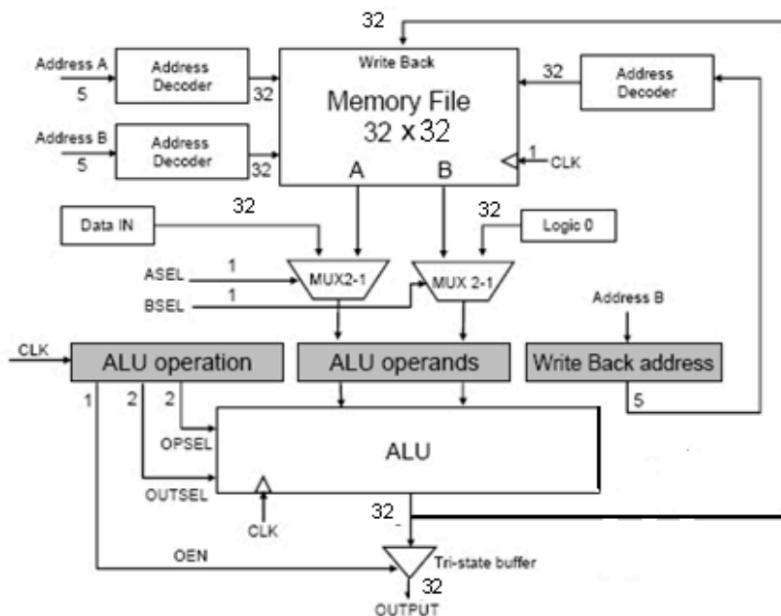


Figure 1. Overview of the primary blocks and signals

The memory file can store 32 32-bit words. At each clock cycle, the memory reads from a 5-bit address. Operations performed by the ALU include arithmetic and logic operations. All operations are synched with an external clock.

Implementation:

Case Study 1 32-bit CPU design with Different Adders:

In the first case study we follow the standard cell based flow for different adders implemented in our CPU. We explore the Carry Ripple Adder, Carry Look-ahead Adder, Carry Skip Adder, and the Carry Select Adder. The source code for each of the adders along with the test bench is provided and we simply need to perform an RTL simulation, Logic synthesis and Post Synthesis Simulation and Place and Route and Post P&R Simulation for each of the different possible CPU configurations.

First we need to detect any bugs in the adder design by running the test bench. Each of the adders is already integrated into the CPU design in the Verilog source file. The generated warning is the result of missing ".over(over)" placeholders as predefined by the function but these are unnecessary. The test bench file validates the store, read, addition and subtraction functionality of each of the CPU configurations.

After validation we follow IIT-ECE429 ASIC flow for the logical and physical synthesis. For the logical synthesis we use Synopsis DC with a desired clock frequency of 30 MHZ.

Finally for case study 1 we perform a Place & Route and Post-P&R Simulation using Cadence SOC Encounter. The layout is automatically generated and we can check the timing report. We modify the test bench to build in some custom operations detailed in the chart above and in the code snippets below.

		CRA (ns)	CLA (ns)	CSA (ns)	CSeA (ns)
Calculate the Path Delay For Each Operation (Post-Synthesis Gate-Level Delay)	5555_5555 + 5	4.9	4.49	3.94	4.06
	AAA_AAA + 555_555	5.2	4.55	4.05	4.07
	0000_00C8 + 0000_012C	5	4.5	3.99	4.06
	5 + 0000_0001	4.9	4.49	3.95	4.06
	FFFF_FFFF - 0000_0001	5.1	4.53	4.01	4.07
	FFFF_FFFF + 0000_012C	5.1	4.53	4.01	4.06
	5555_5555 - 5	4.9	4.49	3.95	4.06
	AAAA_AAAB + 5555_5555	5.2	4.55	4.06	4.08

```
// ADD [1][2]
addressA = 5'd1;
addressB = 5'd2;
dataIn = 32'd0;
opsel = 2'b00;
outsel = 3'b001;
asel = 1;
bsel = 1;
oen = 1;

// STORE AAAA_AAAB in [9]
addressA = 5'b00000;
addressB = 5'b01001;
dataIn = 32'hAAAA_AAAB;
opsel = 2'b01;
outsel = 3'b000;
asel = 0;
bsel = 0;
oen = 1;
```

The Path delay measurements, if correct, make sense. As the operations get more intensive the delay time grows. For example adding numbers requires less than adding letters. The reason for which the adders rank in terms of delay is unclear but they are all relatively close.

Case Study-2: 32-bit CPU design with New ALU Architecture:

In the second case study we are designing the structure of an alternative ALU. Similar to the first case study we are provided with the template source file. First we must write the Verilog code structure for 32 one_bit_comp, 16 mux_4to2, 8 mux_4to2, 4 mux_4to2, 2 mux_4to2, and 1 mux_4to2. After completing the Verilog file we need to write a test bench for the specified operations.

Again similar to Case Study-1 we run the RTL simulation and validate the output. Next we follow the steps of logical and physical synthesis. Again we run a post-synthesis simulation and explore the timing delays

Conclusion:

The final project walked through two different experiments modifying the computer architecture of a 32-bit CPU. First we modified the type of adder used in the CPU switching between four different adders. Next we changed the ALU Verilog file to support a 32-bit design. The project was the culmination of semesters worth of training in VLSI simulation tools and provided a challenging final task.

Appendix:

Because of the abundance of screenshots I will outline the organization here:

Screenshot Outline

- 1. Case Study 1**
 - a. Cpu_CSA related
 - b. Cpu_CRA related
 - c. Cpu_CLA related
 - d. Cpu_CReA related
- 2. Case Study 2**
 - a. RTL Simulation and simvision
 - b. Cell.rep
 - c. Timing.rep
 - d. Post-synthesis simulation
 - e. Simvision
 - f. Timing.rep.5.final
 - g. Post P&R simulation

Case Study 1 by adder design:

CSA:

taikvecadence.com

```
Compiling source file "tb_cpu.v"
Compiling source file "cpu_CSA.v"

Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 598: cs0_15(.s(s[15:0]), .cout(c), .
    a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
    .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
    .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

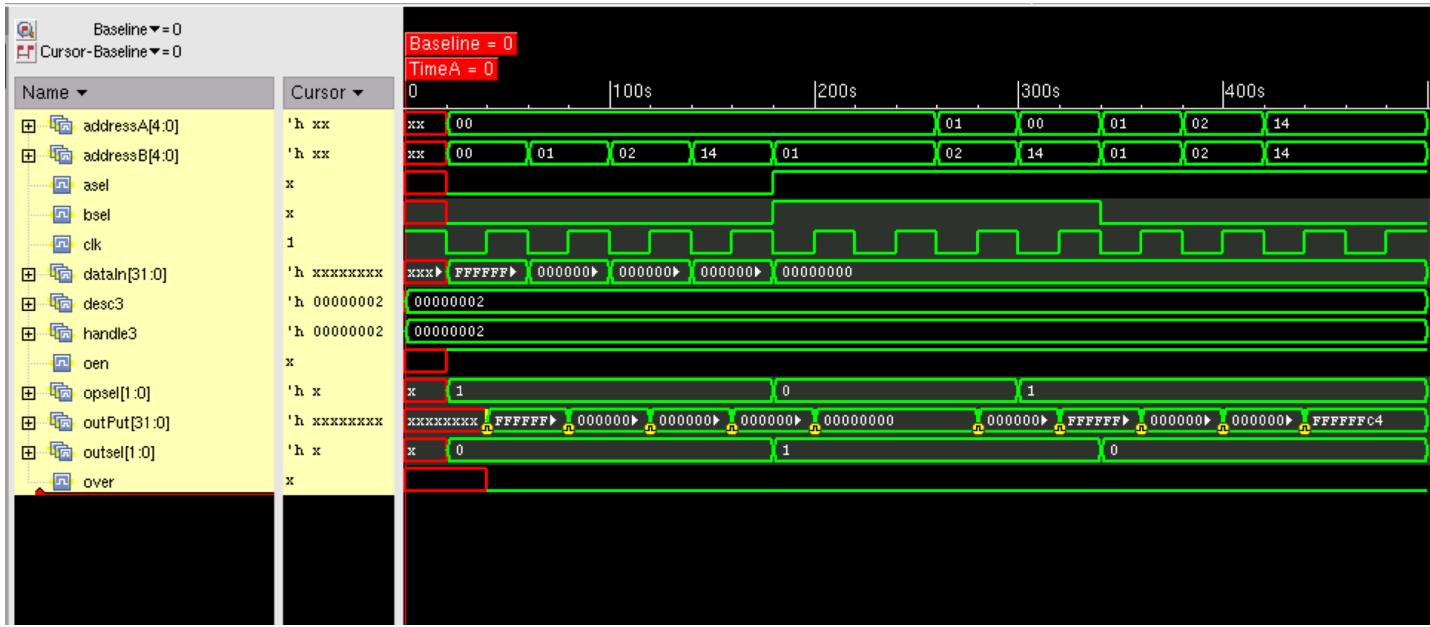
Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2])
    , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))

Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
    .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
    .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

Warning! Too few module port connections [Verilog-TFNPC]
  "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2])
    , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))
Highest level modules:
stimulus

L30 "tb_cpu.v"; $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 21065 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
End of Tool:  VERILOG-XL      08.20.001-p   Dec 6, 2018 19:33:50
avannopp@saturn.ece.iit.edu:"% █
```



compile_dc.tcl x cpu_CSA.v x cell.rep x timing.rep x

o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n	
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n	
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n	
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n	
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n	
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n	
Total 14479 cells			48878.063377		
1					

a/l3/f265/u2/y (XOR2X1)	0.07	0.04	r
a/l3/f274/u5/y (XNOR2X1)	0.06	6.11	r
a/l3/f274/u2/y (XOR2X1)	0.07	6.18	r
a/l3/f283/u5/y (XNOR2X1)	0.06	6.24	r
a/l3/f283/u2/y (XOR2X1)	0.07	6.31	r
a/l3/f292/u5/y (XNOR2X1)	0.06	6.37	r
a/l3/f292/u2/y (XOR2X1)	0.07	6.44	r
a/l3/h301/u2/y (XOR2X1)	0.04	6.48	f
a/U26/Y (AOI22X1)	0.03	6.52	r
U222/Y (BUFX2)	0.04	6.56	r
U67/Y (AND2X1)	0.07	6.62	r
U1832/Y (INVX1)	0.10	6.73	f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78	r
U3835/Y (INVX1)	0.02	6.80	f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80	f
data arrival time		6.80	
clock clk (rise edge)	33.00	33.00	
clock network delay (ideal)	0.00	33.00	
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00	r
library setup time	-0.06	32.94	
data required time		32.94	

data required time		32.94	
data arrival time		-6.80	

slack (MET)		26.14	

# Generated by:	Cadence Encounter 10.13-s292_1		
# OS:	Linux x86_64(Host ID saturn.ece.iit.edu)		
# Generated on:	Thu Dec 6 22:38:33 2018		
# Design:	cpu		
# Command:	report_timing -nworst 10 -net > timing.rep.5.final		
#####	#####	#####	#####
Path 1: MET Setup Check with Pin mb/ram/mer11/ll/me31/qout_reg/CLK			
Endpoint: mb/ram/mer11/ll/me31/qout_reg/D (^) checked with leading edge of			
'clk'			
Beginpoint: m0pd/bb/me1/qout_reg/Q	(v) triggered by	leading edge of	
'clk'			
Other End Arrival Time	0.309		
- Setup	3.945		
+ Phase Shift	33.000		
= Required Time	29.364		
- Arrival Time	11.046		
= Slack Time	18.318		
Clock Rise Edge	0.000		
+ Clock Network Latency (Prop)	0.309		
= Beginpoint Arrival Time	0.309		

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 6 23:20:50 2018

Design Name: cpu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (352.8525, 352.0800)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 23:20:51 **** Processed 5000 nets (Total 12514)
**** 23:20:51 **** Processed 10000 nets (Total 12514)
Time Elapsed: 0:00:02.0

Begin Summary
    Found no problems or warnings.
End Summary

End Time: Thu Dec 6 23:20:52 2018
***** End: VERIFY CONNECTIVITY *****
    Verification Complete : 0 Viols, 0 Wrngs,
    (CPU Time: 0:00:01.7 MEM: 0.500M)

*****
* Encounter script finished *
* *
* Results: *
* ----- *
* Layout: final.gds2 *
* Netlist: final.v *
* Timing: timing.rep.5.final *
* *
* Type 'win' to get the Main Window *
* or type 'exit' to quit *
* *
*****encounter 1>
```

```
Compiling source file "tb_test.v"
Compiling source file "cpu_CSA.v"

Warning! Port sizes differ in port connection (port 7)      [Verilog-PCDPC]
          "tb_test.v", 18: outsel

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 598: cs0_15(.s(s[15:0]), .cout(c), .
          a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
          .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
          .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2]),
          .a(a[11:8]), .b(b[11:8]), .cin(c[1]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
          .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
          .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2]),
          .a(a[11:8]), .b(b[11:8]), .cin(c[1]))
Highest level modules:
stimulus3

L34 "tb_test.v": $finish at simulation time 1501
8 warnings
0 simulation events (use +profile or +listcounts option to count) + 97306 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 1.3 secs in simulation
End of Tool:    VERILOG-XL    08.20.001-p   Dec  7, 2018  00:38:05
avannopp@saturn.ece.iit.edu:"%
```



CRA:

```

For more information on Cadence's Verilog-XL product line send email to
talkv@cadence.com

Compiling source file "tb_cpu.v"
Compiling source file "cpu_CRA.v"

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CRA.v", 557: cra0(.sum(sum[7:0]), .c_out(c7)
, .a(a[7:0]), .b(b[7:0]), .c_in(c_in))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CRA.v", 558: cra1(.sum(sum[15:8]), .c_out(
c15), .a(a[15:8]), .b(b[15:8]), .c_in(c7))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CRA.v", 559: cra2(.sum(sum[23:16]), .c_out(
c23), .a(a[23:16]), .b(b[23:16]), .c_in(c15))

Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
3 warnings
0 simulation events (use +profile or +listcounts option to count) + 21024 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
End of Tool:    VERILOG-XL      08.20.001-p   Dec  6, 2018 19:32:33
avannapp@saturn.ece.iit.edu:"% "

```



	cell.rep	timing.rep		
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14390 cells			48610.093084	
1				

a/l3/f274/U5/Y (XOR2X1)	0.06	6.11	r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18	r
a/l3/f283/U5/Y (XOR2X1)	0.06	6.24	r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31	r
a/l3/f292/U5/Y (XOR2X1)	0.06	6.37	r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44	r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48	f
a/U26/Y (AOI22X1)	0.03	6.52	r
U220/Y (BUFX2)	0.04	6.56	r
U65/Y (AND2X1)	0.07	6.62	r
U1794/Y (INVX1)	0.10	6.73	f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78	r
U3794/Y (INVX1)	0.02	6.80	f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80	f
data arrival time		6.80	
 clock clk (rise edge)	33.00	33.00	
clock network delay (ideal)	0.00	33.00	
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00	r
library setup time	-0.06	32.94	
data required time		32.94	
 data required time	32.94		
data arrival time	-6.80		
 slack (MET)	26.14		

1

<hr/>			
# Generated by:	Cadence Encounter 10.13-s292_1		
# OS:	Linux x86_64(Host ID saturn.ece.iit.edu)		
# Generated on:	Thu Dec 6 23:48:21 2018		
# Design:	cpu		
# Command:	report_timing -nworst 10 -net > timing.rep.5.final		
<hr/>			
Path 1: MET Setup Check with Pin mb/ram/mer15/ll/me30/qout_reg/CLK			
Endpoint: mb/ram/mer15/ll/me30/qout_reg/D (^) checked with leading edge of			
'clk'			
Beginpoint: m0pd/bb/me2/qout_reg/Q	(v) triggered by	leading edge of	
'clk'			
Other End Arrival Time	0.352		
- Setup	4.953		
+ Phase Shift	33.000		
= Required Time	28.398		
- Arrival Time	10.940		
= Slack Time	17.458		
Clock Rise Edge	0.000		
+ Clock Network Latency (Prop)	0.363		
= Beginpoint Arrival Time	0.363		
 +			

```

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:04.7 MEM: 48.7M)

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 6 23:59:35 2018

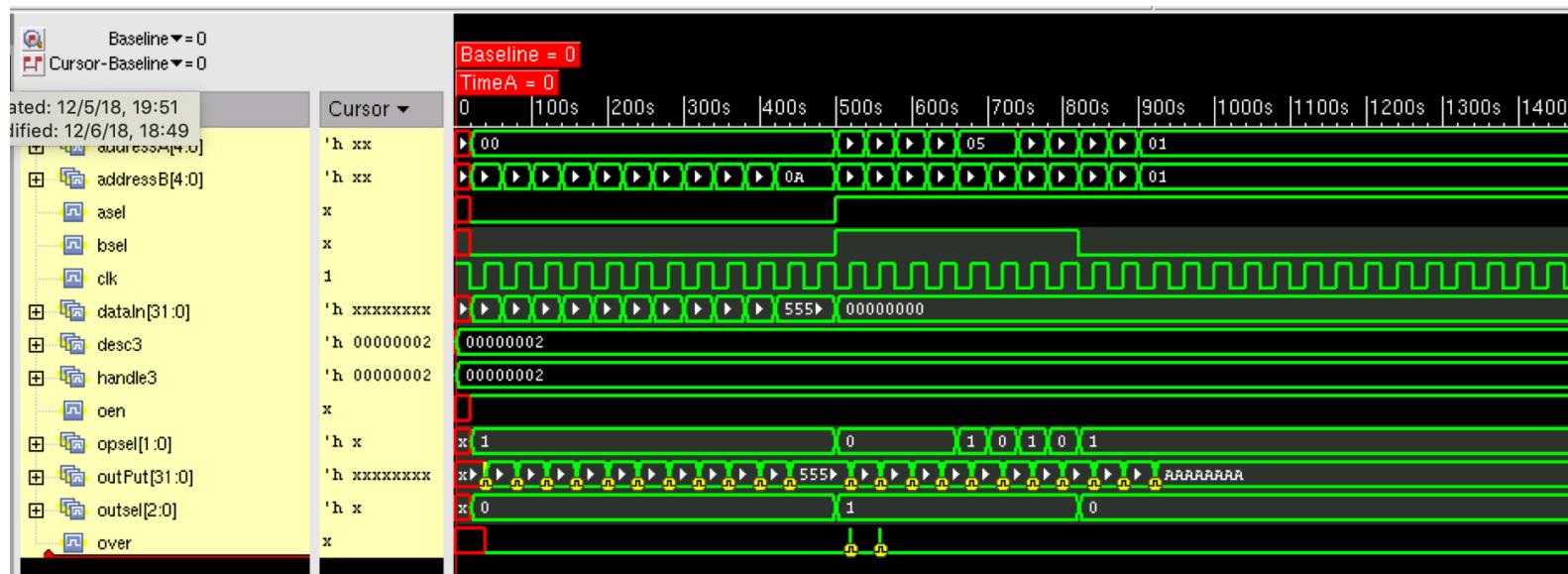
Design Name: cpu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (353.6775, 354.5500)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 23:59:36 **** Processed 5000 nets (Total 12728)
**** 23:59:36 **** Processed 10000 nets (Total 12728)
Time Elapsed: 0:00:02.0

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Thu Dec 6 23:59:37 2018
***** End: VERIFY CONNECTIVITY *****
  Verification Complete : 0 Viols. 0 Wrngs.
  (CPU Time: 0:00:01.7 MEM: 0.500M)

*****
* Encounter script finished *
* *
* Results: *
* ----- *
* Layout: final.gds2 *
* Netlist: final.v *
* Timing: timing.rep.5.final *
* *
* Type 'win' to get the Main Window *
* or type 'exit' to quit *
* *
*****encounter 1>

```



```

Compiling source file "tb_test.v"
Compiling source file "cpu_CRA.v"

Warning! Port sizes differ in port connection (port 7)      [Verilog-PCDPC]
          "tb_test.v", 18; outsel

Warning! Too few module port connections                      [Verilog-TFNPC]
          "cpu_CRA.v", 557; cra0(.sum(sum[7:0]), .c_out(c7),
          , .a(a[7:0]), .b(b[7:0]), .c_in(c_in))

Warning! Too few module port connections                      [Verilog-TFNPC]
          "cpu_CRA.v", 558; cra1(.sum(sum[15:8]), .c_out(
          c15), .a(a[15:8]), .b(b[15:8]), .c_in(c7))

Warning! Too few module port connections                      [Verilog-TFNPC]
          "cpu_CRA.v", 559; cra2(.sum(sum[23:16]), .c_out(
          c23), .a(a[23:16]), .b(b[23:16]), .c_in(c15))

Highest level modules:
stimulus3

L34 "tb_test.v": $finish at simulation time 1501
4 warnings
0 simulation events (use +profile or +listcounts option to count) + 97313 accelerated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 1.3 secs in simulation
End of Tool:    VERILOG-XL    08.20.001-p   Dec  7, 2018  00:40:12
avannopp@saturn.ece.iit.edu:"%
```

CLA:

xterm

```
For technical assistance please contact the Cadence Response Center at  
1-877-CDS-4911 or send email to support@cadence.com

For more information on Cadence's Verilog-XL product line send email to  
talkv@cadence.com

Compiling source file "tb_cpu.v"
Compiling source file "cpu_CLA.v"

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 636: CLA0(.s(s[15:0]), .a(a[15:0]),
.b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
g_16(g[0]))]

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]),
.b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
0]))]

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]),
.b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
1]))]

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
.b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
p[2]))]

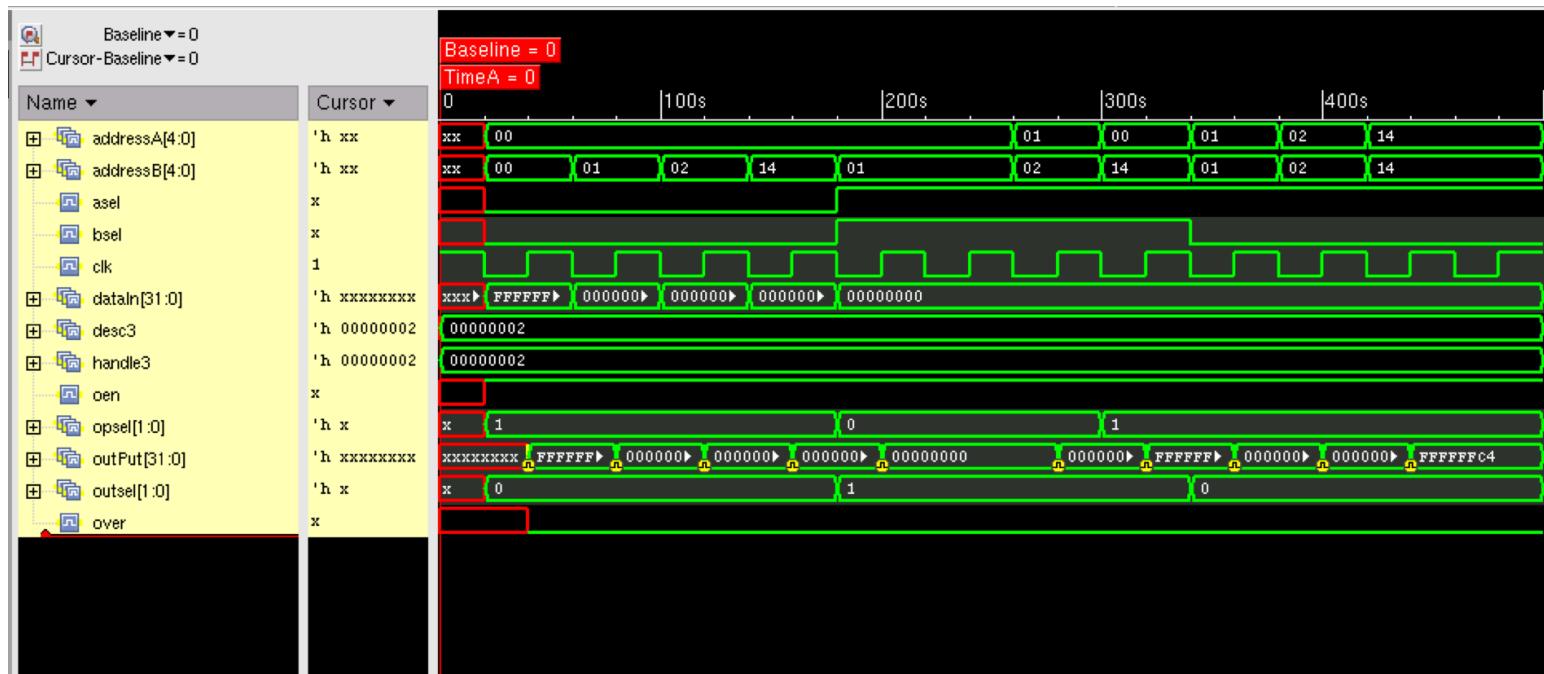
Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]),
.b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
0]))]

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]),
.b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
1]))]

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
.b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
p[2]))]

Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 19773 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
End of Tool:    VERILOG-XL      08.20.001-p   Dec  6, 2018  19:26:49
avannopp@saturn.ece.iit.edu:"%
```



	compile_dc.tcl	cpu_CLA.v	cell.rep	timing.rep
o/tr/t1/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14359 cells			48566.448185	
1				

Timing Report (timing.rep)

a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11	r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18	r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24	r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31	r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37	r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44	r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48	f
a/U26/Y (AOI22X1)	0.03	6.52	r
U219/Y (BUFX2)	0.04	6.56	r
U64/Y (AND2X1)	0.07	6.62	r
U1729/Y (INVX1)	0.10	6.73	f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78	r
U3762/Y (INVX1)	0.02	6.80	f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80	f
data arrival time		6.80	
clock clk (rise edge)	33.00	33.00	
clock network delay (ideal)	0.00	33.00	
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00	r
library setup time	-0.06	32.94	
data required time		32.94	

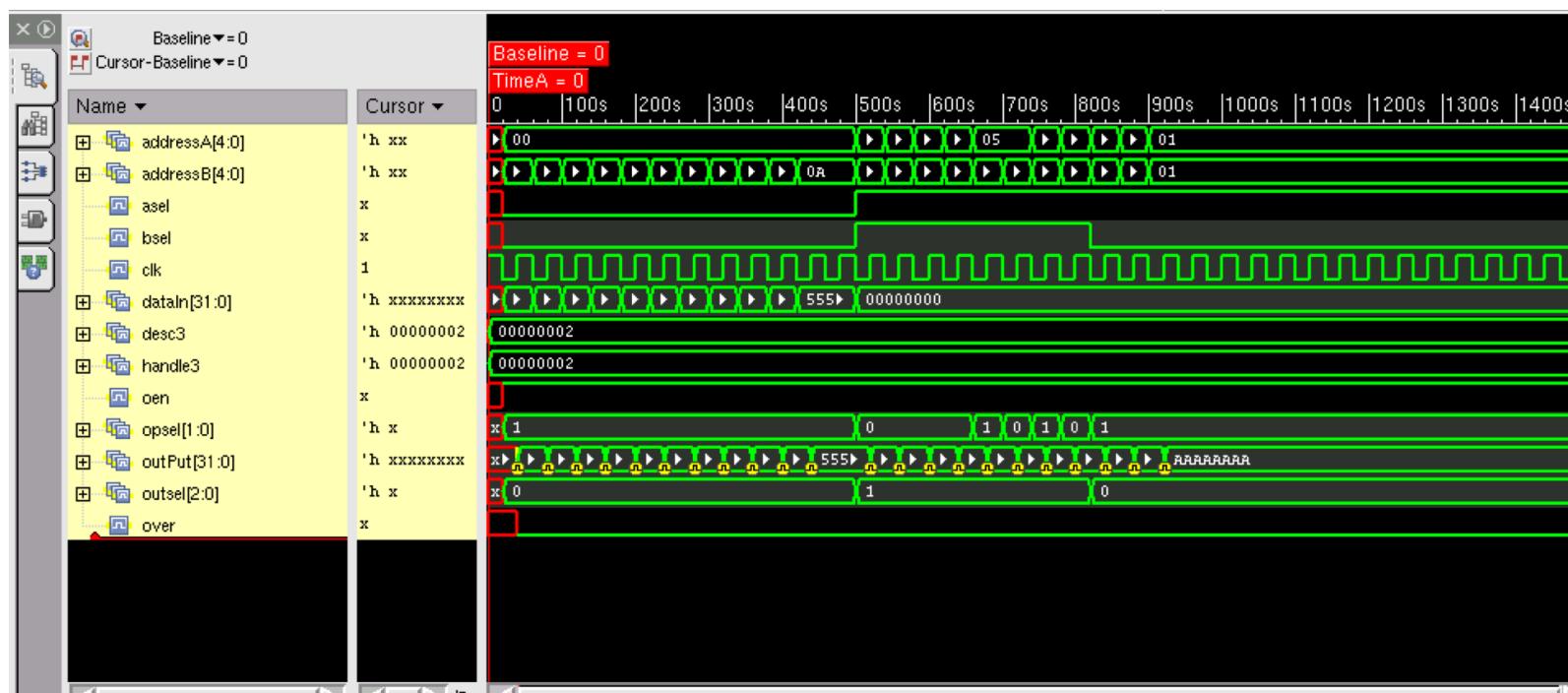
data required time		32.94	
data arrival time		-6.80	

slack (MET)		26.14	

1

Timing Report (timing.rep.5.final)

<hr/>			
# Generated by:	Cadence Encounter 10.13-s292_1		
# OS:	Linux x86_64(Host ID saturn.ece.iit.edu)		
# Generated on:	Thu Dec 6 23:20:38 2018		
# Design:	cpu		
# Command:	report_timing -nworst 10 -net > timing.rep.5.final		
<hr/>			
Path 1: MET Setup Check with Pin mb/ram/mer30/ll/me31/qout_reg/CLK			
Endpoint: mb/ram/mer30/ll/me31/qout_reg/D (^) checked with leading edge of			
'clk'			
Beginpoint: m0pd/bb/me1/qout_reg/Q	(v) triggered by	leading edge of	
'clk'			
Other End Arrival Time	0.344		
- Setup	4.498		
+ Phase Shift	33.000		
= Required Time	28.846		
- Arrival Time	10.925		
= Slack Time	17.921		
Clock Rise Edge	0.000		
+ Clock Network Latency (Prop)	0.333		
= Beginpoint Arrival Time	0.333		



```

Compiling source file "tb_test.v"
Compiling source file "cpu_CLA.v"

Warning! Port sizes differ in port connection (port 7)      [Verilog-PCDPC]
          "tb_test.v", 18: outsel

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 636: CLA0(.s(s[15:0]), .a(a[15:0]),
          .b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
          g_16(g[0]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]),
          .b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0])))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]),
          .b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1])))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
          .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
          p[2])))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 618: CLA0(.s(s[3:0]), .a(a[3:0]),
          .b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0])))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 619: CLA1(.s(s[7:4]), .a(a[7:4]),
          .b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1])))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CLA.v", 620: CLA2(.s(s[11:8]), .a(a[11:8]),
          .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
          p[2])))

Highest level modules:
stimulus3

L34 "tb_test.v": $finish at simulation time 1501
8 warnings
0 simulation events (use +profile or +listcounts option to count) + 94490 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 1.3 secs in simulation
End of Tool:    VERILOG-XL      08.20.001-p   Dec  7, 2018  00:38:55
avannopp@saturn.ece.iit.edu:~% ■

```

CSeA:

```
Compiling source file "tb_cpu.v"
Compiling source file "cpu_CSeA.v"

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 606: csel(.s(s[15:0]), .cout(c), .
a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
a(a[7:4]), .b(b[7:4]), .cin(c[1]))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
a(a[11:8]), .b(b[11:8]), .cin(c[2]))

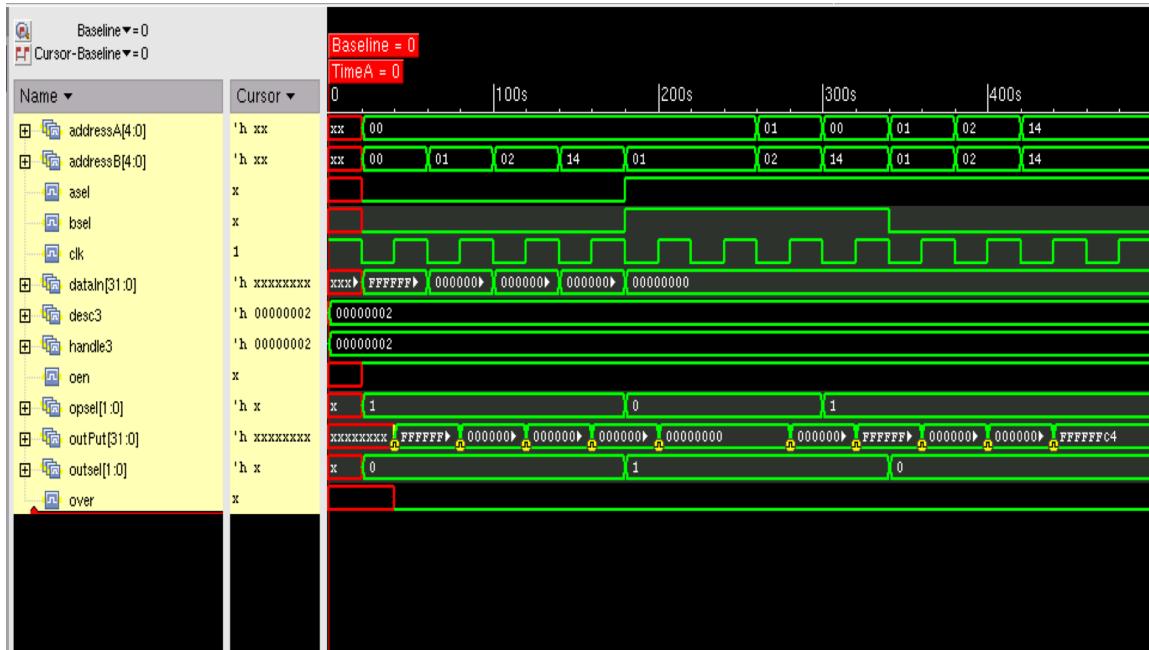
Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
a(a[7:4]), .b(b[7:4]), .cin(c[1]))

Warning! Too few module port connections [Verilog-TFNPC]
"cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
a(a[11:8]), .b(b[11:8]), .cin(c[2]))

Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 21936 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
End of Tool:  VERILOG-XL 08.20.001-p Dec 6, 2018 19:34:44
avannapp@saturn.ece.iit.edu:"% ■
```



compile_dc.tcl x cpu_CSeA.v x cell.rep x timing.rep x

a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11	r
a/l3/f274/U2/Y (X0R2X1)	0.07	6.18	r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24	r
a/l3/f283/U2/Y (X0R2X1)	0.07	6.31	r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37	r
a/l3/f292/U2/Y (X0R2X1)	0.07	6.44	r
a/l3/h301/U2/Y (X0R2X1)	0.04	6.48	f
a/U26/Y (AOI22X1)	0.03	6.52	r
U243/Y (BUFX2)	0.04	6.56	r
U74/Y (AND2X1)	0.07	6.62	r
U1844/Y (INVX1)	0.10	6.73	f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78	r
U3884/Y (INVX1)	0.02	6.80	f
mb/ram/mer12/ll/me31/qout_reg/D (DFFP0SX1)	0.00	6.80	f
data arrival time			6.80
clock clk (rise edge)	33.00	33.00	
clock network delay (ideal)	0.00	33.00	
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFP0SX1)	0.00	33.00	r
library setup time	-0.06	32.94	
data required time			32.94

data required time			32.94
data arrival time			-6.80

slack (MET)			26.14

compile_dc.tcl x cpu_CSeA.v x cell.rep x timing.rep x

o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14577 cells			49150.726672	
1				

cpu_CSeA.v x cell.rep x timing.rep x gscl45nm.v x encounter.conf x timing.rep.5.final x

```
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Thu Dec 6 21:40:47 2018
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer18/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer18/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.319
- Setup 4.060
+ Phase Shift 33.000
= Required Time 29.259
- Arrival Time 11.114
= Slack Time 18.144
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.314
= Beginpoint Arrival Time 0.314

+-----+
+ | Pin | Edge | Net | Cell
| Delay | Arrival | Required | |
| | | | |
| | Time | Time | |
```

```
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus

"gscl45nm.v", 299: Timing violation in stimulus.proj.\a\13\rc30\qout_reg
    $setup( negedge D:36017, posedge CLK:36018, 0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 211984 accelerated even-
ts + 345638 timing check events
CPU time: 0.1 secs to compile + 0.3 secs to link + 0.2 secs in simulation
End of Tool:   VERILOG-XL      08.20.001-p   Dec  6, 2018  22:29:18
avannopp@saturn.ece.iit.edu:~% █
```

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 6 22:38:46 2018

Design Name: cpu
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (352.1725, 354.5500)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 22:38:46 **** Processed 5000 nets (Total 12633)
**** 22:38:47 **** Processed 10000 nets (Total 12633)
Time Elapsed: 0:00:01.0

Begin Summary
    Found no problems or warnings.
End Summary

End Time: Thu Dec 6 22:38:47 2018
***** End: VERIFY CONNECTIVITY *****
    Verification Complete : 0 Viols, 0 Wrngs.
    (CPU Time: 0:00:01.7  MEM: 0.500M)

*****
* Encounter script finished      *
*                                     *
* Results:                         *
* -----                         *
* Layout: final.gds2             *
* Netlist: final.v               *
* Timing: timing.rep.5.final   *
*                                     *
* Type 'win' to get the Main Window *
* or type 'exit' to quit           *
*                                     *
*****
```

```
Compiling source file "tb_test.v"
Compiling source file "cpu_CSeA.v"

Warning! Port sizes differ in port connection (port 7)      [Verilog-PCDPC]
          "tb_test.v", 18; outsel

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 606: cse1(.s(s[15:0]), .cout(c), .
          a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
          a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
          a(a[7:4]), .b(b[7:4]), .cin(c[1]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
          a(a[11:8]), .b(b[11:8]), .cin(c[2]))

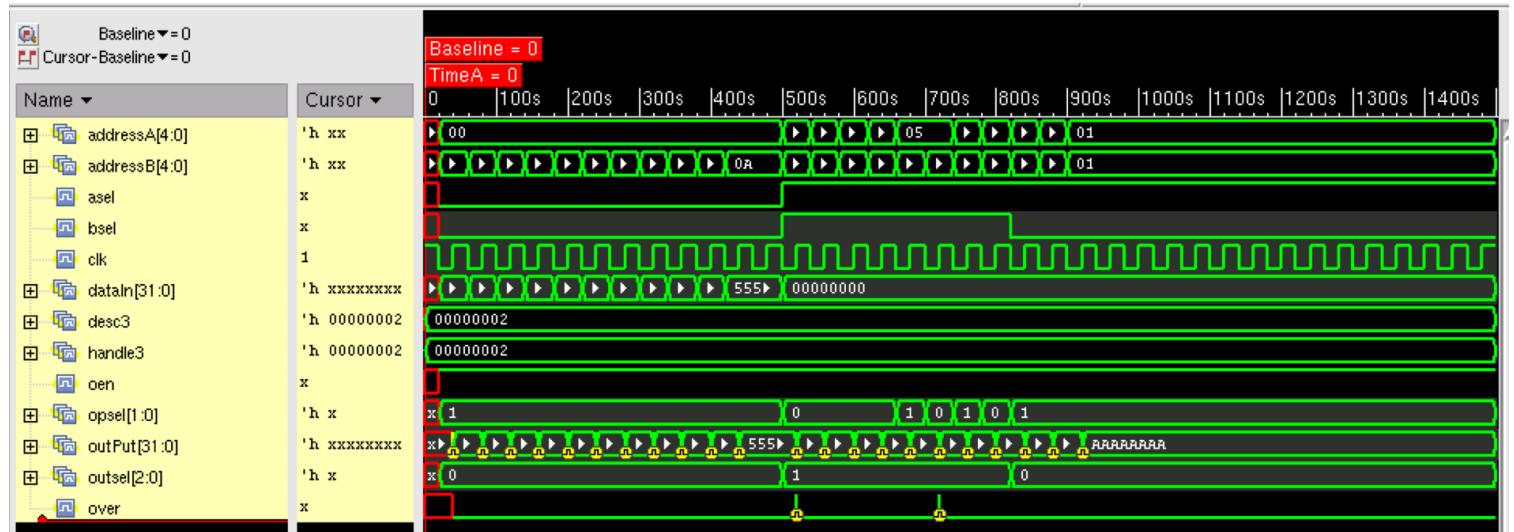
Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
          a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
          a(a[7:4]), .b(b[7:4]), .cin(c[1]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
          a(a[11:8]), .b(b[11:8]), .cin(c[2]))

Highest level modules:
stimulus3

L34 "tb_test.v": $finish at simulation time 1501
8 warnings
0 simulation events (use +profile or +listcounts option to count) + 99769 accelerated event
s
CPU time: 0.0 secs to compile + 0.1 secs to link + 1.3 secs in simulation
End of Tool:    VERILOG-XL    08.20.001-p   Dec  7, 2018  00:35:02
avannopp@saturn.ece.iit.edu:"%
```



Case Study-2:

```
Compiling source file "tb_test_comp.v"
Compiling source file "cpu_comp.v"

Warning! Port sizes differ in port connection (port 7)      [Verilog-PCDPC]
          "tb_test_comp.v", 17: outsel

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 647: CLA0(.s(s[15:0]), .a(a[15:0])
          , .b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
          g_16(g[0]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 626: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[0]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 627: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[1]))

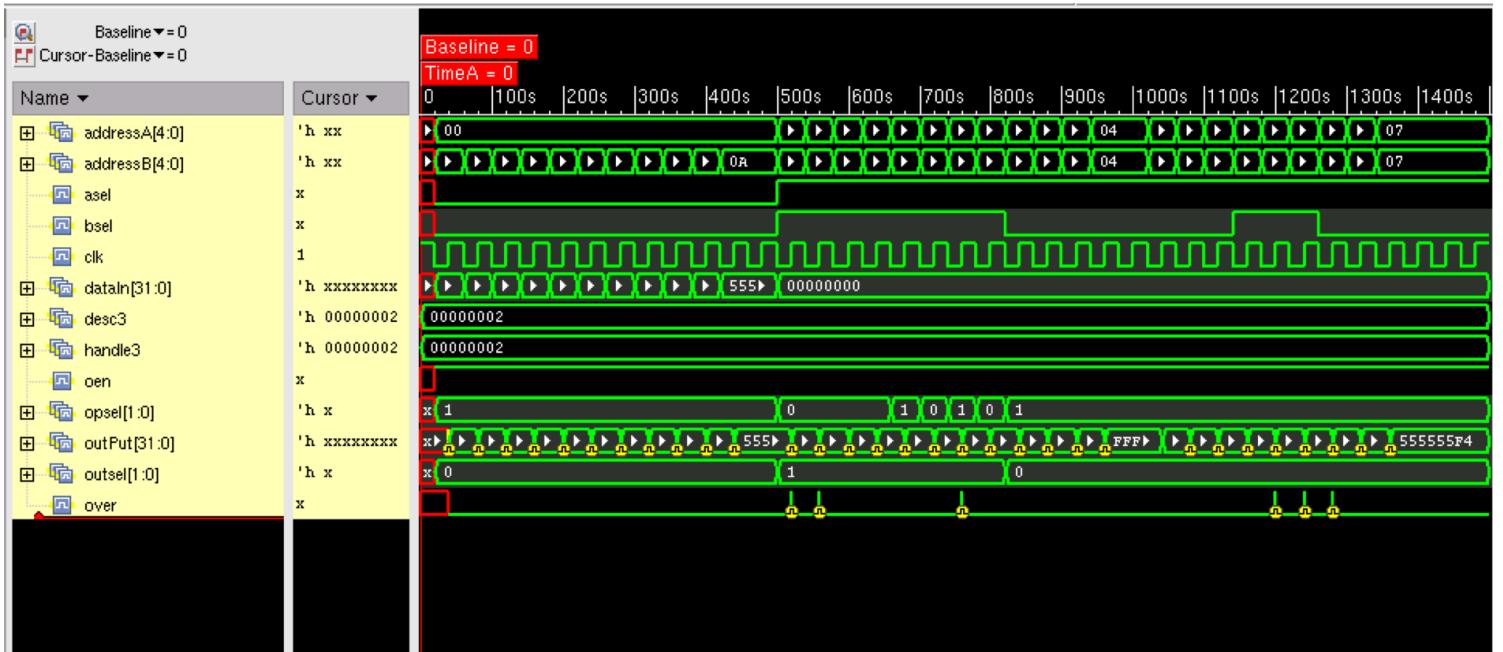
Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 628: CLA2(.s(s[11:8]), .a(a[11:8])
          , .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .
          p_4(p[2]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 626: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[0]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 627: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[1]))

Warning! Too few module port connections                  [Verilog-TFNPC]
          "cpu_comp.v", 628: CLA2(.s(s[11:8]), .a(a[11:8])
          , .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .
          p_4(p[2]))
Highest level modules:
stimulus

Please check Select Lines!
L33 "tb_test_comp.v": $finish at simulation time 1501
8 warnings
0 simulation events (use +profile or +listcounts option to count) + 132441 accelerated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 1.5 secs in simulation
End of Tool:    VERILOG-XL    08.20.001-p   Dec  7, 2018  03:15:40
avannopp@saturn.ece.iit.edu:"%
```



compile_dc.tcl x cpu_comp.v x tb_test_comp.v x cell.rep x timing.rep x

a/l3/f247/U5/Y (XNOR2X1)	0.06	5.72 r
a/l3/f247/U2/Y (XOR2X1)	0.07	5.79 r
a/l3/f256/U5/Y (XNOR2X1)	0.06	5.85 r
a/l3/f256/U2/Y (XOR2X1)	0.07	5.92 r
a/l3/f265/U5/Y (XNOR2X1)	0.06	5.98 r
a/l3/f265/U2/Y (XOR2X1)	0.07	6.05 r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.12 r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.19 r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.25 r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.32 r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.38 r
a/l3/f292/U2/Y (XOR2X1)	0.05	6.43 f
U1703/Y (AND2X1)	0.03	6.46 f
a/l3/rc31/qout_reg/D (DFFP0SX1)	0.00	6.46 f
data arrival time		6.46
clock clk (rise edge)	33.00	33.00
clock network delay (ideal)	0.00	33.00
a/l3/rc31/qout_reg/CLK (DFFP0SX1)	0.00	33.00 r
library setup time	-0.06	32.94
data required time		32.94
data required time		32.94
data arrival time		-6.46
slack (MET)		26.48

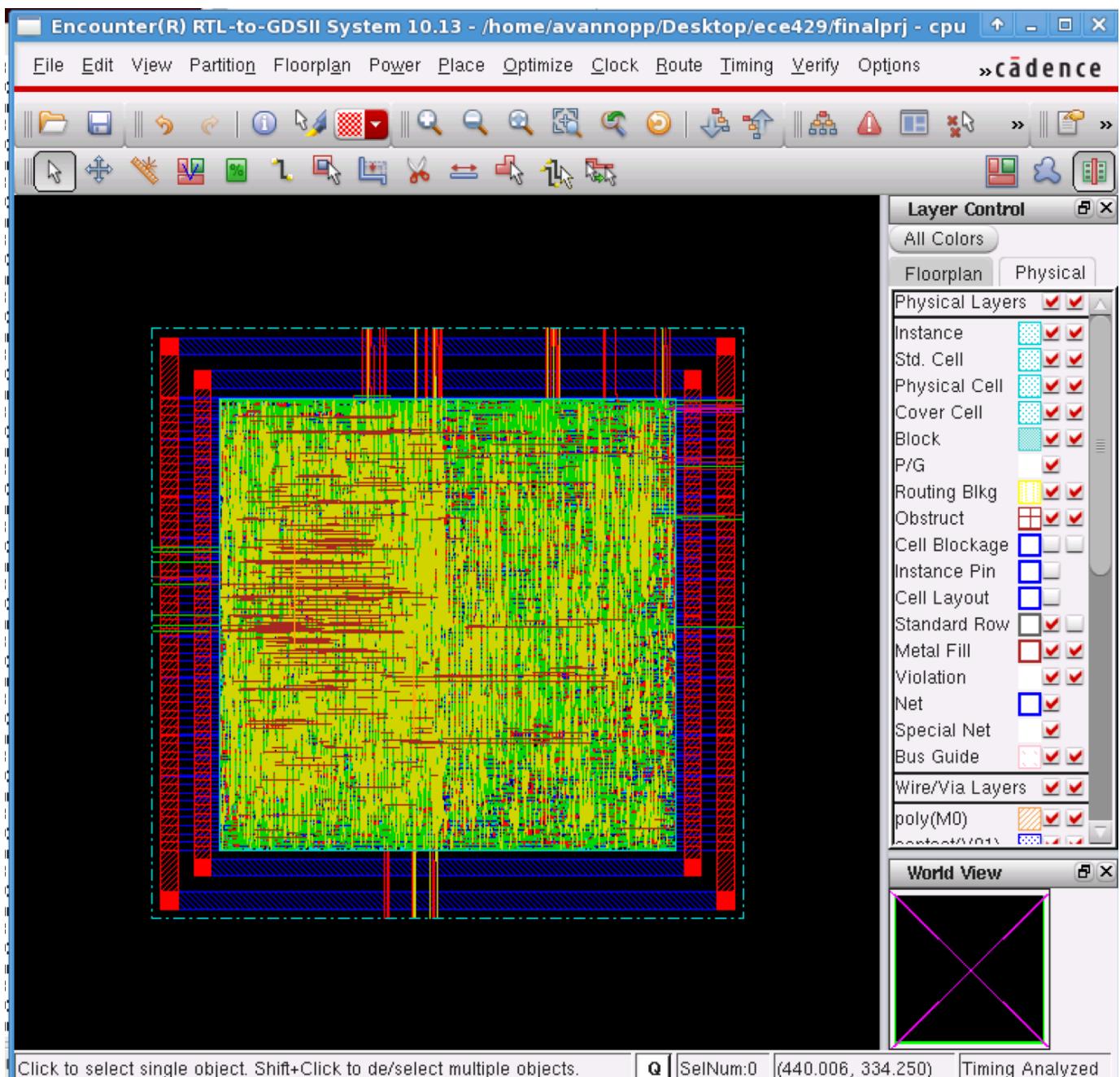
o/tr/t1/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
<hr/>				
Total 14631 cells			49305.595675	
1				



```
Compiling source file "gscl45nm.v"
Compiling source file "tb_test_comp.v"
Compiling source file "cpu.vh"

Warning! Port sizes differ in port connection (port 7)      [Verilog-PCDPC]
          "tb_test_comp.v", 17: outsel
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
MUX2X1
OAI22X1
OR2X2
TBUFX1
stimulus

L33 "tb_test_comp.v": $finish at simulation time 150100
1 warning
0 simulation events (use +profile or +listcounts option to count) + 824683 accelerated events + 1020408 timing check events
CPU time: 0.1 secs to compile + 0.3 secs to link + 0.7 secs in simulation
End of Tool:    VERILOG-XL    08.20.001-p   Dec  7, 2018  03:33:37
avannopp@saturn.ece.iit.edu:"% "
```

```
compile_dc.tcl x cpu_comp.v x tb_test_comp.v x cell.rep x timing.rep x timing.rep.5.final x
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Fri Dec 7 03:46:09 2018
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin a/l3/rc31/qout_reg/CLK
Endpoint: a/l3/rc31/qout_reg/D (^) checked with leading edge of 'clk'
Beginpoint: m0pd/bb/me2/qout_reg/Q (v) triggered by leading edge of 'clk'
Other End Arrival Time 0.352
- Setup 3.344
+ Phase Shift 33.000
= Required Time 30.009
- Arrival Time 10.207
= Slack Time 19.801
| Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.341
= Beginpoint Arrival Time 0.341
+-----+
```