**Main memory for multi-banking system**

**Abstract--**

In this paper we present about the DRAM simulation. Our focus is DDR2/DDR3 ram. The simulator which we used, work on x86. In this paper our focus is to visualize and compare the memory system. We worked on the performance metrics such as bandwidth latency and power.

1. **Introduction**

There are many simulators like simplistic models of memory and many other. The main reason to select DRAMSim2 because of accurate memory cycle. We have also seen that many simulators fail during the high complexity behaviour of memory system. DRAMSim2 have very simple programming interface an object-oriented design which provides a verification tool that can be used to validate the result. In this paper we also understand the structure of memory system and how the multibank is configured. How the data is transferred from the memory bank to the cache buffer. And the main part which we worked on are different kinds of memory latency.

1. **DRAMSim2 Architecture**

In this section we will briefly discuss plus how the DRAM simulator 2 structure is designed and how it works. The structure of the DRAM simulator 2 is given in Figure 1.

Diagram

Description automatically generated

Coming soon ………