ES 215 Computer Organization and Architecture

Assignment 1

Assumptions:

1. Initially, we have initialised the data in memory [31:0]RegFile[31:0] using the initial block.
   Each location contains the square value corresponding to the location.
   1st location contains 1, 2nd location contains 4, similarly, ith location contains i*i value as shown in Figure 1 below.
   For eg. if RS1=1; D1_OUT = 1, RS1 = 2; D1_OUT = 4, and so on.
   We are aware of the fact that the SDLX doesn't have any multiplier block. We have just used the initial block for initialisation. We could have used any other initialisation pattern.
2. LSB is an extra variable, which we have taken in order to show our 32 bit outputs using 16 LEDs available. When LSB=1, then LEDs show lower 16 bits and when LSB=0, then LEDs show upper 16 bits.

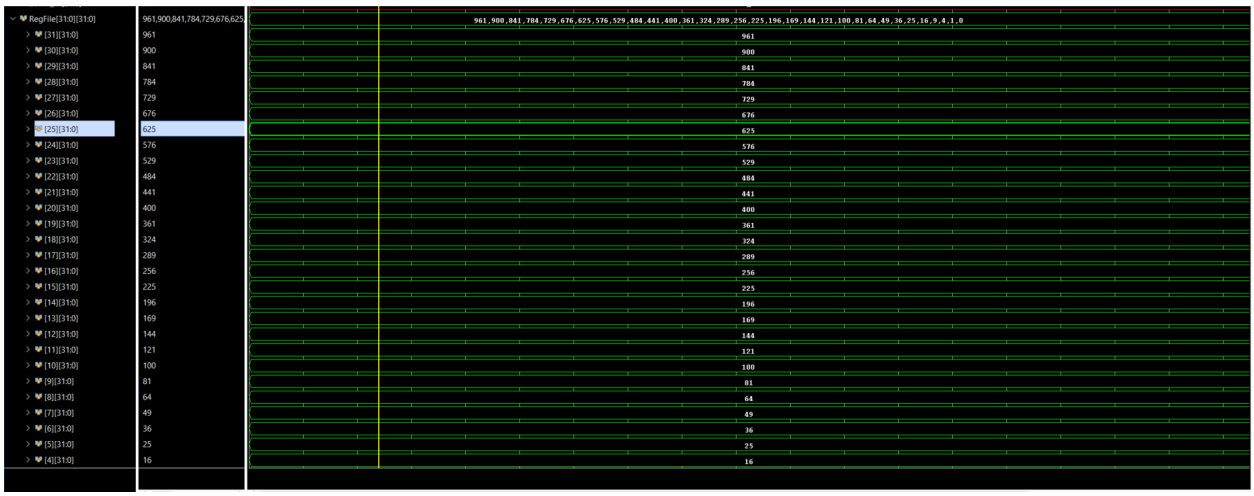
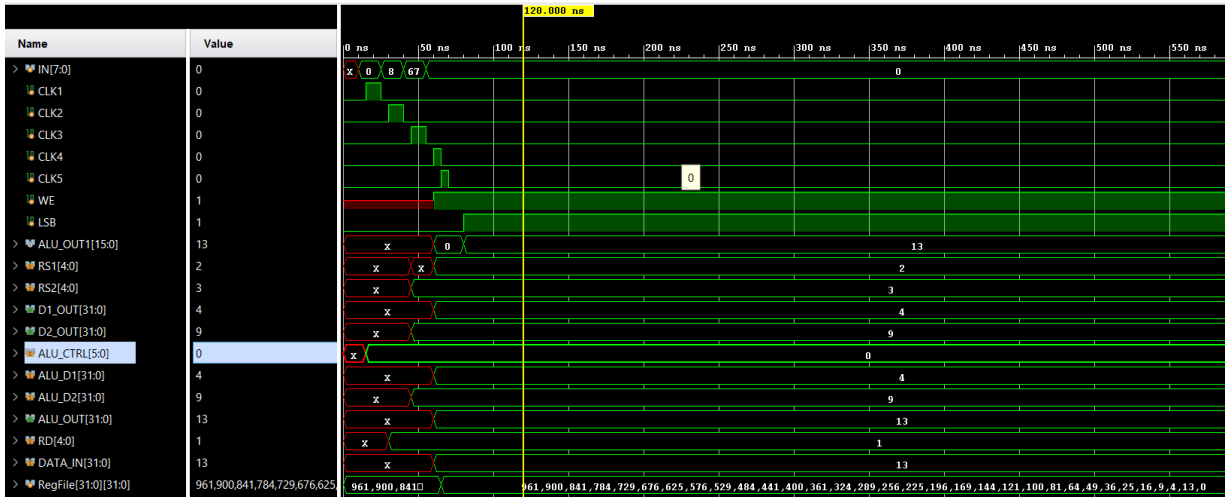


Figure 1

Following figures show the results of different arithmetic operations performed by the Arithmetic Logic Unit module of our code.

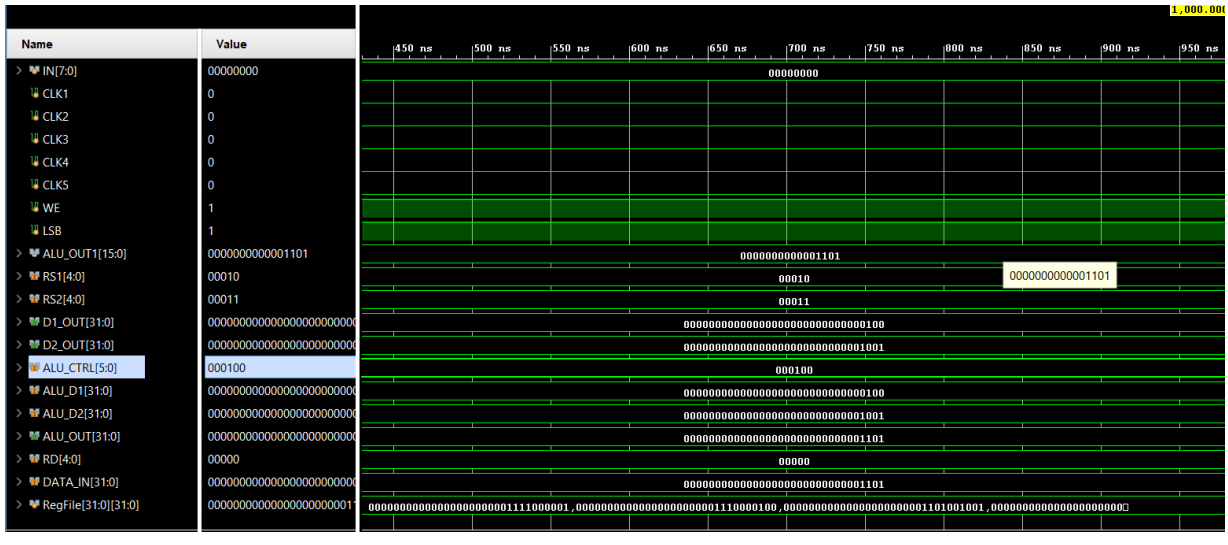
Addition: RS1 contains 2 => D1_OUT = 4, RS2 contains 3 => D2_OUT = 9.
Hence the result 2*2+3*3 = 13 is stored as output in ALU_OUT. So, the value in first location of the RegFile will be updated to 13.



RS1 = 2, RS2=3, RD=1

Figure 2

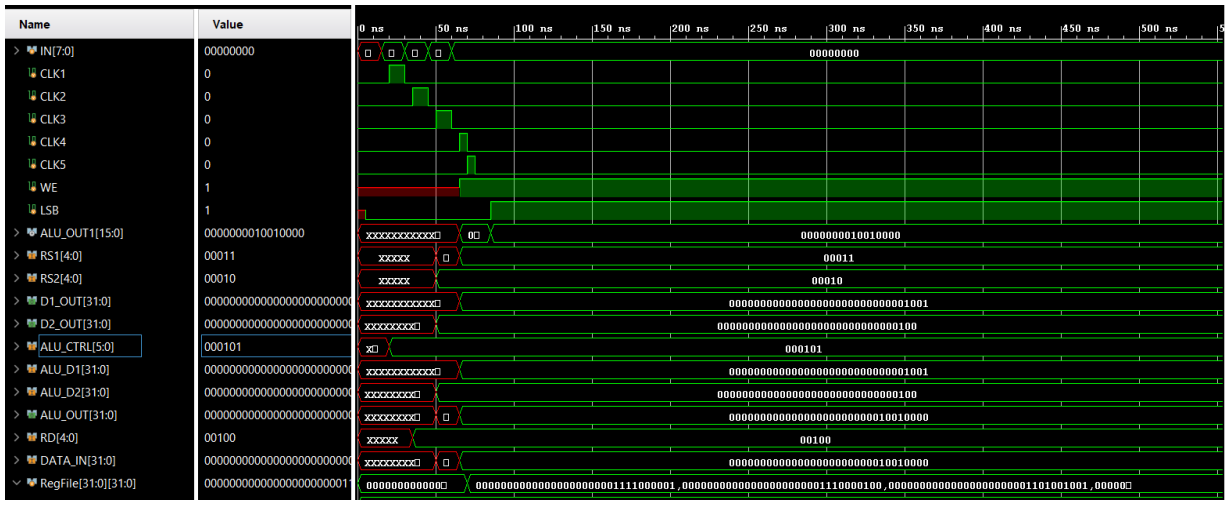
XOR: RS1 contains 2 => D1_OUT = 4, RS2 contains 3 => D2_OUT = 9.
Hence the result of 0100 ^ 1001 = 1101 is stored as output in ALU_OUT. So, the value in first location of the RegFile will be updated to 1101.



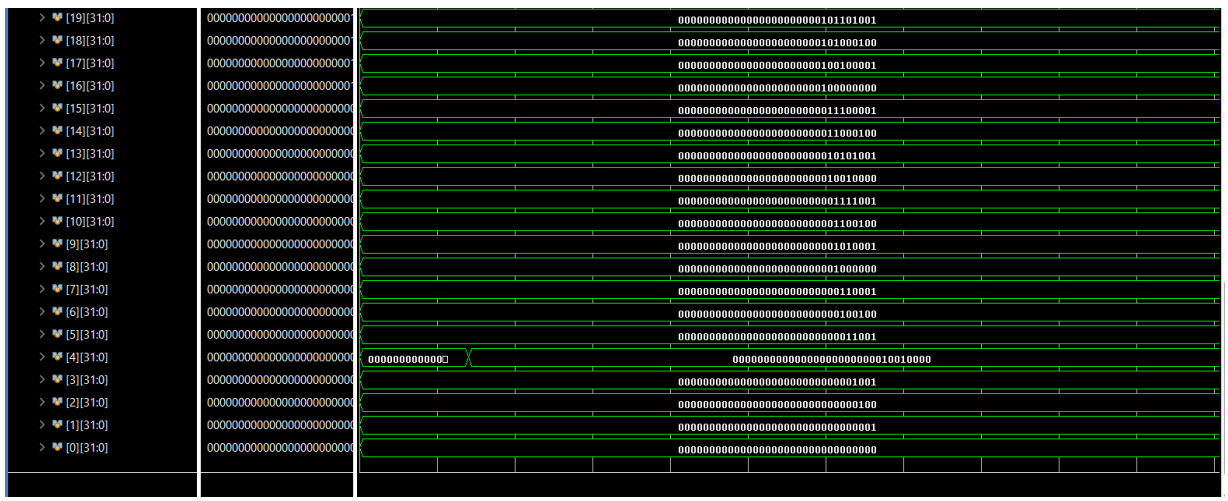
RS1 = 2, RS2=3, RD=1

Figure 3

SLL : RS1 contains 3 => D1_OUT = 9, RS2 contains 2 => D2_OUT = 4. Hence the result of shifting 9 logically left 4 times gives 10010000. This is stored as output in ALU_OUT.
So, the value in the fourth location of the RegFile will be updated to 10010000 as shown in figure below.



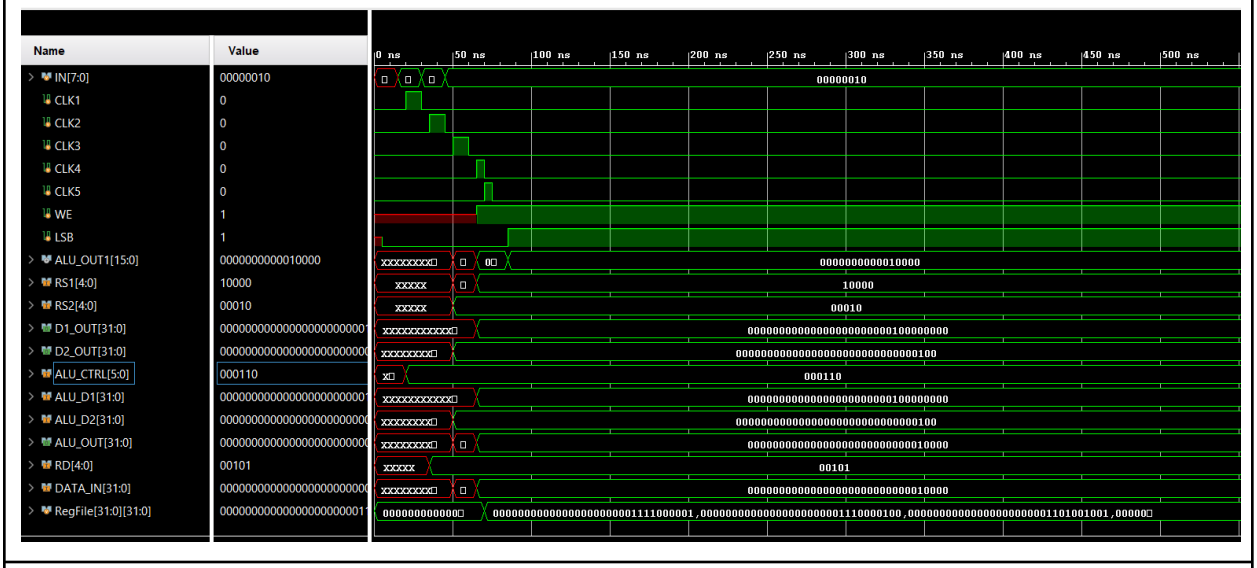
RS1 = 3, RS2=2



RD=4

Figure 4

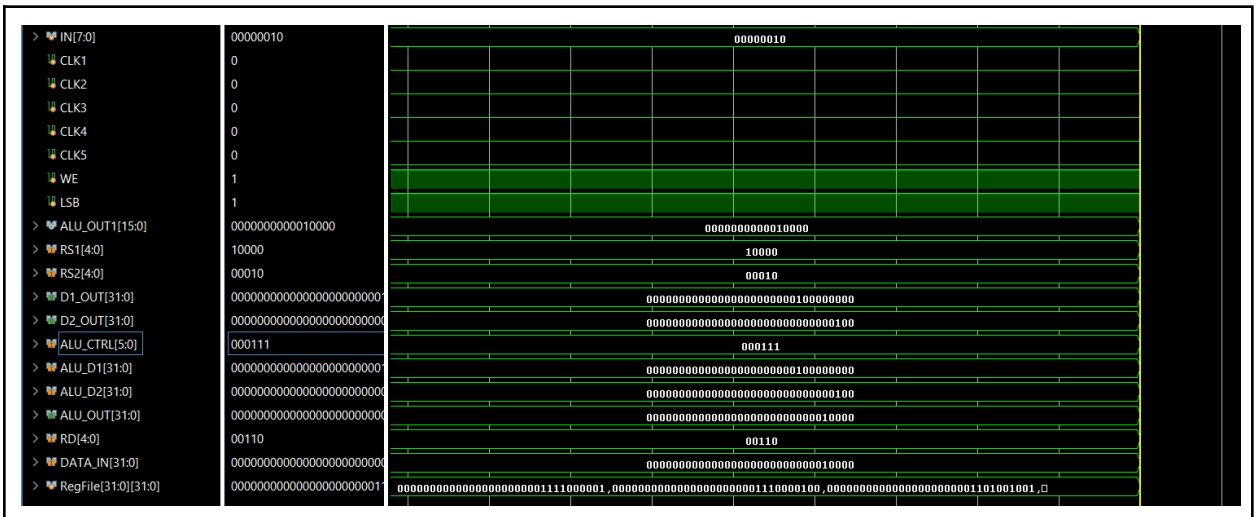
SRL: RS1 contains 16 => D1_OUT = 256, RS2 contains 2 => D2_OUT = 4. Hence the result of shifting 256 logically right 4 times gives 10000. This is stored as output in ALU_OUT.
So, the value in the fifth location of the RegFile will be updated to 10000 as shown in figure below.



RS1 = 16, RS2=2, RD =5

Figure 5

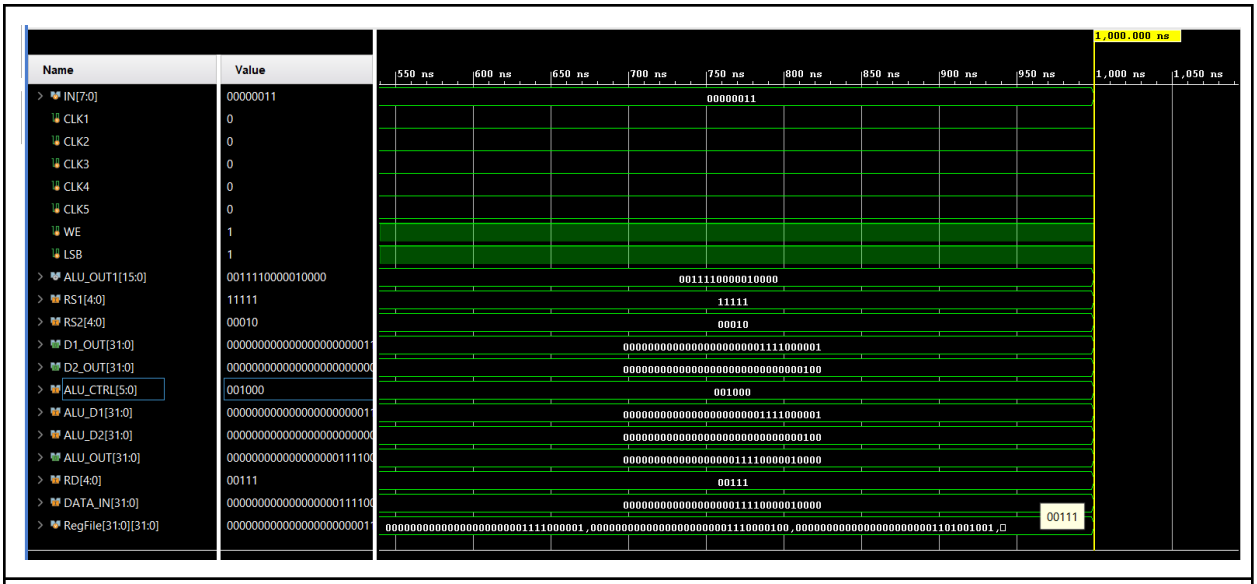
SRA: RS1 contains 16 => D1_OUT = 256, RS2 contains 2 => D2_OUT = 4. Hence the result of shifting 256 arithmetic right 4 times gives 10000. This is stored as output in ALU_OUT.
So, the value in sixth location of the RegFile will be updated to 10000 as shown in figure below.



rs1 = 16 rs2=2 RD =6

Figure 6

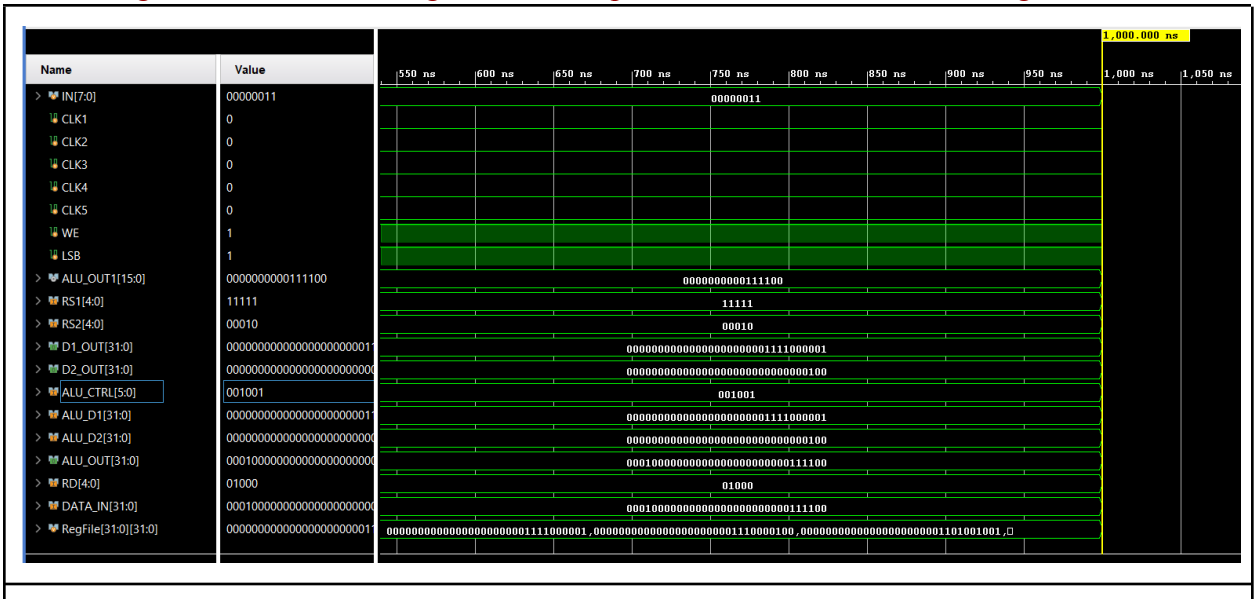
ROL: RS1 contains 31 => D1_OUT = 961, RS2 contains 2 => D2_OUT = 4. Hence the result of shifting 961 logically left 4 times gives 11110000010000. This is stored as output in ALU_OUT. So, the value in the seventh location of the RegFile will be updated to 11110000010000 as shown in figure below.



rs1 = 31 rs2=2 RD =7

Figure 7

ROR: RS1 contains 31 => D1_OUT = 961, RS2 contains 2 => D2_OUT = 4. Hence the result of shifting 961 logically right 4 times gives 111100. This is stored as output in ALU_OUT. So, the value in eight locations of the RegFile will be updated to 111100 as shown in figure below.

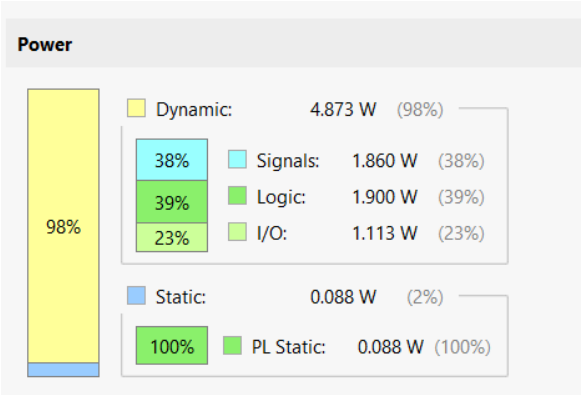


rs1 = 31 rs2=2 RD =8

Figure 8

Synthesis Reports: Synthesis done successfully

RESOURCE	UTILIZATION	AVAILABLE	UTILIZATION%
LUT	743	20800	3.57
LUTRAM	48	9600	0.59
FF	21	41600	0.05
IO	31	106	29.25
BUFG	6	32	18.75



Contribution of each group member: All the group members have participated equally.

1. Alok Pradhan (21250001)-
    a. Combined the individual blocks to complete design
    b. Thoroughly tested the code on simulation level on Vivado.
    c. Implemented design on FPGA.
    d. Commenting the code for better readability
    e. Prepared the report by adding other important information.

2. Sakshi Sawai (21250021)-
    a. Designed ALU Block
    b. Implemented design on FPGA
    c. Verification of code on FPGA Board.
    d. Prepared the report by adding other important information.

3. Sukanya More (20110205) -
    a. Designed Register File.
    b. Implemented design on FPGA.
    c. Verification of code on FPGA Board.
    d. Comments within the code.
    e. Inserted images of all the results, synthesis and implementation in the report.