Roll No

Dr B R Ambedkar National Institute of Technology, Jalandhar B Tech (Electrical Engineering)

EEPC-301, Microprocessors and Interfacing End Semester Examination, Dec 2020

Duration: 02 Hours Max. Marks: 40 Date: 1^{st} Dec 2020

(Marks Distribution & Mapping of Questions with Course Outcomes (COs))									
Question Number	1	2	3	4	5	6	7	8	
Marks	5	5	5	5	5	5	5	5	
CO No.	1	1	2	1	2	2	3	3	
Learning Level	1	1	3	3	3	2	2	2	

Note:

- 1. Attempt all the questions.
- 2. Write the answers in hard copy (on A4 sheet) using blue/black pen with your signature on top left and page number on top right corner of each page of the answer booklet.
- 3. The time allowed for writing examination is 02 hours. Extra 15 minutes are allowed for preparing the PDF file of Answer Booklet and submitting it.
- 4. Follow the instructions regarding submission of answer booklet as issued by the examination section.
 - Q 1. Draw the architecture and pin diagram of microprocessor 8085 and answer the following questions.
 - (a) Name different registers in 8085 and explain their function.
 - (b) What are flags in 8085 and how are they affected.
 - (c) Compare the architecture of 8085 with 8086.
 - Q 2. Explain the machine cycles of the following instruction when it is executed, also draw its timing diagram.

Memory Address Instruction Opcode Oprand 2010 STA 32H 2065

- Q 3. By examining the range of the foldback memory in Figure 1, specify the relationship between the range of foldback memory and the number of don't care lines.
- Q 4. Write the assembly language program to add an array of numbers stored in memory location and subsequently store the result in two consecutive memory locations.
- Q 5. (a) Draw the architecture of interrupts in 8085. Discuss the bit pattern of the accumulator for SIM instruction.
 - (b) In relation to Figure 2 what is the instruction placed on the data bus when input line I_6 of the encoder goes low, thus requesting the interrupt service?
- Q 6. Draw the block diagram of 8255 and explain its control word. Port A of 8255 is set up in Mode 1, and the status word is read as 18H. Is there an error in the status word?

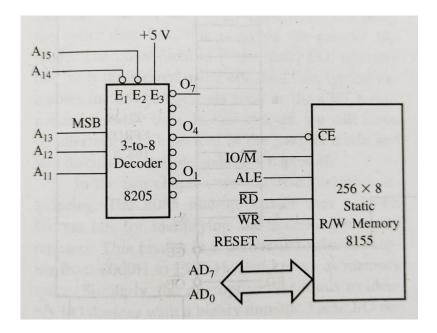


Figure 1:

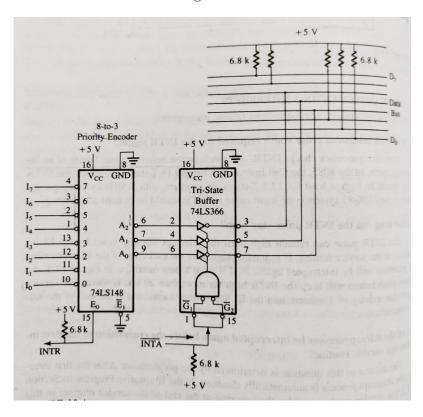


Figure 2:

- Q 7. Explain how the 8237 DMA controller transfers $64\mathrm{K}$ byte of data per channel with eight address lines.
- Q 8. Set up the 8254 as a square-wave generator with a 1 ms period, if the input frequency to the 8254 is 1 MHz.
