ALOK SETHI

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Profile

- More than 4 years of experience with mmWave analog RF design
- Excellent knowledge of C, MATLAB and Linux (both kernel and user plane).
- Good working knowledge of Virtuoso and Shell Scripting.
- Result oriented, responsible and adapt well to changing situations.
- Excellent academic record.

Experience

Doctoral Student (5/2015 – Present), ***Centre for Wireless Communications*** (Oulu, Finland)
CWC is a university based leading research institute in the field of wireless communication.
I am doing my PhD in analog integrated circuit design. My research focus is to design and develop new transmitter architectures for the 5th generation of wireless systems. I have already managed to do three successful tapeout and have measured two. Below are listed few of my responsibilities

- Circuit design and simulations for developing a phased array based transmitter,
- Embedded software design and development for controlling the complete measurement system which includes measurement equipment and the designed IC mounted on a PCB.

Till now, I have managed to publish at least four conference papers and one journal article as a first author. In addition, I have contributed to multiple conference papers and journal articles. Furthermore, I have one patent out of my current research.

Project Researcher (10/2013 – 5/2015), ***Centre for Wireless Communications*** (Oulu, Finland)
My main task was to develop the demonstrator which integrated both the analog and digital cancellation solutions that were being developed by the various partners of project DUPLO, an EU funded FP7 project. Below are listed few of my responsibilities

- Modifying the OFDM programmable core on Spartan 6 FPGA to support in-band Full Duplex physical layer,
- MATLAB simulations for developing a joint RF and baseband cancellation scheme for Full Duplex transceivers.

My biggest achievement was developing the Full Duplex demonstrator which was successfully demonstrated during the project dissemination.

Research Assistant (10/2012 – 09/2013), ***Centre for Wireless Communications*** (Oulu, Finland)
I worked in the Communication Signal Processing group where I studied the self-interference channel for the Full Duplex transceiver. My responsibilities included

- Performing channel measurements using a vector network analyzer and developing a channel model for the same,
- Enhancing the MATLAB simulation model for analog baseband cancellation, developed during the summer internship.

My biggest achievement was publishing my research work in an international conference.

Summer Intern (06/2012 – 09/2012), ***Renesas Mobile Europe*** (Oulu, Finland)
I performed MATLAB simulations for an analog baseband cancellation scheme targeted for Full Duplex transceiver.

Research Assistant (11/2011– 05/2012), ***Centre for Wireless Communications*** (Oulu, Finland)
I worked in the Wireless Sensor Networking lab, where I developed embedded software for STM32F207 microcontroller. My main responsibilities were

- Porting Contiki on STM3220G-EVAL evaluation board,
- Writing drivers for Ethernet, I2C, SPI, and FSMC and adding support for multiple radio drivers in Contiki.

Technical Leader (01/2010– 08/2011), ***VVDN*** (Gurgaon, India)

VVDN is a young firm (established in 2007) with a dedicated vision on embedded systems solution. It has strength of roughly 200 engineers.
I worked on the development of a TDMA wireless backhaul system using off the shelf WiFi cards, which was designed to be part of a carrier grade GSM network. My responsibilities included developing a transport and link layer for a TDMA over 802.11n WiFi system and modifying the Linux kernel to support synchronous operation.

Technical Leader (05/2005 – 01/2010), ***Aricent*** (Gurgaon, India)
Aricent is a product engineering services and software firm with more than 10,000 engineers worldwide. It has a dedicated focus on telecommunications.
At Aricent, I worked on three major projects. My responsibilities varied from a junior team member to a team leader of about ten software developers. My first project was done for Alvarion, where my main responsibilities were

- Designing, developing and testing a fault, performance and shelf manager for the WiMAX gateway,
- Integrating the embedded entity management system with the external management system.

My last two projects were done for Tellabs, where my main responsibilities were

- Designing, developing and testing fast path on Cavium Network Processor,
- Optimizing the fast path for the best possible speed,

My biggest achievement at Aricent was establishing an expertise on Cavium Network Processor. My team was awarded an excellence award for the timely completion of the projects done for Tellabs.

Education

M.Sc. in Wireless Communication Engineering (2011–2013), *University of Oulu* (Oulu, Finland)
Grade – Excellent (4.72), Thesis Topic: Self-interference channel and analog baseband cancellation for Full Duplex transceiver

B.E. in Electronics and Communication (2001–2005), *Delhi College of Engineering* (New Delhi, India)
First class with distinction (76.2 %), Thesis Topic: RTOS implementation on 8051 architecture

Skills

Skill Type	Skill	Level (1 – 5, with 5 being the highest)	Years used
Simulation Environment	MATLAB	4	8+
	Spectre	3	5+
High Level Language	C	4.5	10+
Hardware Description Language	System Verilog	2	1
Scripting Languages	Bash shell Scripting, Python	3	4
Operating System	Linux	3.5	7
	FreeRTOS	4.5	4
Tools & Packages	Cadence Virtuoso	4	5+
	Xilinx Platform Studio	3	1.5

Publications

- R. A. Shaheen, R. Akbar, **A. Sethi**, J. P. Aikio, T. Rahkonen, A. Pärssinen (2019). A fully integrated 4 × 2 element CMOS RF phased array receiver for 5G. Analog Integrated Circuits and Signal Processing.
- **A. Sethi**, J. P. Aikio, R. A. Shaheen, R. Akbar, Tmo Rahkonen, Aarno Pärssinen (2019). A four channel phased array transmitter using an active RF phase shifter for 5G wireless systems. Analog Integrated Circuits and Signal Processing.
- **A. Sethi**, R. Akbar, J. P. Aikio, R. A. Shaheen, A. Pärssinen, T. Rahkonen (2019). Designing at Millimeter-Wave: Lessons from a Triple Coil Variable Transformer.(NORCAS)
- **A. Sethi**, J. Rusanen, J. P. Aikio, A. Pärssinen, T. Rahkonen (2019). Broadband Linearization Technique for mmWave Circuits. (EuMIC).

- R. A. Shaheen, **A. Sethi**, R. Akbar, J. P. Aikio, T. Tuovinen, T. Rahkonen, A. Pärssinen (2018). A simultaneous wideband impedance matching and bandpass filtering technique using NUTL segments at 15~GHz (WiSNet).
- J. P. Aikio, **A. Sethi**, R. A. Shaheen, R. Akbar, T. Rahkonen, A. Pärssinen (2017). A fully integrated 13~GHz CMOS SOI stacked power amplifier for 5G wireless systems (NORCAS)
- R. A. Shaheen, R. Akbar, **A. Sethi**, J. P. Aikio, T. Rahkonen, A. Pärssinen (2017). A 45nm CMOS SOI, four element phased array receiver supporting two MIMO channels for 5G. (NORCAS)
- **A. Sethi**, J. P. Aikio, R. A. Shaheen, R. Akbar, T. Rahkonen, A. Pärssinen (2017). A 10mbox-bit active RF phase shifter for 5G wireless systems. (NORCAS)
- K. Rikkinen, V. Tapio, H. Alves, M. Al-Imari, A. C. Cirik, J. Seddar, **A. Sethi**, B. Debaillie, C. Lavin (2015). Full-duplex transmission in small area radio communication systems. (CAMAD)
- **A. Sethi**, V. Tapio, M. Juntti (2014). Self-interference channel for full duplex transceivers. (WCNC)
- W. Li, J. Lilleberg, **A. Sethi**, (2014) "Method and Apparatus for Reducing Self Interference", Patent application US 20140198688 A1.