ALOK SETHI

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Profile

- mmWave RFIC researcher with more than four years of experience in IC design.
- Excellent knowledge of IC CAD (Cadence Virtuoso), verification (Mentor Calibre) and modelling (Keysight Momentum) tools.
- More than eight years of experience in designing embedded systems.
- Well-versed with C, MATLAB and Linux (both kernel and user plane).
- Good working knowledge of Python, Verilog and Shell Scripting.
- Excellent academic record.

Experience

Doctoral Student (5/2015 – Present), ***Centre for Wireless Communications*** (Oulu, Finland)
CWC is a university based leading research institute in the field of wireless communication.
I am doing my PhD in analog integrated circuit design. My research focus is to design and develop novel transmitter architectures for 5th Generation of wireless systems. Since autumn 2015, I have done three successful tapeouts and am working towards a fourth one since summer 2019. My responsibilities include

- Circuit design and simulations for developing a phased array transceiver,
- Embedded software design and development,
- Measurement campaigns.

During this time, I have authored or co-authored more than twelve conference papers and two journal papers in international peer-reviewed publication venues. Further, I have a patent pending for one of the research results.

Project Researcher (10/2013 – 5/2015), ***Centre for Wireless Communications*** (Oulu, Finland)
My main task was to build a demonstrator that integrated both analog and digital cancellation solutions being developed by the various partners of an EU funded FP7 project called DUPLO. My responsibilities included

- Modifying the OFDM programmable core on Spartan 6 FPGA to support in-band Full Duplex physical layer,
- MATLAB simulations for developing a joint RF and baseband cancellation scheme for Full Duplex transceivers.

My biggest achievement was developing the Full Duplex demonstrator which was successfully exhibited during the project dissemination.

Research Assistant (10/2012 – 09/2013), ***Centre for Wireless Communications*** (Oulu, Finland)
I worked in the Communication Signal Processing group where I studied the self-interference channel for the Full Duplex transceiver. My responsibilities included

- Performing channel measurements using a vector network analyzer and developing a channel model for the same,
- Enhancing the MATLAB simulation model for analog baseband cancellation, developed during the summer internship.

One conference article in an international peer-reviewed conference was published from my research work.

Summer Intern (06/2012 – 09/2012), ***Renesas Mobile Europe*** (Oulu, Finland)
I performed MATLAB simulations for an analog baseband cancellation scheme targeted for Full Duplex transceiver. Further, a patent was filed for one of the research results.

Research Assistant (11/2011– 05/2012), ***Centre for Wireless Communications*** (Oulu, Finland)
I worked in the Wireless Sensor Networking lab, where I developed embedded software for STM32F207 microcontroller. My main responsibilities were

- Porting Contiki on STM3220G-EVAL evaluation board,
- Writing drivers for Ethernet, I2C, SPI, and FSMC and adding support for multiple radio drivers in Contiki.

Technical Leader (01/2010– 08/2011), ***VVDN*** (Gurgaon, India)
VVDN has a dedicated vision on embedded systems solution. It has strength of roughly 200 engineers.
I worked on the development of a TDMA wireless backhaul system using off the shelf WiFi cards, which was designed to be part of a carrier grade GSM network. My responsibilities included developing a transport and link layer for a TDMA over 802.11n WiFi system and modifying the Linux kernel to support synchronous operation.

Technical Leader (05/2005 – 01/2010), ***Aricent*** (Gurgaon, India)
Aricent is a product engineering services and software firm with more than 10,000 engineers worldwide. It has a dedicated focus on telecommunications.
At Aricent, I worked on three major projects. My responsibilities varied from a junior team member to a team leader of about ten software developers. My first project's client was Alvarion, where my main responsibilities were

- Designing, developing and testing a fault, performance and shelf manager for the WiMAX gateway,
- Integrating the embedded entity management system with the external management system.

Tellabs was the client for my last two projects, where my main responsibilities were

- Designing, developing and testing fast path on Cavium Network Processor,
- Optimizing the fast path for the best possible speed,

My biggest achievement at Aricent was establishing an expertise on Cavium Network Processor. My team was awarded an excellence award for the timely completion of the projects done for Tellabs.

Education

M.Sc. in Wireless Communication Engineering (2011–2013), *University of Oulu* (Oulu, Finland)
Grade – Excellent (4.72), Thesis Topic: Self-interference channel and analog baseband cancellation for Full Duplex transceiver

B.E. in Electronics and Communication (2001–2005), *Delhi College of Engineering* (New Delhi, India)
First class with distinction (76.2 %), Thesis Topic: RTOS implementation on 8051 architecture

Skills

Skill Type	Skill	Level (1 – 5, with 5 being the highest)	Years used
IC packages	Cadence Virtuoso	4	4+
	Mentor Calibre	3	4+
	Keysight Momentum	4	4+
Simulation Environment	MATLAB	4	7+
High Level Language	C	4.5	10+
	Python	2	1
Hardware Description Language	Verilog	2	1
	System Verilog	2	1
Scripting Languages	Ocean script	2	3+
	Bash shell Scripting	3	4
Operating System	Linux	3.5	7
	FreeRTOS	4.5	2
PCB Design	Eagle	2	1+
	KiCad	2	1+
Others	GCC, GDB	3.5	10+
	Xilinx Platform Studio	2	1.5
	Latex	3	6
	Microsoft Office Suite	4	14+
	Fusion 360	2	1+
	Git	2	1+
	SVN	3.5	8+

Languages

- **Hindi** (Mother Tongue)
- **English** (Proficient)
- **Finnish** (Basic)