ALON AMID

Computer Architecture, AI Hardware/Software System Design
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Computer architect and system designer with broad experience across the hardware/software boundary. Areas of expertise include artificial intelligence and machine learning acceleration, hyperscaler cloud systems, and the open-source silicon and RISC-V ecosystems. Holds a PhD in electrical engineering and computer sciences from the University of California, Berkeley.

EXPERIENCE

Microsoft Corp. August 2021 - Present
Senior Hardware Engineer *Haifa, Israel*

Artificial intelligence and machine learning acceleration in the Azure cloud.
Azure Hardware Architecture (AHA), Cloud Accelerated Systems and Technologies (CAST) group. Hybrid work in the Microsoft's Israel Development Center as part of a US-based team.
Activities include architectural modeling and definition, high-performance software kernel and firmware development, RTL development, system-level reliability availability and serviceability (RAS) analysis, end-to-end performance modeling and evaluation, performance profiling and benchmarking, large-scale cloud telemetry data analysis.

Microsoft Corp. May 2020 - August 2020
PhD Research Intern *Redmond, Washington (Remote)*

Microsoft Azure AI and Advanced Architectures.
Cloud-hosted FPGA acceleration for data analytics systems.

Google LLC May 2018 - August 2018
PhD Software Engineering Intern *Sunnyvale, California*

Google Cloud data-center platforms.
Far-memory latency analysis and mitigation using machine-learning-based prediction.

University of California, Berkeley August 2016 - August 2021
PhD Graduate Student Researcher *Berkeley, California*

Affiliated with the ASPIRE Lab, ADEPT Lab, and the Berkeley Wireless Research Center.
Development of open-source generator-based simulation and hardware design frameworks within the RISC-V ecosystem, including FireSim (distributed FPGA-accelerated simulation), Chipyard (integrated SoC design framemork), and Gemmini (machine learning accelerator generator).
Research in parallel computing, accelerated computing, and open-source chip design, including related activities and working group participation within the RISC-V ecosystem.

Qualcomm Inc. 2015 - 2016
PHY ASIC Digital Design Engineer *Haifa, Israel*

Digital hardware design of Wi-Fi IEEE 802.11ad (WiGig) physical layer (PHY). High rate multi Gbps wireless communication chipset in the 60 GHz frequency band.
RTL implementations of Matlab algorithms, RTL design of generic DSP modules/functions, configurable debug features, 1x1 bit-exact verification environment setups and stub implementations.

Infosys Ltd. July 2013 - September 2013
Research Intern *Bangalore, India*

Infosys Instep Global Internship Program in Bangalore, India. Work in a large enterprise multi-cultural international environment. Project conducted with the Infosys Labs R&D unit.

"Hybrid Access Control Based Solution for Cloud Services" research project. Designing a new access control model and applying it using Cipher-text Policy Attribute-Based Encryption (CP-ABE).

Unit 8200 - IDF (Israel Defense Forces) 2008-2012
Military Service - Officer (Honorable discharge as a lieutenant.) *Israel*

2011-2012: Intelligence Staff Officer - strategic planning, analysis and product development of large scale and long term intelligence technology projects. Coordination with organizations across the IDF.
2009-2011: Intelligence System Officer - Responsibility for an operational intelligence analysis system, including characterization for future development and implementation. Commander of a team in charge of developing expert-system automatic intelligence analysis processes.

B.M. Carmel Ltd. 2007-2008
Network Administrator *Nesher, Israel*

Small business network administration, including "Priority" ERP system support and administration. New overseas facility computer network set-up and ERP training in Bennington, VT.

EDUCATION

University of California, Berkeley *Graduated 2021*
Ph.D in Electrical Engineering and Computer Sciences
-Research areas: computer architecture and engineering, energy-efficient data-parallel processors, linear-algebra and machine learning acceleration, heterogeneous and distributed systems, RISC-V systems, system-on-chip design methodologies.
-Dissertation topic: Generator-Based Design of Custom Systems-on-Chip for Numerical Data Analysis
-Demetri Angelakos Memorial Achievement Award (2020-2021).
-Service/Leadership: Treasurer (2 years) and President (1 year) of the Electrical Engineering Graduate Student Association. EECS Delegate to the UC Berkeley Graduate Assembly.

University of California, Berkeley *Graduated 2019*
M.Sc. in Electrical Engineering and Computer Sciences
-Thesis topic: Nested-Parallelism PageRank on RISC-V Vector Multi-Processors

Technion - Israel Institute of Technology *Graduated 2016*
B.Sc. in Electrical Engineering
-Graduated Cum-Laude. Overall GPA: 92.5
-Student Exchange semester in the University of Melbourne (Australia)
-Undergraduate research project on clock-power consumption analysis and optimization of GALS partitioned SoC architectures in the VLSI Systems Research Center

SKILLS AND INTERESTS

Interests	Computer Architecture, Machine Learning, Parallel Computing, RISC-V, Specialized Accelerator Design, Distributed Systems, Energy Efficient Computing, Design Methodology and Automation
Computer Languages	C, C++, Python, Matlab, R, Verilog, VHDL, CUDA, Bash, SQL, RISC-V Assembly, Scala, Chisel/FIRRTL
Languages	Hebrew (Native), English (Native)
Cross-Cultural Experience	Visited over 50 countries across 6 continents, multiple relocations
Music	Trumpet playing in the Technion Symphony and Wind Orchestras

TEACHING

Undergraduate Capstone Project Advising Fall 2022 - Present
Adjunct Teaching Fellow *Technion - Israel Institute of Technology*

Advising undergraduate students in capstone projects in the Electrical and Computer Engineering (ECE) department. Projects focus on areas of computer architecture, parallel computing, high performance computing, and machine learning.

EE290-2 - Hardware for Machine Learning Spring 2020
Graduate Student Instructor *University of California, Berkeley*

Content development and project advising for the inaugural offering of a graduate-level course.
Three hands-on labs: DNN model quantization, design of a systolic-array accelerator in Verilog (with integration into a RISC-V SoC), and software optimization and scheduling for the accelerator.
`https://inst.eecs.berkeley.edu/~ee290-2/sp20/`

CS162 - Operating Systems and System Programming Fall 2018
Graduate Student Instructor *University of California, Berkeley*

Lead discussion sections and project advising for an upper-division undergraduate course.
`https://inst.eecs.berkeley.edu/~cs162/fa18/`

Madatech - Israel National Museum of Science 2004-2007
Science Youth Guide *Haifa, Israel*

Explanation of scientific exhibits and instruction of youth activities in the museum.

ACADEMIC PUBLICATIONS

1. Alon Amid, Hasan Genc, Jerry Zhao, Krste Asanović, Borivoje Nikolić, and Yakun Sophia Shao. Accelerating general-purpose linear algebra on dnn accelerators. In *1st Workshop on Democratizing Domain-Specific Accelerators (WDDSA 2022), co-located with the 55th IEEE/ACM International Symposium on Microarchitecture, Chicago, Illinois, USA, October 2nd, 2022*, 2022

2. Abraham Gonzalez, Jerry Zhao, Ben Korpan, Hasan Genc, Colin Schmidt, John Wright, Ayan Biswas, Alon Amid, Farhana Sheikh, Anton Sorokin, Sirisha Kale, Mani Yalamanchi, Ramya Yarlagadda, Mark Flannigan, Larry Abramowitz, Elad Alon, Yakun Sophia Shao, Krste Asanović, and Borivoje Nikolić. A 16mm^2 106.1 GOPS/W heterogeneous RISC-V multi-core multi-accelerator SoC in low-power 22nm FinFET. In *47th IEEE European Solid State Circuits Conference, ESSCIRC 2021, Grenoble, France, September 6-9, 2021*. IEEE, 2021

3. David Biancolin, Albert Magyar, Sagar Karandikar, Alon Amid, Borivoje Nikolić, Jonathan Bachrach, and Krste Asanović. Accessible, FPGA resource-optimized simulation of multi-clock systems in firesim. *IEEE Micro*, 41(4):58–66, 2021

4. Alon Amid, Albert Ou, Krste Asanović, Yakun Sophia Shao, and Borivoje Nikolić. Vertically integrated computing labs using open-source hardware generators and cloud-hosted fpgas. In *Proceedings of the 2021 International Symposium on Circuits and Systems (ISCAS)*, 2021

5. Jerry Zhao, Abraham Gonzalez, Alon Amid, Sagar Karandikar, and Krste Asanović. Cobra: A framework for evaluating compositions of hardware branch predictors. In *Proceedings of the 2021 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pages 310–320. IEEE, 2021

6. Nathan Pemberton and Alon Amid. Firemarshal: Making hw/sw co-design reproducible and reliable. In *Proceedings of the 2021 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pages 299–309. IEEE, 2021

7. Hasan Genc, Seah Kim, Alon Amid, Ameer Haj-Ali, Vighnesh Iyer, Pranav Prakash, Jerry Zhao, Daniel Grubb, Harrison Liew, Howard Mao, Albert Ou, Colin Schmidt, Samuel Steffl, John Wright, Ion Stoica, Jonathan Ragan-Kelley, Krste Asanovic, Borivoje Nikolic, and Yakun Sophia Shao. Gemmini: Enabling systematic deep-learning architecture evaluation via full-stack integration. In *Proceedings of the 58th Annual Design Automation Conference (DAC),* ***Best Paper Award***, pages 769–774, 2021

8. Alon Amid, David Biancolin, Abraham Gonzalez, Daniel Grubb, Sagar Karandikar, Harrison Liew, Albert Magyar, Howard Mao, Albert Ou, Nathan Pemberton, Paul Rigge, Colin Schmidt, John Wright, Jerry Zhao, Yakun Sophia Shao, Krste Asanović, and Borivoje Nikolić. Chipyard: Integrated design, simulation, and implementation framework for custom SoCs. *IEEE Micro*, 40(4):10–21, 2020

9. Alon Amid, David Biancolin, Abraham Gonzalez, Daniel Grubb, Sagar Karandikar, Harrison Liew, Albert Magyar, Howard Mao, Albert Ou, Nathan Pemberton, Paul Rigge, Colin Schmidt, John Wright, Jerry Zhao, Jonathan Bachrach, Yakun Sophia Shao, Borivoje Nikolić, and Krste Asanović. Chipyard - an integrated soc research and implementation environment. In *Proceedings of the 57th ACM/EDAC/IEEE Design Automation Conference (DAC)*, pages 1–6. IEEE, 2020

10. Colin Schmidt, Alon Amid, John Wright, Ben Keller, Howard Mao, Keertana Settaluri, Jarno Salomaa, Jerry Zhao, Albert Ou, Krste Asanović, and Borivoje Nikolić. Programmable fine-grained power management and system analysis of RISC-V vector processors in 28nm FD-SOI. *IEEE Solid-State Circuits Letters*, 3:210–213, 2020

11. Sagar Karandikar, Albert Ou, Alon Amid, Howard Mao, Randy Katz, Borivoje Nikolić, and Krste Asanović. FirePerf: FPGA-Accelerated Full-System Hardware/Software Performance Profiling and

Co-Design. In *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS 20, page 715731, New York, NY, USA, 2020. Association for Computing Machinery

12. Alon Amid, Kiseok Kwon, Amir Gholami, Bichen Wu, Krste Asanović, and Kurt Keutzer. Co-Design of Deep Neural Nets and Neural Net Accelerators for Embedded Vision Applications. *IBM Journal of Research and Development*, 63(6):6:1–6:14, 2019

13. Hasan Genc, Ameer Haj-Ali, Vighnesh Iyer, Alon Amid, Howard Mao, John Wright, Colin Schmidt, Jerry Zhao, Albert Ou, Max Banister, Yakun Sophia Shao, Borivoje Nikolić, Ion Stoica, and Krste Asanović. Gemmini: An Agile Systolic Array Generator Enabling Systematic Evaluations of Deep-Learning Architectures, 2019

14. Alon Amid, Albert Ou, Krste Asanović, and Borivoje Nikolić. Nested-Parallelism PageRank on RISC-V Vector Multi-Processors. In *Third Workshop on Computer Architecture Research with RISC-V (CARRV 2019), Co-located with ISCA 2019*, CARRV 19, 2019

15. Sagar Karandikar, David Biancolin, Alon Amid, Nathan Pemberton, Albert Ou, Randy Katz, Borivoje Nikolić, Jonathan Bachrach, and Krste Asanović. Using FireSim to Enable Agile End-to-End RISC-V Computer Architecture Research. In *Third Workshop on Computer Architecture Research with RISC-V (CARRV 2019), Co-located with ISCA 2019*, CARRV 19, 2019

16. Alon Amid. Nested-Parallelism PageRank on RISC-V Vector Multi-Processors. Master's thesis, EECS Department, University of California, Berkeley, Apr 2019

17. Sagar Karandikar, Howard Mao, Donggyu Kim, David Biancolin, Alon Amid, Dayeol Lee, Nathan Pemberton, Emmanuel Amaro, Colin Schmidt, Aditya Chopra, Qijing Huang, Kyle Kovacs, Borivoje Nikolić, Randy Katz, Jonathan Bachrach, and Krste Asanović. FireSim: FPGA-Accelerated Cycle-Exact Scale-Out System Simulation in the Public Cloud. *IEEE Micro (**Top Picks from Computer Architecture Conferences**)*, 39(3):56–65, 2019

18. Kiseok Kwon, Alon Amid, Amir Gholami, Bichen Wu, Krste Asanović, and Kurt Keutzer. Co-Design of Deep Neural Nets and Neural Net Accelerators for Embedded Vision Applications. In *Proceedings of the 55th Annual Design Automation Conference*, DAC 18, New York, NY, USA, 2018. Association for Computing Machinery

19. Sagar Karandikar, Howard Mao, Donggyu Kim, David Biancolin, Alon Amid, Dayeol Lee, Nathan Pemberton, Emmanuel Amaro, Colin Schmidt, Aditya Chopra, Qijing Huang, Kyle Kovacs, Borivoje Nikolic, Randy Katz, Jonathan Bachrach, and Krste Asanović. FireSim: FPGA-Accelerated Cycle-Exact Scale-out System Simulation in the Public Cloud. In *Proceedings of the 45th Annual International Symposium on Computer Architecture*, ISCA 18, page 2942. IEEE Press, 2018

20. Alon Amid and Borivoje Nikolić. Preventing Babel: Rectifying the Trend of Programming Language Divergence. In *The 8th Workshop on Evaluation and Usability of Programming Languages and Tools (PLATEAU) at SPLASH 2017*, PLATEAU 17, 2019

21. Vijayaraghavan Varadharajan, Alon Amid, and Sudhanshu Rai. Policy based Role Centric Attribute Based Access Control Model Policy RC-ABAC. In *2015 International Conference on Computing and Network Communications (CoCoNet)*, pages 427–432, 2015

ACADEMIC TUTORIALS

Tutorial on FireSim and Chipyard: End-to-End Architecture Research with RISC-V SoC Generators, Agile Test Chips, and FPGA-Accelerated Simulation on Amazon EC2 F1
June 2021
48th IEEE/ACM International Symposium on Computer Architecture *Online*

Jerry Zhao, Abraham Gonzalez, Sagar Karandikar, Harrison Liew, Nathan Pemberton, Albert Ou, Alon Amid

Tutorial on FireSim and Chipyard: End-to-End Architecture Research with RISC-V SoC Generators, Agile Test Chips, and FPGA-Accelerated Simulation on Amazon EC2 F1
December 2019
2019 RISC-V Summit *San Jose, California*

Jerry Zhao, Abraham Gonzalez, David Biancolin, Alon Amid, Colin Schmidt

Tutorial on FireSim and Chipyard: End-to-End Architecture Research with RISC-V SoC Generators, Agile Test Chips, and FPGA-Accelerated Simulation on Amazon EC2 F1
October 2019
52nd IEEE/ACM International Symposium on Microarchitecture *Columbus, Ohio*

Jerry Zhao, Howard Mao, Abraham Gonzalez, John Wright, Sagar Karandikar, David Biancolin, Nathan Pemberton, Albert Ou, Alon Amid
https://fires.im/micro-2019-tutorial/

Tutorial: Easy-to-use, FPGA-Accelerated Hardware Simulation of RISC-V Hardware Designs with FireSim on Amazon EC2 F1 December 2018
2018 RISC-V Summit *Santa Clara, California*

Sagar Karandikar, David Biancolin, Alon Amid

FireSim Intensive Tutorial November 2018
1st Chisel Community Conference *Berkeley, California*

Sagar Karandikar, David Biancolin, Alon Amid