1. Description

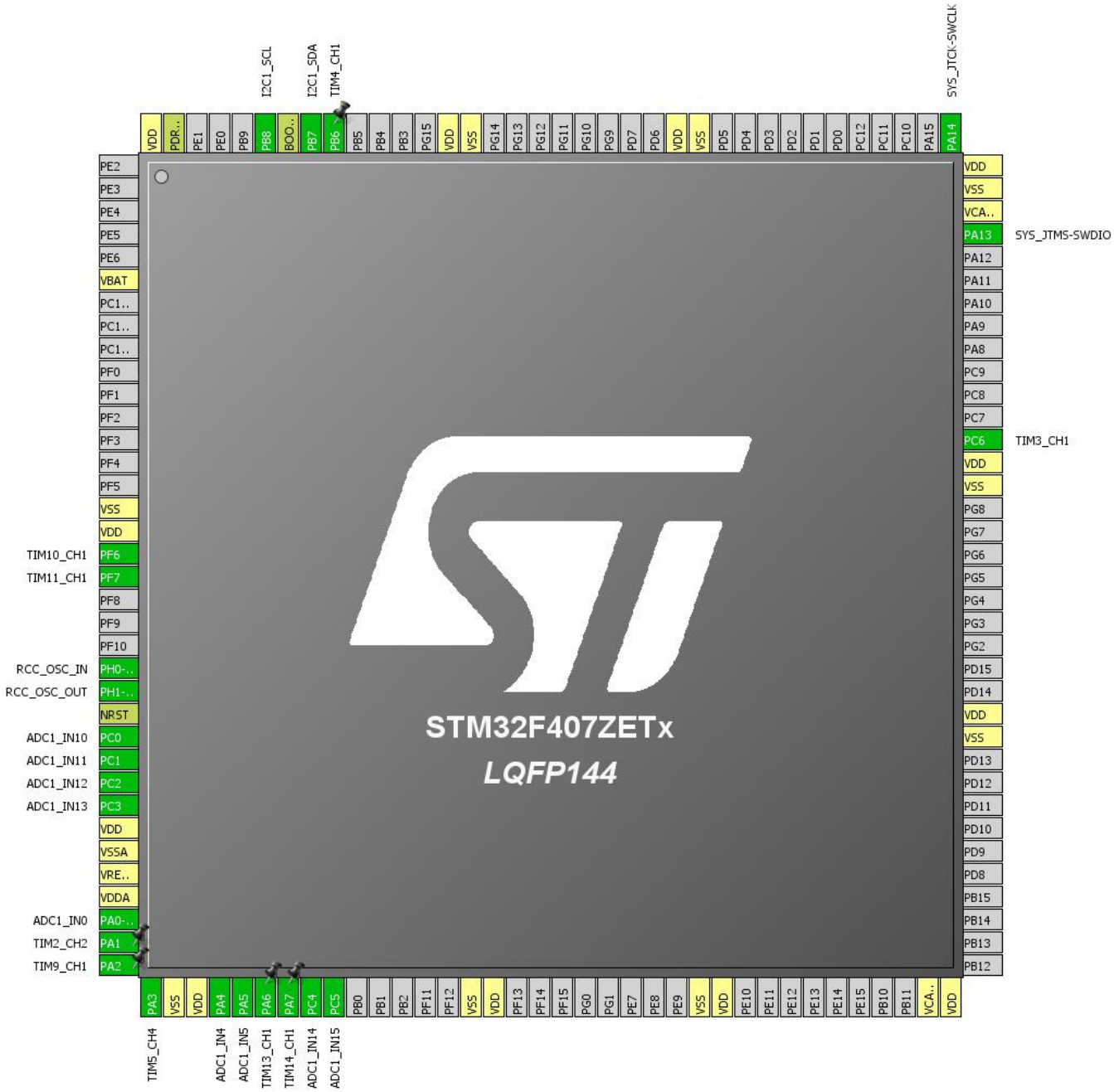
1.1. Project

Project Name	stm32f407_ir
Board Name	stm32f407_ir
Generated with:	STM32CubeMX 4.22.0
Date	09/01/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

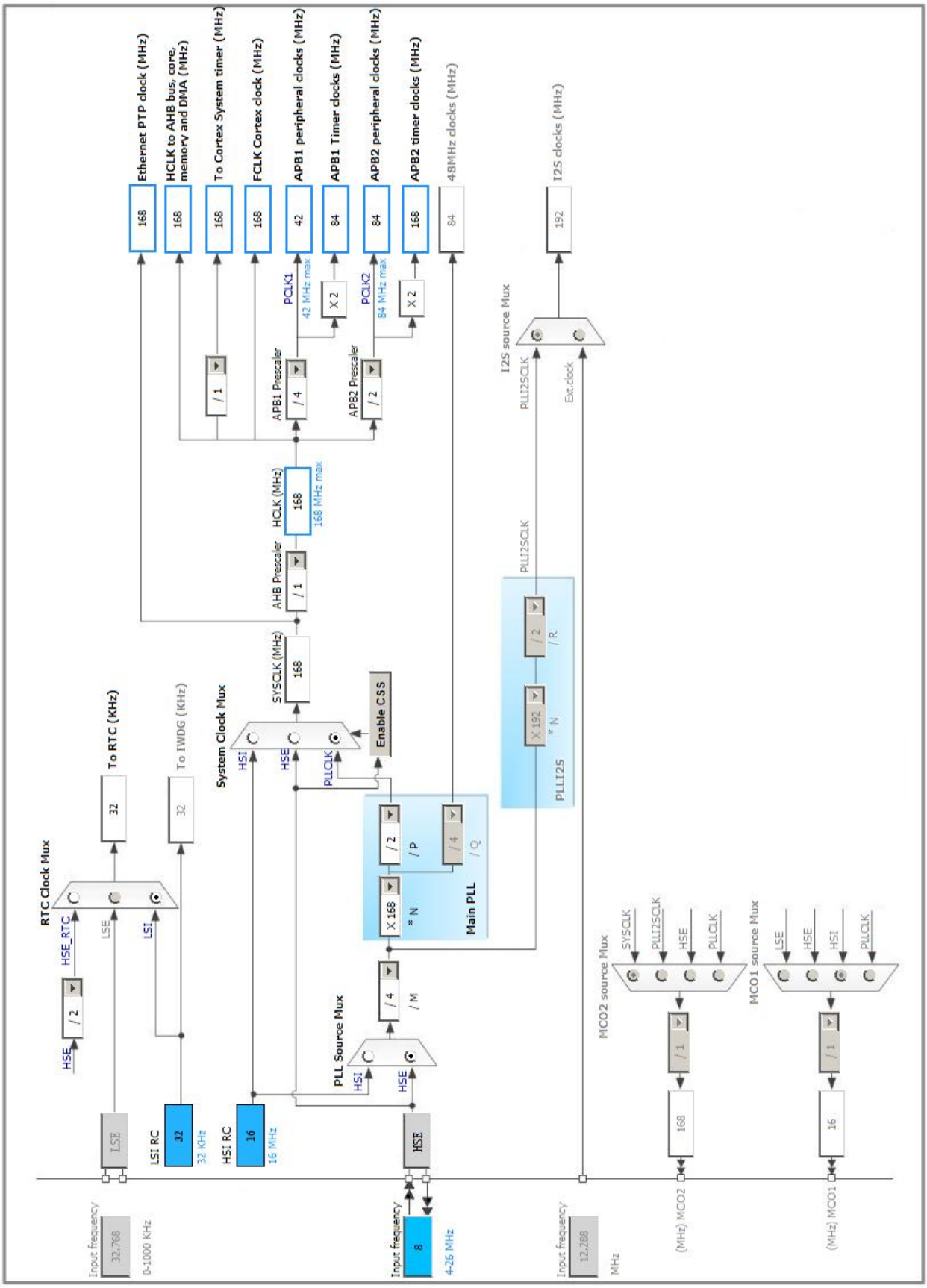


3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	TIM10_CH1	
19	PF7	I/O	TIM11_CH1	
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN10	
27	PC1	I/O	ADC1_IN11	
28	PC2	I/O	ADC1_IN12	
29	PC3	I/O	ADC1_IN13	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	ADC1_IN0	
35	PA1	I/O	TIM2_CH2	
36	PA2	I/O	TIM9_CH1	
37	PA3	I/O	TIM5_CH4	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_IN4	
41	PA5	I/O	ADC1_IN5	
42	PA6	I/O	TIM13_CH1	
43	PA7	I/O	TIM14_CH1	
44	PC4	I/O	ADC1_IN14	
45	PC5	I/O	ADC1_IN15	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	TIM3_CH1	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
136	PB6	I/O	TIM4_CH1	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
139	PB8	I/O	I2C1_SCL	
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0
mode: IN4
mode: IN5
mode: IN10
mode: IN11
mode: IN12
mode: IN13
mode: IN14
mode: IN15

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**9 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	**480 Cycles ***
Rank	**2 ***
Channel	**Channel 4 ***
Sampling Time	**480 Cycles ***

Rank	**3 ***
Channel	**Channel 5 ***
Sampling Time	**480 Cycles ***
Rank	**4 ***
Channel	**Channel 10 ***
Sampling Time	**480 Cycles ***
Rank	**5 ***
Channel	**Channel 11 ***
Sampling Time	3 Cycles
Rank	**6 ***
Channel	**Channel 12 ***
Sampling Time	3 Cycles
Rank	**7 ***
Channel	**Channel 13 ***
Sampling Time	3 Cycles
Rank	**8 ***
Channel	**Channel 14 ***
Sampling Time	3 Cycles
Rank	**9 ***
Channel	**Channel 15 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	**0x29 ***
General Call address detection	Disabled

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM2

Channel2: Input Capture direct mode

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0

Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.6. TIM3

Channel1: Input Capture direct mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.7. TIM4

Channel1: Input Capture direct mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.8. TIM5

Channel4: Input Capture direct mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.9. TIM9

Channel1: Input Capture direct mode

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.10. TIM10

mode: Activated

Channel1: Input Capture direct mode

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.11. TIM11

mode: Activated

Channel1: Input Capture direct mode

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.12. TIM13

mode: Activated

Channel1: Input Capture direct mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**167 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.13. TIM14

mode: Activated

Channel1: Input Capture direct mode

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Input Capture Channel 1:

Polarity Selection	Rising Edge

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM9	PA2	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM10	PF6	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM11	PF7	TIM11_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM13	PA6	TIM13_CH1	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
TIM14	PA7	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407ZETx
Datasheet	022152_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	stm32f407_ir
Project Folder	C:\Users\alongkun\Desktop\stm32f407_ir
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No