Electronic Technology
Electronic systems, 3rd course
Bachelor in telecommunication technologies engineering,
Telematics Engineering, Sound and Image Engineering and Mobile and Space Communications Engineering
Ordinary Exam, January 13th 2022

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EXAM GUIDELINES (Answers submitted that do not follow to what is indicated in these guidelines will not be graded)

- The exam last **a maximum of 3 hours**.
- The exam consists of these instructions and **a case study divided into 4 sections**, distributed over 5 sheets (9 pages).
- The score and estimated completion time are indicated in the title of each section of the exam.
- **It is mandatory to write the name, surname and group** in which the student is enrolled **on this first page of the exam statement (EXAM GUIDELINES), at the beginning of it**.
- Along with the statement, **each student will have blank sheets** to answer **all parts of the exam**, and to carry out calculations and drafts. **All these sheets must include the name, surname and group of the student, at the beginning of the exam**.
- **All parts of the exam will be answered on blank sheets**. **Section 2** must also include **the Bode Plot Diagram** available at the end of the exam statement, with the student's name, surname and group, even if it is blank.
- **Each section will be answered on separate sheets**.
- At the end of the exam, the student **MUST DELIVER THE EXAM STATEMENT and AT LEAST 1 SHEET FOR EACH SECTION, WITH THE PART TITLE AND YOUR ANSWER (even if the answer to the section is blank)**.
- **IN ALL THE ANSWERS TO THE QUESTIONS OF THE EXAM IS MANDATORY TO INCLUDE AN EXPLANATION** (THE DIRECT APPLICATION OF FORMULAS WITHOUT DEDUCTION OR EXPLANATION IS NOT VALID, EXCEPT THOSE EXPRESSLY INDICATED IN THE STATEMENT) **AND THE JUSTIFICATION OF ALL THE APPROXIMATIONS CARRY OUT** FOR THE REQUESTED CALCULATIONS.
- Each question **must be answered in a clear, clean and orderly manner**, avoiding amendments and crossing-outs in the exam answers.

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Figure 1 shows the diagram of an electronic instrumentation system that is used for the signal conditioning of the variation of the electrical magnitude of a sensor (variation of the capacitance as a function of the variation of a physical magnitude) and transform it into a voltage signal that It can already be used by the analog to digital converter (ADC) and finally interpreted by the microprocessor (µP).

The instrumentation system consists of a sinusoidal LC oscillator, which will generate a voltage (V_s) whose frequency will change as the physical magnitude and, therefore, the equivalent capacitance of the sensor varies. Then an amplifier will be used whose output (V_{in}) will have an amplitude adapted for the input of an integrated multiplier (AD633). This multiplier is used as a phase detector in a PLL, in whose output (V_e) the information of the physical magnitude enclosed in the frequency of the oscillator is recovered.

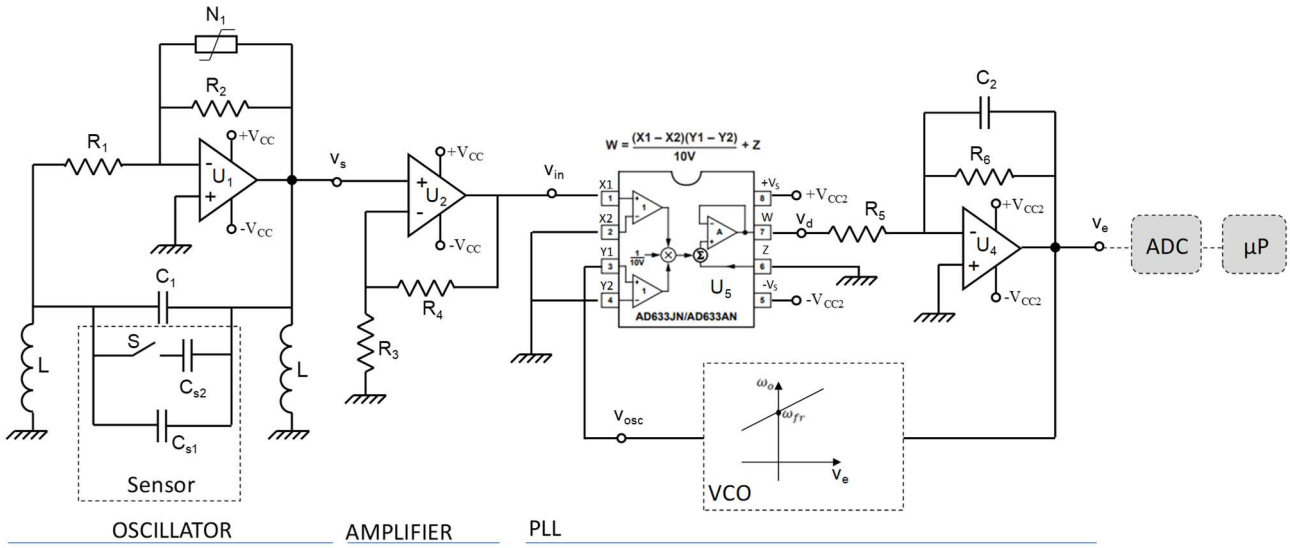

Figure 1: Electronic instrumentation system for signal conditioning of a capacitive sensor.

In Figure 2, the electronic power supply system is shown, which provides the different supply voltages $\pm V_{CC}$ and $\pm V_{CC2}$, starting from the voltage of the electrical network. The unregulated voltage provided by the rectifier, V_{NR}, will be regulated in two steps, using switched and linear voltage regulators. As bipolar supply voltages are required, the supply structure with positive and negative regulators has been duplicated, although **only the positive ones will be analyzed**.

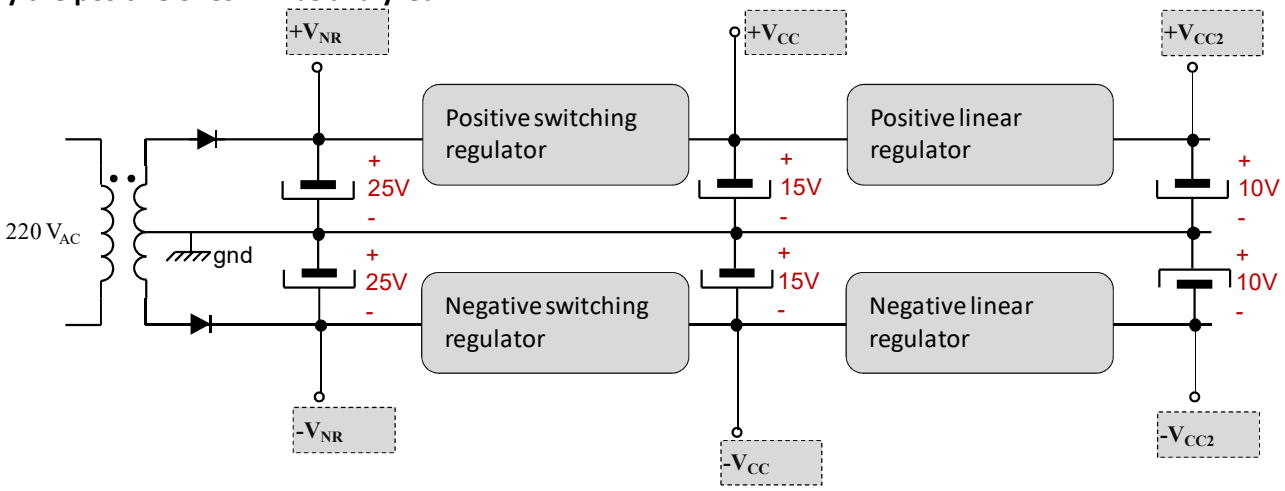

Figure 2: Electronic power supply system to generate the different voltages $\pm V_{CC}$ and $\pm V_{CC2}$.

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The first conversion step (from 25V to 15V) is performed by a step-down switching voltage regulator, and the second step (from 15V to 10V) is performed by a linear voltage regulator. Both circuits are shown in Figure 5 (in Sectiont 4 of the system).

SECTION 1 (40 minutes, 2.5 points)

Analysis of the oscillator that generates the voltage Vs in Figure 1.

DATA:

- The non-linear network, N_1, manages to stabilize the RMS output voltage of the oscillator (Vs) at 1V.
- U_1, real operational amplifier:
  - R_i = 10 MΩ (assume infinity)
  - R_O = 100 mΩ (closed-loop output impedance)
  - Gain-Bandwidth product: 6 MHz
  - Slew rate: 16 V/µs
- R_1 = 100 kΩ
- L = 650 µH
- The sensor has a capacity, which varies between two values:
  - $C_{min} = C_{s1}$ = 240 pF. Switch S open.
  - $C_{max} = C_{s1} + C_{s2}$= 240 pF + 85 pF = 325 pF. Switch S close.
- The oscillator is intended to provide a minimum frequency of oscillation of 200 kHz.

Give a reasoned answer to the following questions:

1. Draw the equivalent circuit representing the loop gain of the oscillator and obtain the expression for the frequency response of the loop gain of the oscillator (T(jω)). Justify all the approximations you make in the calculations.
2. Derive the expressions for the frequency of oscillation and the starting-up and steady-state conditions of the oscillator.
3. Determine the value of capacitor C_1. What will be the maximum oscillation frequency?
4. Justify whether the Op Amp U_1 is suitable to implement the oscillator taking into account its Gain-Bandwidth product and Slew-rate characteristics.

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SECTION 2 (50 minutes, 3 points)

Analysis of the amplifier connecting the voltages V_s and V_{in} in Figure 1.

DATA:

- The operational amplifier U1 is considered to have zero output impedance.
- The AD633 analog multiplier presents an input impedance composed of a resistance R_{AD} = 10 MΩ in parallel with a capacity C_{AD} = 50 pF between terminals X1 and X2 of U5.
- The operational amplifier U2 has the following characteristics:
  - $R_i = 10^{12}\Omega$;
  - $R_o = 318\Omega$;
  - $A_{AO}(jf) = \frac{10^5}{\left(1+j\frac{f}{10\times10^3}\right)\left(1+j\frac{f}{1\times10^6}\right)}$; *f* in Hz.
- R_3 = 100 kΩ
- The amplifier must provide a **RMS** output voltage (V_{in}) of 5V.

Give a reasoned answer to the following questions:

5. Identify the feedback topology type of the amplifier and determine the parameters of the β feedback network. Determine the value of resistor R_4 assuming that the loop gain of the feedback amplifier at mid frequencies satisfies $A_m \cdot \beta >> 1$.
6. Draw the equivalent circuit of network A', including the effect of the capacitive load which introduces the input capacity of the AD 633, C_{AD}.
7. Determine the transfer function A' (s) and calculate the pole (additional to the two of the operational amplifier) introduced in A' (s) by the input capacitance of the AD633, C_{AD}.
8. Obtain A'(jf) and plot the corresponding Bode plot. If you have not solved the previous sections, consider that C_{AD} introduces a pole in A'(jf) at a frequency of 10 MHz.
9. Check the stability of the feedback amplifier connected to the analog multiplier. In case it is unstable, calculate the frequency of the dominant pole that needs to be introduced in the transfer function of the Operational Amplifier U2, so that the feedback amplifier becomes stable with a phase margin of 45º.

Note: The student must use the templates for the representation of the Bode Plots, which are provided at the end of the statement of the exam. The student must deliver the sheet of Bode's Plots, with his name, surname and enrollment group.

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SECTION 3 (50 minutes, 2.5 points)

Analysis of the PLL that generates the output voltage Ve.

DATA:

- Consider that when the PLL is locked, the AD633 analog multiplier has a characteristic as a phase detector that is given by Figure 3a). In Figure 3b) the characteristic of the VCO is represented as well.

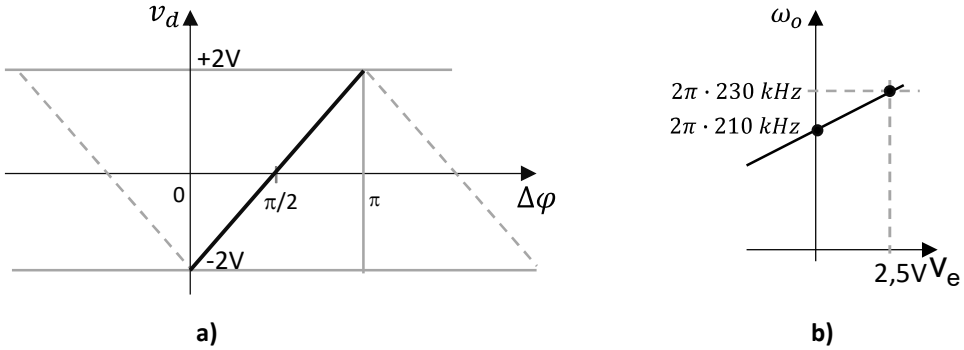

Figure 3: Characteristics of the AD633 as a phase detector and of the VCO.

Give a reasoned answer to the following questions:

10. Determine las constantes características del detector de fase (K_d) y del VCO (K_o).
11. Calculate the transfer function of the input voltage of the VCO (V_e), with respect to the frequency variation of the input signal ($\Delta\omega_i$) in relation to the free oscillation frequency of the VCO, assuming that the PLL remains locked.

If you have not solved the previous section, consider that the transfer function of the PLL is given by: $\frac{v_e}{\Delta\omega_i}(s) = \frac{1}{K_o} \cdot \frac{\omega_p \cdot K_V}{s^2 + \omega_p \cdot s + \omega_p \cdot K_V}$ where ω_p is the cutoff frequency of the filter and K_V is the loop gain of the PLL.

12. Determine the value of the cutoff frequency of the low-pass filter at the output of the AD633, so that the residual voltage at the output of the phase detector is attenuated by at least 30 dBs. Consider that the possible frequencies of the input voltage will be close to the free oscillation frequency of the VCO.
13. Design R_5, R_6 y C_2, to comply with question 12 and that the damping factor of the closed-loop PLL is: ζ=0,55.
14. Draw schematically the evolution in time of the input voltage of the VCO, Ve, if the switch that emulates the behavior of the sensor has a temporal variation as shown in Figure 4, and taking into account the notes indicated below of Figure 4.

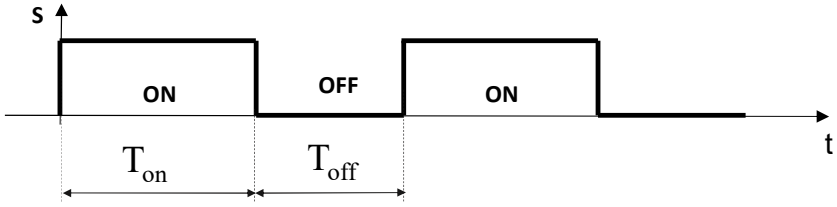

Figure 4: Time evolution of the opening and closing of the switch which emulates the operation of the sensor.

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Notes:

- Consider: Ton = 0,4 ms, Toff = 0,3 ms.
- Remember that the settle time of a second order system is given by the expression: $t_s = \frac{\pi}{\zeta \cdot \omega_n}$, where ζ is the damping factor and ω_n is the natural frequency of the second order system.

SECTION 4 (30 minutes, 2 points)

Analysis of the power supply system (positive voltage regulators).

DATA:

- L_b = 250 µH
- Carrier signal frequency, v_{carr}: f_{sw} = 400 kHz

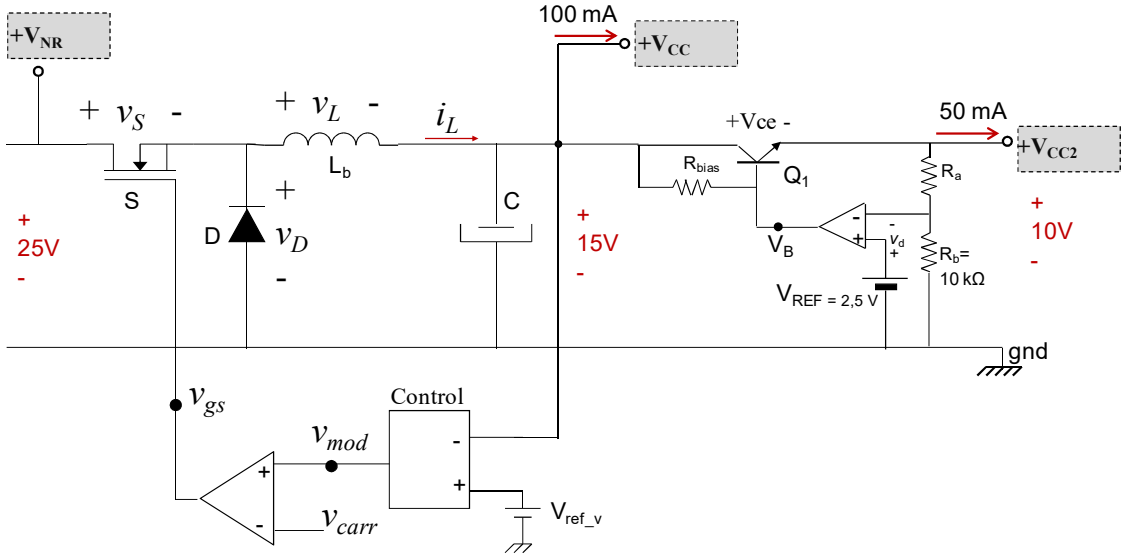

Figure 5: Schematic of the positive voltage regulators, capable of providing $+V_{CC}$ y $+V_{CC2}$ voltages of +15V and +10V starting from unregulated voltage V_{NR}.

Give a reasoned answer to the following questions:

15. Determine what is the duty cycle of the signal v_{gs} that controls the main MOSFET M_1.
16. Calculate the average current in the inductance, i_L. Calculate the peak-to-peak ripple of the current in the inductance and draw its waveform, with appropriate dimensions in Amperes and Microseconds.
17. Calculate the resistance R_a, so that the output voltage, $+V_{CC2}$, is the required 10V.
18. Calculate the efficiency of the linear voltage regulator.

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