Exercise 1 (60 min, 5 pto).

The diagram in the figure shows the physical scheme of a digital circuit.

a) Obtain the transistors scheme from the figure layout.

b) Obtain the status of the P and N transistors (On and Off) for the following two combinations ABCD={0101,1011}. Do not consider transistors in the inverters. Name the transistors from left to right and from top to bottom (also in the scheme of section a).

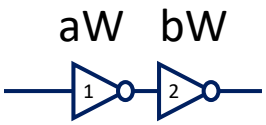
c) Specify the simplified logic function of OUT based on inputs (A, B, C, and D).

d) Get the cross-section view of the XY cut.

e) Could you replace some part of the scheme using pass transistors without getting degradation? Specify which transistor could be replaced and why.

Exercise 2 (40 min, 2.5p)

If the delay produced by inverters of minimum size (transistors with dimensions L and W) is, $t_{pi} = ln2 \cdot R_{eq} \cdot C_g$, deduce the delay that appears in an inverter (1) of size W'=aW, connected to another inverter (2) of size W'=bW (a and b constants).



b) We want to build a chain of inverters of increasing size to minimize the delay caused by a capacity 300 times greater than the capacity of a minimum size inverter (C_L = 300C_g). If we want to get the minimum possible delay, calculate:

- Number of stages required
- Size increase factor between stages
- Total delay, based on the delay of the minimum size inverter
- Estimation of total area, based on the area of the minimum size inverter
- Dimensions (L, W) of the transistors of the first three inverters of the chain, assuming that the dimensions of the transistors of the minimum size inverter are:

$$L_n = L_p = 2\lambda \quad W_n = 6\lambda \quad W_p = 15\lambda$$

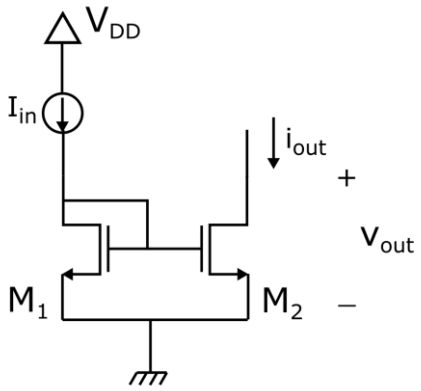
c) We want to design a clock tree for a circuit of 1200 flip-flops. To design this tree:

- only inverters of minimum size must be used
- it needs several stages (forks), and that all stages should have approximately the same *fanout*
- clock input pin must have *fanout* 1 (there must be only one inverter at the input pin)
- the clock reaching the flip-flops must have an even number of inversions

Draw the resulting trees for 3 and 4 stages and calculate their delay.

Exercise 3 (40 min, 2.5p)

The following current mirror has been implemented making use of a 50nm CMOS node. Given the following features and size ratios, answer the questions:



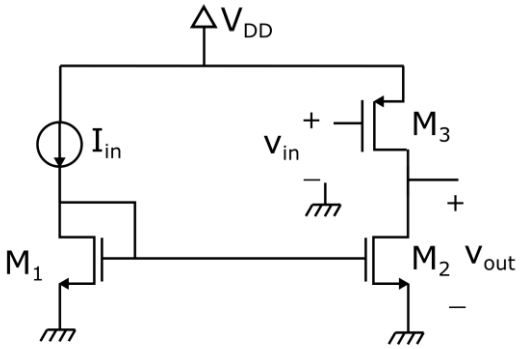
	NMOS	PMOS
μ*Cox (μA/V²)	100	50
λ (V⁻¹)	0.6	0.6
V_{th} (V)	0.28	-0.28

I_{in} = 20 μA, V_{DD} = 0.8 V
L = 100 nm for all the transistors

	W/L
M_1	10

Assume all the transistors of the exercise are biased in saturation.

a) Select proper values for W and L in transistor M_2 to make i_{out} equal to 100 μA.
b) Compute the output resistance of the current mirror.
c) Justify why the same current mirror but implemented in a bigger CMOS node (such as 800nm) would have a higher output resistance.
d) How could you increase the output resistance? With that purpose in mind, redesign and draw a new current mirror by adding one single extra transistor M_3 of size ratio W/L equal to 20. Assume that the gate of M_3 is connected to a voltage V_{bias}, sufficiently high to make it work in saturation. Compute the new output resistance.
e) Compute the gain $|A_v| = |V_{out}/V_{in}|$ of the following circuit, where (W/L) M_3 = 20 (this section is totally independent with respect to section d))



NOTE: All the answers must be justified. Answers either with no justification or incorrect justification will not be scored.