Problem 1 (90 min, 10ptos.)

We want to design a low-pass FIR filter with the following difference equation:

$$y(n) = a_0x(n)+ a_1x(n-1)+ a_2x(n-2)+ a_3x(n-3)+ a_4x(n-4)+ a_5x(n-5)+ a_6x(n-6)+ a_7x(n-7)$$

Where x is the input of the filter and a_n are the coefficient for the filter:

a_0= 0.04727 a_1= 0.00000 a_2= - 0.11600 a_3= 0.56873

a_4= 0.56873 a_5= - 0.11600 a_6= 0.00000 a_7= 0.04727

Considering that the coefficients, inputs and outputs of the filter are defined as signed numbers of 10 bits.

a) **Obtain the difference equation to be implemented in VHDL. The answer must include all the calculations. (1pt)**
b) **Obtain the minimum width of the register to be used to save the final result. The answer must include all calculations. (1pt)**
c) **Draw the schematic of a pipeline architecture where the critical path delay of the circuit is divided by 3. (2pt)**
d) **Describe using VHDL a serial architecture for the filter. Consider the following entity (3,5pt)**

```
ENTITY fir IS
PORT ( clk: IN STD_LOGIC;
       Rst: IN STD_LOGIC;
       Enable: IN STD_LOGIC;
       Data_in: IN SIGNED (9 downto 0);
      Data_out:OUT SIGNED (9 downto 0));
END fir;
```

e) **Design a testbench in VHDL for this circuit where the input Data_in get the 2^8 possible signed values of a *Sawtooth waveform of 750 Hz. Consider a clk signal of 75 MHz. Do NOT use a ROM memory to save the Sawtooth waveform* (2,5pt).**