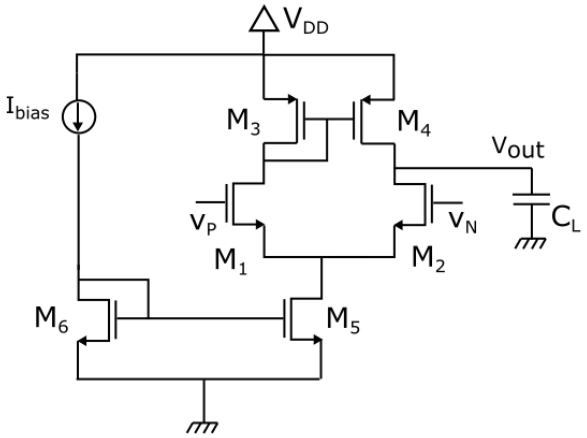
EMPIECE CADA EJERCICIO EN UNA HOJA NUEVA

Exercise1 (2 pts., 30 min.)

Ex. The amplifier below has been designed with a CMOS node of 50nm,



With the following features:

	NMOS	PMOS
μ*Cox (μA/V²)	90	40
λ (V⁻¹)	0.6	0.5
V_{th} (V)	0.28	-0.28

V_{DD} = 1.2 V, L = 100 nm for all the transistors.
All the transistors work in saturation,

$(W/L)\ M_1 = (W/L)\ M_2 = 30$

$(W/L)\ M_3 = (W/L)\ M_4 = 60$

$(W/L)\ M_5 = 20$

$(W/L)\ M_6 = 40$

C_L = 500 fF, 1 fF = 10^{-15} F

V_P and V_N are differential signals

Asnwer the following questions:

a) If V_{GS6} = 0.6 V, compute I_{bias}.
b) Compute the DC gain $V_{out}/(V_P - V_N)$ in dB with the I_{bias} computed previously.
c) Looking only at the dependence of the gain with respect to the output resistance, what happens with the gain if we decrease I_{bias}? Justify your answer.
d) What happens with the bandwidth of the amplifier if we increase C_L? Justify your answer.

Note: All the questions must be justified. Answers with no justification will not score.

Exercise 2 (3.5 pts., 50 min.)

We want to implement a digital circuit to calculate the value of a polynomial:

$$f(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5$$

For its implementation, it is more efficient to transform the operations of the algorithm so that they can be performed in the form of multiplication and addition (MAC). The transformation is performed by taking common factor x successively:

$$f(x) = a_0 + x(a_1 + a_2x + a_3x^2 + a_4x^3)$$
$$f(x) = a_0 + x(a_1 + x[a_2 + a_3x + a_4x^2])$$
$$f(x) = a_0 + x(a_1 + x[a_2 + x\{a_3 + a_4x\}])$$

The values of the coefficients are the following:

a_0 = 1,1423 a_1 = -0,9867 a_2 = 0,4312 a_3 = 0,1824 a_4 = -0,1101

Los puertos del circuito son los siguientes:

- Clk (input, 1 bit): reloj, rising edge active
- Reset (input, 1 bit): asynchronous initialization, high level active
- EnaIn (input, 1 bit): a high level indicates there is new data to be processed in input xData; it lasts a clock cycle.
- xData (input, 10 bits signed): x data input
- EnaOut (output, 1 bit): a high level indicates there is a new result in the output; it lasts one clock cycle.
- yData (output, 16 bits signed): data output

As requirements for implementation, we want (in order of importance):

1. Both the input and output of circuit data must be registered.
2. The circuit must operate at the highest possible clock frequency.
3. Latency between the data input and the data output is as lower as possible.

We ask:

a) Transform the coefficients of the equation so that the algorithm can be implemented using signed 10-bit operands.
b) List the operations of the algorithm, in the order in which they must be performed.
c) Reason the type of architecture to use to meet the requirements. The smaller operator to use is the MAC (multiplication and addition).
d) Draw a schematic of the data path to be implemented, specifying the number of bits of each signal.
e) Write the VHDL code that describes the data path. It is only necessary to write the architecture, including the declaration of the necessary signals.
f) Draw the state diagram of the state machine needed to control the data path. How many clock cycles are required for the polynomial calculation?

Exercise 3 (1 pto., 20min.)

We have an I0 inverter connected to 32 gates.

a) Indicate the switching delay and how this delay can be reduced if we have all the inverters we need. Draw the resulting inverter tree. Indicate the delay achieved and the number of inverters used.

This I0 inverter is also connected to an output pin with an equivalent capacity of 1050 elementary gates.

b) Indicate the delay of I0 based on the standard delay of an inverter (t_{pi})
c) We want to reduce the delay of I0 to an optimal value, without area restrictions. Indicate the number of inverters of increasing size required, the delay obtained and the area increased.
d) If instead of the optimal solution, we use three inverters of increasing size (W, 3W, 9W) indicate the delay obtained and the increased area.

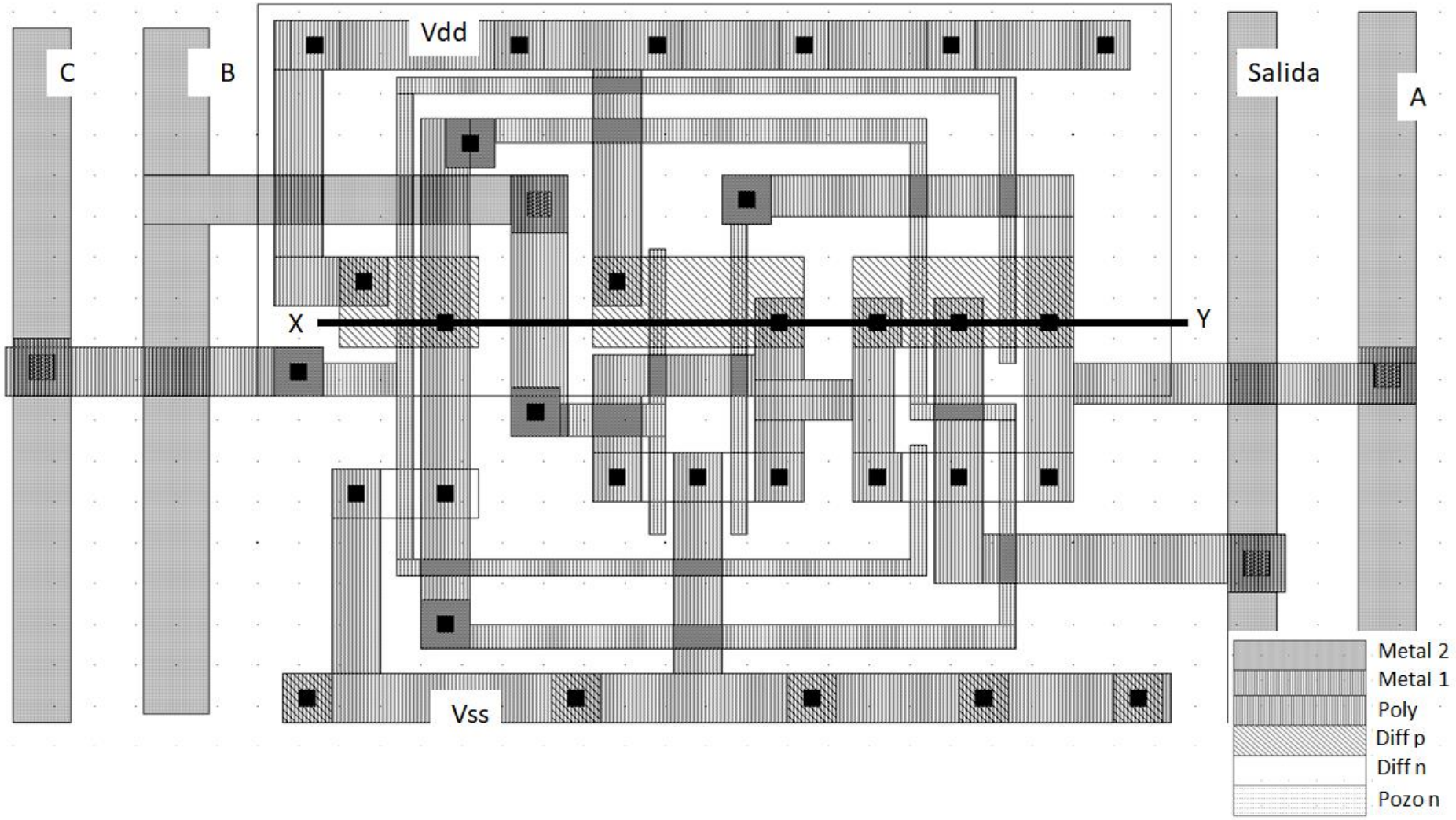
	Delay	Area
Initial		-
W, 3W, 9W		
Optimal solution		

Note: your solution must include a table like this.

Exercise 4 (3,5 pts., 50min.)

Answer the following questions in relation with the give layout:

a) Draw the transistor level schematic of the circuit
b) Write the state of all transistors for the input values CBA="110" and CBA="001".
c) Determine the functionality of the circuit, either by its logic functions or with a gate schematic.
d) Draw the cross section seen through the line X-Y.


C
B
Vdd
Salida
A
X
Y
Vss
Metal 2
Metal 1
Poly
Diff p
Diff n
Pozo n