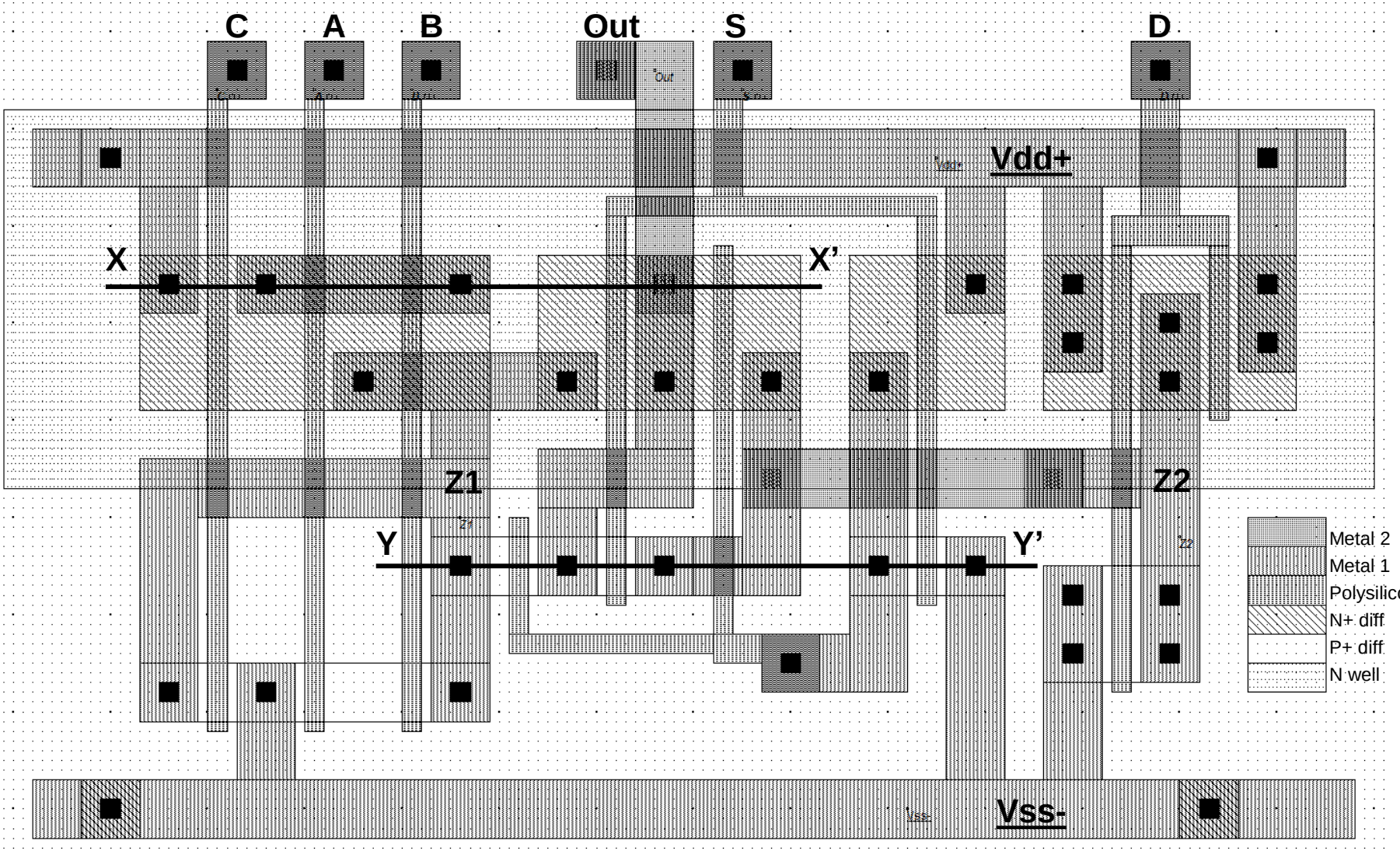
Problem 1 (50 min, 4 pt)

The figure shows the layout of a digital circuito, where A, B, C, D and S are inputs, Out is output and Z1 and Z2 are intermediate signals.

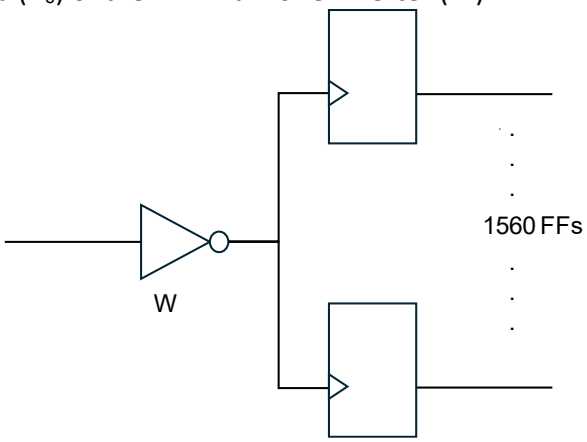
a) List the layers forming the contacts on the Vdd and Vss lines and explain the purpose of these contacts
b) Draw the transistor schematic from the layout
c) Draw the logic function of the intermediate signals Z1 and Z2, and the Out output
d) Draw the circuit gate schematic
e) Draw the cross section of XX' and YY' cuts


C
A
B
Out
S
D
Vdd+
X
X'
Z1
Z2
Y
Y'
Vss-
Metal 2
Metal 1
Polysilicon
N+ diff
P+ diff
N well

Problema 2 (30 min, 3 pto)

A digital circuit has a clock input driving 1560 flip-flops (FFs). We assume each FF shows a parasitic capacitance equivalent to that of a minimum size inverter.

a) Calculate the delay and area of a single-stage tree, such as the one in the figure as a function of the delay (t_{pi}) and area (A_0) of the minimum size inverter (W).

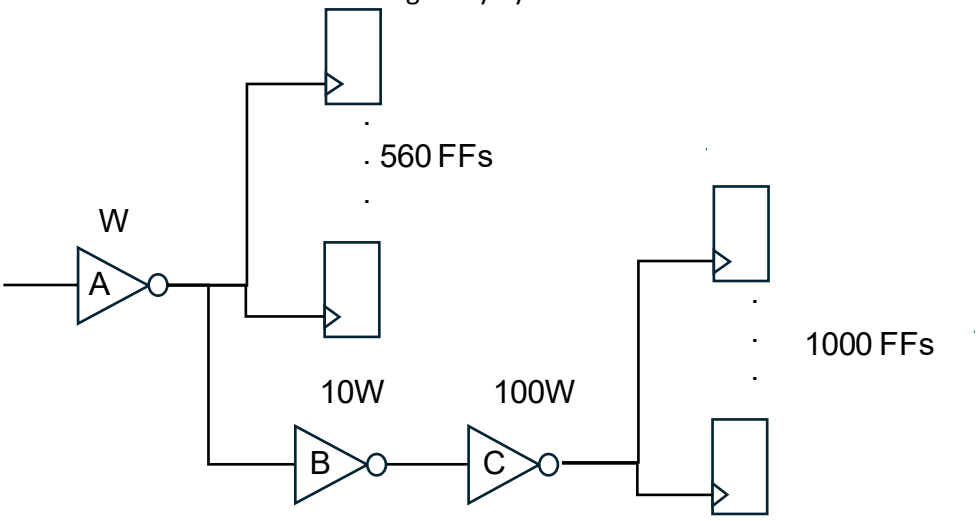


b) Calculate the delay and the area of a clock tree where the maximum *fanout* is 2.

c) The inverter in the figure is to be replaced by a chain of inverters of increasing size. Indicate the number of inverters required for a minimum delay, the delay obtained, and the required area.

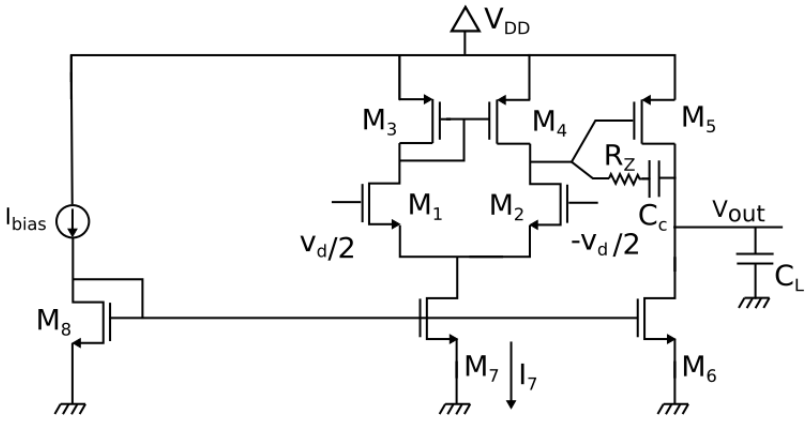
d) The circuit is modified as shown in the figure.

a. Indicate how long it takes for inverter A to switch
b. Indicate the delay from inverter A output to inverter C output
c. Propose a solution to include a pair of inverters of size βW and ϕW in the 560 FFs branch, in order to reduce the delay of inverter A and to balance the delay by the two branches of the new circuit. Indicate the resulting delay by both branches and the total area.



Problema 3 (30 min, 2.5 pto)

An operational amplifier like the one depicted in the figure will be designed, with differential input and single-ended output.



The requirements to accomplish are listed below:

- **Power consumption of 120 µW** (the three branches are included. It is assumed that the three branches consume the same). V_{DD} = 1 V.

a) Set the current I_{bias} considering the transistors M_6, M_7 and M_8 similar (0.5 pts).

- **Minimum and maximum output voltages of 0.2 V and 0.8 V**, respectively.

b) Use the previous requirement to define (W/L) of M_5 and M_6 (0.5 pts).

- **Gain-Bandwidth product higher or equal than 100 MHz.**

c) Use the previous requirement to define (W/L) of M_1 and M_2 (0.5 pts).
d) Compute the gain of the operational amplifier (V_{out}/V_d) (0.5 pts).
e) Justify the operating point of transistor M_8 (0.5 pts).

Data and equations:

$$\mu_P C_{ox} = 45\ {}^{\mu A}/_{V^2} \quad \lambda_P = 0.3\ V^{-1} \quad V_{thp} = -0.3\ V$$

$$\mu_N C_{ox} = 90\ {}^{\mu A}/_{V^2} \quad \lambda_N = 0.6\ V^{-1} \quad V_{thn} = 0.3\ V$$

C_L = 1 pF, C_c = 0.5 pF, L = 200 nm (for all the transistors)

$$GBW = \frac{g_{m1}}{2\pi C_C}$$