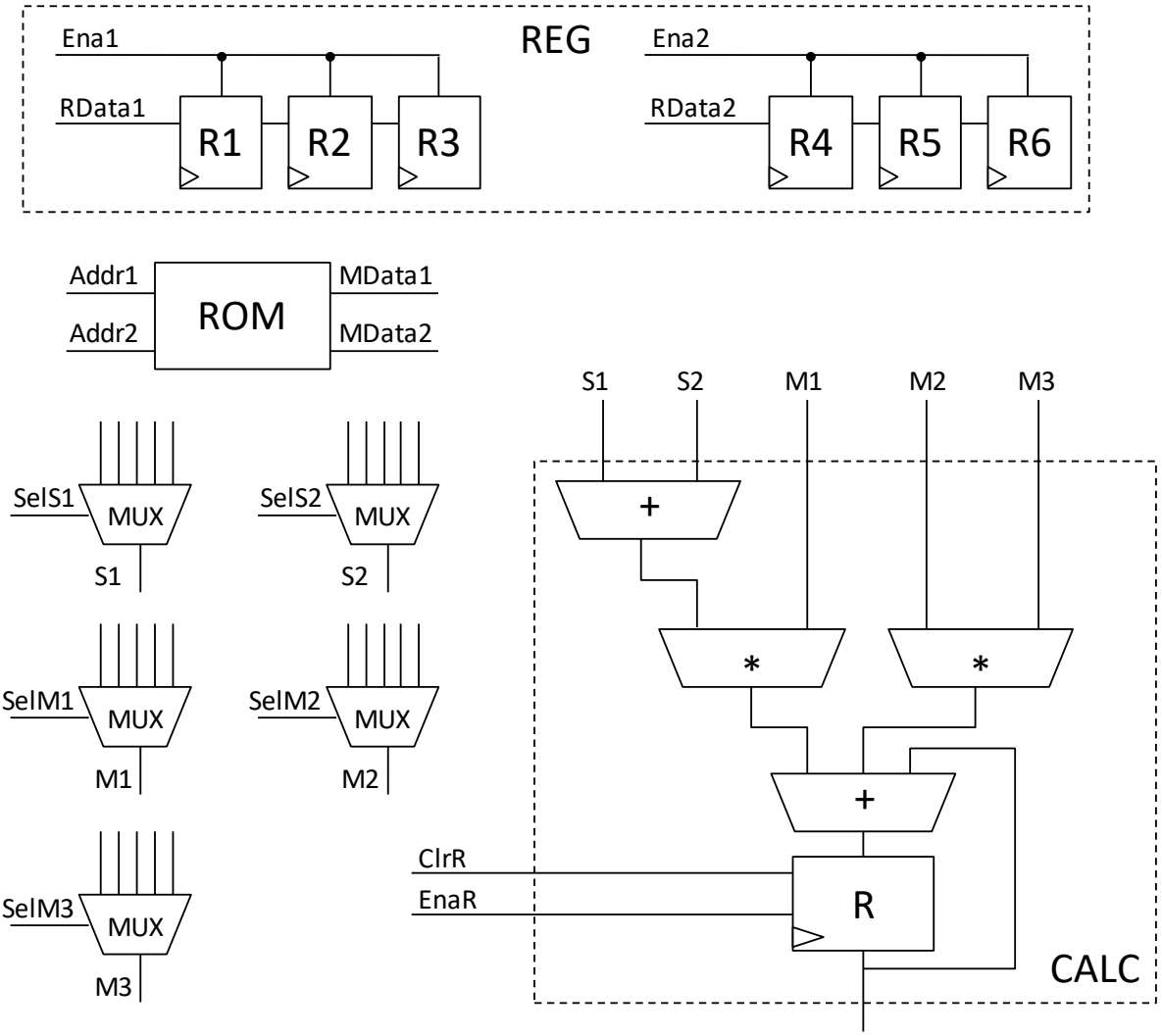
Problem 1 (50 min, 3.5p)

We want to implement a signal processing algorithm using the following data path:



- R is an accumulator register that stores the result of the sum when EnaR is activated. It is reset by activating ClrR.
- Ri are 8-bit registers. When EnaX is enabled, RDataX is passed to the first register and the different registers pass their values to each other in series.
- MUX are multiplexers, and SelXX signals select between their different inputs.
- ROM is a dual-port memory that stores 8-bit constants.

We want to use this data path to implement a low pass IIR filter with the following transfer function (sampling rate 24kHz, cutoff frequency 8kHz):

Se desea utilizar dicha ruta de datos para implementar un filtro IIR paso bajo de orden 3 con la siguiente función de transferencia (Frec. de muestreo 24kH, frecuencia de corte 8kHz):

$$F(z) = \frac{0{,}3318 + 0{,}9954z^{-1} + 0{,}9954z^{-2} + 0{,}3318z^{-3}}{1 + 0{,}9658z^{-1} + 0{,}5826z^{-2} + 0{,}0160z^{-3}}$$

The entity of the complete circuit is as follows (SIZE is a constant to be determined later):

```
entity dsp is
  port ( Reset:  in  std_logic;
         Clk:    in  std_logic;
         Load:   in  std_logic;
         Data:   in  signed(7 downto 0);
         EoP:    out std_logic;
         Result: out signed(SIZE-1 downto 0) );
end dsp;
```

1) Determine the difference equation of the transfer function, expressed in the appropriate form for its implementation, considering the data path operates with integers, and the coefficients and data are implemented with 8 bits.

2) List the sequence of operations to be performed to implement the algorithm with the proposed data path. Determine how many clock cycles are required to perform a complete calculation, including the data loads in the registers.

3) Determine the data to be connected to RData1 and RData2 and the data inputs required in every multiplexer. Since the size of the multiplexers increases with the number of inputs, it will be better considered to have the smallest number of inputs, and even the possibility of eliminating multiplexers.

5) Draw the state transition graph for a state machine that controls this data path to implement the algorithm. The calculation starts with the activation of the Load input, and when finished, the EoP output will be activated to indicate there is a new data in the output. Write in a table the values of the outputs corresponding to each state.

6) Describe in VHDL a model of the ROM memory. It must be asynchronous and contain the necessary coefficients to implement the algorithm.

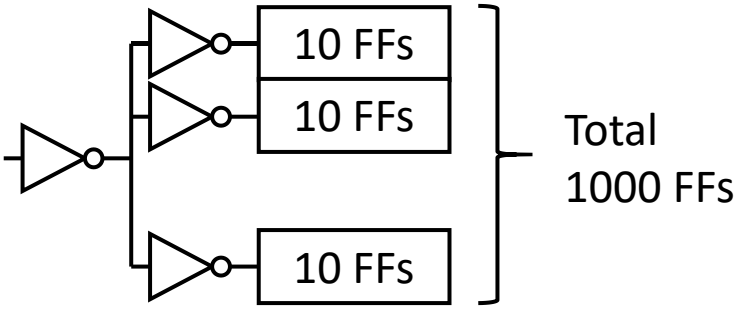
7) Assign the appropriate number of bits to each of the signals in the CALC circuit. Describe in VHDL the REG and CALC circuits. Include the declaration of the signals to be used.

8) Determine the size (SIZE) of the total output of the circuit (Result) and write the VHDL description to generate it.

Problem 2 (20 min, 1p)

We want to implement a clock tree for a circuit with 1000 flip-flops, each of them with a load equivalent to that of a minimum size inverter.

a) In a first approach, the following clock tree is proposed. Calculate its delay and area as a function of the delay (t_{pi}) and the area (A_0) of the minimum size inverter.



b) Calculate the delay and area if the tree is binary (fanout 2).

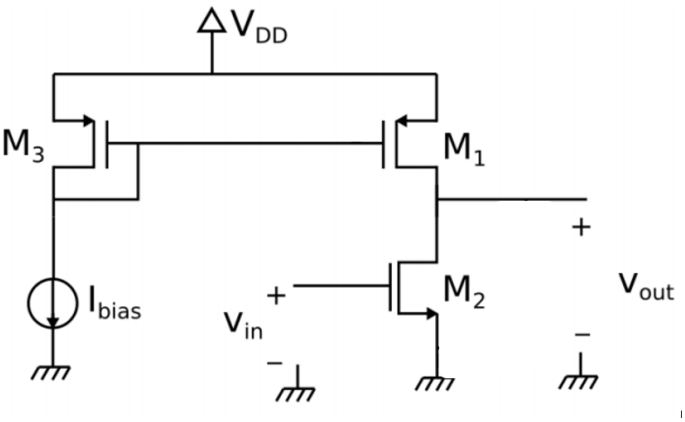
c) Propose a tree that minimizes delay and area. Calculate its delay and area.

Fill in the following table with the previous results.

	a)	b)	c)
Delay (t_p)			
Area (A)			

Problem 4 (30 min, 2p)

The following circuit has been implemented with 800 nm CMOS technology:



	NMOS	PMOS
μ*Cox (μA/V²)	110	50
λ (V⁻¹)	0.04	0.04
V_{th} (V)	0.5	-0.6

I_{bias} = 40 μA, V_{DD} = 2,5 V
L = 800 nm para todos los transistores

	W (μm)
M_1	40
M_2	80
M_3	20

Given the following characteristics and size ratios, answer the questions:

a) Calculate the bias current through M1 and M2 and the voltage V_{gs2}.

b) Calculate the transconductance g_{m2} and the resistance r_{02}

c) Calculate the gain V_{out}/V_{in} of the circuit.

Note: it is not necessary to justify the operating point of the transistors.

d) If we want to make the voltage gain double by changing the width of transistors M1 and M2, what will the new values be?

NOTE: All answers must be justified. Unjustified or incorrectly justified answers will not be marked.

Problem 3 (45 min, 3.5p)

The diagram in the figure below shows the physical schematic of a digital circuit:

a) Obtain the transistor schematic of the layout.
b) Draw a table showing the state of P and N transistors that generate S1 and S2.
c) State the simplified logic functions of *Salida* as a function of the inputs (A, B, C and Sel).
d) Draw the cross-section view of the XY slice.