Problem 1 (50 min, 4p)

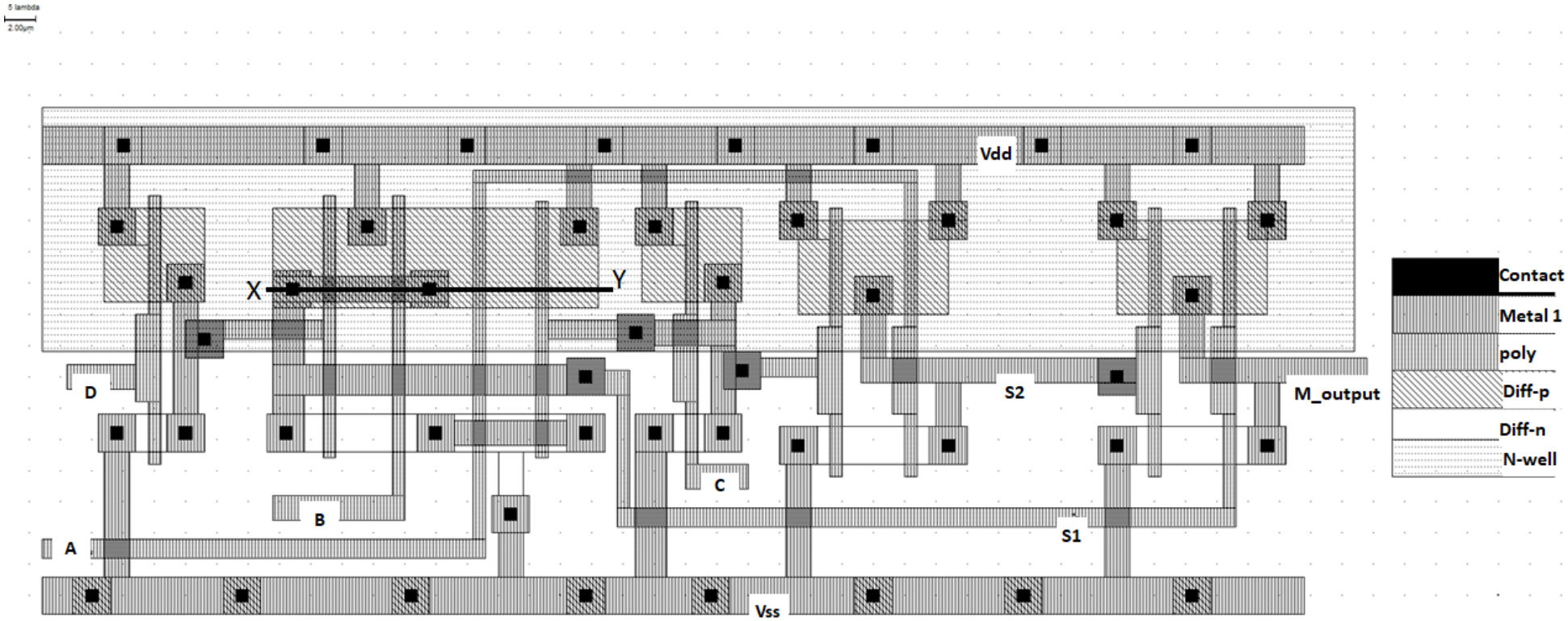
The diagram in the next figure shows the physical scheme of a digital circuit.

a) Obtain the transistors scheme from the figure layout.

b) Draw a table with the status of the P and N transistors (*On* and *Off*) that generate S1 and S2. Do not consider transistors in the inverters. Name the transistors from the left to the right and from the top to the bottom (also in the scheme of section a).

c) Specify simplified logic function of M_output based on inputs (A, B, C, and D).

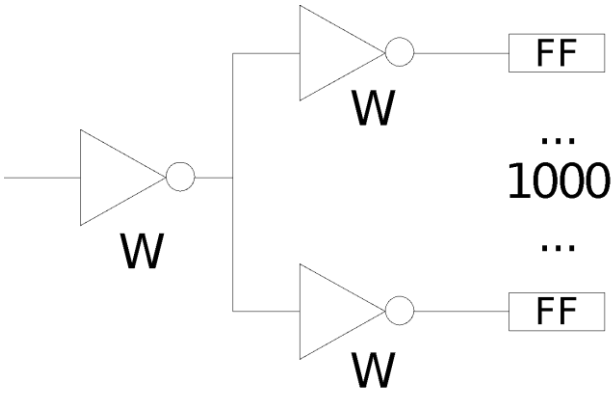
d) Get the cross section view of the XY cut.


5 lambda
2.00µm
Vdd
X
Y
D
S2
M_output
Contact
Metal 1
poly
Diff-p
Diff-n
N-well
C
B
A
S1
Vss

Problem 2 (30 min, 2.5p)

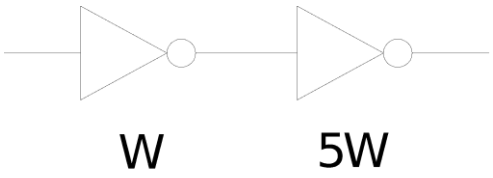
We want to implement a clock tree for a circuit with 1000 flip-flops with an equivalent load of a basic inverter.

a) Obtain the delay and area of the clock tree with a single stage (as shown in the figure) as a function of the delay (t_{pi}) and area (A_0) of a minimum size inverter (W)



b) Obtain the delay and area for a clock tree with a maximum fanout of 10.

c) For the previous configuration (part b) obtain the delay and the area if every inverter is replaced by the following chain.

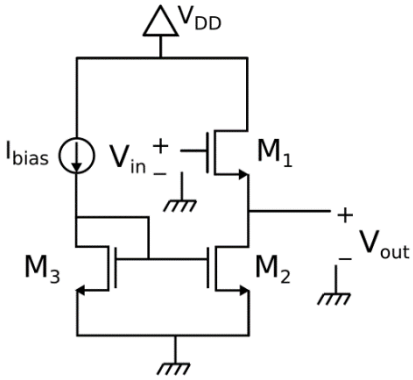


Fill the table with the results:

	Part a	Part b	Part c
Delay (t_p)			
Area (A)			

Problem 3 (30 min, 2.5p)

The following circuit has been implemented making use of an 800-nm CMOS technology node:



Given the following features and size ratios, answer the questions:

	NMOS	PMOS
μ*Cox (μA/V2)	110	50
λ (V-1)	0.04	0.04
Vth (V)	0.5	-0.6

Ibias = 50 μA, VDD = 2.5 V

L = 800 nm for all the transistors

	W/L
M1	50
M2	100
M3	25

a) Compute the gain Vout/Vin of the circuit in V/V. Note: you do not need to justify the operating point of the transistors (1 pt).

b) If we connect a capacitor of 1 nF at the output (between Vout and ground) to work as the load of the circuit, will the previous gain Vout/Vin remain if Vin is a sinusoidal signal with a frequency of 1 kHz? Justify your answer (0.75 pts).

c) With no capacitor we now implement the same circuit in a 50-nm CMOS technology node with the same size ratios as before and the following parameters:

	NMOS	PMOS
μ*Cox (μA/V2)	110	50
λ (V-1)	0.6	0.4
Vth (V)	0.28	-0.28

Does the gain increase or decrease? Justify your answer (0.75 pts).

NOTE: All the answers must be justified. Answers either with no justification or incorrect justification will not be scored.

Problem 4 (10 min, 1p)

Explain which logic value is not transmitted in an optimum way from the input to the outputs in a NMOS pass transistor. Explain how to solve this problem. Justify your answer.