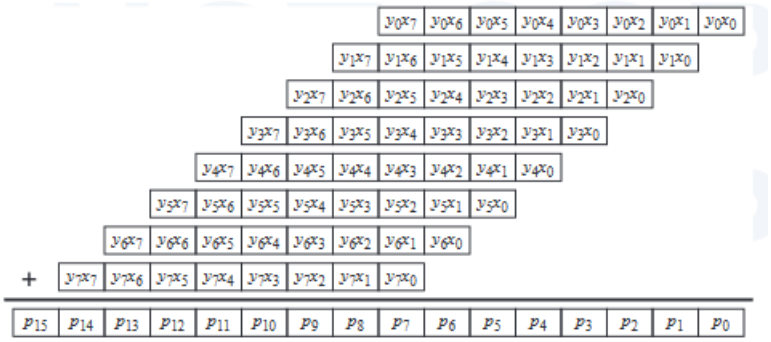
Architecture problem 1:

Most approaches to combinational multiplication are based on the paper-and-pencil shift-and-add algorithm. The following figure illustrates the basic idea for an 8x8 multiplier for two unsigned integers.



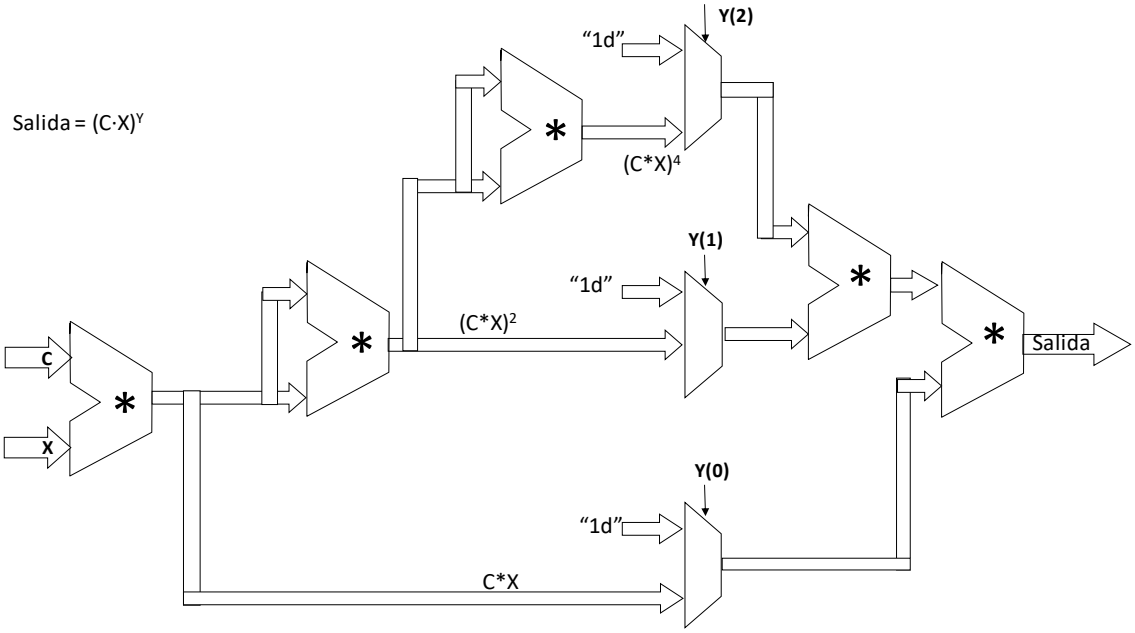
a) Represent at Register Transfer Level (RTL) each of the different architectures studied (serial, parallel and pipeline).
b) Describe using VHDL the different architectures and the corresponding TB to check the functionality of the circuit.

Architecture problem 2:

We want to describe in VHDL the digital circuit that implements the mathematical operation:

$$\text{Output} = (C\text{-}X)Y$$

Where X is the input, C is a constant between 0 and 15 and Y is an input between 0 and 7. For this purpose, the following architecture is proposed, at the Register Transfer Level (RTL):



(a) Describe the circuit entity. Assume that the data X is 16 bits. The output shall be sized to the minimum number of bits that allow us to represent the maximum result for the function.

b) Describe the circuit architecture where the intermediate signals corresponding to the partial results are defined. Size them appropriately so as not to lose accuracy in the final result

c) Describe the concurrent statements necessary to produce the partial results and the output of the circuit.

d) The data X are numbers between 0 and 7.9999389648437, with 3 bits of integer part and 13 bits of decimal part. If the output can only have 16 bits, how many are integer part and how many are decimal part?

Architecture problem 3:

We want to implement in vhdl the following equation:

$$output = 1 - X^2/2 + X^4/4 - X^6/8$$

Considering that the input X is a signed vector of 10 bits.

c) Represent at Register Transfer Level (RTL) each of the different architectures studied (serial, parallel and pipeline).
d) Describe using VHDL the different architectures and the corresponding TB to check the functionality of the circuit.

Architecture problem 4:

Describe using VHDL a serial architecture of the FIR filter of lab sessions. Create a TB to check the filter with different stimulus: step response, sine wave and triangular wave.