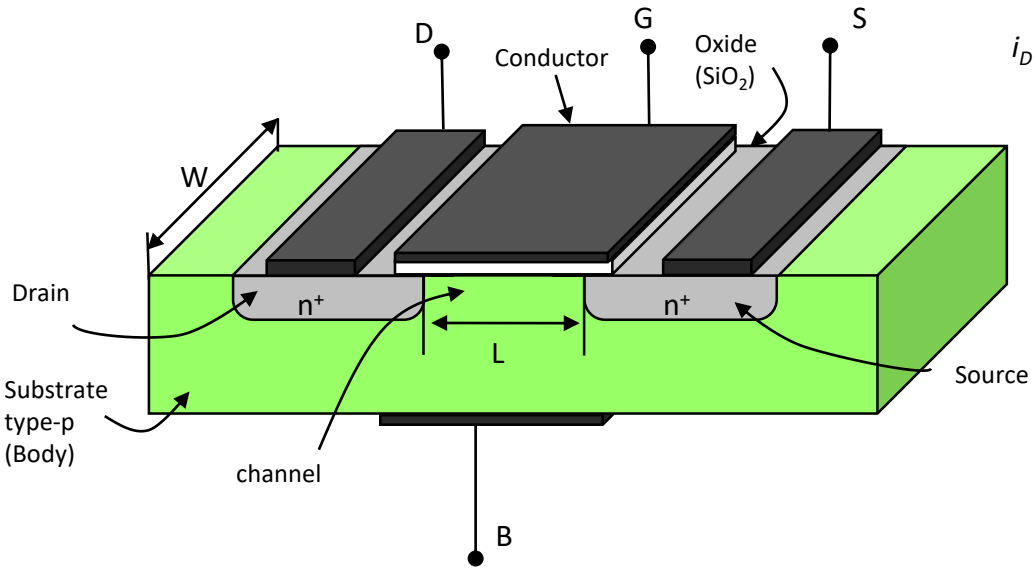
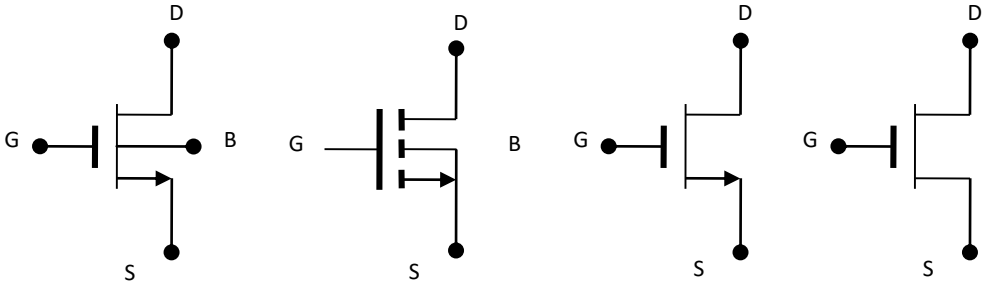
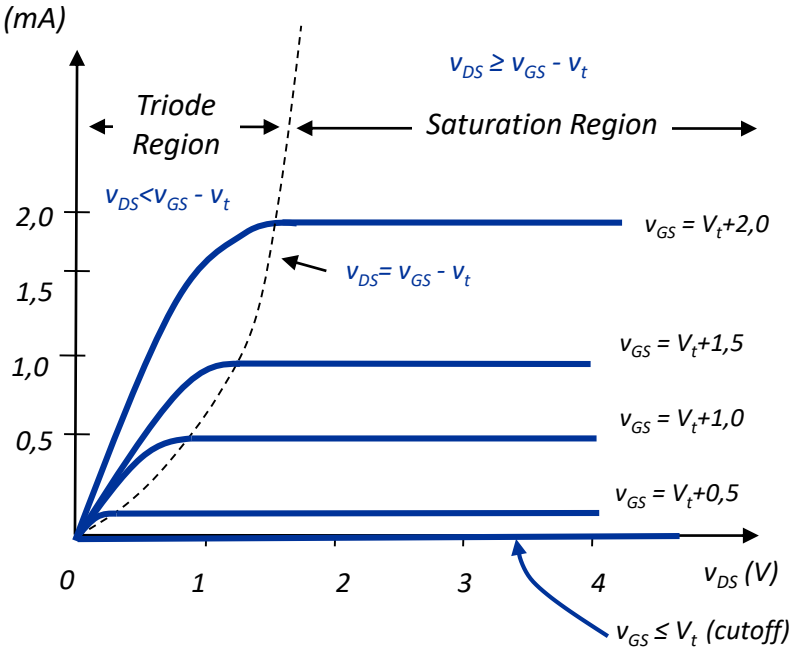
Enhancement NMOS







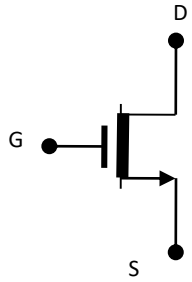
$$K = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

W=> Width
L=> Length
C_{ox}=> Oxide Capacitance
μ_n => Electron Mobility

- Cut-off : $v_{GS}<{}^*v_t$
  $i_{DS}=0$
- Triode: $v_{DS}<v_{GS} - v_t$
  $i_{DS}=K[2(v_{GS} - v_t)\, v_{DS} - v_{DS}^2]$
- *Saturation:* $v_{DS}> v_{GS} - v_t$
  $i_{DS}=K\,(v_{GS} - v_t)^2$

*Vt =Threshold voltage

Depletion NMOS



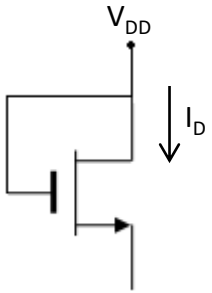
- Pre-manufactured channel

$v_{GS} = 0$ *Conduction*

$v_{GS} < -v_t$ *Channel dissapears*

NMOS Loads

- Enhancement load:

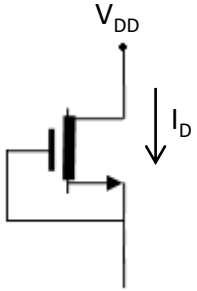


$v_{DG} = 0$ $v_{DS} = v_{GS}$

- Cut-off : $v_{GS} < v_t$
- *Otherwise, Saturation always*

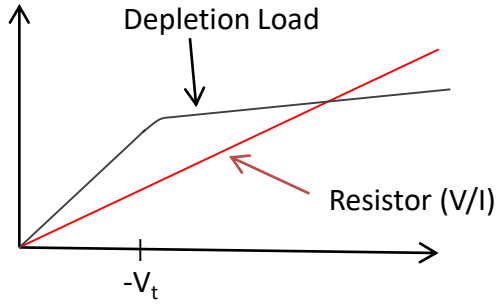
Device acts as a Nonlinear resistor *!!!*

- Depletion load:



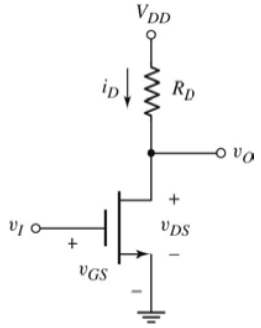
$v_{GS} = 0$

Conducion always
(Triode or Saturation)

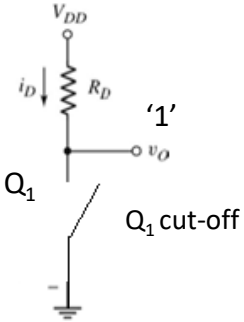


NMOS Inverter

Resistive Load



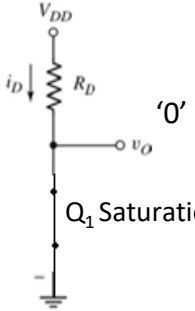
$v_{In} = 0V \rightarrow v_{In} < v_t$ $\quad v_{In} = Vdd$



'1'

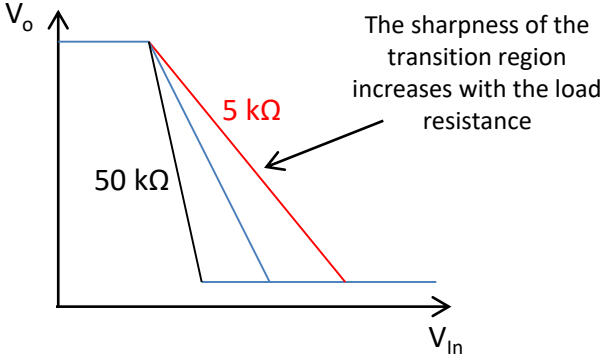
Q_1

Q_1 cut-off



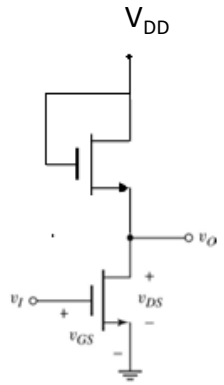
'0'

Q_1 Saturation

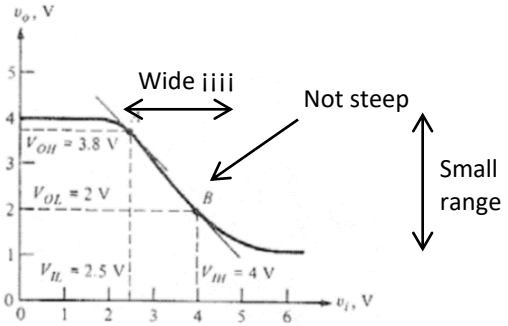


The sharpness of the transition region increases with the load resistance

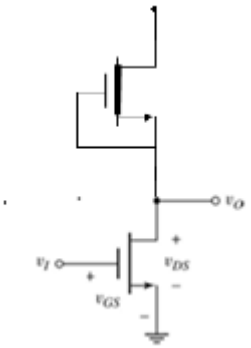
Enhancement Load



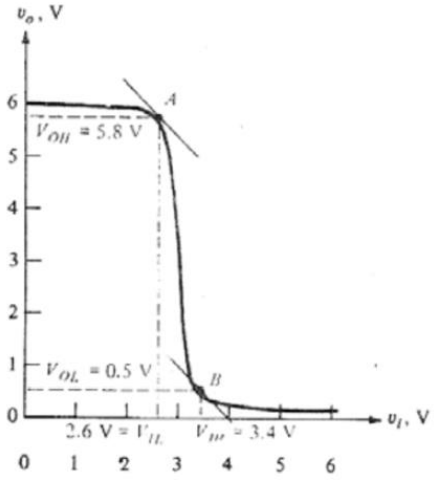
- Much more practical than the resistor loaded inverter, because the resistors are thousand of times larger size than a MOSFET.
- Wide range of inputs where the output is not determined



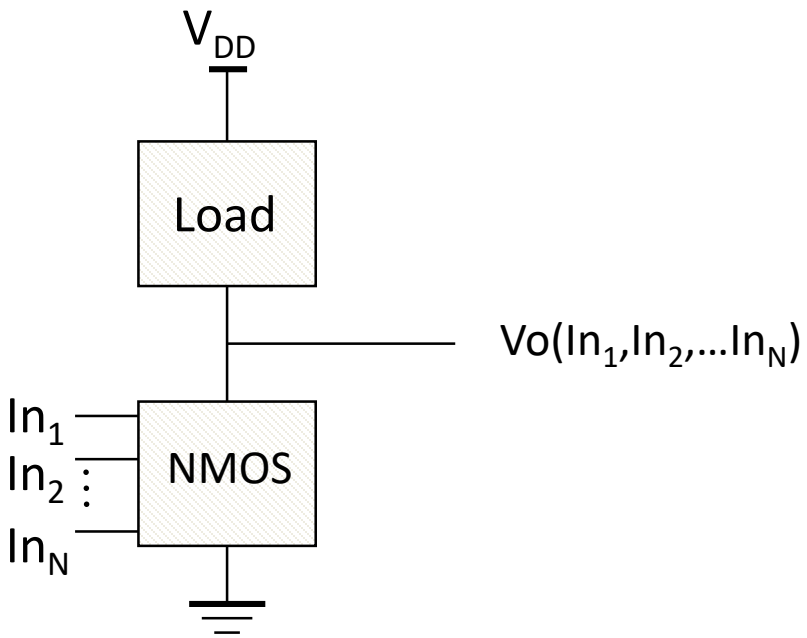
Depletion Load



- The dynamic margin is much better even though the W/L ratio for the output is small.



NMOS Logic Gates

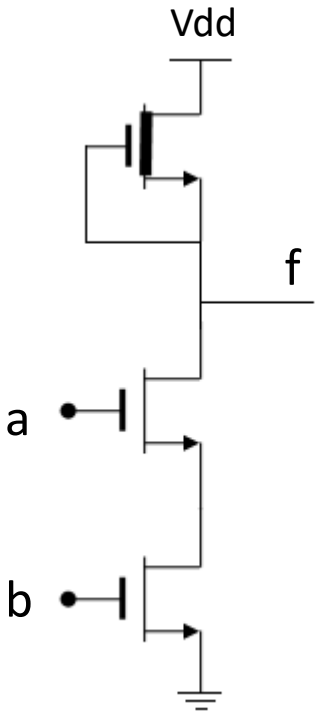


NMOS logic circuits are constructed by connecting driver transistors in **parallel, series** or **combinations** to produce required output logic function.

- Transistors in **serial** make **logic products**
- Transistors in **parallel** make **logic additions**
- Output is **inverted**
  - 2 transistors in **serial** make a **NAND** gate
  - 2 transistors in **parallel** make a **NOR** gate

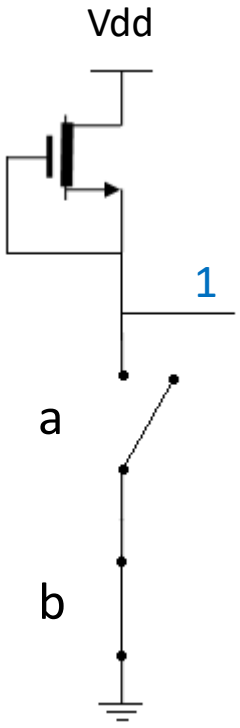
NMOS Logic Gates

NAND GATE $f=\overline{a \cdot b}$

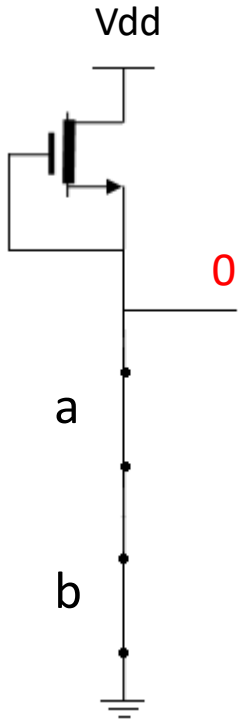


a	b	f
0	0	1
0	1	1
1	0	1
1	1	0

a=0 b=1



a=1 b=1

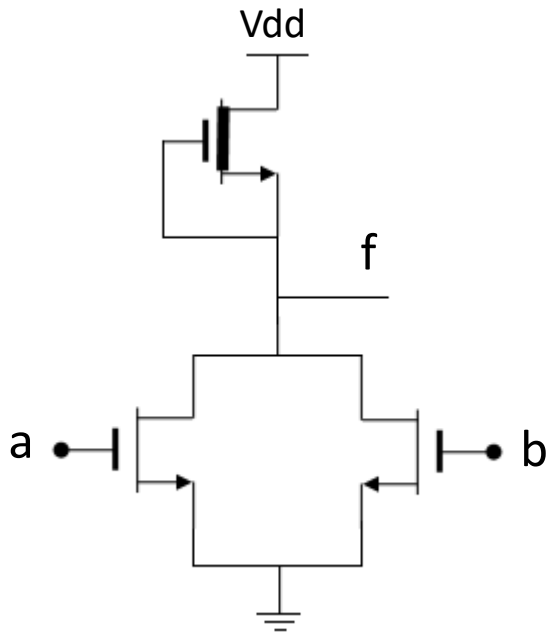


- Transistors in **serial** make **logic products**
- Transistors in **parallel** make **logic additions**
- Output is **inverted**

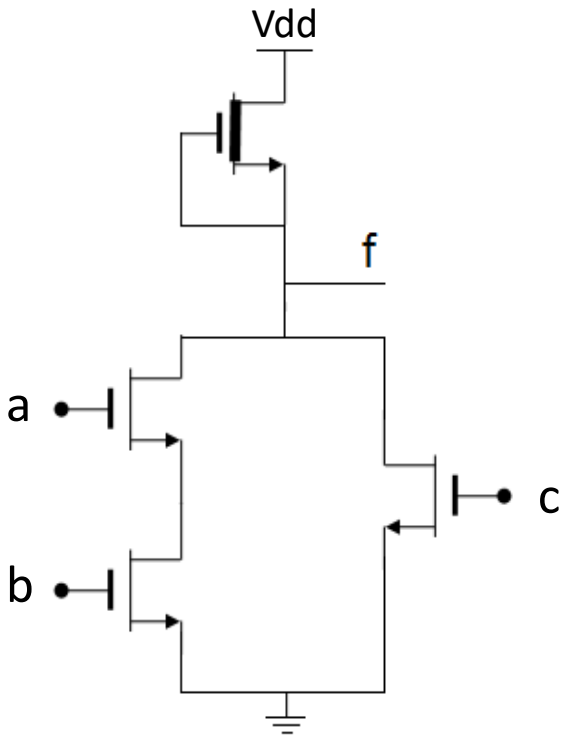
NMOS Logic Gates

NOR GATE $f=\overline{a+b}$

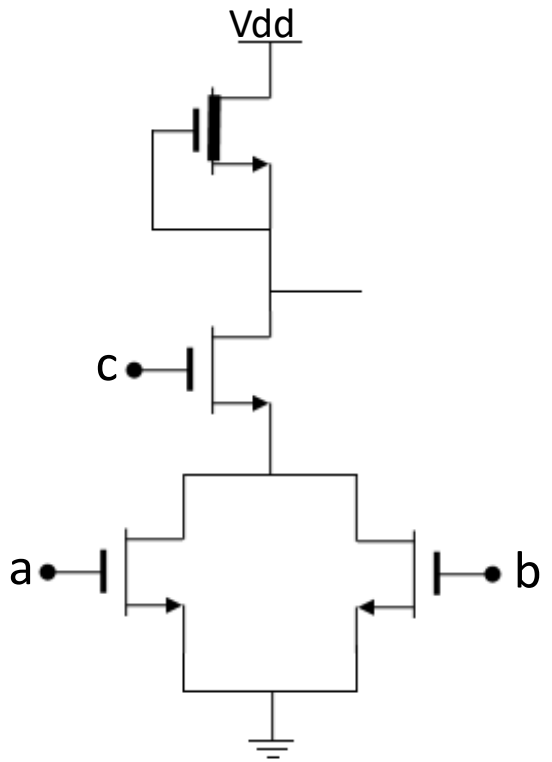
a	b	f
0	0	1
0	1	0
1	0	0
1	1	0



$f=\overline{(a\cdot b)+ c}$



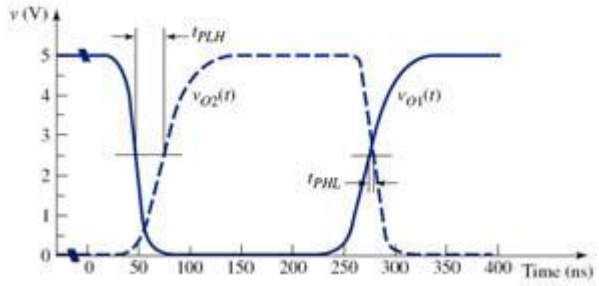
$f=\overline{(a+b)\cdot c}$



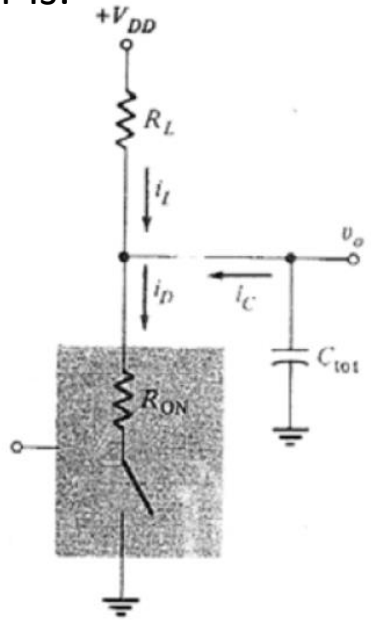
- Transistors in **serial** make **logic products**
- Transistors in **parallel** make **logic additions**
- Output is **inverted**

NMOS gates characteristics

Propagation delay

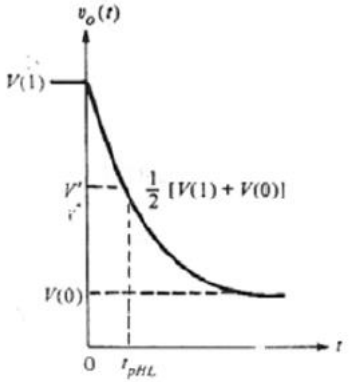


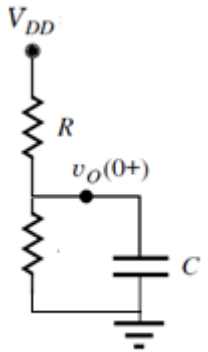
Transitions are not perfect, they are delayed because of **parasitic capacitances** and **resistors**. The considered model for the NMOS inverter is:



Calculation of τ_{PHL}

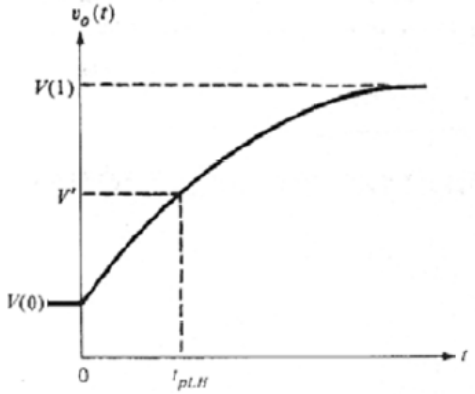
$\tau_{PHL} = (R_L \parallel R_{On}) \cdot C_L$

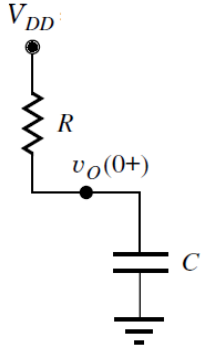




Calculation of τ_{PLH}

$\tau_{PLH} = R_L C_L$





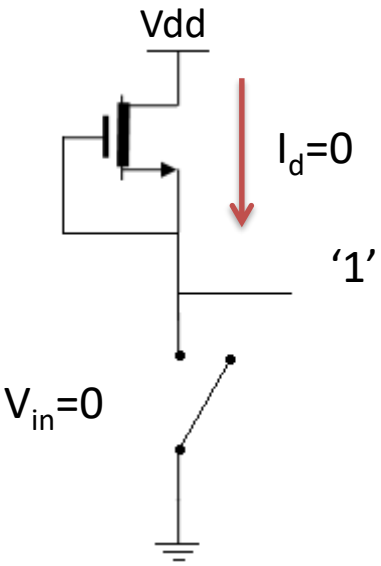
$\tau_{PLH} >> \tau_{PHL}$

Asymetric propagation times ¡¡¡¡

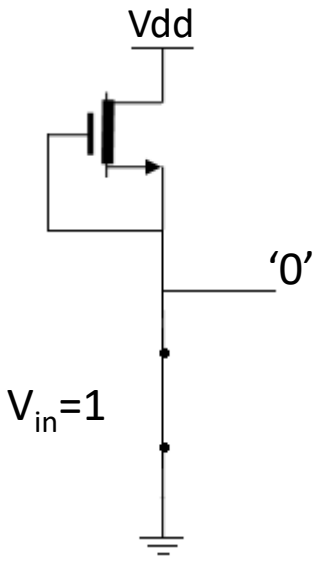
NMOS gates characteristics

Power Consumption

There is static power consumption in NMOS technologies



No consumption¡¡¡¡
(high output)



Consumption¡¡¡¡
(low output)

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

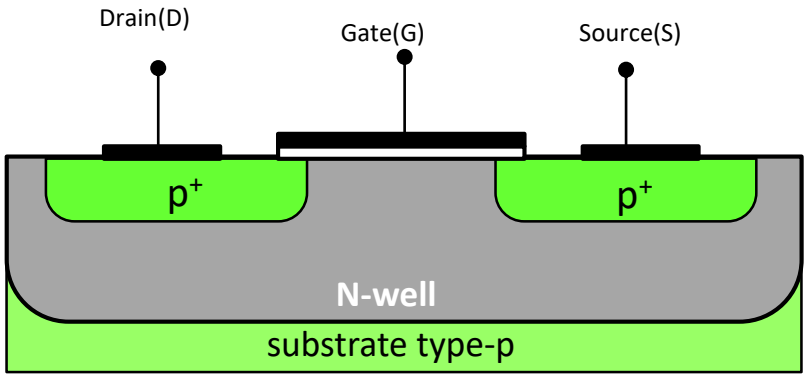
25% of cases drain power

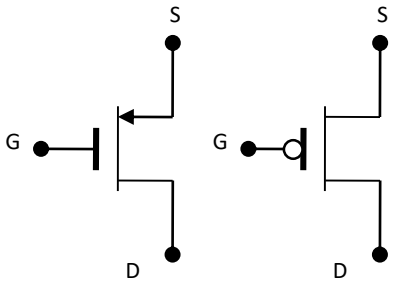
A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

75% of cases drain power

- Better implementation of NMOS circuits with NAND than NOR
- NMOS technologies are not commonly used because teh static power consumption

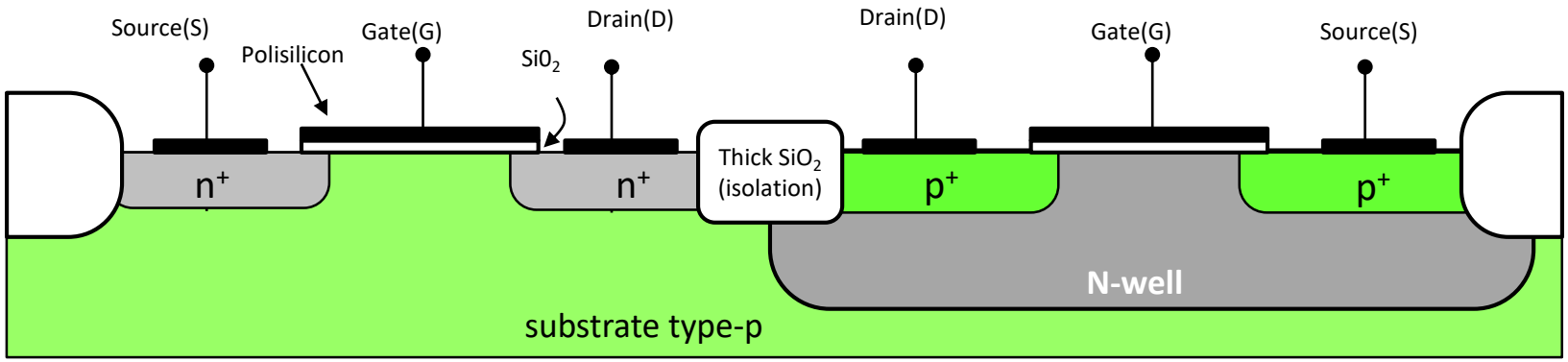
PMOS

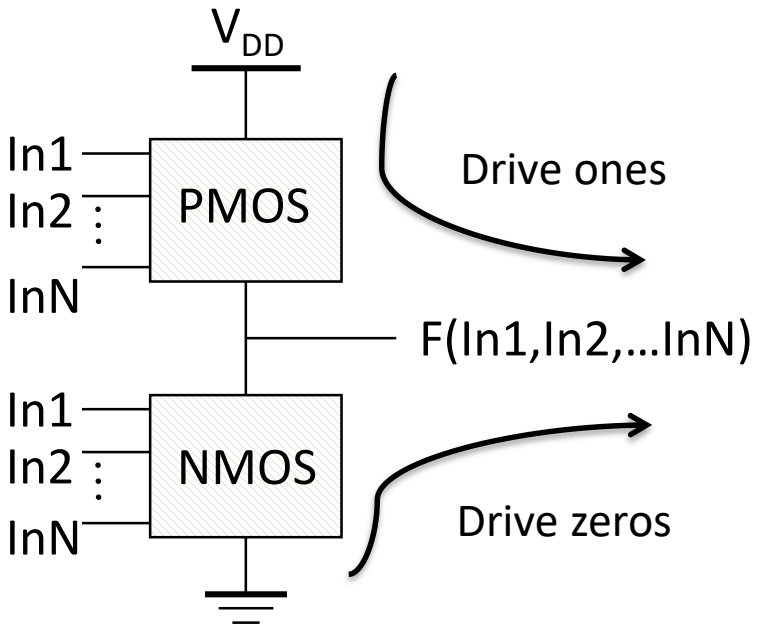




- Same equations than NMOS, changing current and voltaje signs
- Not widely used as NMOS because hole movility (PMOS) is lower than electron mobility (NMOS)
- To get the same current, usuallly we need a bigger transistor ($\mu_n = 2.5 \cdot \mu_p$)

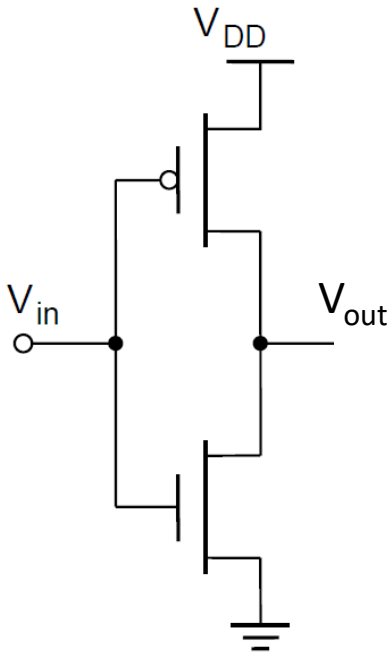
Complementary MOS Technologies (CMOS)



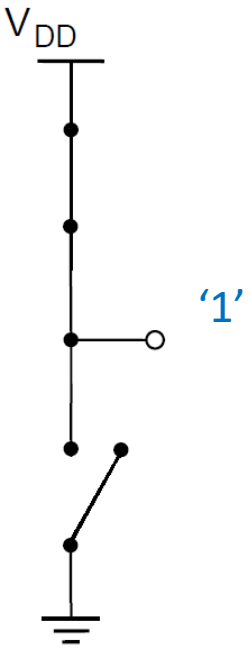


- CMOS has replaced NMOS at all level of integration because power dissipation in CMOS logic circuits is much lower than in NMOS circuits.
- Instead of using a load, we use a dual network with NMOS and PMOS.

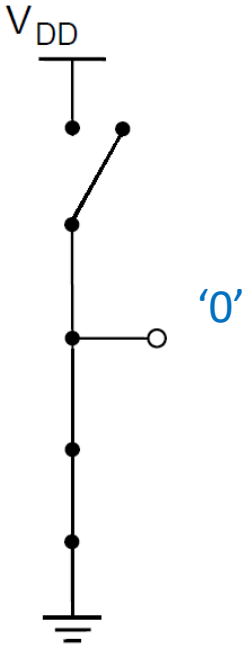
CMOS Inverter



Vin='0'

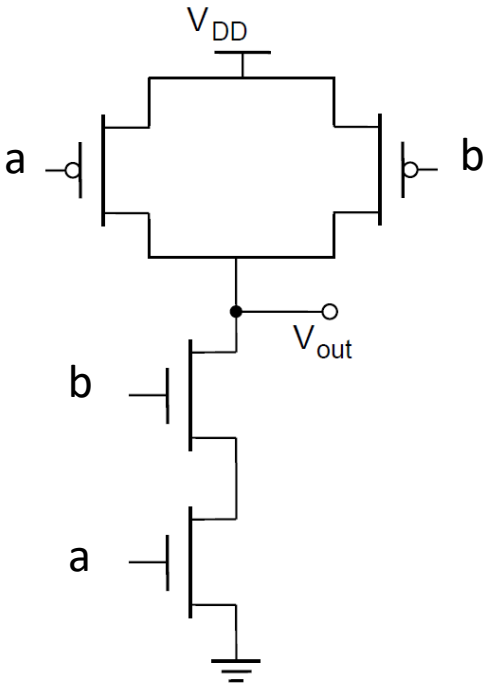


Vin='1'



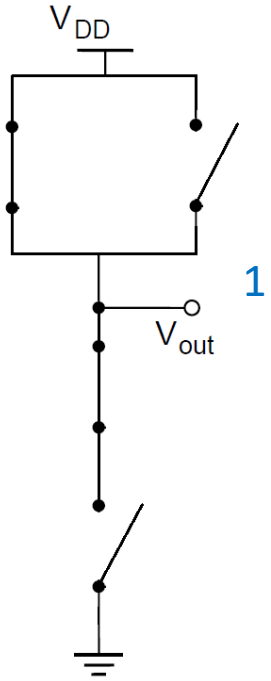
CMOS logic Gates

NAND GATE $f=\overline{a \cdot b}$

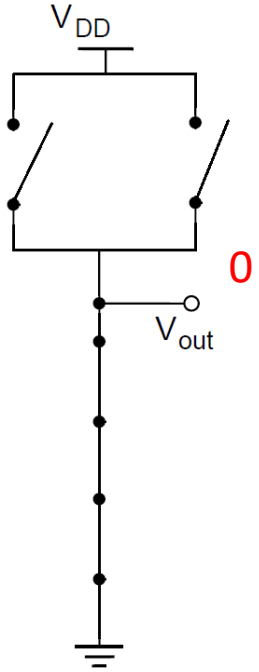


a	b	f
0	0	1
0	1	1
1	0	1
1	1	0

a=0 b=1

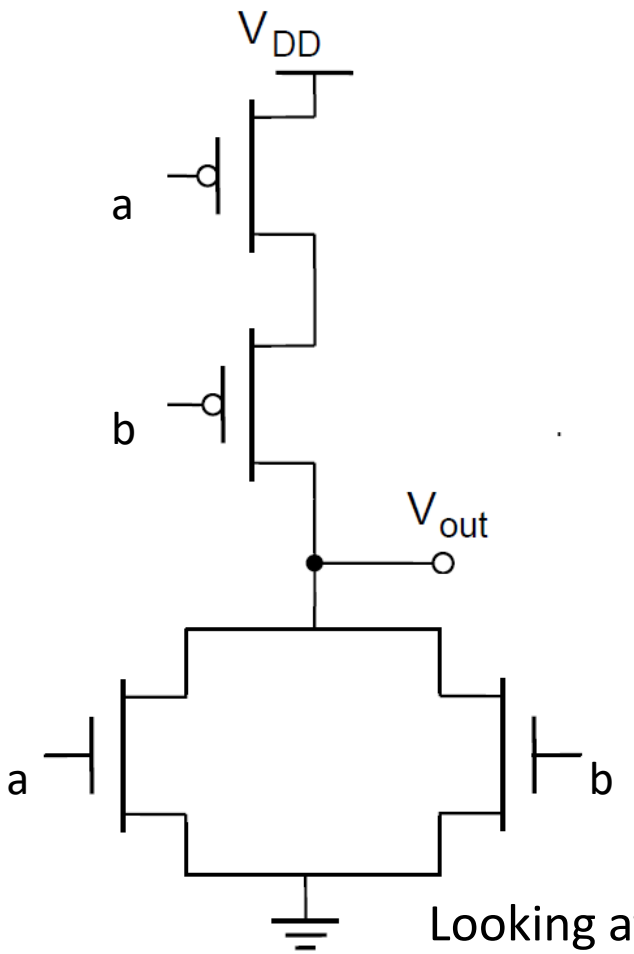


a=1 b=1

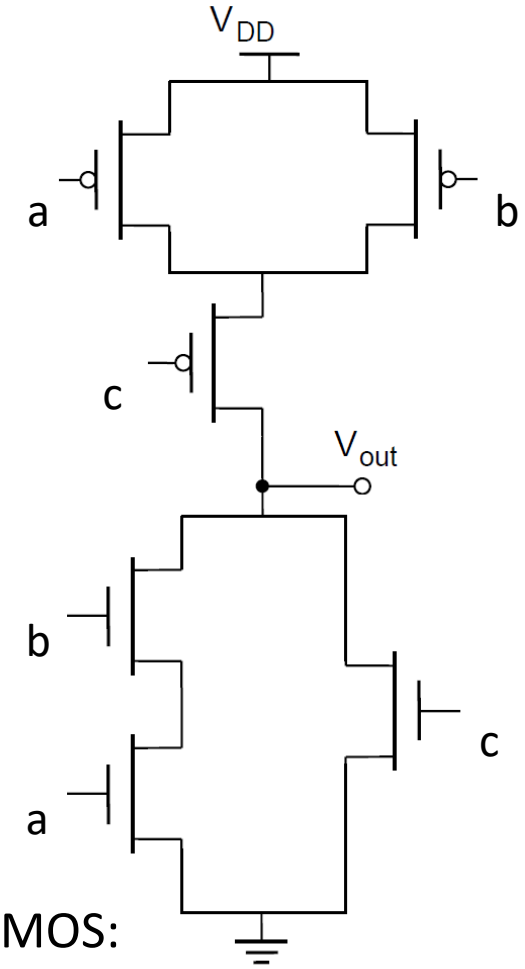


CMOS Logic Gates

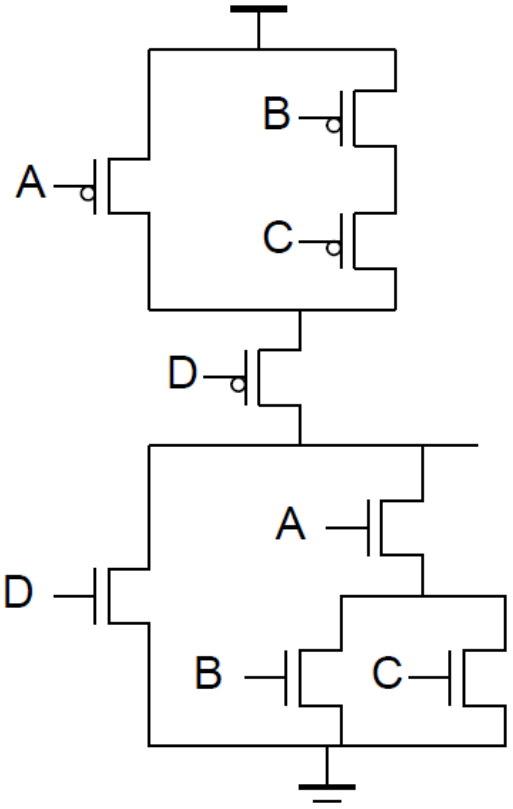
NOR GATE $f=\overline{a+b}$



$f=\overline{(a \cdot b)+ c}$



$f=\overline{D + A \bullet (B + C)}$

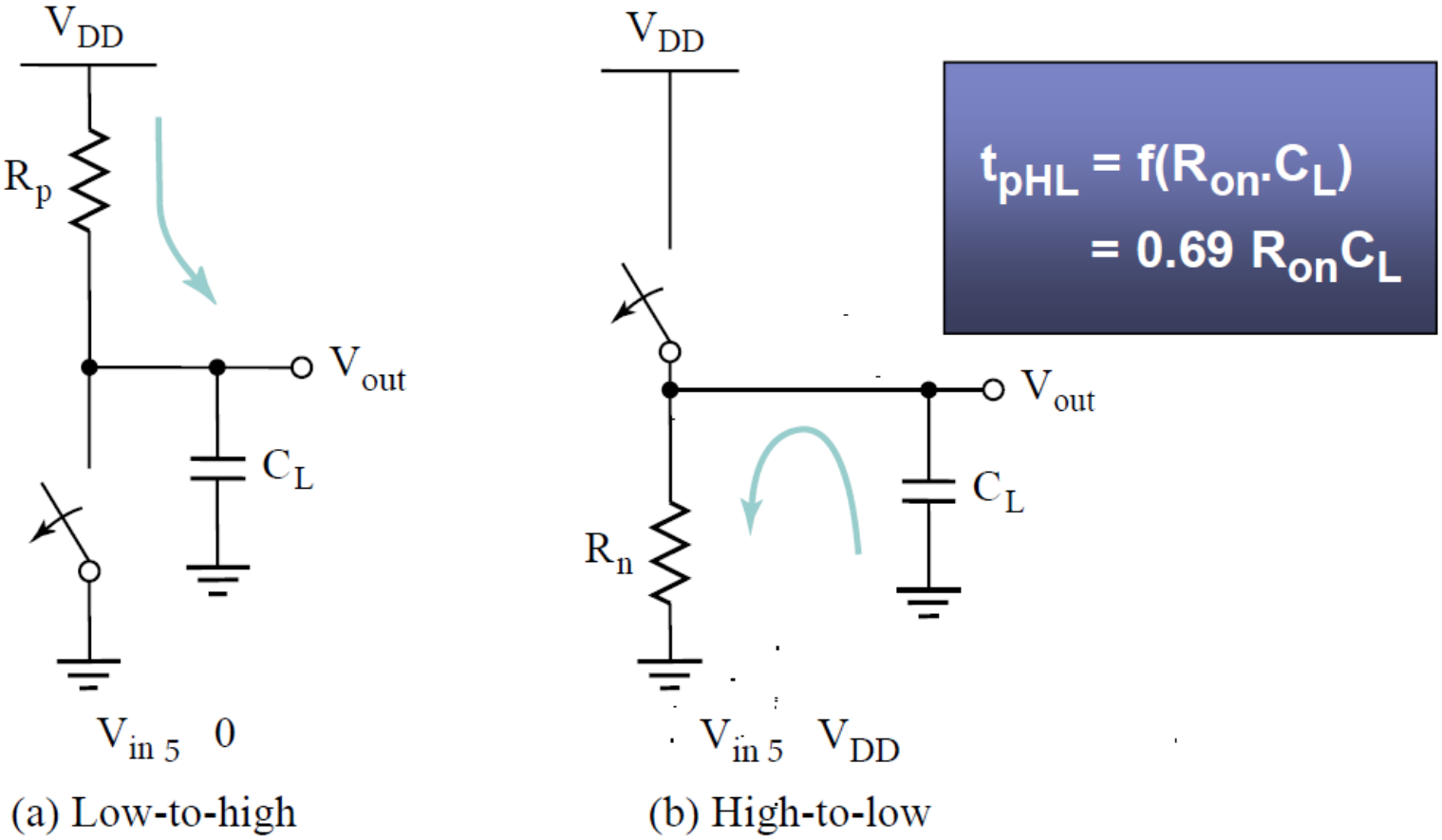


Looking at NMOS:

- Transistors in **serial** make **logic products**
- Transistors in **parallel** make **logic additions**
- Output is **inverted**

CMOS gates characteristics

Delay



$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

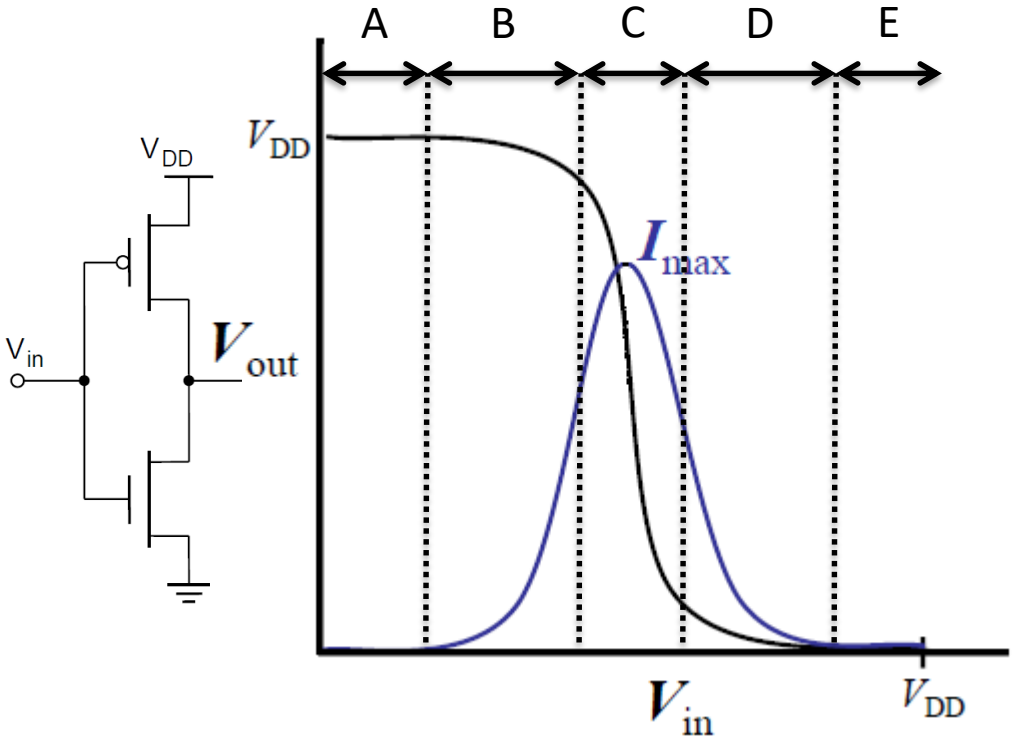
We can manufacture transistors so that $R_p = R_n$

$\tau_{PLH} = \tau_{PHL}$

Symetric propagation times ¡¡¡¡

CMOS gates characteristics

Power Consumption



➢ A=> NMOS Cut-off	No power
➢ B=> NMOS Ohmic PMOS Sat	Consumption limited by N
➢ C=> NMOS Sat PMOS Sat	High Consumption
➢ D=> NMOS Sat PMOS Ohmic	Consumption limited by P
➢ E=> PMOS Cut-off	No power

$P_{dynamic}=freq \cdot C \cdot V_{DD}^2$

CMOS gates characteristics

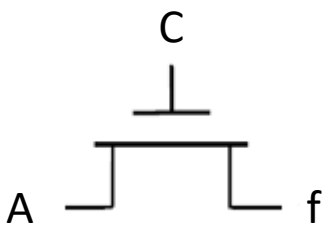
Logic gates Size

- We know that $\mu_n = 2.5 \cdot \mu_p$
- Usually transistors are designed so that L is as small as possible
  - $L_n = L_p$
  - W must be different => Width of P must be bigger
  - $\frac{1}{2}\frac{W_n}{L_n}\mu_n C_{ox} = \frac{1}{2}\frac{W_p}{L_p}\mu_p C_{ox}$
- PMOS transistors need to be 2.5 times (W) bigger than NMOS

Pass transistors

Use of transistors as switches between driving circuits and load circuits are called pass transistors

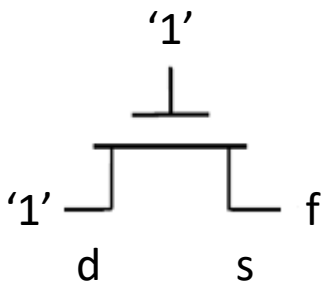
NMOS



C	A	f
0	0	Z
0	1	Z
1	0	0
1	1	$1-V_t$

High impedance

"weak" '1'



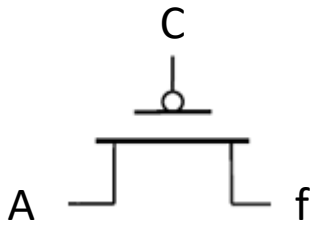
$v_{DS} = v_{DG} - v_{GS} = 0 + v_{GS}$

$v_{GS} > v_t \longrightarrow v_{DS} > v_t$

$v_D - v_S > v_t \longrightarrow v_S < v_D - v_t$

$v_S = 1 - v_t$ Degradation!!!

PMOS



C	A	f
0	0	V_t
0	1	1
1	0	Z
1	1	Z

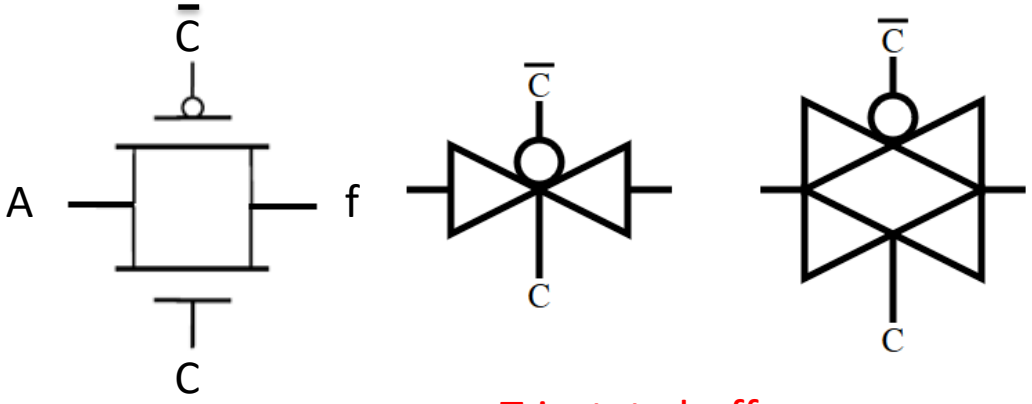
"weak" '0'

CMOS Transmissions gates

- A CMOS transmission gate can be constructed by parallel combination of NMOS and PMOS
  with complementary gate signals.

- The main advantage of the CMOS transmission gate compared to pass transistors is to allow the input signal to be transmmited to the output without the threshold voltage attenuation

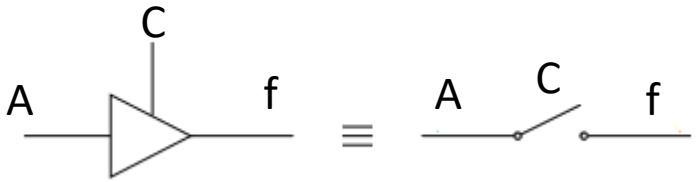
4 Transistors => 2 transmission gate; 2 Inverter



C	A	f
0	0	Z
0	1	Z
1	0	0
1	1	1

A

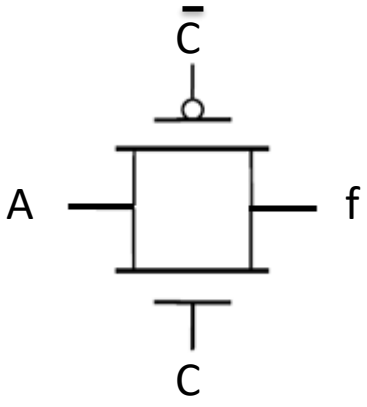
Triestate buffer



CMOS Transmissions gates

C=0
- A=0
  - V_{GSn}= 0 - 0 ⟶ Cut-off
  - V_{GSp}= 5 - 0 ⟶ Cut-off
- A=1
  - V_{GSn}= 0 - 5 ⟶ Cut-off
  - V_{GSp}= 5 - 5 ⟶ Cut-off

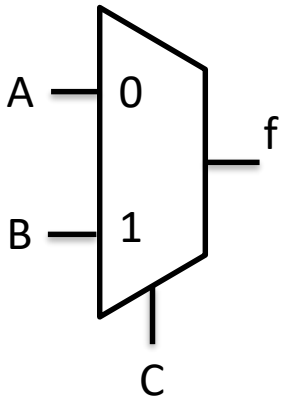
C=1
- A=0
  - V_{GSn}= 5 - 0 ⟶ Conduction
  - V_{GSp}= 0 - 0 ⟶ Cut-off
- A=1
  - V_{GSn}= 5 - 5 ⟶ Cut-off
  - V_{GSp}= 0 - 5 ⟶ Conduction



- C='0', ⟹ High impedance, both transistors are cut-off
- C='1', A='0' ⟹ N conducts ⟹ Puts '0'
- C='1', A='1' ⟹ P conducts ⟹ Puts '1'

Logic gates with Transmissions gates

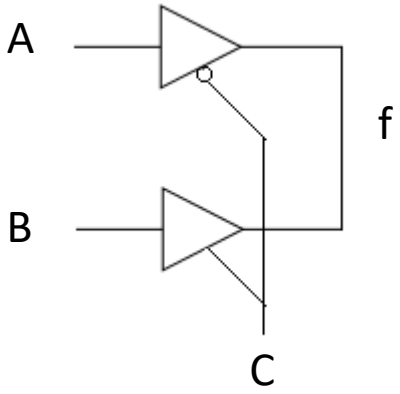
Multiplexer



C	A	B	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

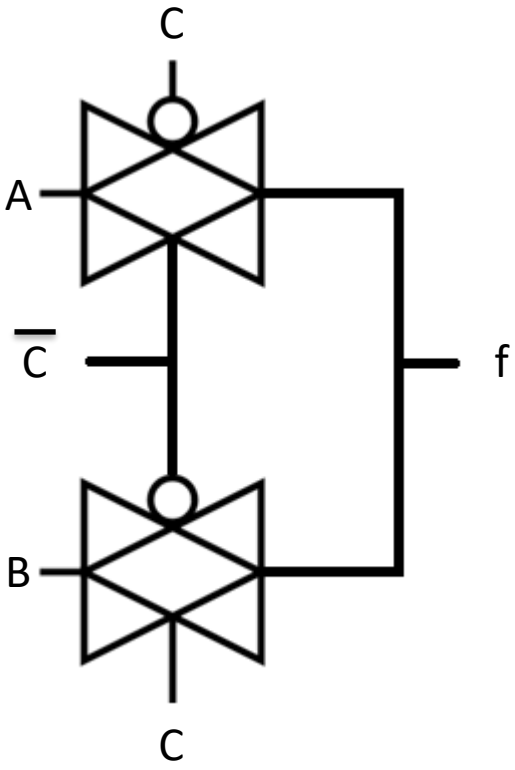
A

B



C=0 → f=A

C=1 → f=B



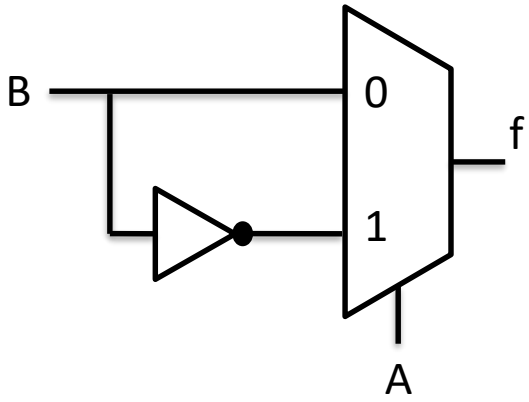
6 transistors¡¡¡

4 for Transmission gates

2 for Inverter

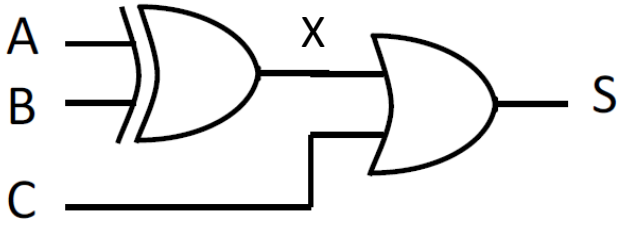
Logic gates with Transmissions gates

XOR



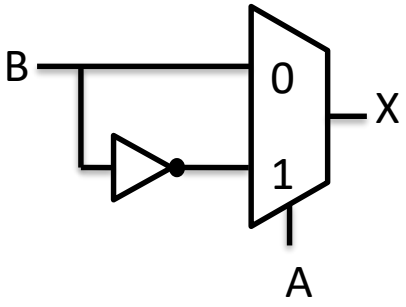
A	B	f	
0	0	0	B
0	1	1	
1	0	1	$\overline{B}$
1	1	0	

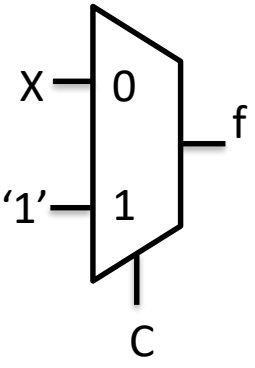
8 Transistorsiiii

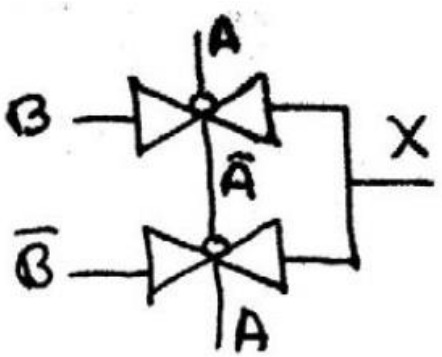


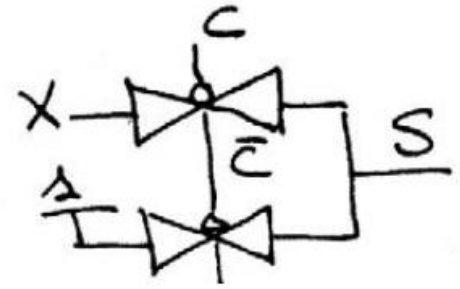
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

C	X	S	
0	0	0	B
0	1	1	
1	0	1	1
1	1	1	









Logic gates with Transmissions gates

D-latch (level triggered bistable)