Universidad
Carlos III de Madrid
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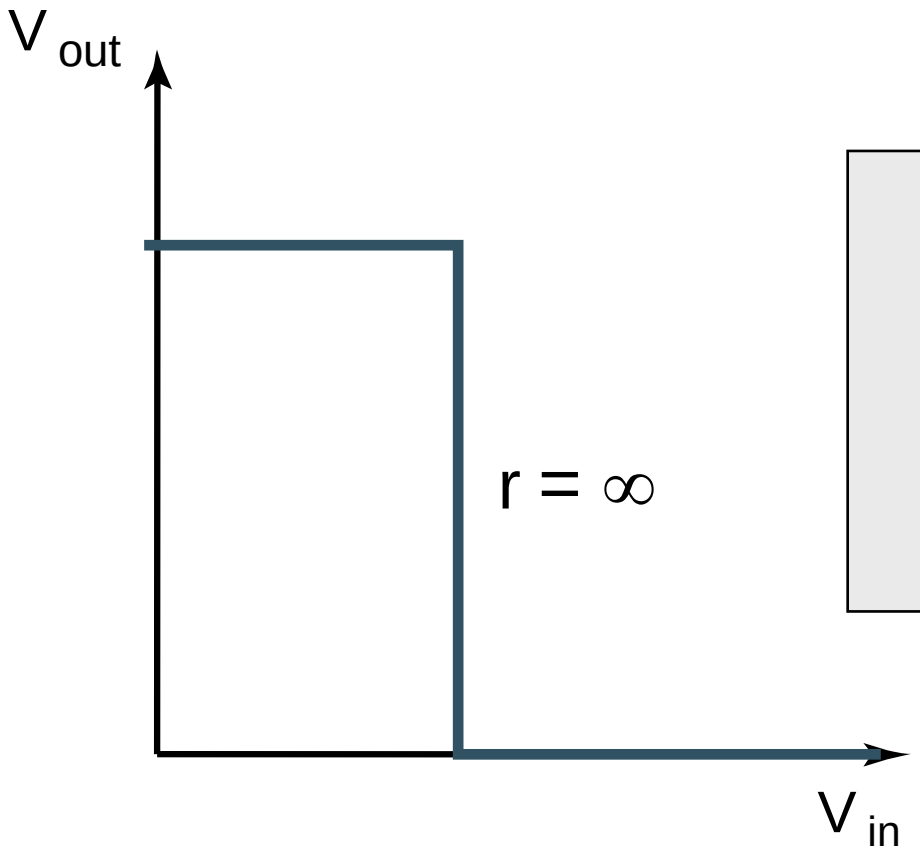
MOS technoloies: review

Ideal inverter



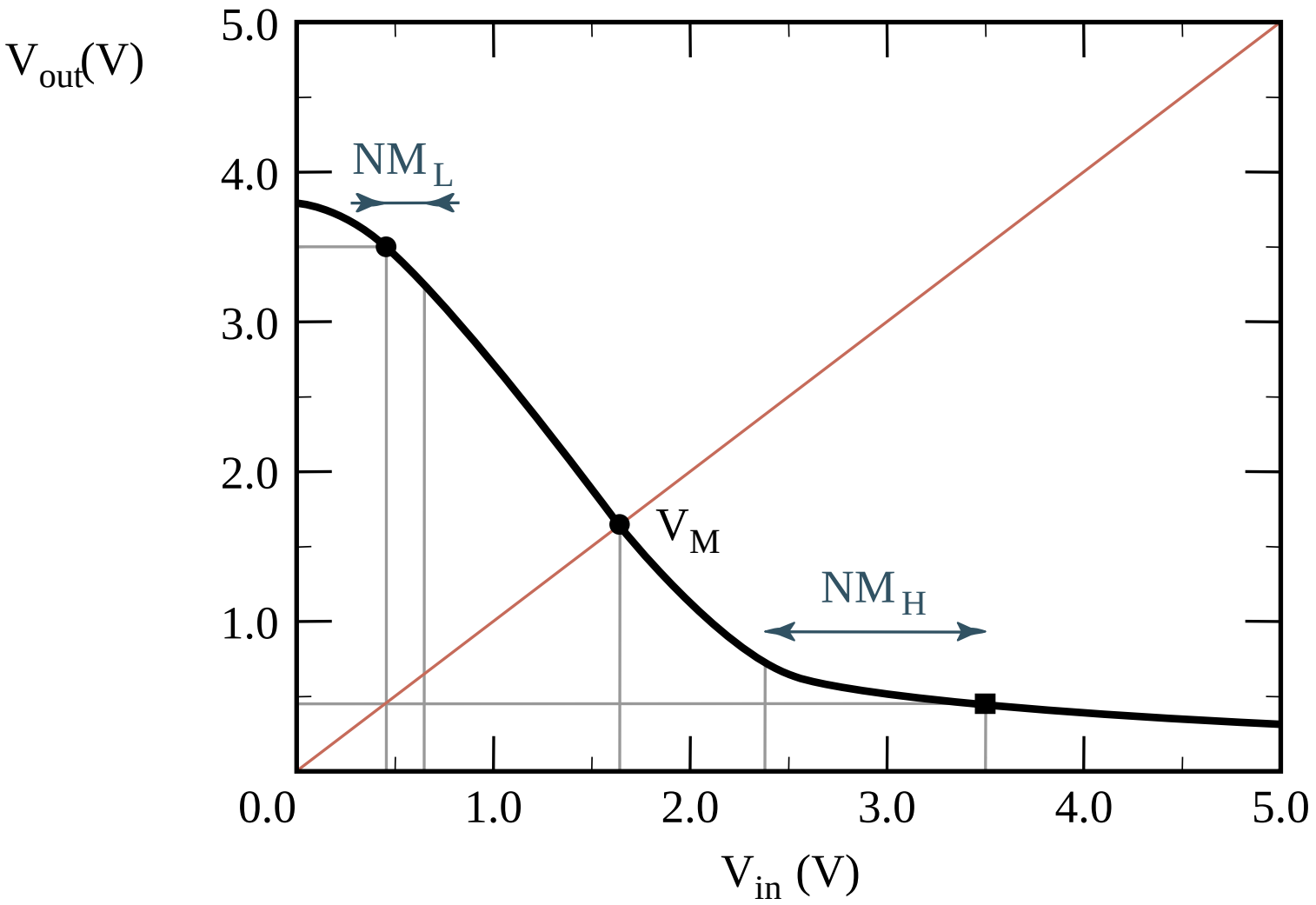
$R_i = \infty$

$R_o = 0$

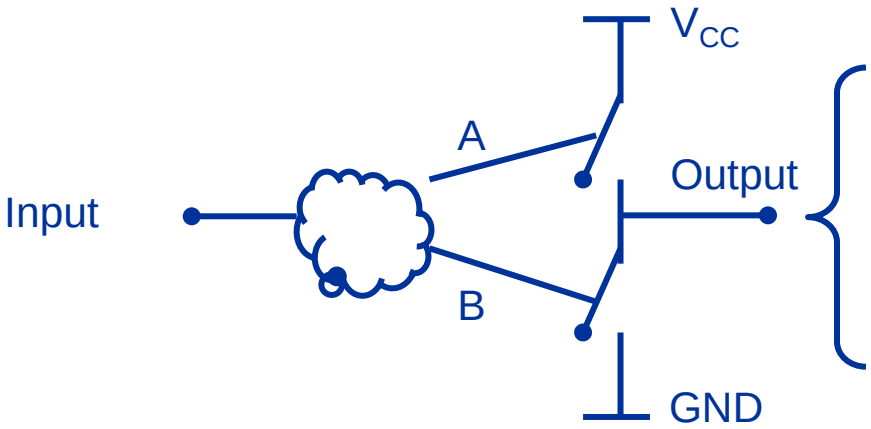
Fanout = ∞

$NM_H = NM_L = V_{DD}/2$

Real inverter



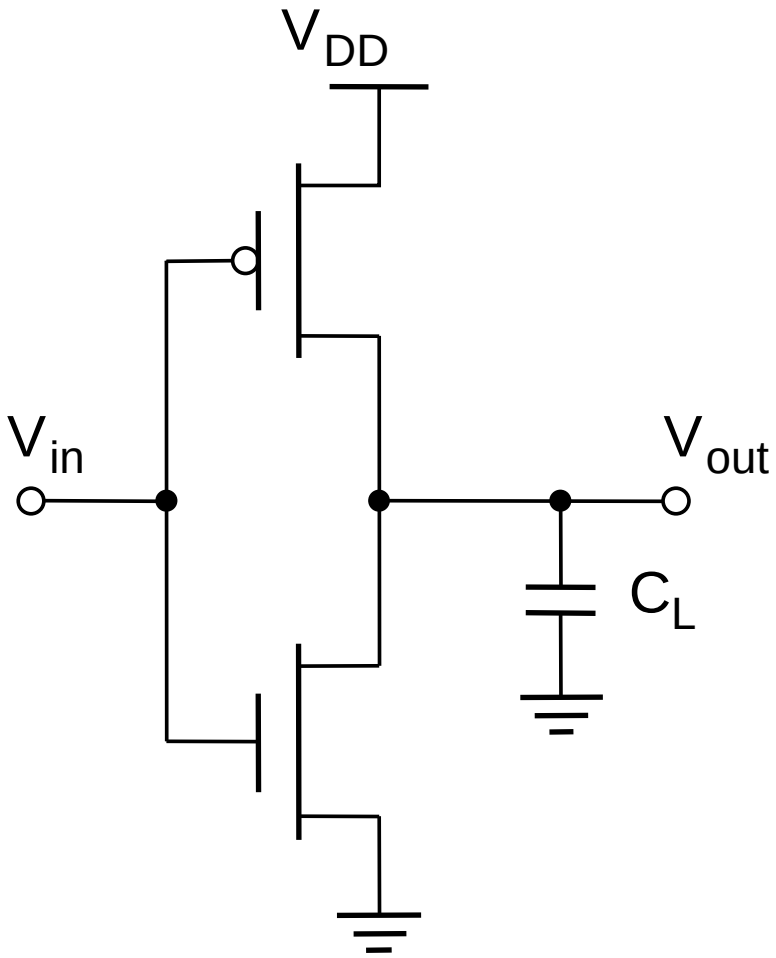
Inverter: operation

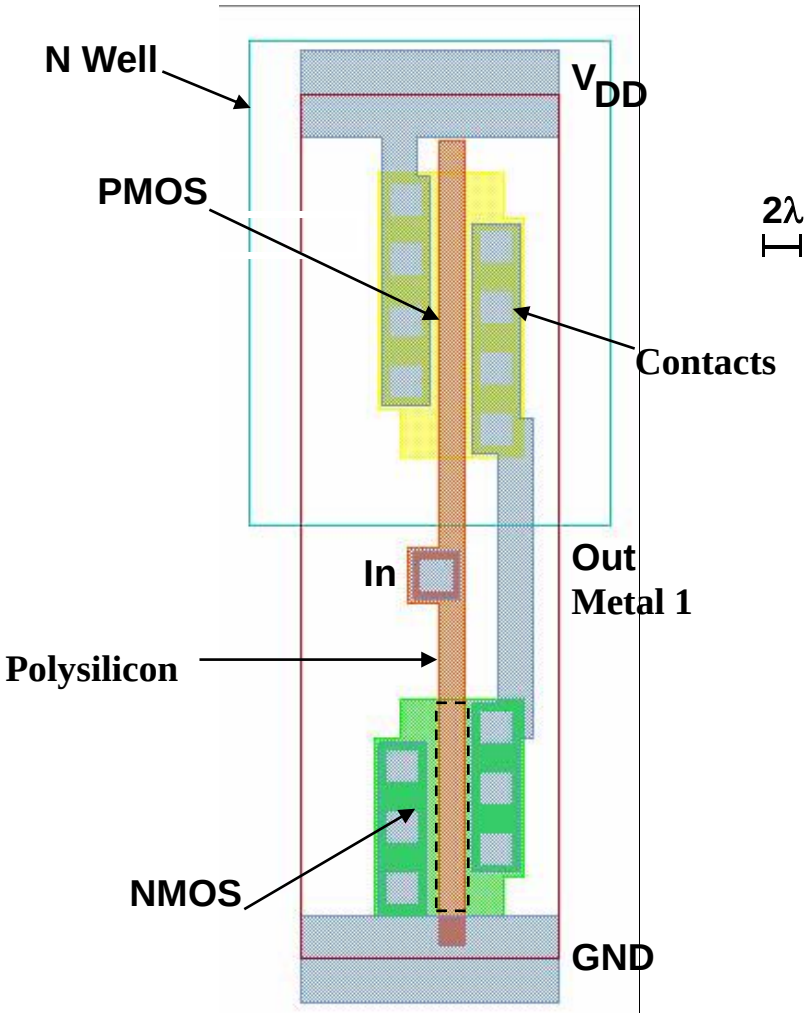


Output = ‘1’ if A closes the path to V_{CC}

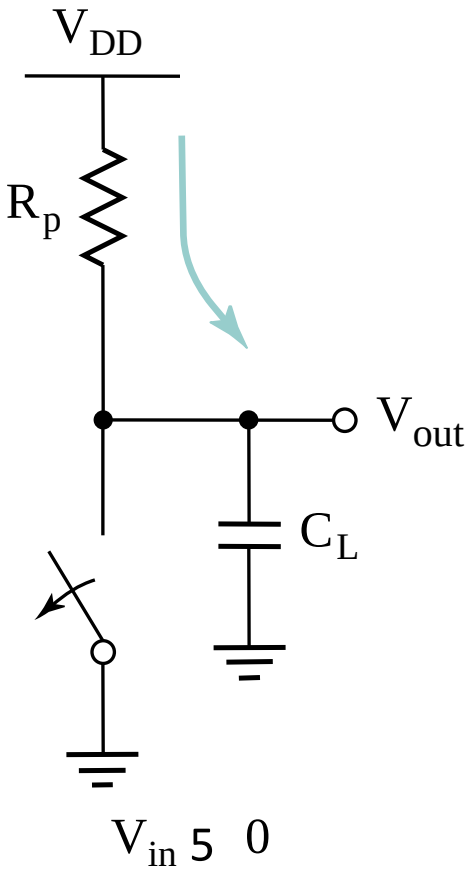
Output = ‘0’ if B closes the path to GND

CMOS inverter

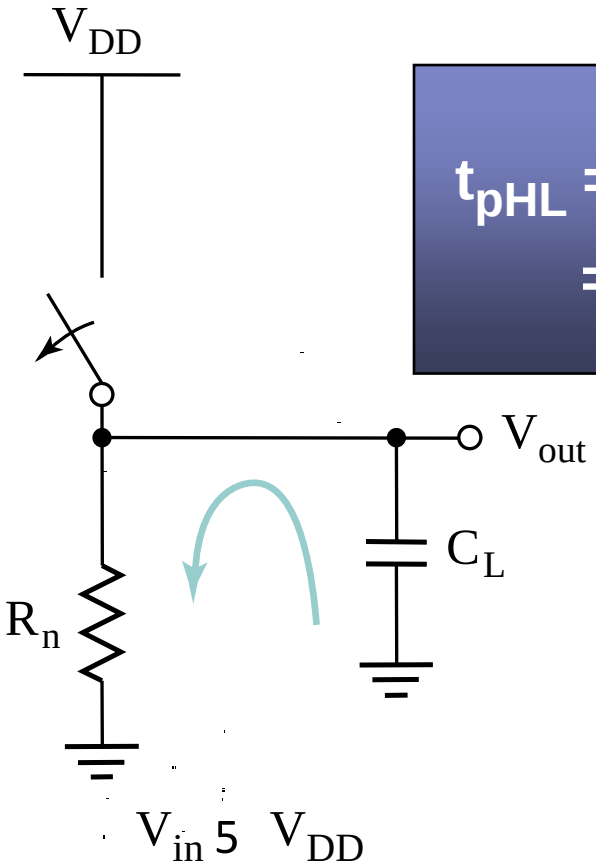




CMOS inverter : delays



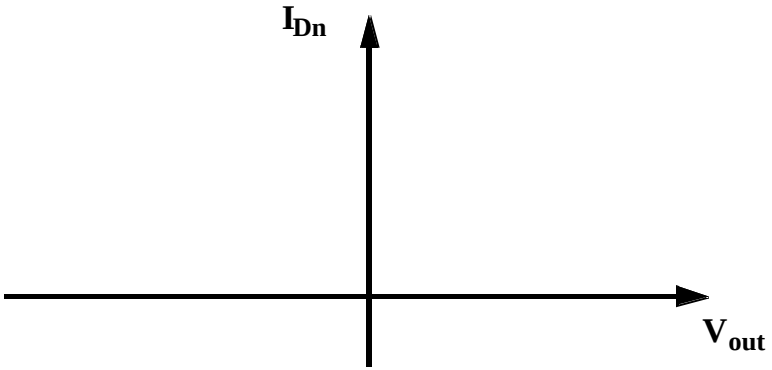
(a) Low-to-high

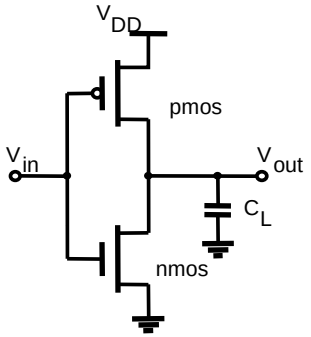


(b) High-to-low

$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

CMOS inverter: pmos loads

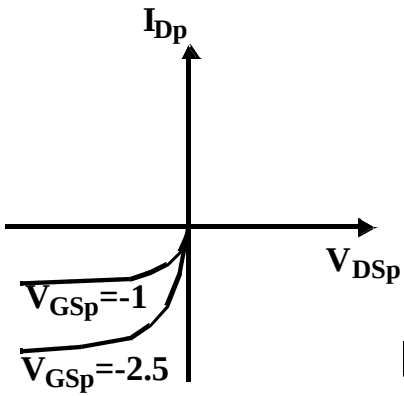


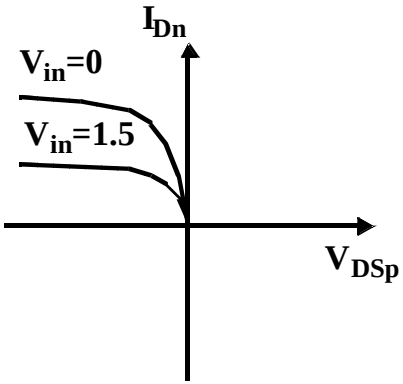


$V_{in} = V_{DD} + V_{GSp}$

$I_{Dn} = - I_{Dp}$

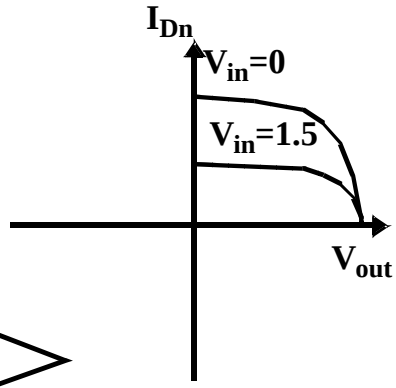
$V_{out} = V_{DD} + V_{DSp}$





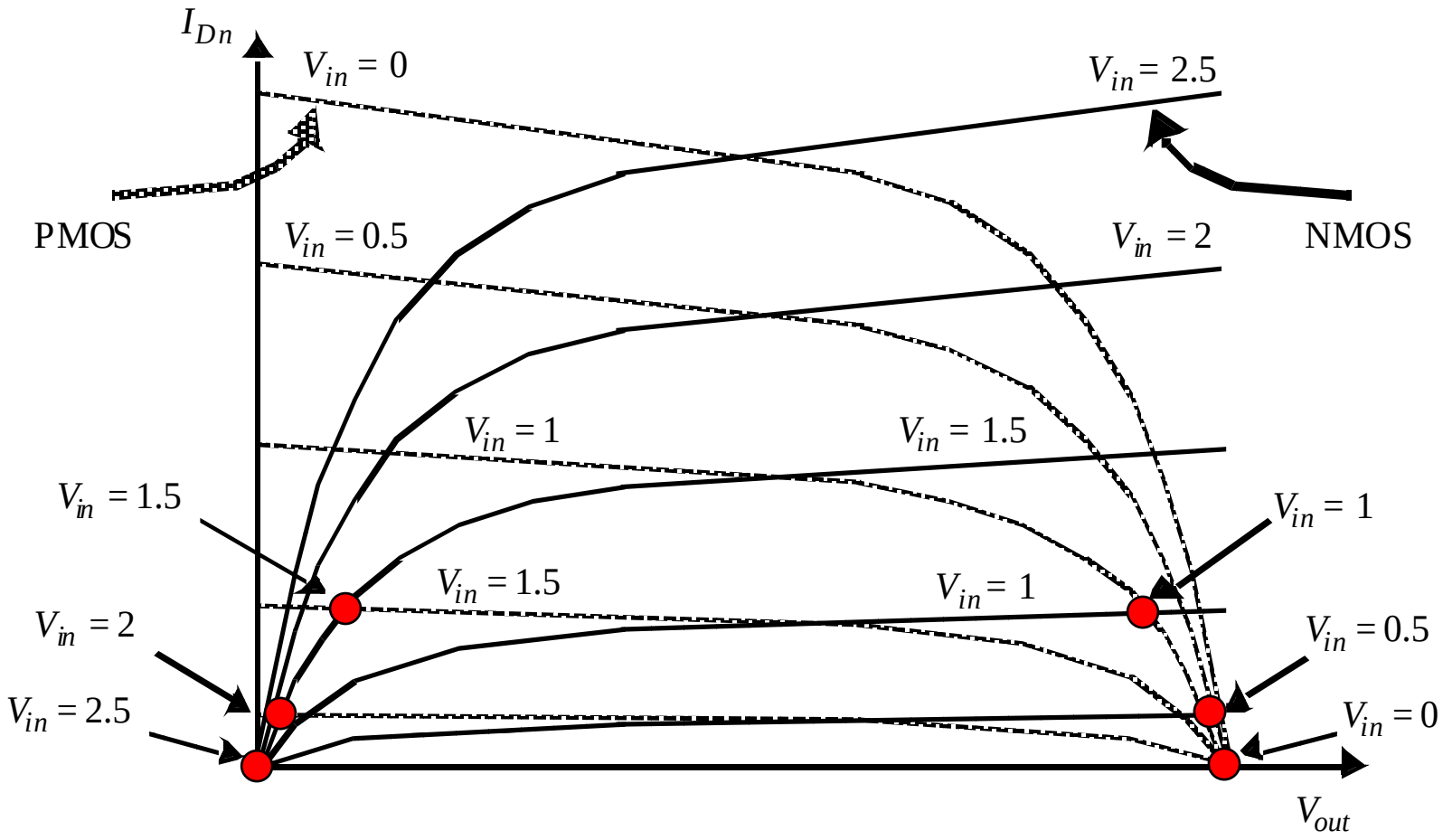
$V_{in} = V_{DD} + V_{GSp}$

$I_{Dn} = - I_{Dp}$

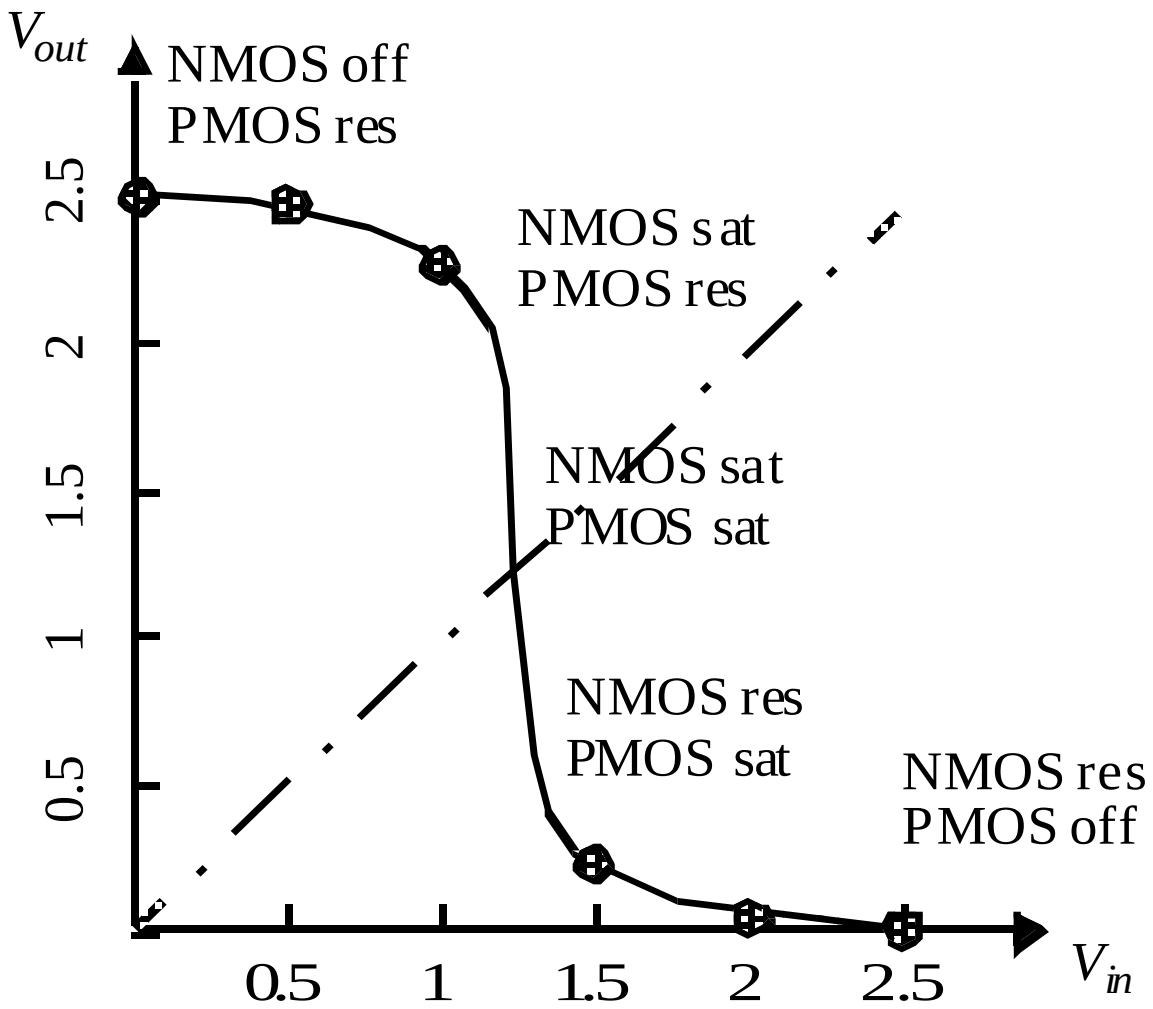


$V_{out} = V_{DD} + V_{DSp}$

CMOS inverter: transfer function



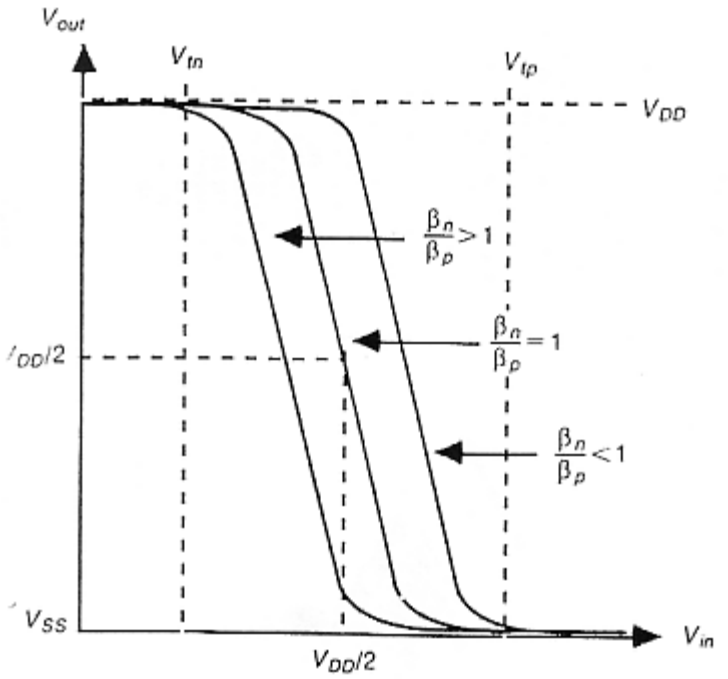
CMOS inverter: transfer function



CMOS inverter

$$\beta_n = \frac{\varepsilon_0 \cdot \varepsilon_{ais}}{D} \mu_n \frac{W_n}{L_n} = K \mu_n \frac{W_n}{L_n}$$

$$\beta_p = \frac{\varepsilon_0 \cdot \varepsilon_{ais}}{D} \mu_p \frac{W_p}{L_p} = K \mu_p \frac{W_p}{L_p}$$

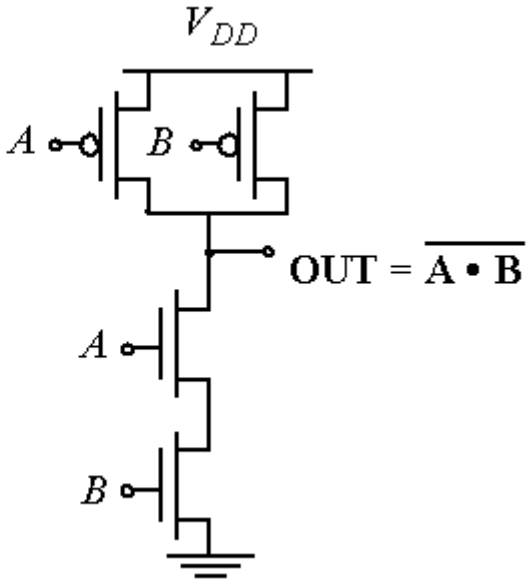


RACTERÍSTICA DE TRANSFE-
ENCIA, EN FUNCIÓN DE LA
ELACIÓN β_n/β_p

NAND CMOS

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

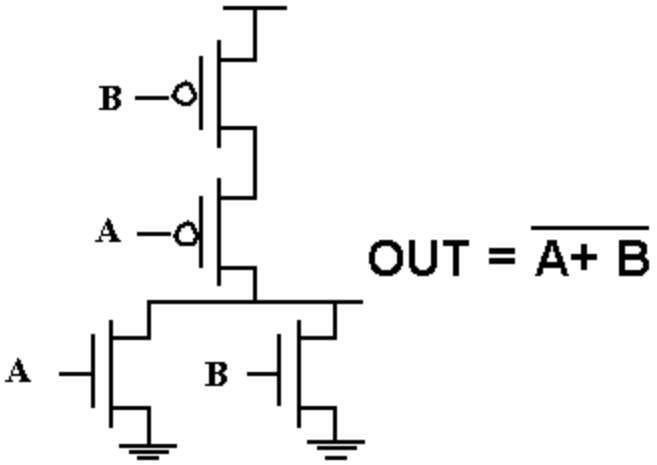
Truth Table of a 2 input NAND gate



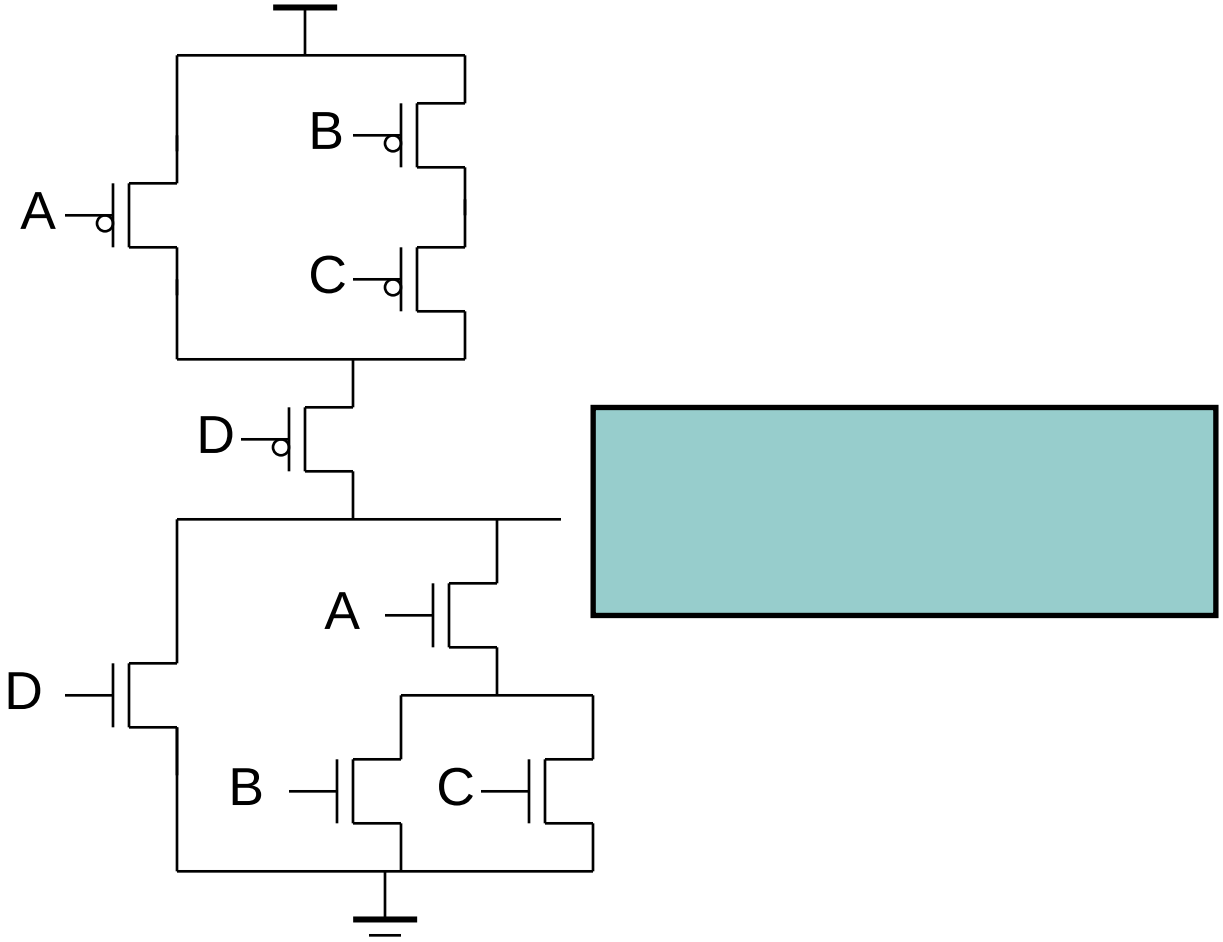
NOR CMOS

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

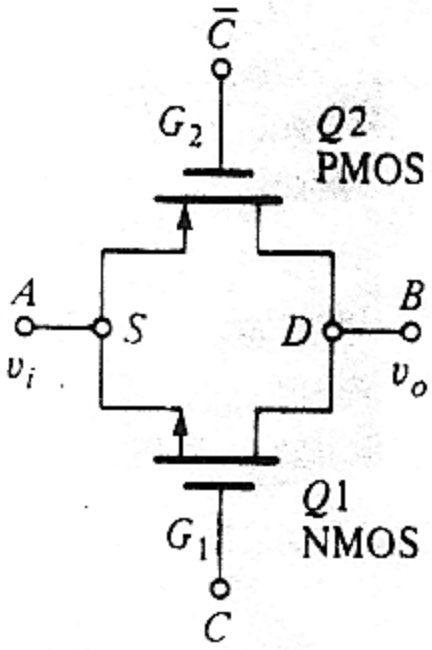
Truth Table of a 2 input NOR gate



CMOS Gate



CMOS transmission gate



References

- Electrónica Digital. Dpto. Tecnología Electrónica. OCW UC3M
- Rabaey (Digital Integrated Circuits: A Design Perspective)