



# MANUFACTURING AND PACKAGING OF INTEGRATED CIRCUITS

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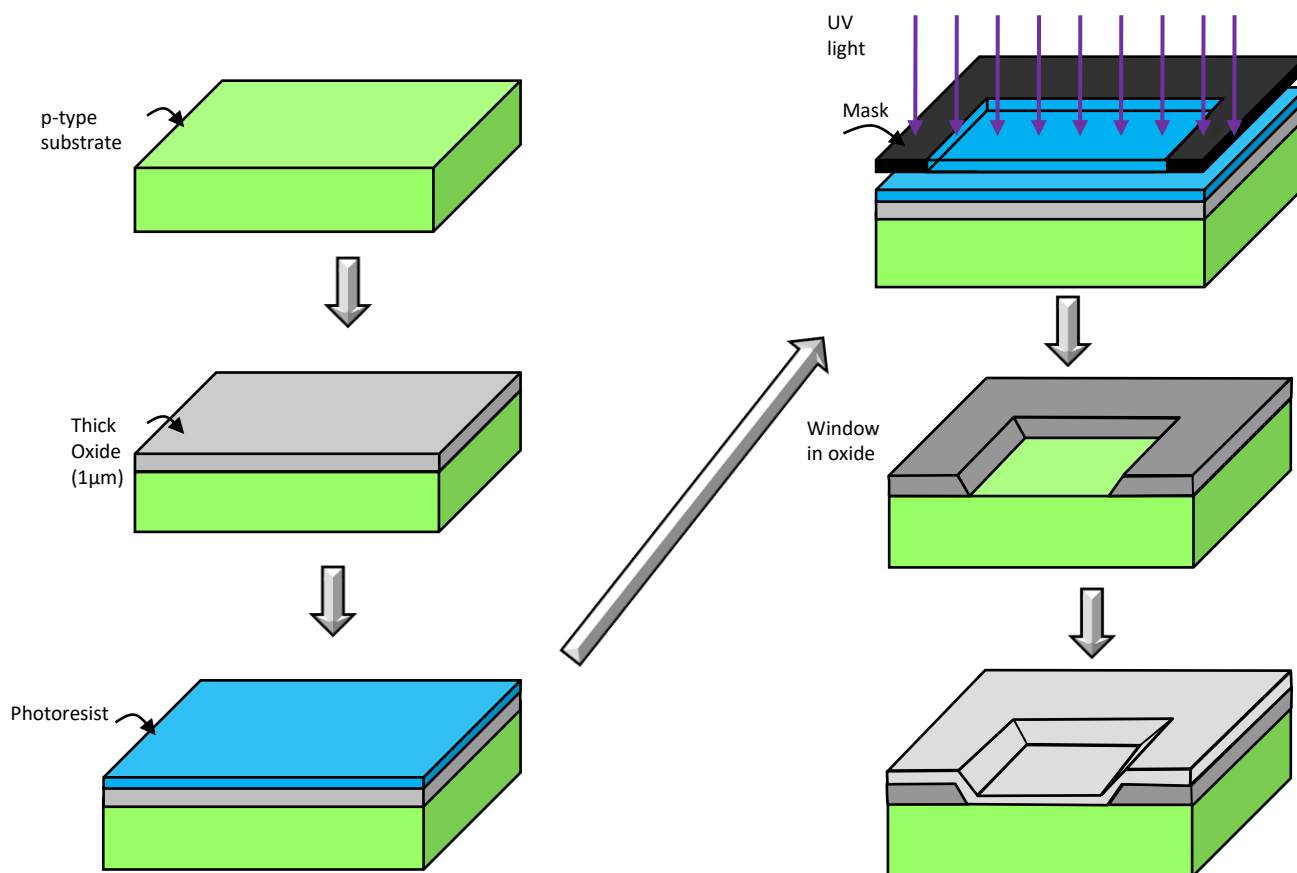
Luis Entrena

Enrique San Millán

## Outline

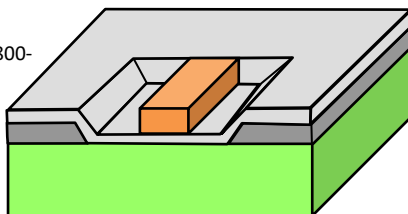
- The manufacturing process of a CMOS circuit
  - Making an NMOS Transistor
  - Manufacturing an inverter
    - Single well
    - Double well (Twin-tub)
- ICs packaging
- Application Specific ICs: types and characteristics

# NMOS transistor manufacturing (1/2)

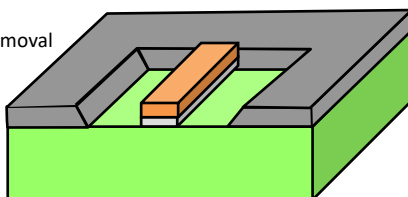


## NMOS transistor manufacturing(2/2)

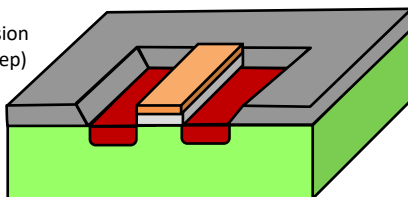
Patterned poly (1-2  $\mu\text{m}$ ) on thin oxide (800-1000  $\text{\AA}$ )



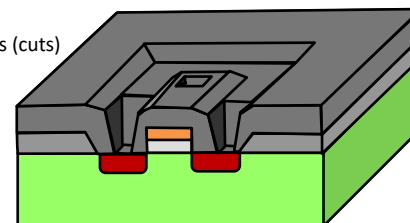
Thin oxide removal



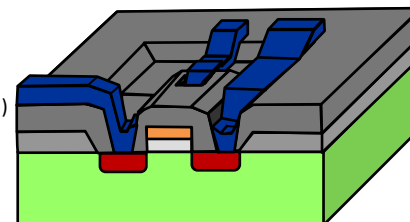
n+ diffusion  
(1  $\mu\text{m}$  deep)



Contact holes (cuts)

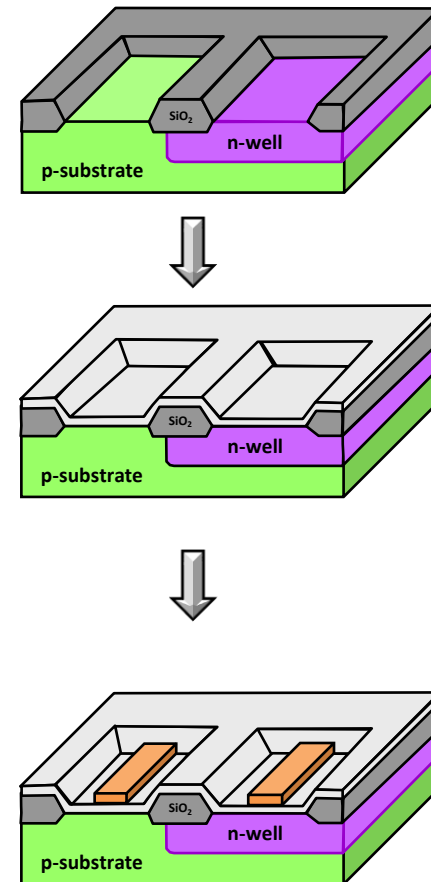
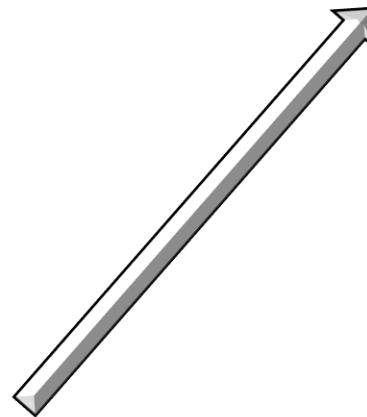
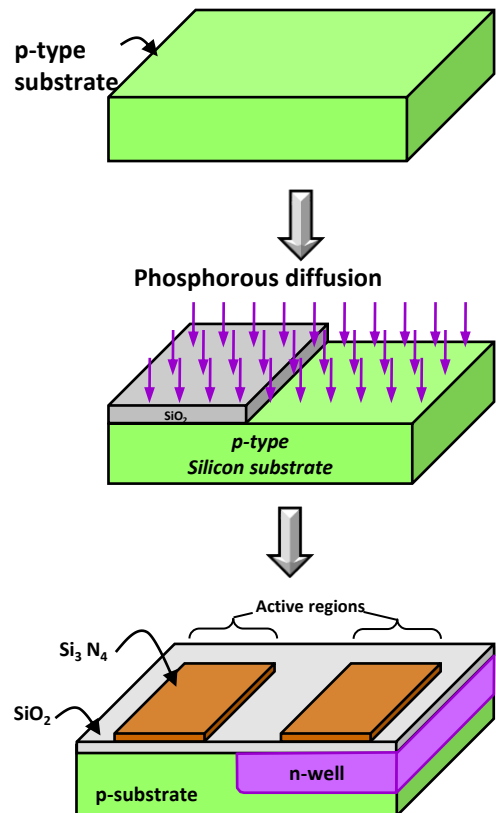


Patterned metallization  
(aluminum 1  $\mu\text{m}$ )



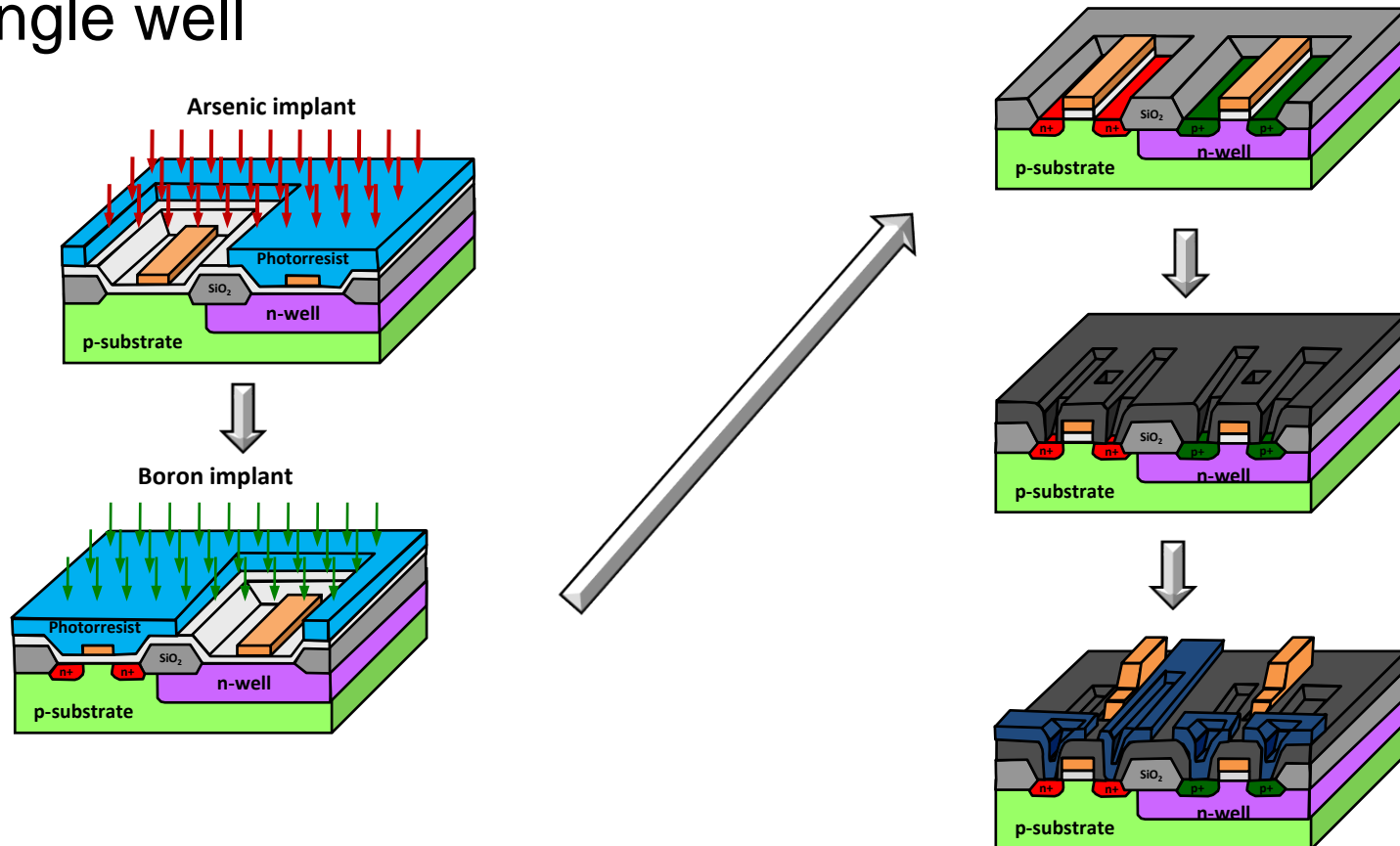
# CMOS inverter manufacturing(1/3)

## ■ Un pozo



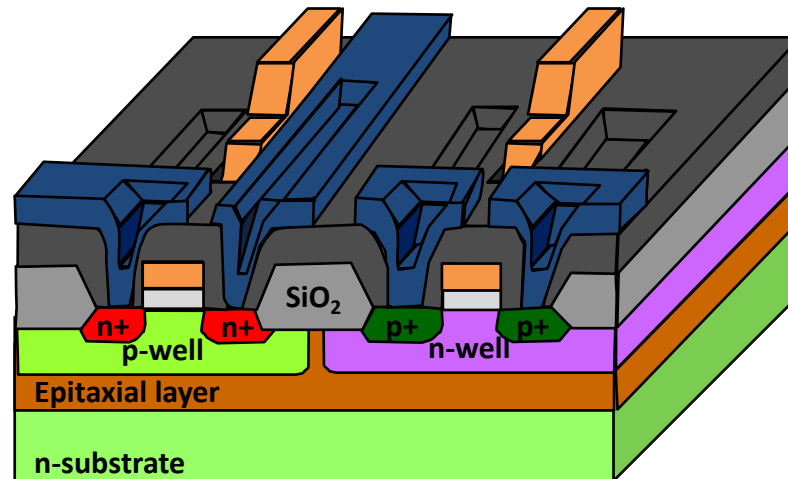
# CMOS inverter manufacturing(2/3)

## ■ Single well



## CMOS inverter manufacturing(3/3)

### ■ Double well (twin-tub)



# Packaging

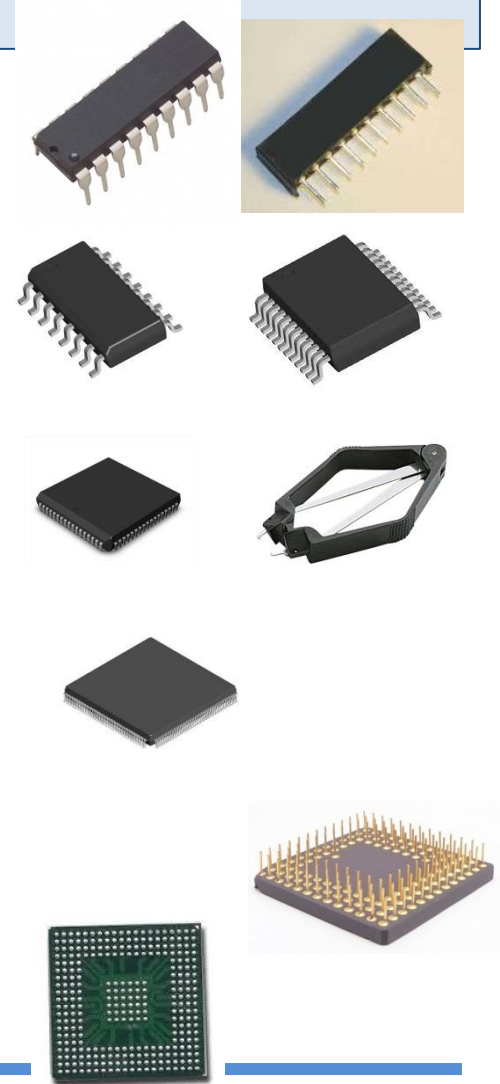
## ■ Functions:

- Isolation. Isolate the circuit from external agents, such as dust or moisture.
- Connectivity. The terminals allow you to connect the inputs and outputs of the chip to the tracks of a board.
- Dissipation. In their normal operation, circuits produce heat, which must be dissipated. That heat must pass through the encapsulation. It may be necessary to add a heatsink, attached to the surface of the package, in case the package does not dissipate sufficiently.
- Manipulation. Since an integrated circuit is very fragile, the package makes it easy to handle, place and assemble.

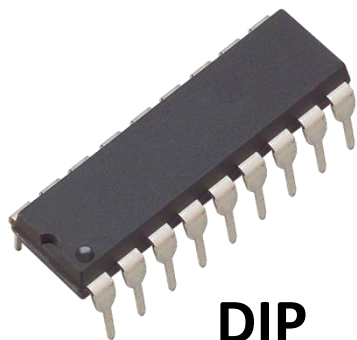


# Packaging : Types

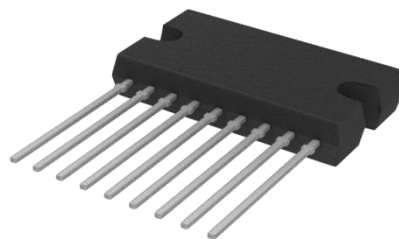
Tipo	Nº pines	Montaje
DIP (Dual In-Line Package) SIP (Single In-Line Package) ZIP (Zig-Zag In-Line Package)	5-64	Insertion
SOIC (Small Outline Integrated Circuit) TSOP (Thin Small Outline Package) SSOP (Shrink Small Outline Package) TSSOP (Thin Shrink Small Outline Package) QSOP (Quarter-size Small Outline Package) VSOP (Very Small Outline Package)	8-32	Surface mount
LCC (Leaded Chip Carrier) PLCC (Plastic Leaded Chip Carrier) CLCC (Ceramic Leaded Chip Carrier)	16-200	Surface mount Insertion through socket
FP (Flat Pack) QFP (Quad Flat Pack) PQFP (Plastic Quad Flat Pack) CQFP (Ceramic Quad Flat Pack) TQFP (Thin Quad Flat Pack) LQFP (Low profile Quad Flat Pack)	10-300	Surface mount
PGA (Pin Grid Array) PPGA (Plastic Pin Grid Array) CPGA (Ceramic Pin Grid Array)	68-500	Insertion
BGA (Ball Grid Array)	>500	Surface mount



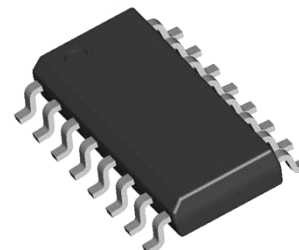
## Packaging : Types



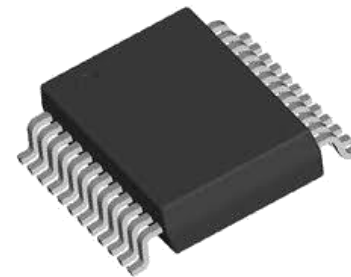
**DIP**



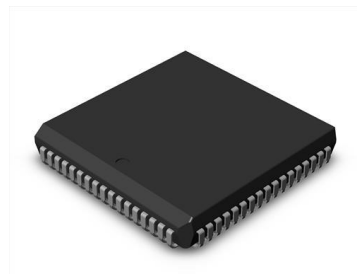
**SIP**



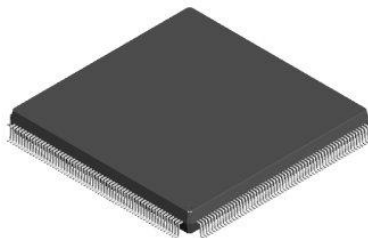
**SOIC**



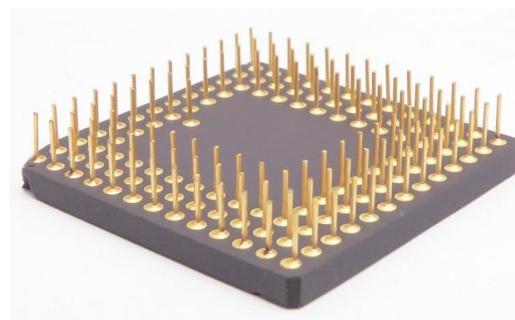
**SSOP**



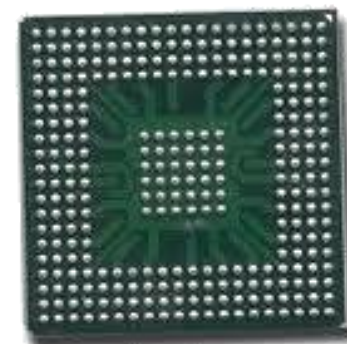
**PLCC**



**QFP**



**PGA**



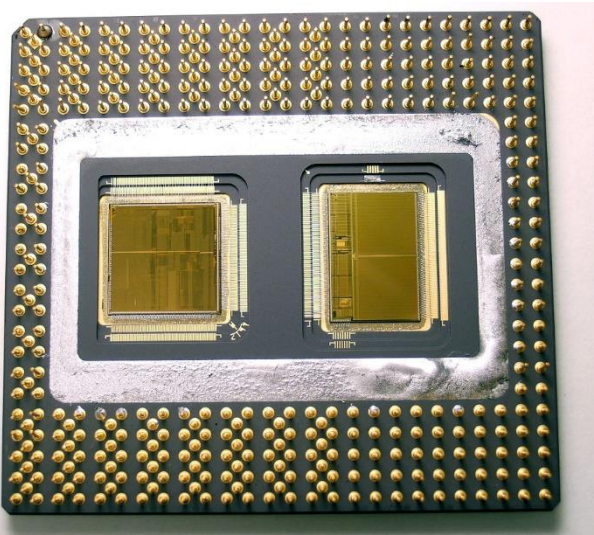
**BGA**

## Packaging : Multi-chip modules

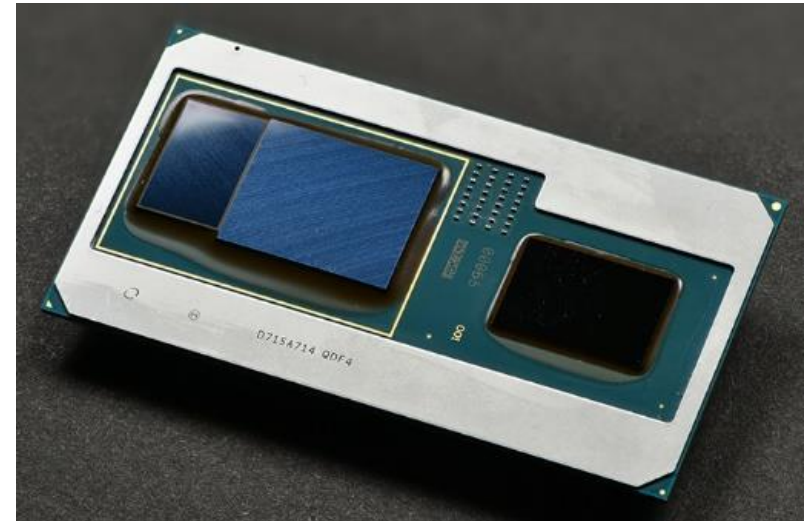
- Multi-Chip Modules (MCM)
- It is an encapsulation that includes several circuits mounted on the same base and connected to each other, so that they can be used as if they were a single chip.
- There are different types with different degrees of integration
- Examples: Pentium Pro, Xenos (Xbox GPU)

Type	Line density (cm/cm <sup>2</sup> )	Line width ( $\mu$ m)	Separation ( $\mu$ m)	Description
MCM-L	30	750	2250	Laminated multi-chip module. The substrate is a multilayer printed circuit board (PCB). Low integration.
MCM-C	20-40	125	125-375	Multi-chip ceramic substrate module. Medium integration.
MCM-D	200-400	10	10-30	Multi-chip module deposited on silicon substrate. High integration.

## Packaging : Multi-chip modules



**Pentium-Pro  
(CPU+cache)**



**Core i7-8809G  
(CPU+GPU)**



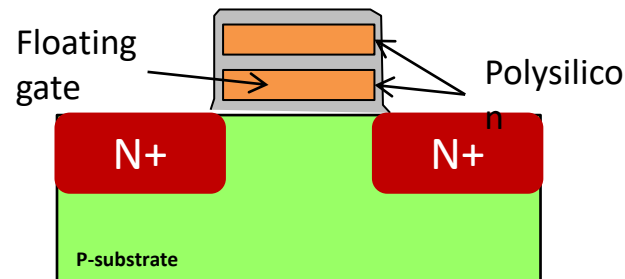
**AMD Radeon E9170  
(GPU+memoria)**

## Application Specific CIs

- ASICs (Application Specific Integrated Circuit): digital, analog or mixed circuits.
- Deployment Types
  - Full-custom
  - Partially custom
    - Partially prefabricated: gate array
    - Partially pre-designed: standard cells and macrocells, IP blocks (Intellectual Property)
  - Fully prefabricated circuits: programmable circuits
    - CPLDs (Complex Programmable Logic Devices)
    - sRAM FPGAs (Field-Programmable Gate Arrays)
    - Antifuse FPGAs

## Application Specific CIs

- Programmable circuits: CPLDs
  - Programming Technology: Floating Gate MOS Transistor



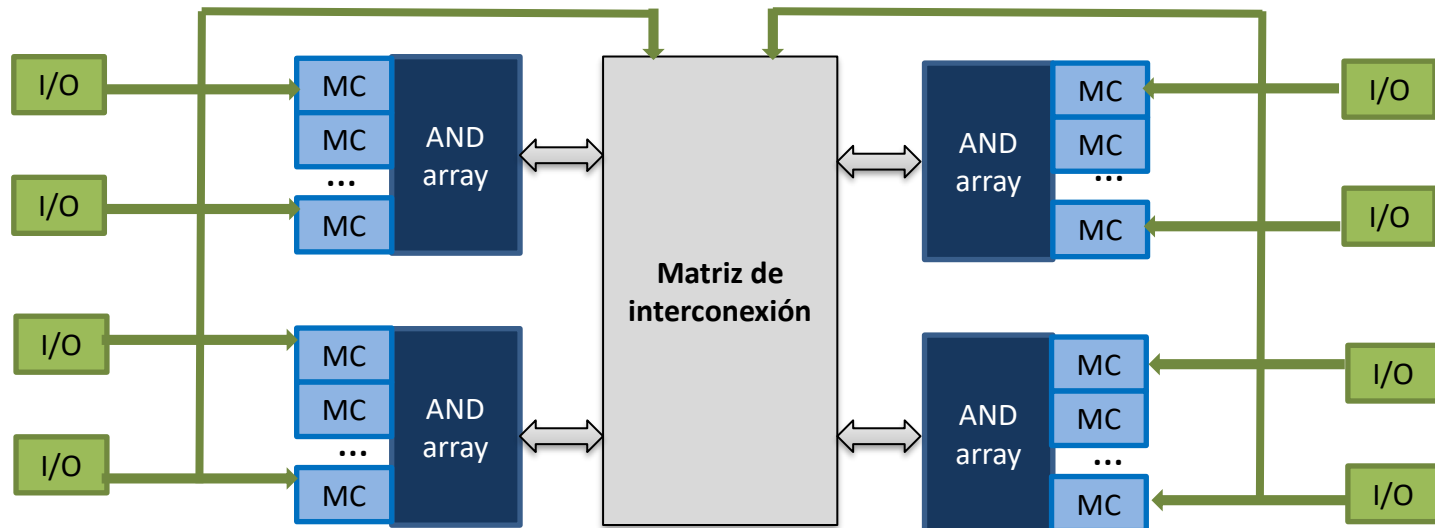
- When the transistor is not programmed, it acts in conventional mode.
- Programmable threshold voltage.
  - By applying a sufficiently large voltage to the gate it is possible to provide the carriers with enough energy to pass through the oxide and be trapped in the floating gate. When the voltage is eliminated the cell is charged (programmed)
- Non-volatile devices
- Reprogrammables
- High power consumption

# Application Specific CIs

## ■ Programmable circuits: CPLDs

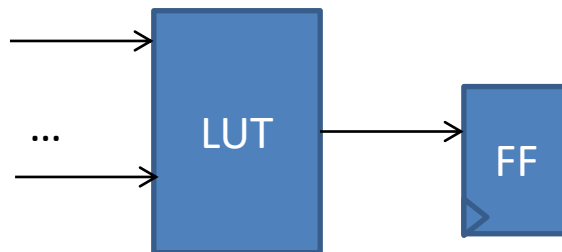
### ■ Basic structure

- Programmable interconnections
- Logical blocks: product terms and bistable macrocells, inverters and multiplexers.
- I/O Cells



## Application Specific CIs

- Programmable circuits: sRAM FPGAs
  - Programming technology: SRAM memory cells for circuit configuration storage
  - Basic cell
    - Flip-flop
    - Look-up Table, LUT

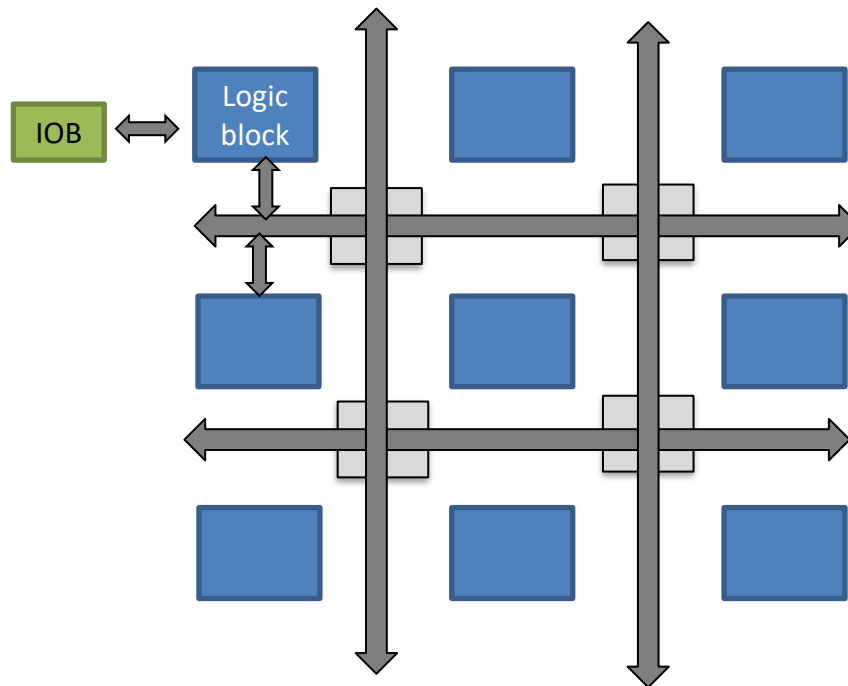


- Volatile devices
- Reprogrammables
- Greater integration capacity → Greater complexity
- Possibility of dynamic reconfiguration



# Application Specific CIs

- Programmable circuits: sRAM FPGAs
  - Structure consists of a matrix distribution of logical cells communicated with each other and with the input and output blocks (IOBs) through programmable routing channels



# Application Specific CIs

- Programmable circuits: antifuse FPGAs
  - Programming technology: Antifuses. The necessary connections are short-circuited during programming. The programming is done by subjecting the antifuse (two electrodes separated by a thin layer of insulator) to a high voltage that breaks the dielectric creating a permanent short circuit
  - They are non-volatile
  - Non-reprogrammable
  - Fast → high-speed applications
  - Electrical stability → high reliability and robustness
  - Specific programmers are needed to supply voltage pulses of adequate duration and value
  - Structure: Only interconnections are programmed, so that basic cells perform a fixed logical function.