CMOS INTEGRATED CIRCUITS FABRICATION PROCESSES

Outline

- Fundamental processes
  - Wafer manufacture
  - Thermal oxidation
  - Doping processes
    - Ion implantation
    - Solid-state diffusion
  - Photolithography
  - Thin-film removal
  - Thin-film deposition

- CMOS process sequence (process flow)

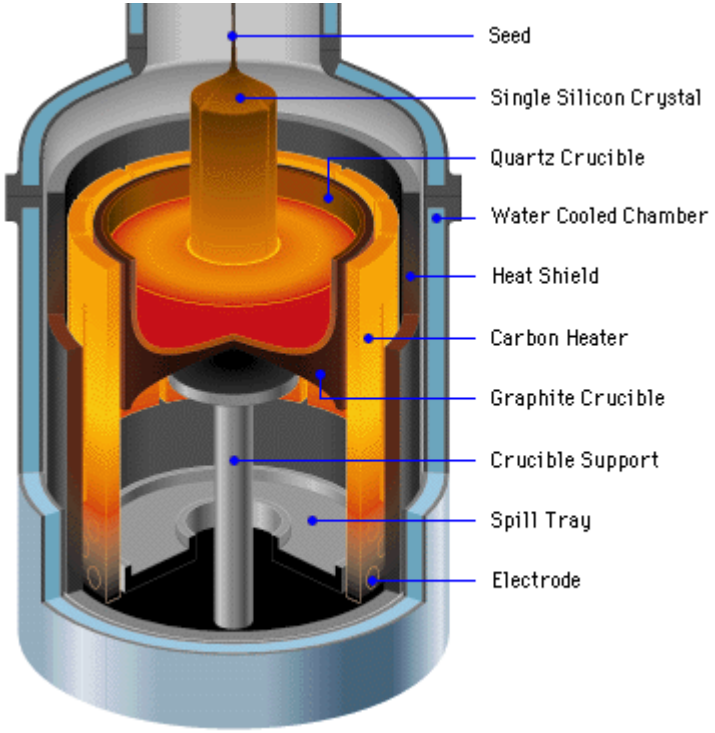
Fundamental processes: Wafer manufacture

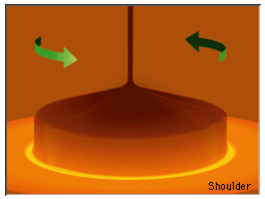
- **Wafer production requires three processes:**
  - **Silicon refinement**: Several processes are necessary in order to obtain polycrystalline chunks of silicon with the enough purity.
    - Silica in a furnace at 2000ºC with carbon source

      $SiO_2(solid)+2C(solid) \rightarrow Si(liquid)+2CO(gas)$
    - Chemical reduction processes
  - **Crystal growth**: Czochralski method
  - **Wafer formation:** 1 mm thick (thickness increases with wafer diameter)

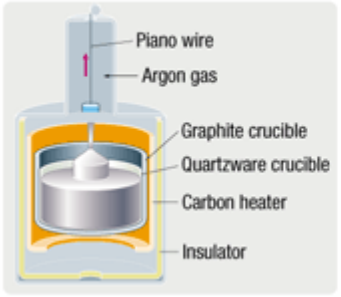
http://www.youtube.com/watch?v=aWVywhzuHnQ

Fundamental processes: Wafer manufacture





Process of monocrystalline silicon ingot creation



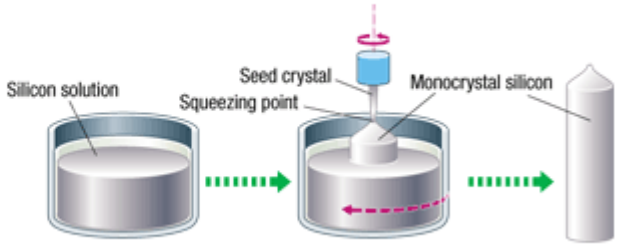
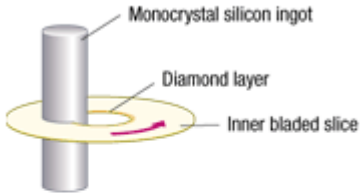
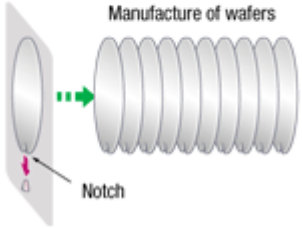


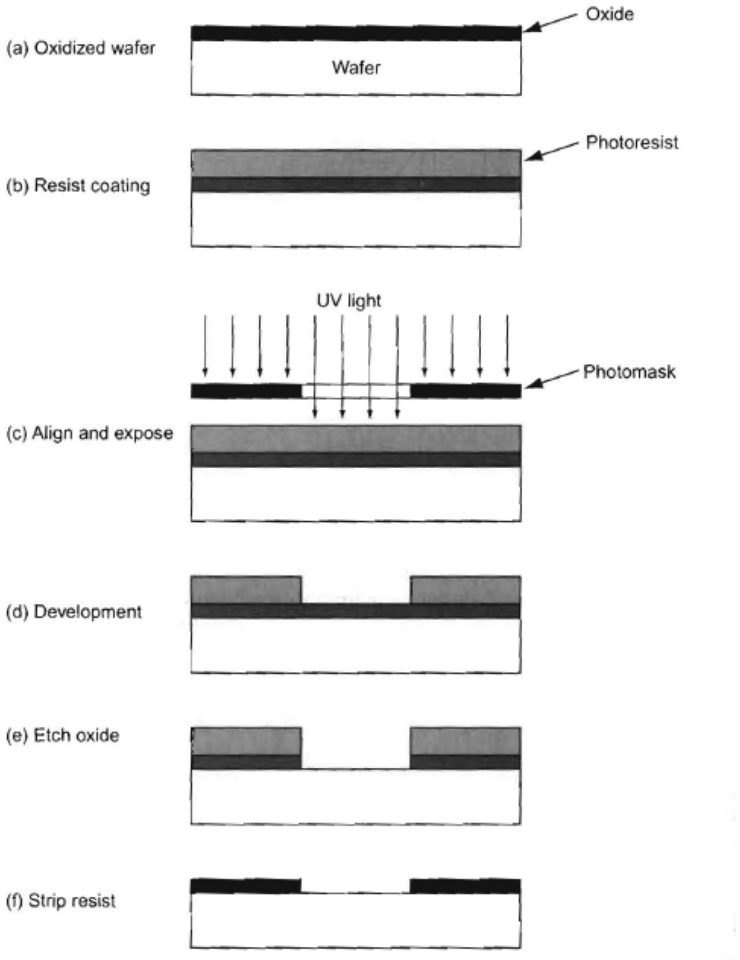
Fig. 1 Cutting of silicon wafer



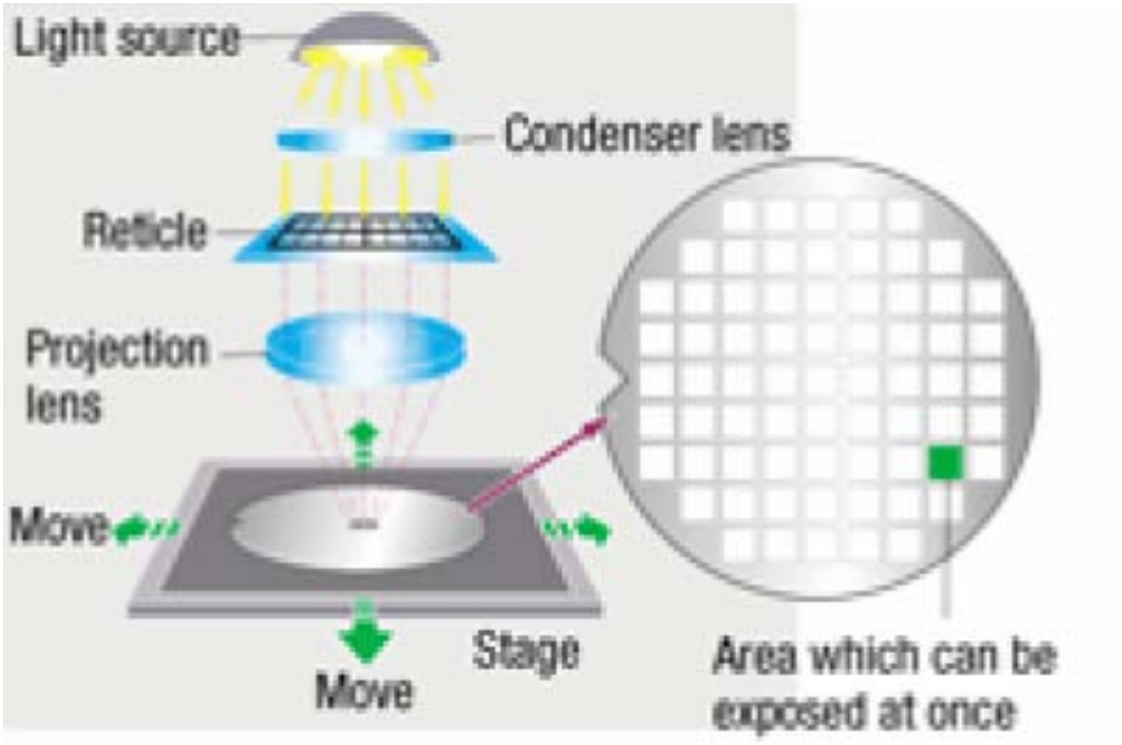


Fundamental processes: Photolithography

- Process used to select the parts in a wafer that must be affected by a given fabrication process
- A light-sensitive polymer called photoresist serve as ion implantation masks and etch masks
- Photoresist can be negative (insoluble (hardened) after exposure to UV) or positive (soluble after exposure to UV light). Positive photoresists present a higher resolution
- Resolution: diffraction of light limits the minimum printable feature size
  - Electron beam

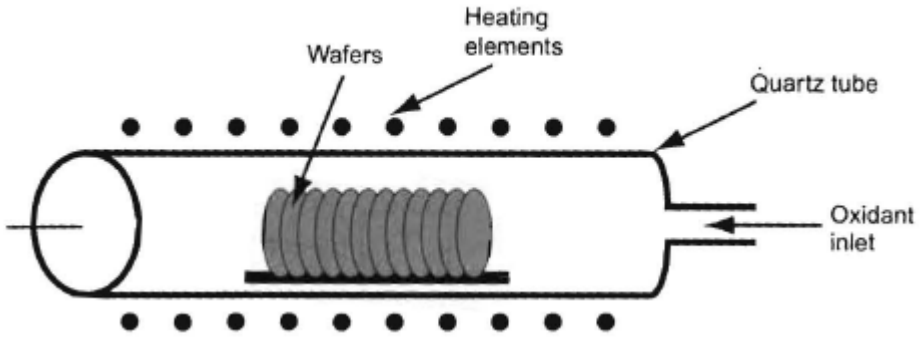


Fundamental processes: Photolithography



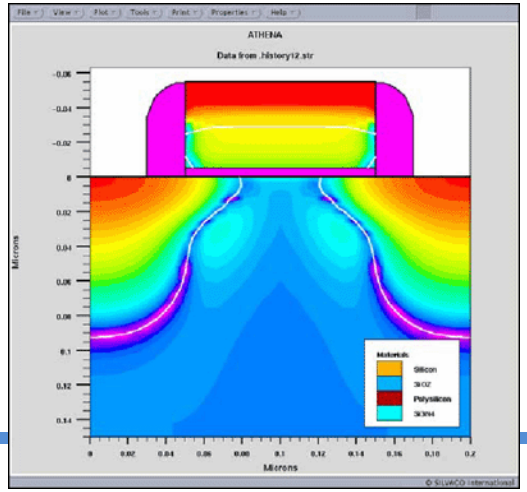
Fundamental processes: Thermal oxidation

- Silicon within an oxidant at elevated temperatures will form a thin layer of oxide (SiO_2) on all exposed surfaces.
- SiO_2 is an essential element in CMOS technology:
  - High quality dielectric such as gate oxides
  - Used for implantation, diffusion and etch masks
  - Near ideal silicon-oxide interface
- The silicon wafer is exposed at high temperatures (900-1200ºC) to a gaseous oxidant:
  - O_2: dry oxidation
  - water vapor: wet oxidation



Fundamental processes: Doping processes

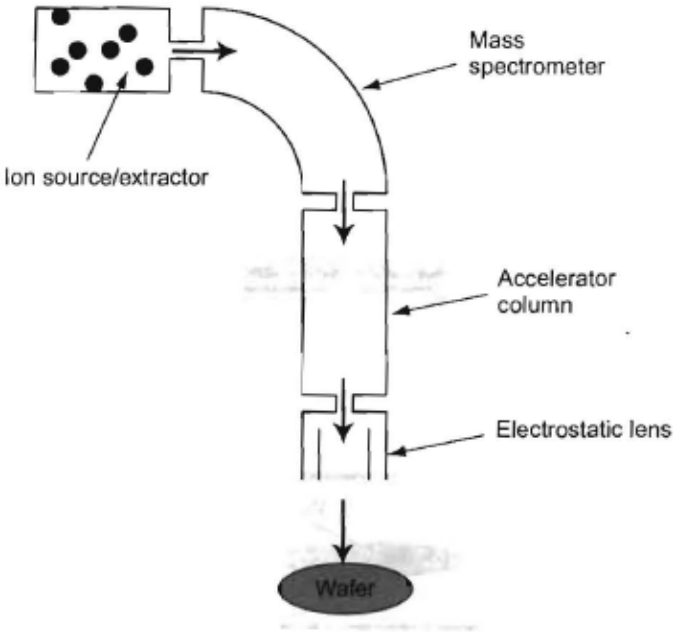
- Controlled introduction of dopant impurities into silicon
  - N-type dopants: P, As, Sb (Phosphorus, Arsenide, Antimony)
  - P-type dopant is B (Boron)
- Solid state diffusion has been the traditional doping process. Diffusion is directly proportional to the concentration gradient and thermal energy

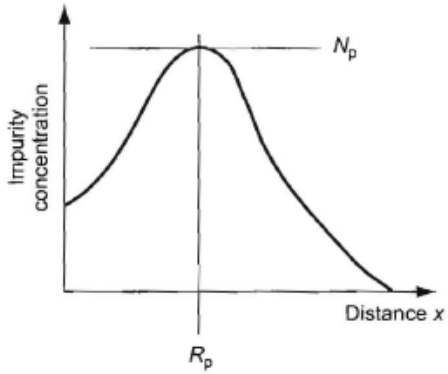


Lateral diffusion

Doping process: Ion implantation

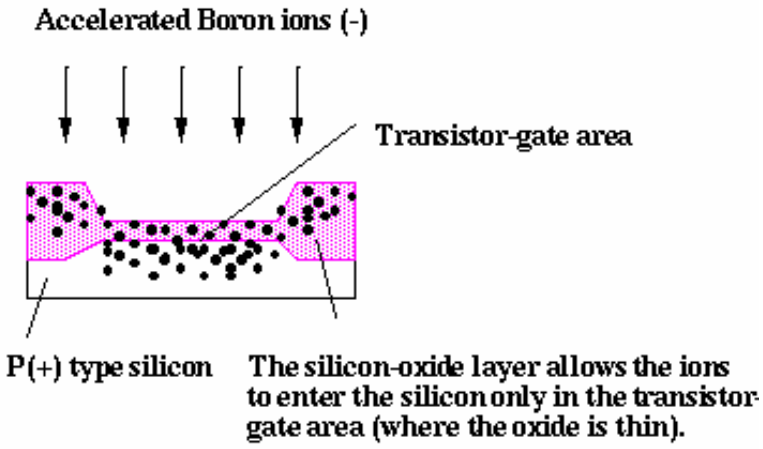
- Ion implantation is the most used method in modern CMOS fabrication
- Dopant atoms are ionized, then accelerated through a large electric potential (few kilovolts to megavolts) toward a wafer. The highly energetic ions bombard and implant into its surface.





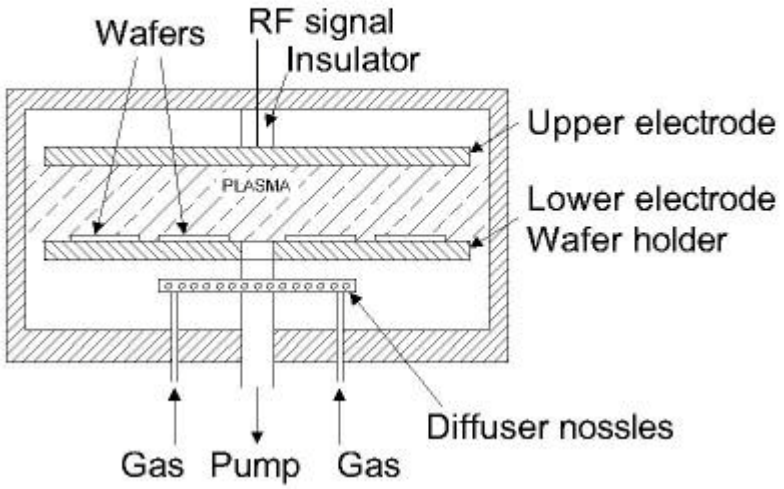
Doping process: Ion implantation

- High degree of lattice damage. It is repaired with annealing at high temperatures agitating dopant impurities into lattice sites.
- Compared with solid-state diffusion, ion implantation has the advantages of being a low-temperature and a highly controlled process.
- Nowadays, diffusion is used to redistributing dopants after the ion implantation



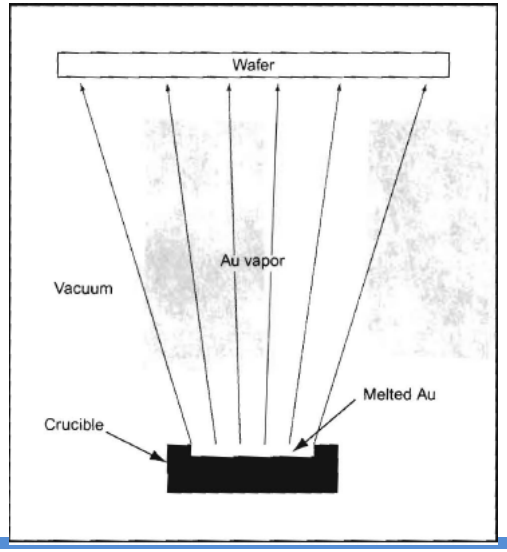
Fundamental processes: Thin-film removal

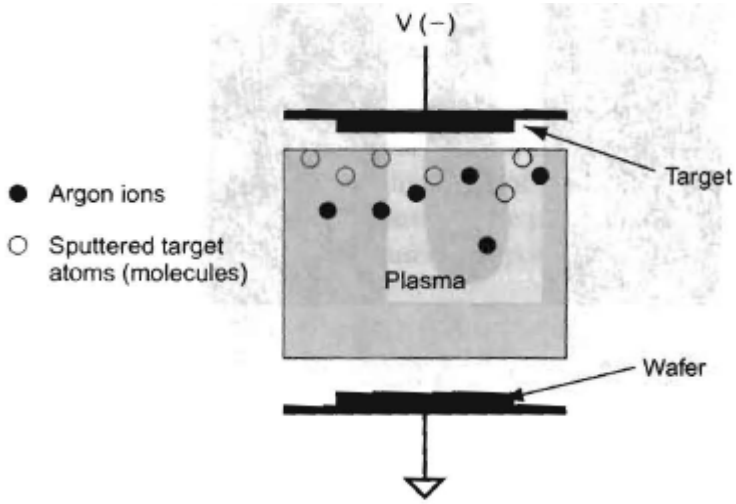
- Processes to remove thin films
  - Wet etching. A chemical solution is used to remove material. Highly selective compared with the dry-etch processes
  - Dry etching.
    - The wafer is bombarded by charged ions that cause material to be ejected off the surface



Fundamental processes: Thin-film deposition

- Methods of depositing thin films of insulators, conductors and semiconductors on the wafer
  - Film thickness uniformity <±5nm
- Physical vapor deposition (PVD). Atoms or molecules pass through a low-pressure gas phase and then condense on the surface of the substrate:
  - Evaporation
  - Sputter deposition (similar to dry etching)





Fundamental processes: Thin-film deposition

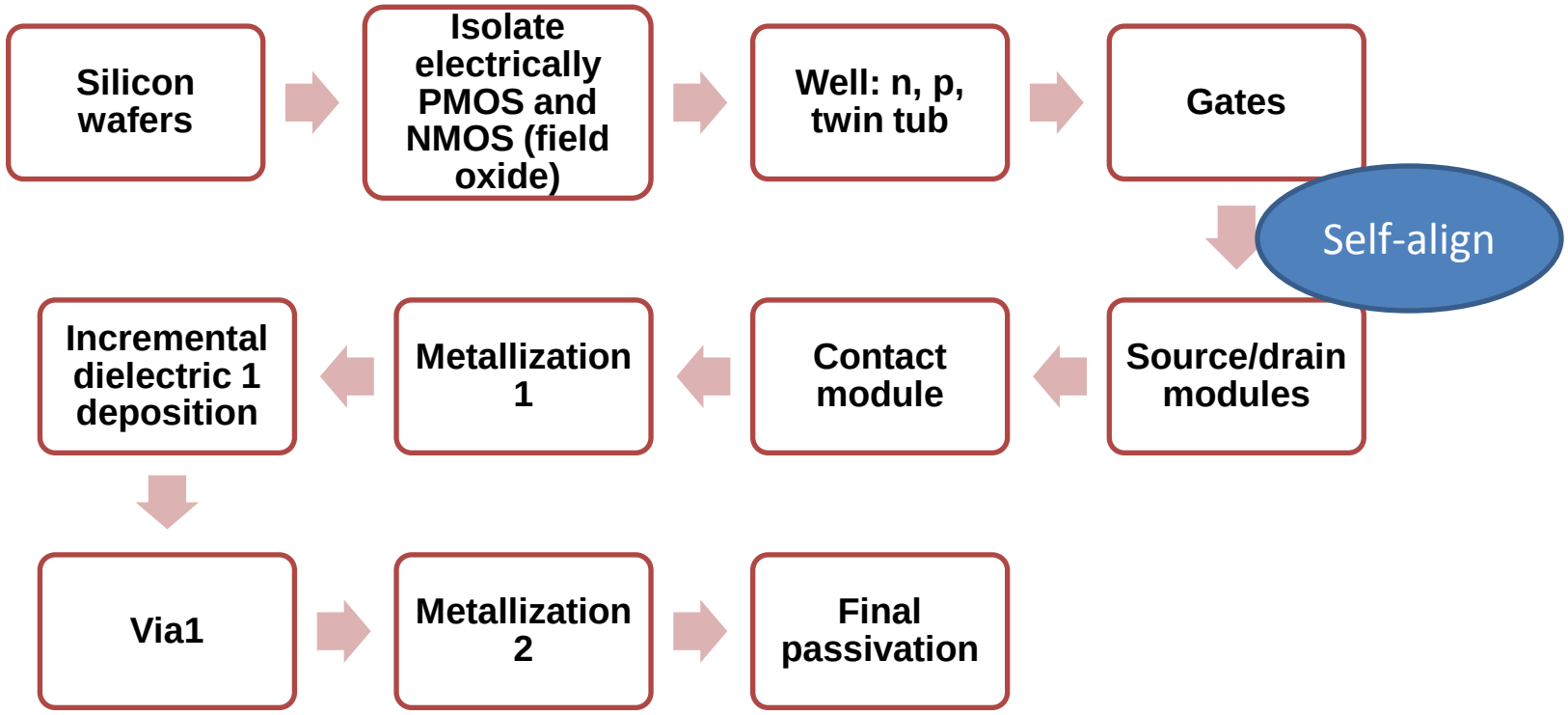
- Chemical vapor deposition (CVD). Reactant gases are introduced into a chamber where chemical reactions between the gases at the surface of the substrate produce the desired film.
- At atmospheric pressure at relatively low temperatures CVD can be applied in a reactor similar to an oxidation tube furnace
- At low pressure the process can yield better films but at the expense of a higher deposition temperature.

Polisilicon→ Thin-film deposition of silicon on SiO_2

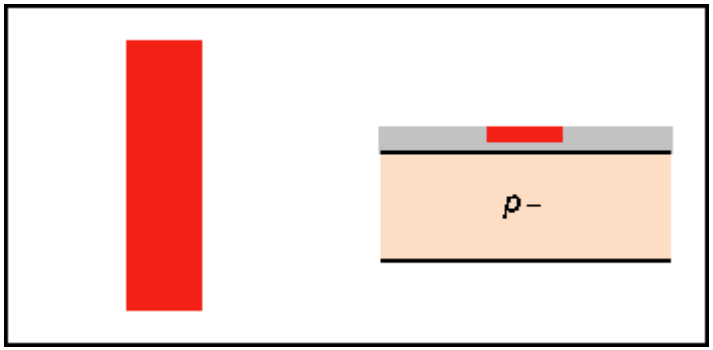
Metallization→ AlCu/Ti

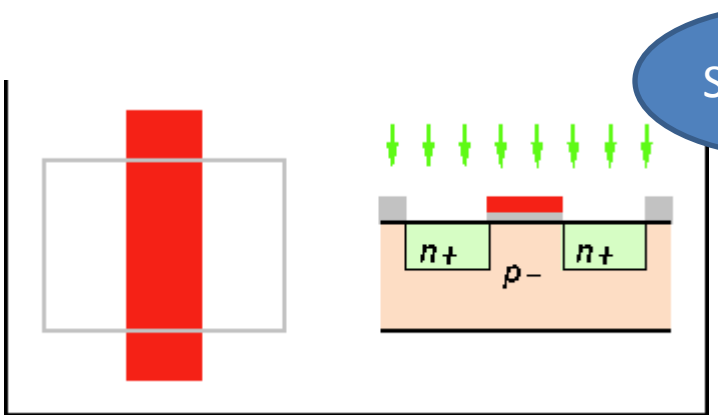
CMOS process sequence

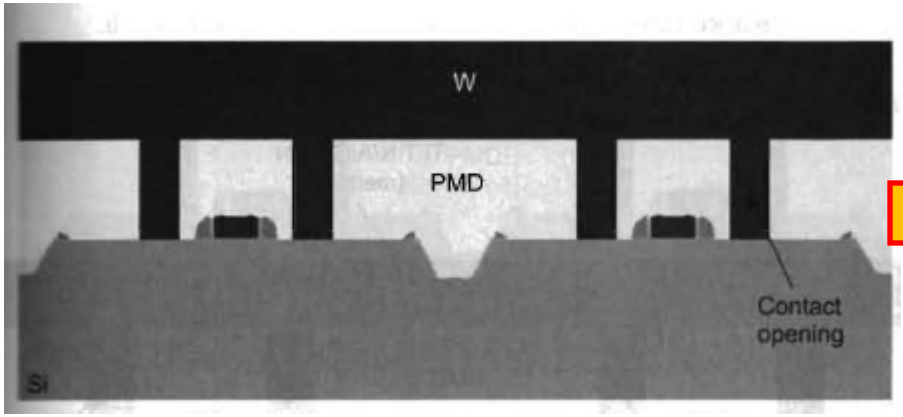
- Several hundred steps are required to manufacture ICs on a silicon wafer.

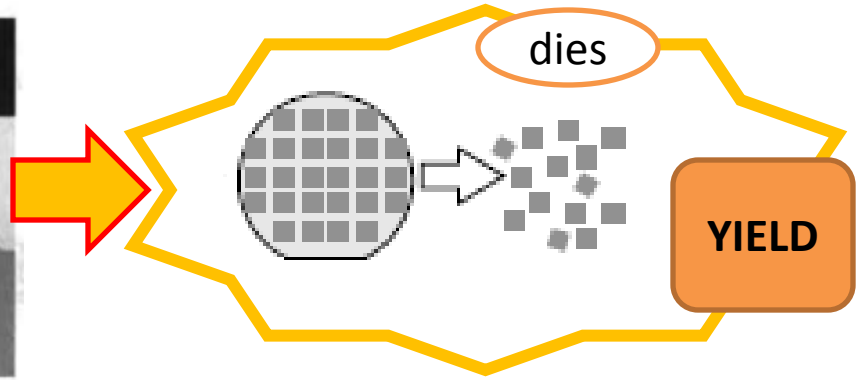


CMOS process sequence









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- Wikipedia

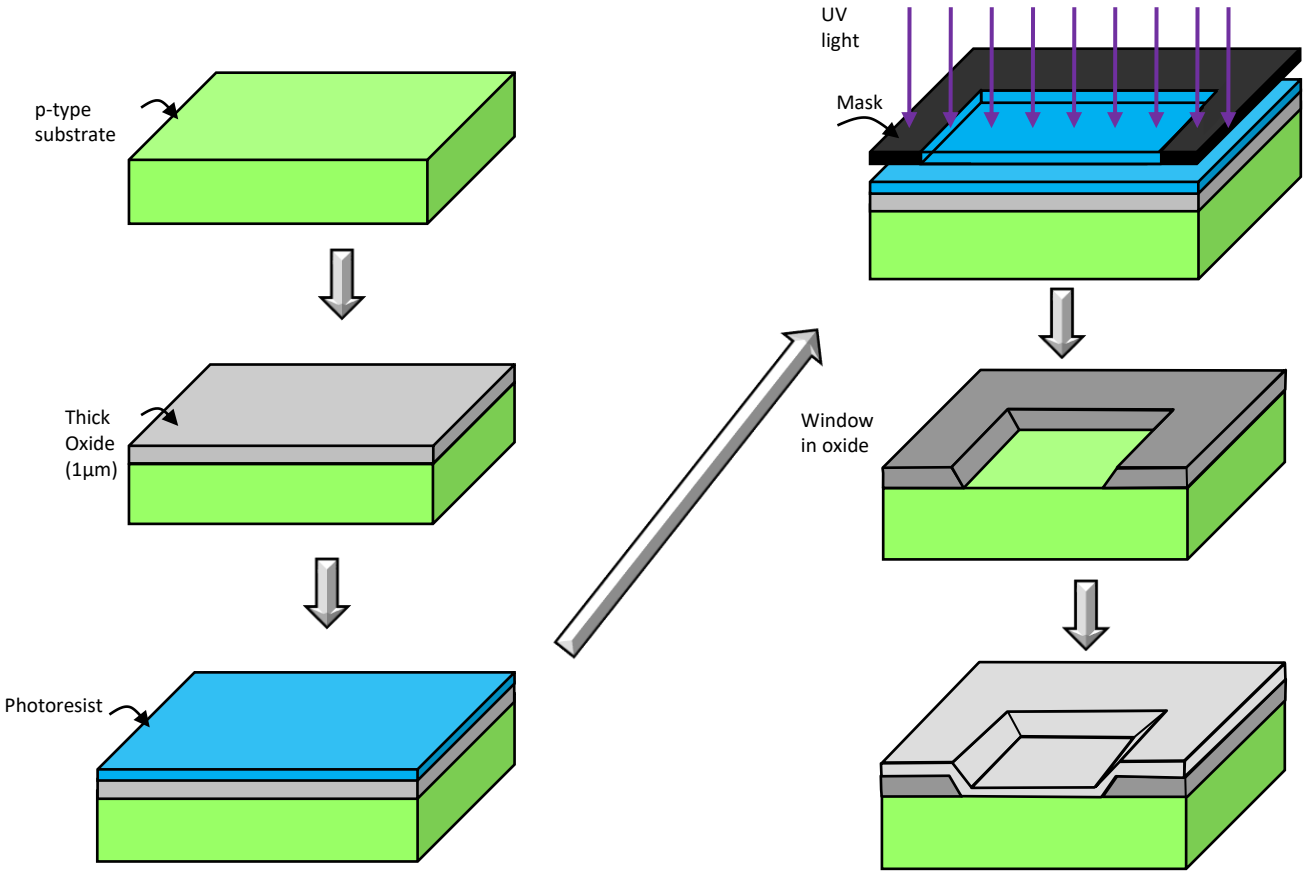
MANUFACTURING AND PACKAGING OF INTEGRATED CIRCUITS

Authors
Celia López Ongil
Mario García Valderas
Marta Portela García
Almudena Lindoso
Luis Entrena
Enrique San Millán

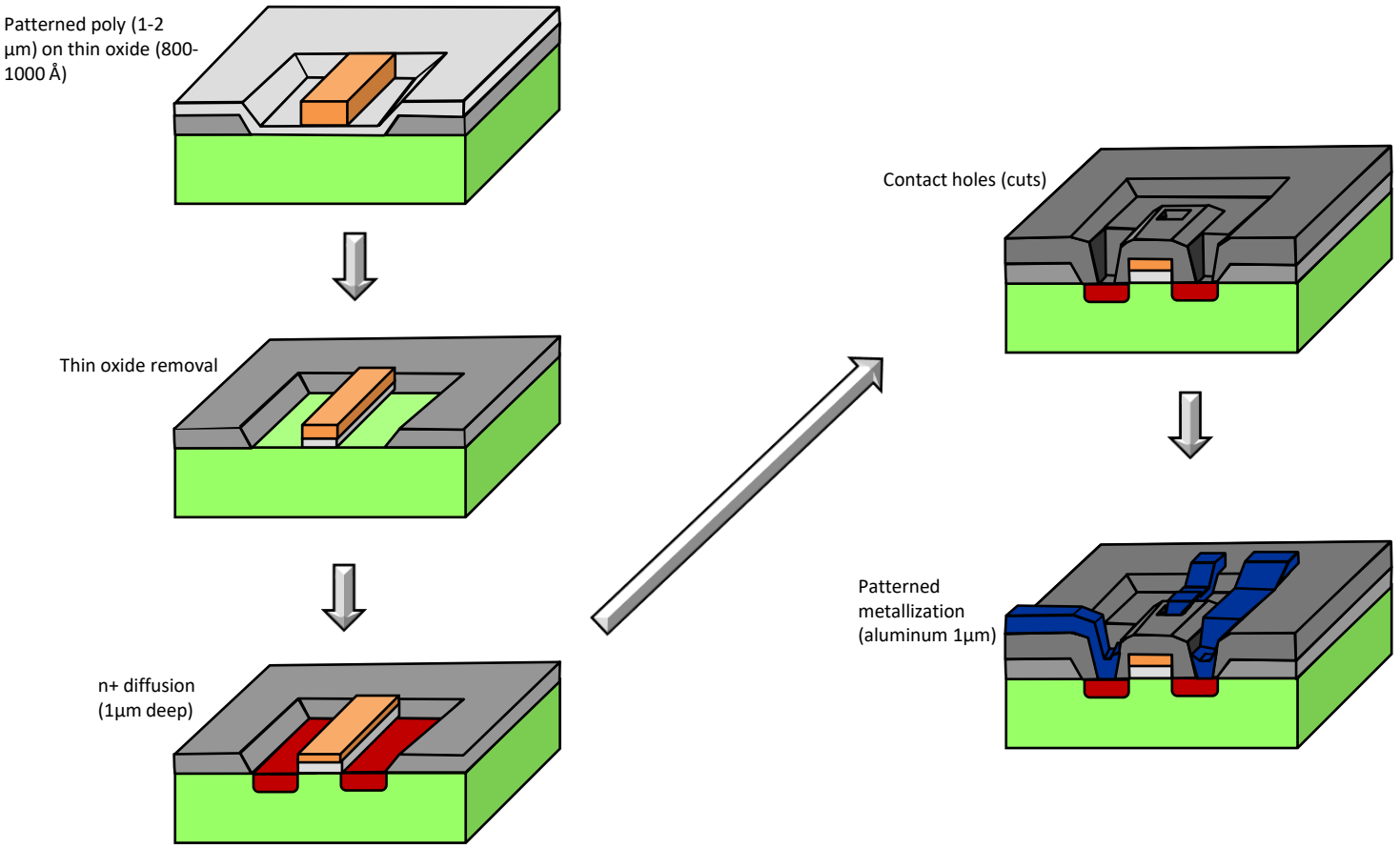
Outline

- The manufacturing process of a CMOS circuit
  - Making an NMOS Transistor
  - Manufacturing an inverter
    - Single well
    - Double well (Twin-tub)
- ICs packaging
- Application Specific ICs: types and characteristics

NMOS transistor manufacturing (1/2)

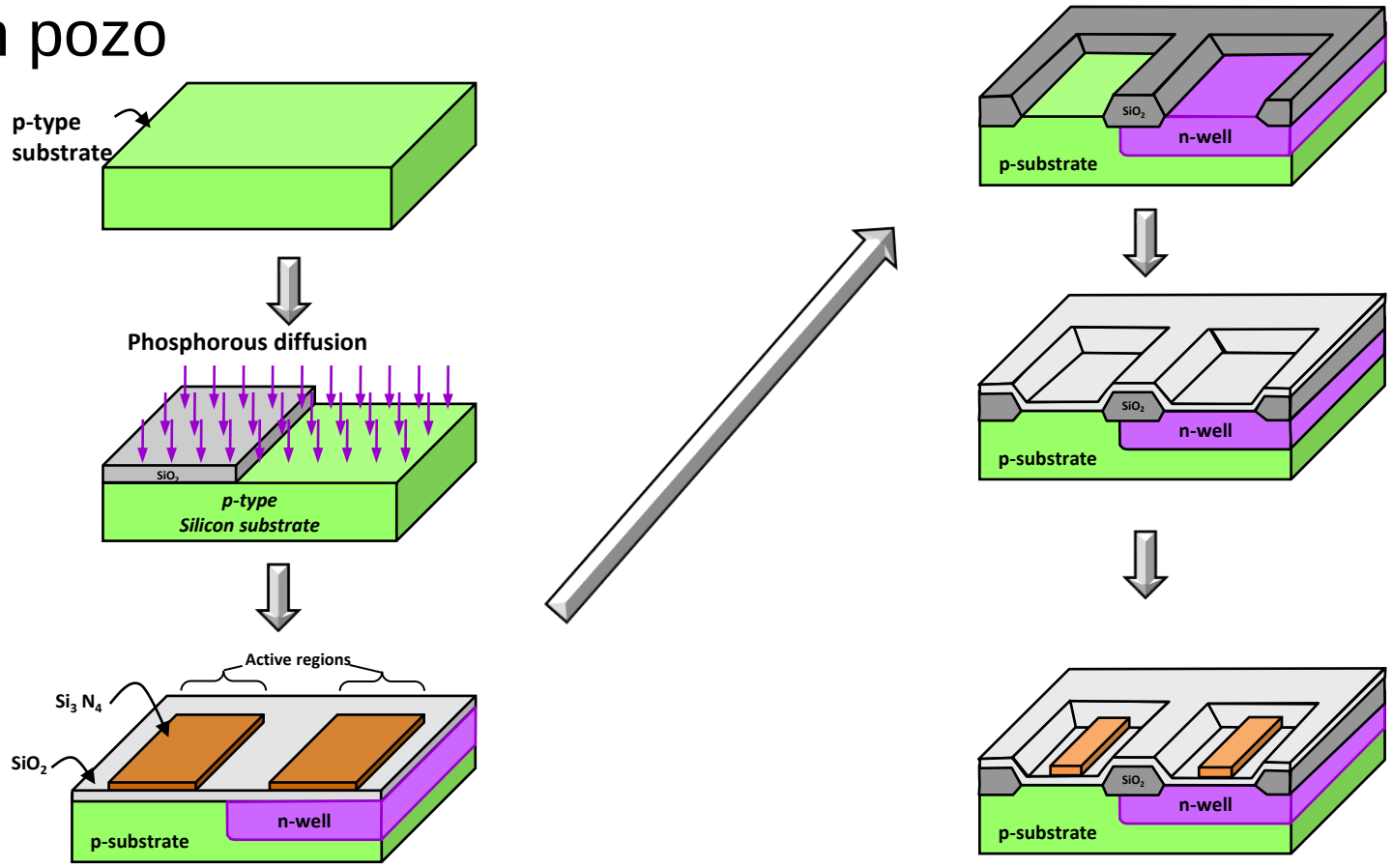


NMOS transistor manufacturing(2/2)



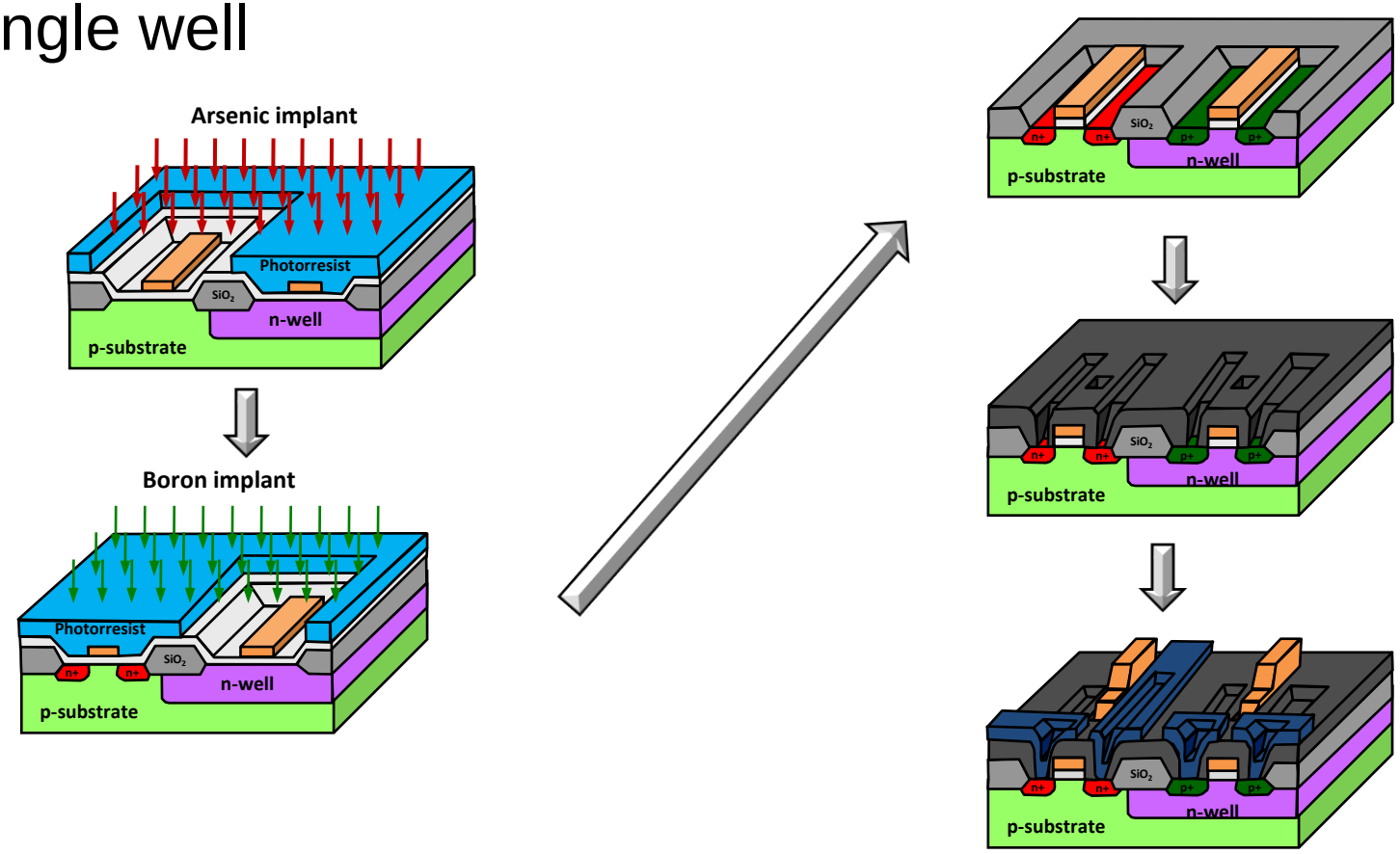
CMOS inverter manufacturing(1/3)

- Un pozo



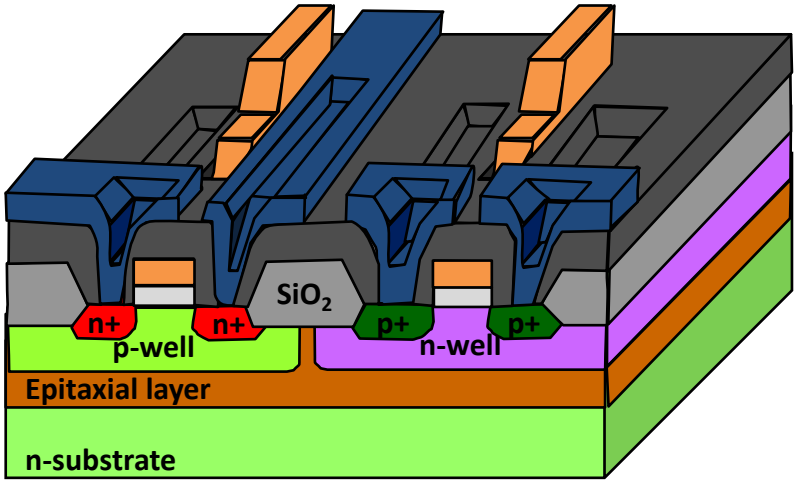
CMOS inverter manufacturing(2/3)

- Single well



CMOS inverter manufacturing(3/3)

- Double well (twin-tub)



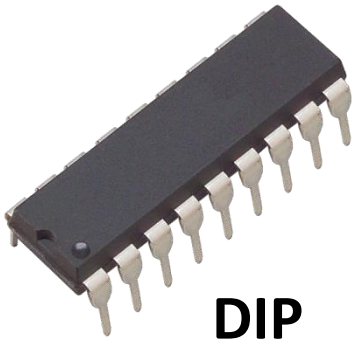
Packaging

- Functions:
  - Isolation. Isolate the circuit from external agents, such as dust or moisture.
  - Connectivity. The terminals allow you to connect the inputs and outputs of the chip to the tracks of a board.
  - Dissipation. In their normal operation, circuits produce heat, which must be dissipated. That heat must pass through the encapsulation. It may be necessary to add a heatsink, attached to the surface of the package, in case the package does not dissipate sufficiently.
  - Manipulation. Since an integrated circuit is very fragile, the package makes it easy to handle, place and assembleje.

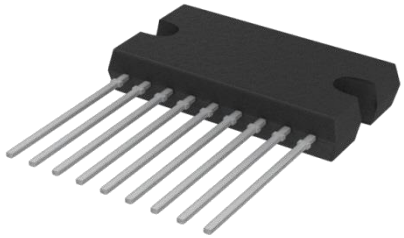
Packaging : Types

Tipo	Nº pines	Montaje
DIP (Dual In-Line Package) SIP (Single In-Line Package) ZIP (Zig-Zag In-Line Package)	5-64	Insertion
SOIC (Small Outline Integrated Circuit) TSOP (Thin Small Outline Package) SSOP (Shrink Small Outline Package) TSSOP (Thin Shrink Small Outline Package) QSOP (Quarter-size Small Outline Package) VSOP (Very Small Outline Package)	8-32	Surface mount
LCC (Leaded Chip Carrier) PLCC (Plastic Leaded Chip Carrier) CLCC (Ceramic Leaded Chip Carrier)	16-200	Surface mount Insertion through socket
FP (Flat Pack) QFP (Quad Flat Pack) PQFP (Plasic Quad Flat Pack) CQFP (Ceramic Quad Flat Pack) TQFP (Thin Quad Flat Pack) LQFP (Low profile Quad Flat Pack)	10-300	Surface mount
PGA (Pin Grid Array) PPGA (Plastic Pin Grid Array) CPGA (Ceramic Pin Grid Array)	68-500	Insertion
BGA (Ball Grid Array)	>500	Surface mount

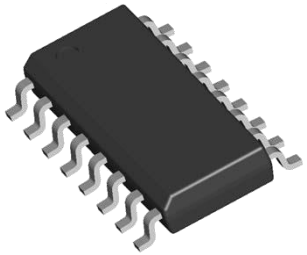
Packaging : Types



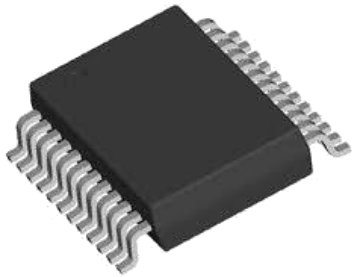
DIP



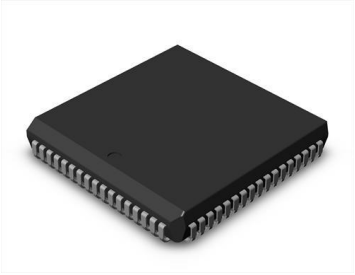
SIP



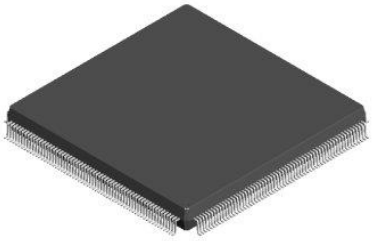
SOIC



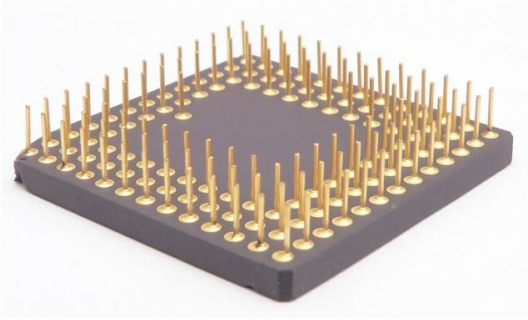
SSOP



PLCC



QFP



PGA

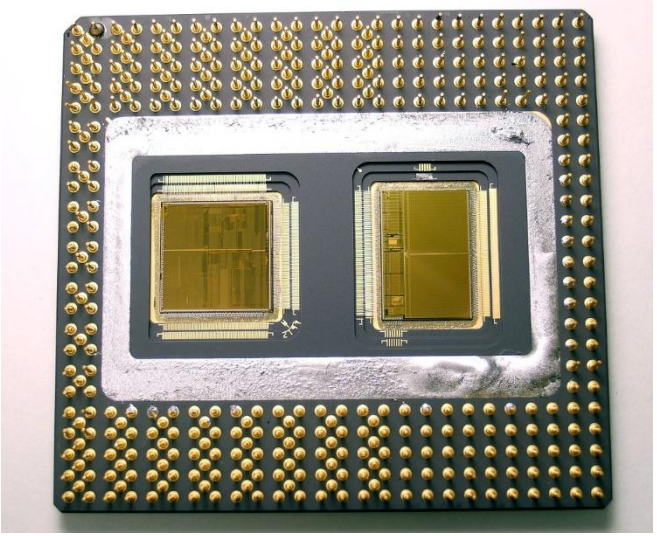
BGA

Packaging : Multi-chip modules

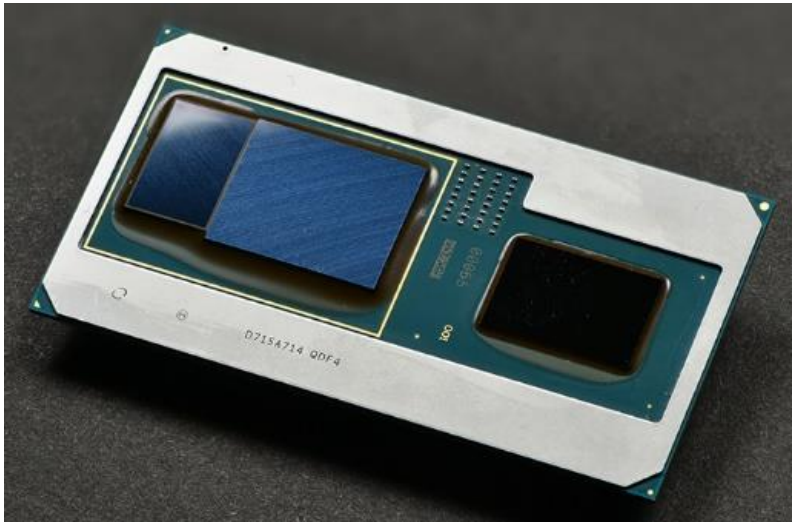
- Multi-Chip Modules (MCM)
- It is an encapsulation that includes several circuits mounted on the same base and connected to each other, so that they can be used as if they were a single chip.
- There are different types with different degrees of integration
- Examples: Pentium Pro, Xenos (Xbox GPU)

Type	Line density (cm/cm^2)	Line width (µm)	Separation (µm)	Description
MCM-L	30	750	2250	Laminated multi-chip module. The substrate is a multilayer printed circuit board (PCB). Low integration.
MCM-C	20-40	125	125-375	Multi-chip ceramic substrate module. Medium integration.
MCM-D	200-400	10	10-30	Multi-chip module deposited on silicon substrate. High integration.

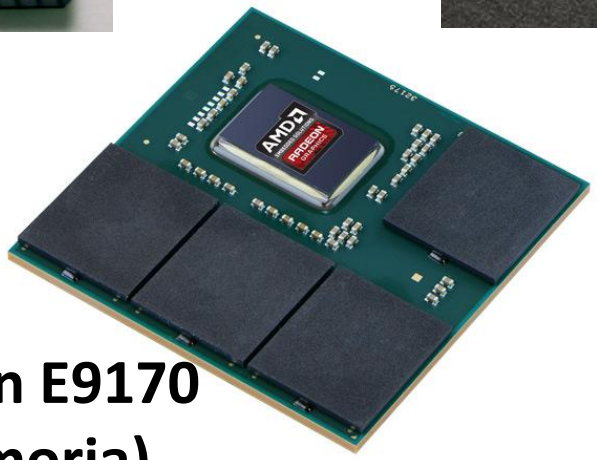
Packaging : Multi-chip modules



Pentium-Pro (CPU+cache)



Core i7-8809G (CPU+GPU)



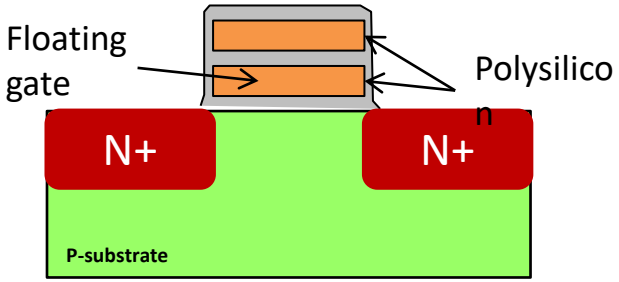
AMD Radeon E9170 (GPU+memoria)

Application Specific CIs

- ASICs (Application Specific Integrated Circuit): digital, analog or mixed circuits.
- Deployment Types
  - Full-custom
  - Partially custom
    - Partially prefabricated: gate array
    - Partially pre-designed: standard cells and macrocells, IP blocks (Intelectual Property)
  - Fully prefabricated circuits: programmable circuits
    - CPLDs (Complex Programmable Logic Devices)
    - sRAM FPGAs (Field-Programmable Gate Arrays)
    - Antifuse FPGAs

Application Specific CIs

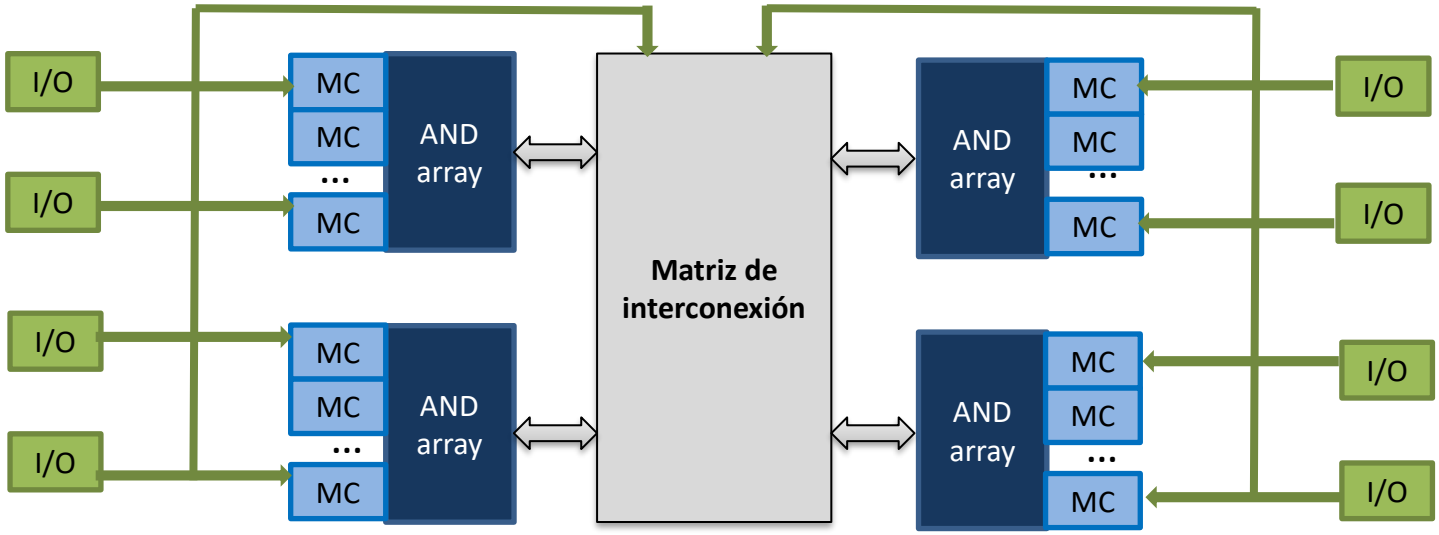
- Programmable circuits: CPLDs
  - Programming Technology: Floating Gate MOS Transistor



    - When the transistor is not programmed, it acts in conventional mode.
    - Programmable threshold voltage.
      - By applying a sufficiently large voltage to the gate it is possible to provide the carriers with enough energy to pass through the oxide and be trapped in the floating gate. When the voltage is eliminated the cell is charged (programmed)
  - Non-volatile devices
  - Reprogramables
  - High power consumption

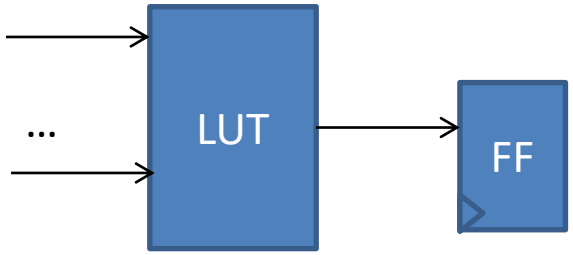
Application Specific CIs

- Programmable circuits: CPLDs
  - Basic structure
    - Programmable interconnections
    - Logical blocks: product terms and bistable macrocells, inverters and multiplexers.
    - I/O Cells



Application Specific CIs

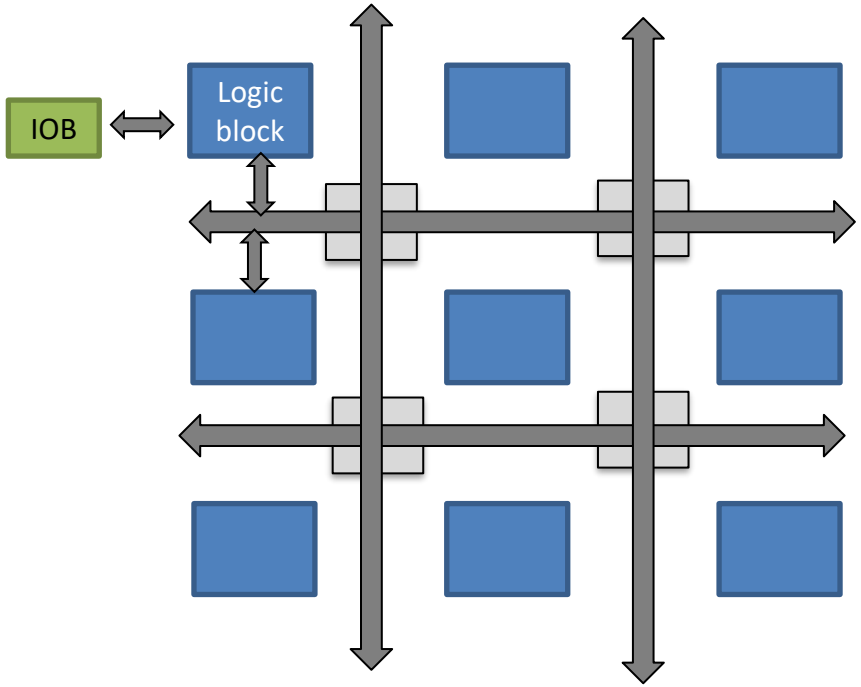
- Programmable circuits: sRAM FPGAs
  - Programming technology: SRAM memory cells for circuit configuration storage
  - Basic cell
    - Flip-flop
    - Look-up Table, LUT



  - Volatile devices
  - Reprogrammables
  - Greater integration capacity → Greater complexity
  - Possibility of dynamic reconfiguration

Application Specific CIs

- Programmable circuits: sRAM FPGAs
  - Structure consists of a matrix distribution of logical cells communicated with each other and with the input and output blocks (IOBs) through programmable routing channels



Application Specific CIs

- Programmable circuits: antifuse FPGAs
  - Programming technology: Antifuses. The necessary connections are short-circuited during programming. The programming is done by subjecting the antifuse (two electrodes separated by a thin layer of insulator) to a high voltage that breaks the dielectric creating a permanent short circuit
  - They are non-volatile
  - Non-reprogrammable
  - Fast → high-speed applications
  - Electrical stability → high reliability and robustness
  - Specific programmers are needed to supply voltage pulses of adequate duration and value
  - Structure: Only interconnections are programmed, so that basic cells perform a fixed logical function.

ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS AT PHYSICAL LEVEL

Authors:
Almudena Lindoso
Marta Portela
Enrique San Millán
Mario García
Luis Entrena
Celia López

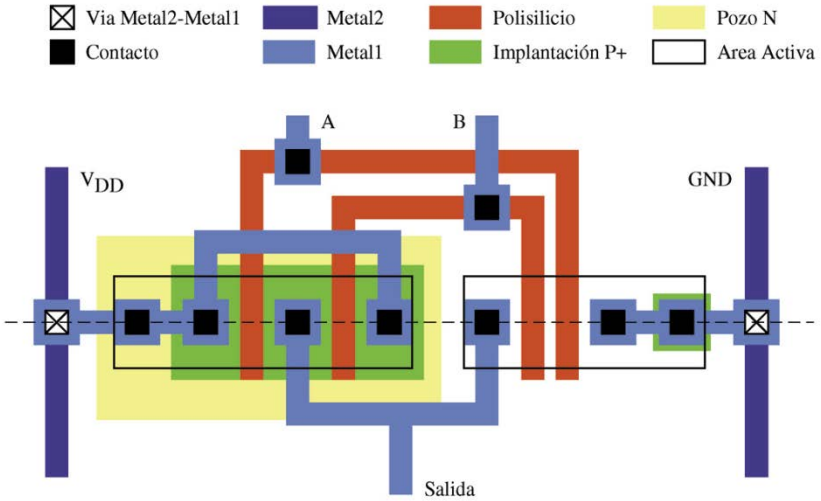
Outline

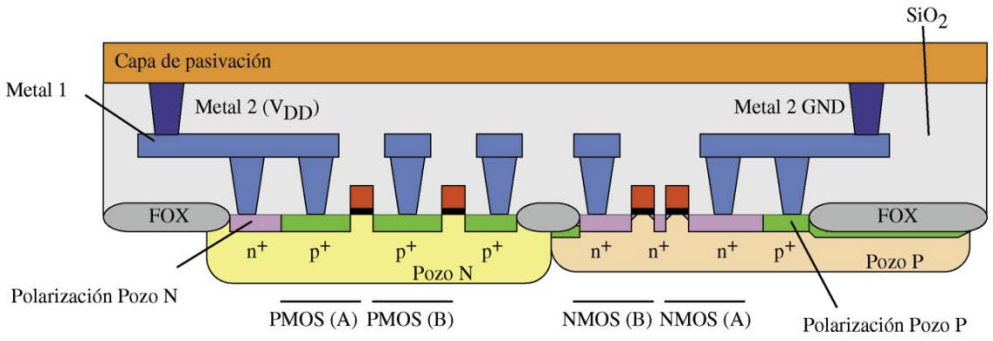
- Required masks for CMOS integrated circuits manufacturing.
  - Layout for a NAND gate
  - Layout for an inverter
- Design rules
- Examples

Required masks for CMOS integrated circuits manufacturing

- Masks are used in order to select the areas in silicon where the different fabrication steps must be applied.
- The graphical representation of required masks that define a circuit to be fabricated is named *layout*.
- A layout consists of a set of rectangles that represent the different layer masks:
  - Substrates and wells
  - Diffusion areas
  - Polysilicon
  - Metal interconnections
  - Contacts and via

Required masks for CMOS integrated circuits manufacturing

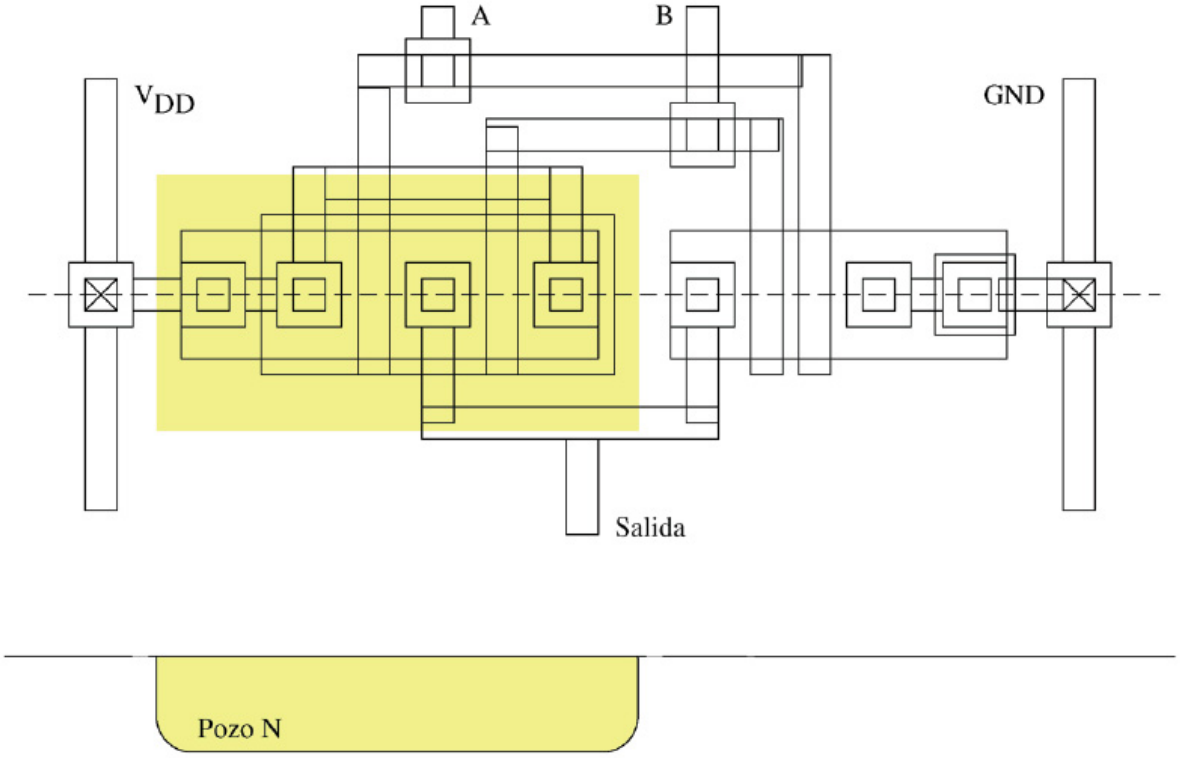




A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing

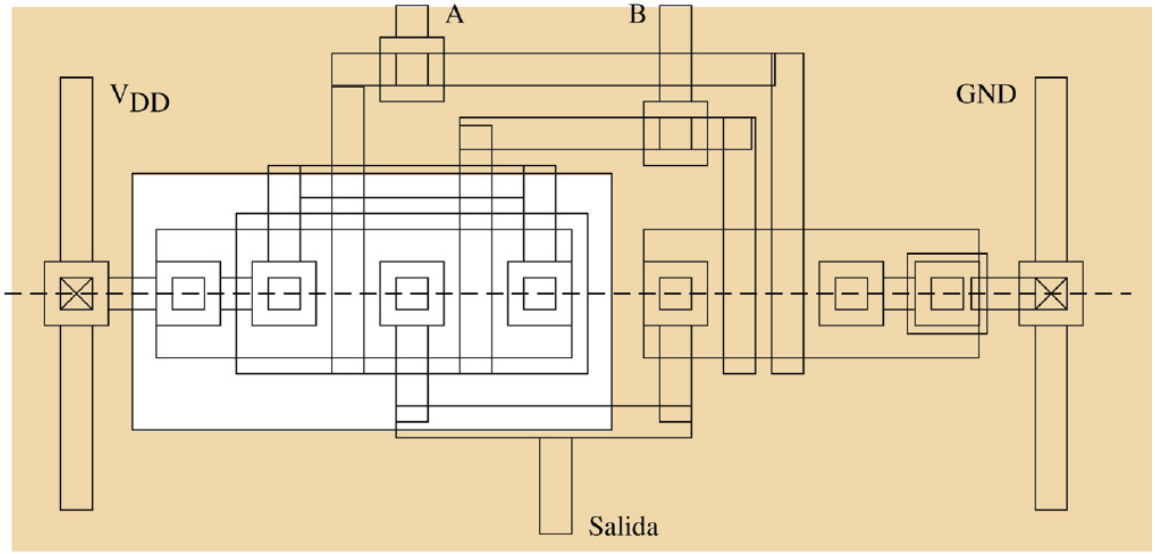
- N-well implantation

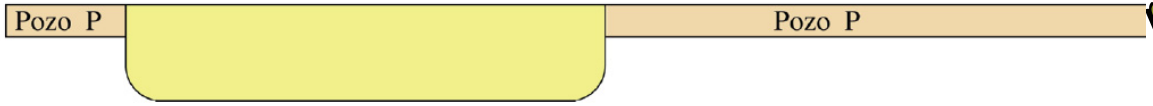


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- P-well implantation

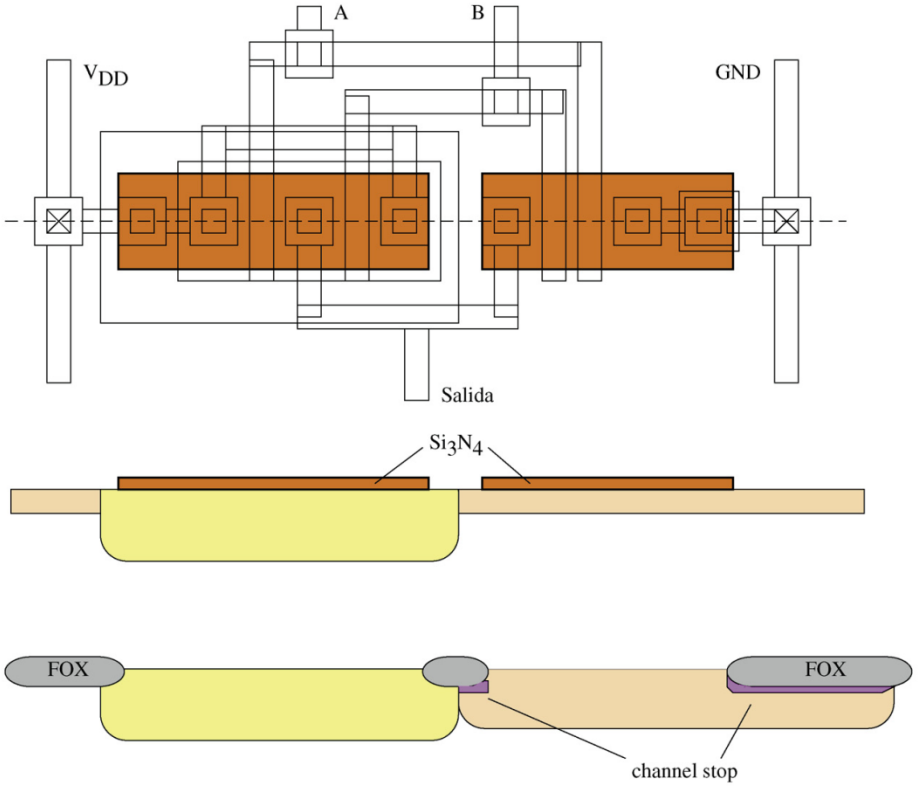




A. Rubio et al., “Diseño de circuitos y sistemas integrados” Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

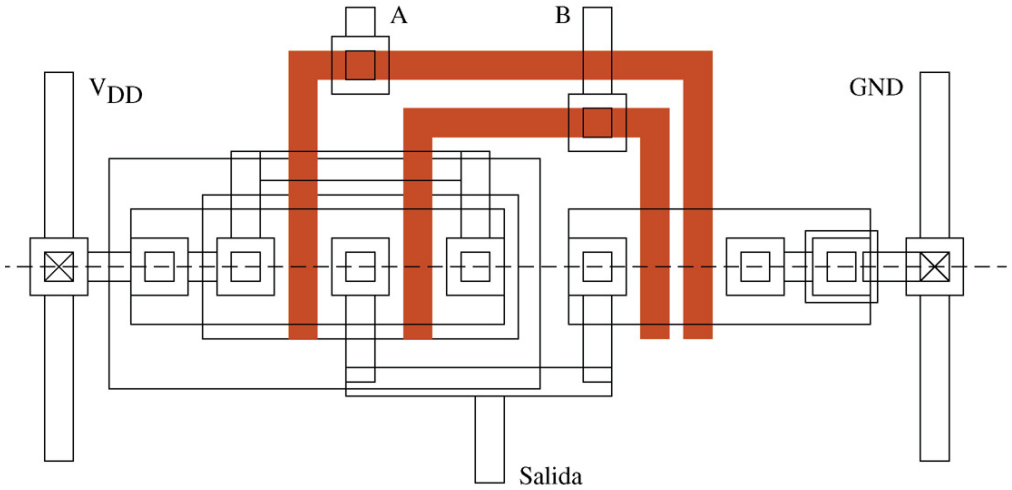
- Active areas mask and thick oxide aimed at isolating transistors

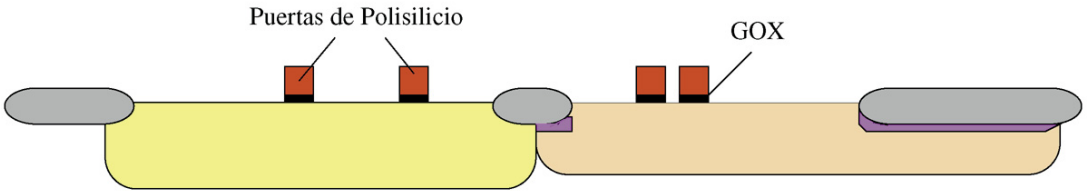


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- Polysilicon for transistor gates

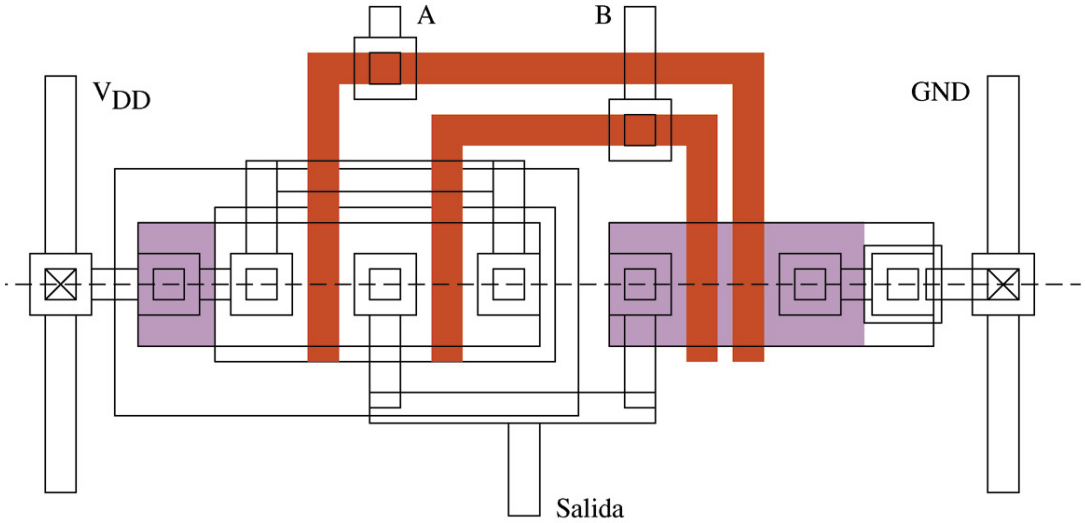


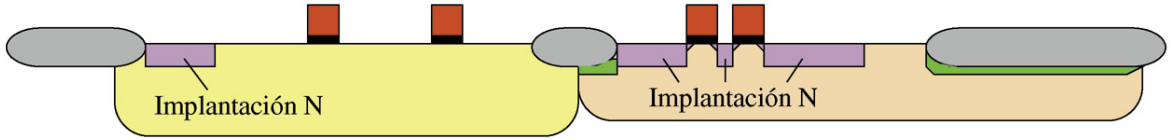


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- N+ dopants implatation

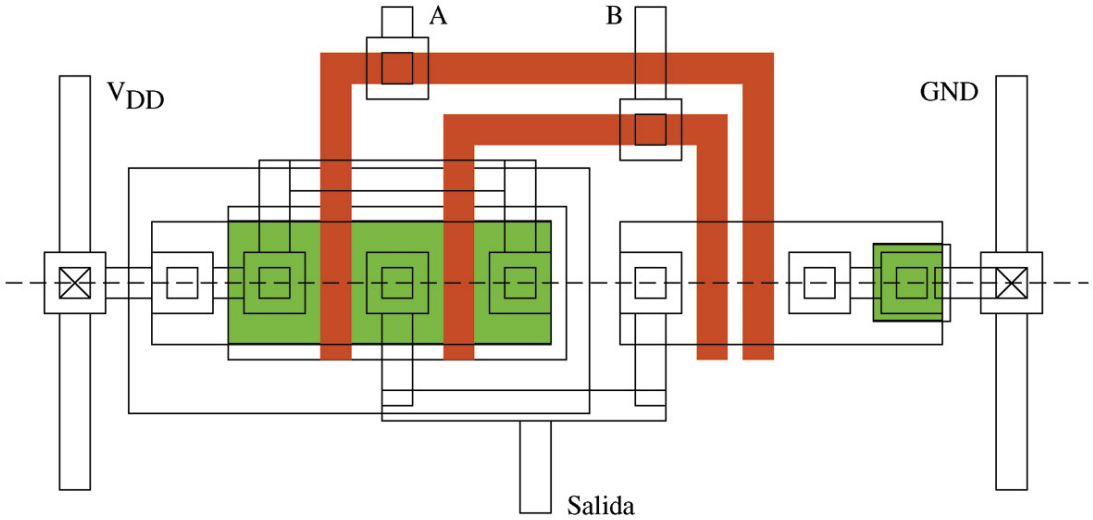


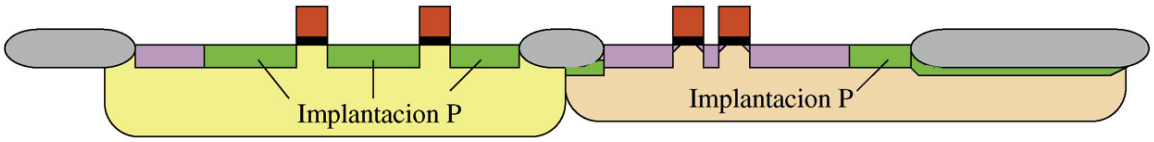


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- P+ dopants implantation

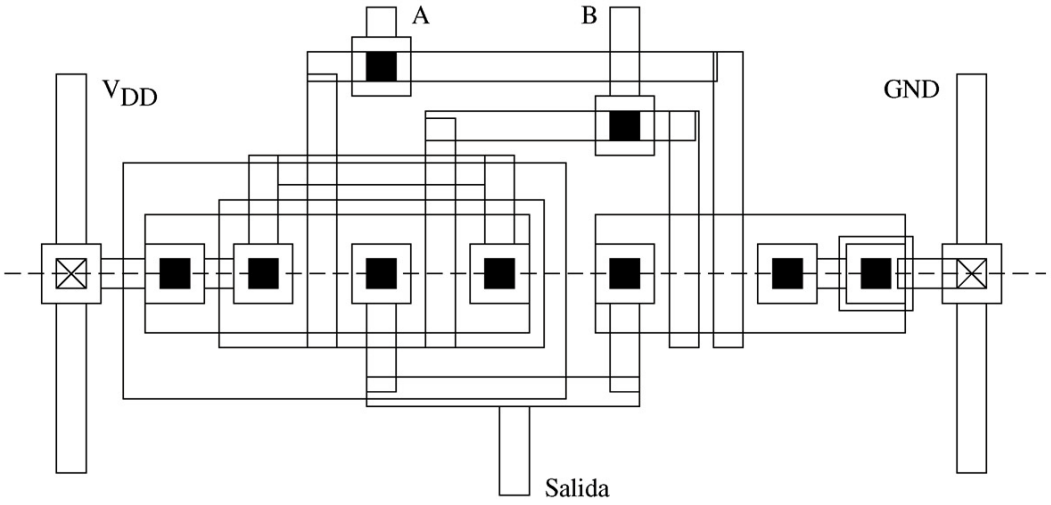




A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

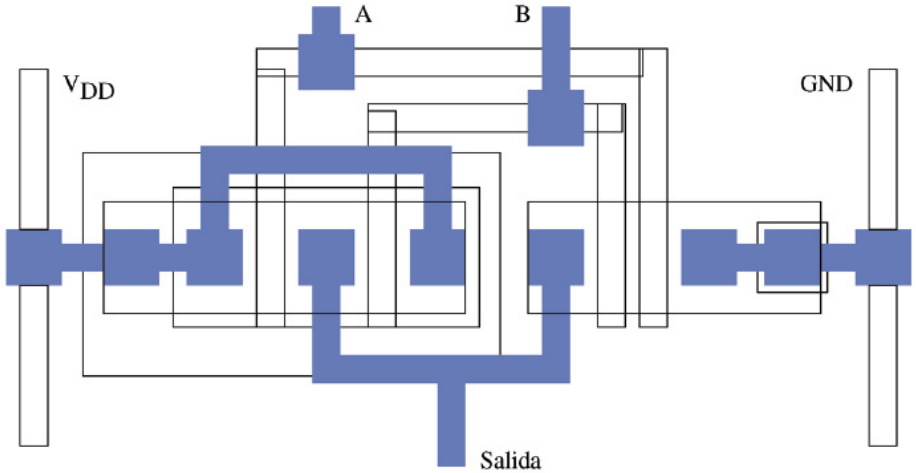
- Adding insulator just keeping free the necessary areas to implement connections



A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

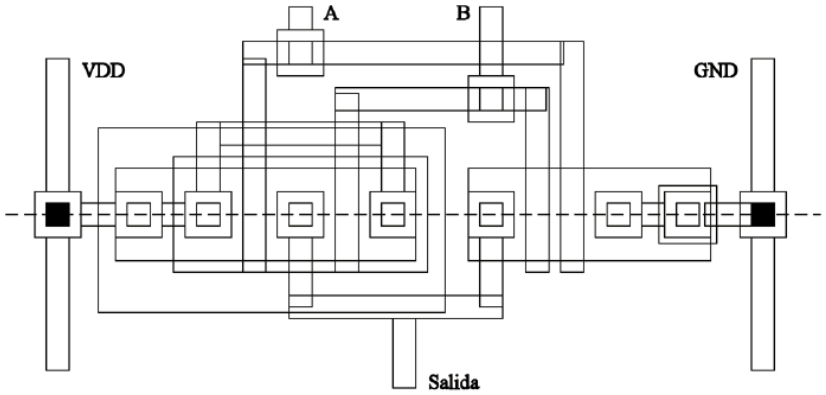
- Metalization: first layer

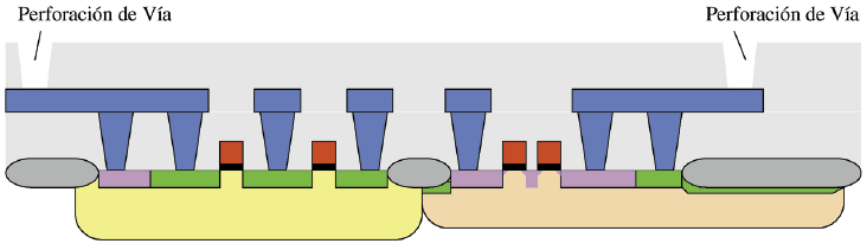


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- Adding insulator just keeping free the necessary areas to implement connections between two metal layers (via)

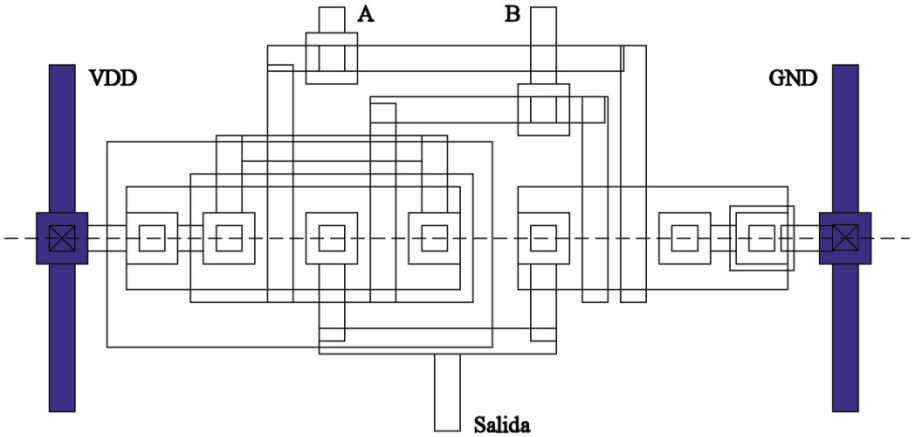


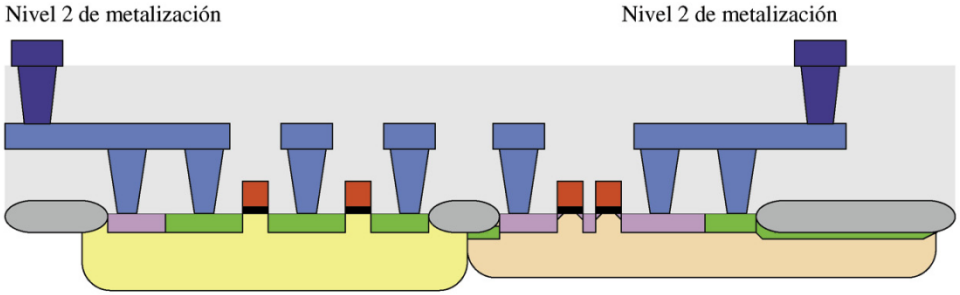


A. Rubio et al., “Diseño de circuitos y sistemas integrados” Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- Metalization: second layer

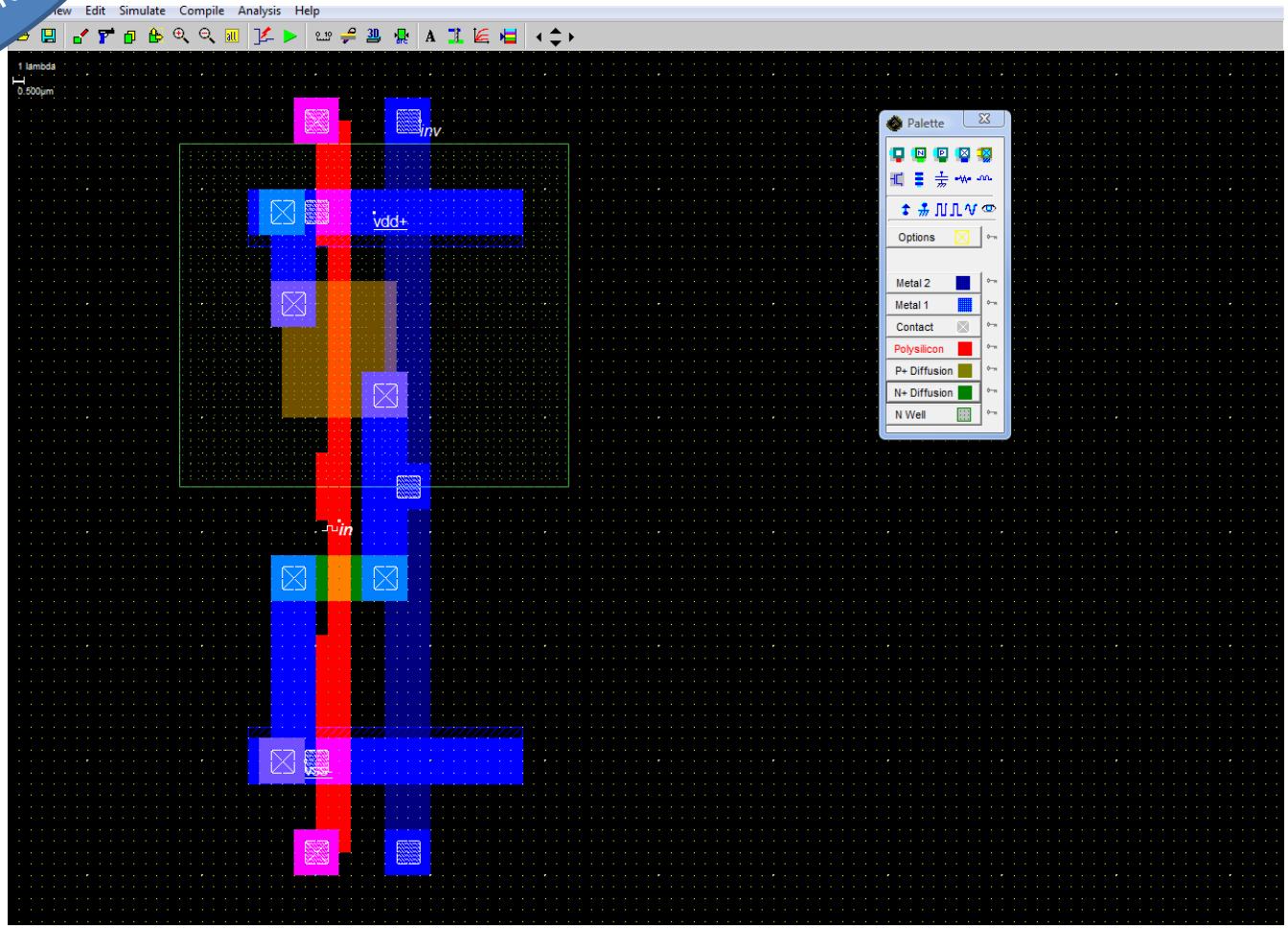




A. Rubio et al., “Diseño de circuitos y sistemas integrados” Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : inverter gate

Microwind



Design rules

- They are the necessary set of rules that allows the designer to specify the design for its implementation on the silicon wafer.

- A complete set of design rules consists of the following elements:
  - Set of layers
  - Relations between the rectangles in the same layer
  - Relations between the rectangles in different layers

- They fix geometric restrictions

Design rules

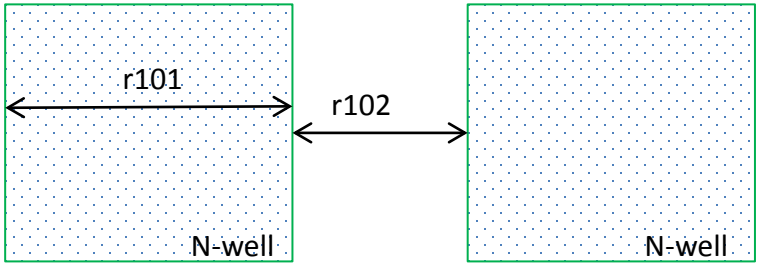
- There are two types:
  - Scalable.- They are represented in base to a parameter (λ)
    - Adimensional rules.
    - 2λ is the minimum size. It depends on the minimum dimension that is possible to etch in the silicion by means of the litographic process.
    - During this course, scalable design rules are used. (Microwind CAD tool)
    - In case of technologies beyond 0.18µm (lower dimensions), the scalability is not linear.
    - These design rules imply the worst case => over-dimensioned circuits
  - Non scalable
    - They are used by the industry

Design rules

Microwind

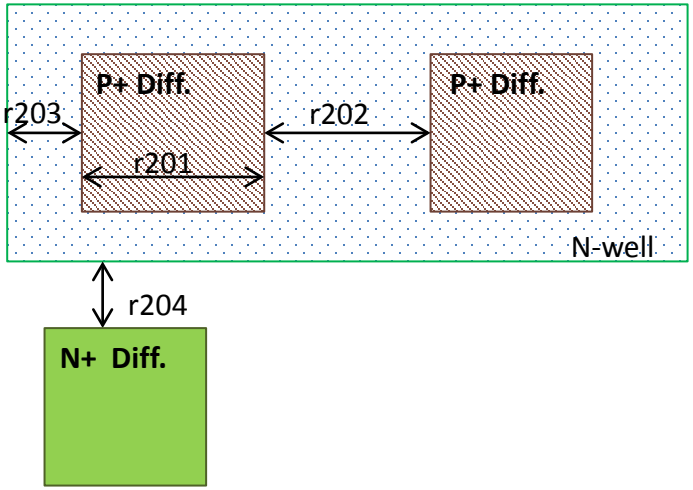
- file.rul

N-well



r101 → Minimum well size
r102 → Minimum distance between wells

Diffusion areas



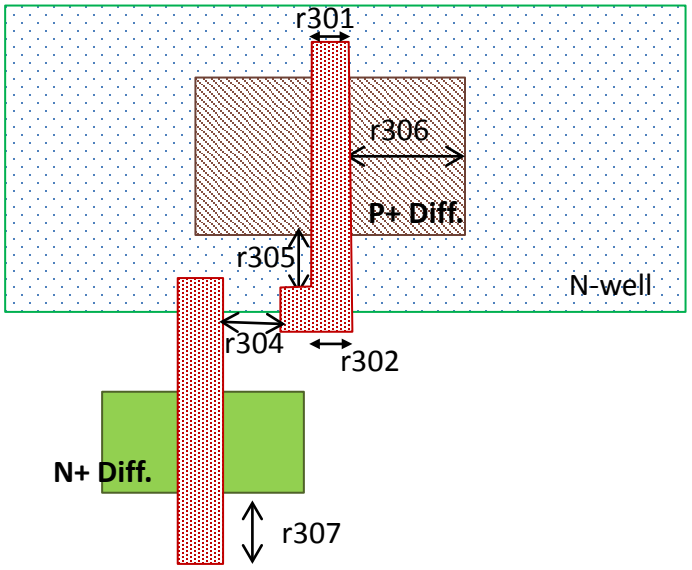
r201 → Minimum P diffusion size
r202 → Minimum distance between P diffusions
r203 → Extra well after diffusion
r204 → Minimum distance between diffusion and well

Design rules

Microwind

- file.rul

Polysilicon



r301 → Minimum polysilicon width
r302 → Minimum polysilicon gate on diffusion N+
r304 → Minimum distance between two polysilicon

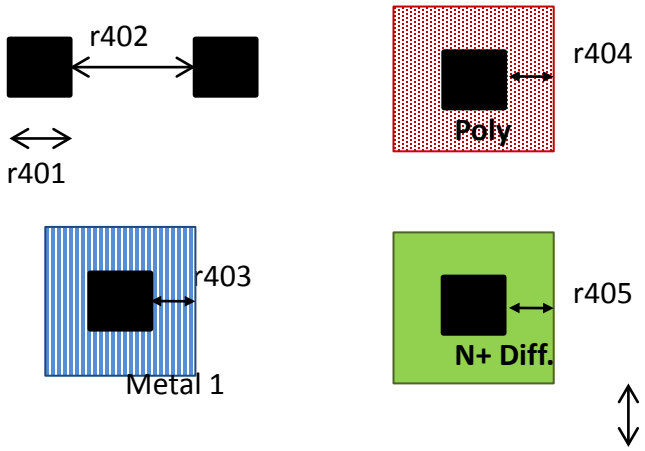
r305 → Minimum distance between polysilicon and other diffusion
r306 → Diffusion after polysilicon
r307 → Extension of polysilicon after diffusion

Design rules

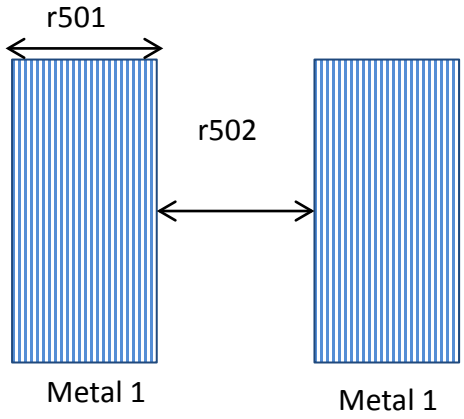
Microwind

- file.rul

Contacts



Metal 1



r401 → Minimum contact widht
r402 → Minimum distance between two contacts
r403 → Extra metal over contact
r404 → Extra polysilicon over contact
r405 → Extra diffusion over contact

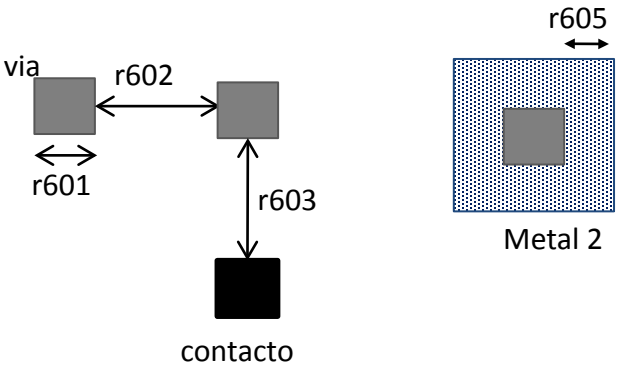
r501 → Minimum metal width
r502 → Minimum distance between metals

Design rules

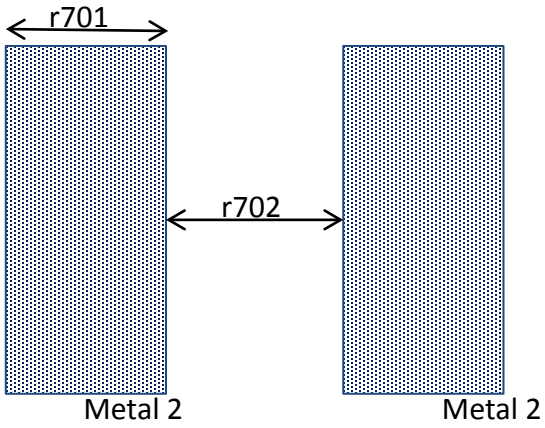
Microwind

- file.rul

Via



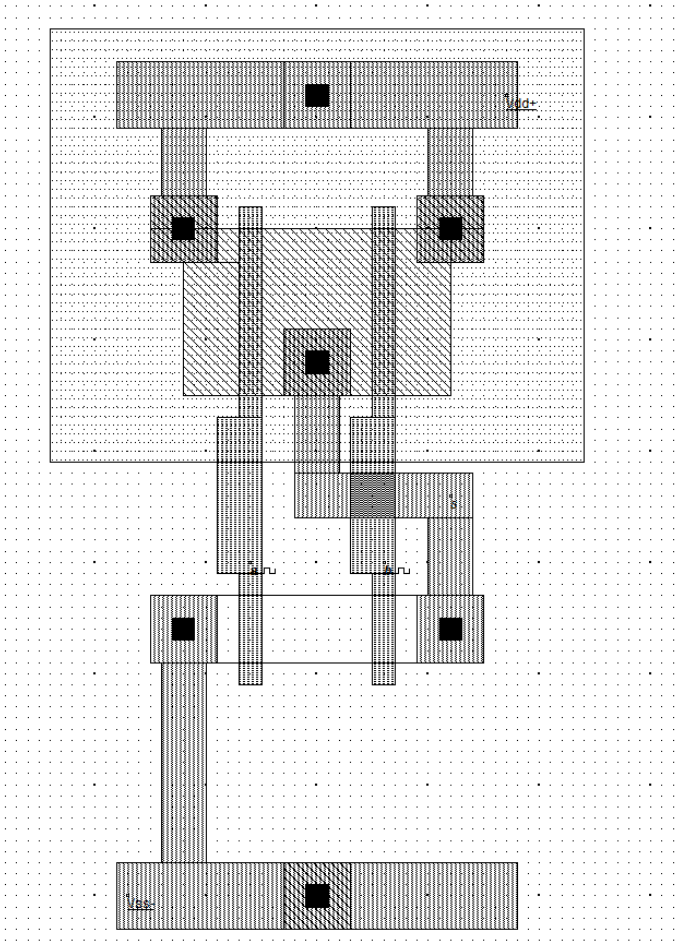
Metal 2

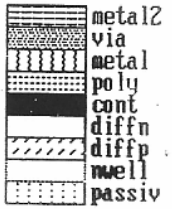


r601 → Minimum via width
r602 → Minimum distance between two via
r603 → Minimum distance between via and contact
r604 → Extra metal 1 over via
r605 → Extra metal 2 over via

r701 → Minimum metal 2 width
r702 → Minimum distance between two metal 2

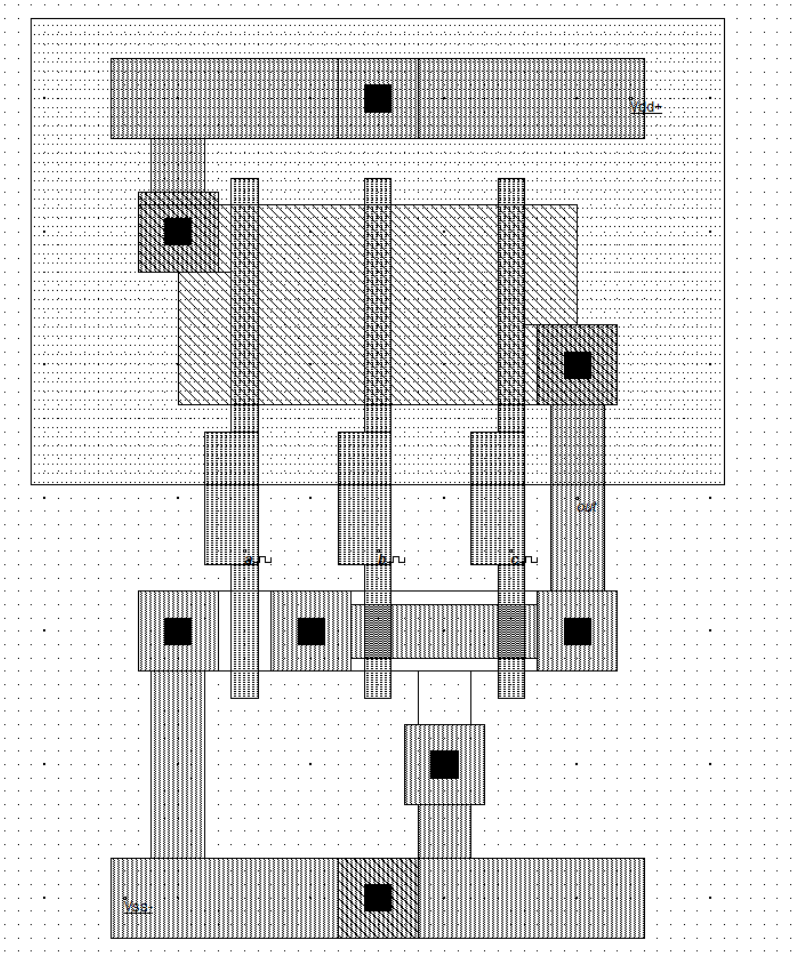
Examples





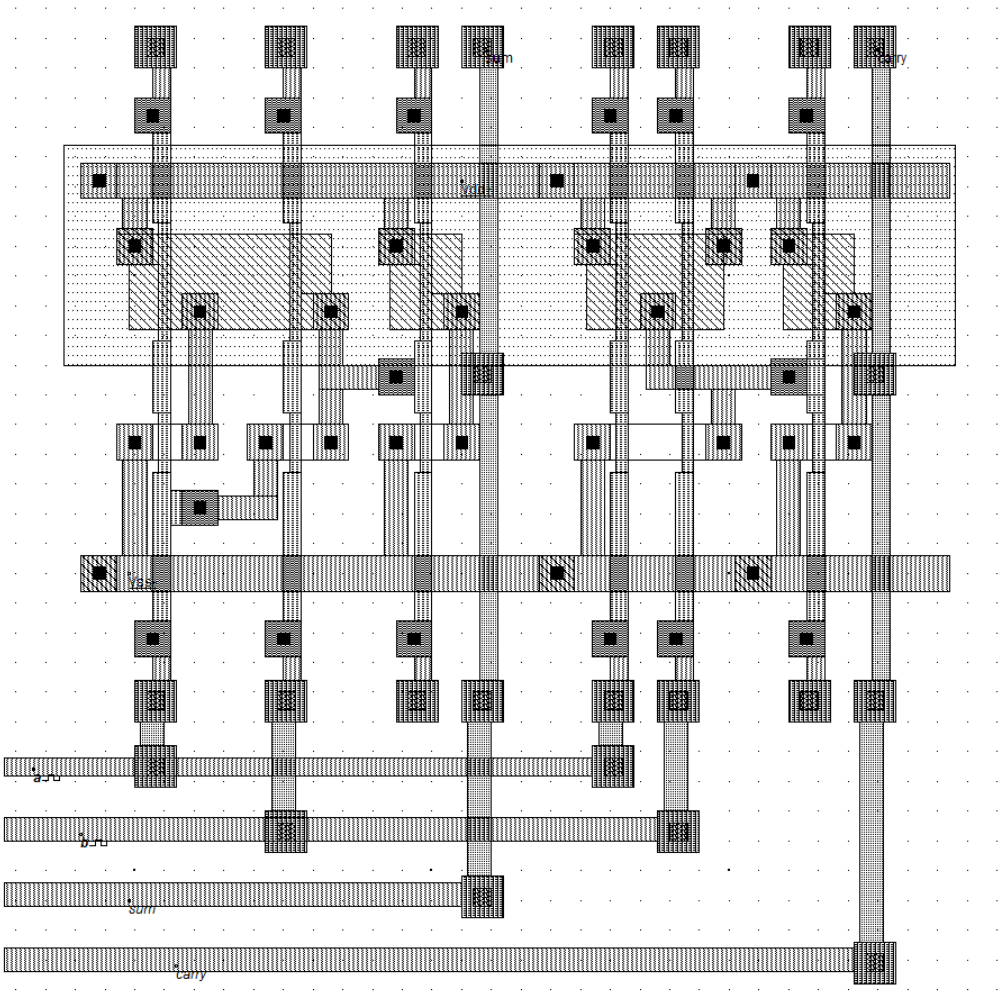
2-inputs NAND

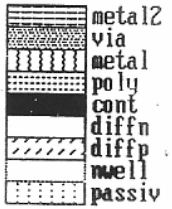
Examples



3-inputs NOR

Examples


vdd
vss
a
b
sum
carry


metal2
via
metal
poly
cont
diffn
diffp
nwell
passiv