Universidad
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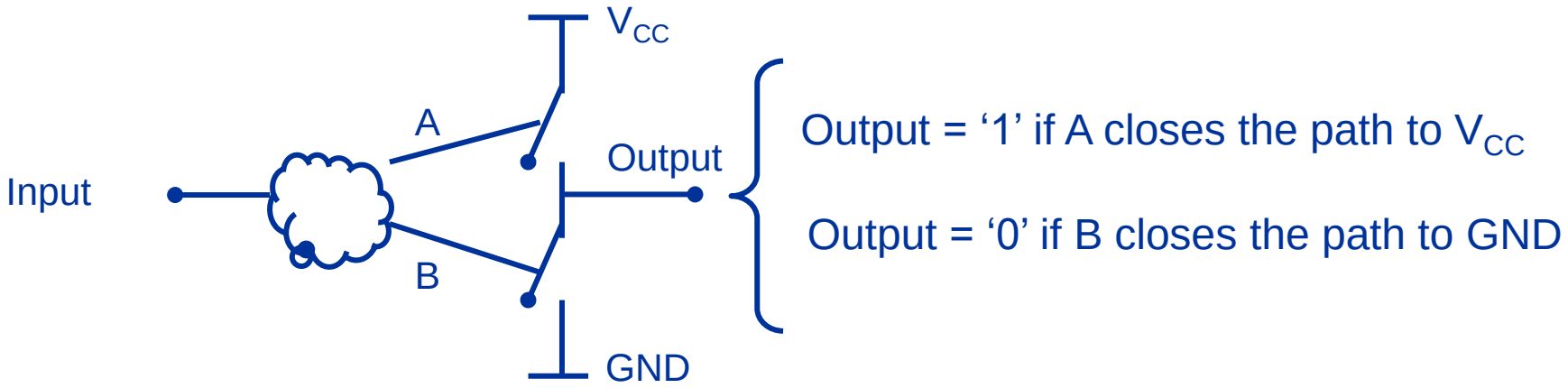
Digital Technologies: review

Contents

Logic families

- Logic gates process digital information (they receive '0's and '1's and generate '0's and '1's).
- The logical values ('0' and '1') are associated with voltage values (0 V and V_{CC}, maximum voltage (0.8, 1.2, 1.5, 3.3, 5 V).
- The construction of logic gates requires the use of electronic devices, which are capable of processing the inputs and generating the outputs, maintaining the correspondence between voltage levels and logical levels.
- These electronic devices can be understood as switches that allow connection to ground (GND) or power (V_{CC}).



Logic families

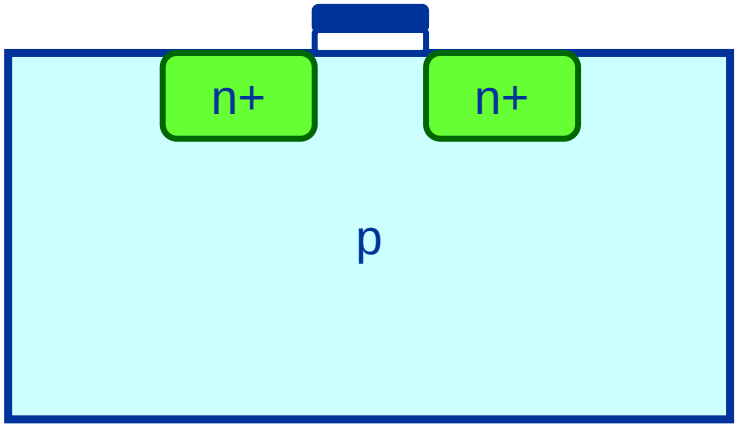
- In general, these "switches" are transistors.
- Depending on the type of transistor used, we speak of "Logical Family" because all logic gates are generated with that device.
- The most widespread logic family is CMOS due to its low power consumption and high integration capacity. It uses the MOSFET transistor.
- Other families are TTL (bipolar transistor: BJT), ECL (differential pair with BJT), BiCMOS (mixed MOSFET-BJT), etc..

CMOS family

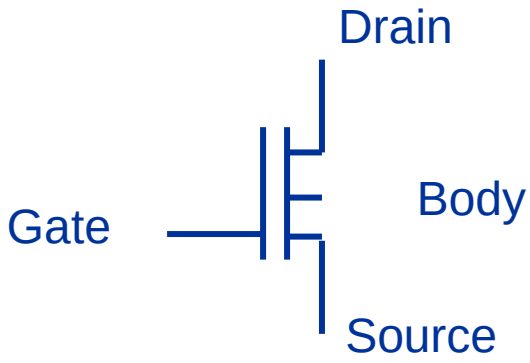
MOSFET (voltage-driven device) transistor-based family).

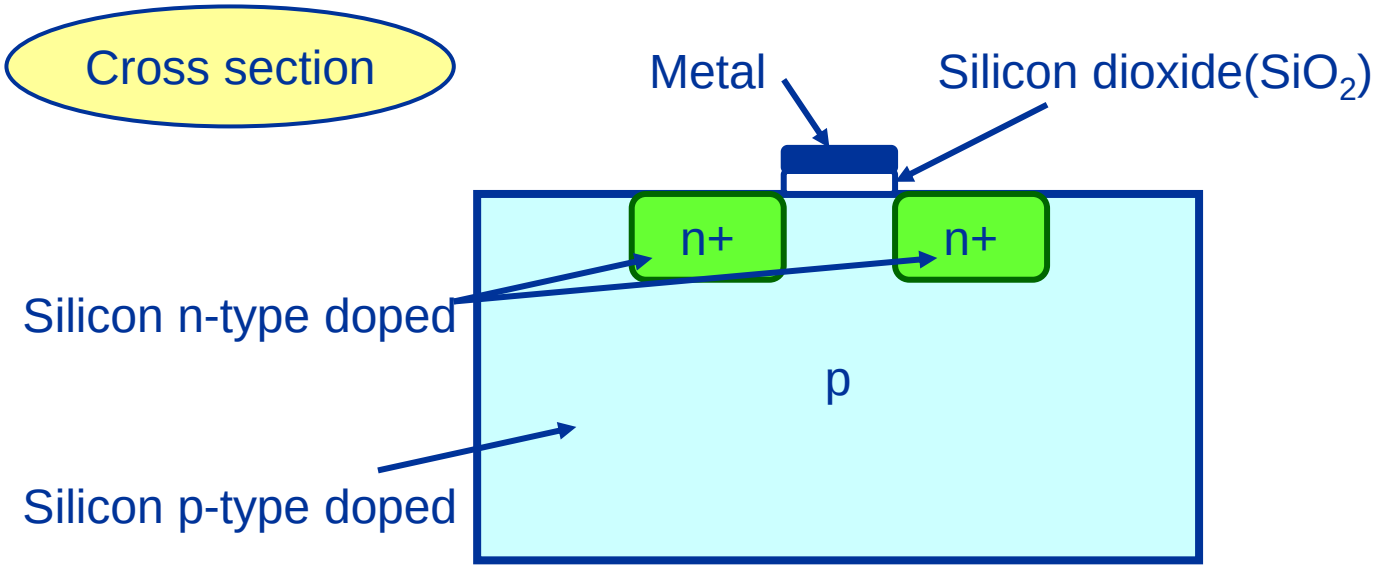
MOSFET: Metal-Oxide-Semiconductor- Field-Effect Transistor

Cross section

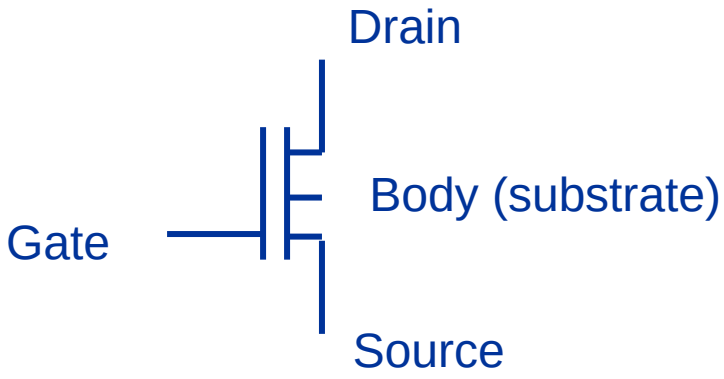


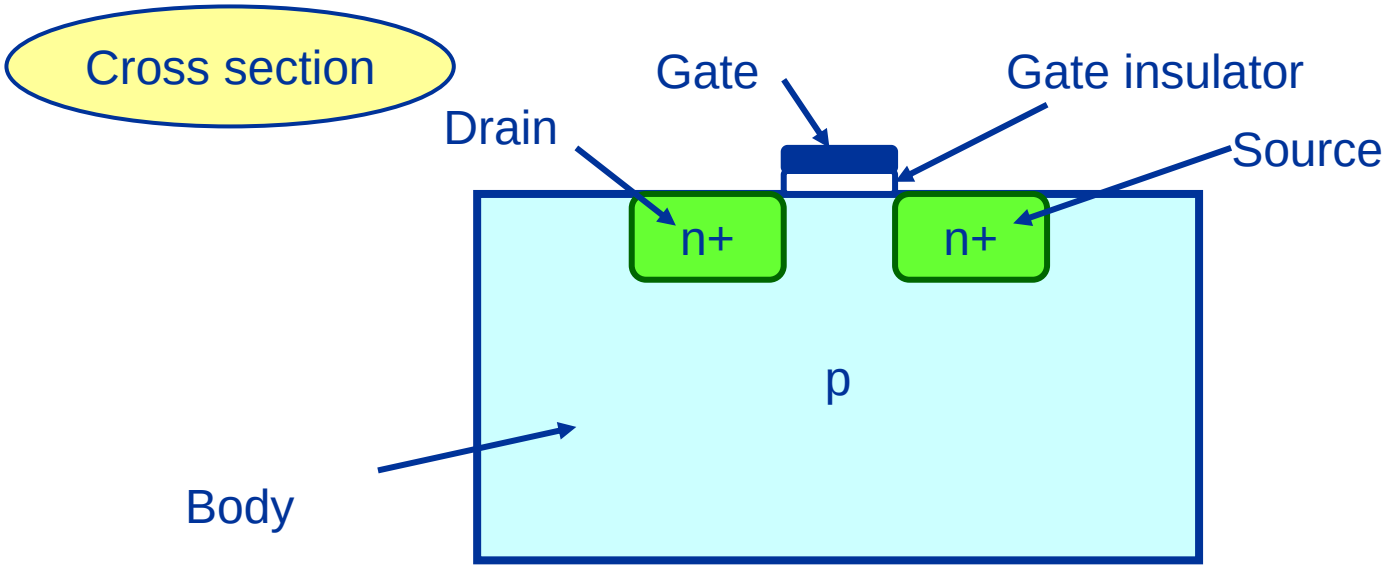
CMOS family





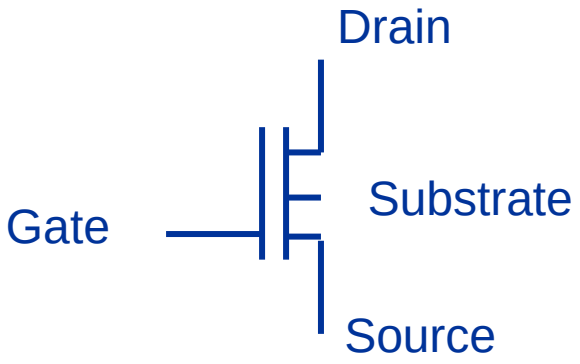
CMOS family

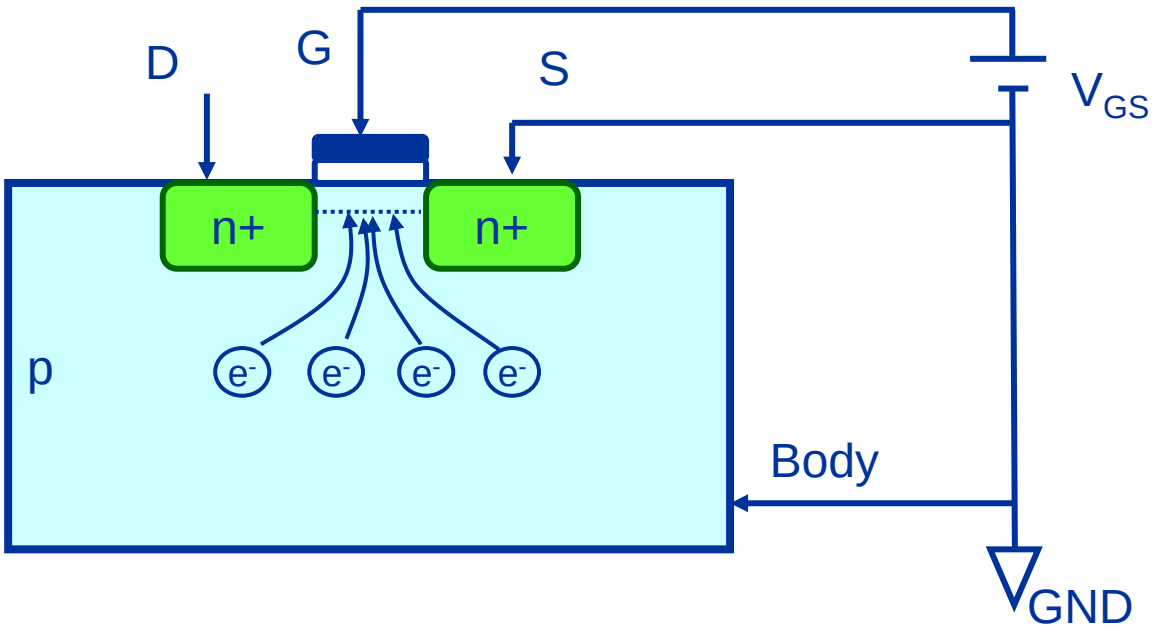




CMOS family

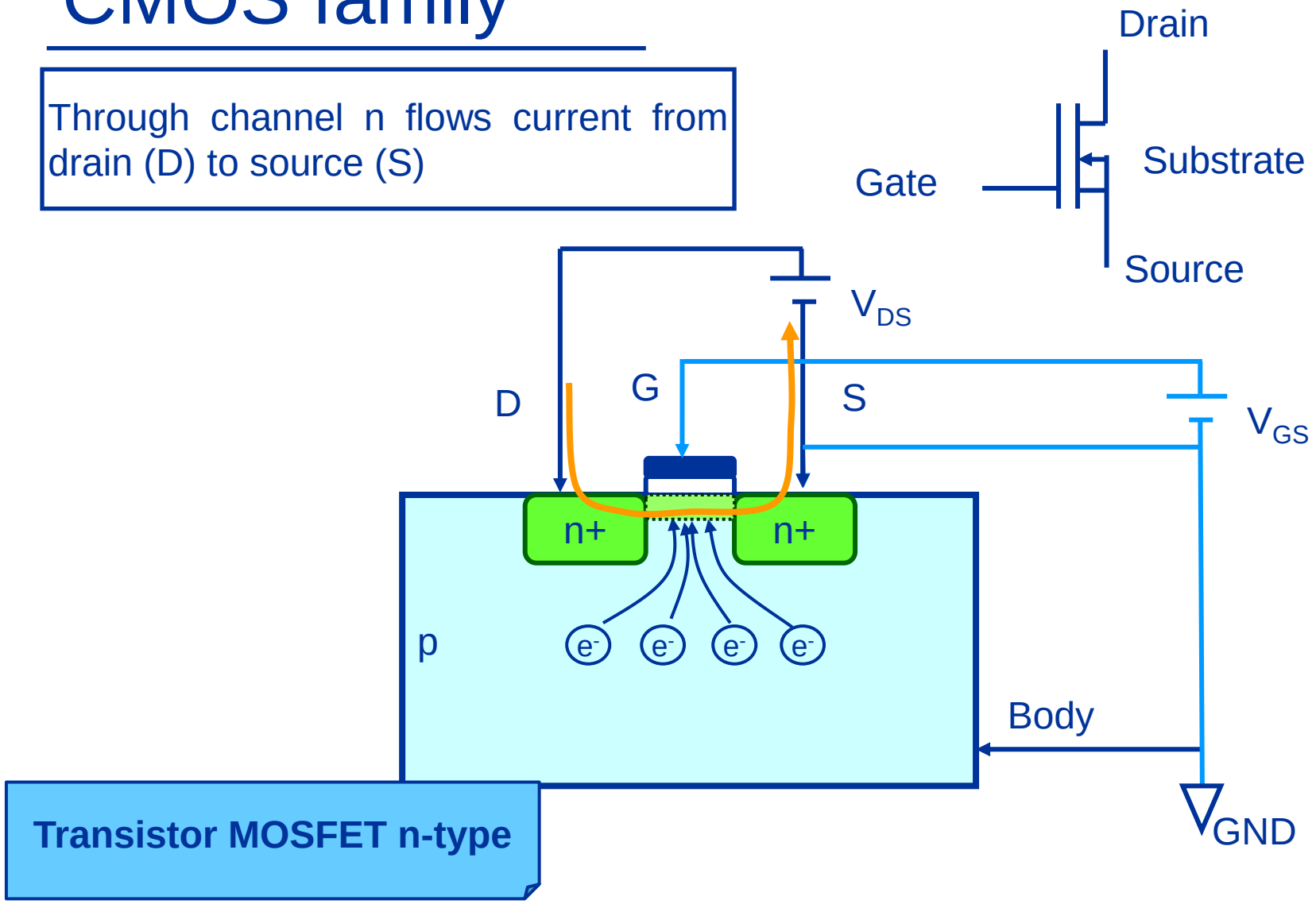
A channel between D and S is generated by voltage application in G.





CMOS family

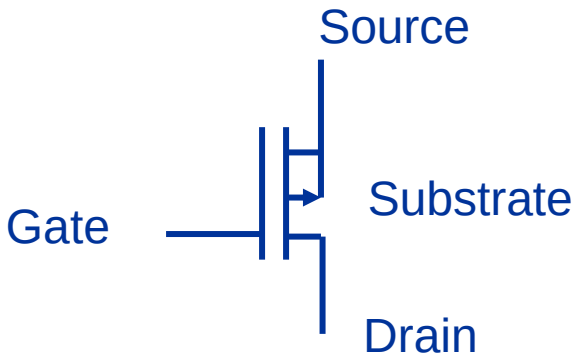
Through channel n flows current from drain (D) to source (S)



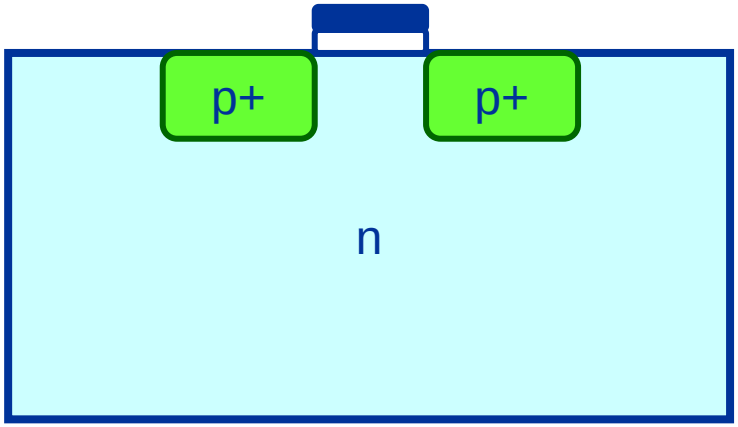
Transistor MOSFET n-type

CMOS family

Transistor MOSFET p-type

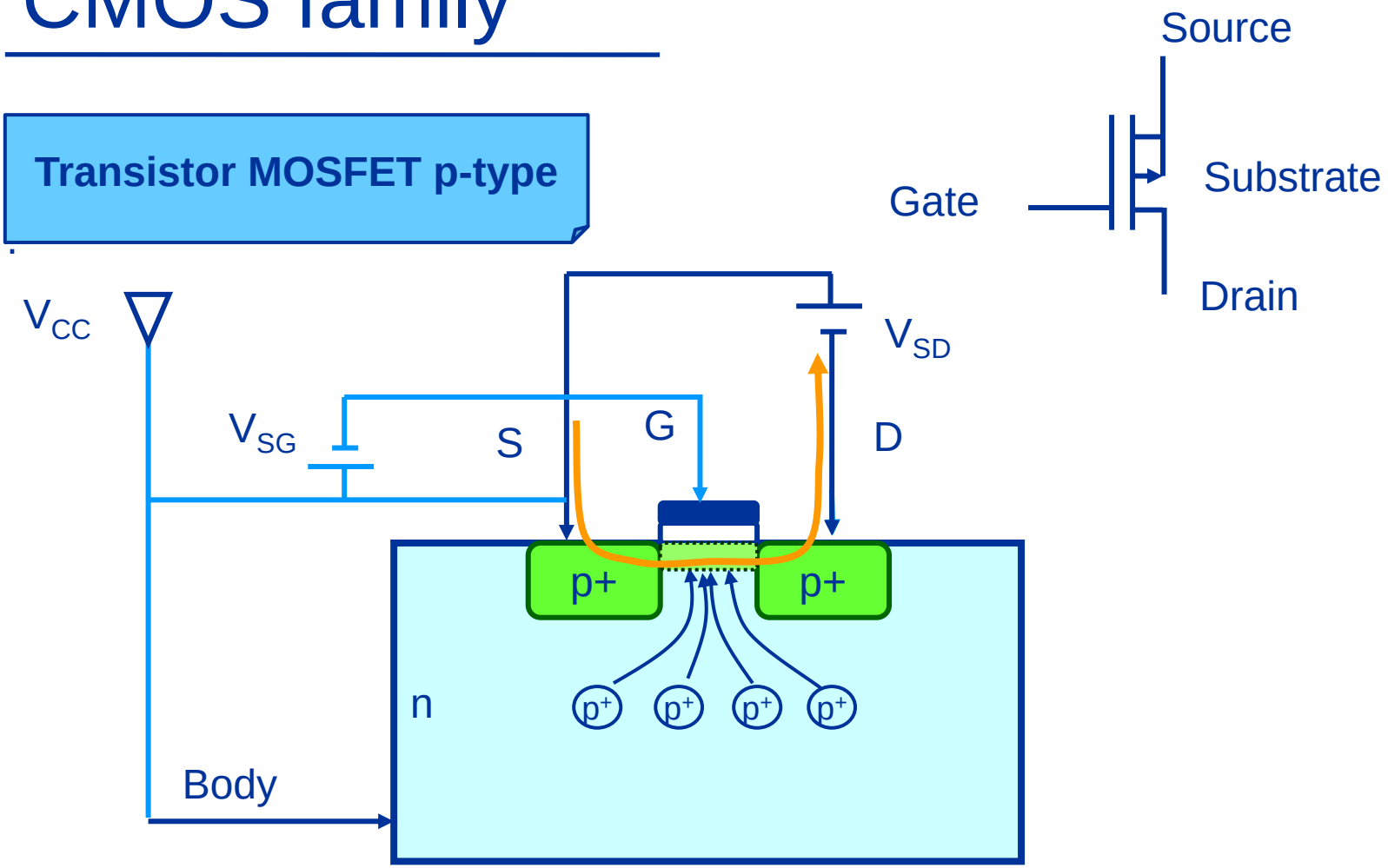


Cross section



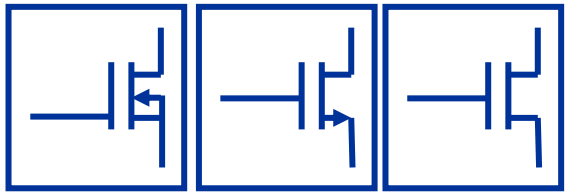
CMOS family

Transistor MOSFET p-type



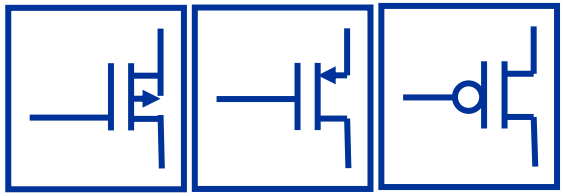
CMOS family

Transistor n-type:



The source is at minimum potential
The substrate is to ground (GND)
The current flows from Drain to Source (D→S)
The Gate-Source (GS) voltage is what generates the channel between D and S

Transistor p-type:



The source is at its maximum potential
The substrate is at power (VCC)
The current flows from Source to Drain (S→D)
The Gate-Source (GS) voltage is what generates the channel between S y D

CMOS family

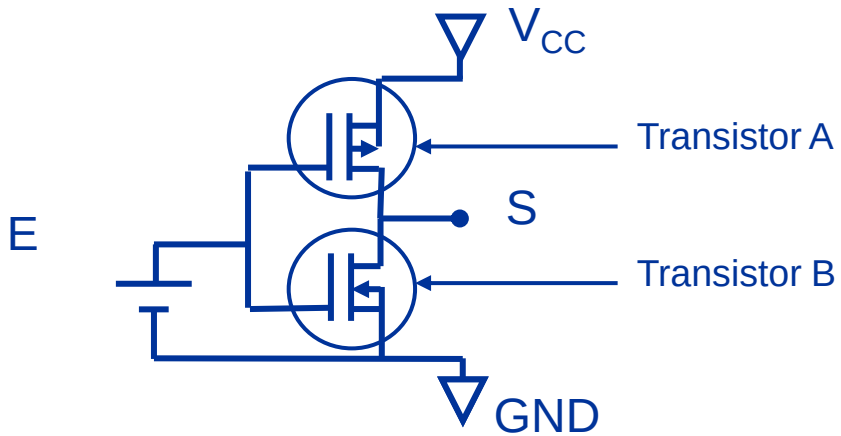
The combination of p-type and n-type transistors generates CMOS (Complementary MOSFET) technology.

Thanks to this technology, digital integrated circuits of great density and with very low consumption are achieved

1. N-type transistors provide the low values (logical '0')
2. P-type transistors provide the high values (logical '1')

CMOS family

INVERTER CMOS

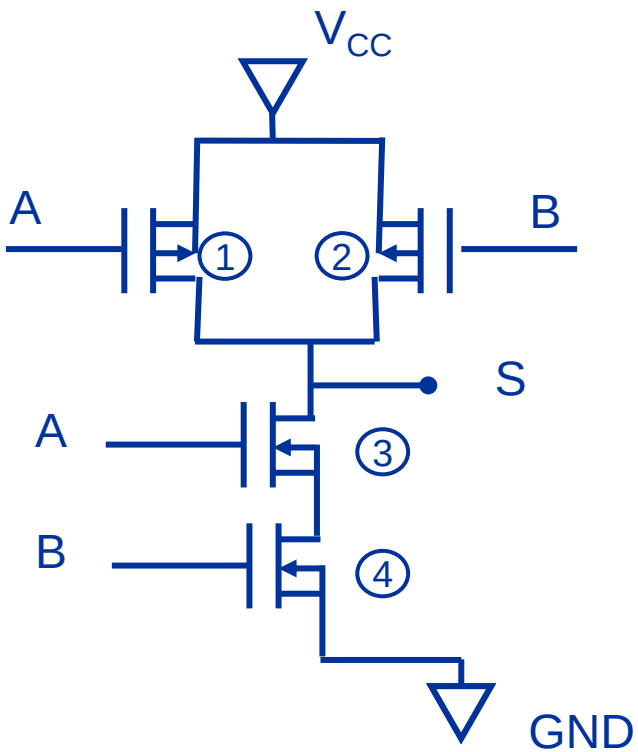


Cases:

1. E = ‘1’
   - A with no channel (no driving)
   - B with channel (yes driving)
2. E = ‘0’
   - A with channel (yes driving)
   - B with no channel (no driving)

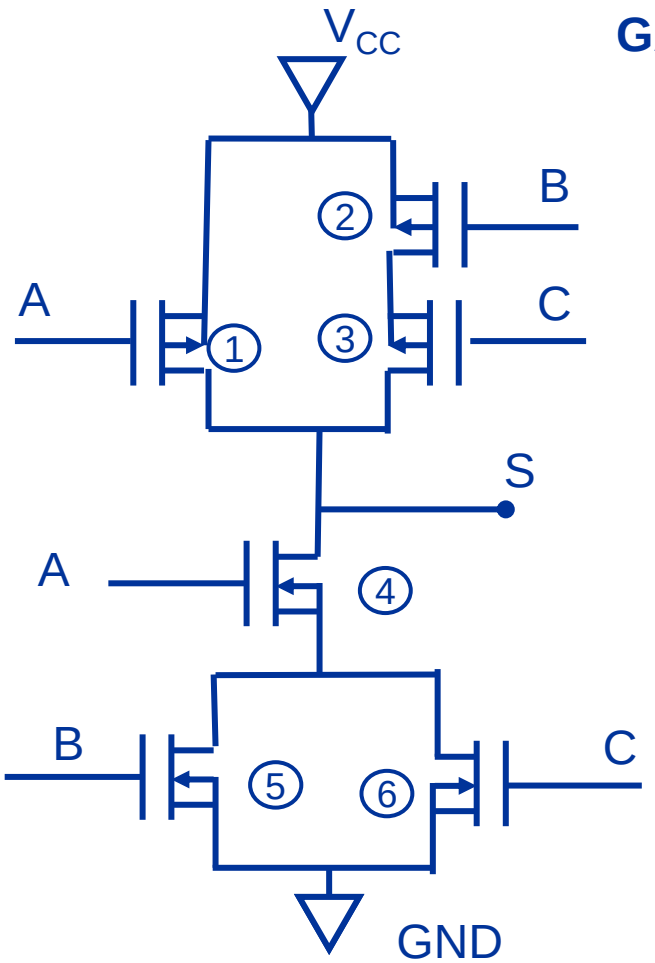
CMOS family

GATE NAND CMOS



A	B	①	②	③	④	S
0	0	on	on	off	off	1
0	1	on	off	off	(on)	1
1	0	off	on	(on)	off	1
1	1	off	off	(on)	(on)	0

CMOS family



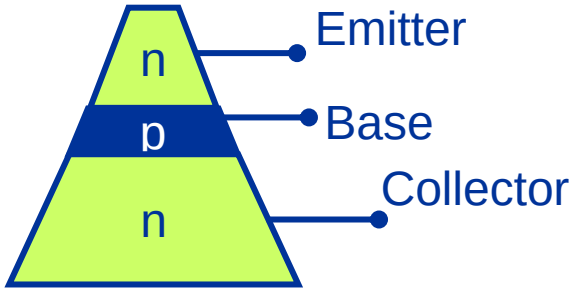
GATE ?? CMOS

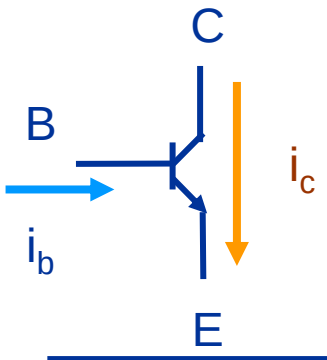
A	B	C	①	②	③	④	⑤	⑥	S
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

TTL family

Family based on the BJT transistor (current-driven device).

TTL: Transistor-transistor Logic
BJT: Bipolar Junction Transistor





The injection of current into the base generates an increase in potential that allows the passage of current between the emitter and the collector.

TTL family

To use the bipolar transistor as a switch it is necessary to use two elements. The first (T1) works governed by the voltage that we put in the emitter (Input).

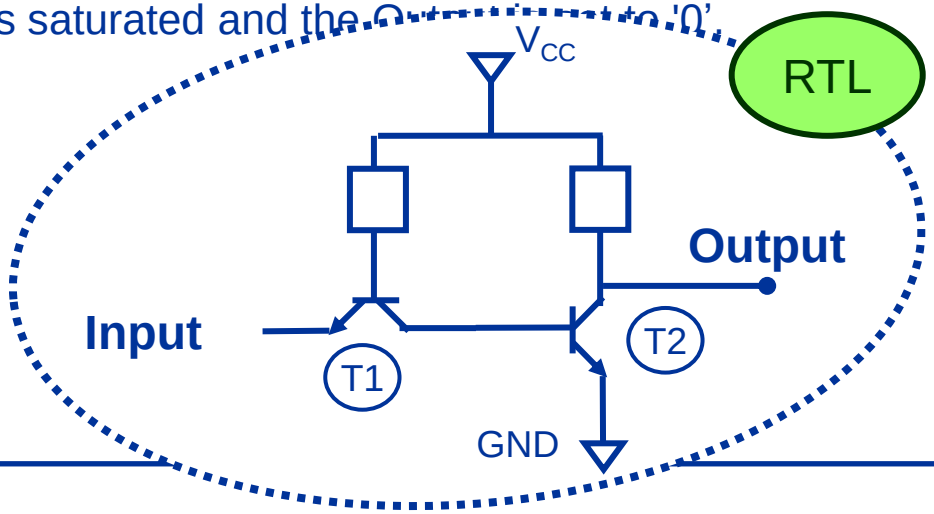
- If we connect the emitter to ground ('0'), T1 is saturated and in its collector there will be a '0'.
- If we connect the emitter to power ('1'), T1 is reverse polarized and there will be a '1' in its collector.

The T1 collector is the basis of T2.

- If in the base of T2 there is a '0', T2 is cut and the Output is set to '1'
- If in the base of T2 there is a '1', T2 is saturated and the Output is set to '0'

THEN:

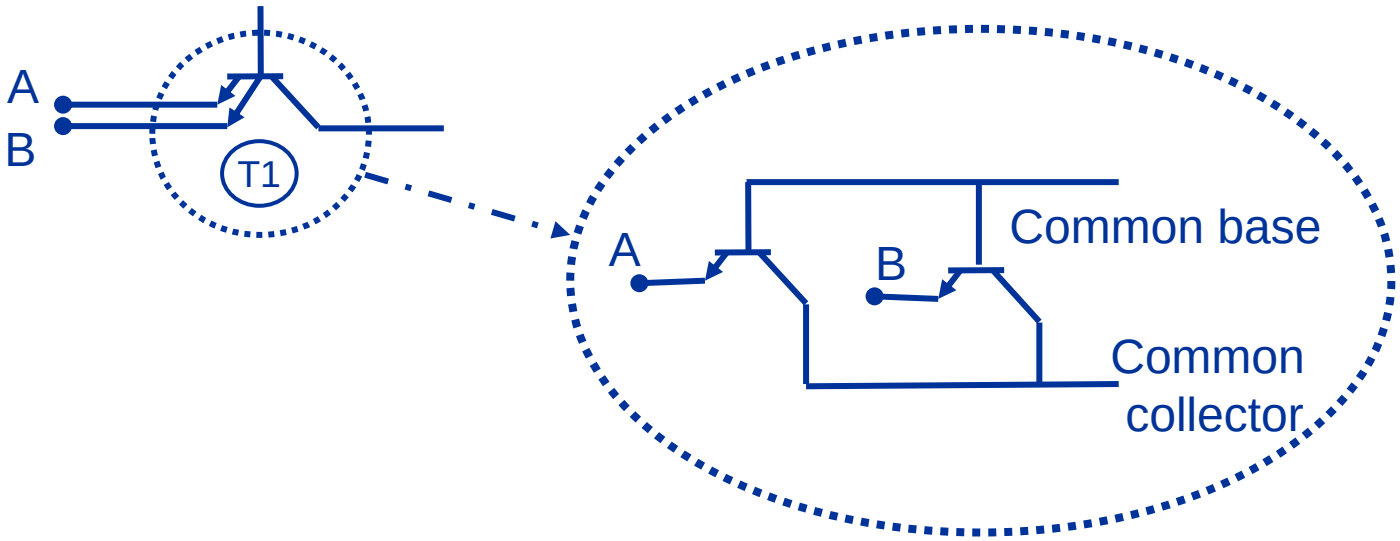
- **Si Input = '0' ➔ Output = '1'**
- **Si Input = '1' ➔ Output = '0'**



TTL family

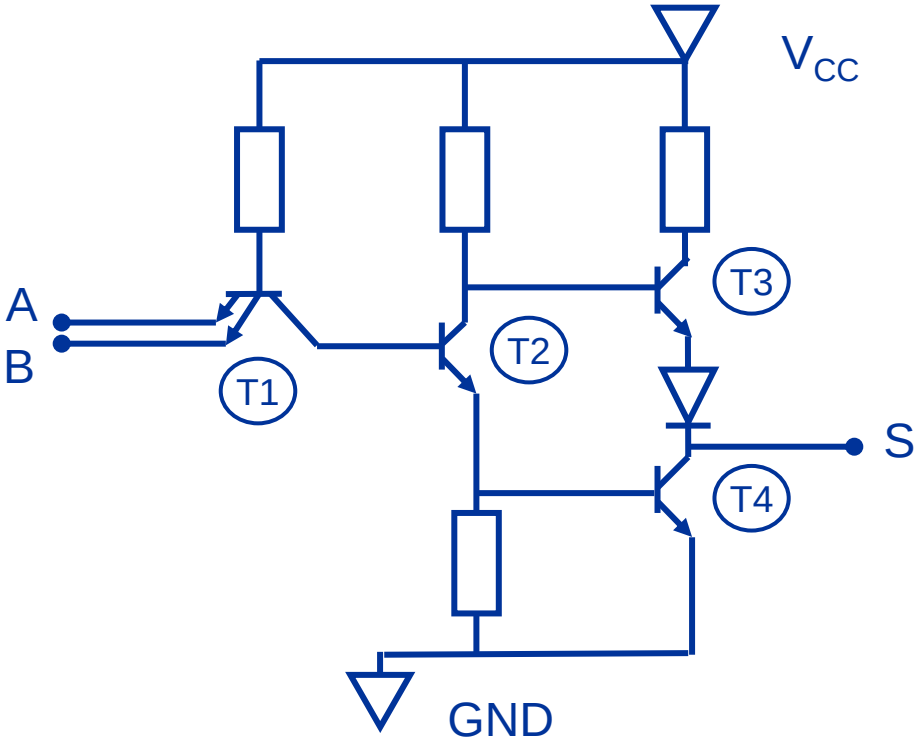
To input more inputs the multi-emitter transistor is used

- If A or B are a '0' (0 V) the transistor is saturated and in the collector there is a '0'
- If in A and B there is a '1' (Vcc) the transistor is reverse biased and the current would circulate from emitter to collector



TTL family

To improve noise immunity and switching speed, output is added in Totem-ple (two transistors in the output stage so that one sets the '0's and one the '1's)



TTL

CASES:

1. A and B = ‘1’.
   - Reverse-polarized T1
   - Saturated T2
   - Saturated T4
   - Output = '0'
2. A or B = ‘0’
   - Saturated T1
   - T2 cut
   - T4 cut
   - Saturated T3
   - Output = '1’

LOGIC GATE➔ NAND

Characteristics of integrated circuits

1. Supply voltage
2. Input and Output Voltages
3. Noise immunity
4. Velocity
5. Consumption
6. Input and Output Intensities
7. Max Fan-out

Characteristics of integrated circuits:

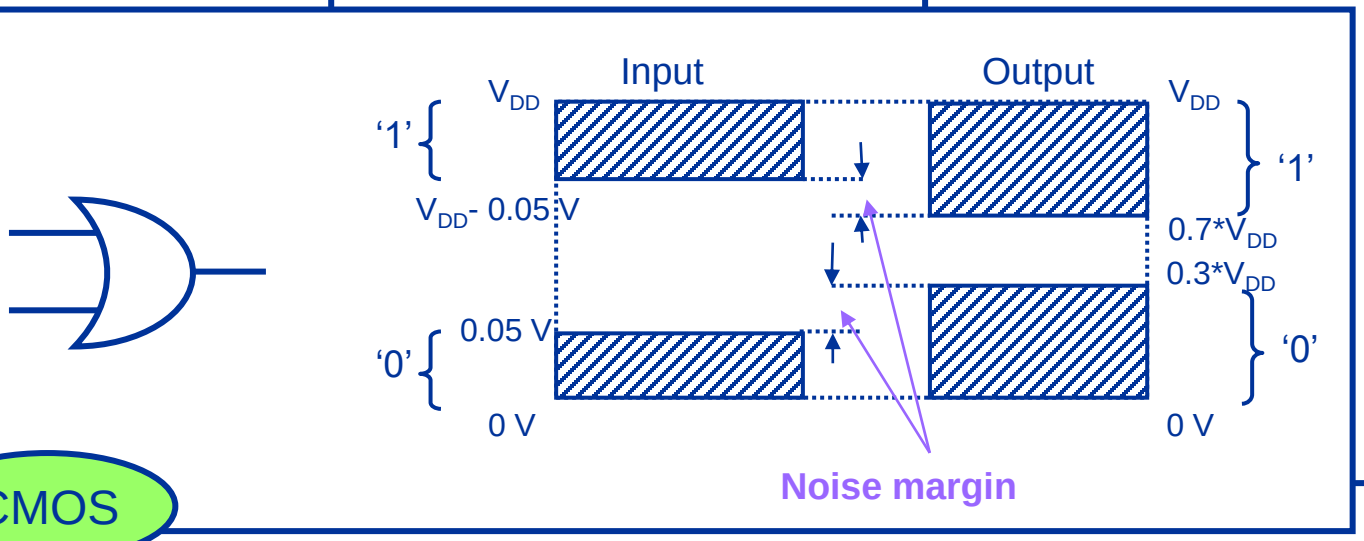
Supply voltaje & Noise inmunity

Characteristic	CMOS	TTL
Supply voltage	0,8 – 15 V	5 V

Characteristics of integrated circuits:

Supply voltaje & Noise inmunity

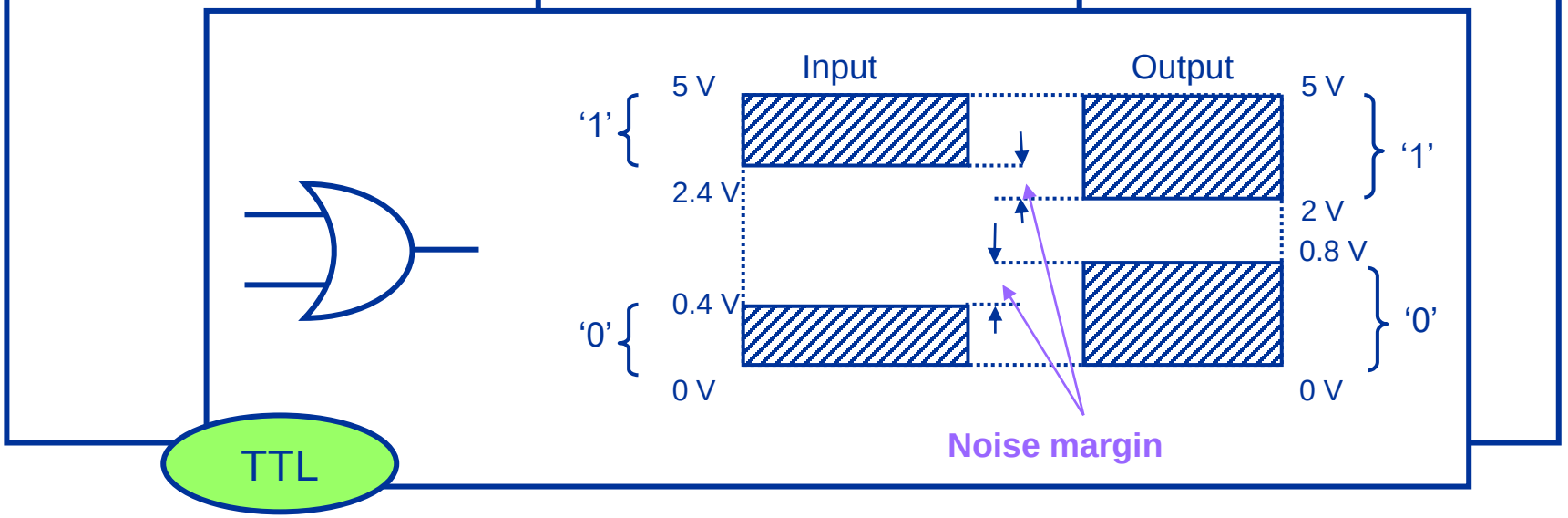
Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}				



Characteristics of integrated circuits:

Voltage levels

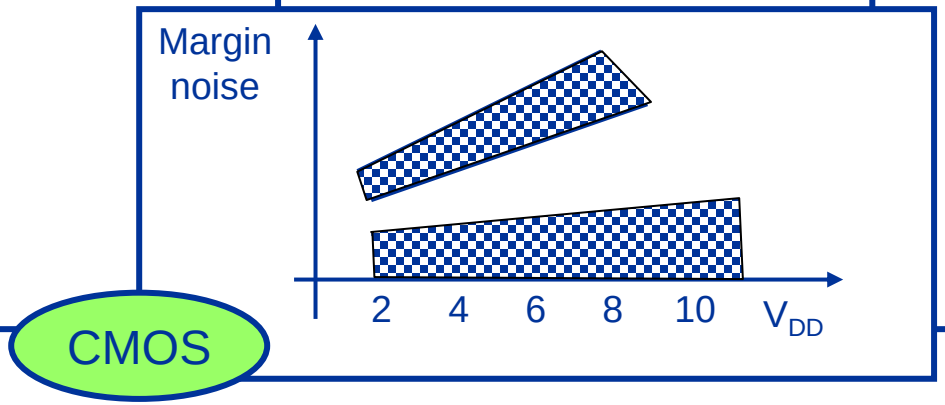
Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}	5 V ÷ 2.4 V	0 V ÷ 0.4 V	5 V ÷ 2 V	0 V ÷ 0.8 V



Characteristics of integrated circuits:

Inmunidad al ruido

Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}	5 V ÷ 2.4 V	0 V ÷ 0.4 V	5 V ÷ 2 V	0 V ÷ 0.8 V
Noise Inmunity	It depends on V_{DD}				0.4 V			



Characteristics of integrated circuits:

Speed

Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}	5 V ÷ 2.4 V	0 V ÷ 0.4 V	5 V ÷ 2 V	0 V ÷ 0.8 V
Noise immunity	It depends on V_{DD}				0.4 V			
Response speed (propagation delay)	t_{pHL}; t_{pLH} ≈ ns (frequencies till GHz)				t_{pHL}; t_{pLH} ≈ ns (**faster than CMOS**)			

Characteristics of integrated circuits :

Power consumption

Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}	5 V ÷ 2.4 V	0 V ÷ 0.4 V	5 V ÷ 2 V	0 V ÷ 0.8 V
Noise immunity	It depends on V_{DD}				0.4 V			
Response speed (propagation delay)	t_{pHL}; t_{pLH} ≈ ns (frequencies till GHz)				t_{pHL}; t_{pLH} ≈ ns (**faster than CMOS**)			
Power consumption	Static consumption = 0 W Dynamic consumption = f(freq) **Much lower than in TTL**				Static consumption = V_{CC}* I_{CC}			

Characteristics of integrated circuits :

I/O currents

Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}	5 V ÷ 2.4 V	0 V ÷ 0.4 V	5 V ÷ 2 V	0 V ÷ 0.8 V
Noise immunity	It depends on V_{DD}				0.4 V			
Response speed (propagation delay)	t_{pHL}; t_{pLH} ≈ ns (frequencies till GHz)				t_{pHL}; t_{pLH} ≈ ns (**faster than CMOS**)			
Power consumption	Static consumption = 0 W Dynamic consumption = f(freq) **Much lower than in TTL**				Static consumption = V_{CC}* I_{CC}			
Input/Output currents	I_{OH}	I_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}	I_{IH}	I_{IL}
	≈ 1mA	≈ 1mA	0 A	0 A	-400 μA	16 mA	40 μA	-1.6 mA

Characteristics of integrated circuits:

Input Capacitance

Characteristic	CMOS				TTL			
Supply voltage	0,8 – 15 V				5 V			
Voltage levels	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}
	V_{DD} ÷ V_{DD}-0.05	0 V ÷ 0.05V	V_{DD} ÷ 0.7* V_{DD}	0 V ÷ 0.3* V_{DD}	5 V ÷ 2.4 V	0 V ÷ 0.4 V	5 V ÷ 2 V	0 V ÷ 0.8 V
Noise immunity	It depends on V_{DD}				0.4 V			
Response speed (propagation delay)	t_{pHL}; t_{pLH} ≈ ns (frequencies till GHz)				t_{pHL}; t_{pLH} ≈ ns (**faster than CMOS**)			
Power consumption	Static consumption = 0 W Dynamic consumption = f(freq) **Much lower than in TTL**				Static consumption = V_{CC}* I_{CC}			
Input/Output currents	I_{OH}	I_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}	I_{IH}	I_{IL}
	≈ 1mA	≈ 1mA	0 A	0 A	-400 μA	16 mA	40 μA	-1.6 mA
Maximum Fan-out	It depends on gate capacitance ≈ 5 pF. **Higher fan-out than TTL**				It depends on I/O currents. **Fan-out around 10.**			

Characteristics of integrated circuits:

Unconnected inputs

Characteristic	CMOS	TTL
Unconnected input	Connect '0' to '1' because you can take any value according to the parasitic capacitors	It is equivalent to having a logical '1'

Logic families : TTL-CMOS compatibility

Causes of incompatibility

1. Supply voltage
2. Input and Output Voltages
3. Input and Output Intensities

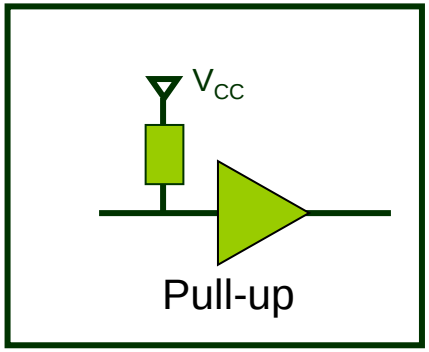
Solutions:

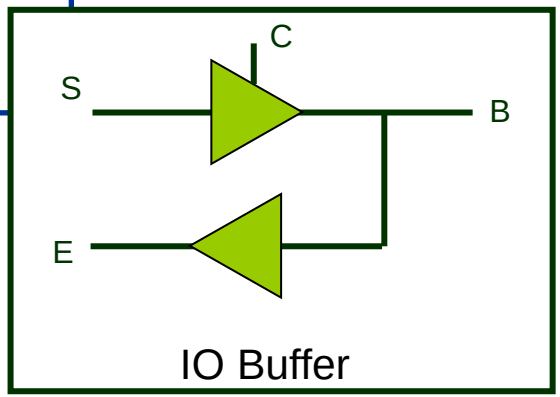
1. Open collector outlets
2. HCT intermediate family
3. Adaptation of levels

Logic families : Types of intputs and outputs

Inputs

1. Normal
2. With pull-up and pull-down resistance
   - Set the default value of the input when no value is set externally
3. Bidirectional





Outputs

1. Normal
2. Triestate
3. Open collector

Logic families:
Other logic families

ECL

1. Uses bipolar transistors
2. Transistors are never saturated
3. Tickets are differential
4. Inconvenience
   - High consumption
   - Current sources and voltage references are necessary → Large size
5. Advantages
   - High speed

AsGA

1. High speed compared to Silicon devices
2. High price