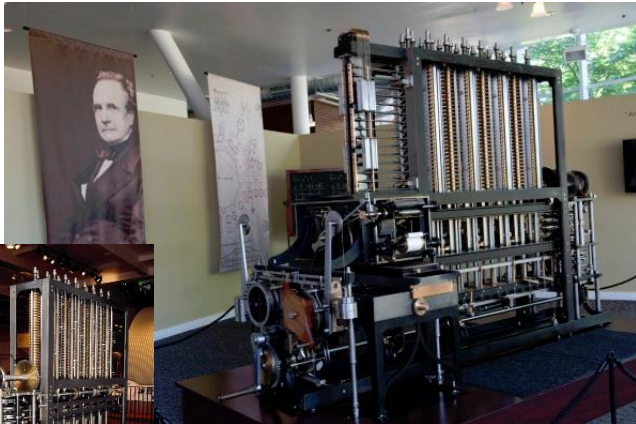


Integrated Circuits and Microelectronics

Difference Machine by Babbage (1822)



Univ. Cambridge

£17.470

25.000 components

Mechanical

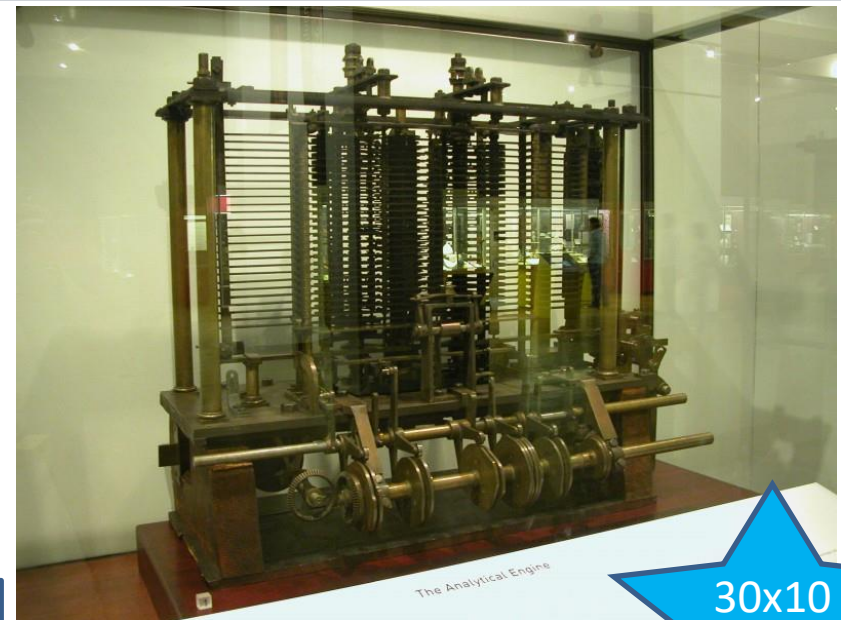
Decimal base

ComputerHistoryMuseum California Video

<https://www.youtube.com/watch?v=be1EM3gQkAY>

ScienceMuseum London

Analytical machine by Babbage (1834)



**Wiber
1875**

1812

**Scheutz
1837..1843
1855**

1822

Electromechanical
Decimal base

**H. Aiken
MARK I**

**1944 Univ. Harvard
(IBM)**

Additions in 4 s
Products in 8 s

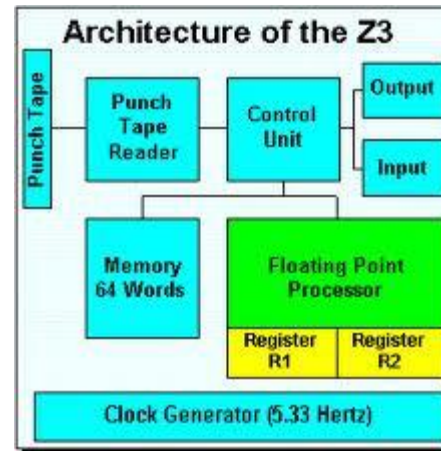
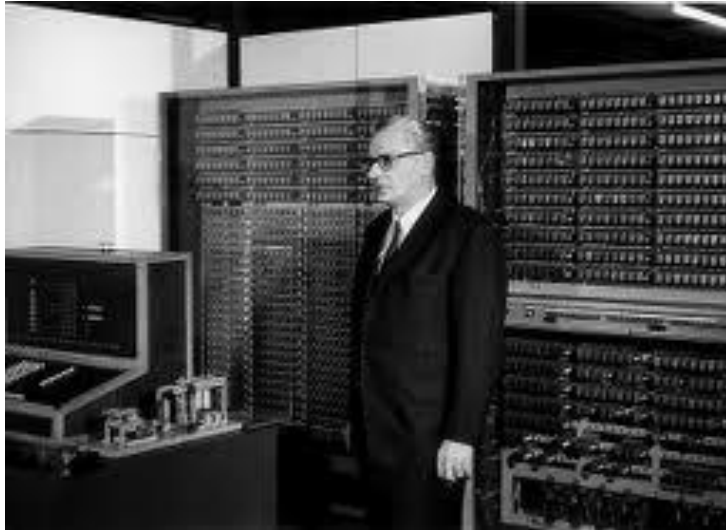
18x2
m²

\$250,000

30x10
m²

Z3: First programmable binary computer (1941)

K. Zuse



2.300 relays

Additions in 0.7 s; Products in 3 s

Electromechanical

Binary base

Float point

5
kW

Z4: First commercial binary computer (1942)

K. Zuse



2,500 relays

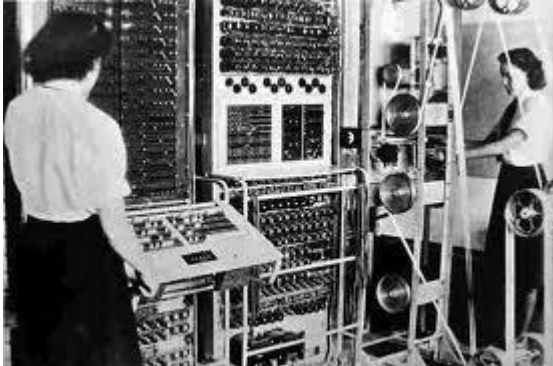
Additions in 400 ms

4
kW

COLOSSUS: First electronic calculator(1943)

Cryptoanalysis → Messages ciphered by Lorenz machine

Turing&Flowers



Electronic

Binary base

VIDEO

<http://www.youtube.com/watch?v=O8WXNPn1QKo&feature=related>



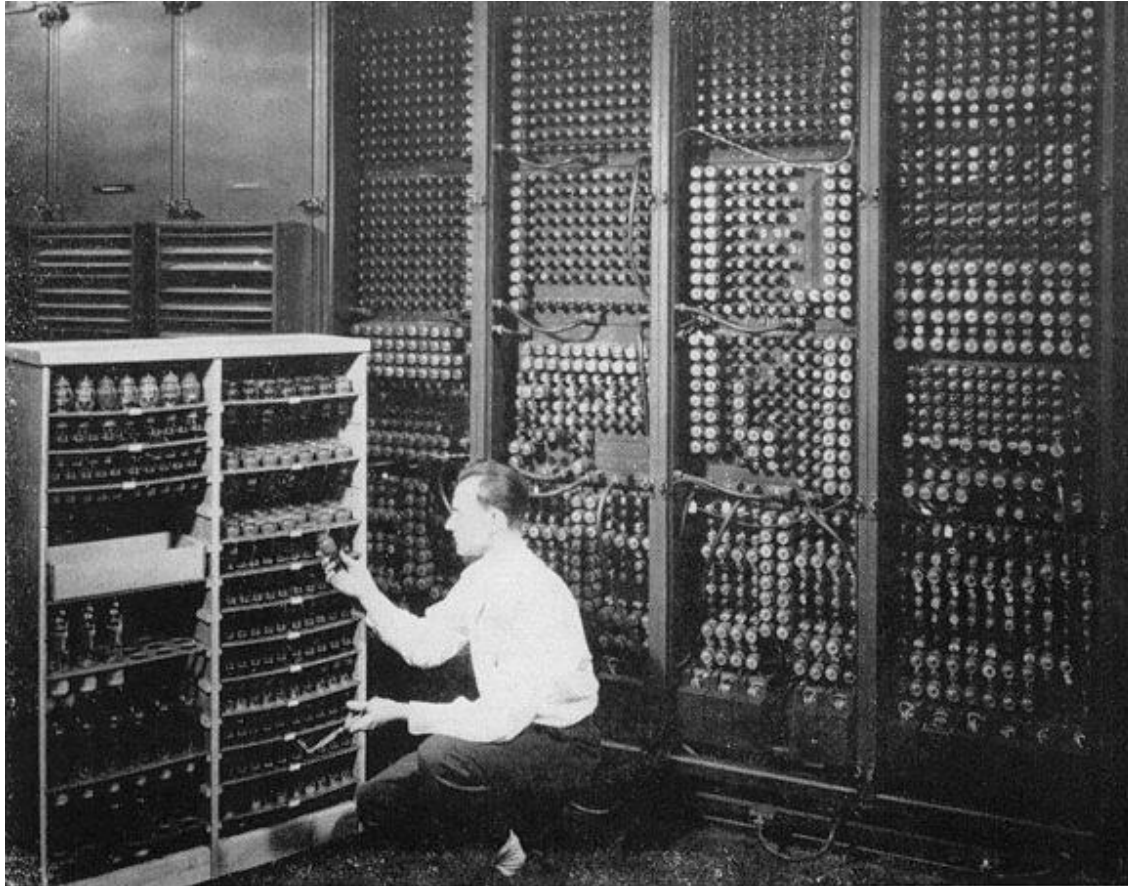
2,5x1.2
x3m³

1,500-2,400 vacuum tubes
5,000 characters per second

ENIAC: First electronic computer(1946)

Electronic Numerical Integrator And Computer

Eckert



Univ. Pennsylvania

167
m²

\$500,000

Electronic

Decimal base

160
kW

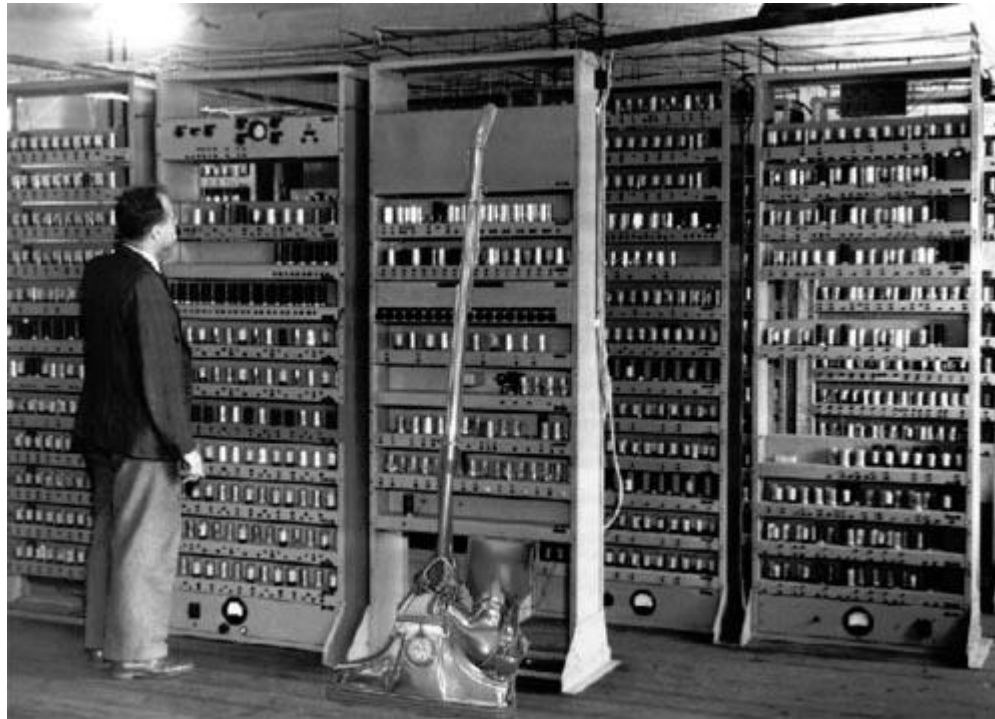
<http://www.youtube.com/watch?v=HJUo8t220Rk>

17,468 vacuum tubes. 7,200 diodes, 1,500 relays, 70,000 resistors, 10,000 capacitors y 5 million weldings
5,000 additions per second; 300 products per second

EDVAC: First electronic computer (arch. von Newman)(1949)

Electronic Discrete Variable Automatic Computer

Eckert&Mauchly



Univ. Pennsylvania

45.5
m²

\$500,000

Electronic

Binary base

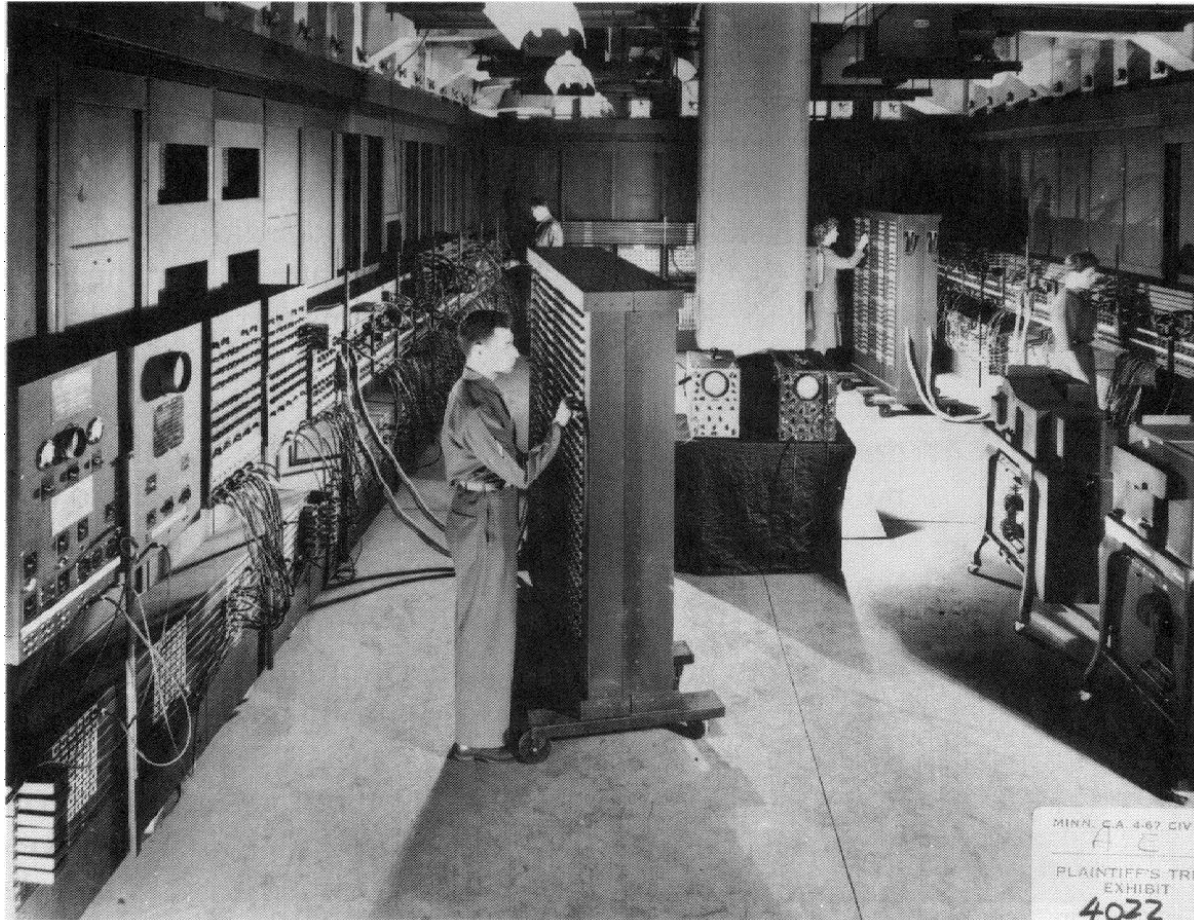
56
kW

6,000 vacuum tubes, 12,000 diodes
Sumas: 864 μ s y Products: 2.8 ms

UNIVAC: First commercial electronic computer(1951)

Electronic Numerical Integrator And Computer

Eckert & Mauchly



Census USA

33
m²

\$961,000

Electrónica

Base decimal

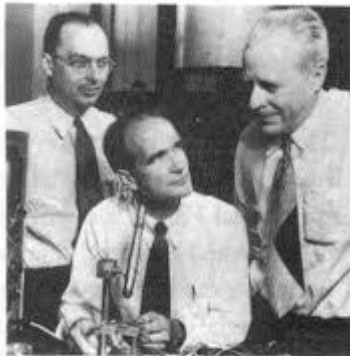
125
kW

[VIDEO](#)

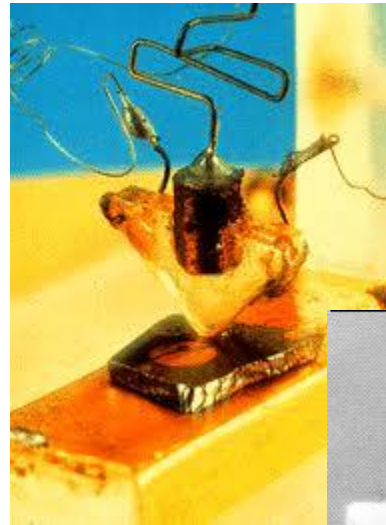
<http://www.youtube.com/watch?v=j2fURxbdIZs>

5,200 vacuum tubes
1,905 operations per second

The transistor (1947)

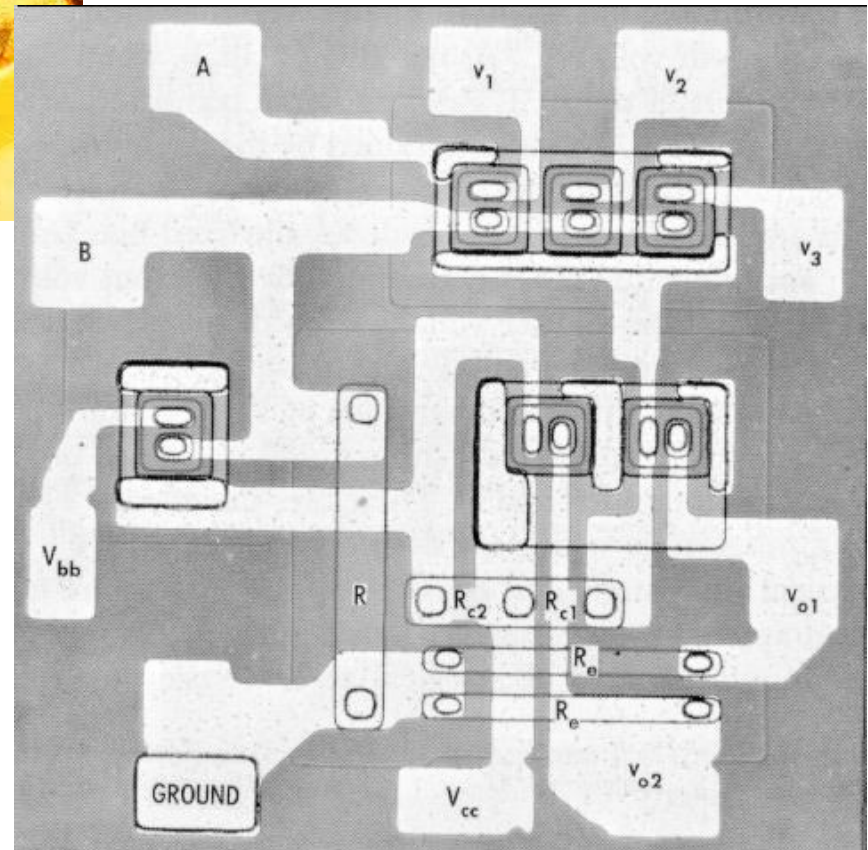


In 1956 John Bardeen, William Shockley and Walter Brattain shared the Nobel Prize in Physics for their discovery of the transistor.



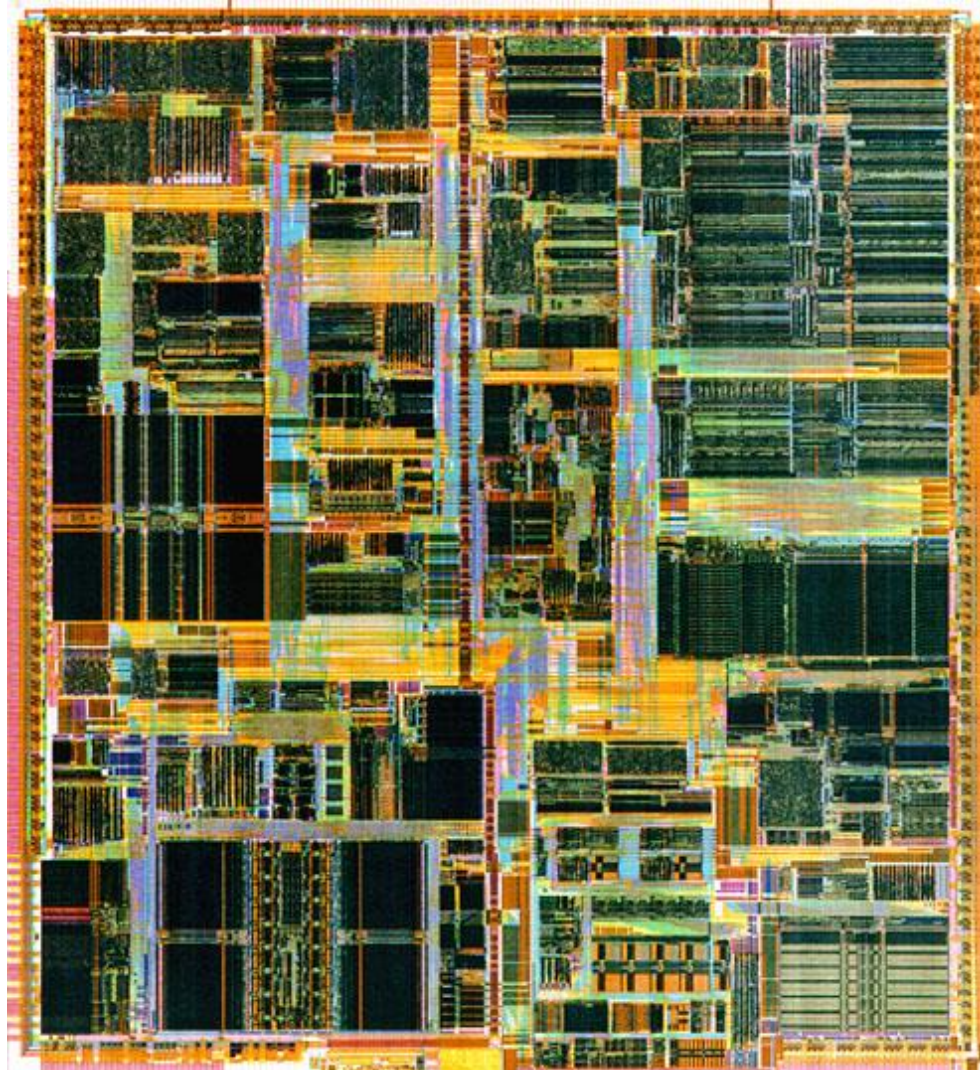
The integrated circuit (1951)

Kilby

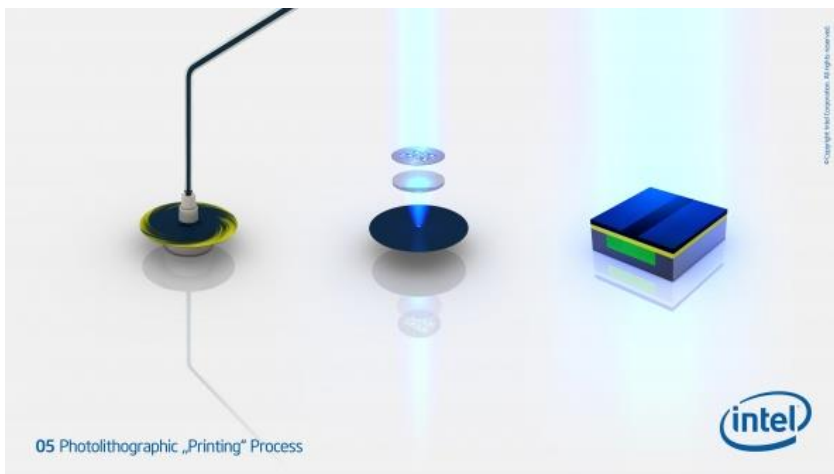
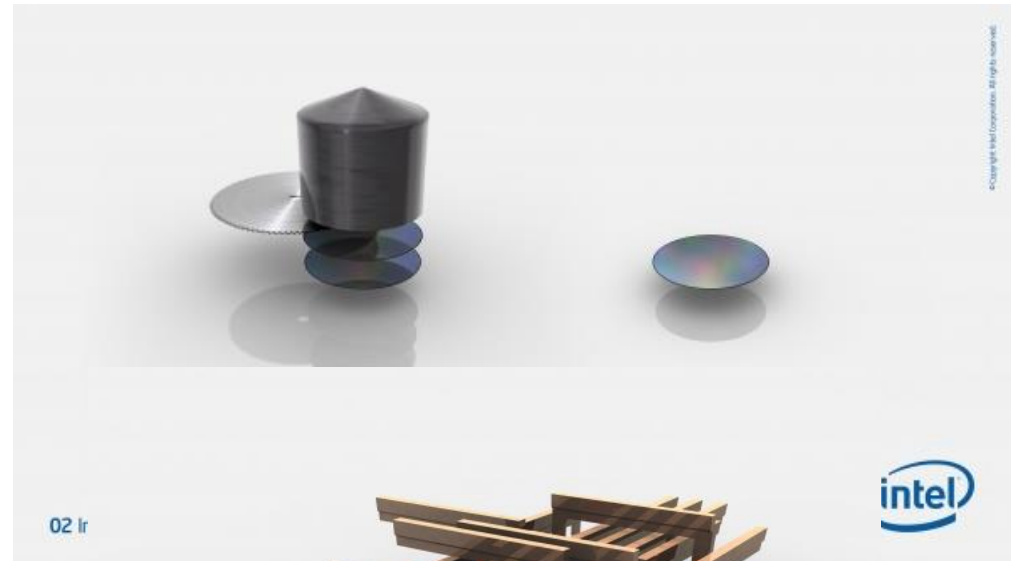


The integrated circuit

Intel Pentium IV



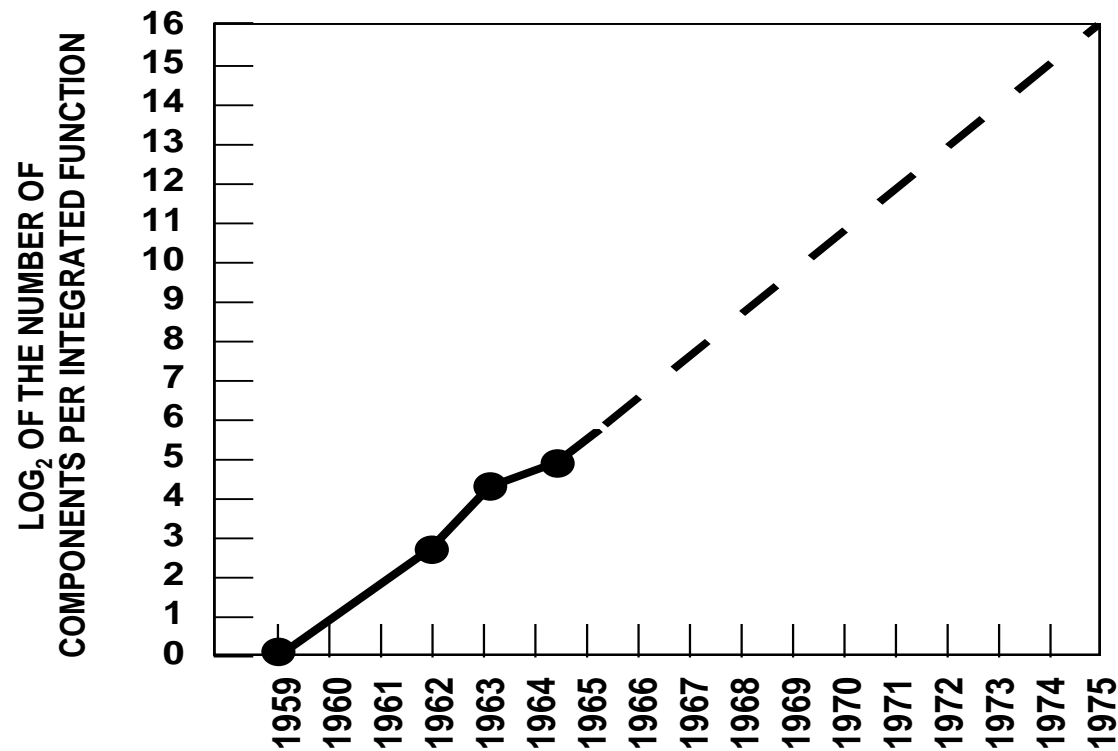
The integrated circuit



Moore's Law

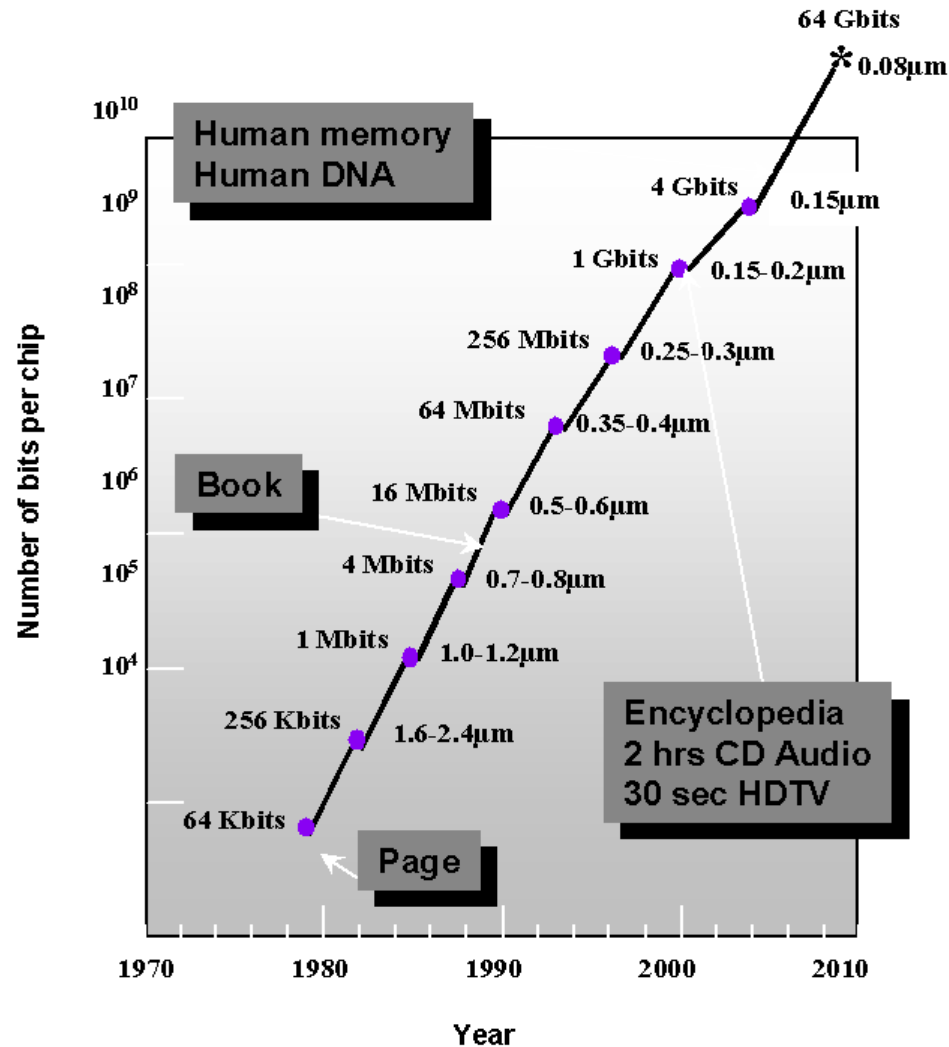
- In 1965, Gordon Moore noted that the number of transistors in an integrated circuit doubled every 18 to 24 months.
- He predicted semiconductor technology would double its capacity every 18 months.

Moore's Law

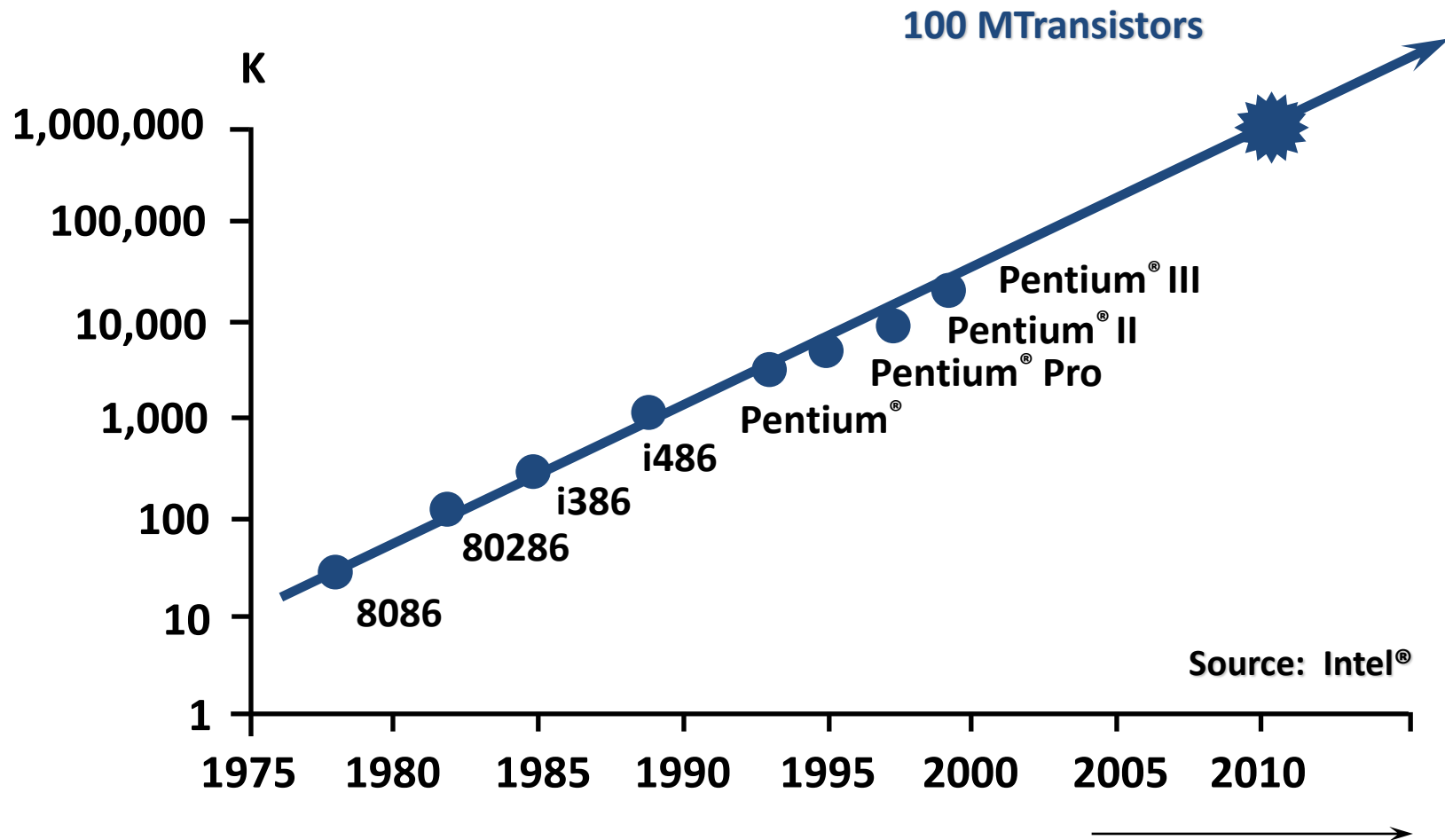


Electronics, April 19, 1965.

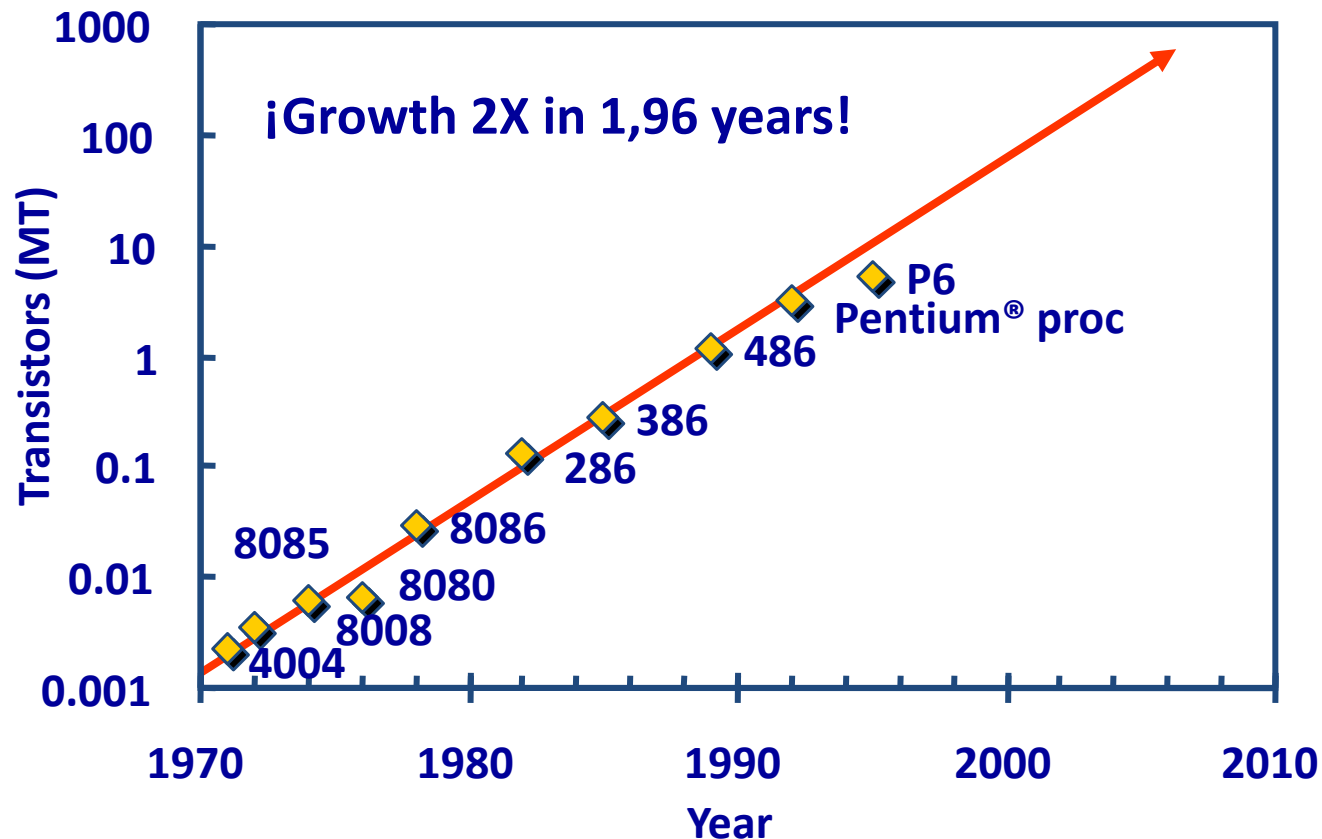
Evolution in complexity



Number of transistors per area unit



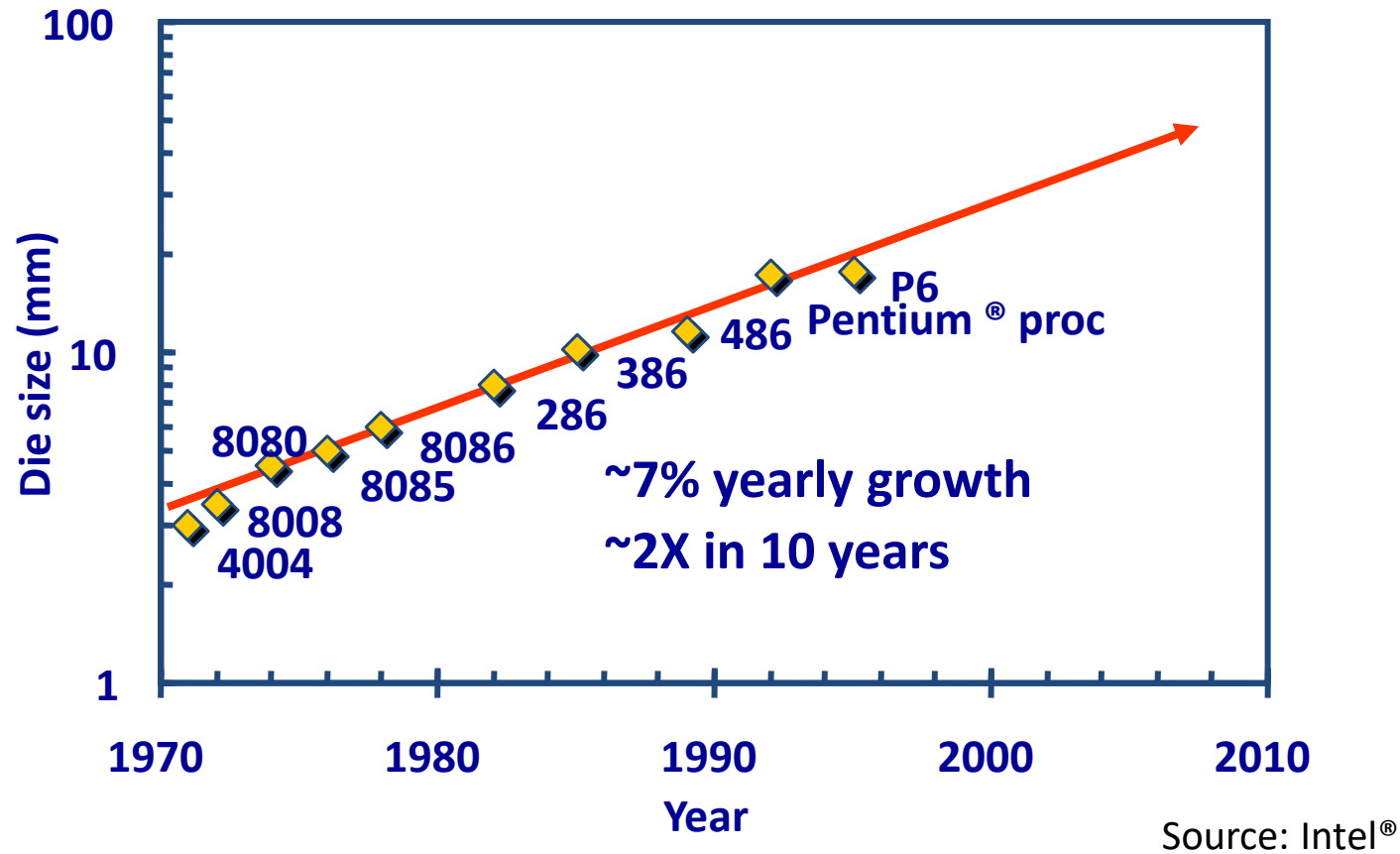
Moore's Law in Microprocessors



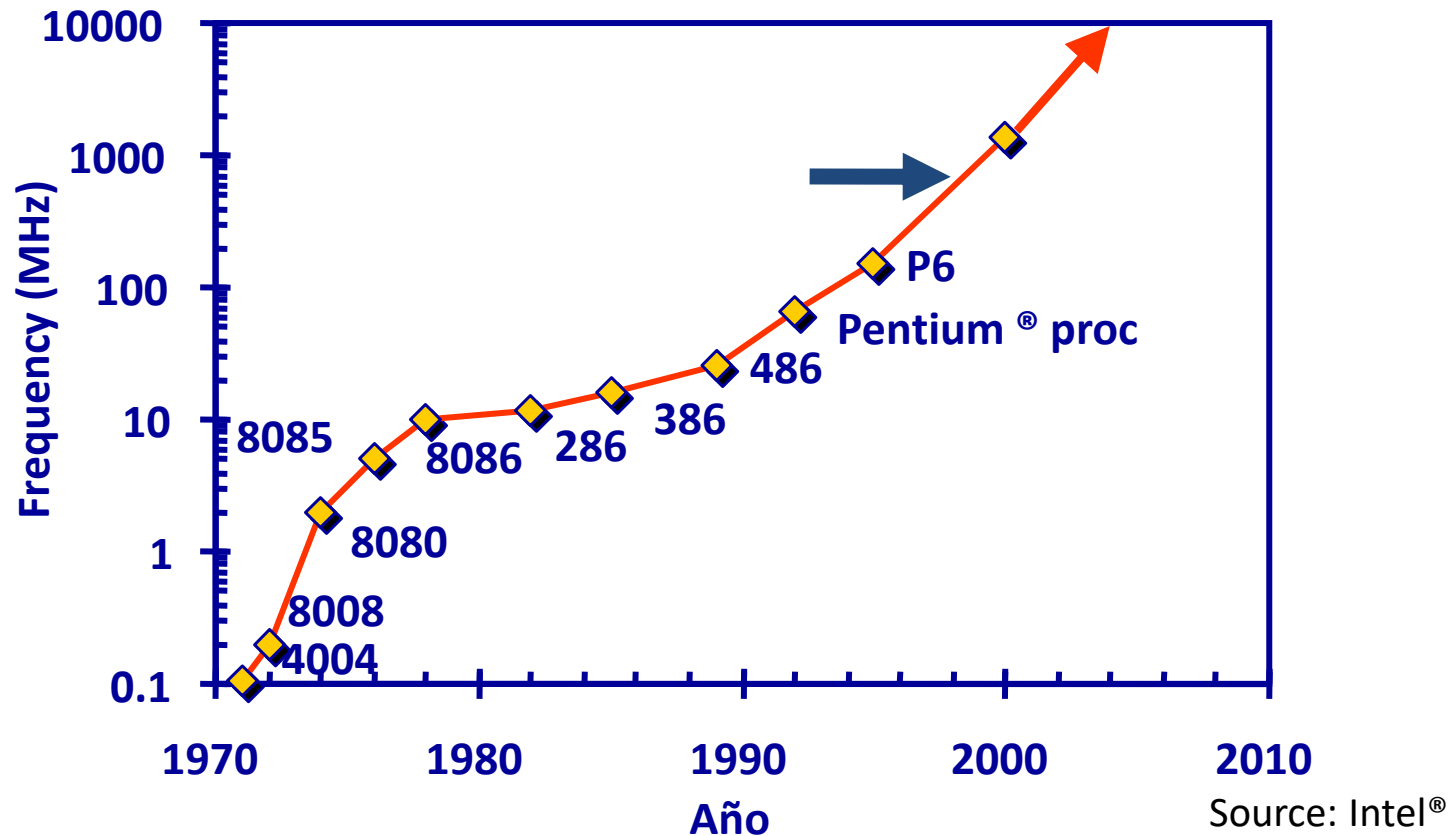
Source: Intel®

The number of transistors in state-of-the-art microprocessors doubles every 2 years

Die size growth

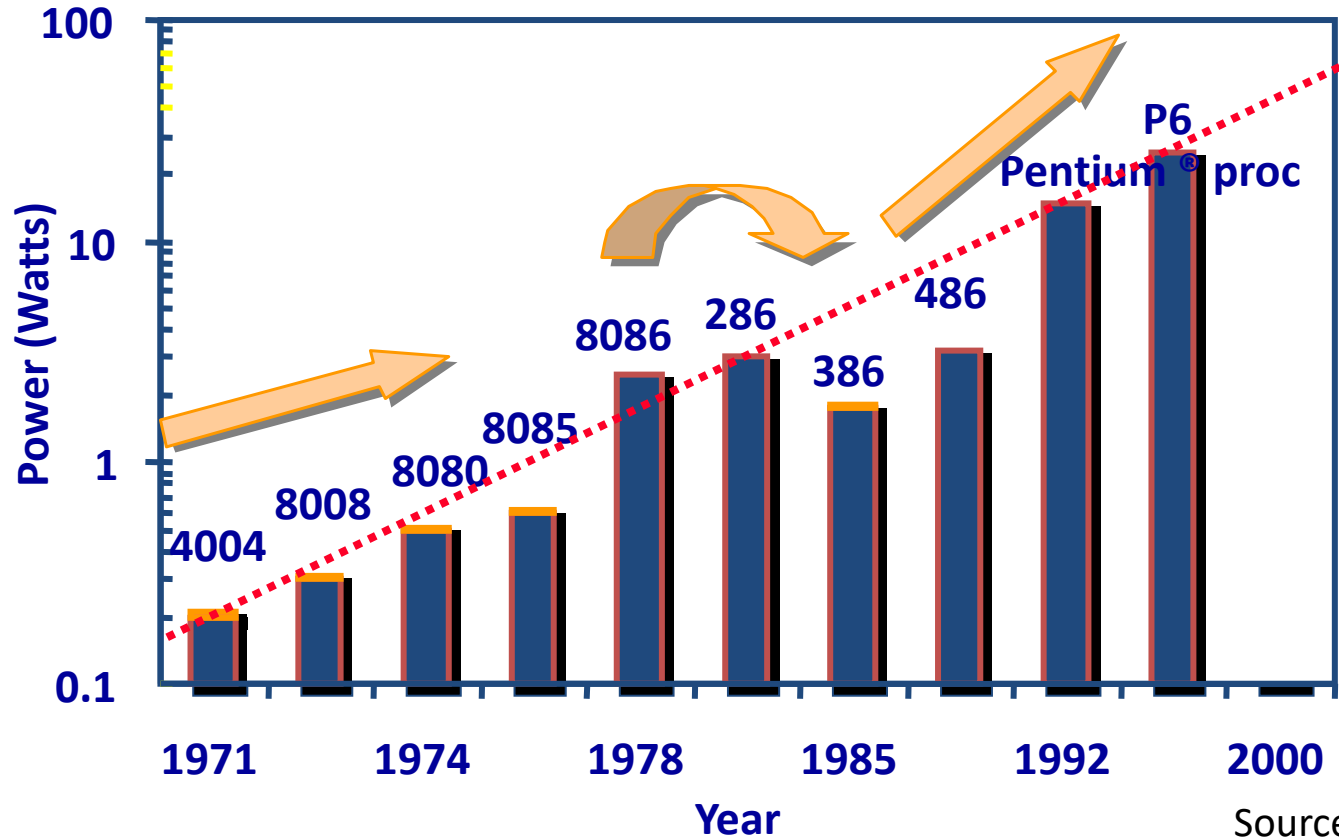


Frequency



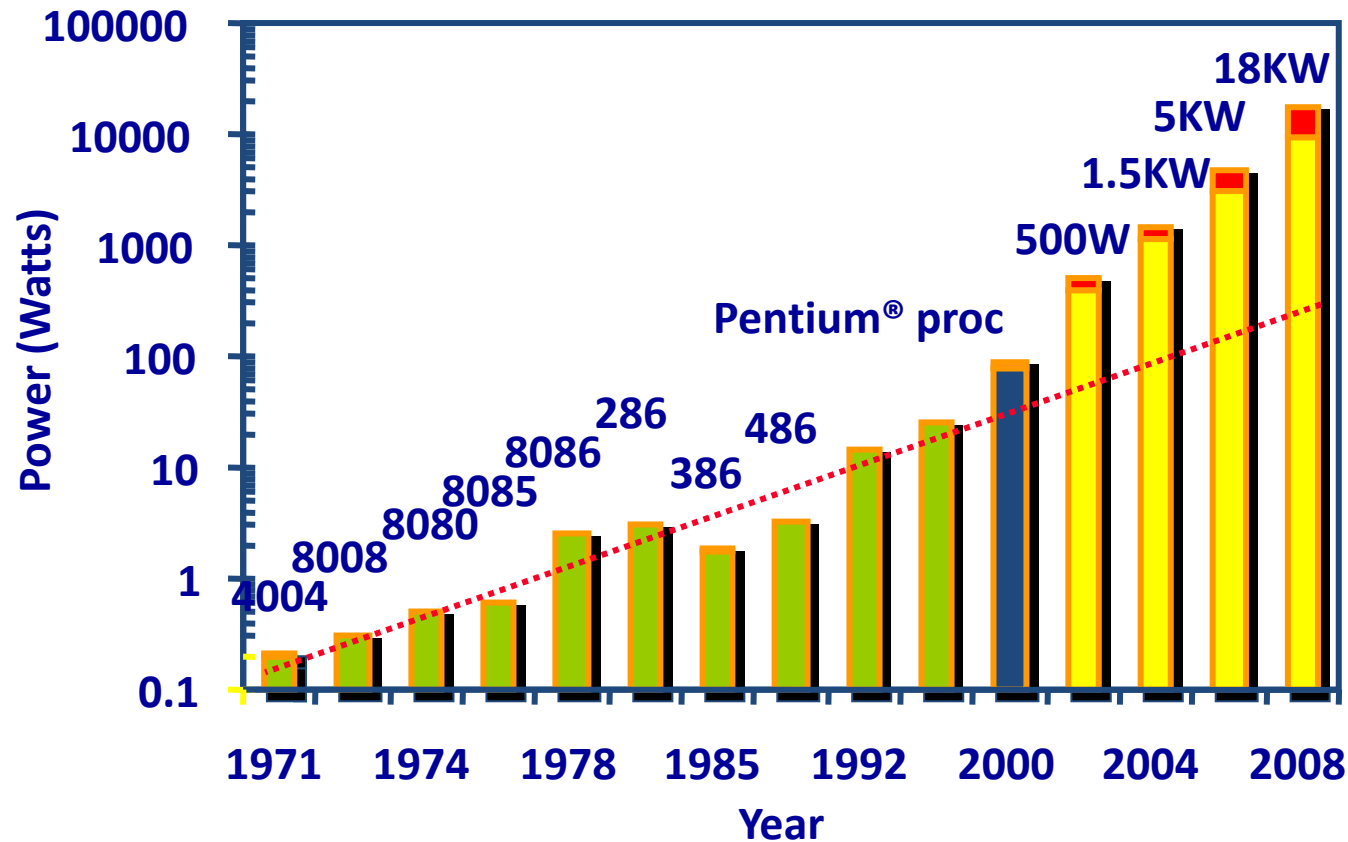
**The frequency of cutting-edge microprocessors
doubles every 2 years**

Power dissipation



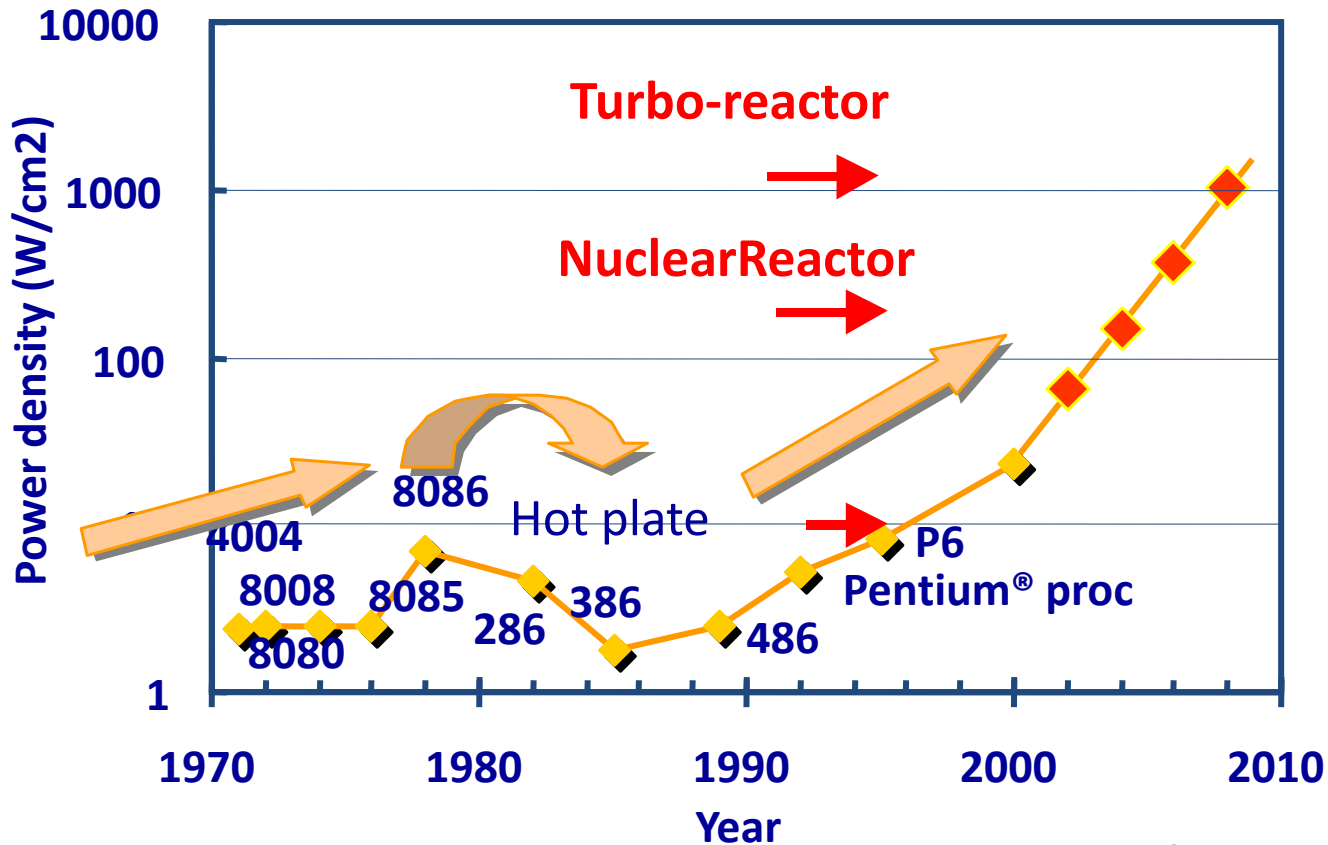
The power consumed continues to increase in the State-of-the-art microprocessors

The power could be a problem...



The distribution of power and its dissipation will be prohibitive...

Power density



Source: Intel®

The power density will be too high for
keeping joints at low temperature

Not only in microprocessors

Cellular phones

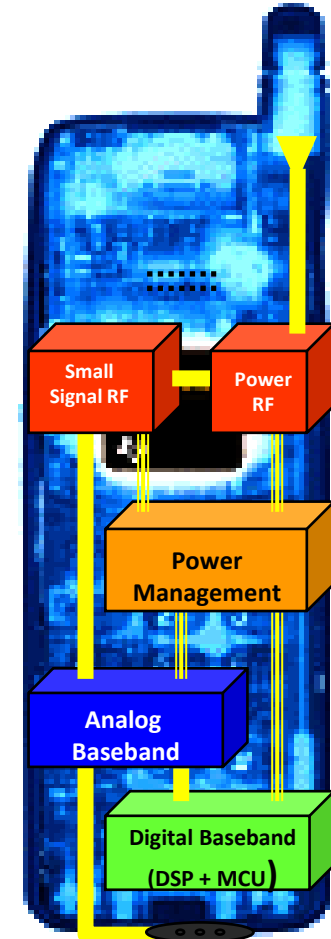


Mobile phone market
(Phones produced)

1996 1997 1998 1999 2000

Units **48M 86M 162M 260M 435M**

(Texas Instruments®)



Advantages of Integrated Circuits

- 😊 Size: Smaller
- 😊 Speed: very high
- 😊 PCB: $f < 100$ MHz
- 😊 FPGA: 500 MHz
- 😊 ASIC: $f < 3$ GHz
- 😊 Cost: depends on the number of units manufactured
- 😊 Initial cost: design and prototyping (100.000€)
- 😊 Cost per piece: 1-200€
- 😊 Cost-effective for large runs (>10,000 pieces/year)
- 😊 Reliability: high; more immune to noise
- 😊 Consumption: lower

Technological scaling

- Electronic technology has historically followed a surprisingly uniform pace
- Generation after generation, the limits have been pushed
- Oriented to market demands
- Lower costs (smaller size, lower cost)
- Increased performance
- Faster processing speed
- Increased data storage capacity
- And currently, nanotechnologies ... (22 nm)

Technologies

- COTS (Commercial Off-The-Shelf)
 - ❖ Components are cheaper because they are manufactured in volume, but they have to be assembled on board
 - ❖ Board size may be a limitation
 - ❖ On-board interconnect is slower
 - ❖ Consumption is higher
 - ❖ The reliability of a board is usually lower than that of the circuits that compose it

Technologies

- ASIC (Application Specific Integrated Circuit)
 - Allow to obtain all the advantages of integrated circuits
 - The cost of designing and manufacturing the prototype (non-recurring cost) is very high
 - The cost per unit is very low
 - Suitable solution for:
 - Very large production volumes
 - Requirements (performance, consumption, size, reliability, etc.) cannot be met by COTS

<https://www.youtube.com/watch?v=bor0qLifjz4>

<http://www.rtve.es/alacarta/videos/tres14/tres14-materias-primas/1306959/>

https://www.youtube.com/watch?v=cVNvJUYL_MM

<http://www.youtube.com/watch?v=YroylXq2Iz0&feature=related>

Technologies

- FPGA (Field-Programmable Gate Array)
 - Intermediate solution between COTS and ASIC
 - The manufacturing cost is eliminated, just programming
 - The cost per unit is higher than that of an ASIC
 - Today's FPGAs have a very wide range in sizes, features and prices
 - Up to 600K logical cells and registers and 22Mbit of internal RAM
 - Up to 550 MHz
 - From a few euros per piece
 - Suitable solution for:
 - Medium/high production volumes

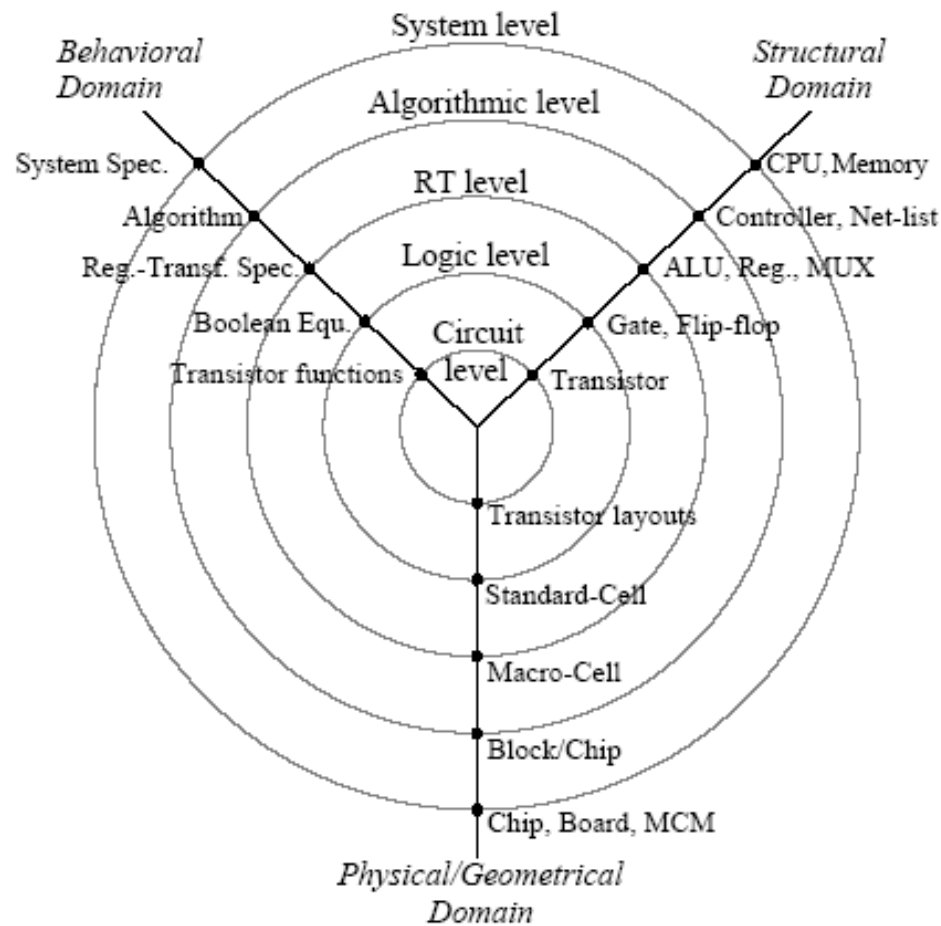
Technologies

- The enormous integration densities that can be achieved (currently around 1G transistor per IC) allow new solutions:
 - SoC (System on Chip): Complete system within a CI, including processor, memory, buses, peripherals
 - SoPC (System on a Programmable Chip): SoC implementado en una FPGA
 - MPSoC (MultiProcessor SoC): System with multiple processors within one IC
 -

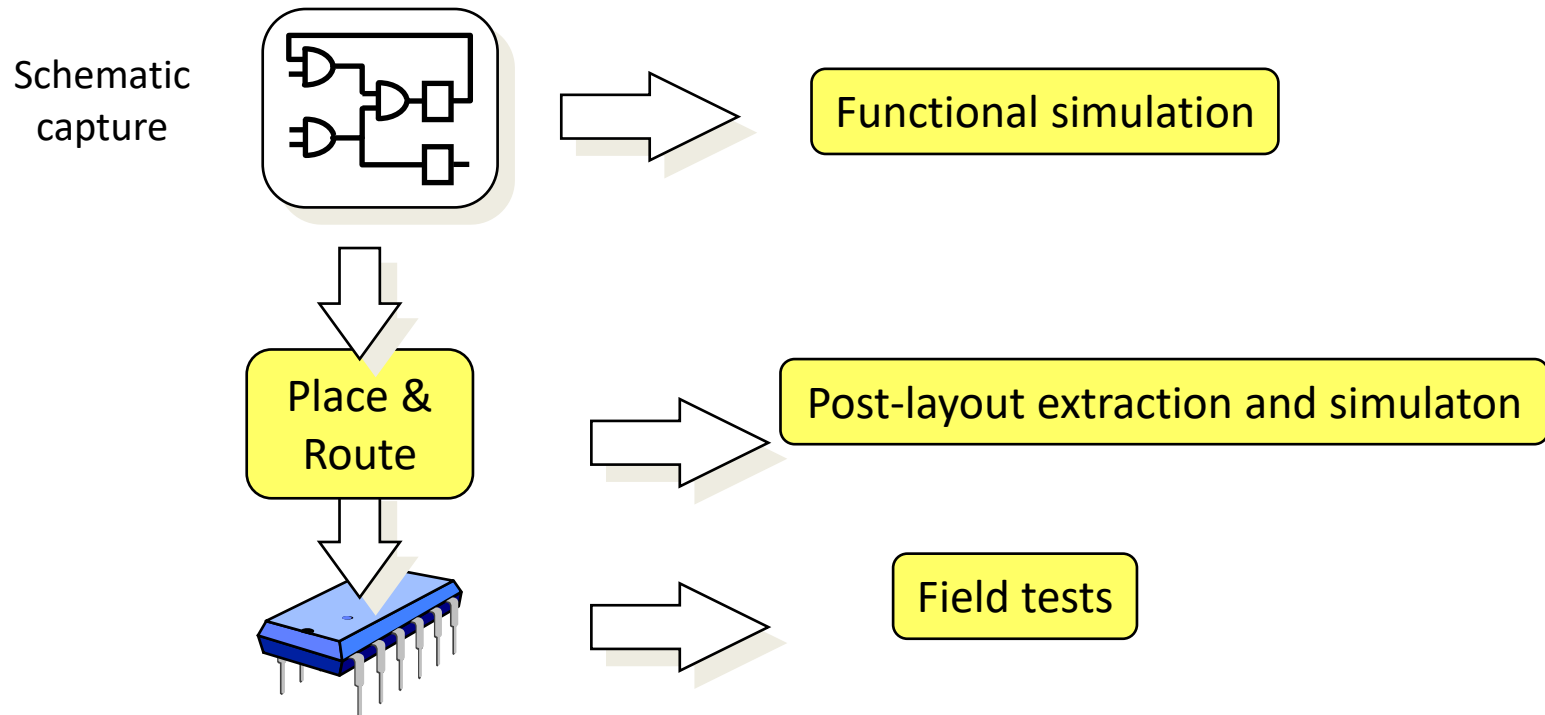
Introduction to Microelectronic Design

- Designing such complex integrated circuits is not feasible with conventional techniques
- Design methodology. Fundamental concepts:
 - Levels of abstraction: "divide and conquer"
 - Hardware Description Languages
 - CAD Tools
 - Synthesis
 - Simulation
 - Place & Route
 - Parameter extraction
 - IP (Intellectual Property)

Levels of abstraction: Y by Gajski

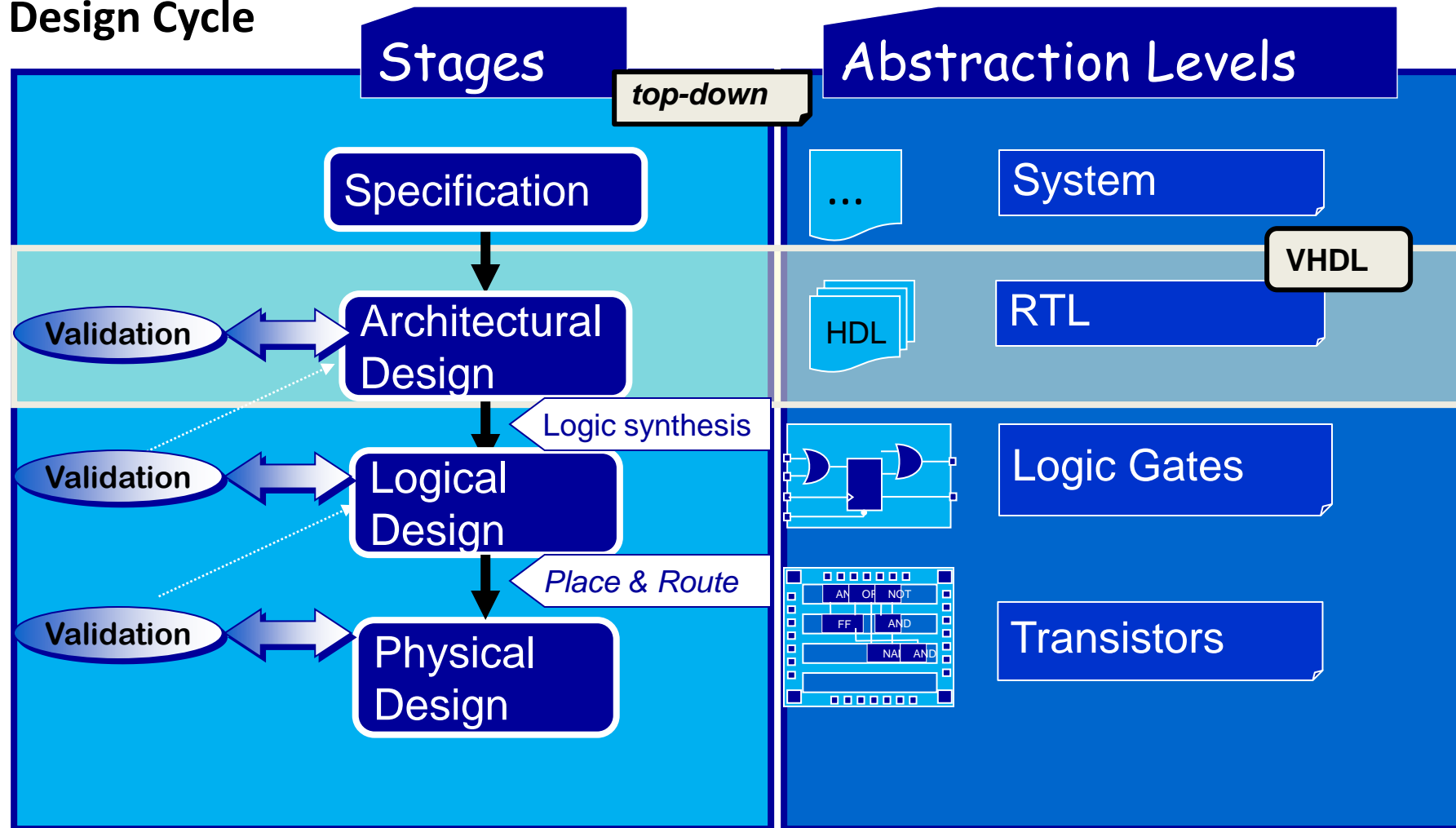


Conventional design methodology



Design methodology: digital circuits

Design Cycle



Simulation

- Simulation is used to validate designs



- Simulation is fundamental in an IC, since controllability and observability are very low!

Synthesis

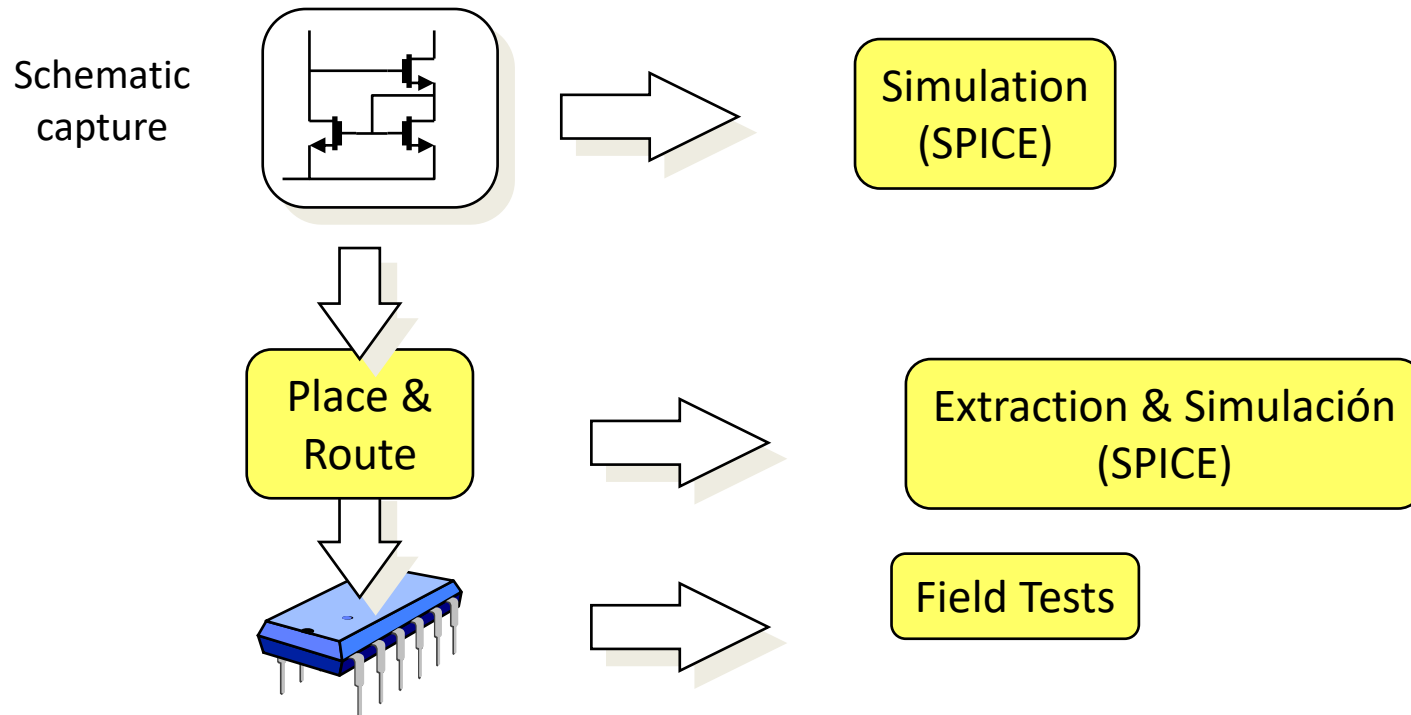
- synthesizers are used to automatically obtain the hardware corresponding to the model of a digital system



Design methodology: digital circuits

- Features
 - The elementary components (logic gates, flip-flops) can be modeled easily. The main difficulty is that a design consists of many (millions!) elementary components.
 - HDLs allow you to raise the level of abstraction (RT or algorithmic)
 - An adequate design methodology, supported by tools, allows complex designs to be carried out
- Objectives:
 - Area (size) -> Cost
 - Delays (Speed) -> Performance
 - Consumption
 - Reliability
 - Time to market!

Design methodology: analogue circuits



Design methodology: analogue circuits

- Features
 - Far fewer components (transistors, amplifiers, etc.) are used, but it is necessary to check very diverse characteristics
 - The simulation has to be done at a lower level of abstraction (electrical)
 - HDLs exist, but they only serve to simulate (there are no synthesis tools)
- Objectives:
 - The same as in digital circuits (area, consumption, etc.) and also
 - Linearity, bandwidth, gain, SNR, etc.

References

- Rabaey (Digital Integrated Circuits: A Design Perspective)