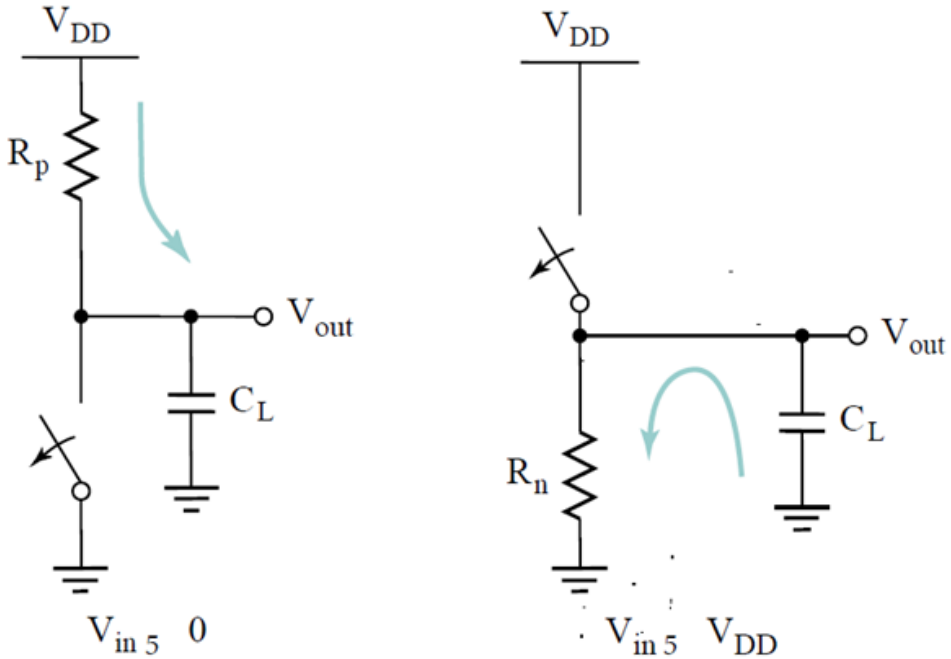
Design practical consideratios in Integrated Circuits

CMOS propagation time



$V_{out} = V_{DD}(1 - e^{-t/\tau})$

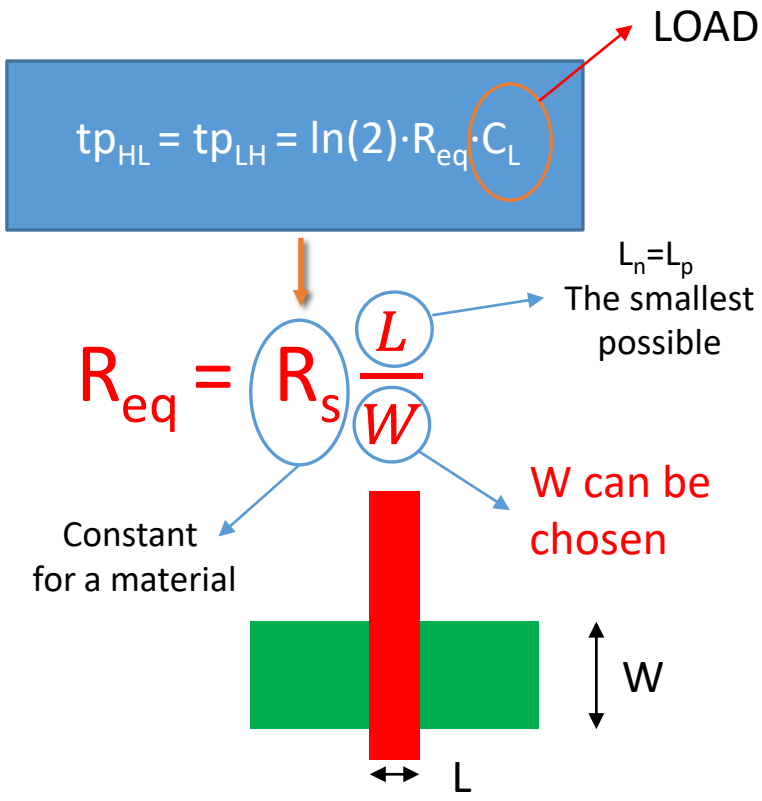
$V_{out} = V_{DD}e^{-t/\tau}$

t_P: $V_{out}(50\%) = \frac{V_{DD}}{2} = V_{DD}(1 - e^{-t_P/\tau})$

$\frac{1}{2} = e^{-t_P/\tau} \Rightarrow t_{PP} = ln2 \cdot \tau = ln2 \cdot R_P \cdot C_L$

Symmetric propagation times, by desing ¡¡¡¡

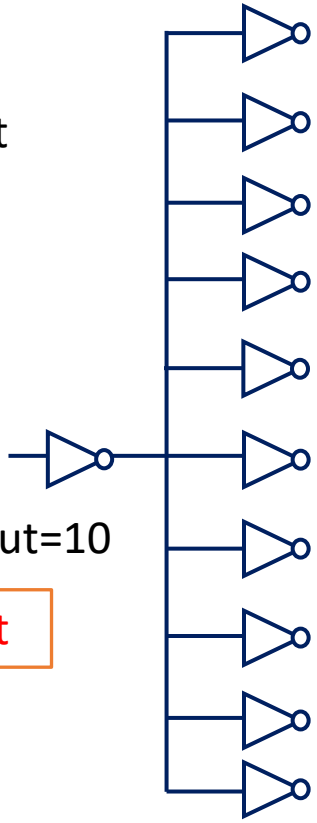
$t_{PN} = t_{PP} \Rightarrow \tau_P = \tau_P \Rightarrow R_P = R_N = R_{eq}$



CMOS propagation time (Load)

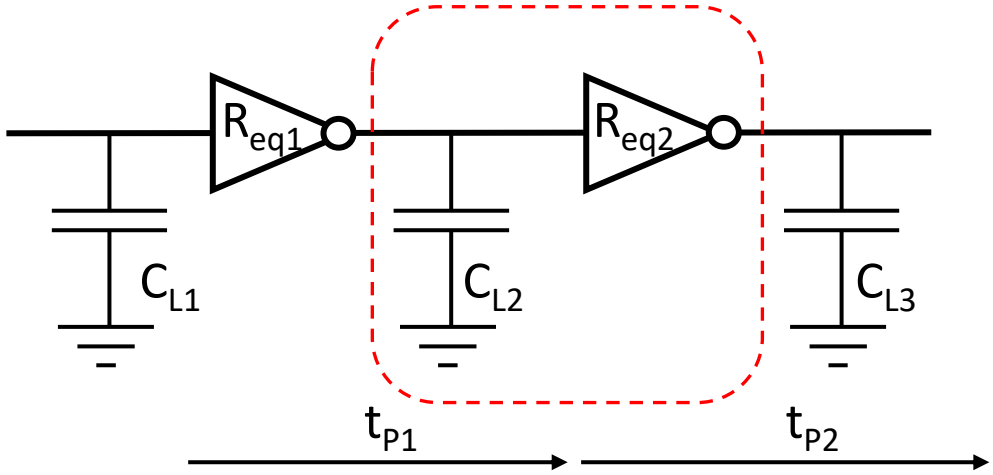
- Parasitic Capacitance
  - Transistor gate capacitance(Cg): $C_g = C_{ox} * W * L$

    C_{ox}: Capacitance per area unit
  - Interconexion capacitance:
    - Increase with Length
    - More important with small technologies



Fan-out is the number of load gates connected to the output

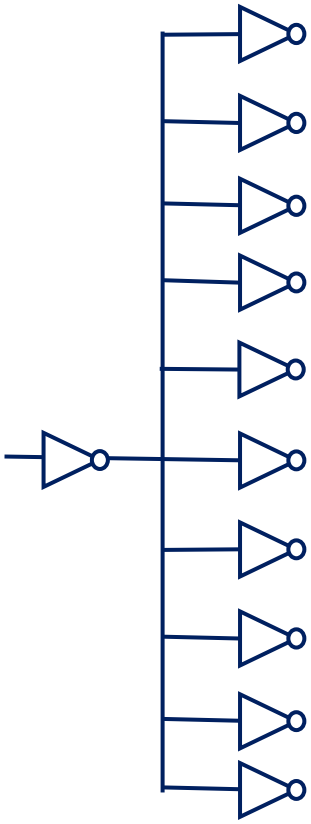
CMOS propagation time (Load)



- R_p, R_n (R_{eq}) are decreased by making transistors BIGGER
- C_L is decreased by making transistors SMALLER

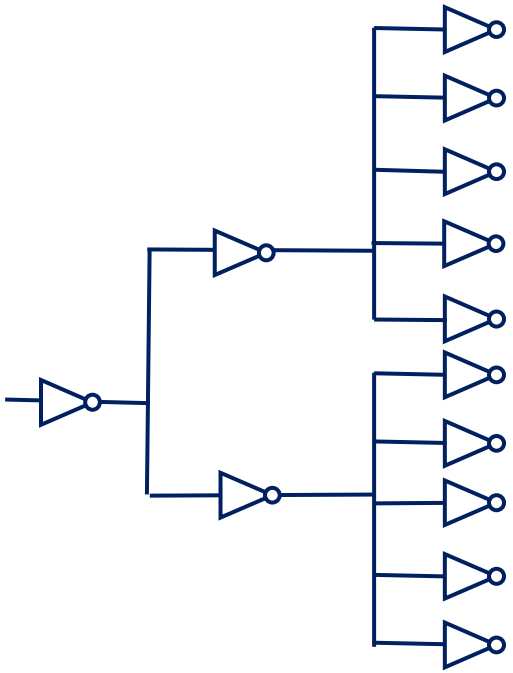
CMOS propagation time (Load)

- Delay due to high fanout



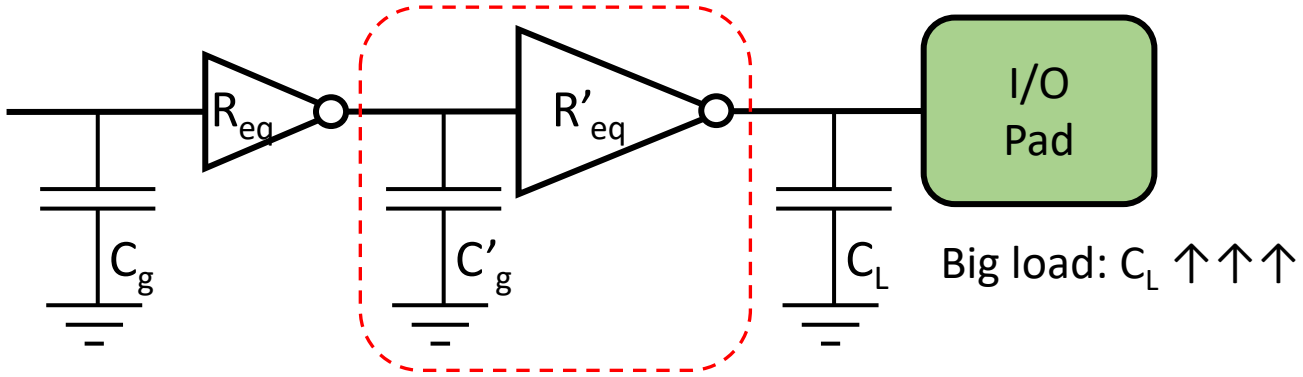
$t_p = 10 * t_{pi}$

t_{pi} = t_p of the minimum size inverter



$t_p = t_{pA} + t_{pB} = 2 * t_{pi} + 5 * t_{pi} = 7 * t_{pi}$

CMOS propagation time (Load)



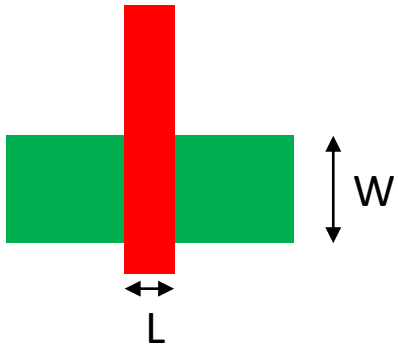
- Delay reduction in propagation time (t_p)

$$t_p = \ln(2) \cdot R_{eq} \cdot C_L$$

$$R_{eq} = R_s \frac{L}{W}$$

$$C_g = C_{ox} \cdot L \cdot W$$

- Increase channel width (W -> W'):



$W' = \Theta \cdot W \quad \Theta > 1 \quad W' \uparrow \quad R'_{eq} \downarrow \quad C'_g \uparrow$

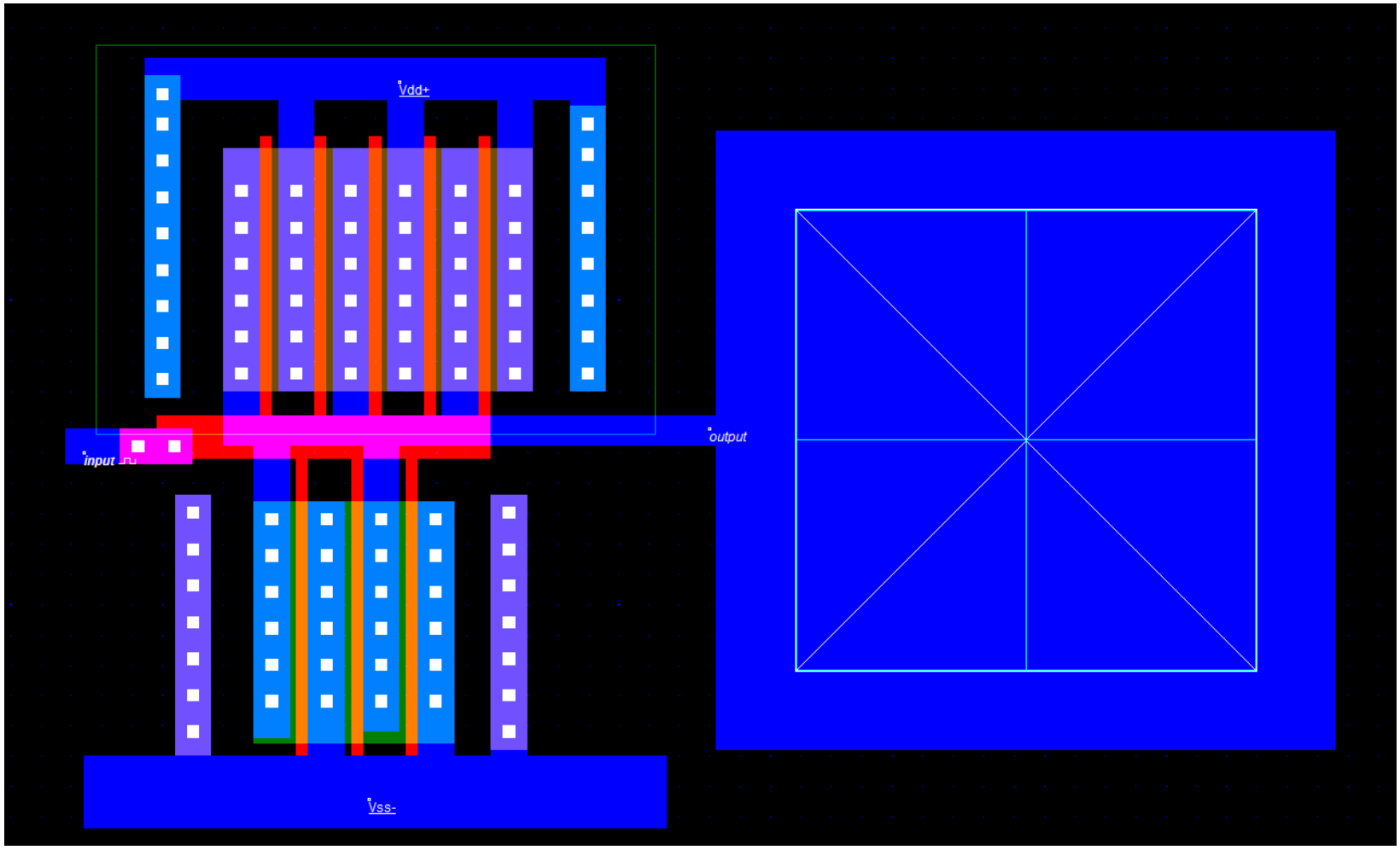
Bad: Area penalty

Good: Delay reduction

Move the delay to previous gate.
Good only if $C_L >> C_g$

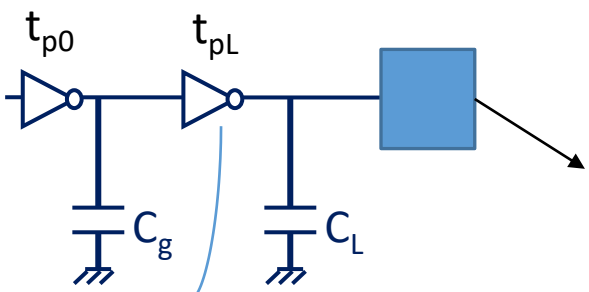
Tiempo de propagación CMOS

Indivisible Load: output pad

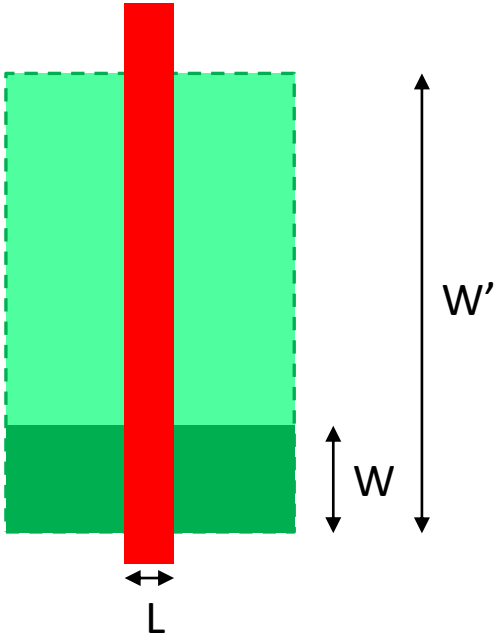


CMOS propagation time (Load)

- Indivisible Load (C_L)



Pad
(big $C_L \approx 1000 \cdot C_g$)



$t_p = t_{pi} + 1000 \cdot t_{pi} = 1001 \cdot t_{pi}$

Bigger transistors: 50 times bigger

$\Theta = 50 \Rightarrow W' = 50 \cdot W \Rightarrow R_{eq}' = R_{eq}/50 \Rightarrow t_{pL}' = t_{pL}/50 = 1000 \cdot t_{pi}/50 = 20 \cdot t_{pi}$

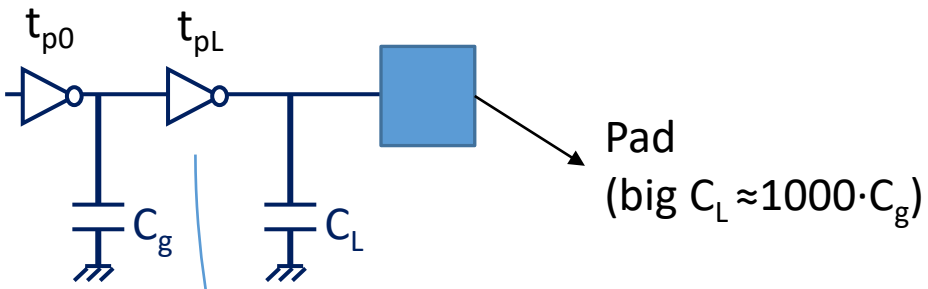
But:

$t_{p0}' = \Theta \cdot t_{p0} = 50 \cdot t_{pi}$

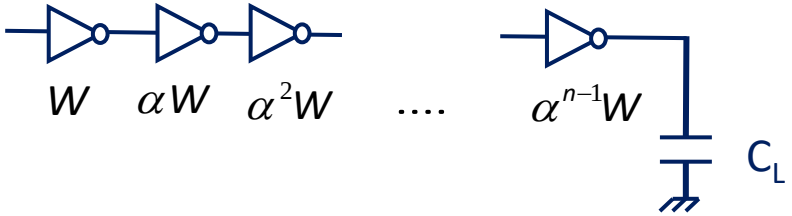
$70 \cdot t_{pi}$ instead of $1001 \cdot t_{pi}$

CMOS propagation time (Load)

- Indivisible Load (C_L)

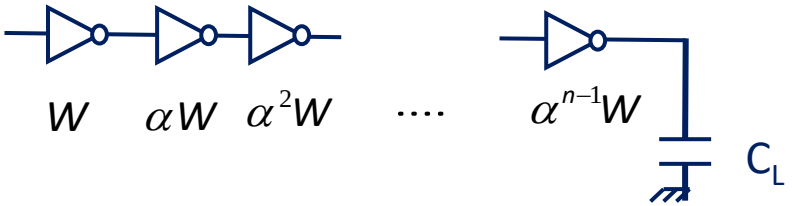


Best solution: several inverter stages with increasing size



CMOS propagation time (Load)

Best solution: several stages (n) with increasing sizes (α) so that: $C_L = \alpha^n C_g$



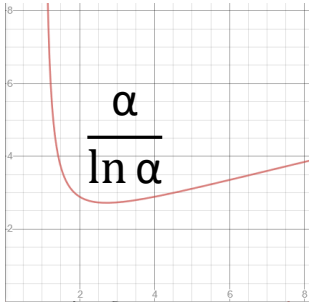
$$n = \frac{\ln\left(C_L/C_g\right)}{\ln \alpha} \qquad \alpha = \sqrt[n]{C_L/C_g}$$

1 stage delay:

$$t_{pk} = \ln(2) \cdot \frac{R_{eq}}{\alpha^k} \cdot \alpha^{k+1} \cdot C_g = \alpha \cdot \ln(2) \cdot Req \cdot C_g = \alpha \cdot t_{pi}$$

Total delay (n stages):

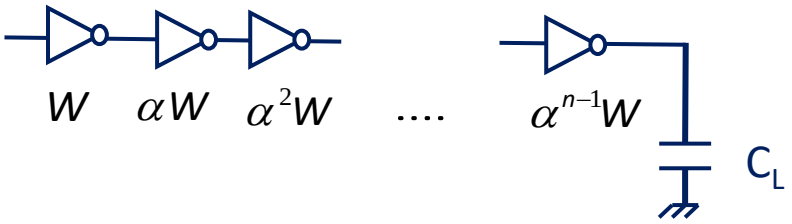
$$t_p = n \cdot \alpha \cdot t_{pi} = \frac{\ln\left(C_L/C_g\right)}{\ln \alpha} \cdot \alpha \cdot t_{pi} = t_{pi} \cdot \ln\left(C_L/C_g\right) \cdot \frac{\alpha}{\ln \alpha}$$



$$Minimum: \frac{dt_p}{d\alpha} = Cte \cdot \frac{\ln \alpha - 1}{(\ln \alpha)^2} = 0 \Rightarrow \boxed{\alpha = e \Rightarrow n = \ln\left(C_L/C_g\right)}$$

CMOS propagation time (Load)

Best solution:



Example: $C_L = 1000\ C_g$

$$n = \ln\frac{C_L}{Cg} = \ln 1000 = 6{,}9 \approx 7$$

Recalculate α:

$$\alpha = \sqrt[7]{1000} = 2{,}68$$

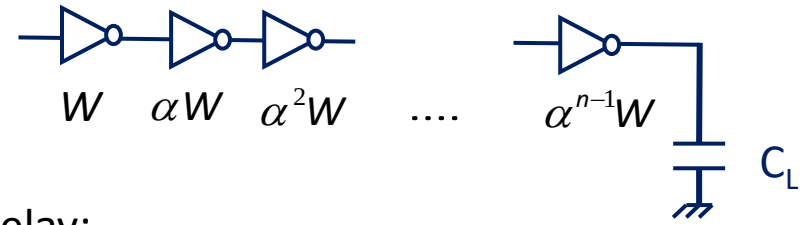
$t_{pi} = \ln(2)\cdot R_{eq}\cdot C_g$

$A_0 = L\cdot W$

Stage	1	2	3	4	5	6	7
Size	W	αW	α^2W	α^3W	α^4W	α^5W	α^6W
R	R_{eq}	R_{eq}/α	R_{eq}/α^2	R_{eq}/α^3	R_{eq}/α^4	R_{eq}/α^5	R_{eq}/α^6
C	αC_g	$\alpha^2 C_g$	$\alpha^3 C_g$	$\alpha^4 C_g$	$\alpha^5 C_g$	$\alpha^6 C_g$	$C_L=\alpha^7 C_g$
R·C	$\alpha R_{eq}C_g$	$\alpha R_{eq}C_g$	$\alpha R_{eq}C_g$	$\alpha R_{eq}C_g$	$\alpha R_{eq}C_g$	$\alpha R_{eq}C_g$	$\alpha R_{eq}C_g$
Area	A_0	αA_0	$\alpha^2 A_0$	$\alpha^3 A_0$	$\alpha^4 A_0$	$\alpha^5 A_0$	$\alpha^6 A_0$

CMOS propagation time (Load)

Best solution:



Example: $C_L = 1000\ C_g$

$$n = \ln\frac{C_L}{Cg} = \ln 1000 = 6{,}9 \approx 7$$

$$\alpha = \sqrt[7]{1000} = 2{,}68$$

Total delay:

$$t_p = \sum_{k=1}^{n} t_i = \sum_{k=0}^{n} (\ln(2)\cdot \alpha R_{eq} C_g) = \ln(2)\cdot R_{eq} C_g \cdot \alpha\cdot n = \alpha\cdot n\cdot tpi$$

$$t_p = \alpha\cdot n\cdot tpi = 2{,}68\cdot 7\cdot t_{pi} = \mathbf{18.7}\cdot t_{pi}$$

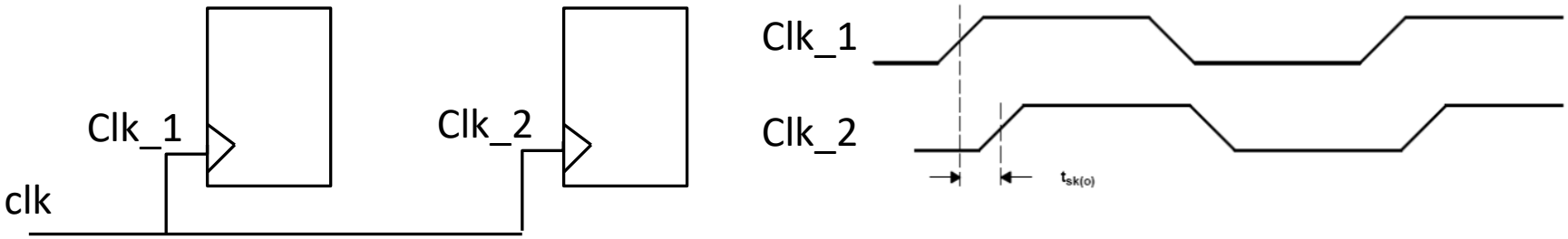
Total area:

$$A = \sum_{k=0}^{n-1} \alpha^k A_o = \frac{\alpha^n - 1}{\alpha - 1} Ao$$

$$A = \frac{\alpha^n - 1}{\alpha - 1} Ao = \frac{2.68^7 - 1}{2.68 - 1} Ao = \mathbf{590}\cdot Ao$$

Clock distribution

- Very high fanout
- Clock-skew: difference time clock arrival between flip-flops



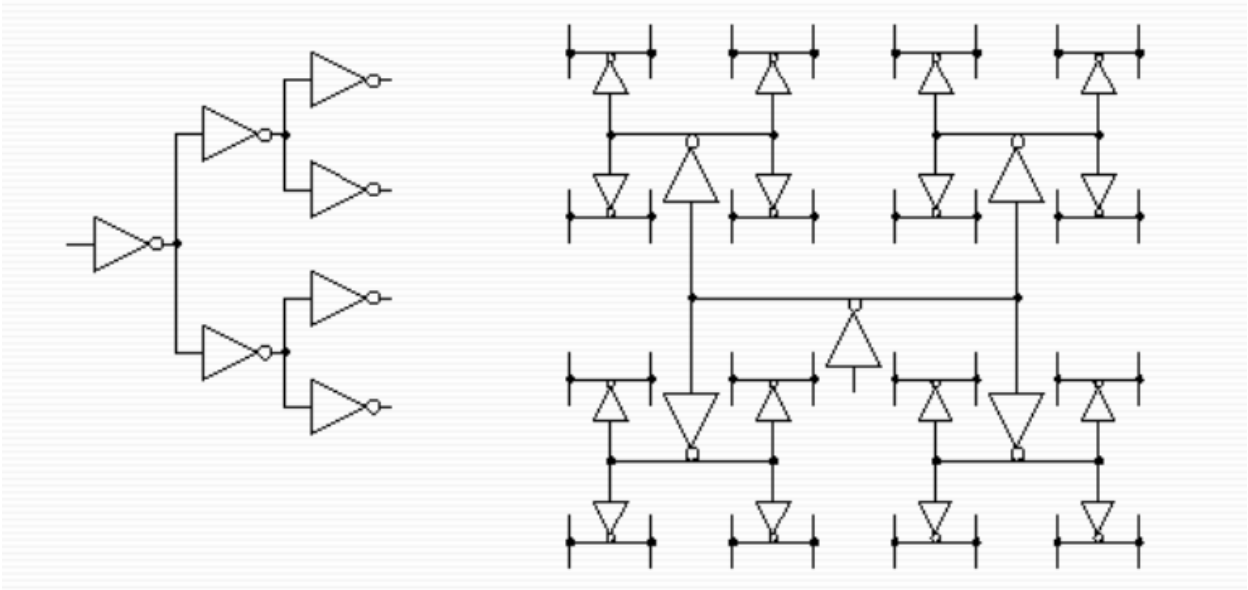
Solutions:

- Routing the clock in the opposite sense to combinational logic.
- Appropiate clock network: clock tree
- Clock buffers.
- Increase the width of the wires to reduce the resistance

Clock distribution

Solutions:

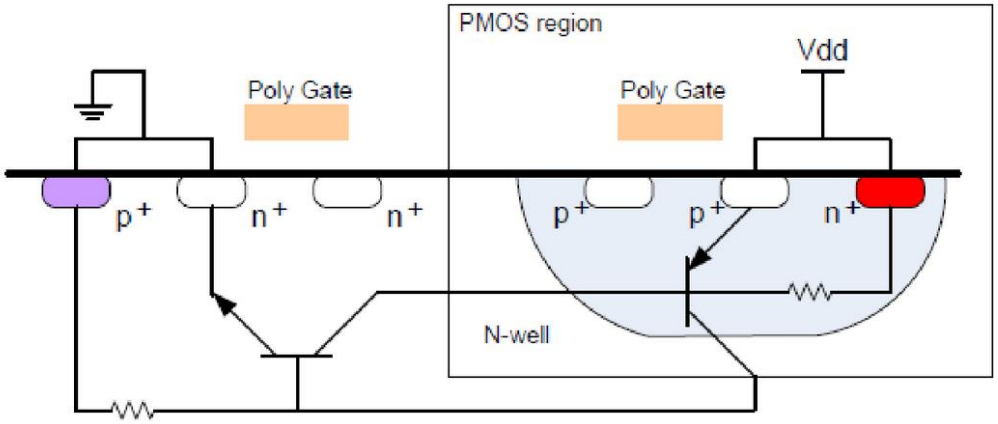
- Appropiate clock network: clock tree
- Clock buffers.

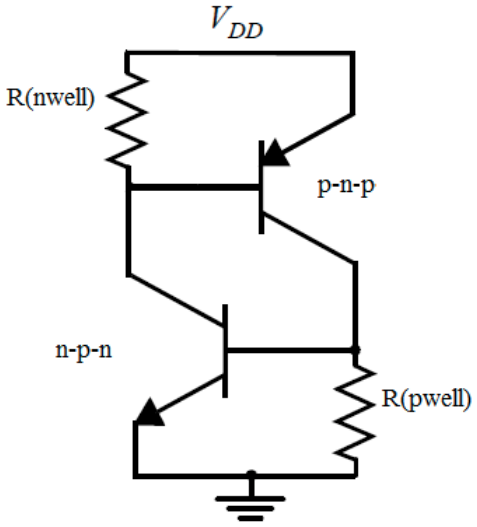


❖ Similar problems appear in the reset signal =>
solution: big buffer and increase the width of the wires.

Latch-up

A *latch-up* is a type of short circuit which can occur in an integrated circuit (IC).





Normal conditions

pnp no conducting

↓

No Voltage through R(nwell)

↓

pnp off

↓

No Voltage through R(pwell)

↓

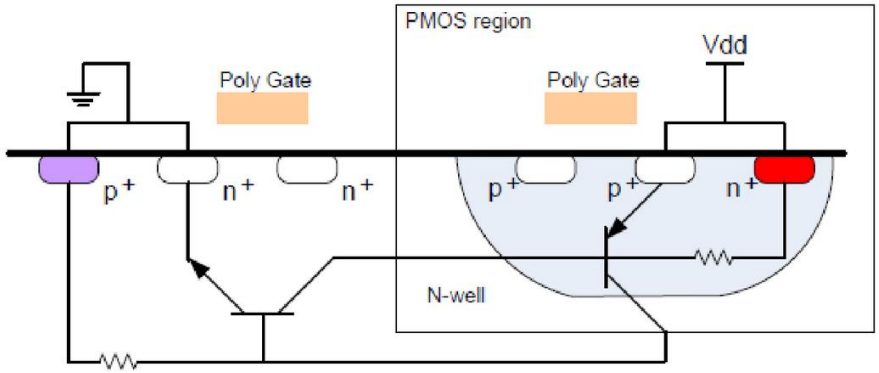
pnp off

Overpowering, radiation, particules

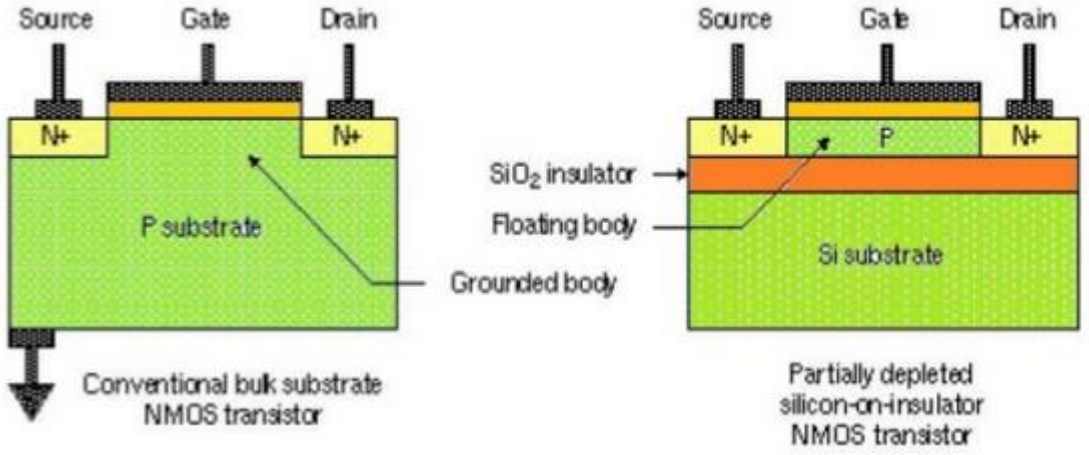
During a latch-up when one of the transistors is conducting, the other one begins conducting too. They both keep each other in saturation for as long as the structure is forward-biased and some current flows through it.

Latch-up

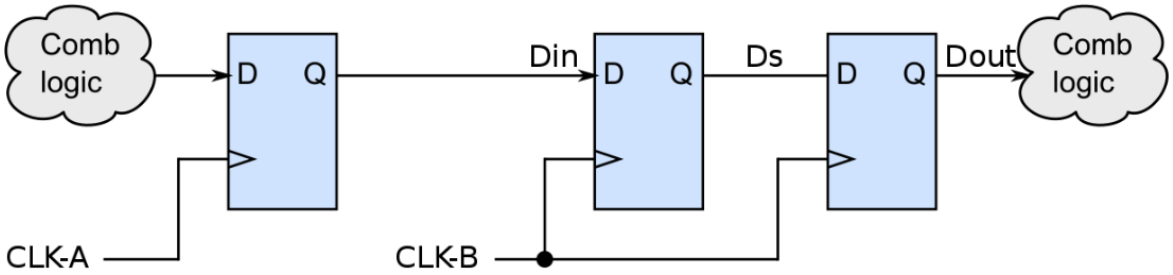
A *latch-up* is a type of short circuit which can occur in an integrated circuit (IC).

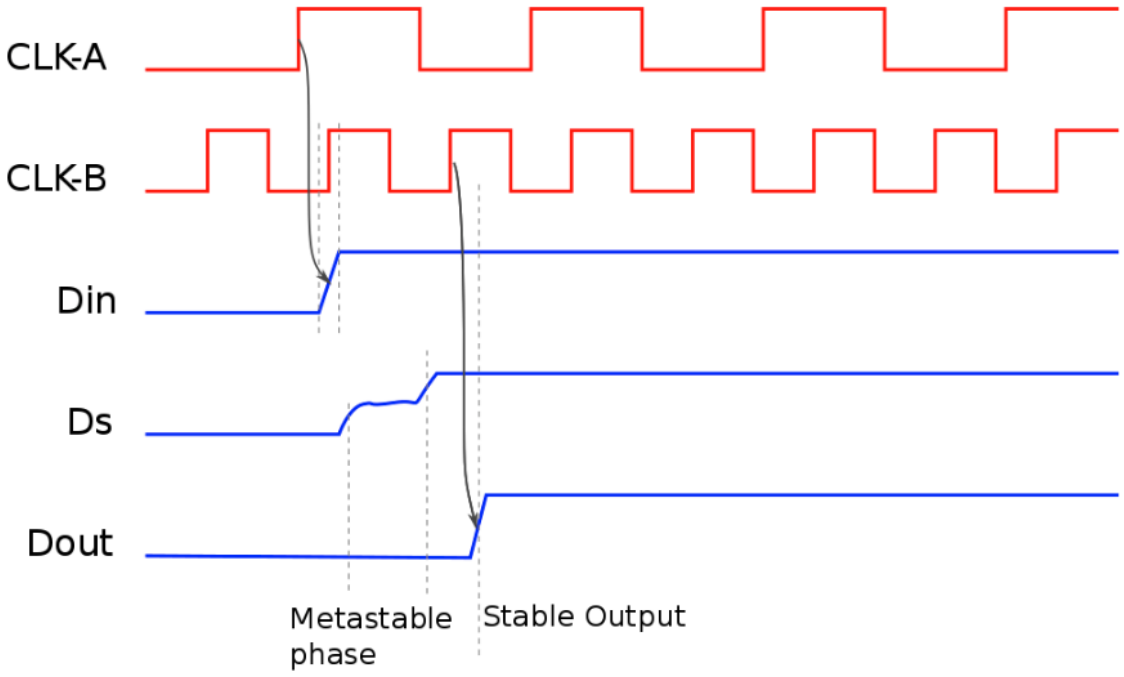


Solution: **Silicon on insulator** (**SOI**) technology.



Metastability





Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'.