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Zmod DAC 1411 AXI Adapter User Guide

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1 Introduction

This user guide describes the Digilent Zmod DAC 1411 AXI Adapter Intellectual Property. This IP provides the means to interface the Zmod DAC1411 Low Level Controller with an AXI based processing system. The Zmod DAC 1411 AXI Adapter provides a set of control registers that can be accessed by the processor over an AXI Lite interface, allows users to indirectly access the SPI configuration interface of the AD9717 featured by the Zmod DAC1411, implements a circular buffer used to store sample data and implements a bridge between the AXI Stream interface and the circular buffer. Sample data is meant to be loaded in the circular buffer through a DMA engine.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	AXI Lite, AXI Stream
Provided with core	
Design files	VHDL
Simulation model	-
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2019.1
Synthesis	Vivado Synthesis 2019.1

2 Features

- Allows control of the Zmod DAC 1411 through a set of control and status registers that can be accessed on the AXI Lite interface.
- Implements a 16Ksample circular buffer for each of the two channels of the Zmod DAC 1411.
- Provides an AXI Stream interface facilitating data transfer through a DMA engine.

3 Performance

The IP is designed to allow interfacing the ZmodDAC1411 Low Level Controller with an AXI based processing system. The sample data is defined by the processing system in system memory and moved by a DMA engine in the 16Ksample circular buffer implemented in BRAM memory. The circular buffer's output channels should be connected to the Low Level Controller's input data channels and can be read at a programmable rate between 100MSPS and 61.035KSPS. The SPI indirect access port (IAP) is meant to be used for configuration purposes only.

4 Overview

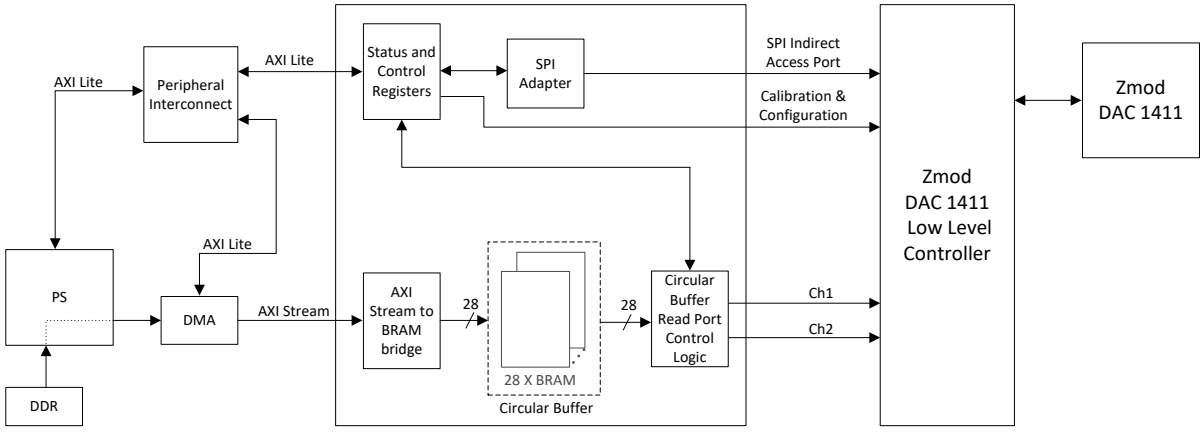

Figure 1. Zmod DAC 1411 Low Level Controller block diagram.

The structure of the IP is presented in Figure 1. The main functional blocks are the Register File, the Circular Buffer and the SPI Command Control block. The details of the hardware implementation are described in the sections below.

4.1 Register Space

The Zmod DAC1411 AXI Adapter register space is described in Table 1.

Address Space Offset	Register Name	Description
00h	CR	Control register
04h	SR	Status register
08h	IER	Interrupt enable register
0Ch	CMD_TX	Command Transmit register
10h	CMD_RX	Command Receive register
18h	AXIS_MM2S_LENGTH	AXI-Stream MM2S Transfer Length (Bytes)
1Ch	SCALE	Scale Control register
24h	SC1LGMULTCOEF	Channel1 low gain multiplicative calibration coefficient
28h	SC1LGADDCOEF	Channel1 low gain additive calibration coefficient
2Ch	SC1HGMULTCOEF	Channel1 high gain multiplicative calibration coefficient
30h	SC1HGADDCOEF	Channel1 high gain additive calibration coefficient
34h	SC2LGMULTCOEF	Channel2 low gain multiplicative calibration coefficient
38h	SC2LGADDCOEF	Channel2 low gain additive calibration coefficient
3Ch	SC2HGMULTCOEF	Channel2 high gain multiplicative calibration coefficient
40h	SC2HGADDCOEF	Channel2 high gain additive calibration coefficient

Table 1: General overview and detailed description of register space.

A detailed description of each individual register can be found in the subsections below.

4.1.1 Control Register (CR – offset 00h)

The main purpose of this register is to provide control over the IP in every aspect of its functionality.

31	30 5	5	4	3	2	1	0
RST	-	TEST_MODE	RUN_STP	INTR_EN	CMD_READ_EN	CMD_R/S	-

Bits	Field Name	Default Value	Access Type	Description
1	CMD_R/S	0	R/W	Setting this bit this will enable the SPI IAP interface to push out commands from the SPI transmit command FIFO. Cleared by the IP when the command sequence is transmitted successfully.
2	CMD_READ_EN	0	R/W	Setting this bit enables the SPI IAP to load received data in the SPI receive command FIFO.
3	INTR_EN	0	R/W	Interrupt enable bit.
4	DAC_EN	0	R/W	Setting this bit enables the Circular Buffer's output address counter and also configures the Zmod DAC 1411 output relay.
6	OUT_ADDR_CNT_RST	0	R/W	Setting this bit resets the Circular Buffer's output address counter.
29-16	DIV_RATE	0	R/W	The Circular Buffer's output counter frequency is divided by DIV_RATE.
31	RST	0	R/W	Resets all registers and state machines to their default values.

4.1.2 Status Register (SR – offset 04h)

The main purpose of this register is to provide status information over the IP in every aspect of its functionality.

31 21	21	20 17	16 10	9 3	2	1	0
-	BUF_FULL	CMD_TX_RX_ERROR	CMD_RX_COUNT	CMD_TX_COUNT	CMD_RUNNING	-	CMD_TX_DONE

Bits	Field Name	Default Value	Access Type	Description
0	CMD_TX_DONE	0	W1C	SPI command interface command sequence complete status bit.
2	CMD_RUNNING	0	R	Signals that the SPI command interface is not idle.
3-9	CMD_TX_COUNT	0h	R	Reports the number of bytes in the SPI command transmit FIFO.

10-16	CMD_RX_COUNT	0h	R	Reports the number of bytes in the SPI command receive FIFO.
17-20	CMD_TX_RX_ERROR	0	R/W	Reserved for error reporting.
21	BUF_FULL	0	W1C	The IP sets this bit once the circular buffer is full. The software can only clear this bit (the access type is write 1 to clear)

4.1.3 Interrupt enable register (IER – offset 08h)

Register to mask which status bits will be used as an interrupt

31 22	21	20 1	0
-	BUF_FULL	-	CMD_TX_DONE

Bits	Field Name	Default Value	Access Type	Description
0	CMD_TX_DONE	0	R/W	SPI command interface transaction complete interrupt enable mask bit
21	BUF_FULL	0	R/W	Buffer Full interrupt enable mask bit

4.1.4 Command Transmit register (CMD_TX – offset 0Ch)

Write accesses to this register will load SPI commands in the SPI command transmit FIFO.

31 24	23	22 21	20 12	11 8	7 0
-	Read/Write	Width	-	Address	Data

Bits	Field Name	Default Value	Access Type	Description
23	Read/Write	0	R/W	Write this bit to 1 for a read command and to 0 for a write command
22-21	Width	0h	R/W	Only 1 byte SPI transfers are supported. This field should be always 0h.
11-8	Address	0h	R/W	AD9717 SPI register address
7-0	Data	0h	R/W	Data byte to be sent to the AD9717. Ignored for read operations

4.1.5 Command Receive register (CMD_RX – offset 10h)

31 0
CMD_RX

Bits	Field Name	Default Value	Access Type	Description
0-31	CMD_RX	0	R	SPI command receive data. Reading this register will trigger a read operation on the SPI command receive FIFO and will decrement the CMD_RX_COUNT field in the Status Register.

4.1.6 AXI-Stream MM2S Transfer Length (AXIS_MM2S_LENGTH – offset 18h)

Number of bytes to be transferred on the data path using the AXI-Stream protocol.

31 26	25 0
-	AXIS_MM2S_LENGTH

Bits	Field Name	Default Value	Access Type	Description
0-25	LENGTH	0	R/W	Indicates the number of bytes to transfer for the MM2S channel.

4.1.7 SCALE register (SCALE– offset 18h)

DAC scale settings.

Bits	Field Name	Default Value	Access Type	Description
21	SC1_HG_LG	0	R/W	Scale select for channe1. 0 – Low gain 1 – High Gain
22	SC2_HG_LG	0	R/W	Scale select for channel2. 0 – Low gain 1 – High Gain

SC1LGMULTCOEF (Offset 24h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 low gain multiplicative coefficient
18-31	Reserved	0	R	Unused

SC1LGADDCOEF (Offset 28h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 low gain additive coefficient
18-31	Reserved	0	R	Unused

SC1HGMULTCOEF (Offset 2Ch)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 high gain multiplicative coefficient
18-31	Reserved	0	R	Unused

SC1HGADDCOEF (Offset30h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 high gain additive coefficient
18-31	Reserved	0	R	Unused

SC2LGMULTCOEF (Offset 34h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 low gain multiplicative coefficient
18-31	Reserved	0	R	Unused

SC2LGADDCOEF (Offset 38h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 low gain additive coefficient
18-31	Reserved	0	R	Unused

SC2HGMULTCOEF (Offset 3Ch)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 high gain multiplicative coefficient

18-31	Reserved	0	R	Unused

SC2HGADDCOEF (Offset 40h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 high gain additive coefficient
18-31	Reserved	0	R	Unused

4.2 Circular Buffer

The circular buffer's write port is controlled by the AXI Stream to BRAM bridge. When the AXI Stream's valid signal is in the logic high state, the circular buffer's wr_en signal will be asserted and the address counter will be incremented. The top value of the address counter is programmed through the MM2S_Length register and is limited at 2^{14}-1. The buffer's read port is enabled by the DAC_EN bit in the Control Register (CR) which also controls the Zmod DAC 1411's RL_EN_AWG signal. Thus, the Zmod's output will be in hugh impedance unless the circular buffer's read port is enabled. While the read port is enabled, the read address is incremented at a rate that can be programmed through the DIV_RATE field in the Control Register.

4.3 SPI Adapter

The SPI Adapter block is a bridge between the Register File and the Zmod DAC 1411 Low Level Controller's SPI indirect access port (IAP). Only 8 byte data transfers are currently supported on the SPI interface. The SPI commands are composed of a command word and a data byte which are passed through the CMD_TX Register. The format of the CMD_TX Register is illustrated in Figure 2.

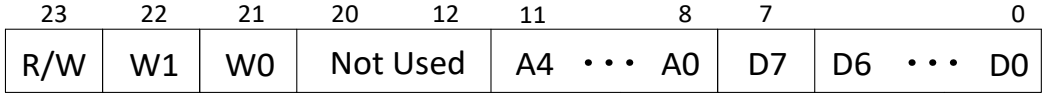

Figure 2: CMD_TX Format (Move to register description)

A write access to the CMD_TX Register on the AXI Lite interface will trigger the SPI Adapter block to load the SPI command in a transmit FIFO and will increment the transmit FIFO command count (CMD_TX_COUNT field in the Status Register). More SPI read and write commands can be queued in the transmit FIFO by successive write accesses to the CMD_TX register. Once all desired SPI commands are loaded in the transmit FIFO the CMD_R/S bit in the Control Register should be set. In response, the IP will assert the sSPI_EnTx port that will enable the Zmod DAC 1411 Low Level Controller to fetch commands from the transmit FIFO. The Zmod DAC 1411 Low Level Controller will decode the R/W bit in the command word and, in the case of a read command, it will load the data byte received on the SPI port in the SPI Adapter's receive FIFO also increasing the receive FIFO data counter (CMD_RX_COUNT field in the Status Register). The CMD_TX_COUNT field will be decremented for each SPI transaction signaled as successful by the Zmod DAC 1411 Low Level Controller. The CMD_DONE bit in the Status Register will be set on the

successful completion of the last command in the transmit FIFO. Read command data can be accessed from software by reading the CMD_RX register. Each read access of this register will assert the receive FIFO's read enable signal also decrementing the CMD_RX_COUNT field in the Status Register. The CMD_RX should only be accessed after the command sequence completion is signaled by the CMD_DONE flag.

4.4 Calibration

The Zmod DAC1411 calibration is not performed at the Zmod DAC 1411 AXI Adapter level. The multiplicative and additive calibration coefficients are computed in software based on parameters read from the Zmod's EEPROM memory and written to the configuration registers (addresses 24h-40h). The content of the configuration registers is exported as eight 18bit output ports(the configuration interface) to the Zmod DAC 1411 Low Level controller.

4.5 Clocking

The IP is divided in three clock domains:

1. The system clock domain (100MHz), which clocks the Circular Buffer read port, the command transmit FIFO read port and the command receive FIFO write port.
2. The AXI Stream clock that clocks the Circular Buffer write port and the Axi Stream to BRAM bridge.
3. The AXI Lite clock that clocks the Register File.

5 Port description

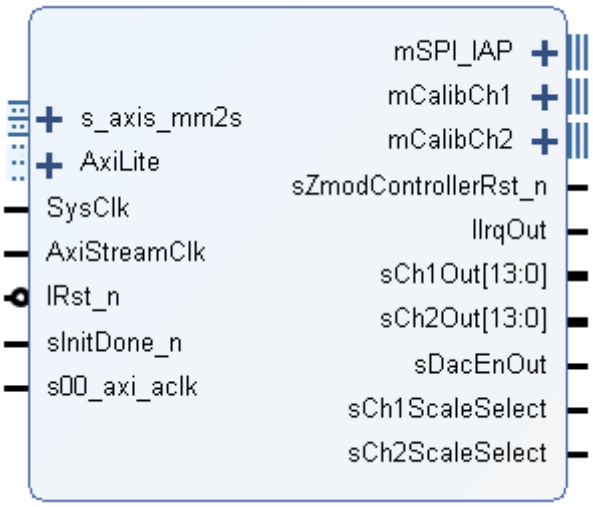

Figure 3: : Zmod DAC 1411 AXI Adapter IP

Signal Name	Interface	Signal Type	Init State	Description
SysClk	-	I	N/A	100MHz input clock signal.
AxiStreamClk	S2MM	I	N/A	Input clock associated with the S2MM AXI Stream interface

lRst_n	-	I	N/A	Synchronous reset of negative polarity.
sZmodControllerRst_n	-	O	N/A	Active low reset output synchronized in the SysClk clock domain. Asserted when the external reset signal (lRst_n) is asserted or when a software reset occurs.
sInitDone_n	-	I	N/A	Active low flag indicating when the Zmod Low Level Controller initialization is complete.
sSync	-	O	N/A	Signal used to synchronize multiple AD9648 devices. For more details see [3] (Zmod DAC 1411 Low Level Controller)
lIrqOut	-	O	N/A	Interrupt output (Level).
sCh1In[13:0]	-	I	N/A	14 bit output data channel 1 (connect to Zmod DAC 1411 Low Level Controller channel 1 input).
sCh1In[13:0]	-	I	N/A	14 bit output data channel 2 (connect to Zmod DAC 1411 Low Level Controller channel 2 input).
sCh1LgMultCoef	-	O	N/A	Channel1 low gain multiplicative coefficient output port.
sCh1LgAddCoef	-	O	N/A	Channel1 low gain additive coefficient output port.
sCh1HgMultCoef	-	O	N/A	Channel1 high gain multiplicative coefficient output port.
sCh1HgAddCoef	-	O	N/A	Channel1 high gain additive coefficient output port.
sCh2LgMultCoef	-	O	N/A	Channel2 low gain multiplicative coefficient output port.
sCh2LgAddCoef	-	O	N/A	Channel2 low gain additive coefficient output port.
sCh2HgMultCoef	-	O	N/A	Channel2 high gain multiplicative coefficient output port.
sCh2HgAddCoef	-	O	N/A	Channel2 high gain additive coefficient output port.
sCh1ScaleSelect	-	O	N/A	Channel1 scale select output port. • 1 = High Gain. • 0 = Low Gain.
sCh2ScaleSelect	-	O	N/A	Channel2 scale select output port. • 1 = High Gain. • 0 = Low Gain.
sExtSPI_Idle	-	I	N/A	Flag indicating that the Low Level Controller configuration state machine is in the IDLE state.
sCmdDone	-	I	N/A	Pulse indicating that the SPI command has been successfully completed.
sSPI_TxRdEn	-	I	N/A	Read enable signal used to load data from the transmit command FIFO.
sSPI_TxDout[23:0]	-	O	N/A	Transmit command FIFO output data containing the transfer length, the register address and the register data that are passed to the SPI controller.
sSPI_TxValid	-	O	N/A	Transmit command FIFO data valid signal.

sSPI_RxWrEn	-	I	N/A	Receive command FIFO write enable signal.
sSPI_RxDin[7:0]	-	I	N/A	Receive command FIFO input data.
AXI4 Lite Interface Signals				
AXI_LITE*		Input / Output		AXI4 Lite interface used to communicate with the control and status registers
AXI4 Stream Interface Signals				
MM2S*		Input		AXI4 Stream interface – connect to a DMA engine to transfer data from system memory to the IP's Circular Buffer

6 Designing with the core

6.1 Constraints

The IP does not constrain the clocks it requires as inputs, therefore clocks need to be constrained in the top-level design either manually or by relying on the auto-derived constraints, if using clock modifying blocks. For more information see [4]. No other constraints are required.

7 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.4, May 13, 2014.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Analog Devices, AD9717 Datasheet, Rev B.
4. Xilinx Inc., UG903: Using Constraints, v2014.3, October 31, 2014