

Zmod ADC 1410 AXI Adapter User Guide

Revised March 17, 2020; Author Tudor Gherman

1 Introduction

This user guide describes the Digilent Zmod ADC 1410 AXI Adapter Intellectual Property. This IP provides the means to interface the Zmod ADC1410 Low Level Controller with an AXI based processing system. The Zmod ADC 1410 AXI Adapter provides a set of control registers that can be accessed by the processor over an AXI Lite interface, allows users to indirectly access the SPI configuration interface of the AD9648 featured by the Zmod ADC1410, implements a basic trigger system that allows acquiring data in a circular buffer and implements a bridge between the circular buffer and an AXI Stream interface that enables connecting the IP core to a DMA engine.

2 Features

- Allows control of the Zmod ADC 1410 through a set of control and status registers that can be accessed on the AXI Lite interface.
- Provides a basic trigger mechanism for acquiring data from the Zmod ADC 1410.
- Implements a 16Ksample circular buffer for each of the two channels of the Zmod ADC 1410.
- Provides an AXI Stream interface facilitating data transfer through a DMA engine.

3 Performance

The IP is designed to allow interfacing the ZmodADC1410 Low Level Controller with an AXI based processing system. The Zmod ADC 1410 Low Level Controller's two output 100MSPS data channels are loaded into to a 16Ksample circular buffer implemented in BRAM memory. The circular buffer's output is converted into an Axi Stream format and it is designed to be connected to a DMA engine that will move buffer's content to system memory. A basic trigger functionality is provided that enables user to select channel 1 or channel 2 as the trigger source, allows selecting the trigger edge type (rising/ falling) and the trigger position in the captured window. The trigger functionality can be disabled by selecting the None trigger mode. The circular buffer can not be written to and read from at the same time.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	AXI Lite, AXI Stream
Provided with core	
Design files	VHDL
Simulation model	-
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2019.1
Synthesis	Vivado Synthesis 2019.1

4 Overview

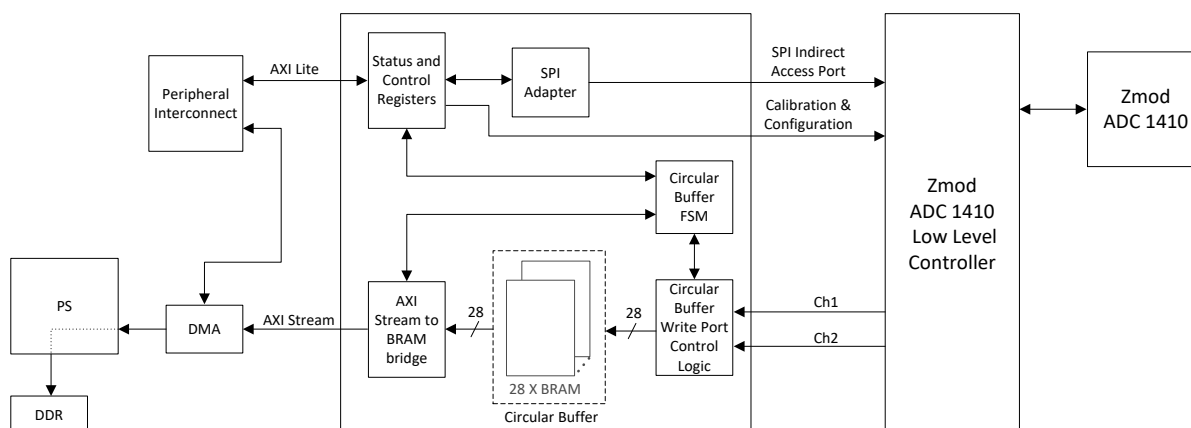


Figure 1. Zmod ADC 1410 Low Level Controller block diagram.

The structure of the IP is presented in Figure 1. The main functional blocks are the Register File, the Circular Buffer and the SPI Command Control block. The details of the hardware implementation are described in the sections below.

4.1 Register Space

The Zmod ADC 1410 AXI Adapter register space is described in Table 1.

Address Space Offset	Register Name	Description
00h	CR	Control register
04h	SR	Status register
08h	IER	Interrupt enable register
0Ch	CMD_TX	Command Transmit register
10h	CMD_RX	Command Receive register
14h	AXIS_S2MM_LENGTH	AXI-Stream S2MM Transfer Length (Bytes)
1Ch	TRIG	Trigger Control register
20h	WINDOW	Window register
24h	SC1LGMULTCOEF	Channel1 low gain multiplicative calibration coefficient
28h	SC1LGADDCOEF	Channel1 low gain additive calibration coefficient
2Ch	SC1HGMULTCOEF	Channel1 high gain multiplicative calibration coefficient
30h	SC1HGADDCOEF	Channel1 high gain additive calibration coefficient
34h	SC2LGMULTCOEF	Channel2 low gain multiplicative calibration coefficient
38h	SC2LGADDCOEF	Channel2 low gain additive calibration coefficient
3Ch	SC2HGMULTCOEF	Channel2 high gain multiplicative calibration coefficient
40h	SC2HGADDCOEF	Channel2 high gain additive calibration coefficient

Table 1: General overview and detailed description of register space.

A detailed description of each individual register can be found in the subsections below.

4.1.1 Control Register (CR—offset 00h)

The main purpose of this register is to provide control over the IP in every aspect of its functionality.

31	30	5	5	4	3	2	1	0
RST	-	TEST_MODE	RUN_STP	INTR_EN	CMD_READ_EN	CMD_R/S	-	-

Bits	Field Name	Default Value	Access Type	Description
1	CMD_R/S	0	R/W	Setting this bit this will enable the SPI IAP interface to push out commands from the SPI transmit command FIFO. Cleared by the IP when the command sequence is transmitted successfully.
2	CMD_READ_EN	0	R/W	Setting this bit enables the SPI IAP to load received data in the SPI receive command FIFO.
3	INTR_EN	0	R/W	Interrupt enable bit.
4	RUNSTP	0	R/W	Setting this bit enables the Circular Buffer to start a new acquisition. Cleared by hardware after the IP successfully transfers the buffer's content in system memory.
5	TEST_MODE	0	R/W	Setting this bit disables calibration on the Zmod ADC 1410 Low Level Controller. If the Zmod's AD9648 is programmed to output a pattern, the Low Level Controller will not alter the ADC's output.
31	RST	0	R/W	Resets all registers and state machines to their default values.

4.1.2 Status Register (SR—offset 04h)

The main purpose of this register is to provide status information over the IP in every aspect of its functionality.

31	21	21	20	17	16	10	9	3	2	1	0
-	BUF_FULL	CMD_TX_RX_ERROR	CMD_RX_COUNT	CMD_TX_COUNT	CMD_RUNNING	-	CMD_TX_DONE	-	-	-	-

Bits	Field Name	Default Value	Access Type	Description
0	CMD_TX_DONE	0	W1C	SPI command interface command sequence complete status bit.
2	CMD_RUNNING	0	R	Signals that the SPI command interface is not idle.

3-9	CMD_TX_COUNT	0h	R	Reports the number of bytes in the SPI command transmit FIFO.
10-16	CMD_RX_COUNT	0h	R	Reports the number of bytes in the SPI command receive FIFO.
17-20	CMD_TX_RX_ERROR	0	R/W	Reserved for error reporting.
21	BUF_FULL	0	W1C	The IP sets this bit once the circular buffer is full. The software can only clear this bit (the access type is write 1 to clear)

4.1.3 Interrupt enable register (IER – offset 08h)

Register to mask which status bits will be used as an interrupt

31	22	21	20	1	0
-		BUF_FULL	-		CMD_TX_DONE

Bits	Field Name	Default Value	Access Type	Description
0	CMD_TX_DONE	0	R/W	SPI command interface transaction complete interrupt enable mask bit
21	BUF_FULL	0	R/W	Buffer Full interrupt enable mask bit

4.1.4 Command Transmit register (CMD_TX – offset 0Ch)

Write accesses to this register will load SPI commands in the SPI command transmit FIFO.

31	24	23	22	21	20	8	7	0
-		Read/Write	Width		Address		Data	

Bits	Field Name	Default Value	Access Type	Description
23	Read/Write	0	R/W	Write this bit to 1 for a read command and to 0 for a write command
22-21	Width	0h	R/W	Only 1 byte SPI transfers are supported. This field should be always 0h.
20-8	Address	0h	R/W	AD9648 SPI register address
7-0	Data	0h	R/W	Data byte to be sent to the AD9648. Ignored for read operations

4.1.5 Command Receive register (CMD_RX – offset 10h)

31	0
CMD_RX	

Bits	Field Name	Default Value	Access Type	Description
0-31	CMD_RX	0	R	SPI command receive data. Reading this register will trigger a read operation on the SPI command receive FIFO and will decrement the CMD_RX_COUNT field in the Status Register.

4.1.6 AXI-Stream S2MM Transfer Length (AXIS_S2MM_LENGTH – offset 14h)

Number of bytes to be transferred on the data path using the AXI-Stream protocol.

31	26	25	0
		AXIS_S2MM_LENGTH	

Bits	Field Name	Default Value	Access Type	Description
0-25	LENGTH	0	R/W	Indicates the number of bytes to transfer for the MM2S channel.

4.1.7 WINDOW – Window position(offset 1Ch)

The value must be between 0 and AXIS_S2MM_LENGTH(Transfer length) -1.

Bits	Field Name	Default Value	Access Type	Description
0-14	WND	0	R/W	This value specifies the trigger position in window (circular buffer)
15-31	Reserved	0	R	Unused

4.1.8 TRIG register (TRIG – offset 18h)

Trigger related settings.

Bits	Field Name	Default Value	Access Type	Description
0	CHANNEL_SELECT	0	R/W	Indicates the channel associated to the trigger: 00 – Channel A 01 – Channel B
2-3	TRIG_MODE	00	R/W	Indicates the trigger mode

				00 – Normal 01 - None
4	TRIG_EDGE	0	R/W	Indicates the trigger edge. 0 – rising 1 – falling
5-18	TRIG_LEVEL	0	R/W	Indicates the trigger level
19	SC1_AC_DC	0	R/W	AC/DC coupling relay control for channel1. 0 - DC Coupling 1- AC Coupling
20	SC2_AC_DC	0	R/W	AC/DC coupling relay control for channel2. 0 - DC Coupling 1- AC Coupling
21	SC1_HG_LG	0	R/W	Gain relay control for channel1. 0 - LG Coupling 1- HG Coupling
22	SC2_HG_LG	0	R/W	Gain relay control for channel2. 0 - LG Coupling 1- HG Coupling
26-23	SYNC		R/W	Used for synchronizing multiple ADC devices.

SC1LGMULTCOEF (Offset 24h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 low gain multiplicative coefficient
18-31	Reserved	0	R	Unused

SC1LGADDCOEF (Offset 28h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 low gain additive coefficient
18-31	Reserved	0	R	Unused

SC1HGMULTCOEF (Offset 2Ch)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 high gain multiplicative coefficient

18-31	Reserved	0	R	Unused
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SC1HGADDCOEF (Offset30h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel1 high gain additive coefficient
18-31	Reserved	0	R	Unused

SC2LGMULTCOEF (Offset 34h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 low gain multiplicative coefficient
18-31	Reserved	0	R	Unused

SC2LGADDCOEF (Offset 38h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 low gain additive coefficient
18-31	Reserved	0	R	Unused

SC2HGMULTCOEF (Offset 3Ch)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 high gain multiplicative coefficient
18-31	Reserved	0	R	Unused

SC2HGADDCOEF (Offset 40h)

Bits	Field Name	Default Value	Access Type	Description
0-17	VAL	0	R/W	Channel2 high gain additive coefficient
18-31	Reserved	0	R	Unused

4.2 Circular Buffer State Machine

Incoming samples sent by the Zmod ADC 1410 Low Level controller are stored in a 16Ksample BRAM memory implemented as a circular buffer. The buffer's write and read ports are controlled by a state machine whose simplified state diagram is illustrated in Figure 2. The behavior of the state machine in each state is described below:

1. **Idle state:** The idle state is entered upon a reset condition and the state machine exits this state if and only if the RunStop bit in the Control Register is set by software. If the Normal trigger mode is selected in the Trigger Control Register, the state machine transitions to the Arm state. If the None trigger mode is selected, the state machine transitions to the Fill Buffer None state.
2. **Arm state:** The state machine can only transition to the Arm state from the Idle state. While in this state, the state machine enables the write port to load a number of samples equal to the value specified in the Trigger Position Register in the circular buffer after which it transitions to the Wait Trigger state. This state ensures that at least the number of samples specified by the Trigger Position Register have been recorded prior to detecting a trigger condition.
3. **Wait Trigger state:** The state machine can only transition to the Wait Trigger state from the Arm state. In this state the state machine constantly records incoming samples while monitoring the trigger source for a trigger condition. If the value of the Trigger Position Register is equal to the buffer length specified by the S2MM_Length Register the buffer is full and the state machine transitions to the Send Buffer state. If the value of the Trigger Position Register is smaller than the buffer length requested, the state machine transitions to the Fill Buffer Normal state. Once the trigger condition is met, the address of the write port is register so that the buffer start address can be determined for the read port.
4. **Fill Buffer Normal state:** The state machine can only transition to the Fill Buffer Normal state from the Wait Trigger state. While in this state, the state machine enables the write port to load a number of sample equal to the difference between transfer length requested and the Trigger position specified (buffer full condition in Normal trigger mode). Once the buffer full condition in Normal trigger mode is met, the write port is disabled and the state machine transitions to the Send Buffer state. The Buffer Full bit in the Status Register is set to indicate that the IP core has the buffer data available and is ready to respond to a DMA transfer request.
5. **Fill Buffer None state:** The state machine can only transition to the Fill Buffer None state from the Idle state. While in this state, the state machine enables the write port to load a number of sample equal to the transfer length requested specified in the S2MM_Length Register (buffer full condition in None trigger mode). Once the buffer full condition in None trigger mode is met, the write port is disabled and the state machine transitions to the Send Buffer state. The Buffer Full bit in the Status Register is set to indicate that the IP core has the buffer data available and is ready to respond to a DMA transfer request.
6. **Send Buffer state:** The state machine can transition to the Send Buffer state from the Wait Trigger state, the Fill Buffer Normal state and the Fill Buffer None state. While in this state, the state machine enables the read port to send the whole buffer content to system memory through the DMA engine. It is the software responsibility to program the DMA engine with the correct transfer length value (the same as the one specified in the S2MM_Length Register). The read port starting address is computed based on the write port address registered in the Wait Trigger state for the Normal trigger option and is zero for the None trigger option. If the DMA transfer is completed

successfully, the state machine will clear the RunStop bit in the Control Register and will transition to the Idle state.

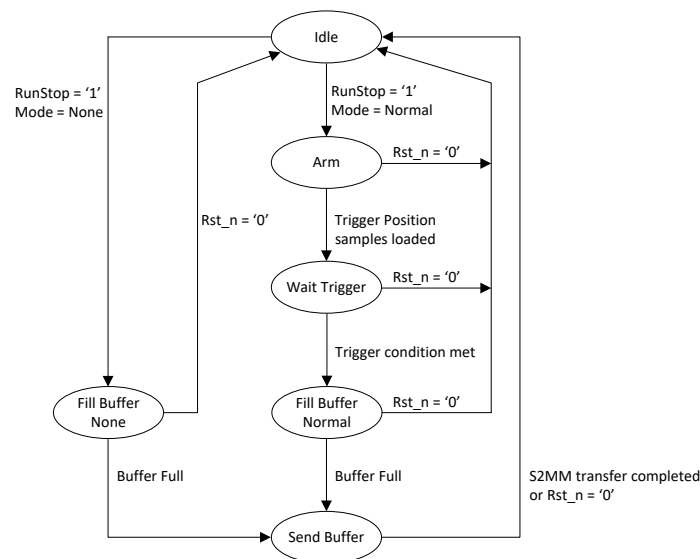


Figure 2: Input data channel demultiplexing

4.3 SPI Adapter

The SPI Adapter block is a bridge between the Register File and the Zmod ADC 1410 Low Level Controller's SPI indirect access port (IAP). Only 8 byte data transfers are currently supported on the SPI interface. The SPI commands are composed of a command word and a data byte which are passed through the CMD_TX Register. The format of the CMD_TX Register is illustrated in Section 4.1.4. A write access to the CMD_TX Register on the AXI Lite interface will trigger the SPI Adapter block to load the SPI command in a transmit FIFO and will increment the transmit FIFO command count (CMD_TX_COUNT field in the Status Register). More SPI read and write commands can be queued in the transmit FIFO by successive write accesses to the CMD_TX register. Once all desired SPI commands are loaded in the transmit FIFO the CMD_R/S bit in the Control Register should be set. In response, the IP will assert the sSPI_EnTx port that will enable the Zmod ADC 1410 Low Level Controller to fetch commands from the transmit FIFO. The Zmod ADC 1410 Low Level Controller will decode the R/W bit in the command word and, in the case of a read command, it will load the data byte received on the SPI port in the SPI Adapter's receive FIFO also increasing the receive FIFO data counter (CMD_RX_COUNT field in the Status Register). The CMD_TX_COUNT field will be decremented for each SPI transaction signaled as successful by the Zmod ADC 1410 Low Level Controller. The CMD_DONE bit in the Status Register will be set on the successful completion of the last command in the transmit FIFO. Read command data can be accessed from software by reading the CMD_RX register. Each read access of this register will assert the receive FIFO's read enable signal also decrementing the CMD_RX_COUNT field in the Status Register. The CMD_RX should only be accessed after the command sequence completion is signaled by the CMD_DONE flag.

4.4 Calibration

The Zmod ADC1410 calibration is not performed at the Zmod ADC1410 AXI Adapter level. The multiplicative and additive calibration coefficients are computed in software based on parameters read from the Zmod's EEPROM memory and written to the configuration registers (addresses 24h-40h). The content of the configuration registers is exported as eight 18bit output ports(the configuration interface) to the Zmod ADC 1410 Low Level controller.

4.5 Clocking

The IP is divided in three clock domains:

1. The system clock domain (100MHz), which clocks the Circular Buffer state machine, the Circular Buffer write port, the command transmit FIFO read port and the command receive FIFO write port.
2. The AXI Stream clock that clocks the Circular Buffer read port and the BRAM to AXI Stream bridge.
3. The AXI Lite clock that clocks the Register File.

5 Port description

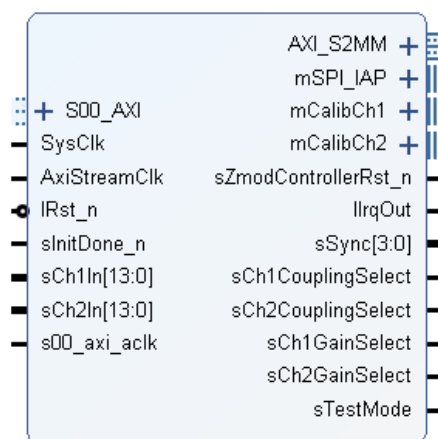


Figure 3: Zmod ADC 1410 AXI Adapter IP

Table 2: IP Port Description

Signal Name	Interface	Signal Type	Init State	Description
SysClk	-	I	N/A	100MHz input clock signal.
AxiStreamClk	S2MM	I	N/A	Input clock associated with the S2MM AXI Stream interface
IRst_n	-	I	N/A	Synchronous reset of negative polarity.
sZmodControllerRst_n	-	O	N/A	Active low reset output synchronized in the SysClk clock domain. Asserted when the external reset signal (IRst_n) is asserted or when a software reset occurs.

sInitDone_n	-	I	N/A	Active low flag indicating when the Zmod Low Level Controller initialization is complete.
sSync	-	O	N/A	Signal used to synchronize multiple AD9648 devices. For more details see [] (Zmod ADC 1410 Low Level Controller)
llrqOut	-	O	N/A	Interrupt output (Level).
sCh1In[13:0]	-	I	N/A	14 bit input data channel 1.
sCh2In[13:0]	-	I	N/A	14 bit input data channel 2.
sCh1LgMultCoef	-	O	N/A	Channel1 low gain multiplicative coefficient output port.
sCh1LgAddCoef	-	O	N/A	Channel1 low gain additive coefficient output port.
sCh1HgMultCoef	-	O	N/A	Channel1 high gain multiplicative coefficient output port.
sCh1HgAddCoef	-	O	N/A	Channel1 high gain additive coefficient output port.
sCh2LgMultCoef	-	O	N/A	Channel2 low gain multiplicative coefficient output port.
sCh2LgAddCoef	-	O	N/A	Channel2 low gain additive coefficient output port.
sCh2HgMultCoef	-	O	N/A	Channel2 high gain multiplicative coefficient output port.
sCh2HgAddCoef	-	O	N/A	Channel2 high gain additive coefficient output port.
sCh1CouplingSelect	-	O	N/A	Channel1 AC DC coupling select output port. • 1 = AC coupling. • 0 = DC coupling.
sCh2CouplingSelect	-	O	N/A	Channel2 AC DC coupling select output port. • 1 = AC coupling. • 0 = DC coupling.
sCh1GainSelect	-	O	N/A	Channel1 gain select output port. • 1 = High Gain. • 0 = Low Gain.
sCh2GainSelect	-	O	N/A	Channel2 gain select output port. • 1 = High Gain. • 0 = Low Gain.
sExtSPI_Idle	-	I	N/A	Flag indicating that the Low Level Controller configuration state machine is in the IDLE state.
sCmdDone	-	I	N/A	Pulse indicating that the SPI command has been successfully completed.
sSPI_TxRdEn	-	I	N/A	Read enable signal used to load data from the transmit command FIFO.
sSPI_TxDout[23:0]	-	O	N/A	Transmit command FIFO output data containing the transfer length, the register address and the register data that are passed to the SPI controller.
sSPI_TxValid	-	O	N/A	Transmit command FIFO data valid signal.

sSPI_RxWrEn	-	I	N/A	Receive command FIFO write enable signal.
sSPI_RxDin[7:0]	-	I	N/A	Receive command FIFO input data.
AXI4 Lite Interface Signals				
AXI_LITE*			Input / Output	AXI4 Lite interface used to communicate with the control and status registers
AXI4 Stream Interface Signals				
S2MM*			Input	AXI4 Stream interface - connect to a DMA engine to transfer data from the IP's Circular Buffer to system memory

6 Designing with the core

6.1 Constraints

The IP does not constrain the clocks it requires as inputs, therefore clocks need to be constrained in the top-level design either manually or by relying on the auto-derived constraints, if using clock modifying blocks. For more information see [4]. No other constraints are required.

7 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.4, May 13, 2014.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Analog Devices, AD9646 Datasheet, Rev C.
4. Xilinx Inc., *UG903: Using Constraints*, v2014.3, October 31, 2014