Zmod DAC 1411 Low Level Controller IP Core User Guide

Revised January 16, 2020; Author Tudor Gherman

1   Introduction

This user guide describes the Digilent **Zmod DAC 1411 Low Level Controller** Intellectual Property. This IP interfaces directly with the Zmod DAC 1411 initializing the hardware and multiplexing two input channels on a single double data rate (DDR) channel as requested by the AD9717 digital to analog converter (DAC) featured by the Zmod DAC 1411. The Zmod DAC 1411 Low Level Controller is intended to be used as a stand-alone IP in projects that do not require processor interaction (standalone mode) or it can be used in conjunction with the Digilent **Zmod DAC1411 AXI Adapter IP** that provides connectivity with the processing system.

IP quick facts	
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Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Custom
Provided with core	
Design files	VHDL
Simulation model	N/A
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2019.1
Synthesis	Vivado Synthesis 2019.1

2   Features

- Initializes the hardware on the Zmod DAC 1411.
- Formats the data received on two single data rate (SDR) channels according to the Zmod DAC 1411 requirements.
- Provides the possibility of overwriting the initial DAC configuration by providing an optional upper level interface that allows indirect access to the DAC's SPI interface.
- Performs offset and gain calibration based on coefficients specified by the user/upper level IPs.

3   Performance

The IP is designed to generate two 100MHz clock signals for the Zmod DAC 1411's DAC, one used to qualify the input data, one used as sample clock and to generate output data at 200MSPS on a 14 bit DDR parallel bus as required by the DAC. The IP core has two SDR input data channels which are synchronous to the system clock input (100MHz) that the IP core requires.
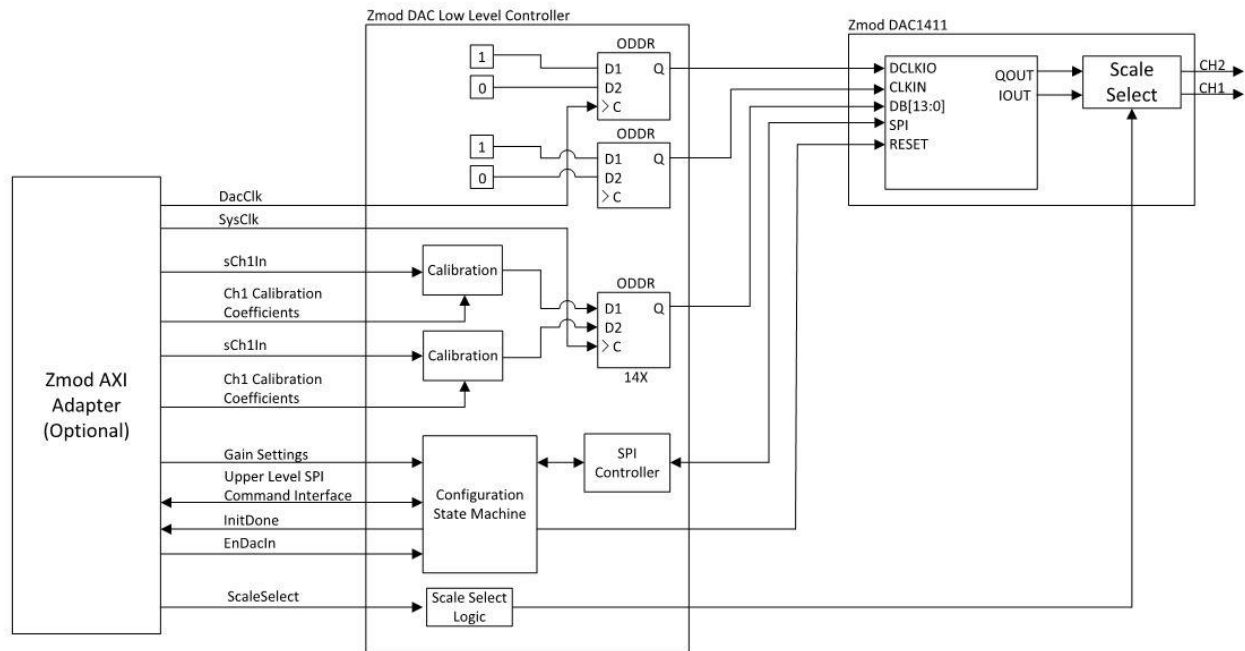
4   Overview

Figure 1. Zmod DAC 1411 Low Level Controller block diagram.

The structure of the IP is presented in Figure 1. The main functionalities are divided as DAC input clock generation, data formatting and calibration (data path) and Zmod DAC 1411 configuration (two items related with configuration functionalities will be detailed separately: the configuration state machine and the SPI controller).

4.1   DAC Input Clock Generation

The IP outputs two 100 MHz clocks (DCLKIO, CLKIN). DCLKIO is used by the AD9717 DAC to qualify the input data, while CLKIN is the DAC's sampling clock. As inputs, the IP requires two 100MHz clock signals: SysClk and DacClk. DacClk needs to be 90 degrees phase shifted in relation with SysClk and it is used to generate DCLKIO.

4.2   Data Path

The data path consists of two stages. The first stage is responsible with applying the multiplicative and additive calibration coefficients to both channels, compensating for the Zmod DAC 1411 DAC output filter tolerances. The calibration coefficients can be introduced as IP parameters or can be passed through (optional) external ports, depending on whether the core is used in the stand alone mode or it is connected to the processing system through the Zmod DAC 1411 AXI adapter IP core. The user can obtain the calibration coefficients by booting the Eclypse board with the Linux image provided at https://github.com/Digilent/Eclypse-Z7/releases and run the "decutil enum" command in the command line. The Zmod DAC 1411 has to be plugged in one of the Eclypse's board SYZYGY ports. The output of the calibration block is computed based on relation (1):

$$ChxODDR = ChxIn * CoefxMult_{LH/HG} + CoefxAdd_{LG/HG} \qquad (1)$$

In the previous relation, the IP core's data input channels are labeled *ChxIn*, the calibration stage outputs are labeled *ChXODDR* while *CoefxMult$_{LG/HG}$* and *CoefxAdd$_{LG/HG}$* represent the gain and offset calibration coefficients.
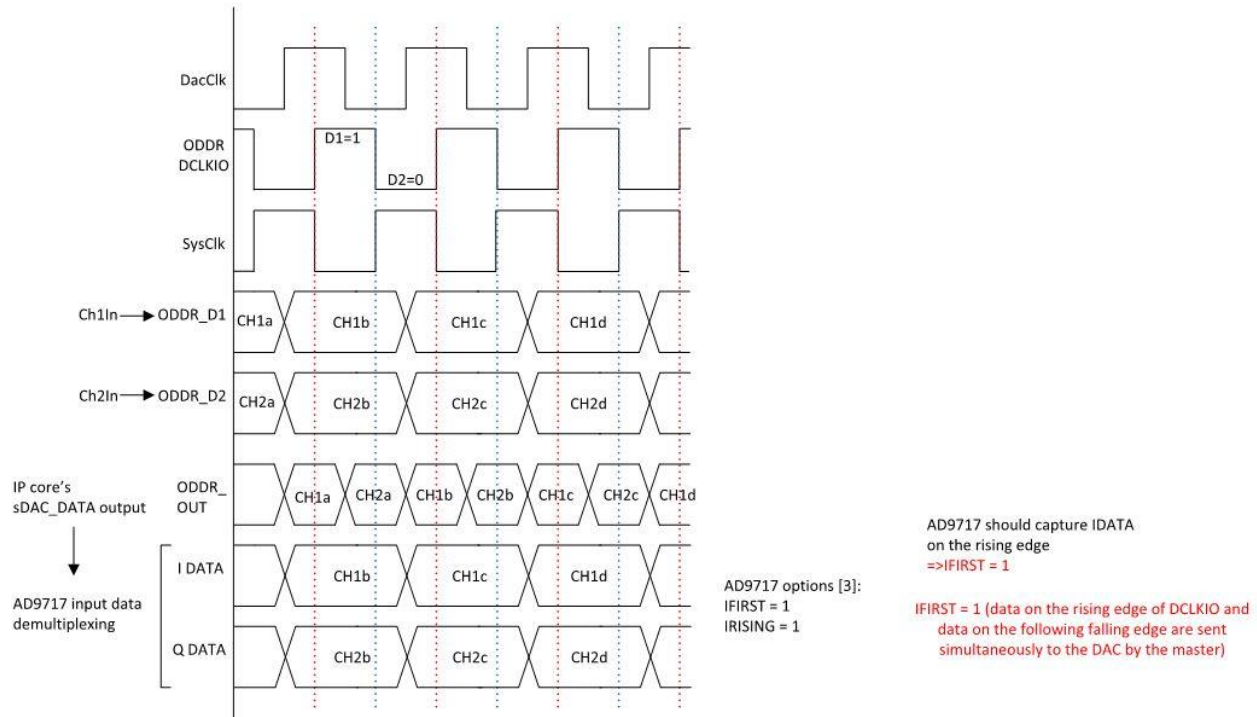

Figure 2: DAC data formatting

Each output bit of the calibration stage is connected to an ODDR primitive which formats the output data according to the AD9717 requirements [3](Figure 2). The two input channels are multiplexed on a 200MSPS 14 bit parallel bus.

4.3   Scale Select

The IP core provides the choice of selecting the Zmod DAC 1411 scale options statically or dynamically. For static configuration, the ExtScaleEn needs to be set as "false" and the scale configuration parameters (See **Error! Reference source not found.**) need to be configured in the IP core GUI. For d ynamic scale control, the ExtScaleEn needs to be set as "true" and the external scale control ports will become available.

4.4   Configuration State Machine

The configuration state machine sends a predefined sequence of SPI commands to the Zmods's AD9717, performing the device's initialization. Once the sequence is executed, the state machine enters the idle state where it monitors if there is any valid data on the upper level SPI command interface. After executing any requested SPI transfers, the state machine passes the received SPI data (for read commands) and returns to the idle state. The initial configuration command sequence is listed below.

After configuring each register, the register data is read back and checked against the expected value in order to determine any SPI transaction error. For more details about configuration registers details please consult [3].

1. **SPI Control register**: Set software reset (Address: 00h; Data: 20h)
2. **SPI Control register**: Release software reset (Address: 00h; Data: 00h)
3. **Data Control Register**: Configuration selected: 2's complement, IDATA latched on DCLKIO rising edge, I first of pair on data input pads, data clock input enable, data clock output disable (Address: 02h; Data: **B4h**)
4. **CLKMODE Register**: Clear the reacquire bit (Address: 14h; Data: 00h)
5. **CLKMODE Register**: Set (toggle) the require bit (Address: 14h; Data: 00h)
6. **CLKMODE Register**: Clear the reacquire bit (Address: 14h; Data: 00h)
7. **Memory R/W Register**: Reset UNCALI and UNCALQ bits are reset (Address: 12h; Data: 00h)
8. **Cal Control Register**: Set up calibration clock to SysClk/64 (Address: 0Eh; Data: 02h)
9. **Cal Control Register**: Enable calibration clock (Address: 0Eh; Data: 0Ah)
10. **Cal Control Register**: Select the DAC to self-calibrate (Address: 0Eh; Data: 3Ah)
11. **Memory R/W Register**: Start self-calibration (Address: 12h; Data: 10h)
12. **Cal Control Register**: Check if self-calibration has completed by reading CALSTATI and CALSTATQ bits (Address: 0Fh; Data: -)
13. **Memory R/W Register**: Clear register (Address: 12h; Data: 00h)
14. **Cal Control Register**: Disable calibration clock (Address: 0Eh; Data: 00h)

4.5   SPI Controller

The SPI controller is designed to carry out basic register access over the AD9717's SPI interface. Only single byte data transfers are currently supported. More details about the AD9717's SPI interface can be found in [3]. The SPI controller's ports are described below.

Table 1. SPI controller IO ports

Signal Name	Interface	Signal Type	Init State	Description
SysClk	-	I	N/A	100MHz input clock signal.
DacClk	-	I	N/A	100MHz input clock signal phase shifted by 90 degrees with respect to SysClk.
sRst_n	-	I	N/A	Synchronous reset of negative polarity.
sSPI_Clk	SPI	O	N/A	Output SPI clock [3] divided from SysClk. Should be connected to the corresponding top level SPI port.
sSDIO	SPI	IO	N/A	SPI SDIO signal [3]. Should be connected to the corresponding top level SPI port.
sCS	SPI	I	N/A	SPI CS signal [3]. Should be connected to the corresponding top level SPI port.

sRdData[7:0]	-	O	N/A	SPI register read received data
sWrData	-	I	N/A	SPI register write data.
sAddr[11:0]	-	I	N/A	SPI instruction phase address.
sWidth[1:0}]	-	I	N/A	SPI instruction phase word length. The only value currently supported is 0 (1 data byte transferred).
sRdEn	-	I	N/A	Triggers a register read operation over SPI.
sWrEn	-	I	N/A	Triggers a register write operation over SPI.
sDone	-	O	N/A	Indicates that the operation requested has completed

4.6   Clocking

The IP operates in a two clock domain. The system clock (SysClk) clocks all logic except the output clock generation blocks. All output clocks being derived from the 100MHz input DacClk. The IP does not constrain any of the input clocks, therefore it needs to be constrained in the top-level design either manually or by relying on the auto-derived constraints, if using clock modifying blocks. For more information see [4].
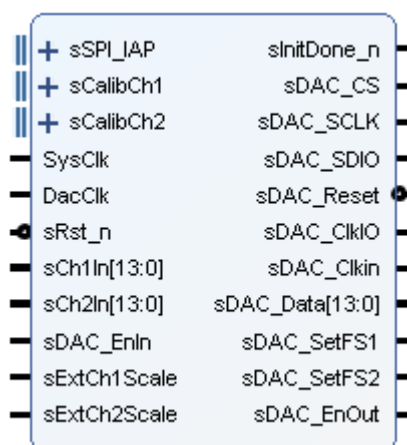
5   Port description

Figure 3: Zmod DAC 1411 Low Level Controller IP

Table 2. IP core port description

Signal Name	Interface	Signal Type	Init State	Description
SysClk	-	I	N/A	100MHz input clock signal.
sRst_n	-	I	N/A	Synchronous reset of negative polarity.

sInitDone_n	-	O	N/A	Active low flag indicating when the Zmod initialization is complete.
sCh1In[13:0]	-	I	N/A	Channel1 data input.
sCh2In[13:0]	-	I	N/A	Channel2 data input.
sExtCh1LgMultCoef	-	O	N/A	Channel1 low gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh1LgAddCoef	-	O	N/A	Channel1 low gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh1HgMultCoef	-	O	N/A	Channel1 high gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh1HgAddCoef	-	O	N/A	Channel1 high gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2LgMultCoef	-	O	N/A	Channel2 low gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2LgAddCoef	-	O	N/A	Channel2 low gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2HgMultCoef	-	O	N/A	Channel2 high gain multiplicative coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh2HgAddCoef	-	O	N/A	Channel2 high gain additive coefficient external port. This port is enabled by setting the ExtCalibEn parameter to "true".
sExtCh1Scale	-	O	N/A	Channel1 scale select external port. This port is enabled by setting the ExtScaleConfigEn parameter to "true". • 1 = Full Scale. • 0 = **Not Full** Scale.
sExtCh2Scale	-	O	N/A	Channel1 scale select external port. This port is enabled by setting the ExtScaleConfigEn parameter to "true". • 1 = Full Scale. • 0 = **Not Full** Scale.
sDAC_EnIn	-	I	N/A	When asserted the Zmod DAC 1411 output relay is placed in the set position. When deasserted the two DAC channels are disconnected from the outputs.
sExtSPI_Idle	-	O	N/A	Flag indicating that the configuration state machine is in the IDLE state. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sCmdDone	-	O	N/A	Pulse indicating that the SPI command has been successfully completed. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".

sExtSPI_TxRdEn	-	I	N/A	Read enable signal used to load data from the upper layer TX command FIFO. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sExtSPI_TxDout[23:0]	-	I	N/A	Upper layer TX command FIFO output data containing the the transfer length, the register address and the register data that are passed to the SPI controller. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sExtSPI_TxValid	-	I	N/A	Upper layer TX command FIFO data valid signal. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sExtSPI_RxWrEn	-	O	N/A	Upper layer RX command FIFO write enable signal. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sExtSPI_RxDin[7:0]	-	O	N/A	Upper layer RX command FIFO input data. This port is enabled by setting the ExtCmdInterfaceEn parameter to "true".
sDAC_ClkIO	-	O	N/A	Should be connected to the AD9717 DCLKIO input [].
sDAC_Clkin	-	O	N/A	Should be connected to the AD9717 CLKIN input [].
sDAC_Data[13:0]	-	O	N/A	Should be connected to the AD9717 DB[13:0] input [].
sDAC_Reset	-	I	N/A	Should be connected to the AD9717 RESET/PINMD input [].
sDAC_SDIO	SPI	IO	N/A	SPI SDIO signal [].
sDAC_CS	SPI	O	N/A	SPI CS signal [].
sDAC_Sclk	SPI	O	N/A	SPI output clock.
sDAC_setFS1	-	O	N/A	This signal control's the Zmod DAC 1411 scale select analog switch for channel1.
sDAC_setFS2	-	O	N/A	This signal control's the Zmod DAC 1411 scale select analog switch for channel2.
sDAC_EnOut	-	O	N/A	This signal controls the Zmod DAC 1411 output relay.

6 Parameter description

Table 3. IP core parameter descriptions.

Signal Name	Description
ExtScaleConfigEn	Enables the external scale configuration port. Set to "true" when dynamic relay configuration is required. Set to "false" when static relay configuration is sufficient.
ExtCalibEn	Enables the external calibration interface. Set to "true" when the IP core is connected to the **Zmod DAC 1411 AXI Adapter IP** core. Set to "false" when the core operates in stand alone mode.

ExtCmdInterfaceEn	Enables the upper layer IP SPI configuration interface. Set to "true" when the IP core is connected to **Zmod DAC 1411 AXI Adapter**. This will enable the processor to access the Zmod DAC 1411 SPI interface. Set to "false" when initial configuration described in Section 4.5 is sufficient.
kCh1CouplinStatic	Channel1 AC DC coupling select static configuration parameter. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. The state of the relay can not be changed afterwards. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored. • 1 = AC coupling. • 0 = DC coupling.
kCh2CouplinStatic	Channel2 AC DC coupling select static configuration parameter. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. The state of the relay can not be changed afterwards. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored. • 1 = AC coupling. • 0 = DC coupling.
kCh1GainStatic	Channel1 gain select static configuration parameter. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. The state of the relay can not be changed afterwards. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored. • 1 = High Gain. • 0 = Low Gain.
kCh2GainStatic	Channel2 gain select static configuration parameter. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. The state of the relay can not be changed afterwards. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored. • 1 = High Gain. • 0 = Low Gain.
kCh1LgMultCoefStatic[17:0]	Channel1 low gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.
kCh1LgAddCoefStatic[17:0]	Channel1 low gain additive calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.
kCh1HgMultCoefStatic[17:0]	Channel1 high gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.

kCh1HgAddCoefStatic[17:0]	Channel1 high gain additive calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.
kCh2LgMultCoefStatic[17:0]	Channel2 low gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.
kCh2LgAddCoefStatic[17:0]	Channel2 low gain additive calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.
kCh2HgMultCoefStatic[17:0]	Channel2 high gain multiplicative calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.
kCh2HgAddCoefStatic[17:0]	Channel2 high gain additive calibration coefficient. If the ExtRelayConfigEn parameter to "false", the configuration state machine will configure the coupling select relay according to this parameter's value at initialization time. If the value of ExtRelayConfigEn parameter is "true", this parameter is ignored and the processing system is expected to update the corresponding external port.

7   Designing with the core

7.1   Customization

The IP through its customizable parameters (ExtScaleConfigEn , ExtCalibEn, ExtCmdInterfaceEn) enables the user to opt for a more basic design, with minimal external ports or a more configurable but also more complex design with several ports that enable dynamic configuration of several hardware features. When using the IP Core with the Zmod DAC 1411 AXI adapter, the hardware configuration features are expected to be controlled by the processing system, so all interfaces should be enabled and connected to the upper layer IP Core.

8   References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.4, May 13, 2014.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Analog Devices, AD9717 Datasheet, Rev B.
4. Xilinx Inc., UG903: Using Constraints, v2014.3, October 31, 2014