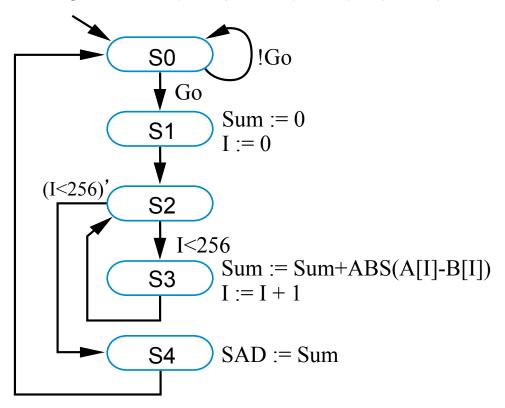
Verilog – High-Level State Machines

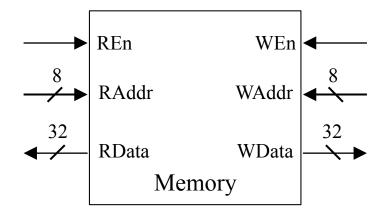
Modify the following HLSM to interface with the memories for A and B

Inputs: Go (bit)

Outputs: SAD (32-bits)

Local registers: Sum (32 bit), SAD (32 bits); I (32 bits)

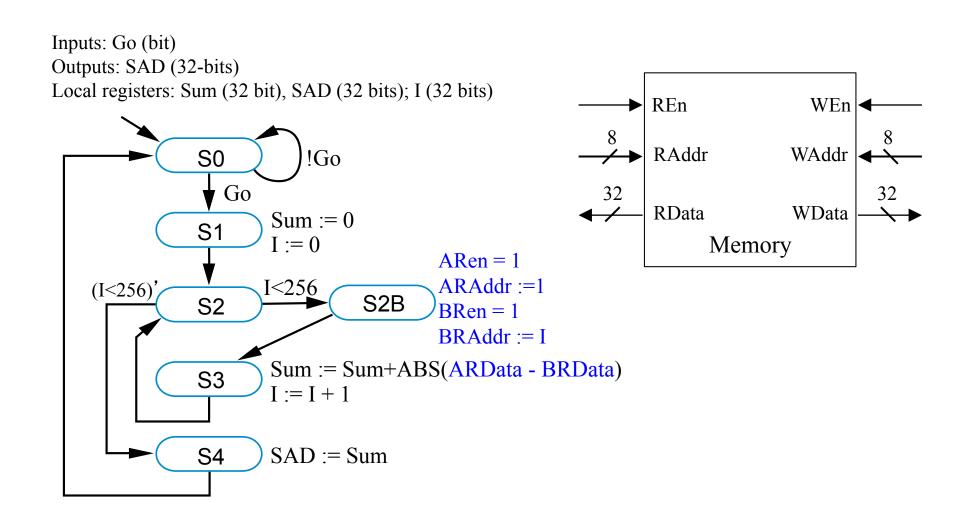




Assume a memory for a synchronous read port.

Verilog – High-Level State Machines

Option1: Add state to Assert Ren and Raddr before S3.



Verilog – High-Level State Machines

Option 2: Use state S2 to start read operation

Inputs: Go (bit) Outputs: SAD (32-bits) Local registers: Sum (32 bit), SAD (32 bits); I (32 bits) REn WEn | RAddr S0 WAddr !Go 32 Go WData **RData** Sum := 0**S1** Memory I := 0ARen = 1(I<256) **S2** ARAddr :=1 BRen = 1I<256 BRAddr := ISum := Sum+ABS(ARData - BRData) S3 I := I + 1SAD := SumS4