ECE 474/574
Homework 0

No deliverable. Complete by: 11.59pm, Sunday, January 21

Work Individually, but you may discuss with your colleagues on Piazza or otherwise. This homework is intended to help you revise the basics of combinational logic and Verilog.

1. If you have not done so already, install Xilinx Vivado on your personal computer.

   Quick Install Instructions (if you've installed it, skip to 2.)
   Use the license-free WebPACK version found here: http://www.xilinx.com/support/download.html. Download the *Self Extracting Web Installer* to install Vivado (no options for Mac, unfortunately. You may need to use a virtual machine to get around it, or use ECE lab computers).

   You may be asked to register for an account with Xilinx if you don't already have one. If, for some reason, your account has been locked due to an "export compliance error", you can email websupport@xilinx.com to get your account reinstated. If you have a slower computer, you may install an older version of Vivado (e.g., 2020) to save some space.

   You may also use a different design tool (e.g., Quartus).

2. Design and simulate the following circuit, with Verilog, using *(a)* **Behavioral design**; and *(b)* **Structural design**.

   "I have two friends from the hiking club and two friends from the basketball team. I will go to a party if, and only if, at least one friend from each team comes with me. Your circuit should output 1 if I go to the party and 0 otherwise."

   You must write one testbench to functionally simulate your circuit (you may need to make a minor change to instantiate the behavioral or structural design). Both behavioral and structural designs should output the same waveform with the same testbench.

   Inspect your waveform and make sure it behaves according to your truth table.