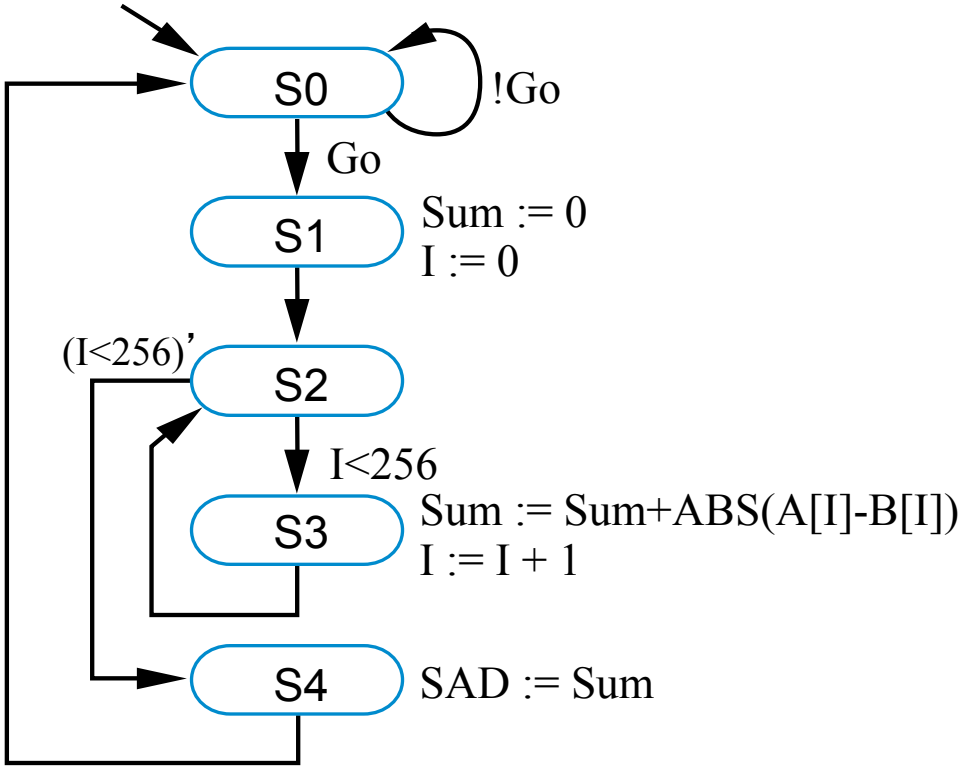
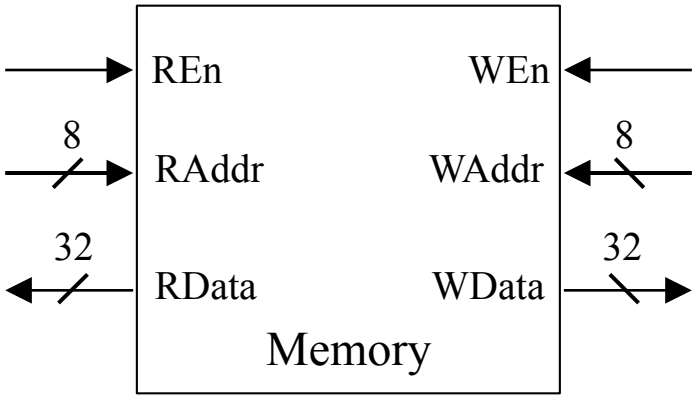
Verilog – High-Level State Machines

Modify the following HLSM to interface with the memories for A and B

Inputs: Go (bit)
Outputs: SAD (32-bits)
Local registers: Sum (32 bit), SAD (32 bits); I (32 bits)



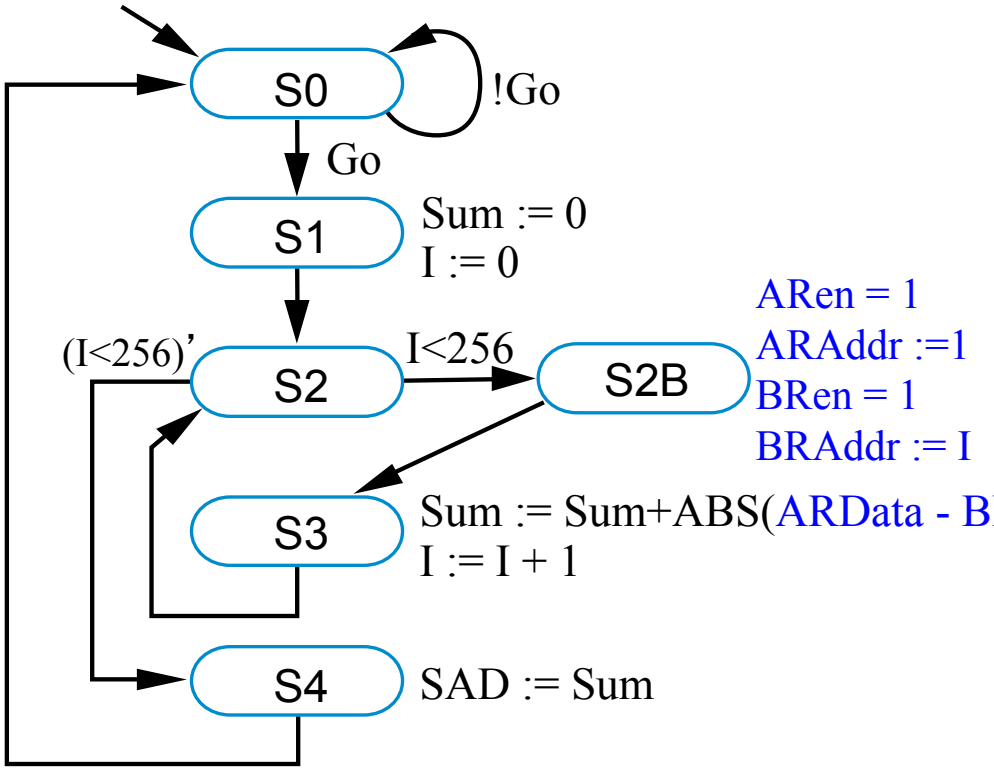


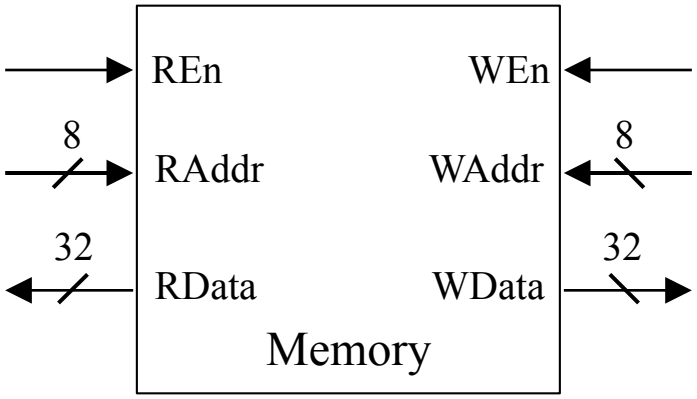
Assume a memory for a synchronous read port.

Verilog – High-Level State Machines

Option1: Add state to Assert Ren and Raddr before S3.

Inputs: Go (bit)
Outputs: SAD (32-bits)
Local registers: Sum (32 bit), SAD (32 bits); I (32 bits)





Verilog – High-Level State Machines

Option 2: Use state S2 to start read operation

Inputs: Go (bit)
Outputs: SAD (32-bits)
Local registers: Sum (32 bit), SAD (32 bits); I (32 bits)