

1.3: A programmer starts by writing high level code. A compiler takes the code and converts it into an assembly language. Then, an assembler takes the assembly code and translates it into binary machine language.

1.4a: 1 pixel = 3 bytes, one byte per color

$$\text{total pixels} = 1280 \times 1024 = 1,310,720 \text{ pixels}$$

$$\text{total size of frame buffer: } 3 \times 1,310,720 = 3,932,160 \text{ bytes}$$

$$1.4b: 3,932,160 \times 8 = 31,457,280 \text{ bits}$$

$$31,457,280 \text{ bits} / 100,000,000 \text{ bits/sec} = .3145729 \text{ seconds}$$

$$1.5a \text{ CPU time} = \frac{\text{instructions} \times CPI}{\text{clock rate}}$$

$$\text{instructions per second} = \frac{\text{clock rate}}{CPI}$$

$$IPS_1 = \frac{3.6 \text{ Hz}}{1.5} = 2 \times 10^9$$

$$IPS_2 = \frac{2.5 \text{ GHz}}{1} = 2.5 \times 10^9$$

$$IPS_3 = \frac{4.6 \text{ Hz}}{2.2} = 1.82 \times 10^9$$

processor 2 has highest instructions per second

1.5b instructions = IPS \times CPU time

$$\text{instructions}_1 = 2 \times 10^9 \times 10 = 2 \times 10^{10} \text{ instructions}$$

$$\text{clock cycles}_1 = 10 \times 3.6 \text{ Hz} = 3 \times 10^{10} \text{ cycles}$$

$$\text{instructions}_2 = 2.5 \times 10^9 \times 10 = 2.5 \times 10^{10} \text{ instructions}$$

$$\text{clock cycles}_2 = 10 \times 2.56 \text{ Hz} = 2.5 \times 10^{10} \text{ cycles}$$

$$\text{instructions}_3 = 1.82 \times 10^9 \times 10 = 1.82 \times 10^{10} \text{ instructions}$$

$$\text{clock cycles}_3 = 10 \times 4 \text{ GHz} = 4 \times 10^{10} \text{ cycles}$$

1.5c

$$\text{Execution time} = \frac{\text{clock cycles}}{\text{clock rate}}$$

$$\text{clock cycles} = \text{instructions} \times \text{CPI}$$

$$\frac{\text{CPI}}{\text{new clock}} = .7 \cdot \frac{\text{CPI}}{\text{old clock}}$$

$$\frac{1.2}{\text{new clock}} = \frac{.7}{\text{old clock}}$$

$$1.71 \times \text{old clock} = \text{new clock}$$

71% increase

1.6 class 1: $10^6 \times .1 = 10^5$ instructions

B: $10^6 \times .2 = 2 \times 10^5$ instructions

C: $10^6 \times .5 = 5 \times 10^5$ instructions

D: $10^6 \times .2 = 2 \times 10^5$ instructions

processor p1:

$$(1 \times 10^5) + (2 \times 2 \times 10^5) + (3 \times 5 \times 10^5) + (3 \times 2 \times 10^5) = 2.6 \times 10^6 \text{ cycles}$$

$$\text{CPU time} = \frac{2.6 \times 10^5}{3.6 \text{ GHz}} = 1.04 \text{ s}$$

processor p2:

$$(2 \times 10^5) + (2 \times 2 \times 10^5) + (2 \times 5 \times 10^5) + (2 \times 2 \times 10^5) = 2 \times 10^6 \text{ cycles}$$

$$\text{CPU time} = \frac{2 \times 10^5}{3.6 \text{ GHz}} = 666 \text{ ns}$$

processor 2 is faster

Q.

processor p1:

$$CPI = \frac{2.6 \times 10^6}{10^6} = 2.6$$

processor p²:

$$CPI = \frac{2 \times 10^6}{10.6} = 2$$

b.

processor p¹:

$$2.6 \times 10^6 \text{ cycles}$$

processor p²:

$$2 \times 10^6 \text{ cycles}$$

1.8.1

$$P = C_L V^2 f$$

Pentium 4 Prescott

$$C_L = \frac{P}{V^2 f} = \frac{90W}{(1.25V)^2 (3.6GHz)} = 1.6 \times 10^{-8}$$

i5 Ivy Bridge:

$$C_L = \frac{P}{V^2 F} = \frac{40W}{(9V)^2 (3.66\text{Hz})} = 1.4 \times 10^{-8}$$

1.8.2

Pentium 4:

$$\frac{10W}{10W + 90W} = 10\%$$

static power

$$\frac{10W}{90W} = .111$$

ratio

static:dynamic

Core i5:

$$\frac{30W}{30W + 40W} = 42.86\%$$

static power

$$\frac{30W}{40W} = .75$$

ratio