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Comprehensive review of GaN HEMTs: Architectures, recent developments, reliability concerns, challenges, and multifaceted applications

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ABSTRACT

The emerging need for high-frequency, high-power electronics and biosensors necessitates the demand for high electron mobility transistors (HEMTs) that outperform the mainstream silicon and other direct bandgap materials. Gallium Nitride (GaN)-based HEMTs can operate in both depletion-mode (D-mode) and enhancement-mode (E-mode), and have garnered significant attention for their superior performance in these applications. These wide band-gap semiconductors exhibit significant outcomes in DC as well as RF applications, such as a higher threshold voltage of 8.6 V, transconductance of 680 S/mm with OIP3 (output third-order intercept point) of 41.2 dB, cut-off frequency (f_T) of 391 GHz compared to the conventional devices. There are also found some meticulous parameters e.g. breakdown voltage (V_{br}) of 1513 V, drain saturation current of 3.41 kA/cm^2 with an equivalent noise resistance (R_n) of 1.21 dB and 20 Ω at 20 GHz, a low on-resistance (R_{ON}) of 0.00269 Ω-mm, at gate length (L_G) of 100 nm in a GaN HEMT by using quaternary InAlGaN barrier is achieved maximum drain current ($I_{DS,\ max}$) of 1940 mA/mm while another HEMT with Carbon doped GaN buffer as well as AlGaN back barrier gets V_{br} around 2900 V. The RF metrics, like a f_T of 200 GHz with moderate L_G of 80 nm for AlGaN/GaN HEMT with Si substrate of plasma molecular beam epitaxy, a maximum oscillation frequency (f_{max}) of 308 GHz, show great impact on High-frequency and microwave applications. Nevertheless, the E-mode outperforms the D-mode HEMTs for secured operations with low leakage loss; there are still some challenges, such as current collapse, short-channel effects, and pinch-off phenomena that persist, impacting device reliability. This review article examines recent advancements in GaN HEMT architectures, emerging materials, and their applications in power and radio-frequency devices, as well as explores future applications in biosensing, satellite, and optical communications.

1. Introduction

GaN-based HEMTs nowadays have gained significant attention for high power and high frequency applications due to their heterostructures having superior material properties, wide band-gap, higher voltage, current, frequency and temperature withstand due to the high electric field strength of the material combined with the high mobility and electron density of the two-dimensional electron gas (2DEG) formed at the heterointerface between the channel and barrier layers [1]. Because of having a strong market share, researchers have recently put enormous effort into optimizing GaN-based HEMT devices [2–8] with improved reliability [9–15], better circuitry and device architecture [16–18]. The primary difference between normally-on and normally-off AlGaN/GaN HEMTs lies in their default conduction state at zero gate bias. Normally-on HEMTs, also known as depletion-mode devices, exhibit a conductive channel due to the spontaneous and piezoelectric polarization-induced formation of a two-dimensional electron gas (2DEG) at the heterointerface even when no gate voltage is applied. In contrast, normally-off HEMTs, or enhancement-mode devices, are engineered to remain non-conductive at zero gate bias, requiring a positive gate voltage to induce channel formation. For high power and RF applications (e.g., 5 G applications) through minimization of power loss & improved device stability, normally-off (Enhancement mode) transistors are preferred. Different approaches have already been proposed to transform a depletion-mode HEMT into an enhancement-mode HEMT. These approaches include recessed-gate structure [34], fluorine ions implantation [35], GaN (p-GaN) gate HEMTs, combining a D-mode HEMT in a “cascode” configuration with an E-mode MOSFET [36].

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However, the implementation of these techniques introduces several challenges. Recessed-gate hybrid MISHEMT (metal-insulated semiconductor high electron mobility transistor) devices often face instability in their threshold voltage (V_{th}), mainly due to charge getting trapped inside the gate insulator [37,38]. Simply adding a p-GaN layer to an AlGaN/GaN structure usually isn't enough to achieve a normally-off mode. Other important factors must be considered, such as the properties of the heterostructure, heat treatment, gate design, how the p-GaN is etched, and the doping process [39]. During the etching of p-GaN in HEMT fabrication, it's important to maintain a high selectivity ratio. If the material is over-etched or under-etched, the device's performance can be seriously affected [41]. Still, problems like unstable threshold voltage [42] and higher leakage current in the off-state are common due to the gate being biased in the on-state [43]. This instability is often linked to charge movement within the device [44].

Moreover, reaching a high positive threshold voltage is tricky because there's a trade-off — as one tries to increase V_{th}, the resistance in the channel (sheet resistance) also tends to increase [45]. This makes optimizing these devices more complex. Another major issue is self-heating, which can damage the device, reduce its efficiency, and shorten its lifespan. That's why thermal management is a key part of the design process [40,46–50]. Additionally, issues like current collapse, on-state resistance fluctuation [51], and high contact resistance at the source and drain remain major challenges. For high-power applications, keeping the ohmic contact resistance (R_c) as low as possible is essential [52].

In short, even though GaN—HEMTs have widespread applications in power [126,127] & RF devices multiple challenges like epitaxial growth & material quality control [27], device scaling, thermal management, ohmic contact [28] quality and the impact of interface and surface states [29] remain concerning issues which must be resolved for reliable and effective performance of the devices. Continuous research & studies are ongoing to mitigate the reliability challenges. Surface passivation techniques have been proposed to mitigate current collapse [30], uniform distribution of electric fields can be achieved through field plate designs [31,32] that reduce the risk of carrier trapping, but these adaptations must be assessed in terms of their impact on other performance metrics such as gate leakage and switching speed. Advanced ESD (Electrostatic Discharge) protection methods [33], including on-chip protection diodes and optimized device structures, can greatly enhance the robustness of the device. Additionally, enhancing grounding and using packaging materials with higher ESD tolerance can offer further protection against ESD-induced failure. Gate oxide deterioration, current collapse, ESD sensitivity, thermal cycling effects, and high-frequency performance degradation are some of the issues that affect the durability of GaN HEMTs. Progressive designs & modern cutting-edge technologies with effective testing procedures are necessary to address these challenges.

HEMTs are crucial for a wide range of applications, including photonics, high-frequency communication, power control, and energy conversion systems like power supplies, inverters, and motor drives. Asif Khan and his team were the first to successfully fabricate an AG-HEMT device [19]. Since then, improvements in both DC and RF performance have allowed GaN—HEMTs to be effectively used in high-power and high-frequency electronics. Varadhan et al. presented a vertical CAVET architecture incorporating a boron-doped GaN layer as the current blocking layer (CBL) within an AlGaN/GaN platform [255]. The implementation of this structure in a vertical AlGaN/GaN metal-–insulated semiconductor field effect transistor demonstrated several performance enhancements, including an increased threshold voltage, higher drain saturation current, suppressed OFF-state leakage, and superior high-frequency and noise characteristics. These findings offer valuable insights into the dominant noise mechanisms in GaN-based transistors and contribute to the ongoing efforts to optimize their noise performance for high-frequency applications. Mohanbabu et al. described AlGaN/GaN HEMTs for use in biosensing applications aimed at detecting cancer, tumors, and kidney malfunction, as AlGaN/GaN materials exhibit outstanding sensing performances, attributed to their unique characteristics—high sensitivity, strong chemical stability, compatibility with high-density integration, and biocompatibility [247]. Such features make them highly suitable for biomedical diagnostics. The developed devices are capable of monitoring and detecting specific biomolecules, enabling early disease detection, minimizing patient discomfort associated with delayed diagnosis, and potentially lowering healthcare costs.

Advancements in substrate engineering have recently shown that combining diamond with GaN-based HEMTs can significantly enhance thermal performance, structural stability, and power output. This integration also improves the device's breakdown voltage and allows for higher power density [20–23]. These benefits make diamond-GaN HEMTs particularly suitable for demanding applications like radar systems, satellite communications, and high-power motors operating at high frequencies (such as K-band and Ku-band). Key performance characteristics of HEMTs — including subthreshold leakage, breakdown voltage, current collapse, short-channel effects, and maximum drain current (I_D) — rely heavily on proper buffer layer design [24]. Additionally, power HEMTs with AlGaN channels containing high aluminum content are becoming more popular. Their ultra-wide bandgap (up to 5.7 eV for $Al_{0.7}Ga_{0.3}N$) makes them well-suited for use in high-temperature and high-power RF applications [25,26].

RF Gallium Nitride devices are experiencing rapid market expansion, rising from USD 0.93 billion in 2024 to USD 1.22 billion in 2025 and soaring to about USD 13.91 billion by 2034, at a CAGR of 31.06 % from 2025 [243]. The technology's strong growth is fueled by rising demand in 6 G, aerospace, defense, and telecommunication sectors due to its high efficiency and power performance. Recent market projections for the AlGaN/GaN HEMTs sector, as analyzed in leading market research and consulting reports referenced as [244–246], have been comprehensively reviewed to provide a clear outlook on the anticipated market growth by 2030. This detailed assessment is visually summarized in Fig. 1, which illustrates the forecasted market scenario for different applications of GaN HEMTs.

Here is a comparison table, differentiates the DC and RF characteristics of various structures of GaN HEMTs. (Ref: Reference, L_G = Gate length, g_m = Transconductance, V_{br} = Breakdown Voltage, V_{th} = Threshold Voltage, R_{on} = On Resistance) (Table 1).

This paper represents an extensive review on the reliability, challenges, and future prospects of GaN-based HEMTs with RF & power device applications. This paper mainly summarizes the developments of GaN HEMTS with issues and challenges that need to be addressed for the extensive use of GaN-based HEMTs. The next segment provides valuable information regarding the innovations and novelties in the structure of GaN-based HEMTs, which show a gradual progress in architecture. Further, the forward segment deals with the state of the art, which displays the enhancement in power devices as well as RF devices. In addition, the latter segment shows what are the issues and challenges

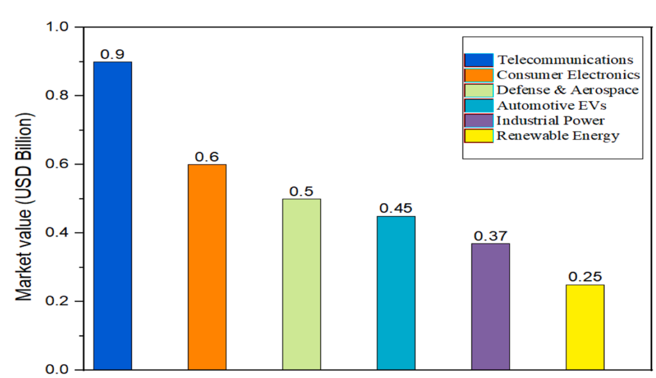

Fig. 1. AlGaN/GaN market scenario for different applications by 2030.

Table 1
DC and RF characteristics of various structures of GaN HEMTs.

Ref.	L_G (nm)	g_m (ms/mm)	I_{DS_max} (mA/mm)	f_T (GHz)	f_{max} (GHz)	V_{br} (V)	V_{th} (V)	R_{on} (Ω/mm)
[248]	200	–	1071	55	–	189		0.4 (R_c)
[227]	800	370	747	–	–	–	0.3	0.002627
[250]	4000	–	–	–	–	1192	3.2	0.0113
[251]	450	200	1000	20	40.8	206	1.1	1.8
[252]	50	541	2710	391	–	–	–	–
[253]	1500	–	242.9	–	–	757	–	2.718
[80]	5000	–	187	–	–	–	2	27
[255]	1000	–	3410	5.12	36.8	1600	6.36	–
[91]	5000	–	–	–	–	–	1.07	22.34
[257]	500	–	500	–	–	–	1.5	–
[258]	1000	783.42	4200	5.12	36.8	1590		–
[259]	1990	97.5	718	–	–	–	8.6	–
[260]	55	710	5900	290	364	73	−3	–
[262]	140	421	1294	65	100	34	–	–
[263]	300	425	1400	55	121		–	–
[73]	2000	142	420	–	–	156	–	–
[265]	200	415	1096	96	110	151	–	–
[266]	600	370	1130	26	60		–	–
[267]	200	422	1200	81	194	134	–	–
[268]		–	200	–	–	2900	–	–
[269]	2000	130	520	4.5	11.5	–	–	–
[270]	265	291	1010	43.7	126.5	–	–	–
[271]	150	439	1000	104	205	127	–	–
[272]	5000	123	321	–	–	2154	–	–
[273]	3000	–	198	–	–	2274	–	–
[274]	500	374	1130	–	–	173	–	–
[275]	200	400	1000	–	–	90	–	–
[86]	2000	199	662	10.2	31.4	–	–	–
[26]	60	540	1300	156	308	–	–	–
[278]	5000	–	610	–	–	1100	–	–
[279]	1500	–	500	–	–	1207	–	–
[280]	1000	150	1050	9.7	20.5	–	–	–
[281]	150	180	400	23	38	–	–	–
[282]	1000	167	300	7.5	16.9	–	–	–
[283]	2200	50	650	10.7	21.5	–	–	–
[284]	300	205	646	34	52	159	–	–
[285]	1500	150	646	–	–	1471	–	–
[286]	80	391	1260	200	33	–	–	–
[287]	700	325	1040	18	31	200	–	–

faced by different structures of these devices, which hinder the performance to be less effective in optimal applications. The recent and future trends of these devices are also discussed in the field of automation, advanced communication, bio-sensor-based devices etc. Finally, the whole concept is summarized in the last section to have the quintessence of these devices with a futuristic vision.

2. AlGaN/GaN HEMT architectures

GaN-based high electron mobility transistors are classified into 2 different structures: lateral structure and vertical structure. Vertical structures need GaN free-standing substrates, which are more expensive and smaller in size. The epitaxial growth of GaN along the gallium plane induces spontaneous and piezoelectric polarization effects. These effects create a high concentration of 2DEG, which is a 2-dimensional electron gas. Vertical devices can't harness the biggest benefits of 2DEG. Conversely, the lateral device can easily exploit the benefits [53,54]. Depletion-mode (normally-on) HEMTs have matured due to a simpler fabrication process. Enhancements in high performance devices led to advantages in power electronics and high frequency applications, including 1200 V cascode structure HEMTs. Nevertheless, these devices exhibit higher conduction, mobility with a high concentration of two-dimensional electron gas. There are still some challenges that have to be dealt with in these devices, such as current collapse, threshold voltage drift that persists under high voltage and high frequency applications. In comparison, enhancement-mode (normally-off) devices show greater advantages, e.g., lower static power consumption, simplified circuit design, and enhanced safety methods. Various methods, such as recessed gate structure, P-GaN cap insertion at barrier, cascode structure, ultrathin barrier structure, and fluorine ion implantation have been made to acquire this desire for the betterment of HEMT applications. Each of these structures is illustrated in Fig. 2.

Nowadays, research is focused on obtaining the E-mode devices for safe and reliable operation, which recessed gate structure successfully achieves normally-off operation by etching the AlGaN layer underneath the gate area, which depletes 2DEG. With the help of gate dielectric thickness modulation, this method can simplify the gate drive circuitry as well as control the breakdown voltage. However, this method faces some issues like balancing threshold voltage, on-resistance, as well as interface quality. Lin et al. utilized high temperature oxidation followed by the KOH wet etching technique to remove the AlGaN barrier layer to minimize damage and achieved higher threshold voltage and breakdown voltage, which is greater than 1000 V [55–57]. Asubar et al. and researchers at Sun Yat-sen University deposited barrier layer regrowth post etching, which showed a higher threshold voltage (V_{th}) of 3.5 V [58,59]. Im et al. utilized tetramethylammonium hydroxide (TMAH) for gate region etching, getting V_{th} of 3.5 V. Also, the tri-gate porous structure enhances breakdown voltage to 2000 V while maintaining high drain current [60]. These advancements highlight the necessity of precise gate controlling and optimizing the performance of metal-insulated semiconductor field effect transistor. There still exist some challenges with this method, like the complex circuitry, loss in dielectrics, which need to be solved.

The positively-doped GaN cap structure achieves normally off operation without etching or the insertion of dielectrics. However, instead of the Schottky contact inherent ohmic contact limits the

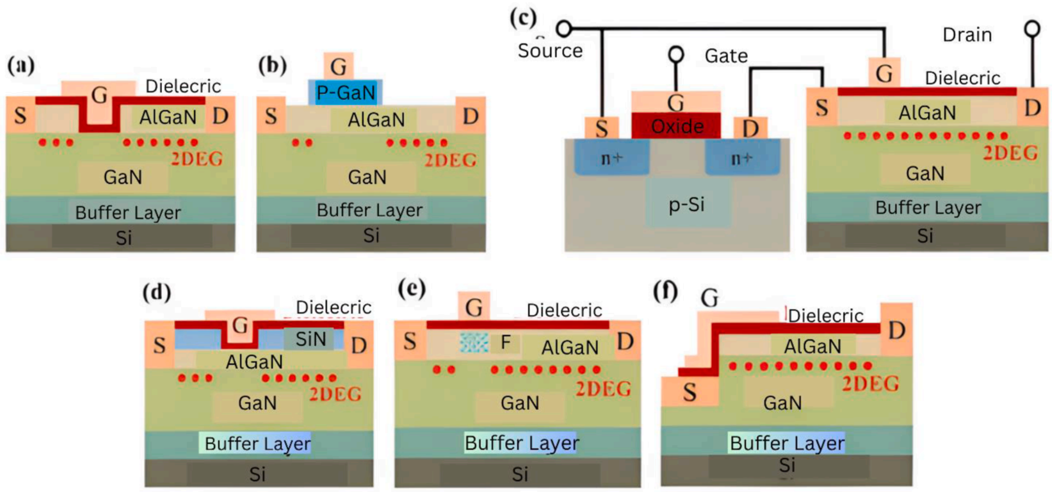

Fig. 2. (a) Confine recessed-oxide gate device, (b) P-GaN cap implantation on E-mode device, (c) E-mode device cascode configuration, (d) Deposition ultrathin-barrier layer structure, (e) Fluorine ion implantation gate structure, (f) Vertical gate structure (VG–HEMT) [55–57,61,65,66,68,70,71].

forward breakdown voltage (V_{br}) to around 6–8 Volts. Several strategies have been made, such as Schottky contacts or insertion of additional layers to optimize the forward (V_{br}) to 10 Volts. The inception of the increased distance between the gate metal and 2DEG channel by Uemoto et al. in 2007, where a V_{th} of 1 V and on-state current of 200 mA are demonstrated, researchers focus on optimizing the thickness of barrier (10–15 nm) as well as Al composition (15–20 %) to balance the 2DEG [61]. Efthymiou et al. reported effective gate depletion with a P-GaN cap whose concentration exceeds 10^{18} cm^{-3} [62]. Greco et al. discovered that the gate work function influences V_{th} and leakage currents when post-annealing with Ti/Al gates [63]. Lukens et al. introduced a gate-first self-formatted operation utilizing Mo as both the etching mask and gate metal, maintaining barrier integrity after annealing at 825 °C [64]. While P-GaN gate shows better compatibility with normally-off operation, there are still some issues which need to be solved, e.g., limited gate voltage swing which leads to gate leakage, threshold voltage instability, gate degradation under stress etc.

Cascode technology is utilized to implement a normally-off high electron mobility transistor with a small voltage Si-based enhancement-mode MOSFET in a common source, common gate configuration. This structure simplifies the gate circuit. Nevertheless, it has some disadvantages, such as increasing packaging complexity, susceptibility to parasitic inductance due to internal loops. These factors become an obstacle to the implementation of E-mode HEMT. For example, the cascode structure shows limitations with high frequency applications exceeding 1 MHz due to the Si MOSFET's lower electron mobility [65]. To mitigate these issues, researchers agree to replace Si MOSFET with SiC-based transistors. Devices like Transphorm's TPH3206PSB have commercially illustrated the feasibility of cascode configuration, offering 650 V operation in a TO-220 package. Despite these improvements, increased parasitic inductance and packaging complexity remain still unsolved.

There is a thin barrier scheme that induces from the recessed gate structure to make the device into enhancement-mode. Guo et al. explored GaN wafer creating AlGaN epitaxial growth around 4 nm. The in-situ remote plasma processing technique improved atomic layer deposition, which was enhanced on the gate region near SiN_x gate dielectric deposition [66]. It facilitates the enhancement-mode operation in AlGaN/GaN HEMTs by reducing the 2DEG concentration. However, this reduction can compromise other performance behaviors like maximum drain current, transconductance, sub-threshold voltage swing, and breakdown voltages. Huang et al. implemented $SiON/Al_2O_3$, multilayer gate dielectrics in an ultrathin barrier, which achieves a breakdown voltage of 700 V [67]. Luan et al. used PEALD-AlN and LPCVD-SiN_x passivation layers to restore 2DEG density, which achieves a breakdown voltage over 700 V, a max I_d of 2.5 Ampere, and an excellent positive bias temperature instability (BTI) performance [68]. The fluorine ion implantation in the barrier can make E-mode HEMTs. In 2005, Cai et al. explored the fluorine gate structure and used thermal annealing to improve the device performance. The threshold voltage increased to 0.9 V by using this approach [69]. Huang et al. explored a two-step fluorine plasma treatment to induce negative charges into both the AlGaN barrier and the Si_3N_4 dielectric layers. This approach effectively modulates V_{th} of AlGaN/GaN HEMTs by depleting the 2DEG to make the device normally-off [70]. The normally-off process of a high electron mobility transistor can also be done by utilizing a vertical gate device. As the vertical structures can't properly exploit the benefit of 2DEG, this device exhibits a higher threshold voltage. This structure was given by Huang et al. at the Dalian University of Technology. This device showed a V_{th} of 3.1 V and an improved dynamic on-resistance of 0.53 milliohms cm^2 [71].

Various advancements have been made in GaN to increase breakdown voltage. One of the reasons the early breakdown voltage happens is because of non-uniform electric field distribution and gate leakage. The vertical distance from top to substrate "breakdown" confines the V_{br}. Ohmic contacts on the source/drain are a severe design feature that may cause early breakdown. Schottky contact is utilized to modulate the electric field in the vicinity of the contacts. Lian et al. proposed a complex ohmic Schottky drain device square gate using a Si substrate in Fig. 3(a) [72]. This structure is estimated to mitigate surface traps and gate leakage. The extended gate length and Schottky contacts over metallic ohmic contact can necessitate on AlGaN/GaN device. Traps at the surface of the channel become an issue of leakage loss. B. Song et al. [73] demonstrated an AlGaN/GaN device utilizing a silicon substrate processing epitaxial grown non-alloyed ohmic contacts, achieving ultralow leakage currents and enhanced contact performance in Fig. 3(b). This structure was evaluated against a conventional device employing alloyed ohmic contacts [Fig. 3(c)]. The 2000 nm gate length is used for both of the structures. Low on-resistance (R_{on}) is also necessary for better transconductance as well as output current. To ensure lower R_{on}, a heavily Si-doped n^+ GaN layer was grown using molecular beam epitaxy is employed. AlGaN/GaN HEMTs fabricated using silicon substrates with regrown non-alloyed ohmic contacts exhibit enhanced performance, including reduced leakage and increased breakdown voltage, compared to devices with conventional alloyed contacts. H. Yoon et al. explored a WHDB T-gate structure with a gate length of 170 nm using a Si substrate [Fig. 3(d)] [74]. This gate structure showed lower noise performance, and a standard field plate reduced the surface trap effects despite having

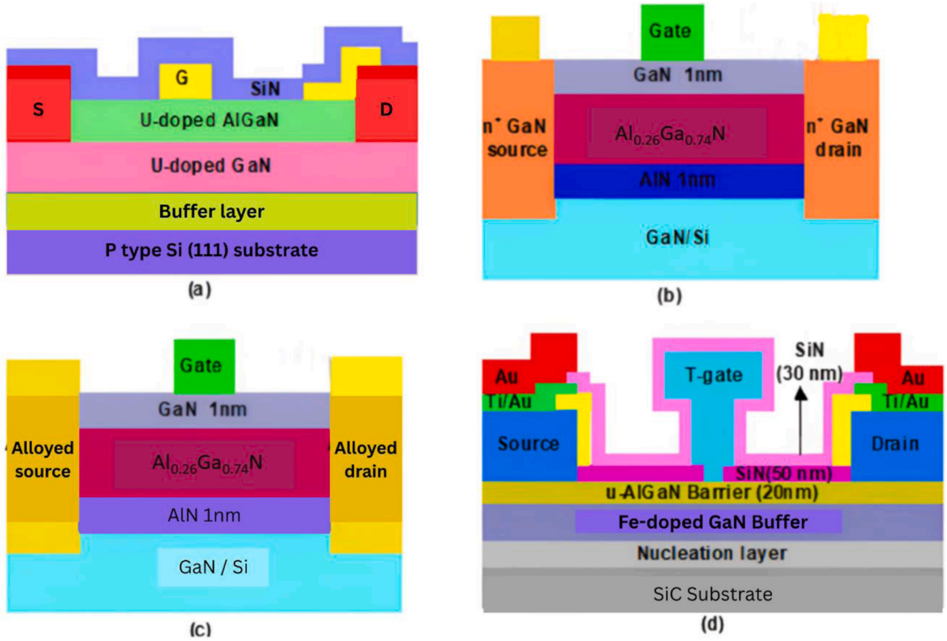

Fig. 3. (a) AlGaN/GaN Structure on Si substrate utilizing a hybrid ohmic-Schottky drain configuration (b) AlGaN/GaN Structure on Si substrate employing n⁺ GaN source/drain regions, (c) AlGaN/GaN Structure on Si substrate utilizing alloyed source and drain contacts, (d) AlGaN/GaN Structure using Si substrate featuring a wide-head T-gate design [72–74].

a large gate area.

Higher f_T and V_{br} are the two crucial metrics of RF microwave electronic devices. To meet this demand, L. Yang et al. proposed a TiN source layer to get a lower R_{on} in Fig. 4(a) [75]. This structure displayed a gate length of 200 nm with higher transconductance, cut-off frequency (f_T), and breakdown voltage. C–Y Chang et al. described a fully transparent drain to source length of 3000 nm. Indium tin oxide is utilized to work in the role of an electrode instead of the traditional alloyed metals [Fig. 4(b)] [76]. To get the enhanced power-added efficiency, RF devices are mandatory for optimal performance at medium and low bias voltages, ensuring optimal performance and energy conservation. To demonstrate the differences between the microwave and high-frequency equipment, Y. Zhou et al. developed a conventional structure [Fig. 4(c)] and an InAlN/GaN heterojunction with significant polarization effects. [Fig. 4(d)] [77].

H. Chiu et al. [78] fabricated a positively-doped GaN cap AlGaN/-GaN device with an extended gate length, exploring a novel complete etching operation with an AlN stop layer, which achieved uniform R_{on} and reduced surface leakage [Fig. 5(a)]. Moreover, this structure showed a great transconductance with a higher cut-off frequency. In the

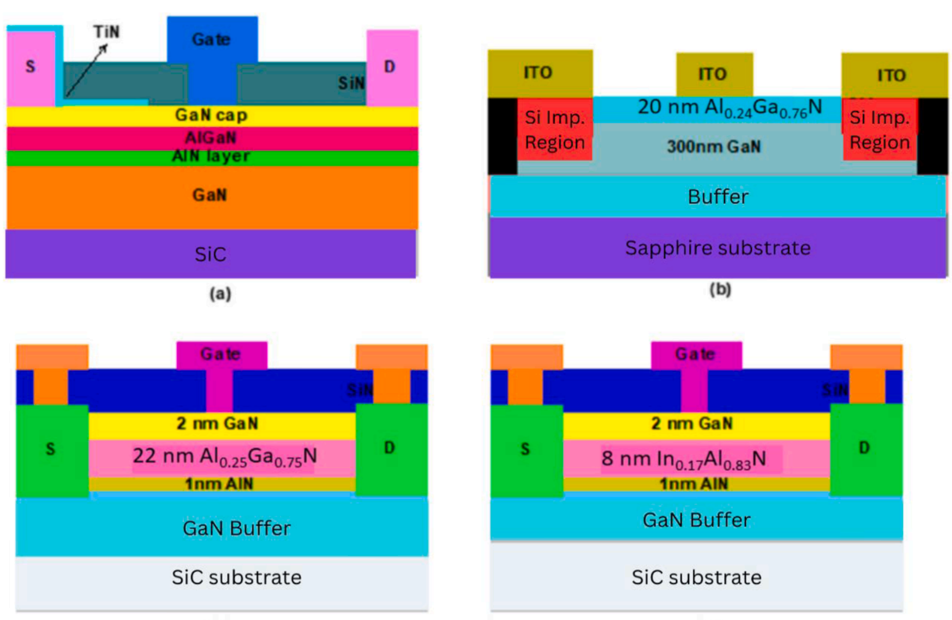

Fig. 4. (a) AlGaN/GaN device using SiC substrate with SiN passivation and TiN based source layer, (b) Completely transparent AlGaN/GaN device using Sapphire incorporating an ITO/n-GaN contact mechanism, (c) T shaped gate incorporating on AlGaN/GaN HEMT with SiC wafer, (d) InAlN/GaN HEMT fabricated on SiC substrate with T shaped gate [75–77].

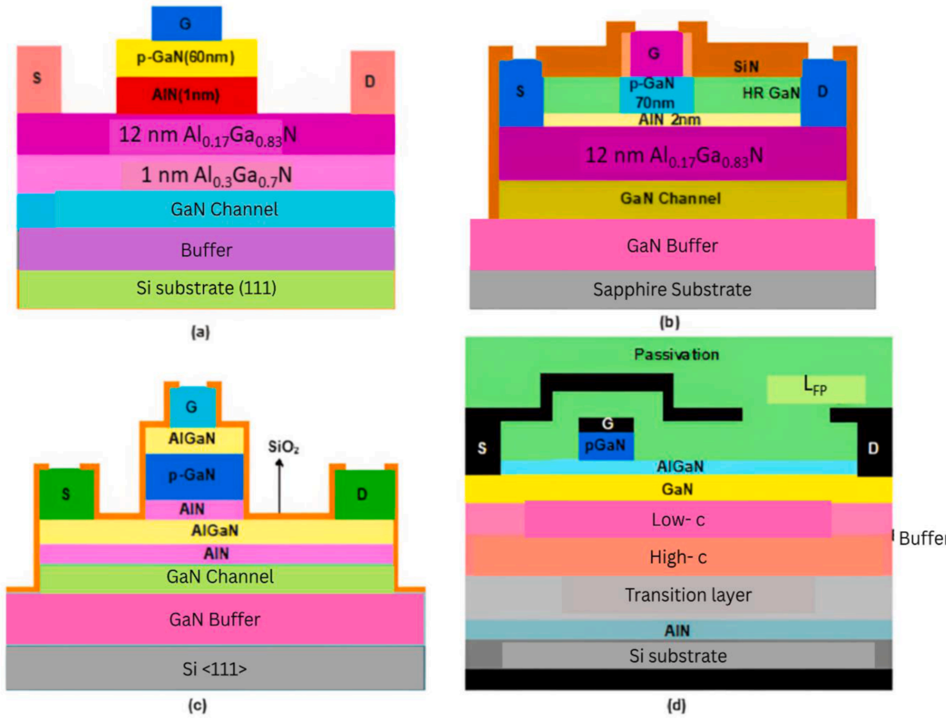

Fig. 5. (a) P-GaN cap AlGaN/GaN device using AlN etching stop layer, (b) P-GaN cap AlGaN/GaN device with Elevated Resistive (ER)-GaN channel, (c) P-GaN cap device with dual junction on Si substrate, (d) P-GaN cap AlGaN/GaN device using source/drain field plates [78–81].

same manner, Liu et al. [79] proposed a positively-doped GaN cap AlGaN/GaN device with high resistive GaN formed wherein oxygen plasma treatment was applied to increase the resistivity as well as an AlN interlayer to hinder oxidation of the AlGaN layer [Fig. 5(b)]. This structure enhanced the output as well as the transfer characteristics with lower leakage and higher breakdown voltage. In the same manner, C. Liu et al. [80] introduced a dual junction P-GaN gate AlGaN cap layer at the top to serve as both a barrier and depletion region [Fig. 5(c)]. This enhances the gate reliability and off-state breakdown voltage. A. Minetto et al. [81] proposed a drain field plate for semi-ON degradation. An extended field plate helps the surface trap in the vicinity of the drain region [Fig. 5(d)].

Daniel et al. developed an AlGaN/GaN high-electron-mobility transistor (HEMT) operating in enhancement mode by integrating a piezo-neutralization layer (PNT) ($Al_{0.07}Ga_{0.93}$ N) to increase threshold voltage [227]. The device, combining a T-shaped gate design with controlled gate recess etching, is shown in Fig. 6(a). When testing two recess depths, the 0.015 mm configuration outperformed traditional designs, delivering 370 mS/mm transconductance (twice conventional values) and a + 0.3V threshold voltage while maintaining low on-resistance **(R_{ON} = 0.00269 Ω).** This approach improved switching characteristics without sacrificing power efficiency. Xiaotian et al. presented a p-GaN normally-off AlGaN/GaN HEMT incorporating a hybrid-source configuration and an integrated reverse-conducting Schottky Barrier Diode (SBD) [250] as shown in Fig. 7. The device utilizes a decoupled AlGaN/GaN double-channel architecture with an inter-channel spacing exceeding 80 nm. The Hybrid-Source design enables the decoupling of reverse conduction characteristics from the forward threshold voltage, thereby achieving reduced reverse conduction losses while maintaining a high forward threshold voltage.

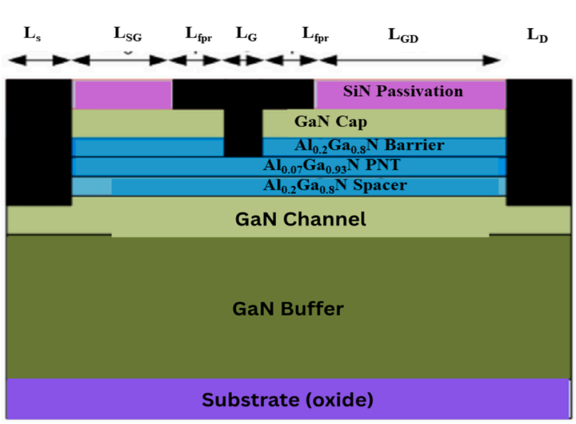

Fig. 6. Structure of AlGaN/GaN HEMT with PNT layer [227].

Successful integration of superconducting Nb gate electrodes to AlGaN/GaN heterostructures and HEMTs, as shown in Fig. 8(a) for low noise cryogenic applications has been reported, where Nb gates show significantly reduced gate resistance (R_g) below critical temperature [288]. Chiu et al. investigated a high power added efficiency (PAE) p-GaN gate HEMT as shown in Fig. 8(b), employing a high/low Mg doping profile in conjunction with an ohmic-gate design [251]. The inclusion of the ohmic gate facilitates hole injection into the channel without relying on the Poole-Frenkel (PF) emission mechanism, thereby enhancing gate-to-channel modulation capability. Additionally, the combination of low Mg-doped p-GaN and the AlGaN heterostructure effectively reduces gate capacitance, which contributes to improved radio-frequency (RF) performance under high power swing conditions.

A numerical simulation study has been conducted on HEMTs incorporating an InGaN channel on a β-Ga_2O_3 substrate to evaluate device performance [260]. The HEMT, as shown in Fig. 9, utilizing an InAlN barrier, exhibited enhanced drain current density and more stable transconductance compared to its AlGaN barrier counterpart. These improvements are attributed to the formation of a deeper quantum well and an increased interface charge density within the channel. The proposed devices demonstrated excellent RF characteristics, indicating the potential of InGaN channel HEMTs on β-Ga_2O_3 substrates for future high-performance RF power amplifiers in wireless communication and radar applications. Various structures of GaN HEMTs are demonstrated

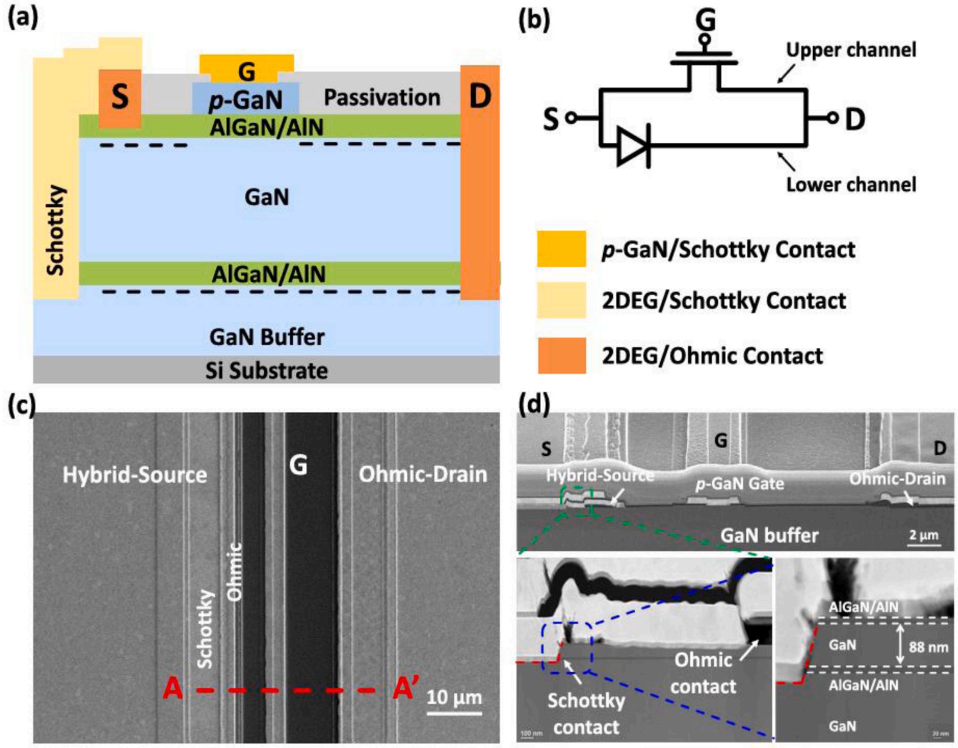

Fig. 7. (a) Structure of decoupled double channel p-GaN gate AlGaN/GaN HEMT, (b) equivalent circuit of the Hybrid-Source double-channel p-GaN gate HEMT based on a decoupled double-channel epitaxial structure, (c) Top view of the HS DC—HEMT, (d) Cross-sectional SEM image along A-A' and TEM images of the Hybrid-Source structure [250].

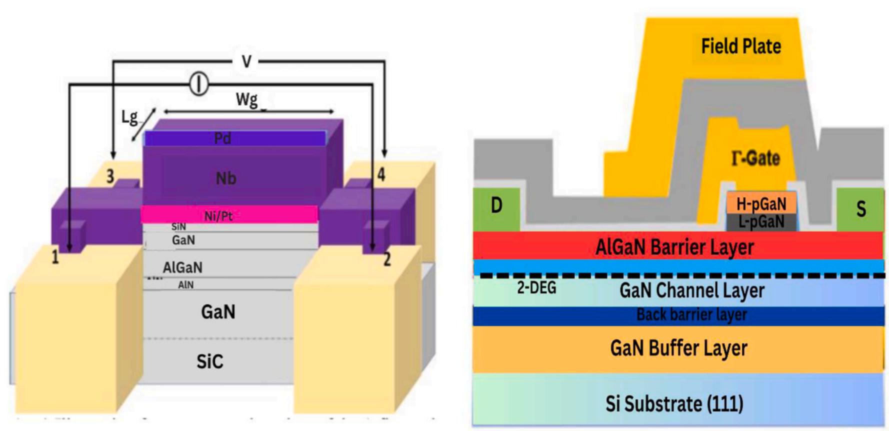

Fig. 8. (a) AlGaN/GaN HEMT with Nb gate electrodes [288], (b) High power added efficiency (PAE) p-GaN gate HEMT [251].

in the architecture section, which is essential to know about the merits and demerits of these structures. To summarize the advantages and limitations of each structure, Table 2 is given to address those metrics.

3. Emerging materials for AlGaN/GaN HEMTs

AlGaN barrier with Al concentration pushes towards high power & high frequency applications. But the excess concentration of Al in AlGaN deteriorates the lattice structure quality by a great margin. W. Wang et al. [82] resolved this issue by introducing InAlGaN barrier material & observing how that impacts the DC & RF operation. Fig. 10(a) & 10(b) show how transconductance (g_m) & I_d enhance in InAlGaN/GaN as compared to traditional AlGaN/GaN HEMT. Later, to improve the output power in the lower voltage range by keeping R_{on} within a reasonable limit, Y. Zhou et al. explored an InAlN/GaN heterostructure that improves g_m & I_d as compared to conventional Ag-HEMT [83]. Fig. 10(c) & 10(d) clearly show the improvement in g_m & I_d. The breakdown voltage in GaN HEMTs tends to drop due to high gate leakage, mainly from tunneling through the thin InAlN barrier [84]. Still, InAlN-based devices show promising performance with lower knee voltage, higher drain current, and reduced on-resistance, which makes them a strong candidate for future low-voltage, high-efficiency applications. The effects of AlGaN and InAlN on gate leakage & I_d are shown in Fig. 11(a) & 11(b) respectively. When operated at high drain bias, these devices experience self-heating from increased electric fields and electron scattering [85], but using a diamond substrate helps dissipate heat more effectively than silicon [86]. This results in improved DC and RF performance, especially under continuous wave operation.

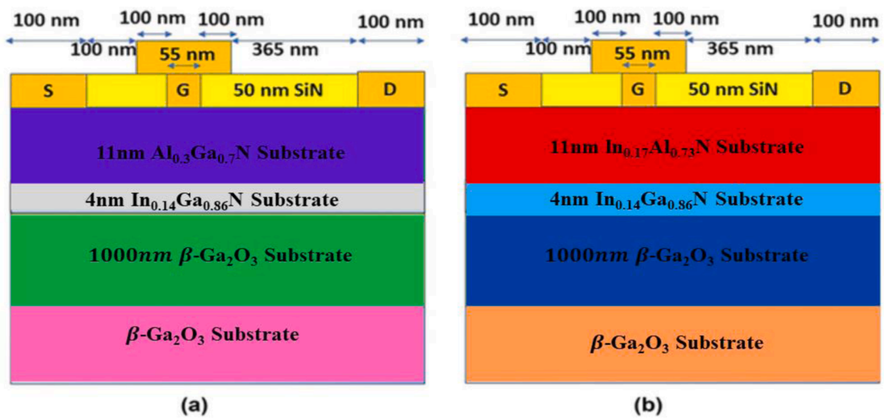

Fig. 9. Device structures of (a) AlGaN/InGaN HEMT and (b) InAlN/InGaN HEMT [260].

Additionally, using non-alloyed contacts through n^+ GaN regrowth lowers contact and sheet resistance, which leads to better overall device performance. The effect of substrates on output & alloyed/non-alloyed contact on G_m has been shown in Fig. 11(c) & (d).

Fig. 12(a) & (b) depict the effects of Alloyed/Non-Alloyed contact on I_d vs V_{gs} & I_d vs V_{gs} respectively, where non-alloyed contact shows improved performance. Fig. 13(a) shows how the current changes with gate voltage for both SG-HEMT and DG-HEMT devices when the drain voltage is fixed at 5 V. The SG-HEMT turns on at a gate voltage of about 1.07 V, while the DG-HEMT turns on at around 1.02 V or 1.12 V, depending on whether the auxiliary gate (GR) is set to 0 V or +1 V. In the DG-HEMT, the main gate (GL) controls the switching, and the auxiliary gate helps maintain charge in the channel. Although both devices should ideally have the same threshold voltage when GR is at 0 V, small differences in the manufacturing process can cause slight variations. Fig. 13 (b), (c), and (d) show how the current behaves with increasing voltage. The DG-HEMT has a lower maximum current compared to the SG-HEMT, mainly because the auxiliary gate slightly restricts the flow of electrons. However, the resistance when the device is on (called R_{ON}) doesn't change much, which is important for power switching performance.

Appropriate gate trench interface treatment can significantly improve the device performance. He et al. used N_2O for interface treatment with an improved V_{th} & Sub-threshold swing [88]. Huang et al. demonstrated oxygen & fluorine mixed plasma interface treatment [89] that remarkably reduced the leakage current as compared to single oxygen plasma treatment, which is clearly depicted in Fig. 14(a). This technique also improves the transfer characteristics of the device owing to the presence of fluorine ions on the barrier layer surface that cause a positive shift of the threshold voltage, as shown in Fig. 14(b).

The materials used for the dielectric layer significantly affect the performance of HEMT devices. To address the issues associated with single layer dielectric, multilayer dielectric layers are developed. Al_2O_3/SiON multilayer dielectric approach used for fabrication of HEMT devices has been employed to navigate the breakdown characteristics of dielectric layer [90]. Fig. 15 clearly depicts that multilayer HEMT device shows better transfer characteristics.

Proper multilayer dielectric techniques can improve the electrical characteristics of HEMTs at a staggering pace. Further investigation on the effect of SiON on multilayer dielectric has been performed using three samples as shown in Fig. 16(a) & 16(b), where gate breakdown and breakdown characteristics have been displayed. It's quite evident that SiON has a better critical breakdown field [90]. Yusuf et al. presented an enhancement-mode p-type Mg-doped $In_{0.2}Ga_{0.8}N$ cap gate double-heterojunction high electron mobility transistor (DH—HEMT) optimized for high-efficiency, low-loss boost converter applications [87]. The device exhibited significantly improved dynamic on-resistance (R_{ON}), superior off-state breakdown voltage ($V_{BR, OFF}$), and remarkably reduced gate-to-drain leakage currents compared to conventional GaN buffer structures. Mohanbabu et al. conducted a theoretical study on $Al_{0.23}Ga_{0.77}N/GaN/Al_xGa_{1-x}N$ DH—HEMTs incorporating a boron-doped GaN cap under the gate [119]. The B-doped cap effectively reduced leakage current and carrier trapping, while improving subthreshold swing, I_{ON}/I_{OFF} ratio, and $V_{BR, OFF}$, all while maintaining a positive V_{th}. These findings suggest the structure's potential for high-power, normally-off motor drive electronics. High-performance III-nitride MIS-HEMTs employing a high-κ $HfAlO_x$ gate insulator with a graded barrier architecture demonstrate remarkable enhancements in I_{DS}, threshold voltage (V_{th}), transconductance (g_m), and breakdown voltage ($V_{BR, OFF}$), while effectively suppressing drain leakage, making them highly suitable for high-power boost converter applications [154]. As research progresses, emerging materials promise to enhance the performance, efficiency, and scalability of AlGaN/GaN HEMTs, pushing the boundaries of high-power and high-frequency applications.

4. State-of-the-art

4.1. Power devices

Numerous research studies are ongoing on GaN HEMTs for the betterment of performance, as wide bandgap materials like GaN, B-Ga_2O_3 have been top choices in the power electronics industry. Power devices with wide bandgap material like GaN have far better performance with higher efficiency & temperature tolerance, lower leakage current, along with high switching speed as compared to Silicon [117, 118,137]. The formation of 2DEG occurs at the interface between AlGaN & GaN layers, which improves the electron mobility significantly, was first shown by Khan et al. in 1993 [19]. Since then, eye-catching progress has been observed in the development of GaN HEMTs for high power applications [120,121,138,139,148–150].

Power transistors based on GaN have two types of structures: lateral & vertical structures. Normally off HEMTs (Enhancement mode) are required for improved device performance. When a p-type GaN layer is added to the AlGaN/GaN HEMT shown in Fig. 17(a), it becomes a p-GaN E-mode HEMT, as seen in Fig. 17(b). Based on reviewed studies, there are different variations of p-GaN devices [124,129,153]. E-mode HEMTs can be achieved through fluorine ion implantation [122] that avoids dry etching & designing HEMT with a thin/ultra-thin barrier layer [122, 123]. The structures with fluorine ion implantation and thin/ultra-thin barrier layer are shown in Fig. 18(a) & 18(b). The recessed gate method appears to be another key technique to convert D-mode HEMTs into E-mode HEMTs through the reduction of thickness in the AlGaN barrier layer. GaN MOS or MIS HEMTs have attracted significant attention [125, 130,144,156], along with MISHEMTs that incorporate high-k gate dielectrics [132,133,147,157]. Compared to Schottky gate GaN HEMTs,

Table 2
Specifying advantages and limitations of various structures of GaN HEMT.

Structure	Advantages	Limitations
Recessed Gate	a) Simple gate drive circuit. b) Flexible dielectric thickness for better gate breakdown voltage. c) V_{th} can be adjustable up to 3.5 V.	a) Surface trap states due to etching damage. b) There is a trade-off between enhanced threshold voltage and dynamic on-resistance. c) Intricate interface treatment needed.
P-GaN gate	a) No need for gate dielectric. b) Simple and adjustable fabrication. c) Low leakage current with good dynamic performance.	a) The threshold voltage is limited to not >2 V. b) Etching damage outside the gate reduces 2DEG. c) Needs protection circuits to avoid gate current damage.
Cascode configuration	a) The gate driver design is simplified. b) High stability device. c) Uses well-established Si MOSFET technology	a) Parasitic inductance due to internal loops. b) Reduced high-frequency performance.
Ultrathin barrier	a) E-mode is easier to achieve due to lower polarization charge. b) Good frequency characteristics with high output current.	a) Lower breakdown voltage. b) Reduced electron mobility. c) Passivation in the interface is needed to recover 2 DEG and stability.
Fluorinated gate	a) Threshold voltage can be enhanced from negative to positive. b) E-mode achieved without mobility degradation with combined MIS.	a) Difficult to control fluorine ion distribution and uniformity. b) Fluorine can penetrate the GaN layer, reducing 2DEG mobility. c) Gate damage risks from implantation.
AG-HEMT on Si-wafer with Hybrid Ohmic-Schottky Drain (HO-SDS)	a) Lower gate leakage. b) Reduced trapping effect due to square gate configuration. c) Improved breakdown voltage due to the field plate.	a) Complexity in Schottky drain metal deposition. b) Dry etching is less favorable than wet etching damage.
AG-HEMT on Si-wafer with Non-Alloyed Ohmic Contacts (NAOCs)	a) Low leakage current. b) High ON/OFF current ratio with reduced subthreshold slope.	a) Regrowth process complexity. b) Requires precise surface shielding.
AG-HEMT on Si-wafer with Alloyed Ohmic Contact	a) Enhanced contact technique. b) Simple and finer fabrication than growth.	a) High-temperature alloying causes surface traps. b) Larger subthreshold slope. c) Higher gate leakage.
AG-HEMT on SiC wafer with Wide-Head-Double-Deck (WHDD) T-gate	a) Improved noise performance. b) Reduced gate resistance and parasitic capacitance.	a) Large gate area complexity. b) High epitaxial growth and processing complexity. c) Precise gate footprint fabrication required.
TiN-based Source Ledge AG-HEMT on SiC wafer	a) High transconductance and cut-off frequency. b) High breakdown voltage. c) Low source resistance due to TiN source ledge.	a) Fabrication is high maintenance. b) High cost for complexity in the TiN layer.
AG-HEMT on SiC wafer with T-shaped gate (AlGaN/GaN)	a) Good RF performance. b) Higher concentrated 2DEG.	a) Moderate polarization effect. b) Gate design complexity due to the T-shape.
InAlN/GaN HEMT on SiC wafer with T-shaped gate	a) Strong polarization effect due to InAlN barrier. b) Enhanced RF performance.	a) More complex material growth. b) Potential challenges in barrier layer uniformity.
P-GaN gated AG-HEMT with High Resistive (HR) GaN layer	a) Lower drain leakage with higher on/off current ratio. b) Less current collapse. c) Higher breakdown voltage.	a) Requires oxygen plasma treatment and an AlN barrier layer. b) Fabrication complexity.
P-GaN AG-HEMT with Drain Field Plates (S/D FPs)	a) Provides insights into semi-ON degradation. b) Ability to optimize the drain FP length to manage hot electron trapping.	a) Longer drain FP leads to faster and severe drain current degradation due to hot electron trapping. b) Trade-off between field plate length and reliability.

MIS HEMTs provide benefits like reduced gate leakage and a wider gate voltage swing [158]. A 2DEG resistor-based methodology, combined with a design of experiment (DOE) approach, was used to assess dispersion in three buffer types: step graded, LT AlN interlayers, and superlattices. This enabled identification of the physical origins and key buffer regions affecting 2DEG dispersion [128]. Numerous AlGaN/GaN heterostructure MIS-HFETs have been developed to enhance dynamic behavior and overall device performance [134,135,146,151,152].

Performance of GaN HEMTs is affected by the source field plate, enhancing the breakdown voltage, where the longer field plate has been observed to produce better performance than a short one. However, field plates affected by dielectric layer need to be optimized in terms of length for different device architectures [92,93]. Furthermore, super field plates, in comparison to other charge balance techniques, provide much better performance in LDMOS without using the drift region, along with the eradication of longstanding issues in charge balancing [94–96]. An n-type LDMOS with three super field plates has been shown in Fig. 19(a). Li et al. demonstrated a p-GaN buried layer with a field plate into a composite stepped gate as shown in Fig. 19(b) that exhibits excellent progress in the reduction of leakage current and modification of electric field [97,98]. A p-GaN gate device with a BHSC, as shown in Fig. 20, depicted by Yang et al., confronted the issue of dynamic R-on degradation [99–102].

Use of TaN as the gate contact material in the development of normally off p-GaN HEMTs exhibits impressive threshold voltage with outstanding gate stability & reliability [103–106]. Inclusion of AlInN/AIN/Gan double heterostructure with an INAlGaN back barrier pushed towards a low resistance device with enhanced DC performance & efficiency [107–110]. Trench engineering techniques, where the metal trench is in the buffer region lessen the trapping of channel carriers [111,112]. GaN HEMTs have wide applications in power electronics [143] and other technologies where large power handling is crucial. An innovative technique called regrowing GaN HEMTs over Mg-implanted layers has been projected by Döring et al. [113–116]. The epitaxial quality of materials affects the device performance. Proper optimization of the epitaxial layers [145] can greatly enhance device reliability [134]. Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) are commonly used in power electronics because of their excellent characteristics, including high breakdown voltage, fast switching speed, low on-resistance, and thermal efficiency. Table 3 presents the key applications of GaN HEMTs power devices.

The AlGaN/GaN HEMT power device market is poised for sustained growth, fueled by the electrification of transportation, renewable energy adoption, industrial automation, and advanced telecommunications. AlGaN/GaN HEMTs remain the dominant technology and are expected to expand the market further as technology matures and costs decline. Through a thorough study of the reviewed references [243–246], a pie chart has been depicted in Fig. 21 to illustrate the relative contributions of GaN HEMTs across various application sectors. This visual representation highlights the dominant and emerging areas of application for GaN HEMTs power devices. Researchers across the globe are putting

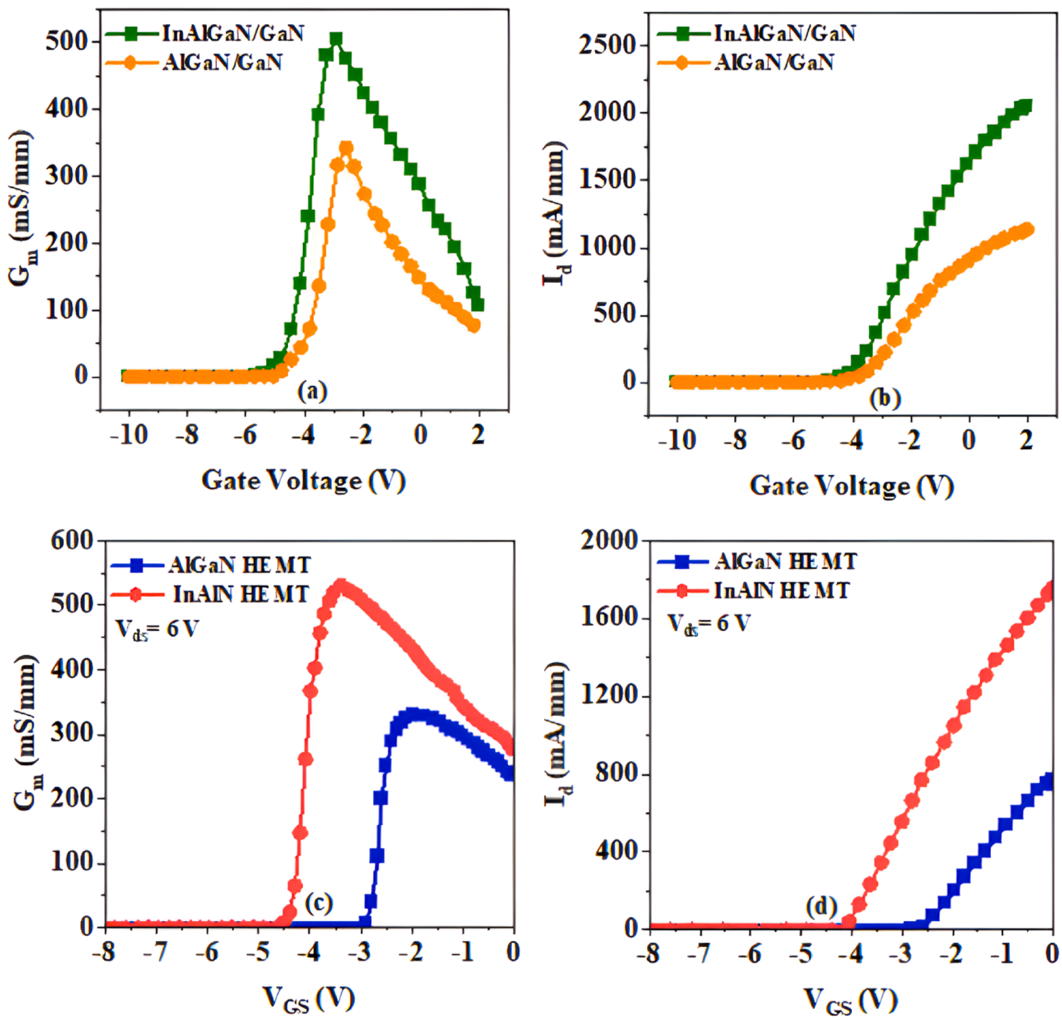

Fig. 10. (a) & (b) G_m/I_d vs Gate voltage for InAlN & AlGaN [82]. (c) & (d) G_m/I_d vs V_{gs} for InAlN & AlGaN [83].

enormous effort into the innovative design of GaN HEMTs to develop architectures that will improve performance at a staggering pace.

4.2. RF devices

GaN HEMTs are extensively employed in RF devices as they have superior electron mobility due to their wide bandgap. They have added new dimensions in RF electronics with improved thermal management & power efficiency. Ti/Au/Al/Ni metallization stack with shallow trench etching ohmic contact in GaN HEMTs, as shown in Fig. 22, described by Lu et al., significantly reduced the contact resistance with a smooth surface morphology [160–162]. Controlling surface morphology is of high importance for the long-term reliability & improved performance. He et al. achieved a remarkable cut-off frequency f_T/f_{max} at 190/301 GHz fabricating GaN HEMT on sapphire, which was a significant breakthrough [163–165]. Yadav et al. demonstrated the Utilization of GaN-on-QST, which has been a tremendous achievement in RF HEMT fabrication that opened a new door for substrate engineering with improved thermal management & RF device performance. AlGaN/GaN structure on QST has been shown in Fig. 23(a) and (b). RF applications significantly require low-noise amplification. Tungsten gate metal and CMOS contacts for source/drain terminals achieved a remarkably low noise amplification at re of 0.9 dB, having a gain of 12.8 dB at 2 GHz [166–168]. RF switch model introduced by Bansal et al. extends applications of GaN-based RF switches in telecommunication industries & others [169]. Hsieh et al. showed the GaN HEMTs device performance with varying AlGaN back barrier thickness as depicted in Fig. 24.

Researchers have designed dual-gate AlGaN/GaN HEMTs, which show a significant enhancement in RF linearity, improving by 5.9 dB over traditional single-gate designs [171]. MEC has established a stable operating range for GaN MISHEMTs in RF power amplifiers, effectively tackling the issue of positive bias instability. This progress helps in developing reliable GaN-based power amplifiers, making them suitable for use in 6 G handset applications [172]. Recent studies have concentrated on Ku-band GaN HEMT high-power amplifiers (HPAs), highlighting their current development status and key technical challenges.

A more advanced nonlinear model for GaN HEMTs has been introduced, which includes self-heating effects to improve the precision of DC simulation results [173]. A robust Pareto-based design method has been developed for choosing GaN HEMTs, especially for power and low-noise amplifier applications in 5 G systems. This approach considers multiple factors, such as output power, efficiency, and junction temperature, to identify the best design trade-offs [174].

5. Reliability issues in GaN HEMT

While GaN-based HEMTs offer extraordinary performance in high-power and high-frequency applications, some unique reliability issues have to be faced compared to Si or SiC devices [175]. These issues encompass threshold voltage instability, gate leakage, trapping effects, hot carrier degradation, self-heating, and off-state breakdown. Comprehending and addressing these reliability concerns are essential for

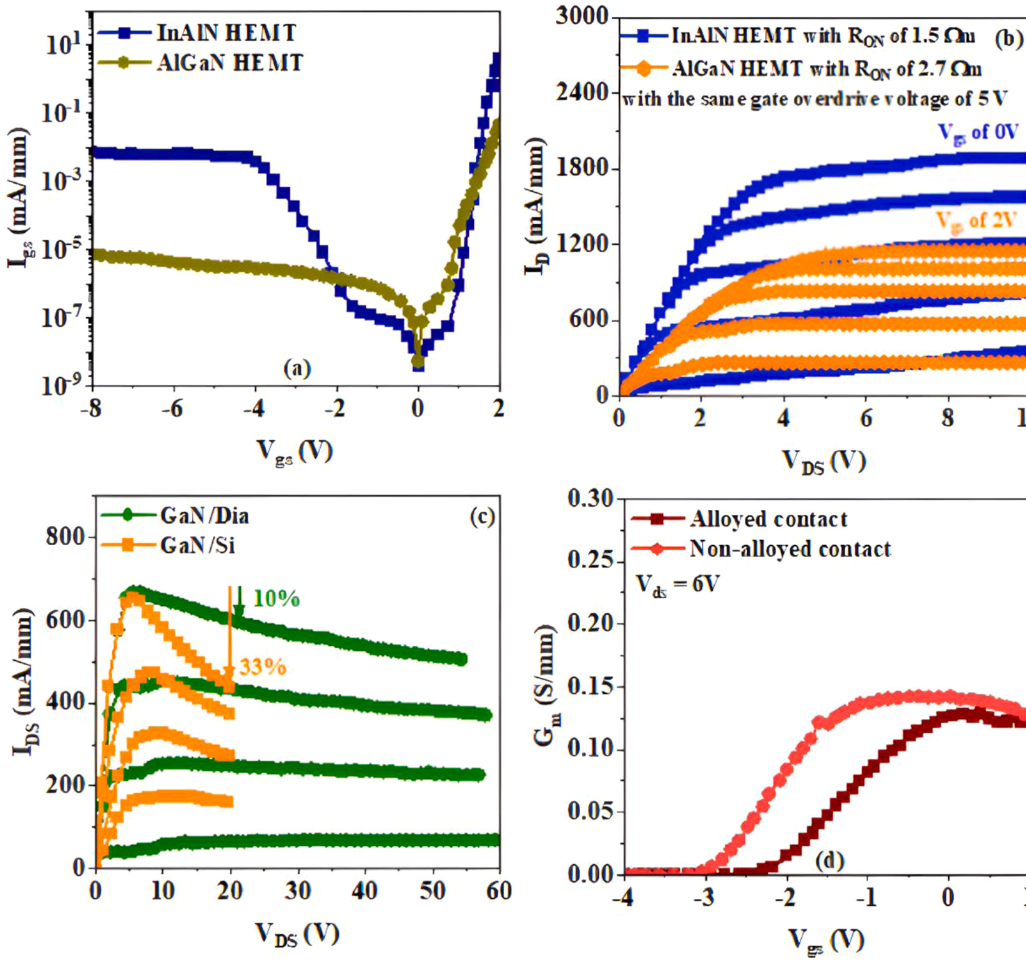

Fig. 11. (a) & (b) The effects of AlGaN and InAlN on gate leakage & I_d (c) I_{DS} vs V_{DS} for different substrates [86] (d) G_m vs V_{gs} for alloyed/non-alloyed contact [73].

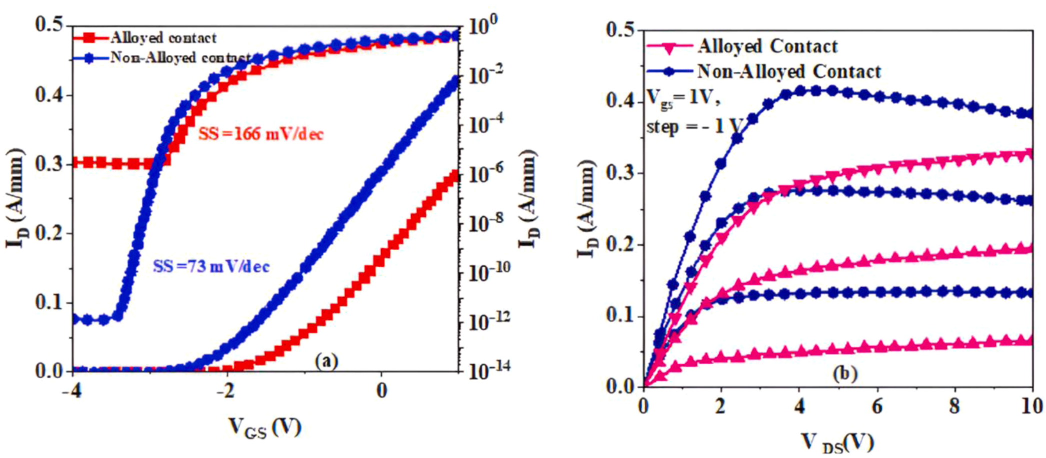

Fig. 12. (a) I_D vs V_{GS} for alloyed/non-alloyed contact [73], (b) I_D vs V_{DS} for alloyed/non-alloyed contact [73].

the widespread commercial adoption of GaN technologies.

5.1. Threshold voltage instability

One of the most critical issues is threshold voltage instability, which is primarily attributed to defects in the AlGaN barrier, structural variations in the p-GaN gate, and charge trapping at the gate interface. During prolonged operation under bias or temperature stress, both negative and positive V_{th} shifts can occur, largely due to trapped charges at the surface or within the GaN buffer, as illustrated in Fig. 25 [176, 289]. A negative V_{th} drift can lead to unintended partial conduction of the device, whereas a positive shift raises the on-resistance, thereby degrading switching performance. For example, in p-GaN gate HEMTs, the gate contact quality strongly influences V_{th} stability, where devices with higher gate leakage show negative shifts due to hole injection, and low-leakage designs can shift V_{th} positively [177].

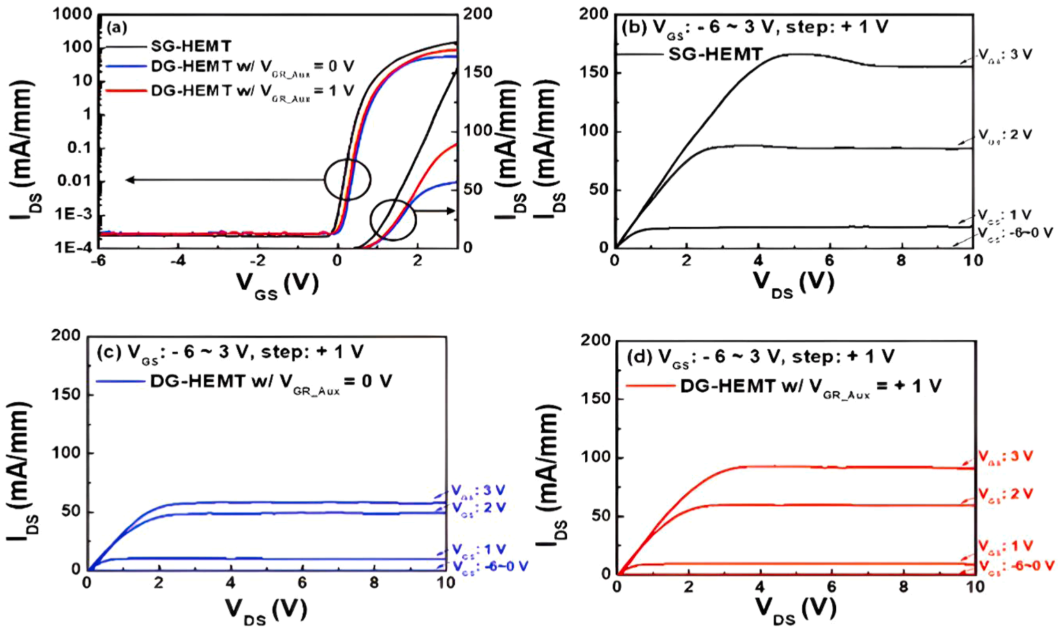

Fig. 13. (a) Shows the transfer characteristics (I_D vs. V_{GS}) of both an SG-HEMT and a DG-HEMT using a setup where the main gate (GL) is used to control the device and the auxiliary gate (GR) is biased at either 0 V or +1 V [91].(b), (c), and (d) present the output characteristics (I_D vs. V_{DS}) [91]:(b) for the SG-HEMT,(c)for the DG-HEMT with the auxiliary gate at 0 V, and (d) for the DG-HEMT with the auxiliary gate at +1 V, all operating in forward conduction modes.

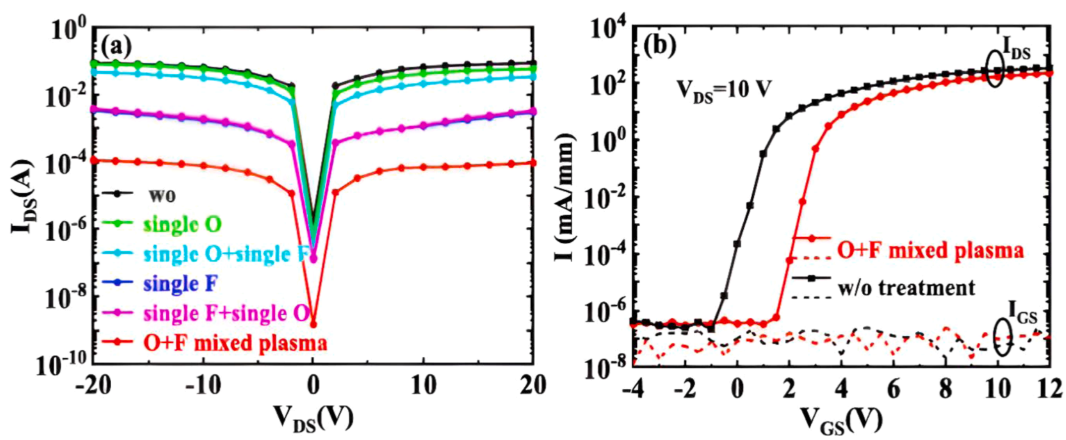

Fig. 14. (a) Leakage current characteristics of device for different plasma treatment, (b) Transfer characteristics of devices before and after mixed plasma treatment [89].

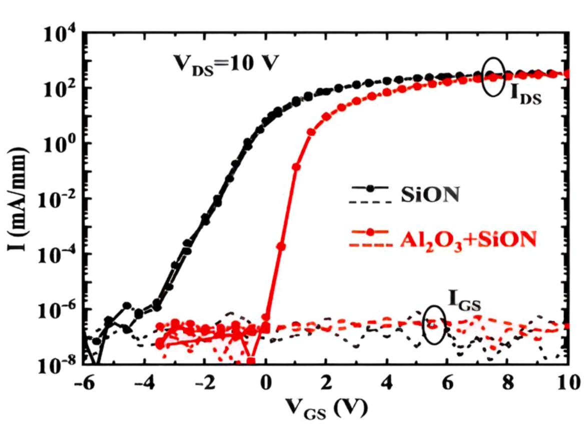

Fig. 15. Transfer characteristics of recessed-gate E-mode HEMTs with different dielectrics [90].

To mitigate threshold voltage instability in p-GaN gate HEMTs, a combination of material and structural strategies is applied. Surface passivation and optimized AlGaN barrier composition reduce charge trapping, while buffer layer adjustments lower defect density [106,290]. Improving gate contact quality through leakage control, suitable metal selection and refined geometry further enhances stability [292,293]. Structural measures like back-barriers and MIS gate designs improve channel control [294,295]. Additionally, managing temperature, limiting bias stress, and ensuring precise gate voltage contribute to long-term device reliability.

5.2. Gate leakage current

Closely related to threshold instability is the issue of gate leakage current, which becomes particularly problematic at high electric fields, especially in Schottky-gate HEMTs under reverse bias. In such devices, the Schottky contact can emit or tunnel electrons through various mechanisms, including thermionic emission [179], trap-assisted

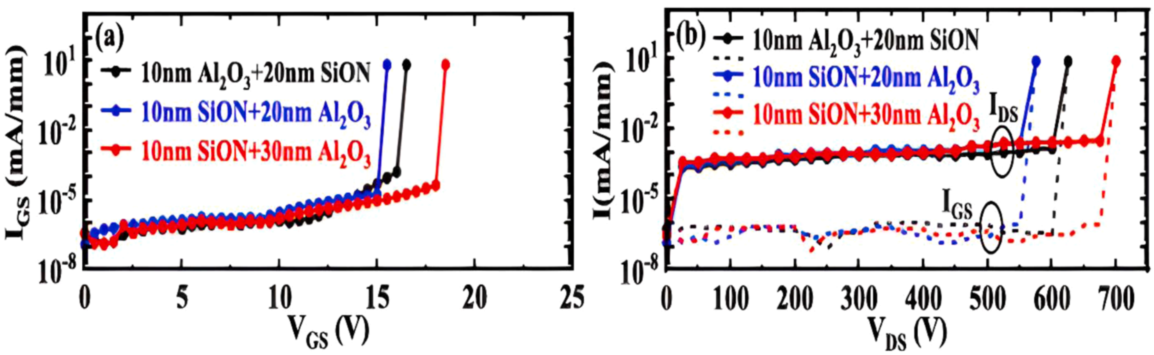

Fig. 16. (a) Gate breakdown and (b) off-state breakdown characteristics of different dielectric combinations [90].

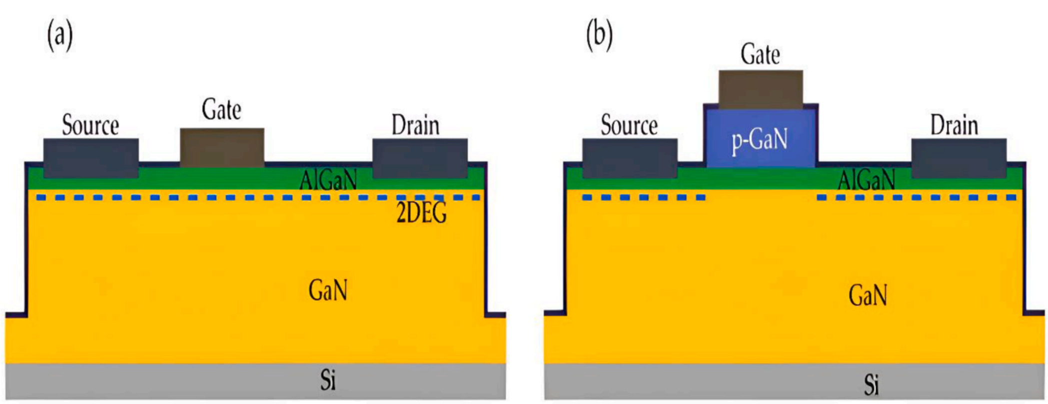

Fig. 17. Architecture of GaN HEMT, (a) Depletion mode HEMT and (b) Enhancement-mode HEMT(p-GaN) [159].

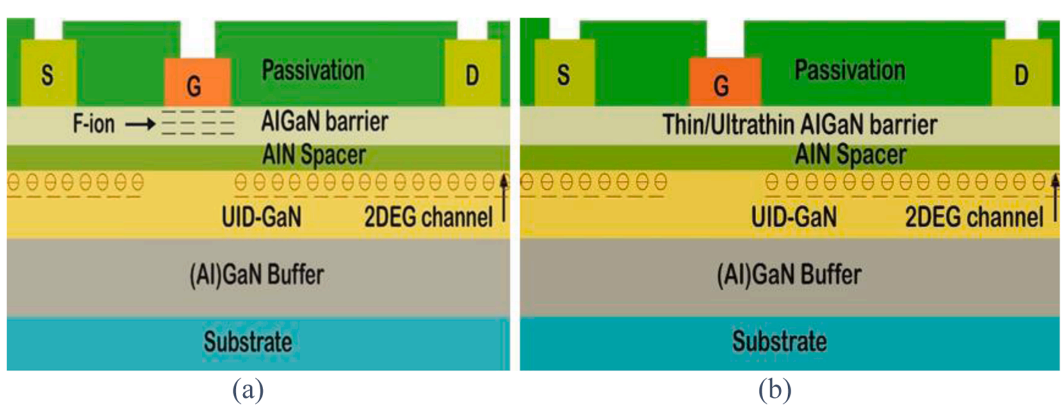

Fig. 18. (a) E-mode device with fluorine ion implantation [140], (b) E-mode device with thin/ultra-thin barrier layer [141,142].

tunnelling [180], dislocation-related leakage [181], Fowler–Nordheim tunnelling [182], defect hopping [183], and space charge-limited conduction [184]. Moreover, leakage current is typically caused by dielectric defects, improper gate biasing, and metal-barrier interactions. These leakage currents not only raise off-state power dissipation but also effectively lower the gate-to-drain breakdown margin. As the gate voltage increases, leakage typically rises, which can also elevate the noise figure (NF) and reduce power-added efficiency (PAE) [178]. Consequently, the recent focus on reducing gate leakage and stabilizing V_{th} is critical in the research of GaN HEMTs.

In response, recent efforts have focused on mitigating leakage through control of conduction mechanisms and structural refinement. Optimizing gate bias reduces tunnelling and emission, while high-quality dielectrics with low defect densities limit leakage paths [190, 296,297]. Interface defects are minimized through surface preparation, passivation, and careful material selection. Structural modifications, such as shorter gate lengths and improved channel design, further suppress leakage. Post-fabrication treatments like annealing and plasma processes enhance surface quality, and routine monitoring ensures consistent and reliable device performance.

5.3. Charge trapping and current collapse

The charge trapping effect is a significant concern, as it results in dynamic instabilities such as transconductance dispersion and current collapse. These effects are often seen in AlGaN/GaN HEMTs and happen when electrons get stuck in surface states or the buffer while the device is working, especially when there is a high drain voltage [186]. Fig. 26 provides a detailed illustration of different trapping mechanisms, including gate electron injection under negative gate bias, hot-electron

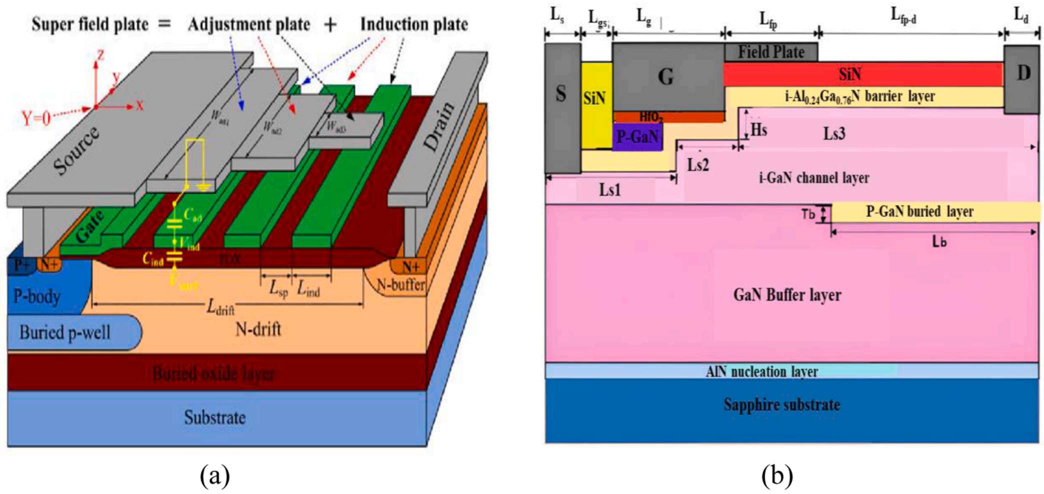

Fig. 19. (a) structure of n-type LDMOS with three super field plates [94], (b) composite stepped gate GaN device with p GaN buried layer and field plate [97].

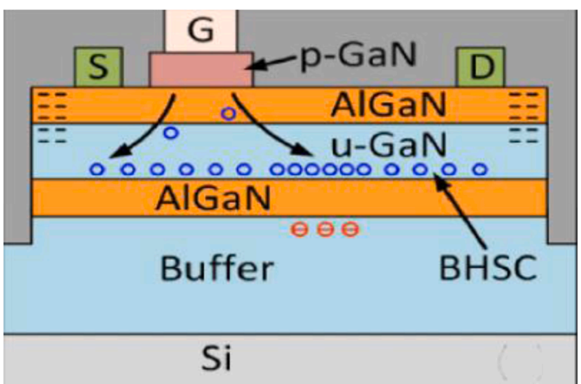

Fig. 20. P-GaN gate HEMT with buried hole spreading channel [99].

Table 3
A breakdown of key applications of GaN HEMTs power devices [99].

Application Area	Example	Benefits of GaN HEMTs
Power Supplies	SMPS, AC-DC converters	Higher efficiency, compact size
Electric Vehicles	OBC, Inverter, DC-DC converters	Weight reduction, improved range
RF/Microwave	Radar, 5 G base stations	High frequency and power handling
Renewable Energy	Solar inverters, wind turbines	High efficiency, better power density
Data Centers	Server power supplies	Lower cooling requirements, higher efficiency
Aerospace/ Defense	Drones, satellites, radar	Lightweight, reliable in harsh environments
Consumer Electronics	Phone chargers, audio systems	Compact, fast-charging, energy-efficient

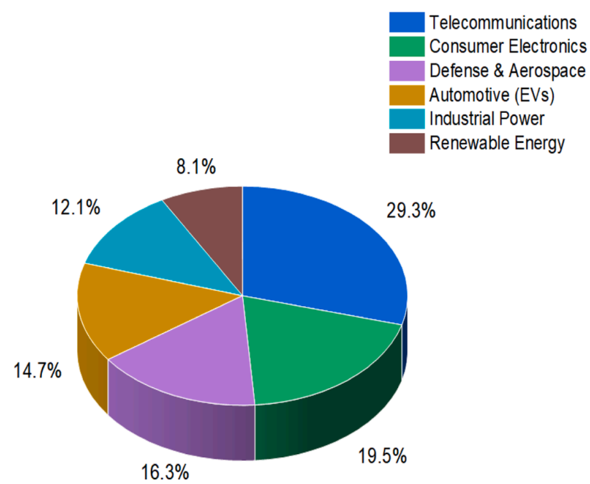

Fig. 21. Pie chart describing GaN HEMTs market share by applications.

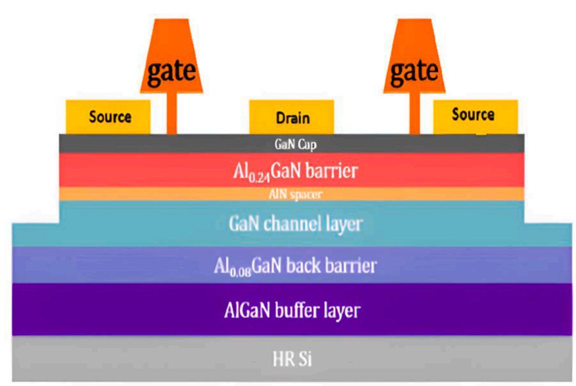

Fig. 22. AlGaN/GaN heterostructure with Ti/Au/Al/Ni/Au metal stack [160].

injection at high drain voltage, dislocation-induced deep-level traps, and donor-like surface states [185].

As a result of these trapping phenomena, dynamic effects such as gate lag and drain lag are frequently observed. These refer to the transient response of current at sudden changes in the gate and drain voltage, respectively [191,192]. This delay is introduced due to surface donor-like traps near the AlGaN surface and buffer traps [136], which store the electrons and release them gradually [193–195]. Specifically, gate lag is commonly associated with donor-like surface traps near the AlGaN barrier, while drain lag is primarily influenced by deep-level traps within the GaN buffer. When a strong negative gate voltage is applied, electrons can get trapped on the surface, which lowers the 2DEG density by acting like a "virtual gate" [196–201], while a high drain voltage can fill deep traps in the buffer with energetic electrons, affecting the device's performance until those charges are released [202–204]. These trapping-induced transient effects not only limit RF performance, like causing power “droop” or phase lag in amplifiers, but also complicate power switching applications by increasing dynamic

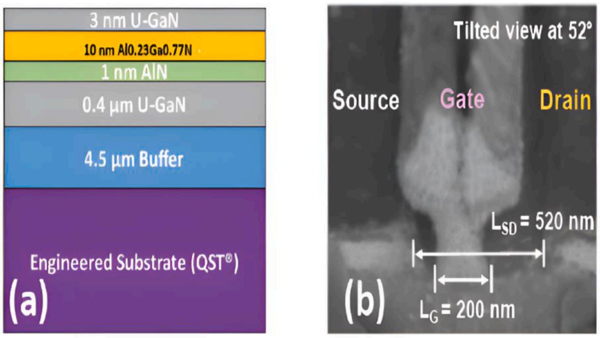

Fig. 23. (a) AlGaN/Gan epitaxial structure on QST, (b) fabricated transistor (cross section) [163].

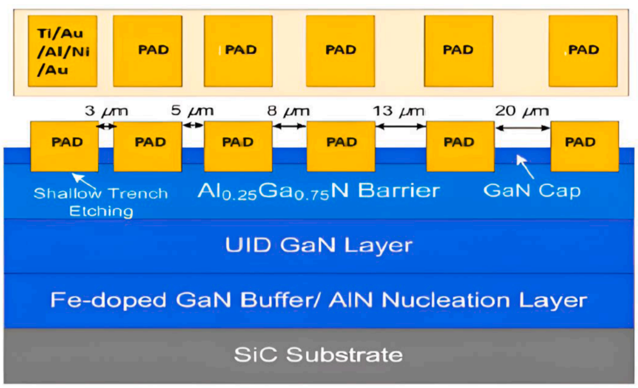

Fig. 24. AlGaN HEMT with AlGaN back barrier [170].

on-resistance.

Furthermore, a well-documented outcome of charge trapping in GaN-based HEMTs is current collapse, a dynamic degradation phenomenon caused by the trapping of electrons in surface and buffer states, particularly during high-drain-voltage operation [188]. When the device is stressed with high electric fields, electrons can become captured in deep-level traps near the channel. To maintain charge neutrality, the free carrier population in the 2DEG channel is reduced, resulting in a drop in drain current upon the next conduction cycle. This behavior is especially evident in pulsed operation, where the current does not recover to its initial steady-state level due to persistent trapping. Additionally, the loss of positive polarization charges at the surface of a heterojunction transistor is also a contributing factor to current collapse. As the positive polarization charges diminish, an equivalent number of electrons in the 2DEG are lost, further decreasing the channel's carrier density and leading to a drop in drain current [189]. To better understand and characterize current collapses, drain-lag and gate-lag conditions with quiescent bias (Q-bias) are commonly used [187]. The drain-voltage (I_D-V_D) characteristics curve presented in Fig. 27 indicates significant changes, like the increment of knee voltage (V_{knee}), the decrease of maximum current ($I_{D\text{-}max}$), and the reduction of maximum output power (P_{max}) [190]. As the operating window (P_{max}) decreases, the device becomes less capable of handling high-power operations efficiently, significantly affecting its reliability. Addressing the current collapse in GaN HEMTs remains a critical aspect of enhancing device reliability in high-frequency and high-power applications. A variety of engineering strategies have been developed to address this issue by focusing on the physical origins of charge trapping and the decline in dynamic performance. The dual-layer SiN_x stressor passivation (DSSP) technique is an impressive method that successfully reduces charges caused by polarization, leading to a significant drop in the amount of trapped charge.

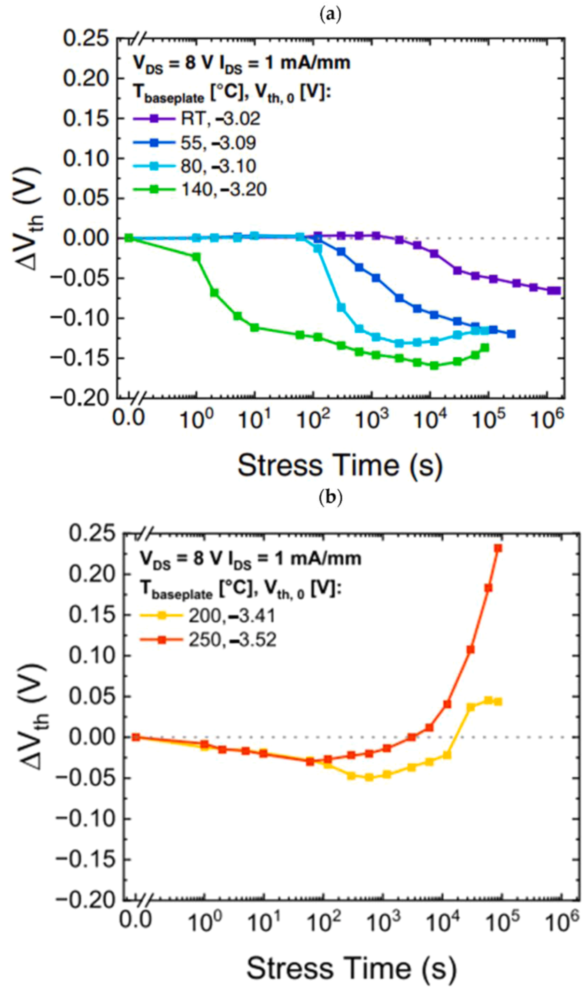

Fig. 25. Threshold voltage shifts due to thermal stress [289]: (a) negative shift and (b) positive shift.

This method has achieved a substantial reduction in current collapse, from approximately 34 % to 3 %, underscoring its potential for practical device applications [299]. Another promising solution involves reconfiguring the device architecture by integrating a heavily doped *N*++ layer. This design keeps the surface intact and helps restore the two-dimensional electron gas (2DEG), which reduces current loss by preventing interference with the p-GaN area [300]. Additionally, dual-gate structures have been utilized to regulate channel charge dynamically by injecting electrons during switching transitions, which helps minimize the extent of current collapse and lowers on-resistance [301].

Significant advancements in surface passivation have also played a crucial role. The use of Si_3N_4 layers, coupled with high-pressure water vapor annealing (HPWVA), has been shown to passivate surface defects and nitrogen vacancies, which are common trapping sites [302,303]. Structural modifications such as grooved barrier layers help redistribute electric fields more evenly, which has been associated with a >22 % improvement in collapse suppression [304]. Furthermore, combined surface treatments, including oxygen plasma exposure followed by field plate implementation, have been proven to be effective in lowering both trap densities and emission time constants, ultimately achieving lower dynamic resistance and enhanced transient performance [305]. While significant advancements have been made, certain techniques exhibit trade-offs, including elevated process complexity or restrictions in output current capacity. Consequently, ongoing research initiatives are essential to refine these strategies for wider implementation across

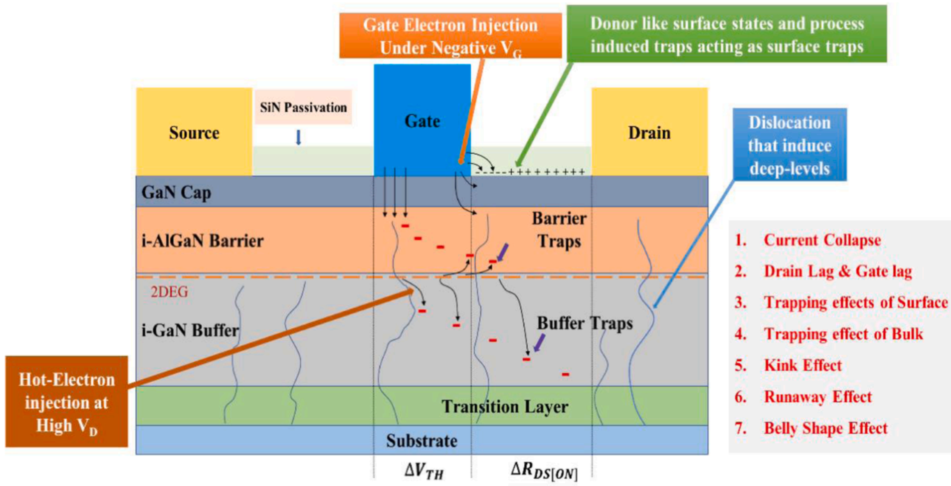

Fig. 26. A schematic of the AlGaN/GaN heterostructure illustrating different trapping mechanisms and their impact on device performance [185].

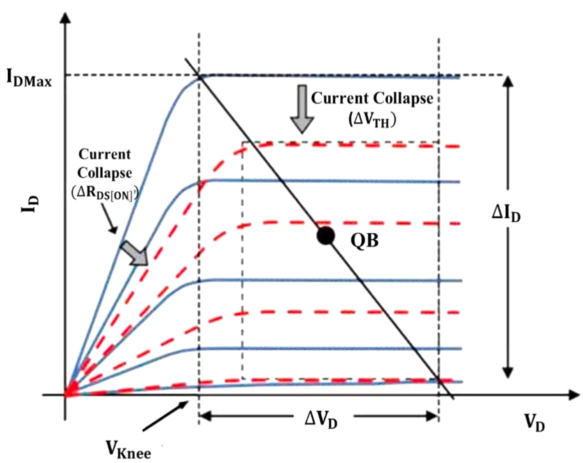

Fig. 27. This diagram shows the I_D–V_D characteristics of the HEMT both before (solid lines) and after (dashed lines) current collapse [190].

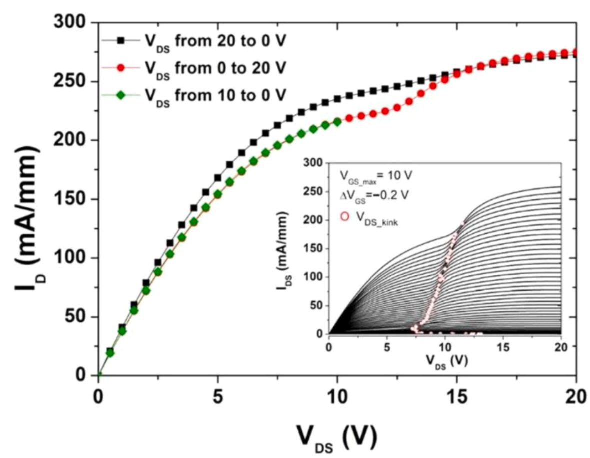

Fig. 28. A strong dependence on the direction of the V_{DS} sweep is evident in the kink effect in the I_D [306].

various circuit topologies and operational conditions.

5.4. Kink and runaway effects

Hot electron effect is another significant degradation mechanism in GaN HEMTs, particularly under high electric fields. Though GaN's wide bandgap allows it to sustain very high critical fields, electrons accelerated in these fields can attain high kinetic energy (hot carriers) that damage the device. These hot carriers can induce defects in the AlGaN/GaN interface or degrade gate dielectrics, leading to shifts in threshold voltage and increased leakage currents over time, similar to what happens with hot carriers in Si MOSFETs [205]. One sign of hot-electron effects in GaN HEMTs is the **kink** in the I-V curves, which shows a sudden change in drain current at specific drain voltage levels. This "kink" is attributed to trap emission or impact-ionization events that momentarily increase conductivity, and it depends on the prior bias history and temperature [206]. It may appear benign in small-signal analysis, but in high-power applications, it can introduce nonlinearities, signal distortion, and long-term instability.

The kink effect, shown in Fig. 28, arises due to trap dynamics influenced by the electric field between the source and drain. When the drain to source voltage (V_{DS}) is swept down from a high level, the drain current I_{DS} dips around $V_{DS\_kink} \approx 24.2$ V, but recovers when V_{DS} is swept upward. This effect is largely independent of V_{GS}, suggesting that trap filling does not require high current levels. The kink does not appear unless the maximum drain to source voltage ($V_{DS.\ max}$) exceeds the kink threshold. Additionally, the kink voltage shows a nonmonotonic shift with V_{GS}; for instance, as V_{GS} is stepped from 10 V to 0 V in – 0.2 V intervals, V_{DS_kink} first increases at V_{GS} and then decreases near pinch-off, as illustrated in the figure's inset. Each sweep was followed by a 5-minute rest period to allow for recovery [306].

While the kink is an operational nuance, a more dangerous high-field phenomenon is the **runaway effect**. When the device is pushed into a high-voltage saturation regime, a point can be reached where both drain current and gate current suddenly rise uncontrollably [207,208]. During runaway, the gate leakage skyrockets as V_{DS} approaches a critical threshold, and if biasing continues, the simultaneous increase in I_D and I_G can lead to catastrophic failure, effectively making this a rapid end-of-life trigger. The absolute gate current in runaway mode increases as the V_{GS} levels decrease, as illustrated in Fig. 29 [207]. Ageing tests that induce runaway conditions may result in catastrophic failures, compromising reliability. Under open channel conditions, runaways may be associated with Fowler-Nordheim tunnelling, as they transition to negative V_G values and lower V_{DS}. In reliability testing like High Temperature Operating Life (HTOL) or High Temperature Reverse Bias (HTRB), devices that undergo such runaway show permanent damage, characterized by a "belly-shaped" gate I-V characteristic, where an abnormal leakage hump appears after stressing, as illustrated in Fig. 30

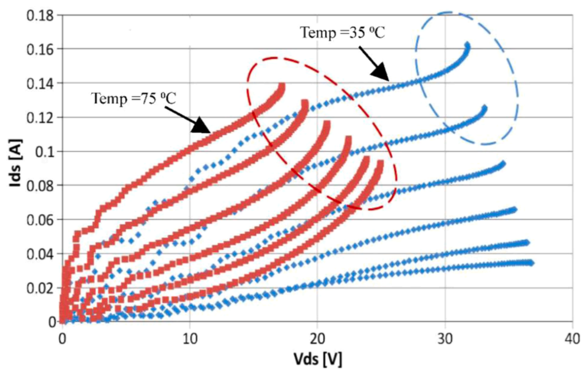

Fig. 29. The device's output characteristics indicate a runaway mechanism within the elliptical region at varying temperatures [207].

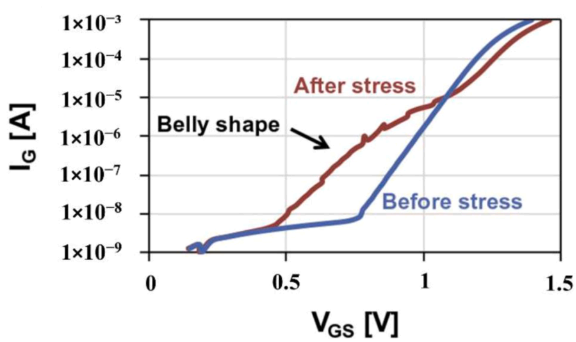

Fig. 30. The forward characteristics of a HEMT with belly shape effect are presented before (blue) and after (red) 4000 h of HTRB stress [210].

[209,210].

Preventing runaway and kink effects in GaN HEMTs relies on effective electric field management through field plates, optimized drain-to-gate spacing, and advanced gate design. Field plates help distribute the electric field uniformly, reducing peak stress regions. Proper drain spacing limits field crowding near the gate edge, while robust gate engineering, such as using high-quality dielectrics and tailored recess structures, enhances control over carrier injection and suppresses instability under high-voltage conditions. While these techniques have shown promising results, there are still unresolved questions about their effectiveness under various operating conditions, prompting continued research into more advanced solutions.

5.5. Thermal effects and material degradation

Thermal effects further intertwine with GaN reliability. Self-heating is pronounced in GaN HEMTs because they can handle high power densities in a small area. During operation, the channel and junction regions heat up substantially above ambient temperature, with local hotspots near the gate reaching well over 200 °C in high-power conditions [211]. This self-heating directly impacts reliability, accelerating degradation mechanisms and shortening device lifetime [212,213]. Elevated temperatures exacerbate trap-related phenomena by altering trap kinetics, which can make some traps more susceptible to capture or emission delays. These effects are reflected in shifts in parameters, such as V_{th} drift with temperature, and can vary based on device structure and biasing conditions [186,214,215].

Moreover, thermal cycling introduces mechanical stress due to mismatched thermal expansion coefficients between layers. In extreme cases, this leads to material damage, including nano-crack formation beneath ohmic contacts and interfacial delamination, which increases contact resistance and can eventually trigger failure [216]. These cracks, probably caused by spikes in the metal contacts or differences in how materials expand with heat, can grow into the GaN channel, increasing contact resistance or leading to serious failure. Additionally, thermal mismatches, heteroepitaxy, and polarization effects with the substrate cause inherent material challenges [186]. Further, Material degradation due to radiation exposure, thermal stress, and electrical overstress also affects long-term device reliability. Thus, managing the thermal environment of GaN HEMTs is critical. Compared to silicon devices, GaN's higher power density means significantly greater heat flux, on the order of three times higher than silicon IGBTs for a given area [215], making thermal management a paramount reliability concern. Without proper heat removal, self-heating can trigger secondary failure modes or a thermal runaway in which increasing temperature further degrades performance in a feedback loop.

Importantly, GaN HEMTs don't show a significant increase in on-resistance with temperature until they reach very high levels, allowing them to operate at higher temperatures before current starts to decrease, which highlights the importance of having designed thermal limits. Effective ways to manage heat include using materials that conduct heat well (like SiC or diamond), designing layouts that help with heat distribution, and utilizing advanced packaging methods to ensure that junction temperatures stay within safe limits. A more detailed discussion of these thermal management approaches is provided in Sections 6.3 and 6.6.

5.6. High-voltage off-state breakdown

GaN HEMTs receive special attention in high-voltage applications because of their elevated breakdown field (>300 V/μm), which makes them valuable for the next generation of power converters. But during the off-state in the switching operation, subthreshold leakage current (STL) rises at very high drain voltages, eventually exceeding the device's maximum current threshold, which leads to breakdown early [217]. As illustrated in Fig. 31 [186], source-drain punch through, Schottky gate reverse bias tunnelling, vertical breakdown through the buffer layer, and surface breakdown due to passivation issues are the main causes for this early breakdown. Among these, source-drain punch through often dominates. This effect arises when electrons penetrate the buffer beneath the gated channel, influenced by the vertical electric field in the gate region [307]. It is sensitive to gate voltage and gate length, especially at large gate-to-drain spacing. The punch-through creates a potential barrier in the buffer that initially restricts leakage current. Breakdown occurs when this barrier is overcome, allowing current to surge uncontrollably through the buffer [308]. In addition to Schottky gate tunneling, which is initiated by high electric fields near the gate edge, and vertical breakdown, which is the consequence of leakage through conductive substrates like n-type SiC, there are other critical failure mechanisms. Additionally, surface-related breakdown frequently results from inadequate passivation or poor interface quality, which permits the formation of leakage paths and erodes device reliability.

To improve off-state robustness, several advanced strategies have been developed to mitigate electric field crowding and surface leakage. These include utilizing thick, non-conductive buffer layers, tailored doping profiles, edge termination structures, and effective surface passivation. For instance, using fluoride plasma treatment near the drain-side gate edge makes the area more even in terms of electric fields, which raises the breakdown voltage from 900 V to 1400 V and also lowers leakage [309]. Field plate technology further enhances breakdown voltage by up to 17 % by changing how electric fields are spread out, allowing AlGaN/AlN/GaN HEMTs to reach voltages as high as 958 V [310]. Additionally, changes in the device design, like using Schottky-ohmic hybrid electrodes, help reduce the current that passes through the barrier, which improves breakdown performance for high-power uses. Finally, managing time-dependent dielectric breakdown via enhanced epitaxial growth and process control significantly enhances device reliability and prolongs operational lifespans [311].

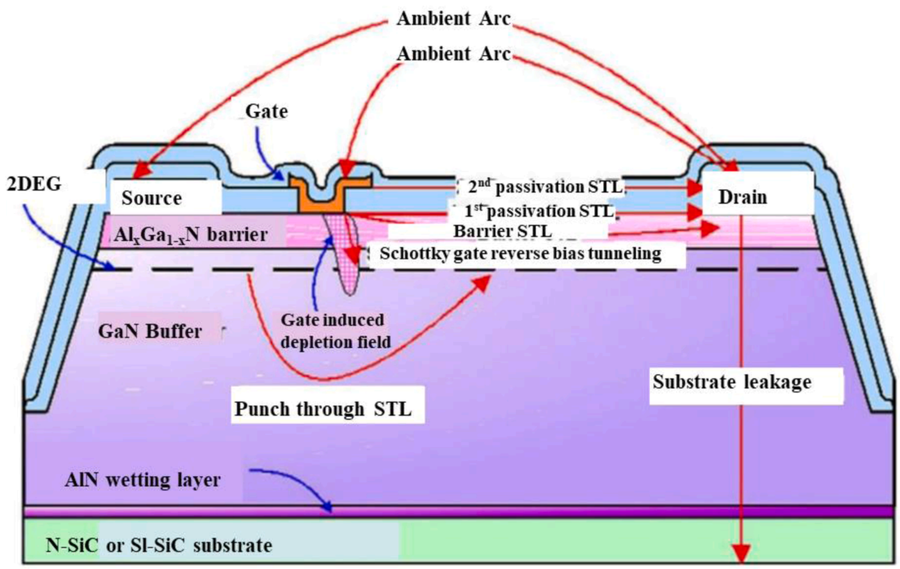

Fig. 31. Cross-sectional view of a GaN HEMT showing key layers and breakdown mechanisms [217].

6. Challenges in GaN HEMT technology

6.1. Epitaxial growth and substrate issues

Among the many challenges facing GaN HEMT technology, issues related to epitaxial growth and substrate quality stand out as particularly critical. These devices depend on high-quality epitaxial GaN layers, yet producing defect-free GaN remains difficult. Bulk GaN substrates are expensive and difficult to manufacture due to the extreme conditions required for crystallization—temperatures above 2200 °C and nitrogen pressures exceeding 6 GPa [186,218]. The defect densities of these wafers are still significant, ranging from 10^4 to 10^6 cm^{-2}, even after they have been obtained.

Because of the high cost and limited availability of bulk GaN, most commercial devices are fabricated using heteroepitaxy on silicon carbide (SiC) or silicon (Si) substrates. However, these platforms introduce significant lattice mismatch, leading to a high density of threading dislocations (~10^8 to 10^{10} cm^{-2}), which often results in film cracking and degraded material quality [219]. These crystalline defects negatively impact key device parameters, such as breakdown voltage and carrier mobility, while also contributing to long-term reliability issues.

Moreover, precise doping in GaN remains a difficult task. Achieving selective ion implantation requires post-implantation annealing at very high temperatures (~1200 °C) and pressures to activate dopants [220]. This complexity poses major hurdles in realizing p-type GaN (needed for enhancement-mode or normally-off devices) and heavily doped n-type regions for low-resistance ohmic contacts. Efforts to address these limitations include innovative buffer layer architectures and advanced in-situ growth methods. For instance, the insertion of nano-patterned SiN_x masks or the use of compositionally graded transition layers has helped to reduce dislocation densities. Still, the fundamental issues tied to epitaxial quality and substrate compatibility remain a bottleneck in scaling GaN HEMTs for broader commercial and high-reliability applications.

6.2. Short-channel effects and device scaling challenges

In the case of increasing frequency and device density, GaN HEMTs are being scaled to shorter gate lengths, but this miniaturization faces several issues. Short-channel effects (SCEs) become pronounced when the gate length is not much larger than the barrier thickness or depletion regions. These effects include drain-induced barrier lowering (DIBL), channel length modulation (CLM), subthreshold swing degradation, and threshold voltage shifts, leading to higher off-state leakage and loss of gate control [312–314]. Fig. 32 schematically illustrates these phenomena in GaN N-polar HEMTs. As the drain bias increases, the energy barrier between the source and drain is pulled down, especially in short-gate-length devices. When this barrier dips below the source Fermi level, unwanted carrier injection occurs, resulting in V_{th} reduction and off-state leakage. Additionally, the figure depicts how the high electric field near the drain side causes significant band bending, facilitating tunneling of electrons from the gate to the drain—an effect known as gate-induced drain leakage (GIDL).

The shortening of the effective channel length due to field crowding at the drain end, characteristic of CLM, is also visualized through the narrowing of the barrier region. These short-channel phenomena degrade both DC and RF performance, reducing transconductance and cutoff frequencies, while increasing leakage currents and compromising device reliability [315–317]. For GaN HEMTs, a gate-length-to-barrier-thickness ratio above ~6 is reported to effectively suppress SCEs [221], yet many high-frequency GaN devices approach this limit. As gate length shrinks, the peak electric field in the channel increases, which can precipitate premature breakdown unless mitigated

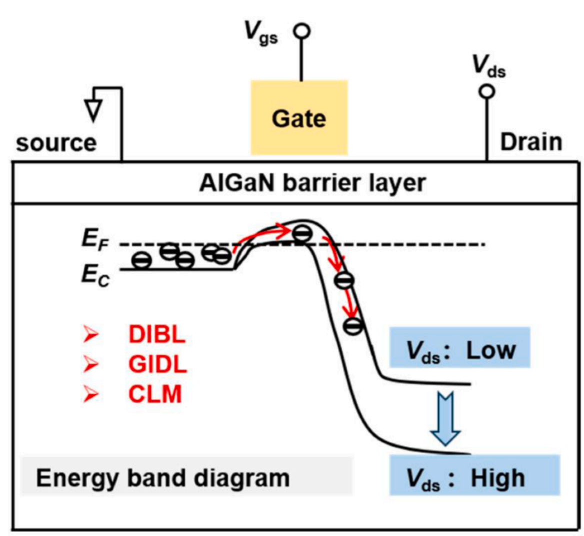

Fig. 32. Schematic diagram of SCEs for GaN HEMTs [315].

by field plates or new device architectures. Furthermore, aggressive scaling exacerbates surface and buffer-related phenomena—for instance, trapped charge has a proportionally greater impact in short channels, causing V_{th} instability and transconductance dispersion [222]. Another scaling challenge is achieving enhancement-mode (normally--off) operation in deeply scaled GaN HEMTs. Techniques like p-GaN gate layers or ultra-thin barriers can enable normally-off behavior, but they often introduce new trade-offs such as increased gate leakage or reduced channel mobility. Overall, while GaN offers excellent high-frequency performance potential, SCEs and maintaining performance at nanometer-scale gate lengths remain major hurdles. Ongoing research is exploring T-gate designs, recess etching, multi-channel (multi-2DEG) structures, advanced modeling approaches including charge-based models and Monte Carlo simulations, and optimized doping profiles with advanced lithography techniques to allow further scaling without compromising control or reliability [223–228,318,319].

6.3. Thermal management and heat dissipation

GaN HEMTs can handle high power densities, but removing their generated heat is a critical challenge. GaN's thermal conductivity (~130–200 W/m·K) is lower than that of SiC (~400 W/m·K) or diamond, and heteroepitaxial devices are often on substrates like Si (~150 W/m·K), which further limits heat dissipation [229]. Self-heating leads to elevated channel temperatures, which in turn can reduce mobility and cause current degradation during operation (thermal droop). Without proper thermal management, device lifetime also shortens, as high junction temperatures accelerate degradation mechanisms. Advanced thermal solutions are being pursued to address this. GaN-on-diamond technology, for example, integrates GaN devices on diamond substrates or caps, exploiting diamond's extreme thermal conductivity (~2000 W/m·K) to spread heat. This approach has demonstrated >50 °C lower channel temperatures and significantly higher power output compared to GaN-on-SiC baselines [229,230]. However, integrating GaN with diamond is non-trivial; challenges include managing the thermal boundary resistance at the GaN–diamond interface and stress from their lattice mismatch. Other strategies include flip-chip packaging, embedded microfluidic cooling, and the use of high-thermal-conductivity materials like AlN or novel substrates (e.g., polycrystalline AlN or Cu heat spreaders) to draw heat away from the device. Ensuring effective heat removal is especially important for high-power RF amplifiers and power switching HEMTs. Otherwise, insufficient cooling can lead to thermal runaway or degradation of RF performance (e.g., gain collapse) during high-duty-cycle operation. Thus, thermal management remains a key challenge, and the reliability of GaN HEMTs in high-power applications is often thermally limited.

6.4. Ohmic contact formation and contact resistance

Forming low-resistance, thermally stable ohmic contacts on GaN HEMTs is difficult due to the wide bandgap and high contact potential barrier of GaN. Unlike silicon devices, which rely on degenerately doped regions to facilitate ohmic behavior, GaN's ionization energy for dopants is high. Therefore, achieving sufficient carrier concentrations at the surface is challenging to support efficient tunneling or thermionic emission, particularly in the access regions of lateral devices. As a result, traditional methods of achieving ohmic behavior through heavy doping are not readily applicable to GaN-based devices.

The most widely adopted solution in GaN technology has been the use of alloyed metal contact stacks, such as Ti/Al/Ni/Au, which are subjected to high-temperature (~800 °C) rapid thermal annealing. During this process, metal stacks react with the AlGaN/GaN to form an interfacial alloy and tunnel contacts. Although this approach enables functional device operation, it typically results in a specific contact resistance (R_c) in the range of 0.5–1 Ω·mm, which remains considerably higher than the R_c values achievable in mature silicon or GaAs technologies.

High R_c in GaN devices contributes significantly to the total on-resistance (R_{on}), especially in high-frequency and high-power applications where low insertion loss and minimal source impedance are critical. In RF applications, elevated contact resistance introduces parasitic voltage drops, reduces gain, and adversely affects overall device efficiency and linearity. Therefore, minimizing R_c is a key goal in GaN HEMT research and development, particularly as these devices are pushed to operate at higher frequencies and in more demanding power regimes.

Recent advances have shown impressive improvements, like regrowth of heavily Si-doped n^+ GaN in the source/drain regions by MOCVD or MBE, have demonstrated R_c values as low as 0.16 Ω·mm [231], marking a substantial reduction compared to conventional contacts. Similarly, ion implantation to create localized n^+ regions under the contacts has been explored, though activating implants in GaN requires very high temperatures [176]. Novel metallization schemes are also being tried, such as non-alloyed ohmic contacts using multi-layer Ti/Al/TiN or Ti/Al_3O_x that can be annealed at lower temperatures, as well as gold-free contact stacks for CMOS compatibility [232–234]. Despite this progress, challenges persist in terms of contact reliability and scalability. The alloyed contacts can suffer from morphology issues (edge spiking, roughness) and diffusion of metals (e.g., Au) into the semiconductor at high temperatures, which raises concerns for long-term stability at the elevated junction temperatures GaN HEMTs often operate. Developing ohmic contacts that are ultra-low resistance, thermally stable, and manufacturable at scale is still an active area of research. Success in this area directly impacts power device performance (lower R_{on}) and RF device efficiency (higher output power and PAE).

6.5. Charge trapping effects

Addressing trapping effects is critical for both high-power applications, where efficiency during transient operation must be maintained, and digital circuits, where threshold voltage stability is essential for reliable logic switching. GaN HEMTs are particularly vulnerable to charge trapping in surface states and bulk crystal defects, which degrade performance. While surface-state-related issues have been discussed earlier, traps can also originate from intrinsic crystal defects such as vacancies and dislocations formed during epitaxy, or from extrinsic factors like impurities and dopants (e.g., carbon or iron deep acceptors used to semi-insulate the buffer) [222].

Several reliability concerns are introduced by these traps, such as an increase in dynamic on-resistance, V_{th} drift with bias and temperature, and frequency dispersion in capacitance and output power. To guarantee the stability of devices, it is imperative to implement effective mitigation strategies. This encompasses advanced buffer engineering to reduce bulk trap densities, as well as surface passivation techniques, such as SiN_x or Al_2O_3 layers deposited via ALD, to suppress surface traps and reduce current collapse. For example, the elimination of hetero-interface defects can be achieved through GaN-on-GaN homoepitaxy, while the occupancy of traps can be reduced through the use of innovative buffer doping profiles.

Furthermore, circuit-level strategies, including gate shaping and drain quiescent bias control, mitigate the effects of trapping during operation. Trapping continues to be a persistent issue, despite the ongoing progress. The current collapse and significant V_{th} shifts are still being reported in numerous devices. To mitigate this issue, researchers are implementing sophisticated characterization tools (e.g., deep level transient spectroscopy, pulsed I-V measurements) and investigating novel material growth techniques, including iron-free buffer technologies and substrates with lower defect densities, to prevent trap formation at the source [222].

6.6. Mechanical stress and device durability

GaN HEMTs experience significant internal mechanical stress due to the material's piezoelectric properties and device architecture. These stresses can lead to failure modes such as crack formation, delamination, or contact degradation. To mitigate these effects, stress-relief strategies are employed at multiple levels. Within the epitaxial structure, carefully engineered buffer or transition layers serve to relieve accumulated strain resulting from lattice and thermal expansion mismatches. Device layout optimization can reduce current crowding and localized heating, while advanced packaging—using compliant substrates or thermally conductive fillers—alleviates mechanical stress during operation. These combined approaches are critical for improving mechanical integrity and ensuring long-term device reliability.

Overall, while GaN HEMTs are robust in many respects, they do face reliability challenges under high-stress conditions. Long-term testing has shown failure mechanisms like gate leakage increase, drain current degradation, and even catastrophic breakdown linked to these mechanical stress factors [186,235,236]. Ensuring adequate derating (operating below absolute max ratings) and developing fabrication techniques to strengthen device structures, like crack-resistant metallization or strain-engineered buffer layers, are active areas of work to improve GaN HEMT reliability.

7. Recent applications of GaN HEMT

7.1. Satellite and aerospace systems

GaN HEMTs are gaining importance in satellite and space electronics because of their radiation hardness and high-power capability. They have demonstrated resilience to high total ionizing doses and minimal performance shifts, making them well-suited for satellites and spacecraft. In satellite communication systems, GaN HEMTs are enabling powerful, compact, and efficient RF amplifiers. For example, in Ku-band applications, they can deliver up to 100 W of output power with a power-added efficiency (PAE) of 30 %, significantly outperforming GaAs-based counterparts [320]. Their efficiency is also clear in power systems, where GaN-based converters have achieved a peak efficiency of 86 %, which is 4.54 % better than traditional silicon-based designs in 75-W space-rated converters [321]. Thermal performance is another significant advantage, as GaN HEMTs can operate at temperatures as high as 250 °C, whereas GaAs transistors are restricted to 175 °C. This capability alleviates the burden of thermal management in space environments. The utilization of silicon carbide (SiC) bases in GaN HEMTs further enhances heat management, resulting in superior performance when managing high power. GaN HEMTs are also employed in aerospace defense systems to produce high-powered microwave signals that are resistant to radiation and operate at extreme altitudes. These signals are generated using airborne radar and electronic warfare systems. In the context of modern satellite communication systems, GaN HEMTs are indispensable due to their capacity to operate at high frequencies and bandwidths. For example, AlGaN/GaN MMICs can generate high output power density and efficiency at frequencies exceeding 10 GHz [322]. Their low distortion characteristics are essential for the preservation of signal integrity across a wide range of bandwidths in multi-carrier communication systems.

Despite these benefits, the deployment of GaN HEMTs encounters obstacles, such as the scarcity of radiation-hardened devices and the requirement for specialized manufacturing processes that may impede their extensive use in space applications. Moreover, the expense associated with GaN technology may exceed that of conventional materials, potentially affecting its viability for specific projects. Nevertheless, the potential of GaN technology for future satellite and aerospace systems is being further developed through ongoing advancements. GaN is expected to experience a market growth rate of approximately 26 % CAGR through the mid-2020s as the space industry rapidly adopts it. This growth rate is indicative of its critical role in both commercial "New Space" satellites and traditional military/aerospace platforms [237].

7.2. Biosensors and medical diagnostics

In biomedical sensing, GaN HEMTs are emerging as a platform for advanced biosensors that can detect biomolecules and physiological parameters with high sensitivity. The unique material properties of the AlGaN/GaN heterostructure (especially the high-density 2DEG at the interface) are advantageous for biosensing. In a typical setup, GaN HEMTs use an open or functionalized gate exposed to an analyte, such as proteins, DNA strands, or ions. When target molecules bind to the gate surface, the resulting change in surface charge modulates the channel conductivity, enabling precise detection [238]. For instance, a GaN HEMT-based biosensor for Interleukin-6 (IL-6) detection achieved a peak sensitivity of 158.01 μA/pg/mL [323], while ethanolamine-modified devices have pushed the detection limit for prostate-specific antigen (PSA) down to just 1 pg/mL [324]. This result is a twofold improvement over the previous generation.

Beyond their sensitivity, GaN HEMTs provide exceptional thermal and chemical stability. In contrast to silicon-based sensors, they are capable of withstanding corrosion and oxide degradation, which enables them to operate reliably in aqueous or harsh environments, even at high temperatures or extreme pH levels [238–240]. These characteristics render them optimal for real-time, reusable biomedical assays. Additionally, GaN HEMT biosensors are capable of supporting point-of-care applications owing to their fast response times (as low as 5–10 s) and low sample volume requirements (1–2 μL) [325]. Recent research has extended their use to detecting cancer biomarkers like c-erbB-2 (HER2) and PSA [240], as well as viral proteins such as SARS-CoV-2 [241]. Moreover, GaN-based biosensors, which are also biocompatible, demonstrate high sensitivity for various biosensing conditions. For example, devices with gate lengths of 1 μm and 5 μm show sensitivities of 2.5 mA/mg and 0.72 mA/mg, respectively. I_D is commonly used as the sensing metric for biomarkers like HER2 in saliva and serum, supporting non-invasive diagnostics [247]. Besides, devices that are functionalized with aptamers or antibodies have successfully detected trace levels of cytokines such as interferon-gamma, with responses that are observable at concentrations as low as picograms per milliliter.

GaN HEMTs also lend themselves well to miniaturization and integration. Multiple sensors can be fabricated on a single chip, enabling simultaneous detection of different biomarkers. This scalability and low power consumption open the door to compact, portable diagnostic tools for use outside traditional laboratory settings. Despite the immense potential of GaN HEMTs, their fabrication is more complex and costlier than that of silicon-based devices, and more research is needed to adapt them for a broader range of biosensing targets. So, ongoing advancements in GaN materials and device engineering continue to address these issues, positioning GaN HEMTs as a promising frontier in next-generation medical diagnostics.

7.3. Renewable energy technologies

wind turbines, by enabling more efficient and compact power conversion. In solar energy, one of the critical components is the inverter or microinverter, which converts DC power from solar panels into AC power for the grid. GaN-based power transistors allow these inverters to operate at much higher switching frequencies than silicon IGBTs or MOSFETs, which directly translates to smaller magnetic components (inductors, transformers) and filters. This reduction in passive component size can greatly shrink the inverter's volume and weight. Moreover, the higher efficiency of GaN (due to lower switching losses and near-zero reverse recovery charge) means less heat is generated; thus, heatsinks can be smaller, or in some cases, fans can be eliminated in sealed photovoltaic inverter units. Besides, using GaN transistors in renewable energy inverters has been shown to improve power density and reduce heat dissipation. For example, commercial solar inverters built with GaN HEMTs achieve efficiencies in the 98–99 % range, noticeably reducing losses compared to silicon-based designs (which might be 95–97 %). This efficiency gain means more of the harvested solar energy is delivered to the grid rather than wasted as heat, improving the overall yield and economics of solar farms.

In wind energy systems, GaN devices are finding roles in the power converters that manage the variable output of wind turbines. A wind turbine's generator often produces wide-frequency AC that must be rectified and then inverted to grid-frequency AC – a process typically done with power electronics. GaN HEMTs, capable of handling medium voltage levels (several hundred volts), are particularly suitable for parts of these systems, such as auxiliary converters or modular converter stages in lower-power turbines. Their faster switching speeds and lower conduction losses compared to silicon-based devices allow for more precise power flow control and higher overall energy conversion efficiency.

Additionally, GaN-based power electronics can be beneficial in battery storage interfaces that often accompany renewable installations (like solar with storage systems), enabling faster switching [131] chargers/dischargers with lower losses. Renewable energy systems also benefit from GaN's reliability at high temperatures – solar inverters on rooftops can face high ambient temperatures, and GaN's wide-bandgap nature gives it an inherent advantage in high-T operation (lower leakage currents and no thermal runaway). Companies have reported that in renewables applications, GaN power devices have led to as much as 50 % reduction in volume of power converters and a notable drop in cooling. This not only lowers cost but also improves longevity (as cooler devices typically last longer). As the renewable energy sector continues to grow, GaN HEMTs are increasingly adopted in everything from microinverters to MW-scale central inverters and wind farm converters, helping to push efficiency towards the theoretical limits and making clean energy systems more compact and cost-effective.

7.4. Advanced communication infrastructure (5G, IoT, cloud computing)

GaN HEMTs are becoming essential in next-generation communication systems, especially in 5 G and emerging 6 G networks, because of their superior power handling, high-frequency operation, and efficiency [155,242,298]. In 5 G base stations, they are crucial for RF power amplifiers, delivering high output power over broad bandwidths, particularly in millimeter Wave bands like 28 GHz and 39 GHz, which is vital for massive MIMO systems [249,254]. Additionally, recent improvements have shown that GaN HEMTs can reach a power-added efficiency (PAE) of 62 % at 30 GHz and maintain 55 % efficiency even when reduced by 3 dB, which is leading performance for mmWave RF amplifiers. They also achieve a carrier-to-third-order intermodulation (C/IM3) ratio of 30 dB, minimizing signal distortion [249]. Their excellent thermal and electrical stability supports low-latency, high-throughput wireless links essential for applications like autonomous vehicles and smart cities. As communication technology progresses toward 6 G, the capabilities of GaN will be essential for achieving ultra-fast, low-power wireless connectivity [256,261,264].

In the Internet of Things (IoT), GaN HEMTs are increasingly used for compact and efficient RF components, particularly in industrial settings where high-temperature and chemically harsh environments are common. Their sensitivity to changes in the environment improves how well they respond, making it possible to create highly accurate sensors for different monitoring applications [276]. Integration with edge computing platforms facilitates local processing, improving latency and data privacy in distributed IoT architectures [277]. Moreover, coupling HEMT sensors with cloud infrastructures provides scalable data management and real-time analytics. Hybrid cloud models further support resource optimization and data security, particularly in sensitive sectors like healthcare. Service-oriented models such as Sensing-as-a-Service (SaaS) and Database-as-a-Service (DBaaS) allow HEMT-based IoT systems to deliver actionable insights from sensor data efficiently [291].

Despite encountering challenges such as standardization, interoperability, and high costs, GaN technology plays a crucial role in advancing communication, sensing, and computing technologies. Its efficiency, linearity, reliability, and flexibility in integration make it an essential enabler for the development of future wireless technologies, IoT systems, and energy-efficient cloud infrastructures.

7.5. Industrial power conversion and automation

In industrial settings, GaN HEMTs are playing a transformative role in power conversion, motor drives, and automation systems. Their fast-switching speed and low conduction losses make them particularly well-suited for compact, high-efficiency inverters, essential for applications like robotics, drones, and automated machinery. By enabling higher switching frequencies, GaN devices allow for the use of smaller magnetic components, thereby enhancing power density while reducing both system weight and energy loss.

Factory automation and industrial control systems also benefit from GaN's capability to integrate high-performance power electronics into smaller, more efficient units. This not only reduces system costs but also aligns with the demands of smart manufacturing and Industry 4.0, where responsiveness, efficiency, and reliability are critical. Moreover, GaN HEMTs offer strong resilience in harsh environments, such as high-temperature zones or areas with significant electromagnetic interference, making them ideal for mission-critical systems within automated factories and industrial plants [91].

8. Conclusion

This review has significantly explored the potential of Gallium Nitride-based HEMTs in high-frequency, microwave, as well as high mobility applications, including 6 G communications and biosensing. In biosensing, these kinds of devices have remarkable attributes in high sensitivity in detecting biomarkers like PSA and HER2, with detection stems as low as 1pg/mL. With a view to advancement in 6 G communications, research is prior to focusing on the integration of Gan HEMTs with CMOS technology to enhance the performance. This article also addresses the issues and challenges like current collapse, kink effect, pinch-off effects, short-channel effects etc. It further mentions the strategies to mitigate these issues, including dual-layer SiN_x passivation, heavily doped $N++$ layer integration, dual-gate architectures, surface treatments (e.g., HPWVA), grooved barriers, and advanced field plate/gate designs. This review stands unique by offering a comprehensive and current overview of GaN HEMT technology, integrating insights across device architectures, reliability concerns, and emerging application domains such as biosensing and 6 G RF systems. In contrast to earlier reviews, this article presents a structured comparison of the latest architectural developments, includes detailed performance metrics, and analyzes recent strategies for addressing critical reliability challenges based on recent studies. A key distinguishing feature of this work is its emphasis on bridging laboratory innovation with industrial relevance, demonstrating how advanced device designs and novel materials meet practical performance needs. By aligning leading-edge research with persistent technical hurdles and next-generation use cases, this review delivers concrete guidance and identifies future directions of interest to both researchers and industry stakeholders.

Recommendation for future research and development:

1. Device Optimization: Refinement of gate alignment and advanced passivation techniques to enhance device reliability and performance.
2. Material innovations: Examine the use of better-quality materials to optimize thermal management and diminish self-heating issues.
3. Integration strategies: Explore proportional fabrication of GaN HEMT with the addition of CMOS technology.

4. Application-specific tailoring: Customize GaN HEMT designs to meet the specific requirements of emerging applications, ensuring optimal performance and efficiency.

Declaration of generative AI and AI-assisted technologies in the writing process

We the undersigned declare that this manuscript is original, has not been published before and is not currently being considered for publication elsewhere. During the preparation of this work the author(s) used Chatgpt and Canva in order to enhance the grammar, language readability, and to recreate some structures of GaN devices for clearer picture with high image quality. After using this tool/service, the author(s) reviewed and edited the content as needed and take(s) full responsibility for the content of the publication.

CRediT authorship contribution statement

Arnab Talukder: Investigation, Conceptualization, Methodology, Data curation, Supervision, Formal analysis, Writing – original draft, Project administration. **Mohiminur Rahman Ifty:** Writing – review & editing, Writing – original draft, Methodology, Formal analysis, Conceptualization, Investigation, Data curation. **Abdullah Al Fahad:** Supervision, Formal analysis, Resources, Investigation, Writing – original draft, Data curation, Writing – review & editing, Methodology, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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