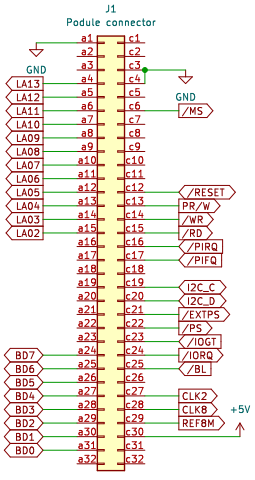
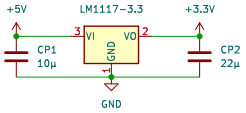


ARM Podule connector (DIN 41612)



3.3V Power supply

System logic selection

A) When Computer is switched on, Raspberry pi is pulling /RESET line to GND
until IDT Memory address 0 is filled with Podule ID byte.
Then, /RESET line is released by RPI, allowing ARM side to boot and
Podule identification process id done.

B) After completion, /RESET line on the RPI side is set as input.
If a LOW level is detected, it means that ARM /RESET line is activated.
Then, RPI side set /RESET line as output and control the /RESET procedure (see topic A)

NOTE

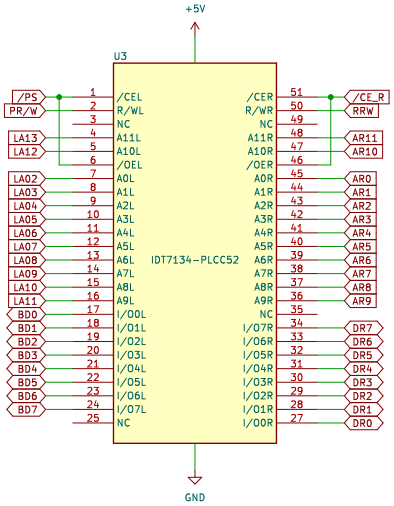
On Raspberry Pi side, level converter are controlled by the R_OE signal available on GPIO Port (pin 13)

On Raspberry Pi side, IDT output enable is controlled by the /R_CE signal available on GPIO Port (pin 5)

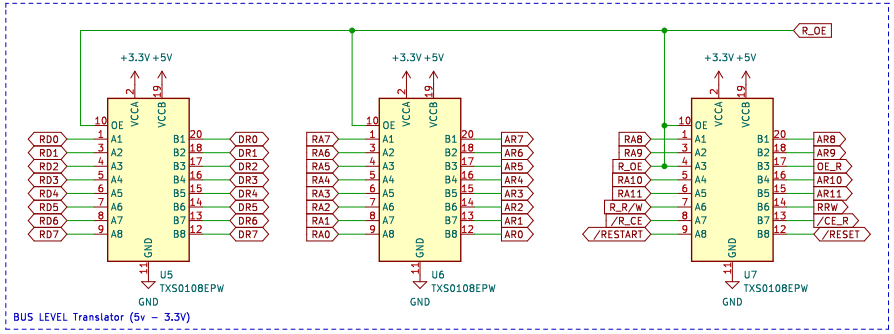
INFO

IRQ – Bit 0 – Set bit to 1 if IRQ line is used by podule
ENABLE – Bit 1 – Always set to 1 to enable podule detection by the system
FIQ – Bit 2 – Set bit to 1 if FIQ line is used by podule
ID1 – Bit 3 – First ID bit setting
ID2 – Bit 4 – Second ID bit setting
ID3 – Bit 5 – Third ID bit setting
ID4 – Bit 6 – Fourth ID bit setting
ACORN – Bit 7 – ACORN compliance podule setting

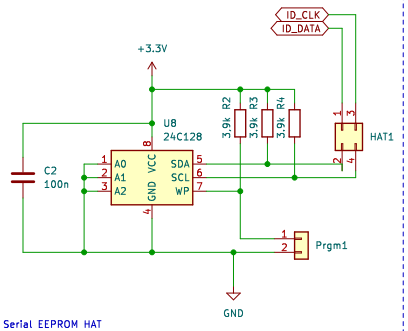
Notice



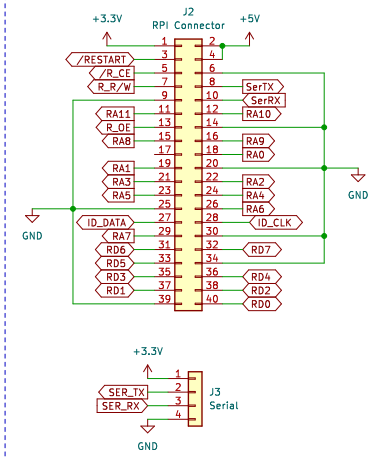
IDT Two Port RAM & Podule ID logic



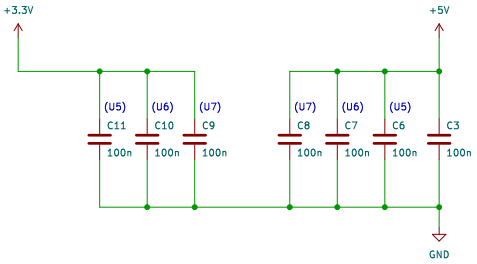
BUS LEVEL Translator (5v – 3.3V)



Serial EEPROM HAT



RPI GPIO Port



Sheet: /
File: A410_Bridge_4Mb.kicad_sch

Title: Acorn Archimedes Double port RAM podule for RPI

Author: Alain.Lowet@gmail.com

Size: A3 | Date: 25/09/2023 | **Rev:** 1.1

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