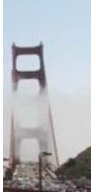
Alpa Desai Gupta

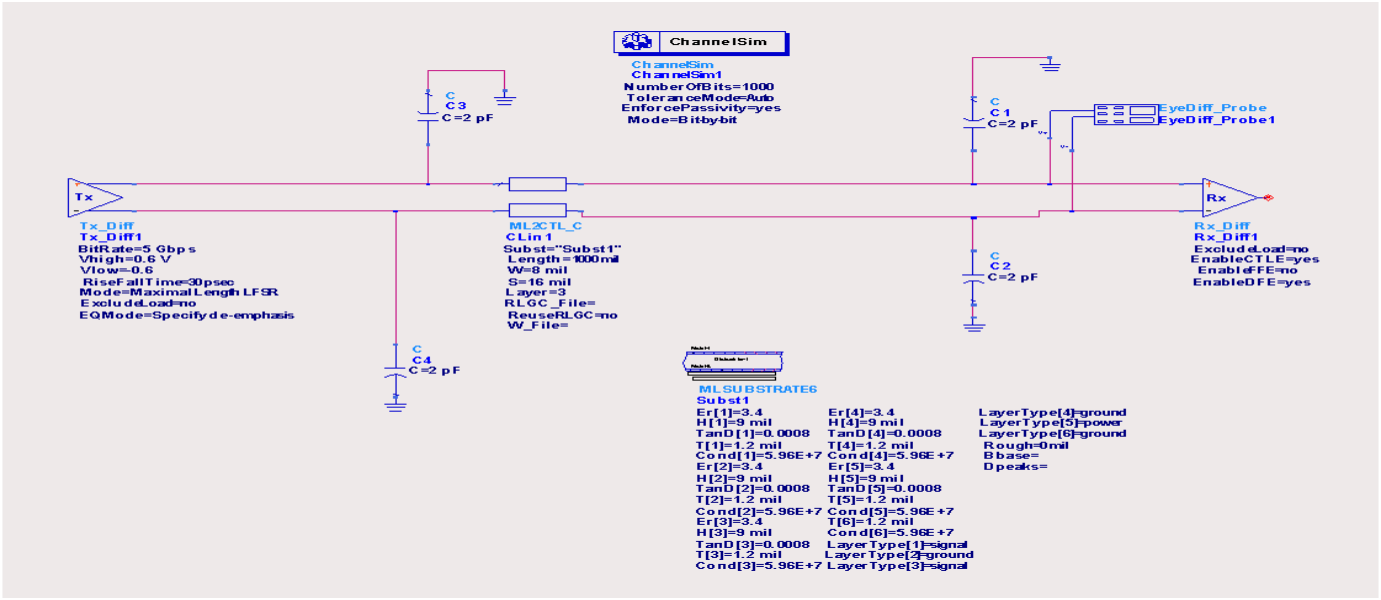
|United States Citizen| www.linkedin.com/in/alpadesaigupta| Boston, MA | #617-602-2179|
| Objective: Actively seeking full-time employment opportunities in the San Francisco or Boston Locations |



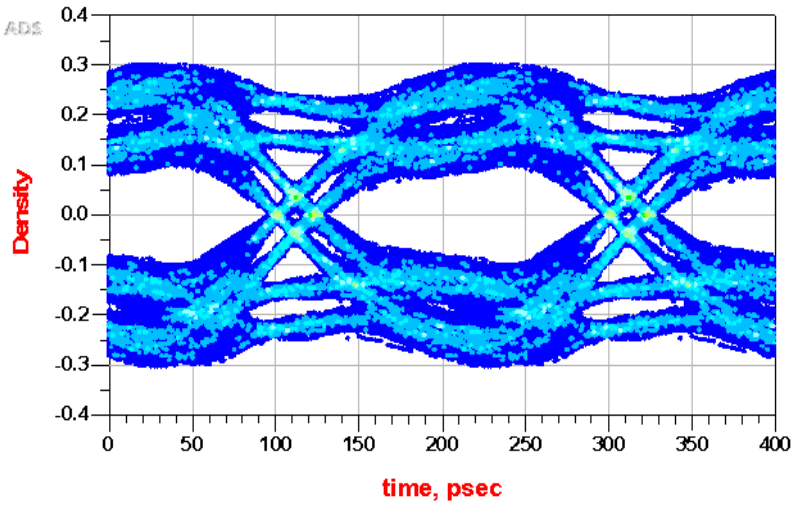
Alpa Desai Gupta
Graduate Student
Northeastern University
Boston, MA

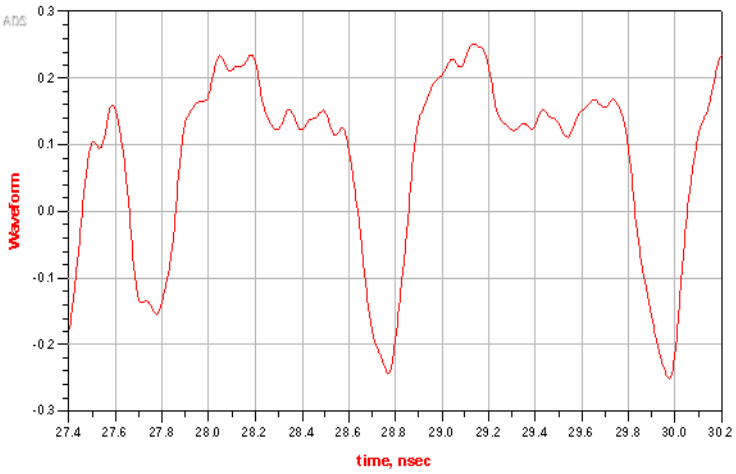
Dear Engineering Design Team,

Past engineering coursework at Santa Clara University, Graduate School of Engineering has provided an opportunity to ramp up to the latest technologies. To demonstrate I have provided demos of non-confidential professional experience that matches a few job descriptions that I have applied to. The simulations diagrams are from Santa Clara University Oct/Nov/Dec 2018. Latest programming experience is from Northeastern University 2019.



Experience with Advanced Design Systems The differential transmitter with 6db de-emphasis does include minimal jitter parameters. The bit rate is 5Gbps with amplitude of +/-0.6v. The transmission path is a tightly coupled differential trace, the substrate has a dielectric value of 3.4 and a ground reference on either side with 9 mil height. The length of the transmission path is 1inch, at the receiver end and equalization is enabled. Jitter is not included on the receiver side. The 2pF capacitance on either side of the transmitter and receiver displays a realistic parasitic capacitance on the channel link. The eye diagram and waveform is shown on the next page.





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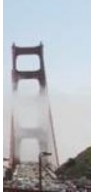

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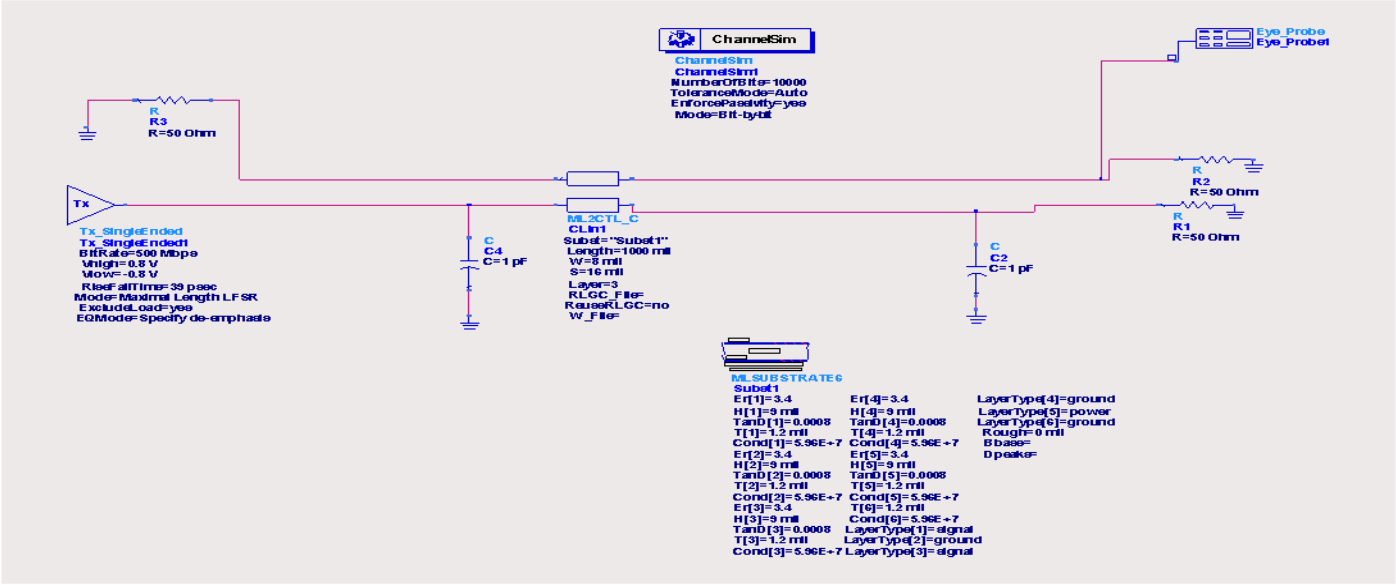
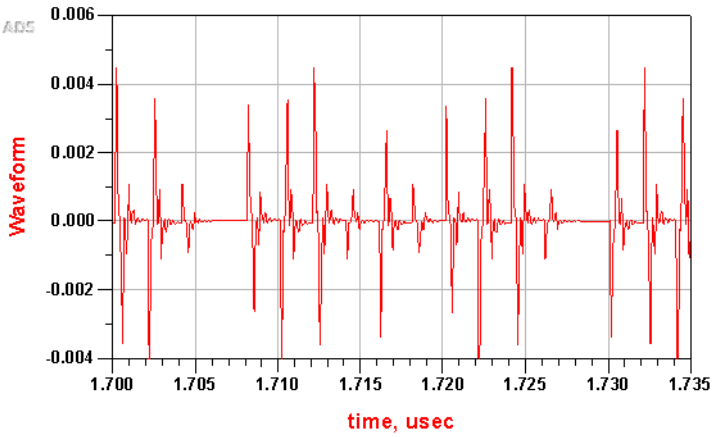
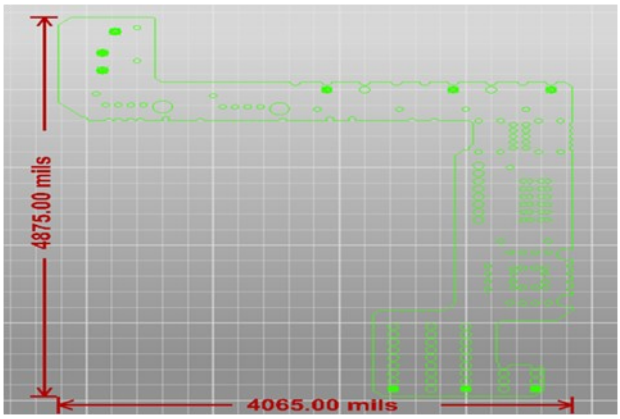
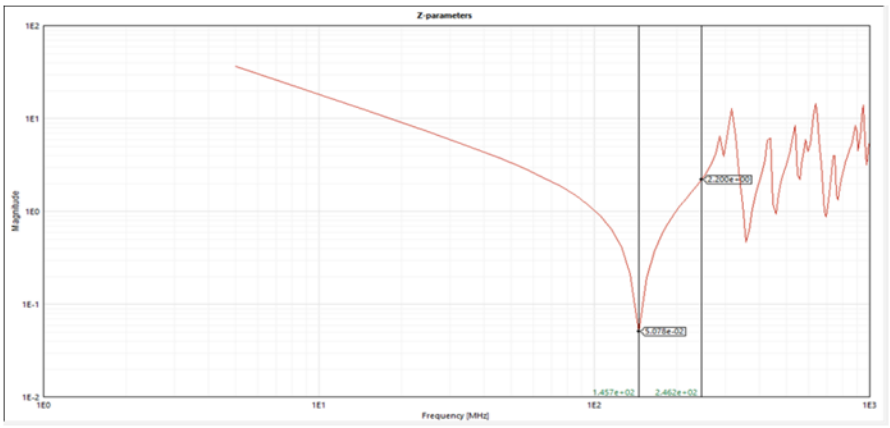




ADS transient analysis can also be utilized to characterize far end and near end crosstalk on pcb traces. The waveform shows the cross talk noise on a trace with less than 3x spacing. The spacing is at 2x the trace width and the data rate is 5Mpbs on the transmitter.

Experience with Ansys SIWave/ Sigrity Power SI





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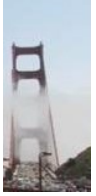

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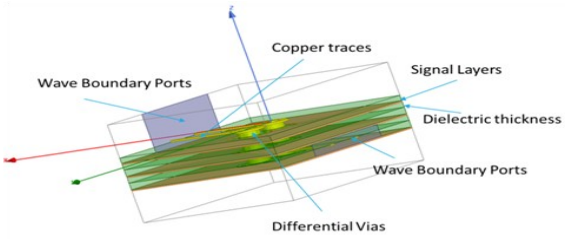
Optimizing PDN networks involves having an extensive knowledge of the schematic design including power generation and distribution. Minimizing noise generated by switchers involves utilizing digitally controlled power generation components. Once an optimal design has been laid out in the schematic including the bypass capacitance distribution, the PDN analysis at the board level involves designing a cost effective stack up that meets all the required specifications of a design, analyzing the power planes and resonant peaks from the impedance power plot. The resonant peaks are generated due to planar capacitance, bypass capacitor network, via inductance, size and placement of the power planes.



Experience with Ansys SIWave/ Sigrity Power SI

The goal is to build an insertion loss budget for the differential traces when they transition layers through differential vias. Hence the insertion loss budget will take into account the via inductance, loss tangent of dielectric, via impedance due to the anti plane spacing and size of the via hole length of the differential traces and the wave port impedance.

The diagram is a Ansys 3D via simulation that shows the impact of transitioning layers for critical high speed differential nets. When differential nets transition layers, the via model introduces via inductance and via capacitance to the differential trace path hence impacting the insertion loss budget of the differential traces. Different parameters can be slightly modified on this via demo including the length of vias, the anti-plane spacing , the length of differential traces along with changes in stack up. If the board design has buried vias, then this 6 layer model is perfect for optimizing the various parameters associated with the board designs.

For designs within manufacturing, the +/-20 % impedance mismatch due to the manufacturing vendor also needs to be taken into account when designing insertion loss budgets.

Basic rule of thumb design guidelines include why does the insertion loss decrease when the dielectric constant value is changed, what is the impact on the mismatch in impedance when the via length is increased, why is optimizing power distribution networks important?

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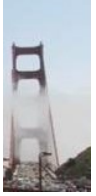

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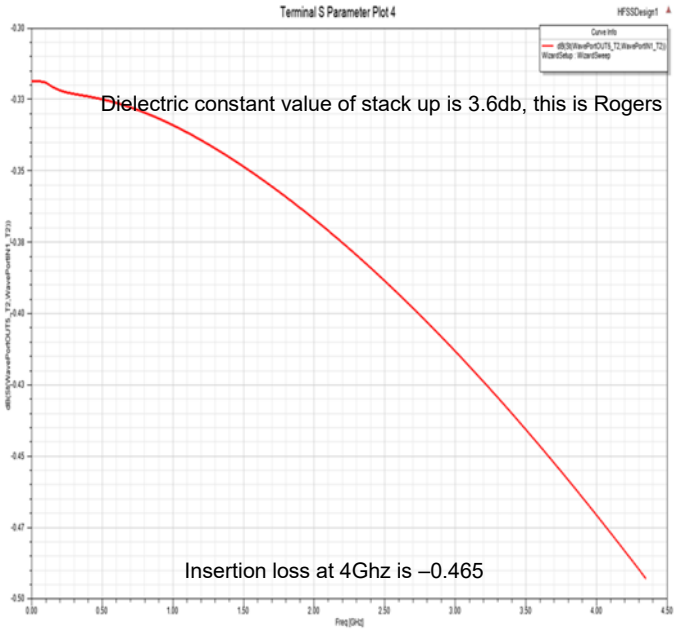
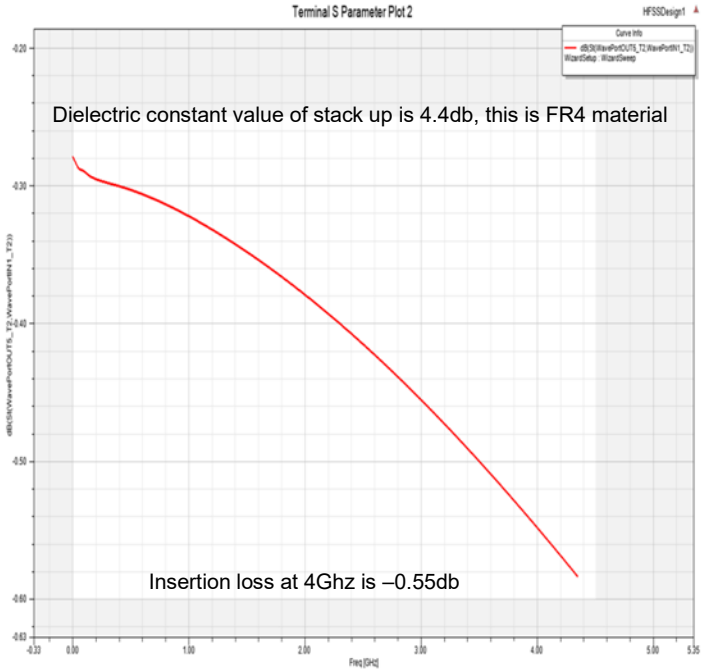
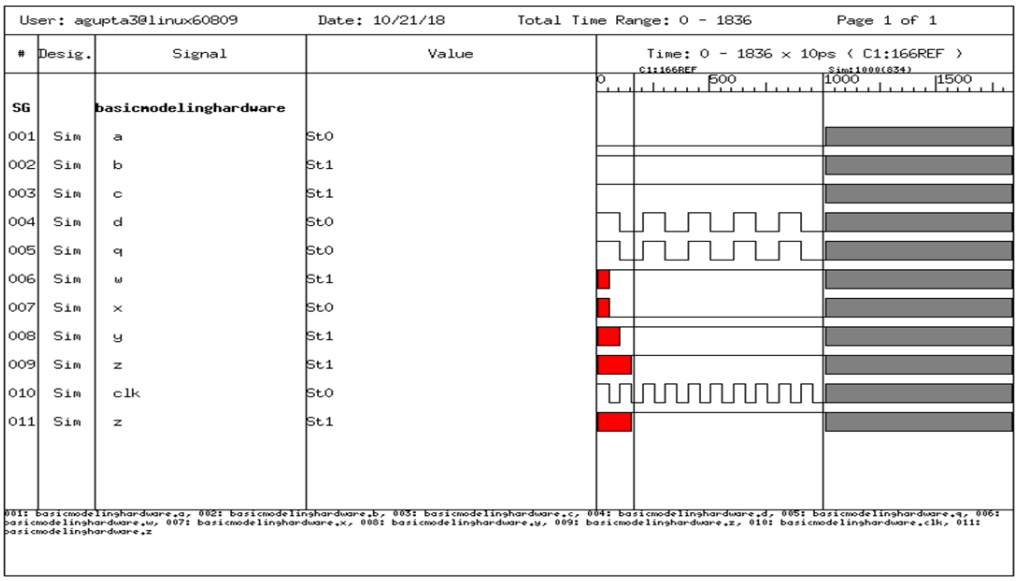




Basic Digital Design with Verilog

Basic Digital design experience includes basic concepts of combinatorial and sequential logic, crossing time domains, understanding propagation delays. Professional experience includes coding design verification test cases in Verilog to test product functionality. These skills are important for a board designer to interact effectively with the FPGA designers responsible for complex design, contributing to architectural level meetings, contributing to team brainstorming sessions and being able to make effective decisions.



Please do contact me at your earliest convenience.

Regards
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617-602-2179

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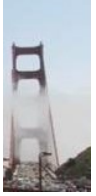

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PROFESSIONAL ACCOMPLISHMENTS

- Product Marketing: Applied engineering experience towards generating marketing collateral for new product features 2017
- Team projects on collecting requirements for a data acquisition design and coordinating changes of a multi-die system on chip. 2015
- Global team experience in collecting product requirements, executing schedules and delivering products. 2012-2014
- Pro-active in creating risk mitigation strategies by improving product quality through complex simulations. 2012-2014
- Generating project cost estimates and identifying risk to key stakeholders on project deliverables. 2011-2014
- Lead designer: Base instrument for a high speed (>5Ghz) test subsystem, active in the field. 2010
- Technical leadership experience: Initiated verification process improvements which expedited design schedules. 2008-2009
- Agile methodology product development processes and board design accomplishments including analog circuit design. 2007
- Outstanding academic achievements include excellent test scores, top ten in my undergraduate institute along with an MSEE and MBA. Latest accomplishments includes design coursework in Santa Clara, California and Northeastern University Boston, MA
- Collateral projects include an investment portfolio, generating market capital gains of $4688.65 with an investment upwards of $20,000.

EDUCATION

Northeastern University, **Master of Science**, Graduate School of Engineering, evening classes, Boston, MA Present
Santa Clara University, Graduate School of Engineering, **ASIC Design and Test Certificate** program, San Francisco Bay Area **2018**
Babson College, Graduate School of Business, **Master of Business Administration**, G.P.A 3.34, evening classes, Wellesley, MA 2014
Northeastern University, **Master of Science**, Electrical Engineering, Major: Computer Eng, G.P.A 3.26, evening classes, Boston, MA 2006
L.D College of Engineering, **Bachelor of Engineering**, Major: Electrical Engineering, G.P.A 3.95, Ahmedabad, Gujarat, India 2003

PROFESSIONAL HARDWARE DESIGN ENGINEERING SKILL SET

- HyperLynx Signal Integrity and Power Integrity Analysis
- High speed board design process with production level designs
- Advanced statistical analysis with Excel applied academic concepts focused on quality control and regression testing
- Ansys HFSS 3DFEM simulations
- Advanced Design Systems with Momentum and signal integrity analysis
- 5+ years of experience with testing and designing embedded systems for production level designs at Teradyne
- C++ in MS Visual Studio. Net and engineering prototype bring-up
- Minor embedded firmware design experience with a load board design
- Schematic design experience includes Allegro Project Manager and collaboration with PCB layout design teams
- Sigrity Power Integrity Analysis on Device Interface Boards
- Basic Digital Design using Verilog and company confidential design tools
- PSpice simulations with Simulink and OrCad at Cadence Design System, published technical content on Cadence.com
- Production level design testing
- Ansys Signal and Power Integrity Analysis
- Academic experience with Eclipse, Synopsys and ModelSim

PROFESSIONAL EXPERIENCE

Cadence Design System, Technical Product Marketing Internship , Chelmsford, MA, HQ San Jose 2017
Generated technical marketing content focused on the value proposition of product releases. Published content on cadence.com

Self employed, Global real estate investment portfolio with high appreciation rates 2016

Draper Laboratory, Digital Electronics Design Engineer, HQ Cambridge, MA 2015
- Designed a high speed signal degradation risk analysis on a nanometer substrate of a system-in-package design
- Utilized industry level signal and power integrity simulation tools to evaluate the power distribution network of the design

Teradyne Inc., HQ North Reading, MA 2005-2014
Project Manager I (technical) *2011-2014*
- Gathered requirements with application teams on hardware device interface boards to provide an optimal signal delivery solution.
- Conducted high speed signal integrity simulations and power integrity simulations on RF and high speed device interface boards.
- Cross functional team experience with the hardware design team, applications engineering and signal integrity design team.

Hardware Engineer II *2006-2011*
- Multi-layer board design experience on multiple projects and designs includes schematic design, timing analysis, component and routing guidelines. Contributed to the engineering board proto-type bring up process and gained industry standard knowledge on the board design process.
- Experience with component selection and schematic design for power fets, convertors, amplifiers, Xilinx FPGAs, buffers, clock generation and distribution circuitry, memory chips and high speed communication links. Gained industry standard knowledge on high speed memory interfaces.
- Initiated design process improvements for hardware design and hardware verification regression cycles for firmware releases.
- Minor FPGA design and FPGA design verification experience with Virtex FPGAs and industry level synthesis tools for production level hardware.
- Programming, regression testing and automation experience includes writing design verification test cases in C and Visual C++.

Application Engineer *2005-2006*
- Coded application level test cases to test product functionality, created test plans and evaluated functional product test coverage.

Northeastern University, 360 Huntington Avenue, Boston, MA 02115
- *Graduate Teaching Assistant,* Boston, MA 02115 2004-2005 **|** On-campus employment, Snell Library, Boston, MA 2004

Steel Point Technologies, *Technical Support Intern,* Software engineering internship involving data processing, Boston, MA 2004