THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY.
THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: GLOBAL SIGNALS
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: KU15P POWER AND SIGNAL (NON-MGT)
6: VU7P POWER AND SIGNAL (NON-MGT)
7: KU15P MGT TRANSCEIVERS
8: VU7P MGT TRANSCEIVERS

TO DO:

CHECK "bc" AND "ac" PREFIXES ON AC-COUPLED SIGNALS

ON VU7P QUAD "S', CHANGE "...133" TO "...S" IN PIN NAMES

ON VU7P QUAD "A-J', CHANGE "...GTH" TO "...GTY" IN PIN NAMES

ASSIGN AND LABEL I2C ADDRESSES

SOLDERPASTE PATTERNS FOR UEC5_UCCE FOOTPRINT

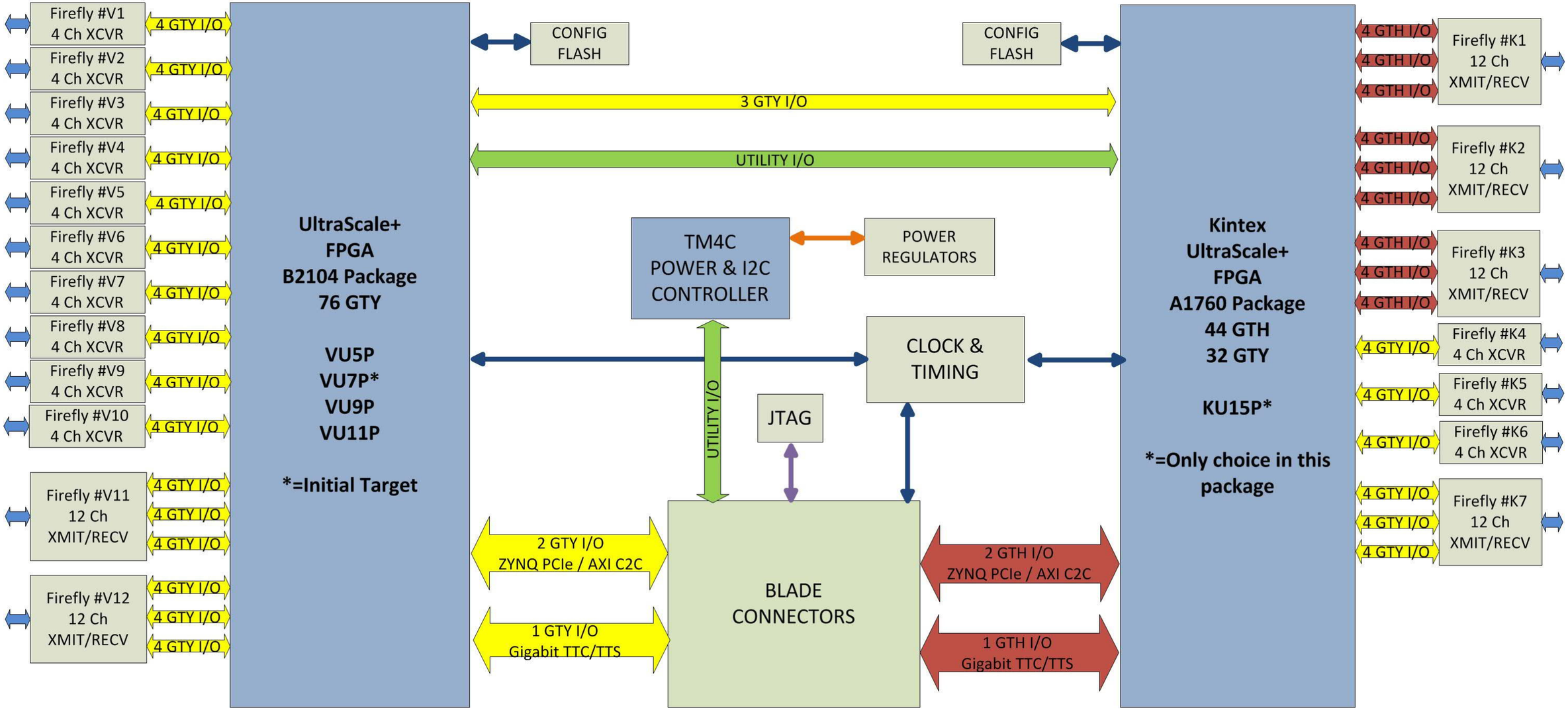
NETS TO STUDY / DOCUMENT

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 1.01: NOTES

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 1 of 74



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 1.02: BLOCK DIAGRAM

Size | Document Number: 6089-103 | Rev: A

Date: Wednesday, March 06, 2019 | Sheet 2 of 74

KU15P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

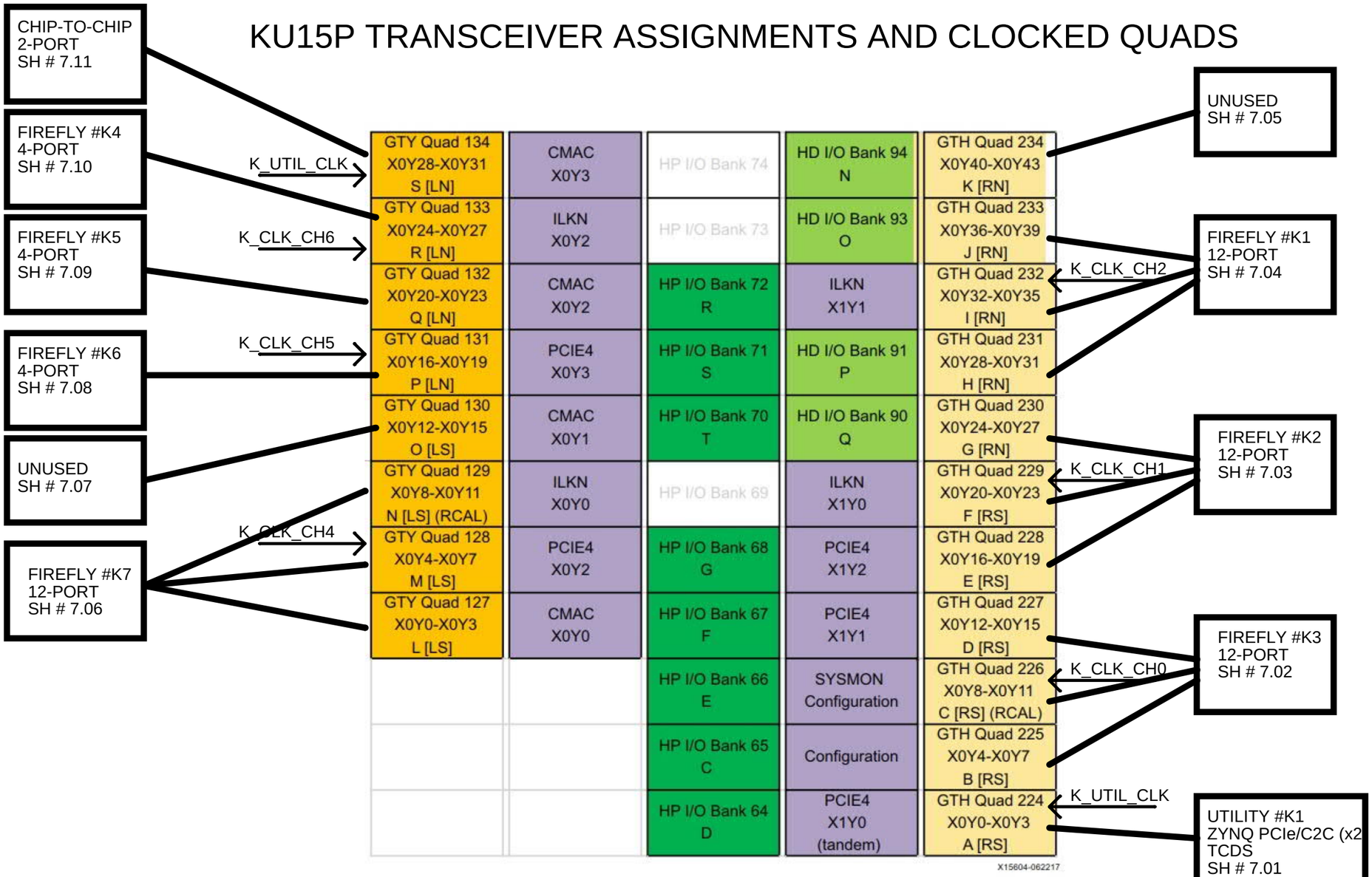


Figure 1-86: **XCKU15P Banks in FFVA1760 Package**

EACK "K_CLK_CHn" CONSISTS OF TWO CLOCKS.
ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.03: KU15P TRANSCEIVERS		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 3 of 74	

VU7P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

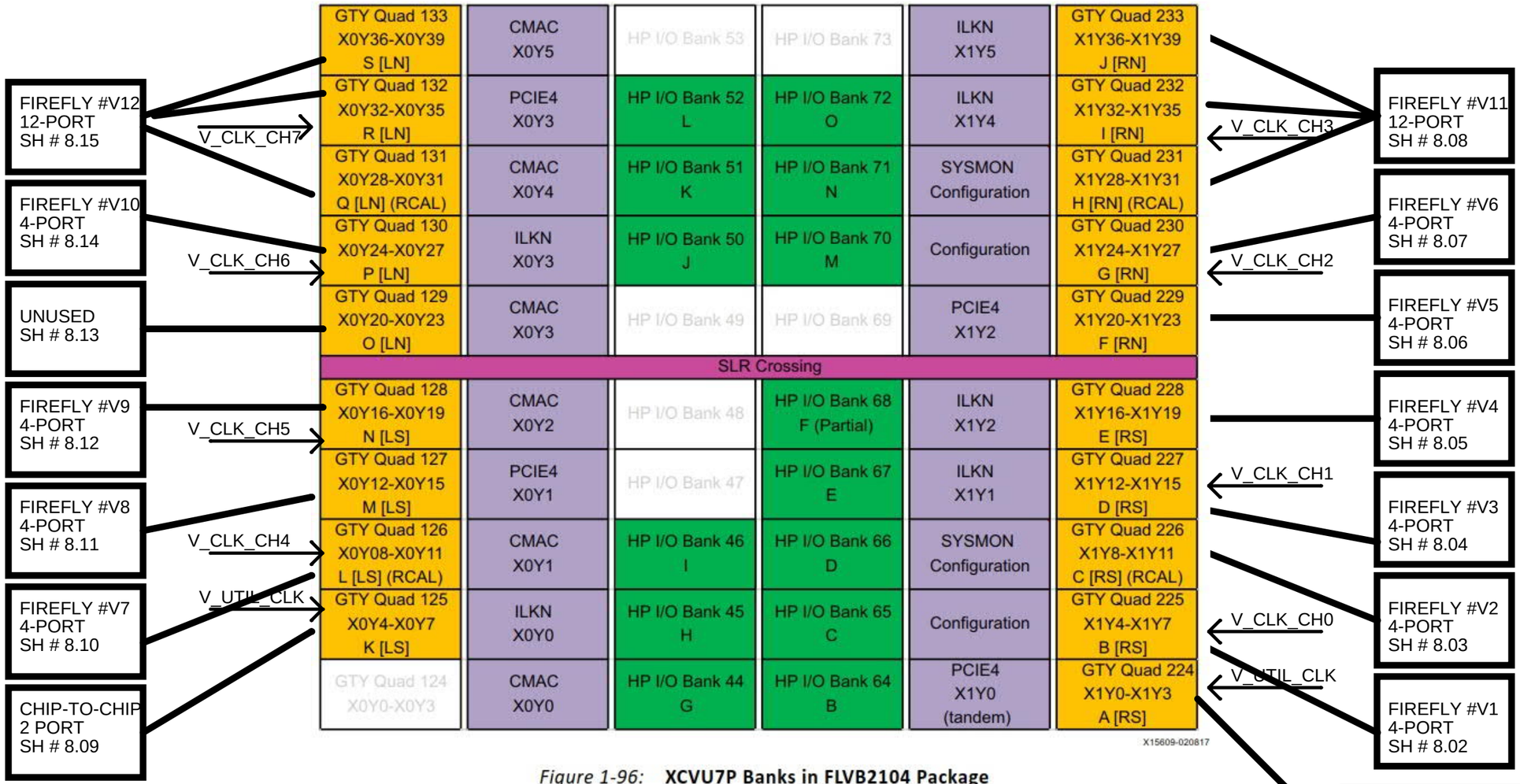


Figure 1-96: **XCVU7P Banks in FLVB2104 Package**

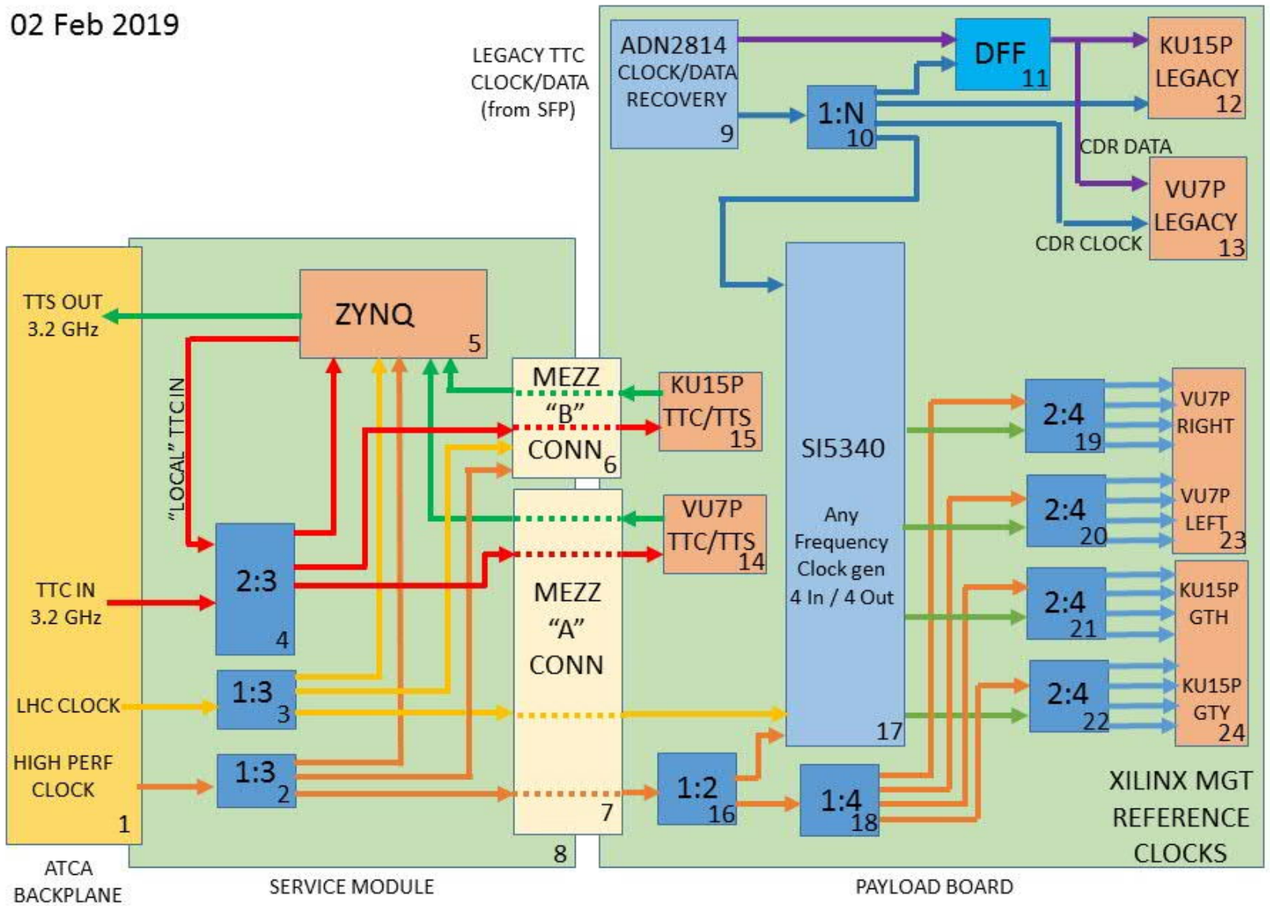
EACK "V_CLK_CHn" CONSISTS OF TWO CLOCKS.
ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.04: VU7P TRANSCEIVERS		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 4 of 74	

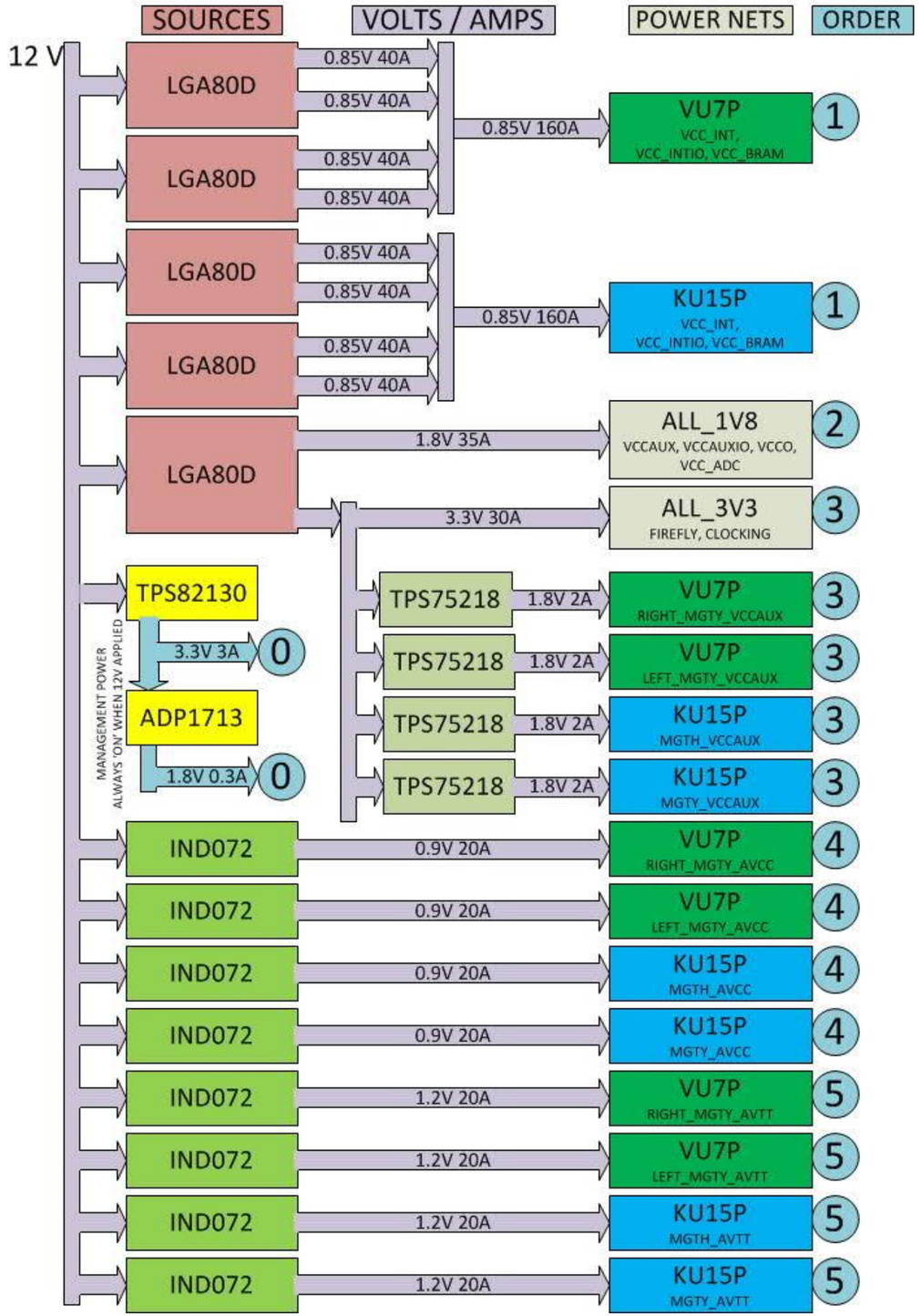
BU/CU Apollo ATCA Backplane Signal Distribution

02 Feb 2019



Charlie Strohman crs5@cornell.edu

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.05: LHC SIGNAL DISTRIBUTION		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 5 of 74	



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 1.06: POWER DISTRIBUTION

Size	Document Number	Rev
	6089-103	A

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J17
CON4
1 VCC_12V
2 VCC_12V
3 GND
4 GND

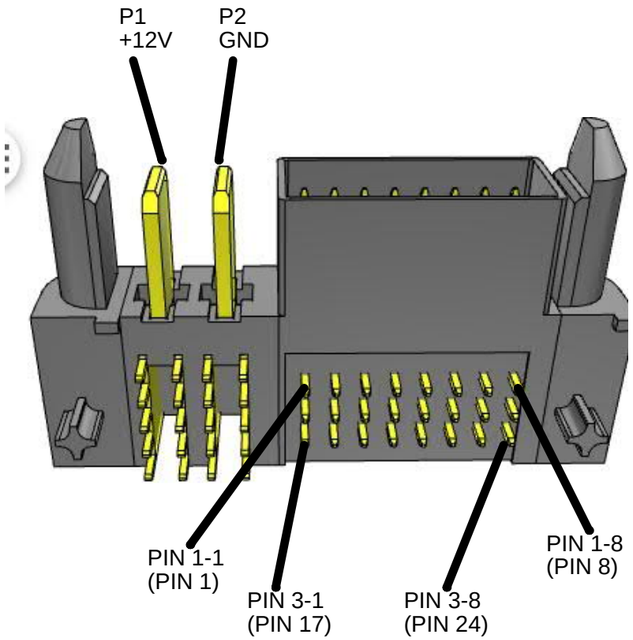
Bench Top Power Inlet

P1
ET60T-D02-3-08-000

VCC_12V	P1-1	P1-1	PWR_GOOD 1-1	1 → BLADE_POWER_OK PG 11,17
	P1-2	P1-2	TMS 1-2	2 → BLADE_JTAG_TMS PG 10
	P1-3	P1-3	TDO 1-3	3 → BLADE_JTAG_TDO PG 10
	P1-4	P1-4	TX_IPMC 1-4	4 → R726 0 0603 → BLADE_IPMC_TX PG 11
	P1-5	P1-5	TX_ZYNQ 1-5	5 → R728 0 0603 → BLADE_ZYNQ_TX PG 11
	P1-6	P1-6	SENSE_SDA 1-6	6 → BLADE_MASTER_I2C_SDA PG 25
	P1-7	P1-7	GPIO0 1-7	7 → PWR_ENABLE PG 11
	P1-8	P1-8	GPIO2 1-8	8 → BLADE_ZYNQ_GPIO2 PG 11
	P1-9	P1-9	GND_LOGIC 2-1	9 → GND
	P1-10	P1-10	2-2	10 → GND
GND	P2-1	P2-1	2-3	11 → GND
	P2-2	P2-2	2-4	12 → GND
	P2-3	P2-3	2-5	13 → GND
	P2-4	P2-4	2-6	14 → GND
	P2-5	P2-5	2-7	15 → GND
	P2-6	P2-6	2-8	16 → GND
	P2-7	P2-7	EN 3-1	17 → BLADE_POWER_EN PG 11
	P2-8	P2-8	TCK 3-2	18 → BLADE_JTAG_TCK PG 10
	P2-9	P2-9	TDI 3-3	19 → BLADE_JTAG_TDI PG 10
	P2-10	P2-10	RX_IPMC 3-4	20 → R727 0 0603 → BLADE_IPMC_RX PG 11
			RX_ZYNQ 3-5	21 → R729 0 0603 → BLADE_ZYNQ_RX PG 11
			SENSE_SCL 3-6	22 → BLADE_MASTER_I2C_SCL PG 25
			GPIO1 3-7	23 → BLADE_ZYNQ_GPIO1 PG 11
			/PS_RST 3-8	24 ×

/PS_RST IS NOT USED IN THIS DESIGN

ZERO-OHM RESISTORS R726 AND R727 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES. THE SAME IS TRUE FOR R728 AND R729.



ET60T-D02-3-08-000

THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.

SP2 (1 2 3) DNI
SP1 (1 2 3) DNI

THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINKS

H13 DNI, H12 DNI, H11 DNI
H8 DNI, H7 DNI, H6 DNI

THESE HOLES ARE FOR MOUNTING THE TOP COVER

H5 DNI, H18 DNI, H4 DNI
H17 DNI, H3 DNI, H16 DNI

THESE HOLES ARE FOR MOUNTING THE BOTTOM COVER

H1 DNI, H14 DNI, H9 DNI
H15 DNI, H10 DNI, H2 DNI

THESE SHAPES DEFINE MECHANICAL OBJECTS THAT SHOULD BE IN THE BILL OF MATERIALS.

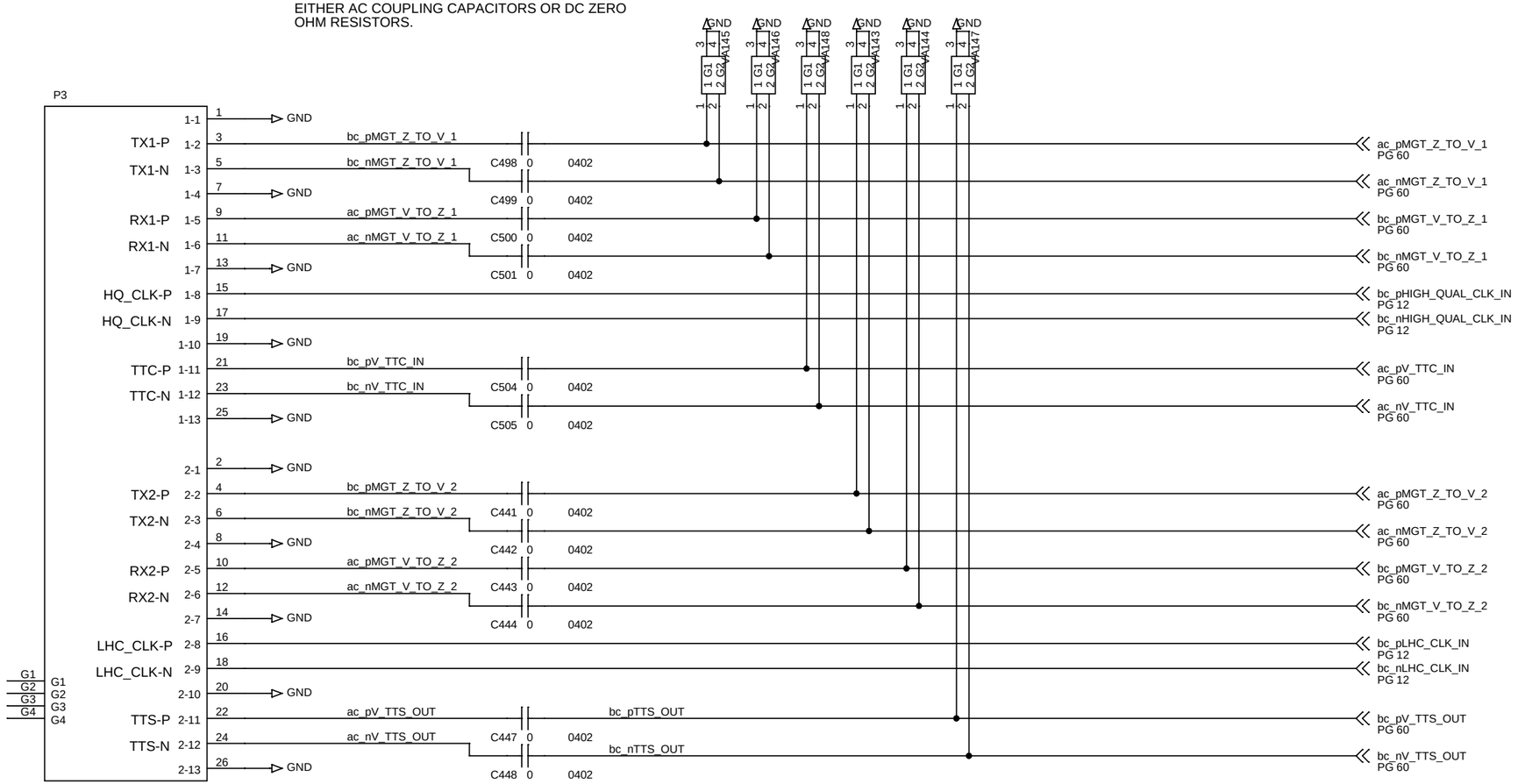
BR1 BRACKET, BR2 BRACKET, BR3 BRACKET

BRACKETS FOR SUPPORTING A SUB-FRONT PANEL

M1 KU15P HEATSINK
M23 HEATSINK PLATE
M3 M3 STANDOFF, M4 M3 STANDOFF, M5 M3 STANDOFF, M6 M3 STANDOFF, M7 M3 STANDOFF, M8 M3 STANDOFF
M2 VU7P HEATSINK
M24 HEATSINK PLATE
M9 M3 STANDOFF, M10 M3 STANDOFF, M11 M3 STANDOFF, M12 M3 STANDOFF, M13 M3 STANDOFF, M14 M3 STANDOFF
M15 FIREFLY HEATSINK (LEFT SIDE)
M16 M2.5 STANDOFF, M17 M2.5 STANDOFF, M18 M2.5 STANDOFF
M19 FIREFLY HEATSINK (RIGHT SIDE)
M20 M2.5 STANDOFF, M21 M2.5 STANDOFF, M22 M2.5 STANDOFF

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.01: BLADE POWER CONNECTOR		
Size	Document Number: 6089-103	Rev: A
Date: Friday, August 30, 2019	Sheet 7 of 74	

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.



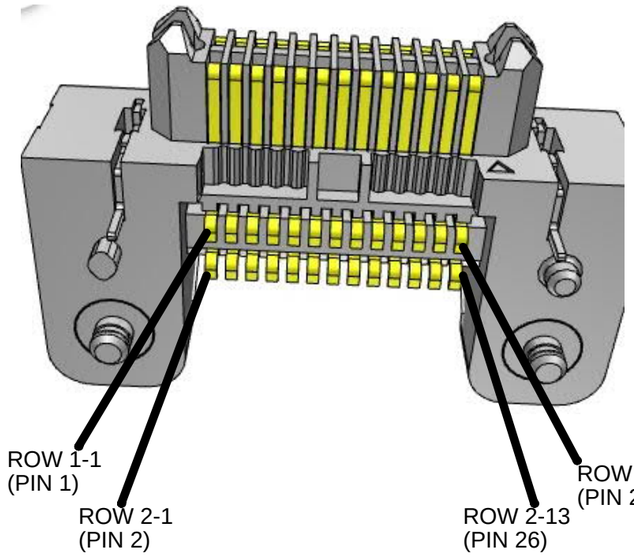
AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

REPLACED THE DC BLOCKING CAPACITORS WITH ZERO-OHM RESISTORS. THE SERVICE BLADE ALREADY PROVIDES CAPACITORS.

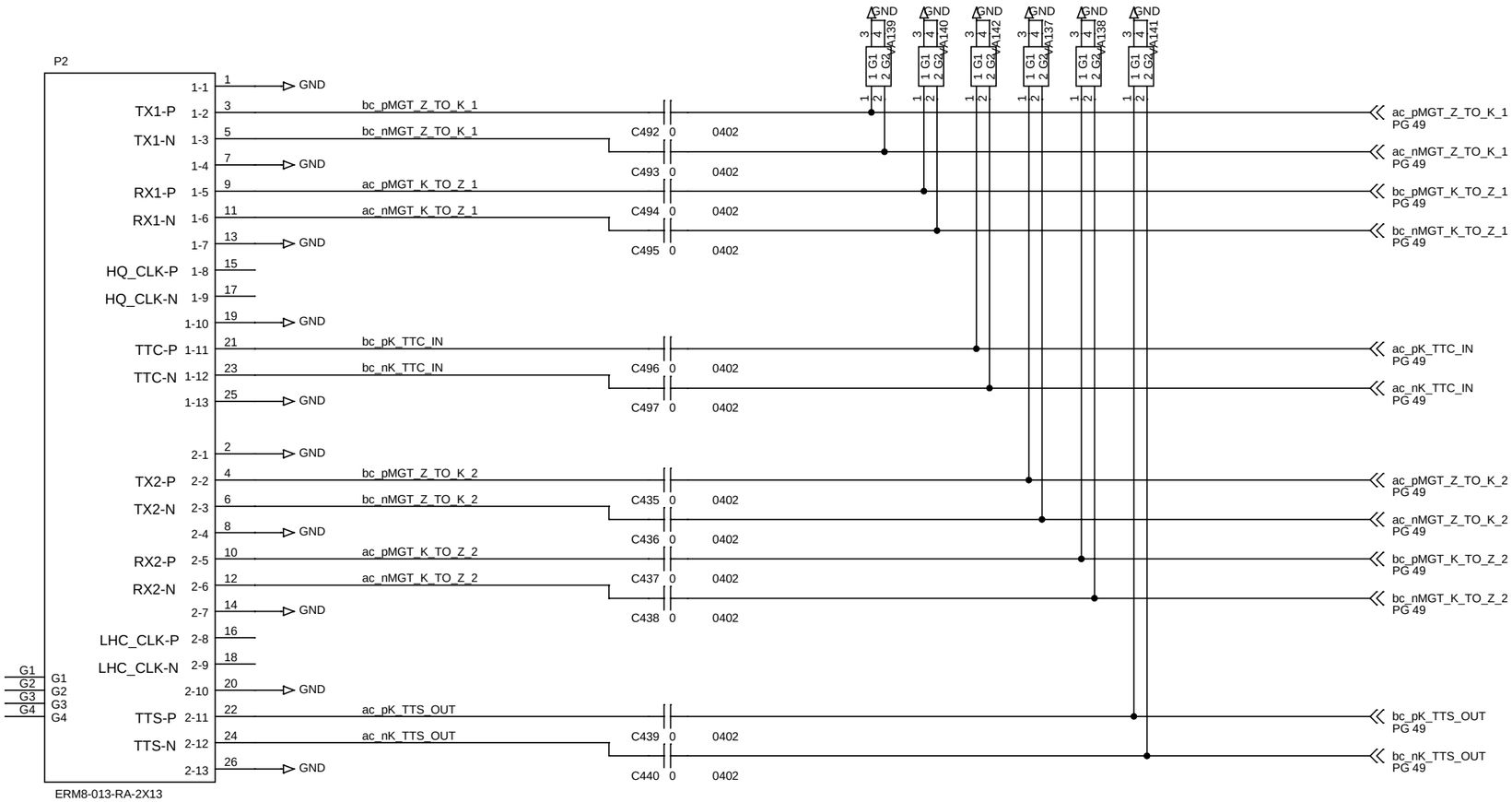
VU7P AND BACKPLANE CLOCK SIGNALS ONLY



ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.02: BLADE HS CONNECTOR #1		
Size	Document Number: 6089-103	Rev: A
Date: Friday, March 08, 2019	Sheet 8 of 74	

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.



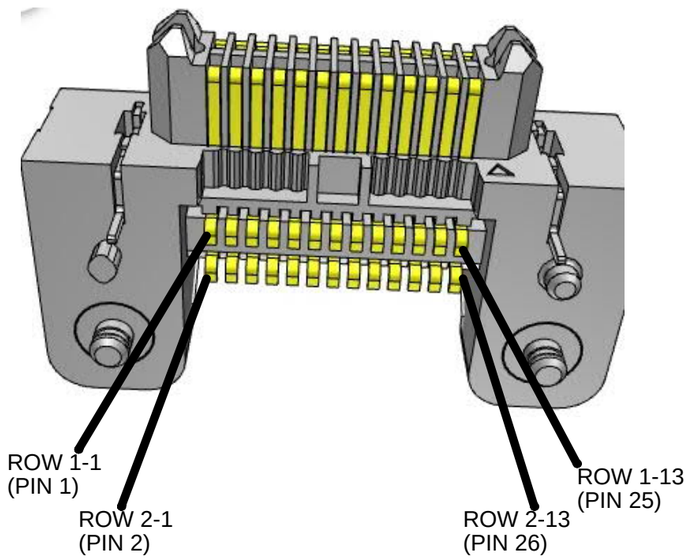
AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

REPLACED THE DC BLOCKING CAPACITORS WITH ZERO-OHM RESISTORS. THE SERVICE BLADE ALREADY PROVIDES CAPACITORS.

KU15P SIGNALS ONLY



ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.03: BLADE HS CONNECTOR #2

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TO BYPASS A DEVICE, CONNECT A JUMPER FROM 1 TO 3.
TO INCLUDE A DEVICE IN THE CHAIN, CONNECT A JUMPER FROM 1 TO 2 AND FROM 3 TO 4.
AS ILLUSTRATED, THE CONTROLLER AND THE VU7P ARE PART OF THE CHAIN, AND THE KU15P IS BYPASSED.

BLADE JTAG

BLADE_JTAG_TMS PG 7

VCC_M3V3 — R108 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

U49 74LVC1G126 — R92 33 0603 — V_TMS_1V8
U53 74LVC1G126 — R98 33 0603 — K_TMS_1V8
U57 74LVC1G126 — R107 33 0603 — C_TMS_3V3
U50 74LVC1G125 — R95 33 0603
U55 74LVC1G125 — R101 33 0603
U60 74LVC1G125 — R109 33 0603
U62 74LVC1G126 — R113 33 0603 — V_TCK_1V8
U77 74LVC1G126 — R123 33 0603 — K_TCK_1V8
U84 74LVC1G126 — R133 33 0603 — C_TCK_3V3
U67 74LVC1G125 — R116 33 0603
U78 74LVC1G125 — R130 33 0603
U86 74LVC1G125 — R136 33 0603

VCC_M3V3 — R94 10K 0603

VCC_M3V3 — R115 10K 0603

BLADE JTAG

BLADE_JTAG_TCK PG 7

VCC_M3V3 — R134 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

FORCE JTAG CABLE

IF EITHER THE JUMPER IS IN PLACE, OR THE PROGRAMMING CABLE IS PLUGGED IN, THE OUTPUT OF THIS BUFFER WILL BE LOW. THIS WILL ENABLE ALL OF THE DRIVERS RELATED TO THE CABLE SIGNALS, AND DISABLE ALL OF THE DRIVERS RELATED TO THE MAIN BLADE.

VCC_M3V3 — R70 10K 0603 — J12 JUMPER — GND

U37 74LVC1G125 — GND — VCC_M3V3

THE JTAG REFERENCE IS 3.3 VOLTS.

J1 CON_2X7_RA
CONN_JTAG_TMS
CONN_JTAG_TCK
CONN_JTAG_TDO
CONN_JTAG_TDI

USE THE JUMPER IF PIN 13 IS NOT AUTOMATICALLY PULLED LOW WHEN THE CABLE IS PLUGGED IN.

PIN 13 SHOULD BE PULLED LOW WHEN THE CABLE IS PLUGGED IN.

FRONT PANEL JTAG

BLADE JTAG

BLADE_JTAG_TDI PG 7

VCC_M3V3 — R86 10K 0603

VCC_M3V3 — R82 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

TDI_3V3

U42 74LVC1G126 — R85 33 0603 — VCC_M3V3 — GND
U41 74LVC1G125 — R83 33 0603 — VCC_M3V3 — GND

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE MAIN BLADE OR THE EXTERNAL PROGRAMMER.

U38 74AUP1T34 — R72 33 0603 — VCC_M1V8 — VCC_M3V3 — GND

BLADE JTAG

U40 74AUP1T34 — R81 33 0603 — BLADE_JTAG_TDO PG 7 — VCC_M1V8 — VCC_M3V3 — GND

U66-43 FPGA_VU7P_B2104 — JTAG

JUMPER_2X2 J13 — BYPASS JUMPER

V_TDO — AC13 — TDO_0
V_TDI — AE15 — TDI_0
V_TMS_1V8 — AG15 — TMS_0
V_TCK_1V8 — AE13 — TCK_0

VU7P

U7 74LVC1G125 — R11 33 0603 — VCC_M1V8 — GND

U65-11 FPGA_KU15P_A1760 — JTAG

JUMPER_2X2 J14 — BYPASS JUMPER

K_TDO — AK16 — TDO_0
K_TDI — AJ15 — TDI_0
K_TMS_1V8 — AJ17 — TMS_0
K_TCK_1V8 — AK15 — TCK_0

KU15P

TDI_1V8

U9 74LVC1G125 — R25 33 0603 — VCC_M1V8 — GND

U52-1 TM4C1290NCPDT

JUMPER_2X2 J15 — BYPASS JUMPER

C_TDO — 97 — JTAG_TDO
C_TDI — 98 — JTAG_TDI
C_TMS_3V3 — 99 — JTAG_TMS
C_TCK_3V3 — 100 — JTAG_TCK

CONTROLLER

VCC_M3V3 — C771 0.1 UF 0402 — C766 0.1 UF 0402 — C752 0.1 UF 0402 — C747 0.1 UF 0402 — C825 0.1 UF 0402 — GND
VCC_M3V3 — C812 0.1 UF 0402 — C809 0.1 UF 0402 — C803 0.1 UF 0402 — C826 0.1 UF 0402 — GND
VCC_M1V8 — C794 0.1 UF 0402 — C786 0.1 UF 0402 — C781 0.1 UF 0402 — C778 0.1 UF 0402 — C762 0.1 UF 0402 — GND
VCC_M1V8 — C761 0.1 UF 0402 — C758 0.1 UF 0402 — C755 0.1 UF 0402 — C969 0.1 UF 0402 — C971 0.1 UF 0402 — GND

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.04: JTAG CHAIN

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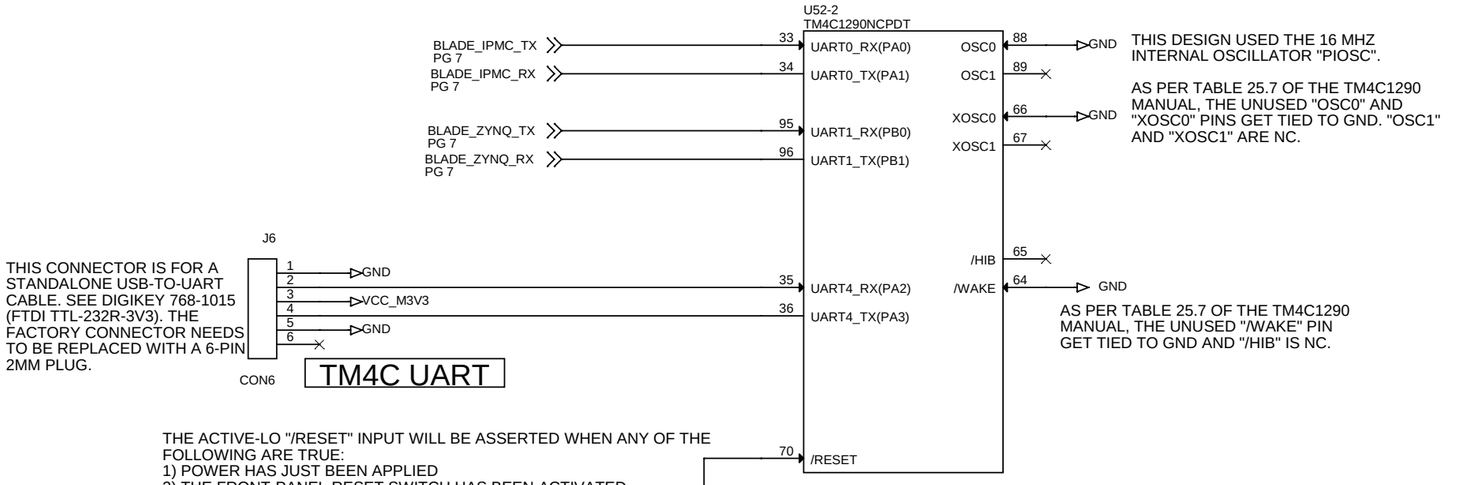

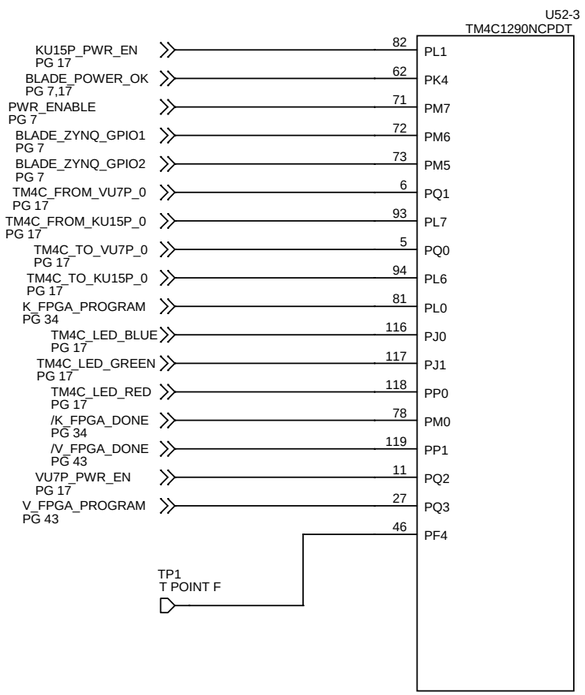

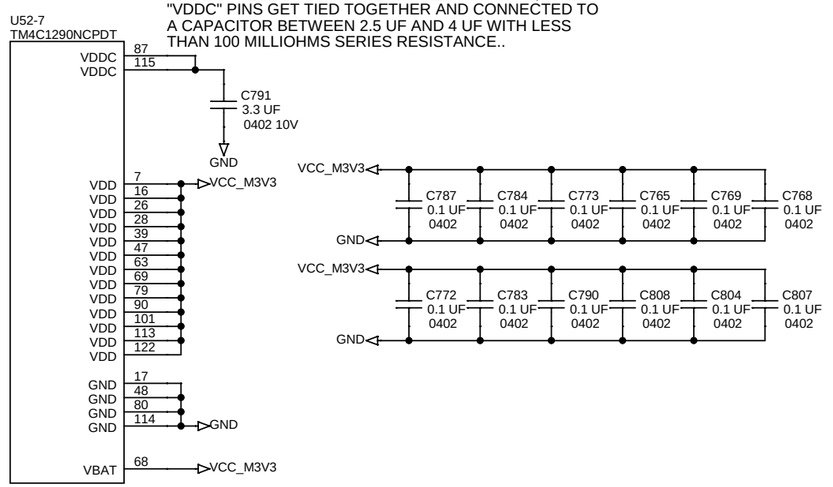

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.05 CONTROLLER		
Size	Document Number: 6089-103	Rev: A
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DO WE NEED TO ADD A BUFFER TO GET AN LHC-BASED CLOCK INTO THE FPGA LOGIC SECTION? WILL USING THE "TXOUTCLK" FROM A GTH/GTY BLOCK BE ADEQUATE?

bc_pLEGACY_CLK PG 14 → C1 0.1 UF 0402 → ac_pLEGACY_CLK
bc_nLEGACY_CLK PG 14 → C2 0.1 UF 0402 → ac_nLEGACY_CLK
R129 49.9 0402, R131 49.9 0402, C216 0.1 UF 0402 → GND
bc_pLHC_CLK_IN PG 8 → C445 0.1 UF 0402 → ac_pLHC_CLK_IN
bc_nLHC_CLK_IN PG 8 → C446 0.1 UF 0402 → ac_nLHC_CLK_IN
R120 49.9 0402, R119 49.9 0402, C205 0.1 UF 0402 → GND
bc_pHIGH_QUAL_CLK_IN PG 8 → C502 0.1 UF 0402 → ac_pHIGH_PERF_CLK_IN
bc_nHIGH_QUAL_CLK_IN PG 8 → C503 0.1 UF 0402 → ac_nHIGH_PERF_CLK_IN
R138 49.9 0402, R139 49.9 0402, C250 0.1 UF 0402 → GND

U81-1 SI5340

pXTAL	5	XA	FB_IN /FB_IN 41, 42
X1	2	X1_SHIELD	
48 MHz	4	X2_SHIELD	OUT_0 /OUT_0 → 20 pSYNTH_CLK0, 19 nSYNTH_CLK0
	7		
nXTAL	6	XB	OUT_1 /OUT_1 → 25 pSYNTH_CLK1, 24 nSYNTH_CLK1
			OUT_2 /OUT_2 → 31 pSYNTH_CLK2, 30 nSYNTH_CLK2
ac_pLEGACY_CLK	43	IN_0 /IN_0	OUT_3 /OUT_3 → 36 pSYNTH_CLK3, 35 nSYNTH_CLK3
ac_nLEGACY_CLK	44		
ac_pLHC_CLK_IN	1	IN_1 /IN_1	
ac_nLHC_CLK_IN	2		
ac_pHIGH_PERF_CLK_IN	10	IN_2 /IN_2	
ac_nHIGH_PERF_CLK_IN	11		

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

WE DO NOT HAVE AN UNUSED OUTPUT, SO WE CAN NOT USE FEEDBACK. ZERO-DELAY BUFFERING IS NOT A REQUIREMENT, NOR IS FIXED PHASE BETWEEN OUTPUTS.

THE SPLIT TERMINATOR WITH A CAPACITOR TO GND IS USED FOR CLOCKS COMING FROM OFF THE BOARD. CLOCKS THAT ARE STRICTLY WITHIN THE BOARD USE SIMPLE 100 OHM TERMINATORS.

U80 SI53340 1:2

ac_pHIGH_PERF_CLK_IN	6	CLK0 /CLK0	Q0 /Q0 → 9 pHIGH_PERF_CLK_BUF1, 10 nHIGH_PERF_CLK_BUF1
ac_nHIGH_PERF_CLK_IN	7		
	3	CLK1 /CLK1	Q1 /Q1 → 11 pHIGH_PERF_CLK_BUF0, 12 nHIGH_PERF_CLK_BUF0
	4		
	8	NC8	Q2 /Q2 → 13, 14
R126 4.7K 0603 → GND	2	CLK_SEL	Q3 /QE → 15, 16
	5	VDD	← VCC_3V3
	1, 17	GND PAD	→ GND; VCC_3V3 → C751 1 UF 0402 10v → GND

<Implementation>

DC COUPLED LVDS

R121 100 0402, R110 100 0402

U61 SI53340 1:4

	6	CLK0 /CLK0	Q0 /Q0 → 9 pHIGH_PERF_CLK0, 10 nHIGH_PERF_CLK0
	7		
	3	CLK1 /CLK1	Q1 /Q1 → 11 pHIGH_PERF_CLK1, 12 nHIGH_PERF_CLK1
	4		
	8	NC8	Q2 /Q2 → 13 pHIGH_PERF_CLK2, 14 nHIGH_PERF_CLK2
R105 4.7K 0603 → GND	2	CLK_SEL	Q3 /QE → 15 pHIGH_PERF_CLK3, 16 nHIGH_PERF_CLK3
	5	VDD	← VCC_3V3
	1, 17	GND PAD	→ GND; VCC_3V3 → C767 1 UF 0402 10v → GND

<Implementation>

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

AC COUPLED LVDS

U83 SI53340 2:4

pHIGH_PERF_CLK0	6	CLK0 /CLK0	Q0 /Q0 → 9 bc_pV_CLK1_CHAN0, 10 bc_nV_CLK1_CHAN0
nHIGH_PERF_CLK0	7		
pSYNTH_CLK0	3	CLK1 /CLK1	Q1 /Q1 → 11 bc_pV_CLK1_CHAN1, 12 bc_nV_CLK1_CHAN1
nSYNTH_CLK0	4		
			Q2 /Q2 → 13 bc_pV_CLK1_CHAN2, 14 bc_nV_CLK1_CHAN2
	8	NC8	Q3 /QE → 15 bc_pV_CLK1_CHAN3, 16 bc_nV_CLK1_CHAN3
R135 4.7K 0603 → GND	2	CLK_SEL	
V_GTY1_SEL_SYNTH PG 27	5	VDD	← VCC_3V3
	1, 17	GND PAD	→ GND; VCC_3V3 → C754 1 UF 0402 10v → GND

<Implementation>

R127 100 0402, R132 100 0402

C228 0.1 UF 0402 → ac_pV_CLK1_CHAN0 PG 61
C232 0.1 UF 0402 → ac_nV_CLK1_CHAN0 PG 61 — QUAD B
C241 0.1 UF 0402 → ac_pV_CLK1_CHAN1 PG 63
C244 0.1 UF 0402 → ac_nV_CLK1_CHAN1 PG 63 — QUAD D
C251 0.1 UF 0402 → ac_pV_CLK1_CHAN2 PG 66
C257 0.1 UF 0402 → ac_nV_CLK1_CHAN2 PG 66 — QUAD G
C269 0.1 UF 0402 → ac_pV_CLK1_CHAN3 PG 67
C273 0.1 UF 0402 → ac_nV_CLK1_CHAN3 PG 67 — QUAD I

THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.

U56 SI53340 2:4

pHIGH_PERF_CLK1	6	CLK0 /CLK0	Q0 /Q0 → 9 bc_pV_CLK1_CHAN4, 10 bc_nV_CLK1_CHAN4
nHIGH_PERF_CLK1	7		
pSYNTH_CLK1	3	CLK1 /CLK1	Q1 /Q1 → 11 bc_pV_CLK1_CHAN5, 12 bc_nV_CLK1_CHAN5
nSYNTH_CLK1	4		
			Q2 /Q2 → 13 bc_pV_CLK1_CHAN6, 14 bc_nV_CLK1_CHAN6
	8	NC8	Q3 /QE → 15 bc_pV_CLK1_CHAN7, 16 bc_nV_CLK1_CHAN7
R106 4.7K 0603 → GND	2	CLK_SEL	
V_GTY2_SEL_SYNTH PG 27	5	VDD	← VCC_3V3
	1, 17	GND PAD	→ GND; VCC_3V3 → C780 1 UF 0402 10v → GND

<Implementation>

R97 100 0402, R100 100 0402

C149 0.1 UF 0402 → ac_pV_CLK1_CHAN4 PG 69
C151 0.1 UF 0402 → ac_nV_CLK1_CHAN4 PG 69 — QUAD L
C158 0.1 UF 0402 → ac_pV_CLK1_CHAN5 PG 71
C160 0.1 UF 0402 → ac_nV_CLK1_CHAN5 PG 71 — QUAD N
C162 0.1 UF 0402 → ac_pV_CLK1_CHAN6 PG 73
C166 0.1 UF 0402 → ac_nV_CLK1_CHAN6 PG 73 — QUAD P
C172 0.1 UF 0402 → ac_pV_CLK1_CHAN7 PG 74
C174 0.1 UF 0402 → ac_nV_CLK1_CHAN7 PG 74 — QUAD R

THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.

AC COUPLED LVDS

U87 SI53340 2:4

pHIGH_PERF_CLK2	6	CLK0 /CLK0	Q0 /Q0 → 9 bc_pK_CLK1_CHAN0, 10 bc_nK_CLK1_CHAN0
nHIGH_PERF_CLK2	7		
pSYNTH_CLK2	3	CLK1 /CLK1	Q1 /Q1 → 11 bc_pK_CLK1_CHAN1, 12 bc_nK_CLK1_CHAN1
nSYNTH_CLK2	4		
			Q2 /Q2 → 13 bc_pK_CLK1_CHAN2, 14 bc_nK_CLK1_CHAN2
	8	NC8	Q3 /QE → 15, 16 SPARE
R140 4.7K 0603 → GND	2	CLK_SEL	
K_GTH_SEL_SYNTH PG 27	5	VDD	← VCC_3V3
	1, 17	GND PAD	→ GND; VCC_3V3 → C736 1 UF 0402 10v → GND

<Implementation>

R147 100 0402, R143 100 0402

C286 0.1 UF 0402 → ac_pK_CLK1_CHAN0 PG 50
C281 0.1 UF 0402 → ac_nK_CLK1_CHAN0 PG 50 — QUAD C
C270 0.1 UF 0402 → ac_pK_CLK1_CHAN1 PG 51
C264 0.1 UF 0402 → ac_nK_CLK1_CHAN1 PG 51 — QUAD F
C252 0.1 UF 0402 → ac_pK_CLK1_CHAN2 PG 52
C249 0.1 UF 0402 → ac_nK_CLK1_CHAN2 PG 52 — QUAD I

THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.

U68 SI53340 2:4

pHIGH_PERF_CLK3	6	CLK0 /CLK0	Q0 /Q0 → 9 bc_pK_CLK1_CHAN4, 10 bc_nK_CLK1_CHAN4
nHIGH_PERF_CLK3	7		
pSYNTH_CLK3	3	CLK1 /CLK1	Q1 /Q1 → 11 bc_pK_CLK1_CHAN5, 12 bc_nK_CLK1_CHAN5
nSYNTH_CLK3	4		
			Q2 /Q2 → 13 bc_pK_CLK1_CHAN6, 14 bc_nK_CLK1_CHAN6
	8	NC8	Q3 /QE → 15, 16
R114 4.7K 0603 → GND	2	CLK_SEL	
K_GTY_SEL_SYNTH PG 27	5	VDD	← VCC_3V3
	1, 17	GND PAD	→ GND; VCC_3V3 → C759 1 UF 0402 10v → GND

<Implementation>

R125 100 0402, R117 100 0402

C211 0.1 UF 0402 → ac_pK_CLK1_CHAN4 PG 54
C204 0.1 UF 0402 → ac_nK_CLK1_CHAN4 PG 54 — QUAD M
C200 0.1 UF 0402 → ac_pK_CLK1_CHAN5 PG 56
C191 0.1 UF 0402 → ac_nK_CLK1_CHAN5 PG 56 — QUAD P
C189 0.1 UF 0402 → ac_pK_CLK1_CHAN6 PG 58
C181 0.1 UF 0402 → ac_nK_CLK1_CHAN6 PG 58 — QUAD R

THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.

AC COUPLED LVDS
bc = BEFORE CAPACITOR
ac = AFTER CAPACITOR

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.06: LHC CLOCKING

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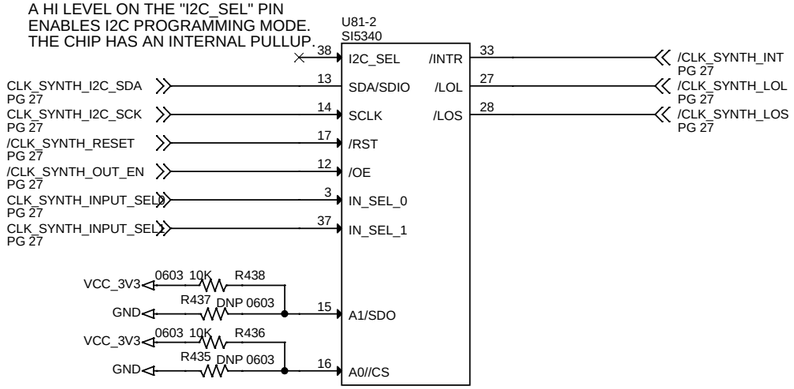
A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

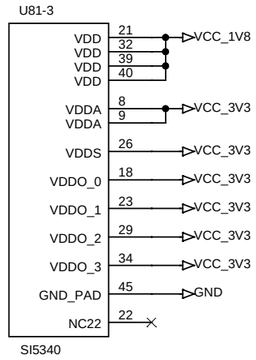


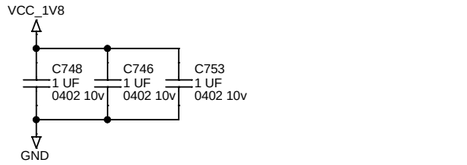
I2C ADDR = 0X77

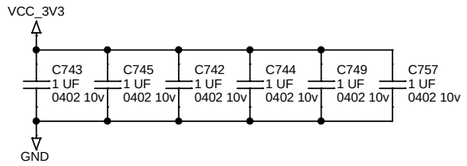
SI5340 I2C ADDRESS:
READ OR WRITE
1 1 1 0 1 A1 A0
RANGE: 0X74 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.







ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.07: LHC CLOCKING SUPPORT

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THIS CIRCUIT ON THIS PAGE IS FOR USE IN THE PROTOTYPE ONLY. IT ALLOWS US TO FEED LEGACY TTC SIGNALS INTO THE SYSTEM.

U13-2
SFP_CONN_WITH_CAGE

U13-1
SFP_CONN_WITH_CAGE

THE SFP I2C SIGNALS AND CONTROL LINES ARE WIRED TO THE CHIPS THAT SUPPORT ACCESS TO THE KU15P OPTICS. THEY CAN BE CONNECTED ELSEWHERE IF DESIRED.

AMC13 CLK IN

SFP+ CONNECTOR TO RECEIVE ENCODED TTC CLOCK/DATA STREAM.

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTS_OUT" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS WILL GENERATE THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

J11 JUMPER_DIFF

THESE RESISTORS MUST BE NEAR THE 65LVDS100 INPUT PINS.

U8 65LVDS100

DC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J10 JUMPER_DIFF

THIS BUFFER CONVERTS 2.5V CML SIGNALS TO LVDS LEVELS THAT ARE COMPATABLE WITH ULTRASCALE "HP" BANK INPUTS.

THIS JUMPER ALLOWS DIRECT CONNECTION OF "CDR_DATA" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

U12 NB7V52M

U14 ADN2814

THE CLOCK POLARITY IS INVERTED.

U11 SY89832U

THIS DIVIDER NETWORK PROVIDES A DIFFERENTIAL VOLTAGE OF 0.83 VOLTS. IT HOLDS THE RESET INPUT AT A "FALSE" VALUE.

U10 SY89872

AC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J9 JUMPER_DIFF

S1=0, S0=1 -> B=INPUT/4

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTC_CLK40" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS CLOCK, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

THE THRESHOLD ADJUST SET BY R27=33 IS NOT MUCH DIFFERENT THAN R27=10 OHMS. MAYBE CHECK WITH ERIC HAZEN TO VALIDATE THIS VALUE.

PLACE ONE OF EACH VALUE NEAR PINS 2, 12, 18, 24, AND 31.

THIS DESIGN ONLY USES 2,5 VOLTS FOR LEGACY TTC SUPPORT. IT DOES NOT NEED A DC-DC CONVERTER SUPPLY.

U19 LT1963A

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 2.08: LEGACY TTC			
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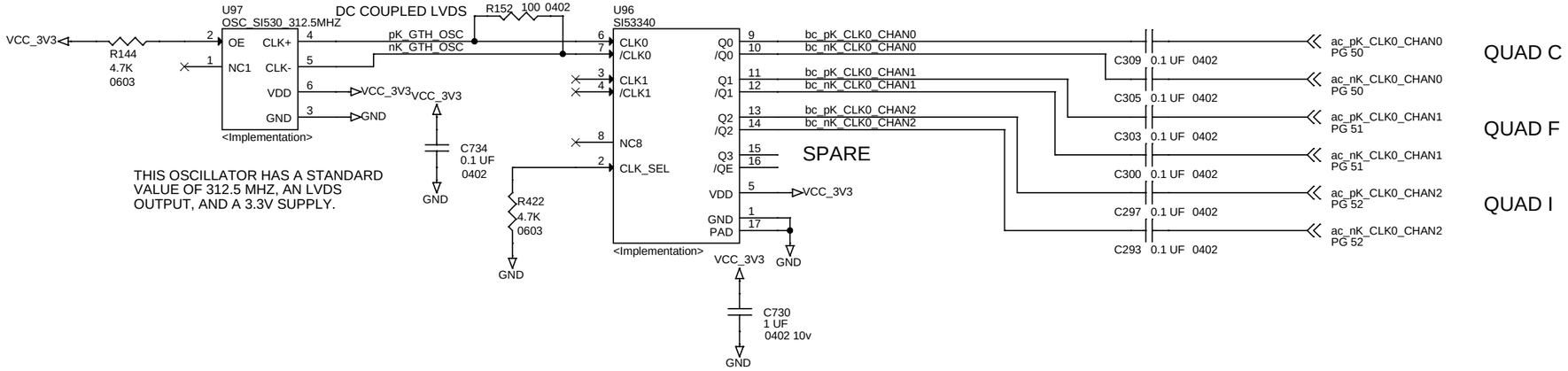
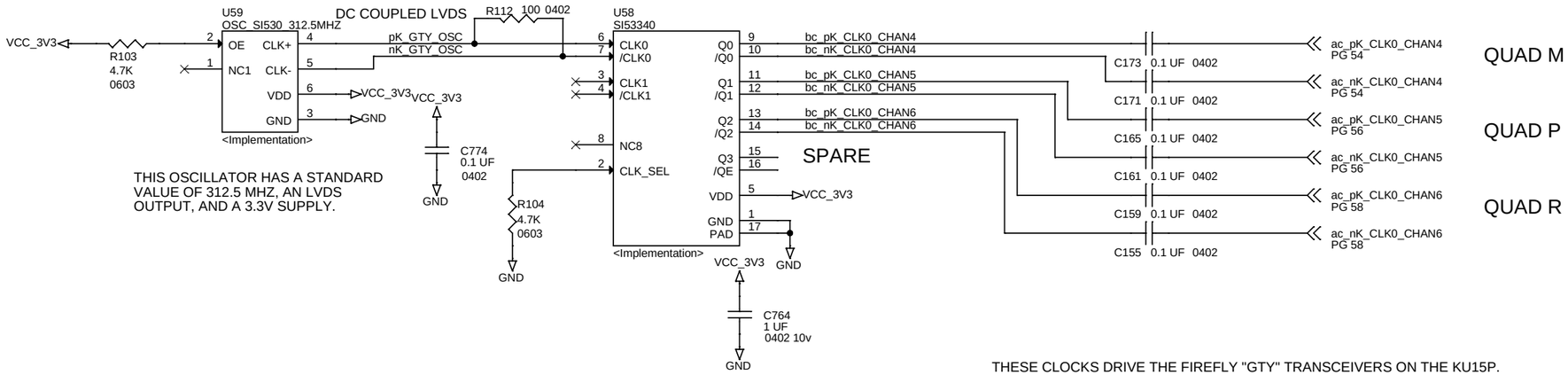
AC COUPLED LVDS

bc = BEFORE CAPACITOR

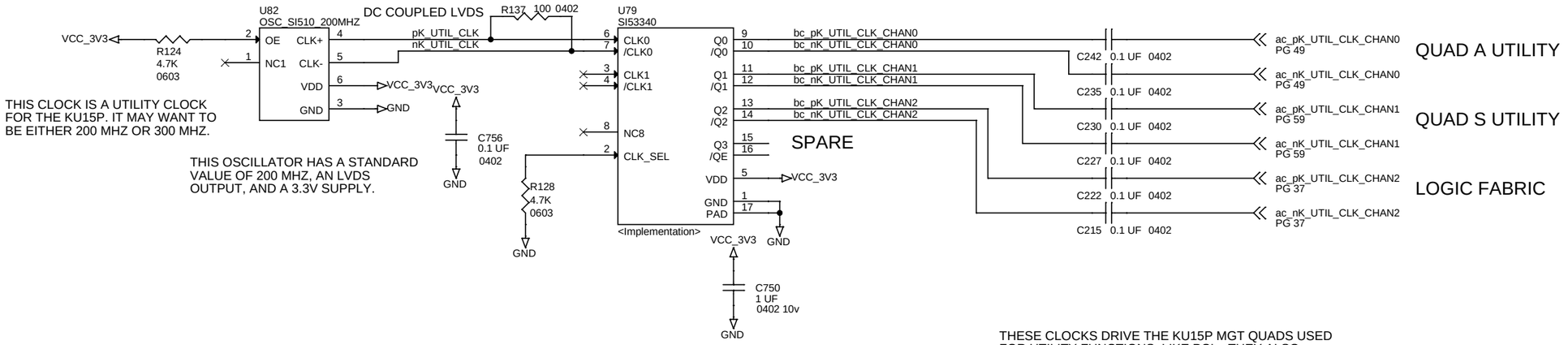
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.



THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.



THESE CLOCKS DRIVE THE KU15P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.09: KU15P OSCILLATOR CLOCKING

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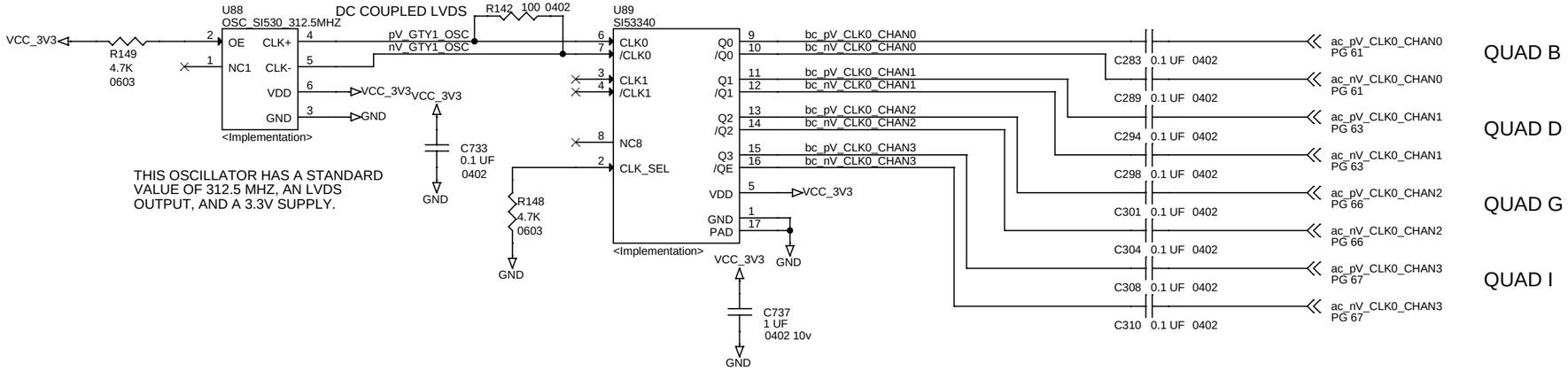
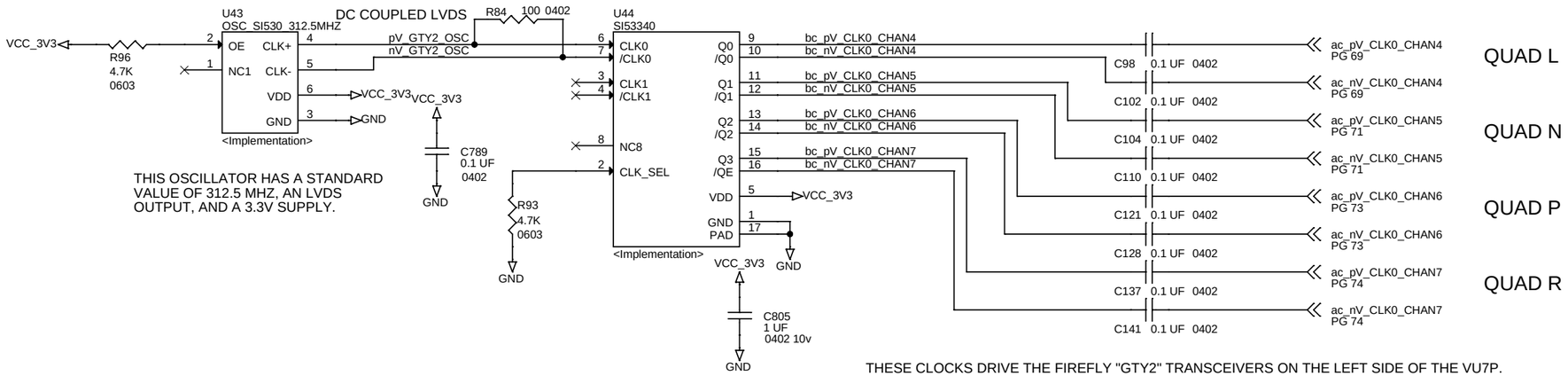
AC COUPLED LVDS

bc = BEFORE CAPACITOR

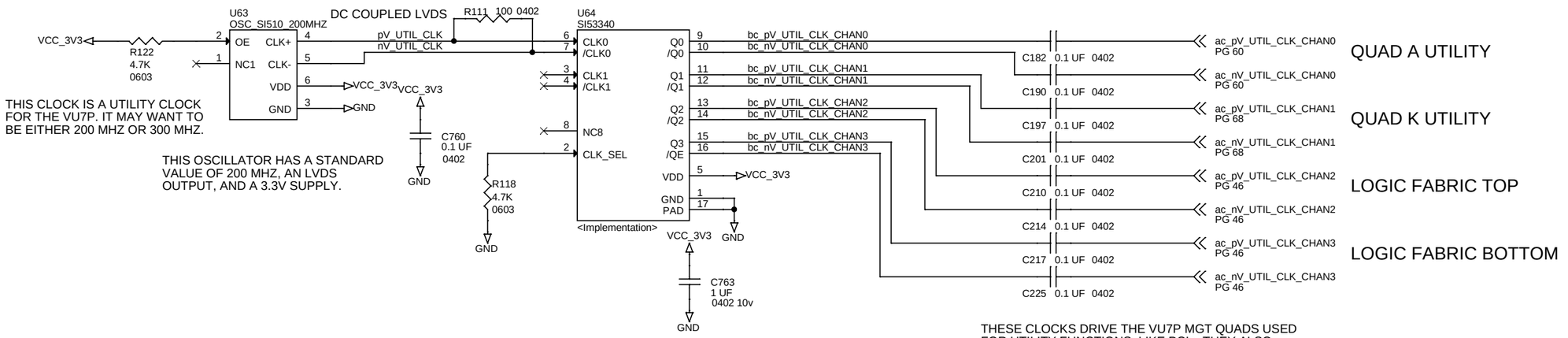
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.



THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.



THESE CLOCKS DRIVE THE VU7P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title

2.10: VU7P OSCILLATOR CLOCKING

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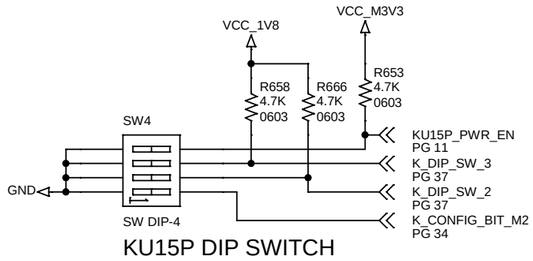
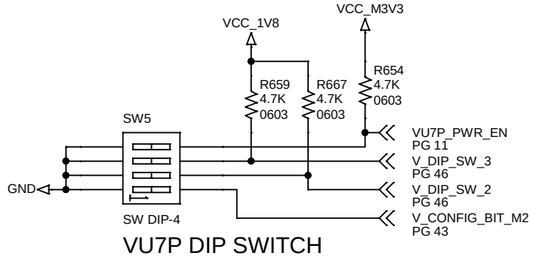


KU15P DIP SWITCH

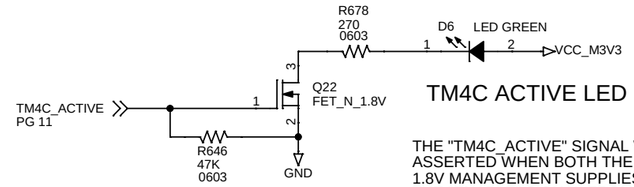


VU7P DIP SWITCH

SWITCH POSITION 4 IS USED TO TELL THE TM4C WHETHER OR NOT THE ASSOCIATED FPGA SHOULD BE POWERED. A HI LEVEL (SWITCH OPEN) MEANS "TURN ON FPGA POWER".

SWITCH POSITION 1 IS USED TO TELL THE FPGA WHETHER THE BOOT MODE IS "MASTER SPI (WITH JTAG OPTION)", OR "JTAG ONLY (MASTER SPI DISABLED)". A HI LEVEL (SWITCH OPEN) MEANS "JTAG ONLY (MASTER SPI DISABLED)"

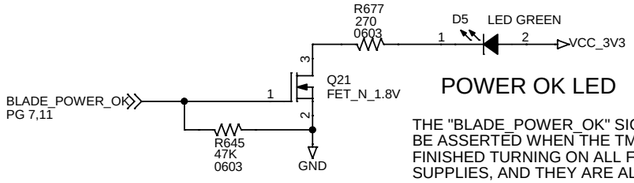
THE FUNCTION OF SWITCH POSITIONS 2 AND 3 ARE UNDEFINED AT THIS TIME.



TM4C ACTIVE LED

THE "TM4C_ACTIVE" SIGNAL WILL BE ASSERTED WHEN BOTH THE 3.3V AND 1.8V MANAGEMENT SUPPLIES ARE GOOD, THE "ENABLE" SIGNAL FROM THE SERVICE BLADE IS HIGH, AND THE "RESET" SWITCH IS NOT ACTIVATED.

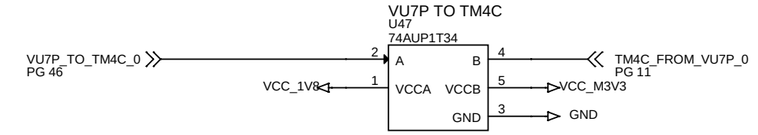
FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

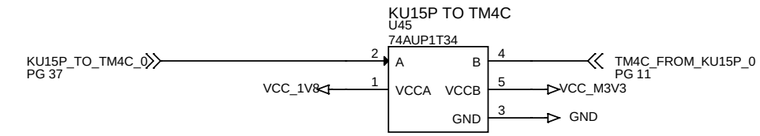


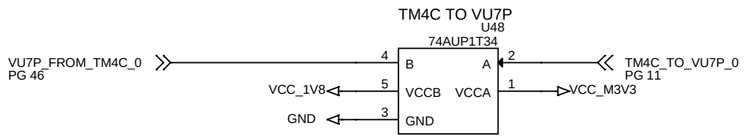
POWER OK LED

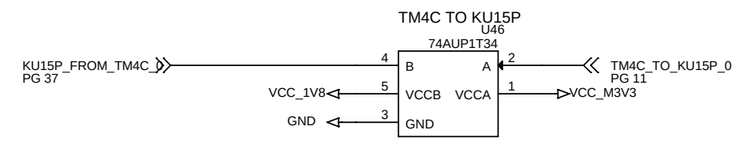
THE "BLADE_POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE TM4C HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

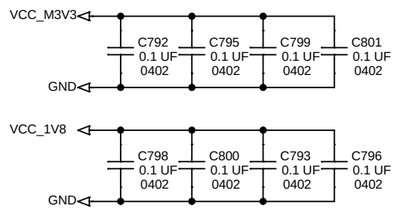






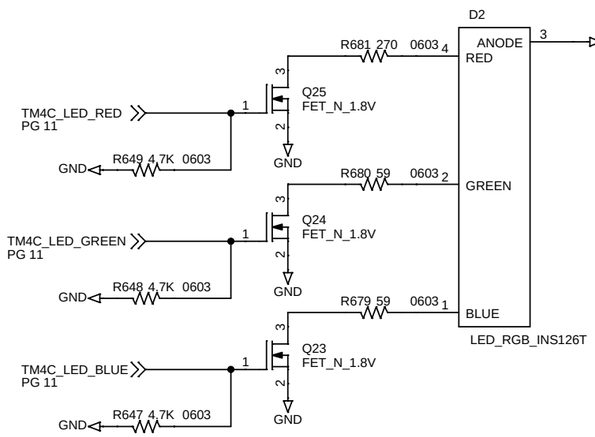


UTILITY CONNECTIONS BETWEEN THE TM4C CONTROLLER AND THE FPGAS. THE LEVEL TRANSLATORS ARE UNI-DIRECTIONAL.

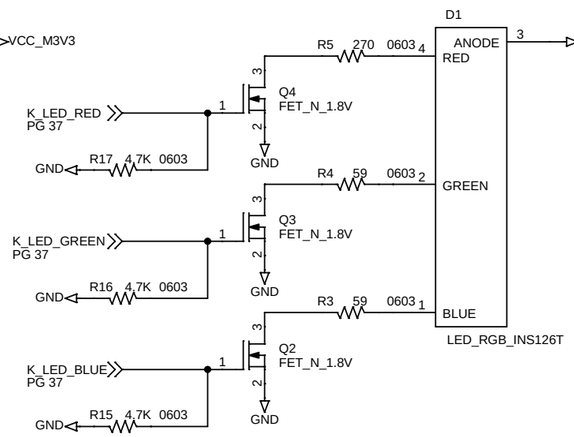


FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROPS ARE:
RED 2.0V. USE 270 OHM RESISTOR
BLUE 3.0V. USE 59 OHM RESISTOR
GREEN 3.0V. USE 59 OHM RESISTOR

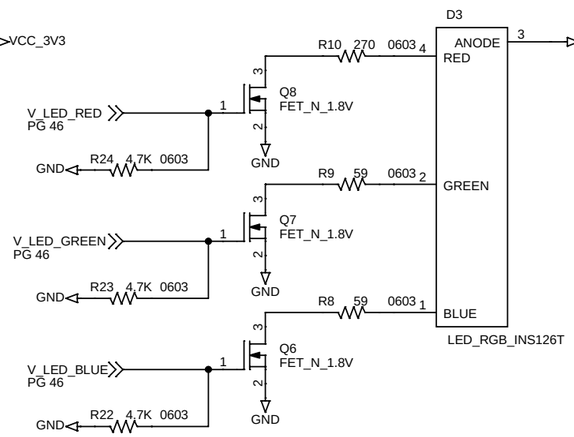
TM4C CONTROLLER LED



KU15P LED



VU7P LED



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.11: LEDS, SWITCHES, LEVEL SHIFTERS		
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U69
K_VCCINT_PG_A_1 PG 20
K_VCCINT_PG_A_2 PG 20
K_VCCINT_PG_A
VCC_M3V3
GND
74LVC1G08

U70
K_VCCINT_PG_B_1 PG 20
K_VCCINT_PG_B_2 PG 20
K_VCCINT_PG_B
VCC_M3V3
GND
74LVC1G08

U75
V_VCCINT_PG_A_1 PG 22
V_VCCINT_PG_A_2 PG 22
V_VCCINT_PG_A
VCC_M3V3
GND
74LVC1G08

U76
V_VCCINT_PG_B_1 PG 22
V_VCCINT_PG_B_2 PG 22
V_VCCINT_PG_B
VCC_M3V3
GND
74LVC1G08

USE 2-INPUT "AND" GATES TO COMBINE "PG" PINS FROM THE SAME MODULE AND SAVE CONTROLLER PINS

U52-6
TM4C1290NCPDT

K_VCCINT_PG_A	61	PK5	PF2	44	CTRL_K_VCCINT_PWR_EN
K_VCCINT_PG_B	60	PK6			
V_VCCINT_PG_A	32	PH3	PA4	37	CTRL_V_VCCINT_PWR_EN
V_VCCINT_PG_B	31	PH2	PP4	105	TP3 T POINT F
			PP3	104	TP2 T POINT F
VCC_3V3_PG PG 19	30	PH1	PF1	43	CTRL_VCC_3V3_PWR_EN
VCC_1V8_PG PG 19	29	PH0	PA5	38	CTRL_VCC_1V8_PWR_EN
			PN5	112	CTRL_V_MGTY1_VCCAUX_EN
			PN4	111	CTRL_V_MGTY2_VCCAUX_EN
			PL2	83	CTRL_K_MGTY_VCCAUX_EN
			PL3	84	CTRL_K_MGTH_VCCAUX_EN
K_MGTY_AVCC_OK PG 21	76	PM2	PL4	85	CTRL_K_MGTY_AVCC_PWR_EN
K_MGTH_AVCC_OK PG 21	75	PM3	PL5	86	CTRL_K_MGTH_AVCC_PWR_EN
K_MGTY_AVTT_OK PG 21	77	PM1	PQ4	102	CTRL_K_MGTY_AVTT_PWR_EN
K_MGTH_AVTT_OK PG 21	74	PM4	PP2	103	CTRL_K_MGTH_AVTT_PWR_EN
V_MGTY2_AVTT_OK PG 23	25	PC4	PN0	107	CTRL_V_MGTY2_AVTT_PWR_EN
V_MGTY1_AVTT_OK PG 23	22	PC7	PN1	108	CTRL_V_MGTY1_AVTT_PWR_EN
V_MGTY2_AVCC_OK PG 23	24	PC5	PN2	109	CTRL_V_MGTY2_AVCC_PWR_EN
V_MGTY1_AVCC_OK PG 23	23	PC6	PN3	110	CTRL_V_MGTY1_AVCC_PWR_EN

U71
CTRL_K_VCCINT_PWR_EN
R454 4.7K 0603
GND
K_VCCINT_PWR_EN PG 20
VCC_M3V3
74LVC1G08

U74
CTRL_V_VCCINT_PWR_EN
R457 4.7K 0603
V_VCCINT_PWR_EN PG 22

U72
CTRL_VCC_3V3_PWR_EN
R455 4.7K 0603
VCC_3V3_PWR_EN PG 19

U73
CTRL_VCC_1V8_PWR_EN
R456 4.7K 0603
VCC_1V8_PWR_EN PG 19

/V_MGTY1_VCCAUX_EN PG 42
CTRL_V_MGTY1_VCCAUX_EN
R498 4.7K 0603
Q15 FET_N_1.8V

/V_MGTY2_VCCAUX_EN PG 42
CTRL_V_MGTY2_VCCAUX_EN
R405 4.7K 0603
Q13 FET_N_1.8V

/K_MGTY_VCCAUX_EN PG 33
CTRL_K_MGTY_VCCAUX_EN
R501 4.7K 0603
Q16 FET_N_1.8V

/K_MGTH_VCCAUX_EN PG 33
CTRL_K_MGTH_VCCAUX_EN
R460 4.7K 0603
Q14 FET_N_1.8V

THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN VCC_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

/K_MGTY_AVCC_PWR_EN PG 21
CTRL_K_MGTY_AVCC_PWR_EN
R591 4.7K 0603
Q17 FET_N_1.8V

/K_MGTH_AVCC_PWR_EN PG 21
CTRL_K_MGTH_AVCC_PWR_EN
R313 4.7K 0603
Q9 FET_N_1.8V

/K_MGTY_AVTT_PWR_EN PG 21
CTRL_K_MGTY_AVTT_PWR_EN
R594 4.7K 0603
Q18 FET_N_1.8V

/K_MGTH_AVTT_PWR_EN PG 21
CTRL_K_MGTH_AVTT_PWR_EN
R316 4.7K 0603
Q10 FET_N_1.8V

/V_MGTY2_AVTT_PWR_EN PG 23
CTRL_V_MGTY2_AVTT_PWR_EN
R322 4.7K 0603
Q12 FET_N_1.8V

/V_MGTY1_AVTT_PWR_EN PG 23
CTRL_V_MGTY1_AVTT_PWR_EN
R600 4.7K 0603
Q20 FET_N_1.8V

/V_MGTY2_AVCC_PWR_EN PG 23
CTRL_V_MGTY2_AVCC_PWR_EN
R319 4.7K 0603
Q11 FET_N_1.8V

/V_MGTY1_AVCC_PWR_EN PG 23
CTRL_V_MGTY1_AVCC_PWR_EN
R597 4.7K 0603
Q19 FET_N_1.8V

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. A VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

THE TPS82130 HAS BEEN REPLACED BY AN IND045 ON SEVERAL BOARDS, DUE TO ASSEMBLY ISSUES. FUTURE DESIGNS WILL USE THE IND045.

SPREAD THESE CAPACITORS AROUND THE BOARD

VCC_M3V3
C960 22 UF 6.3V 0603
C858 22 UF 6.3V 0603
C479 22 UF 6.3V 0603
C548 22 UF 6.3V 0603
GND

VCC_M1V8
C829 22 UF 6.3V 0603
C968 22 UF 6.3V 0603
GND

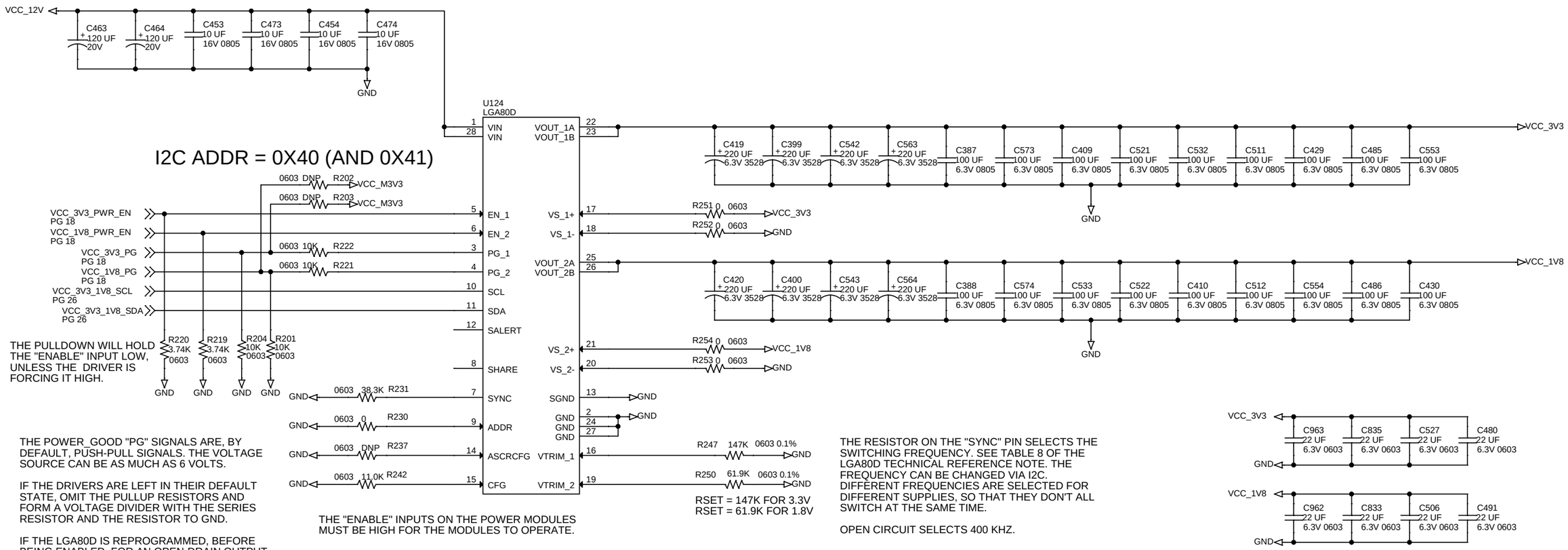
U31
TPS82130
VCC_12V
C15 10 UF 16V 0805
C834 3.3 NF 50V 0603
VIN
EN
SS/TR
VOUT
VOUT
FB
PG
GND
PAD
R28 110K 0603 0.1%
R29 34.8K 0603 0.1%
C52 22 UF 6.3V 0603
VCC_M3V3

THE VOLTAGE IS 3.33 VOLTS WITH RESISTORS OF 110K AND 34.8K.

VCC_M3V3 AND VCC_M1V8 ARE THE "MANAGEMENT" POWER. THEY PROVIDE POWER TO THE POWER SEQUENCING CIRCUIT. THEY ARE ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

U90
ADP1713_1V8
EN
IN
OUT
BYP
GND
C731 4.7 UF 0402
C732 0.1 UF 0402
C272 4.7 UF 0402
C260 0.1 UF 0402
C271 0.01 UF 0402
VCC_M1V8

Title	ATCA FPGA BOARD, KU15P AND VU7P, MK1
	3.01: POWER CONTROL
Size	Document Number 6089-103 Rev A
Date:	Friday, August 30, 2019 Sheet 18 of 74



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.02: POWER GLOBAL 3.3V AND 1.8V

Size	Document Number	Rev
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KU15P VCCINT MUST BE 0.85V.

U122
LGA80D

A

VCC_12V

C459 120 UF 20V, C460 120 UF 20V, C449 10 UF 16V 0805, C469 10 UF 16V 0805, C450 10 UF 16V 0805, C470 10 UF 16V 0805

GND

I2C ADDR = 0X44

K_VCCINT_PG_A_1 PG 18
K_VCCINT_PG_A_2 PG 18
K_VCCINT_A_SCL PG 26
K_VCCINT_A_SDA PG 26

0603 DNP R194 VCC_M3V3
0603 DNP R195 VCC_M3V3
0603 10K R216
0603 10K R215

R196 10K 0603, R193 10K 0603

K_VCCINT_PWR_EN PG 18

R213 3.74K 0603

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

0603 12.1K R227
0603 DNP R235
0603 90.9K R240

1, 28	VIN	VOUT_1A, VOUT_1B	22, 23
5	EN_1	VS_1+	17
6	EN_2	VS_1-	18
3	PG_1		
4	PG_2	VOUT_2A, VOUT_2B	25, 26
10	SCL		
11	SDA		
12	SALERT		
		VS_2+	21
8	SHARE	VS_2-	20
7	SYNC	SGND	13
		GND	2, 24, 27
9	ADDR		
14	ASCRCFG	VTRIM_1	16
15	CFG	VTRIM_2	19

R191 0 0603
R192 0 0603

R245 16.2K 0603 0.1%

RSET = 16.2K FOR 0.85V

C415 330 UF 2.5V 3528, C393 330 UF 2.5V 3528, C538 330 UF 2.5V 3528, C559 330 UF 2.5V 3528, C425 100 UF 4V 0805, C405 100 UF 4V 0805, C528 100 UF 4V 0805, C550 100 UF 4V 0805, C383 100 UF 4V 0805, C569 100 UF 4V 0805, C481 100 UF 4V 0805, C507 100 UF 4V 0805, C517 100 UF 4V 0805

C416 330 UF 2.5V 3528, C394 330 UF 2.5V 3528, C539 330 UF 2.5V 3528, C560 330 UF 2.5V 3528, C426 100 UF 4V 0805, C406 100 UF 4V 0805, C529 100 UF 4V 0805, C551 100 UF 4V 0805, C384 100 UF 4V 0805, C570 100 UF 4V 0805, C482 100 UF 4V 0805, C508 100 UF 4V 0805, C518 100 UF 4V 0805

K_VCCINT

U123
LGA80D

B

C461 120 UF 20V, C462 120 UF 20V, C451 10 UF 16V 0805, C471 10 UF 16V 0805, C452 10 UF 16V 0805, C472 10 UF 16V 0805

GND

I2C ADDR = 0X43

K_VCCINT_PG_B_1 PG 18
K_VCCINT_PG_B_2 PG 18
K_VCCINT_B_SCL PG 26
K_VCCINT_B_SDA PG 26

0603 DNP R198 VCC_M3V3
0603 DNP R199 VCC_M3V3
0603 10K R218
0603 10K R217

R200 10K 0603, R197 10K 0603

0603 21.5K R229
0603 11.0K R228
0603 DNP R236
0603 100K R241

1, 28	VIN	VOUT_1A, VOUT_1B	22, 23
5	EN_1	VS_1+	17
6	EN_2	VS_1-	18
3	PG_1		
4	PG_2	VOUT_2A, VOUT_2B	25, 26
10	SCL		
11	SDA		
12	SALERT		
		VS_2+	21
8	SHARE	VS_2-	20
7	SYNC	SGND	13
		GND	2, 24, 27
9	ADDR		
14	ASCRCFG	VTRIM_1	16
15	CFG	VTRIM_2	19

R246 16.2K 0603 0.1%

RSET = 16.2K FOR 0.85V

C417 330 UF 2.5V 3528, C396 330 UF 2.5V 3528, C540 330 UF 2.5V 3528, C561 330 UF 2.5V 3528, C427 100 UF 4V 0805, C407 100 UF 4V 0805, C530 100 UF 4V 0805, C552 100 UF 4V 0805, C385 100 UF 4V 0805, C571 100 UF 4V 0805, C519 100 UF 4V 0805, C509 100 UF 4V 0805, C483 100 UF 4V 0805

C418 330 UF 2.5V 3528, C397 330 UF 2.5V 3528, C541 330 UF 2.5V 3528, C562 330 UF 2.5V 3528, C428 100 UF 4V 0805, C408 100 UF 4V 0805, C531 100 UF 4V 0805, C549 100 UF 4V 0805, C386 100 UF 4V 0805, C572 100 UF 4V 0805, C520 100 UF 4V 0805, C510 100 UF 4V 0805, C484 100 UF 4V 0805

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=90.9K SELECTS 4-PHASE MASTER @ 35A EACH
R=100K SELECTS 4-PHASE SLAVE @ 35A EACH

THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

21.5K SELECTS 432 KHZ.

THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. EVEN THOUGH EACH LGA80D IS ON A DIFFERENT I2C BUS, UNIQUE ADDRESS ARE ASSIGNE TO EACH. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

3.3/1.8V: R=0 -> ADDR = 0X40 (AND 0X41)
K_VCCINT MASTER: R=12.1K -> ADDR = 0X44
K_VCCINT SLAVE: R=11K -> ADDR = 0X43
V_VCCINT MASTER: R=14.7K -> ADDR = 0X46
V_VCCINT SLAVE: R=13.3K -> ADDR = 0X45

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.03: POWER SOURCE KU15P INTERNAL

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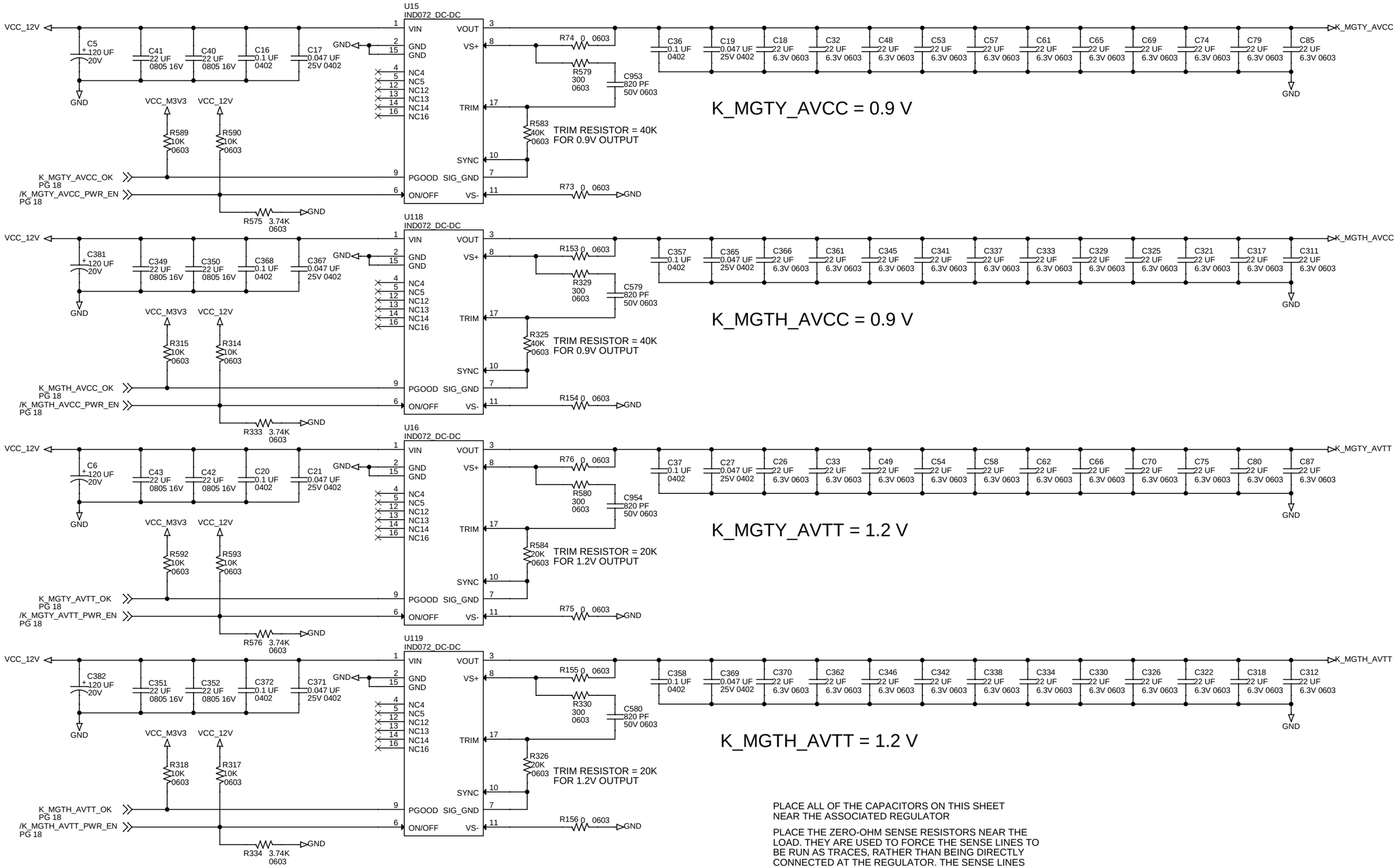
Date: Thursday, March 07, 2019 | Sheet 20 of 74



THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.04: POWER SOURCE KU15P MGT XCVR

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VU7P VCCINT MUST BE 0.85V.

VCC_12V

C465 120 UF 20V, C466 120 UF 20V, C455 10 UF 16V 0805, C475 10 UF 16V 0805, C456 10 UF 16V 0805, C476 10 UF 16V 0805

GND

U125
LGA80D

A

VIN (1, 28)
VOUT_1A (22)
VOUT_1B (23)
V_VCCINT

C421 330 UF 2.5V 3528, C401 330 UF 2.5V 3528, C544 330 UF 2.5V 3528, C565 330 UF 2.5V 3528, C431 100 UF 6.3V 0805, C411 100 UF 6.3V 0805, C534 100 UF 6.3V 0805, C555 100 UF 6.3V 0805, C389 100 UF 6.3V 0805, C575 100 UF 6.3V 0805, C523 100 UF 6.3V 0805, C513 100 UF 6.3V 0805, C487 100 UF 6.3V 0805

GND

I2C ADDR = 0X46

EN_1 (5) — 0603 DNP R206 — VCC_M3V3
EN_2 (6) — 0603 DNP R207 — VCC_M3V3
PG_1 (3) — V_VCCINT_PG_A_1 PG 18 — 0603 10K R224
PG_2 (4) — V_VCCINT_PG_A_2 PG 18 — 0603 10K R223
SCL (10) — V_VCCINT_A_SCL PG 26
SDA (11) — V_VCCINT_A_SDA PG 26
SALERT (12) — R208 10K 0603, R205 10K 0603 — GND GND

VS_1+ (17) — R256 0 0603 — V_VCCINT
VS_1- (18) — R255 0 0603 — GND

VOUT_2A (25), VOUT_2B (26)

C402 330 UF 2.5V 3528, C422 330 UF 2.5V 3528, C566 330 UF 2.5V 3528, C545 330 UF 2.5V 3528, C432 100 UF 6.3V 0805, C412 100 UF 6.3V 0805, C535 100 UF 6.3V 0805, C556 100 UF 6.3V 0805, C390 100 UF 6.3V 0805, C576 100 UF 6.3V 0805, C524 100 UF 6.3V 0805, C514 100 UF 6.3V 0805, C488 100 UF 6.3V 0805

GND

VS_2+ (21)
SHARE (8)
VS_2- (20)
SYNC (7) — V_VCCINT_PWR_EN PG 18 — R214 3.74K 0603 — GND
SGND (13) — GND
GND (2, 24, 27) — GND
ADDR (9) — GND — 0603 14.7K R232
ASCRCFG (14) — GND — 0603 DNP R238
VTRIM_1 (16) — R248 16.2K 0603 0.1% — GND
CFG (15) — GND — 0603 90.9K R243
VTRIM_2 (19)

RSET = 16.2K FOR 0.85V

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

U126
LGA80D

B

VIN (1, 28)
VOUT_1A (22)
VOUT_1B (23)

C467 120 UF 20V, C468 120 UF 20V, C457 10 UF 16V 0805, C477 10 UF 16V 0805, C458 10 UF 16V 0805, C478 10 UF 16V 0805

GND

C423 330 UF 2.5V 3528, C403 330 UF 2.5V 3528, C546 330 UF 2.5V 3528, C567 330 UF 2.5V 3528, C433 100 UF 6.3V 0805, C413 100 UF 6.3V 0805, C536 100 UF 6.3V 0805, C557 100 UF 6.3V 0805, C391 100 UF 6.3V 0805, C577 100 UF 6.3V 0805, C525 100 UF 6.3V 0805, C515 100 UF 6.3V 0805, C489 100 UF 6.3V 0805

GND

I2C ADDR = 0X45

EN_1 (5) — 0603 DNP R210 — VCC_M3V3
EN_2 (6) — 0603 DNP R211 — VCC_M3V3
PG_1 (3) — V_VCCINT_PG_B_1 PG 18 — 0603 10K R226
PG_2 (4) — V_VCCINT_PG_B_2 PG 18 — 0603 10K R225
SCL (10) — V_VCCINT_B_SCL PG 26
SDA (11) — V_VCCINT_B_SDA PG 26
SALERT (12) — R212 10K 0603, R209 10K 0603 — GND GND

VS_1+ (17)
VS_1- (18)

VOUT_2A (25), VOUT_2B (26)

C424 330 UF 2.5V 3528, C404 330 UF 2.5V 3528, C568 330 UF 2.5V 3528, C547 330 UF 2.5V 3528, C434 100 UF 6.3V 0805, C414 100 UF 6.3V 0805, C537 100 UF 6.3V 0805, C558 100 UF 6.3V 0805, C392 100 UF 6.3V 0805, C578 100 UF 6.3V 0805, C490 100 UF 6.3V 0805, C516 100 UF 6.3V 0805, C526 100 UF 6.3V 0805

GND

VS_2+ (21)
SHARE (8)
VS_2- (20)
SYNC (7) — GND — 0603 23.7K R234
SGND (13) — GND
GND (2, 24, 27) — GND
ADDR (9) — GND — 0603 13.3K R233
ASCRCFG (14) — GND — 0603 DNP R239
VTRIM_1 (16) — R249 16.2K 0603 0.1% — GND
CFG (15) — GND — 0603 100K R244
VTRIM_2 (19)

RSET = 16.2K FOR 0.85V

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=90.9K SELECTS 4-PHASE MASTER @ 35A EACH
R=100K SELECTS 4-PHASE SLAVE @ 35A EACH

THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

23.7K SELECTS 457 KHZ.

THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. EVEN THOUGH EACH LGA80D IS ON A DIFFERENT I2C BUS, UNIQUE ADDRESS ARE ASSIGNE TO EACH. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

3.3/1.8V: R=0 -> ADDR = 0X40 (AND 0X41)
K_VCCINT MASTER: R=12.1K -> ADDR = 0X44
K_VCCINT SLAVE: R=11K -> ADDR = 0X43
V_VCCINT MASTER: R=14.7K -> ADDR = 0X46
V_VCCINT SLAVE: R=13.3K -> ADDR = 0X45

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.05: POWER SOURCE VU7P INTERNAL

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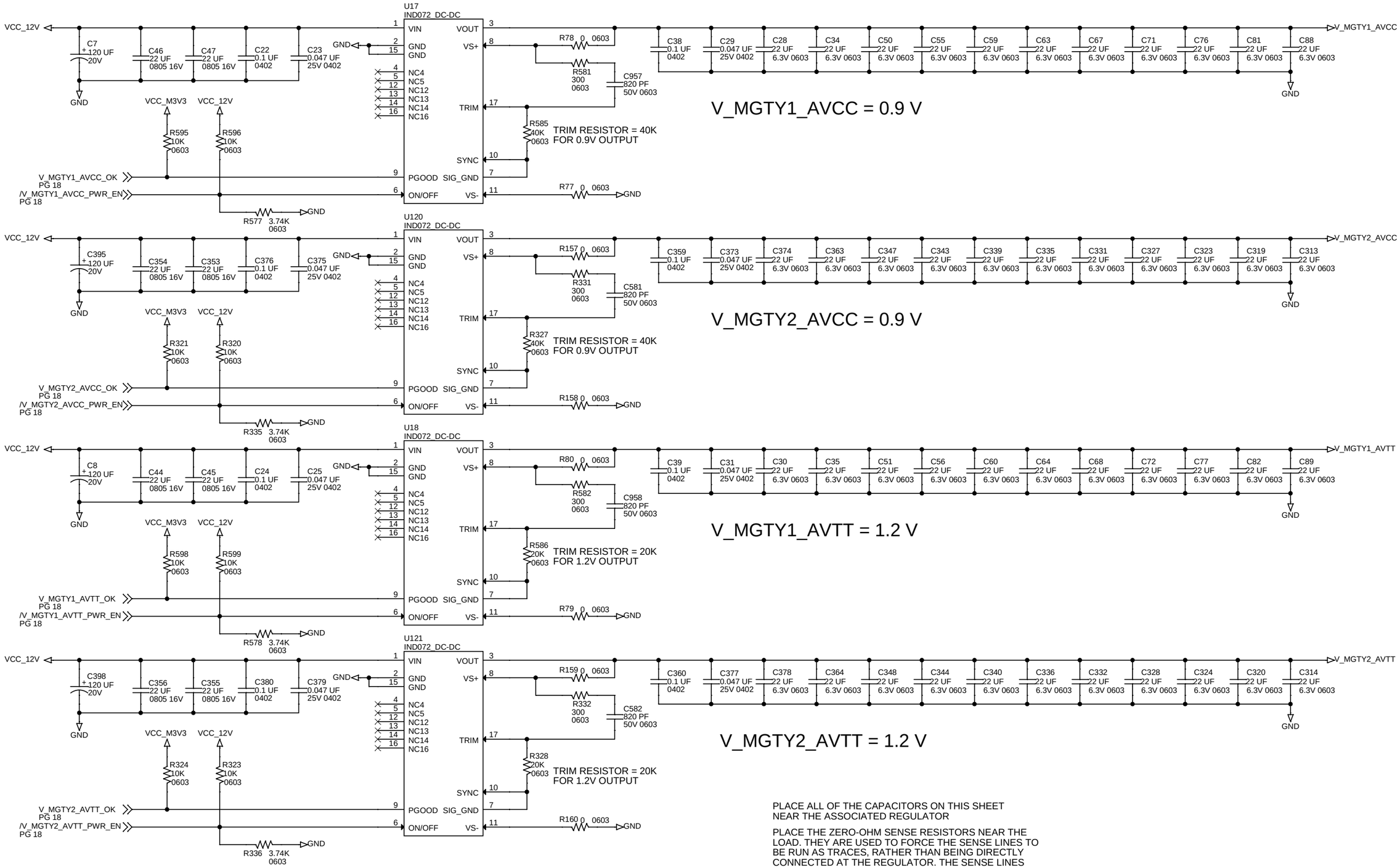

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 3.06: POWER SOURCE VU7P MGT XCVR		
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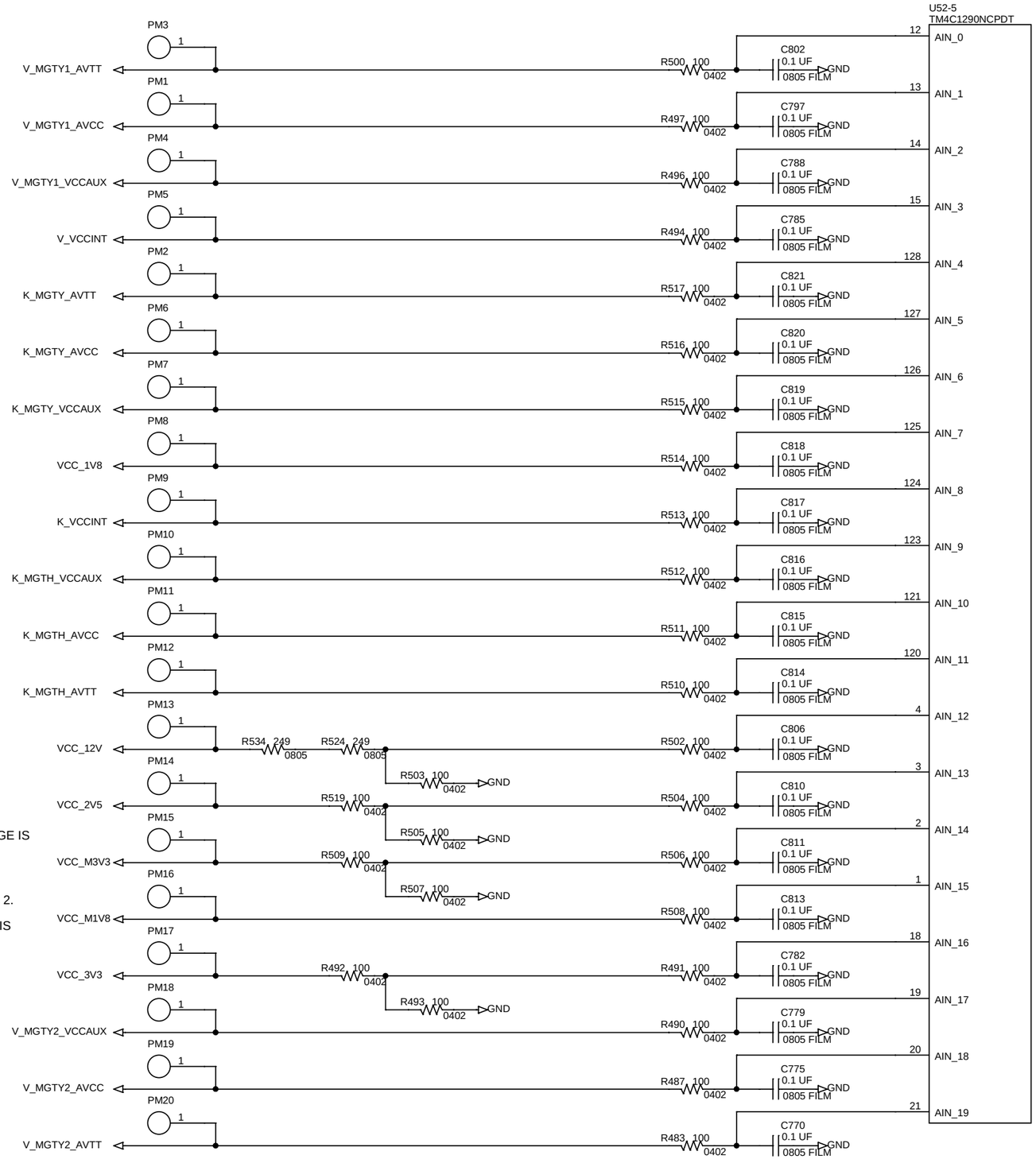

THE FULL SCALE ADC VOLTAGE IS 2.5 VOLTS, AS SET BY THE VOLTAGE REFERENCE.

THE 2.5 VOLT AND 3.3 VOLT SUPPLY LEVEL IS DIVIDED BY 2.

THE 12 VOLT SUPPLY LEVEL IS DIVIDED BY 6.

TEST POINTS TO MEASURE VOLTAGES

PM21 1 GND
PM22 1 GND
PM23 1 GND
PM24 1 GND
PM25 1 GND
PM26 1 GND

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.07: POWER MEASUREMENT

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IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH.
IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

VCC_M3V3
R674 2.2K 0603
R675 2.2K 0603

J2 JUMPER_4X2
BLADE_MASTER_I2C_SCL PG 7
BLADE_MASTER_I2C_SDA PG 7
TM4C I2C
GND

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.
TM4C SLAVE I2C ADDR = 0X40

U52-4 TM4C1290NCPDT

91	I2C_SCL0	I2C_SCL1	49
92	I2C_SDA0	I2C_SDA1	50
		PF3	45
		I2C_SCL2	51
		I2C_SDA2	52
		PQ5	57
		I2C_SCL3	53
		I2C_SDA3	54
		PQ6	58
		I2C_SCL4	55
		I2C_SDA4	56
		PK7	59
		I2C_SCL6	40
		I2C_SDA6	41
		PF0	42
106	PP5		

VCC_3V3: R689 2.2K 0603, R690 2.2K 0603, R692 2.2K 0603, R693 2.2K 0603, R695 2.2K 0603, R696 2.2K 0603, R683 2.2K 0603, R684 2.2K 0603, R686 2.2K 0603, R687 2.2K 0603

THE OUTPUTS THAT DRIVE THE "RESET" SIGNALS NEED TO BE OPEN-DRAIN.

MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.

J5 JUMPER_4X2
PWR I2C
PWR_I2C_SCL PG 26
PWR_I2C_SDA PG 26
/PWR_I2C_RESET PG 26
R691 10K 0603 VCC_3V3

J7 JUMPER_4X2
CLOCKS I2C
CLOCKS_I2C_SCL PG 27
CLOCKS_I2C_SDA PG 27
/CLOCKS_I2C_RESET PG 27
R694 10K 0603 VCC_3V3

J8 JUMPER_4X2
V OPTICS I2C
V_OPTICS_I2C_SCL PG 30
V_OPTICS_I2C_SDA PG 30
/V_OPTICS_I2C_RESET PG 30
R697 10K 0603 VCC_3V3

J3 JUMPER_4X2
K OPTICS I2C
K_OPTICS_I2C_SCL PG 29
K_OPTICS_I2C_SDA PG 29
/K_OPTICS_I2C_RESET PG 29
R685 10K 0603 VCC_3V3

J4 JUMPER_4X2
FPGA I2C
FPGA_I2C_SCL PG 28
FPGA_I2C_SDA PG 28
/FPGA_I2C_RESET PG 28
R688 10K 0603 VCC_1V8

HEADERS ARE PROVIDED TO SUPPORT DRIVING ANY I2C BUS WITH A STAND-ALONE USB-TO-I2C CONTROLLER.

NORMALLY, JUMPERS WILL CONNECT THE ON-BOARD "SCL", "SDA", AND "/RESET" SIGNALS STRAIGHT THROUGH THE HEADERS.

TO CONNECT THE STAND-ALONE CONTROLLER, PULL THE JUMPERS FROM THE HEADER AND CONNECT THE CONTROLLER'S SIGNALS TO PINS 2, 4, AND 6, AND CONNECT GND TO PIN 8.

CONFIGURE THE "SPI MISO" PIN ON THE AARDVARK CONTROLLER AS A "GPIO OUTPUT" TO CONTROL THE "RESET" SIGNAL.

THIS LAYOUT ASSUMES THAT THE STAND-ALONE CONTROLLER PROVIDES PULL-UP RESISTORS ON THE I2C SIGNALS.

THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.

U35 24LCS52
VCC_M3V3
R530 0603 10K
R521 0 0603
R531 0603 10K
R522 0 0603
R532 0603 10K
R523 0 0603
GND
A2 A1 A0 SDA SCL WP VCC GND
C832 0.1 UF 0402
R533 10K 0603
J16 JUMPER_3X1
ID_EEPROM_WP

24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

R/W I2C ADDR = 0X50
WP I2C ADDR = 0X30

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THIS JUMPER CONFIGURES THE HARDWARE WRITE-PROTECT PIN.

IF NO JUMPER IS IN PLACE, THE HARDWARE WRITE PROTECTION IS ALWAYS ENABLED.

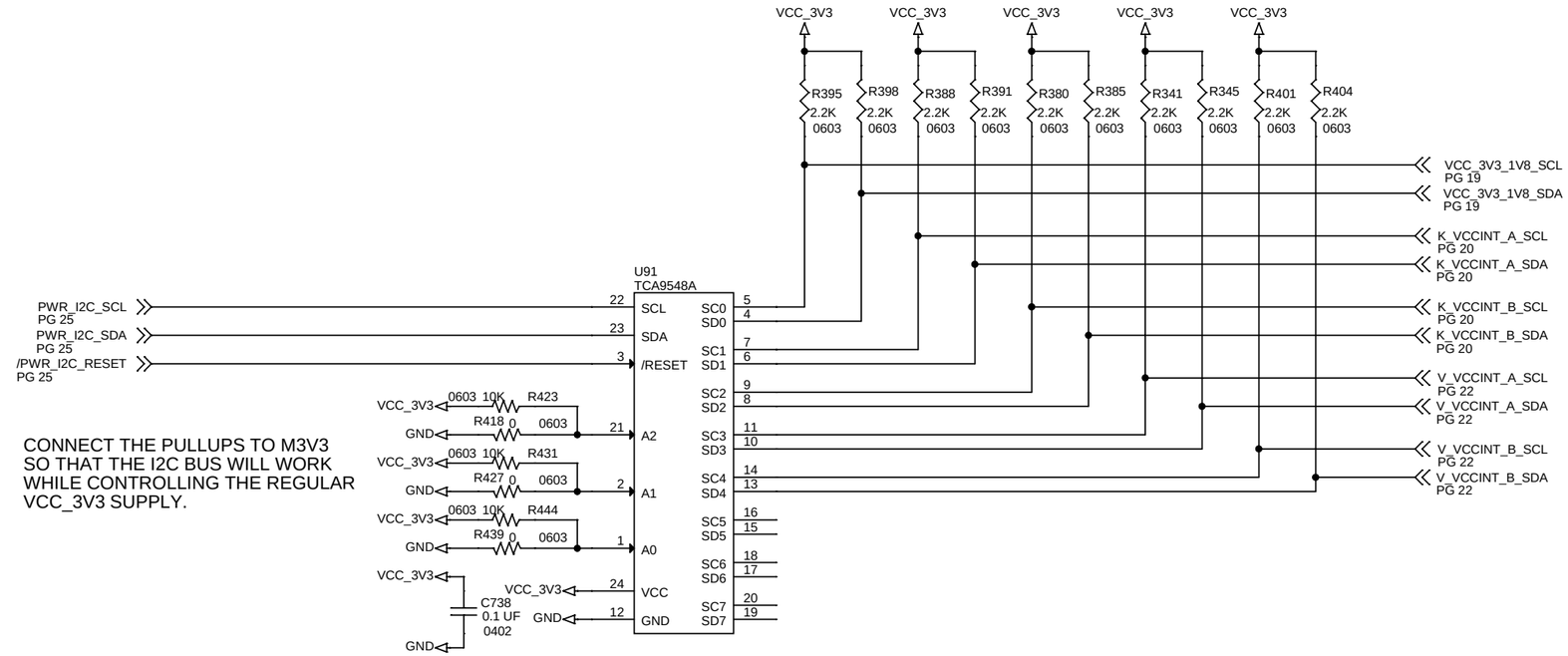
IF THE JUMPER CONNECTS PINS 1 AND 2, THE HARDWARE WRITE PROTECTION IS ALWAYS DISABLED.

IF THE JUMPER CONNECTS PINS 2 AND 3, THE HARDWARE PROTECTION IS CONTROLLED BY A GPIO PIN ON THE CONTROLLER.

REFER TO THE DATA SHEET FOR DETAILS ABOUT CONNECTING AN EXTERNAL HIGH VOLTAGE TO RESET THE SOFTWARE WRITE PROTECT FUSE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title: 4.01: I2C CONTROLLER
Size | Document Number: 6089-103 | Rev: A
Date: Tuesday, April 16, 2019 Sheet 25 of 74

CONNECT THE PULLUPS TO M3V3
SO THAT THE I2C BUS WILL WORK
WHILE CONTROLLING THE REGULAR
VCC_3V3 SUPPLY.



CONNECT THE PULLUPS TO M3V3
SO THAT THE I2C BUS WILL WORK
WHILE CONTROLLING THE REGULAR
VCC_3V3 SUPPLY.

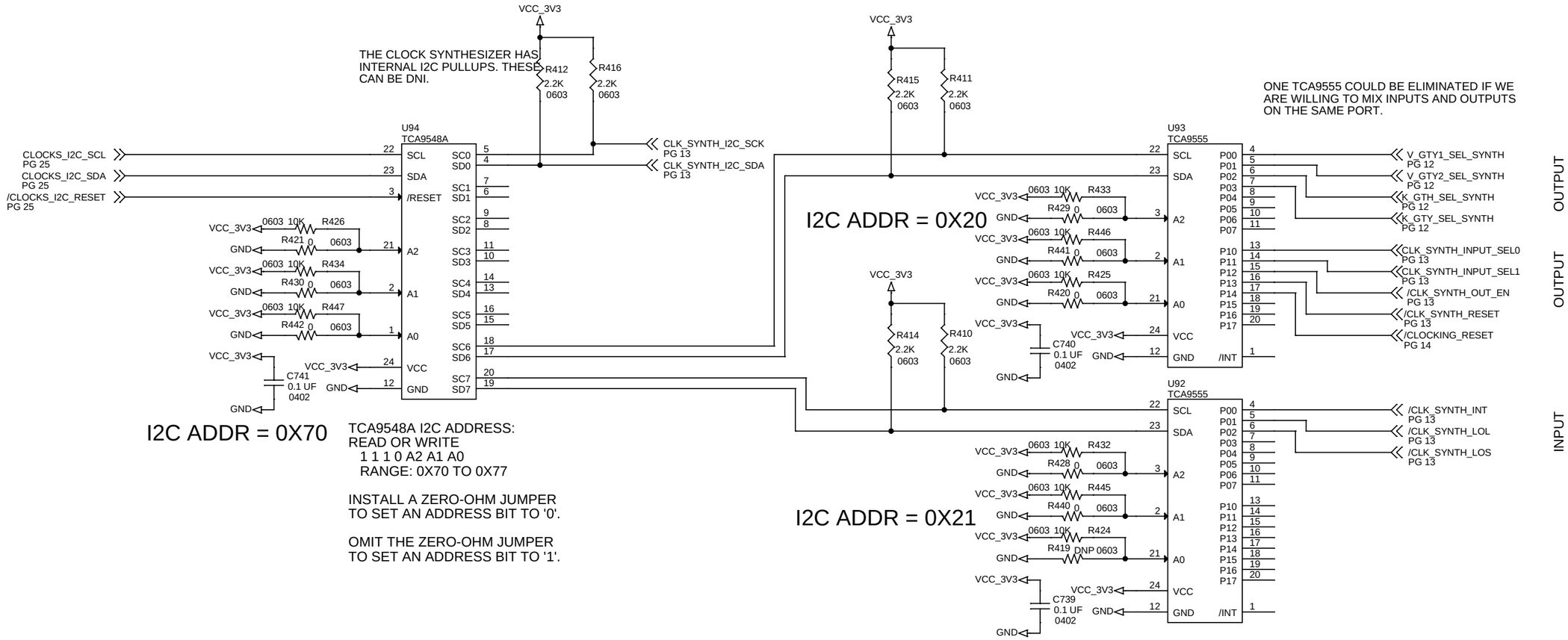
I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.02: I2C POWER CONTROL		
Size	Document Number: 6089-103	Rev: A
Date: Friday, August 30, 2019	Sheet 26 of 74	



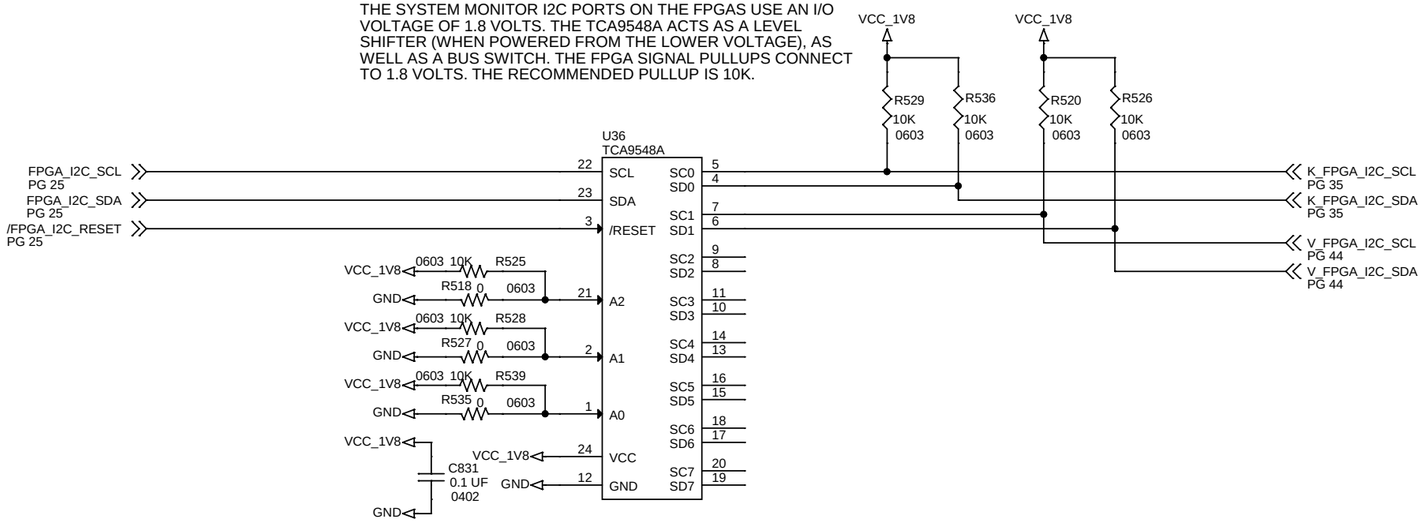
ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.03: I2C CLOCK SOURCE CONTROL

Size	Document Number	Rev
	6089-103	A

Date: Thursday, March 07, 2019 Sheet 27 of 74

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

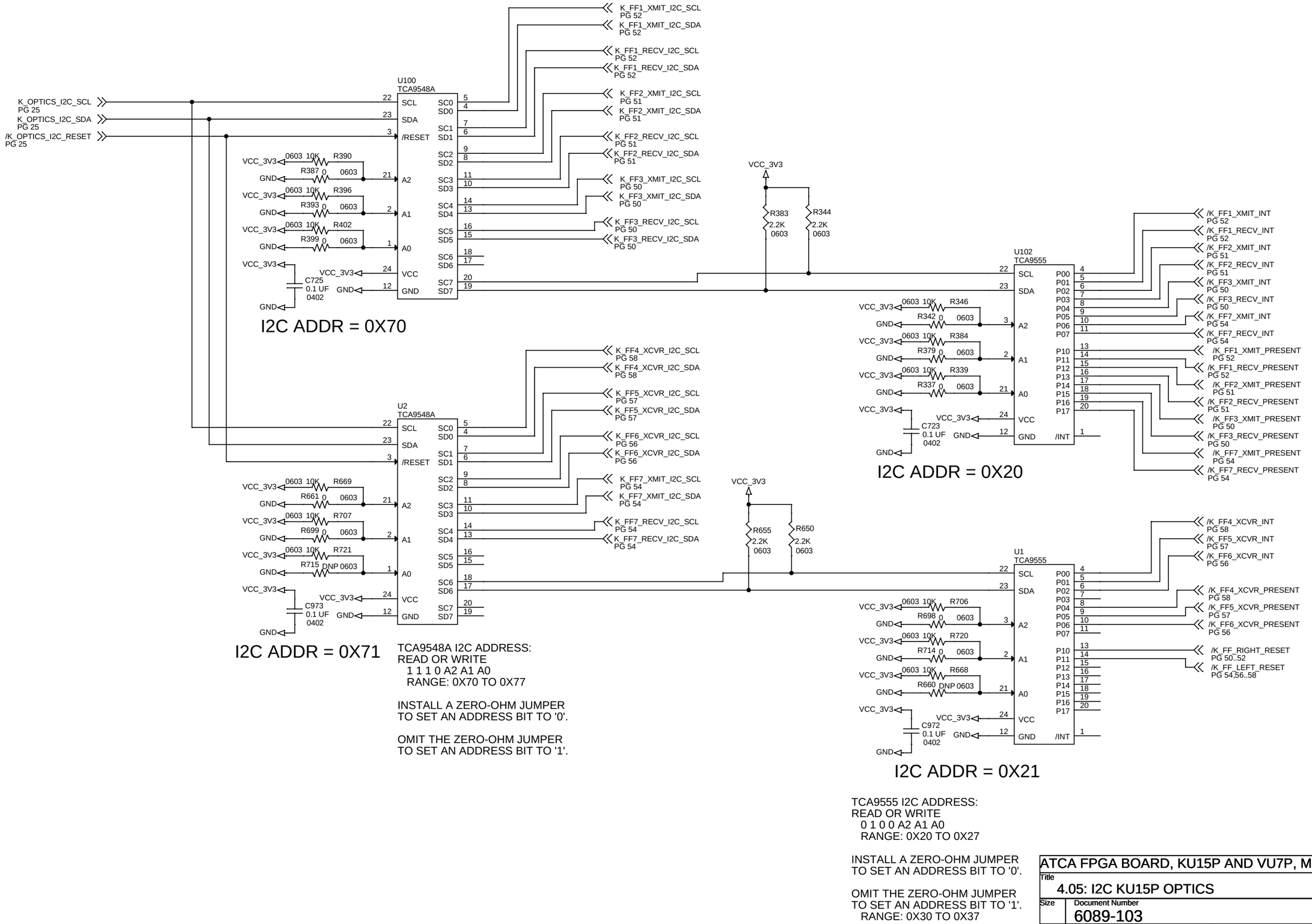
A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.04: I2C FPGA SYSMON

Size | Document Number: 6089-103 | Rev: A

Date: Thursday, March 07, 2019 Sheet 28 of 74



TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

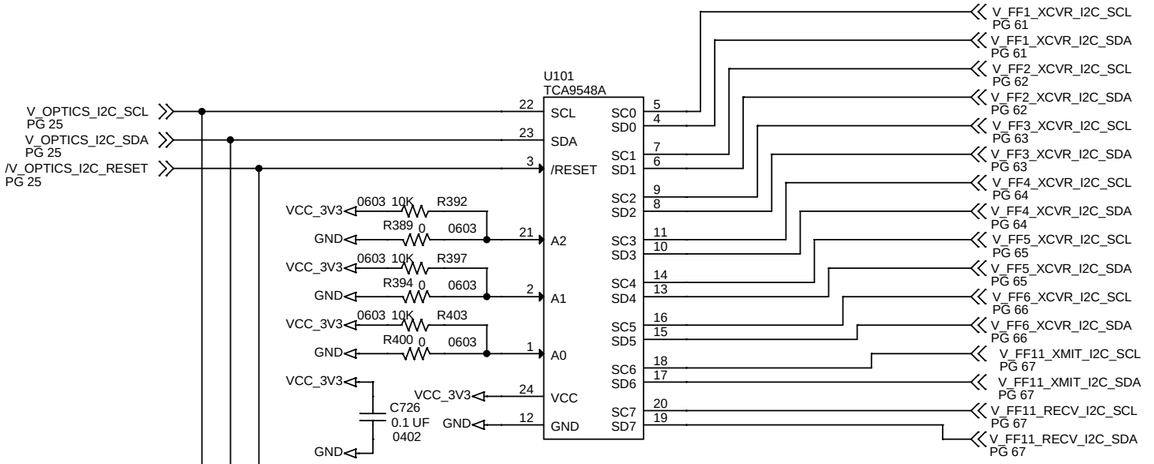
OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

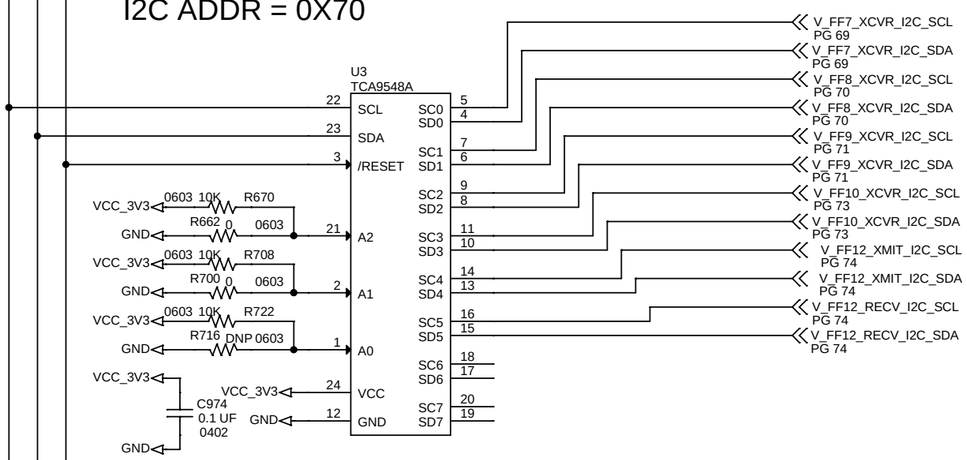
TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

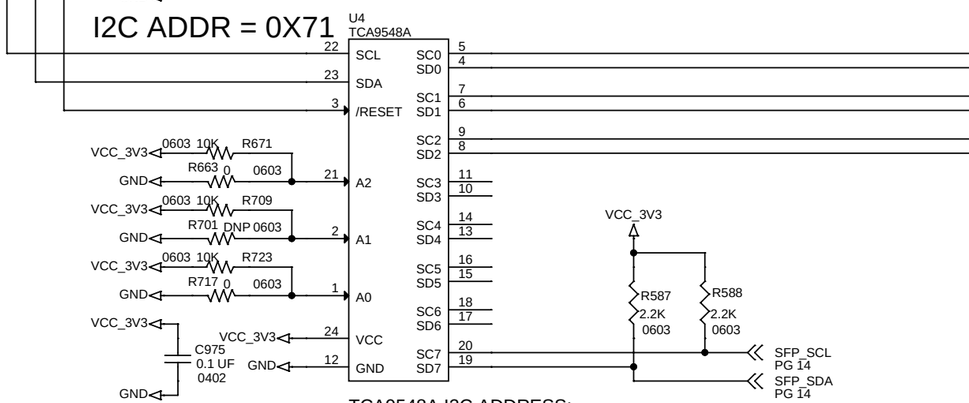
INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.05: I2C KU15P OPTICS		
Size	Document Number: 6089-103	Rev: A
Date: Thursday, March 07, 2019	Sheet 29 of 74	





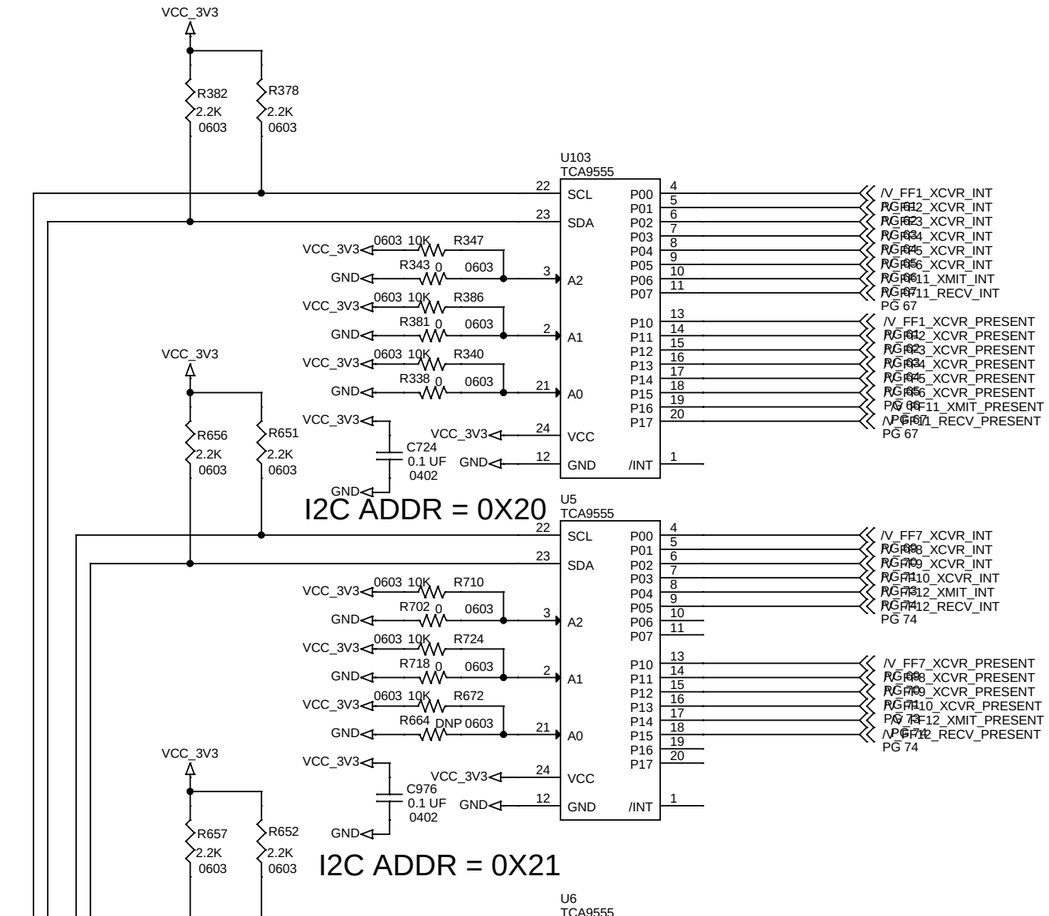


TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

THE I2C BUS FOR THE SFP THAT
PROVIDES LEGACY TTC SUPPORT IS
LOCATED HERE. IT CAN BE MOVED TO
A DIFFERENT I2C NETWORK IF
DESIRED.

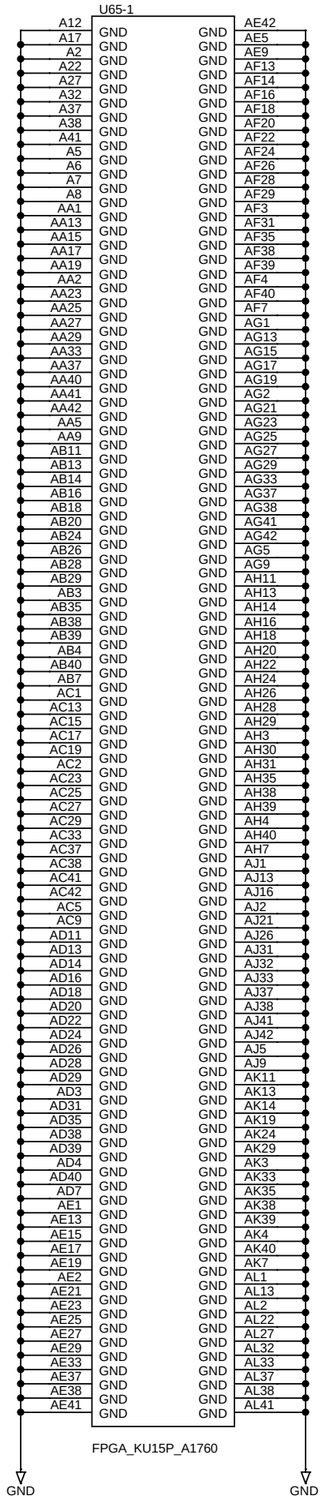


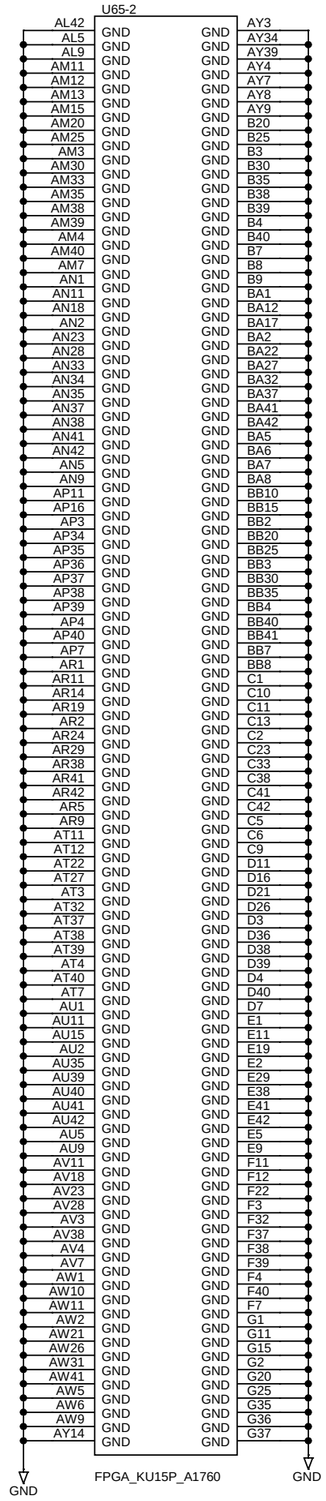
TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

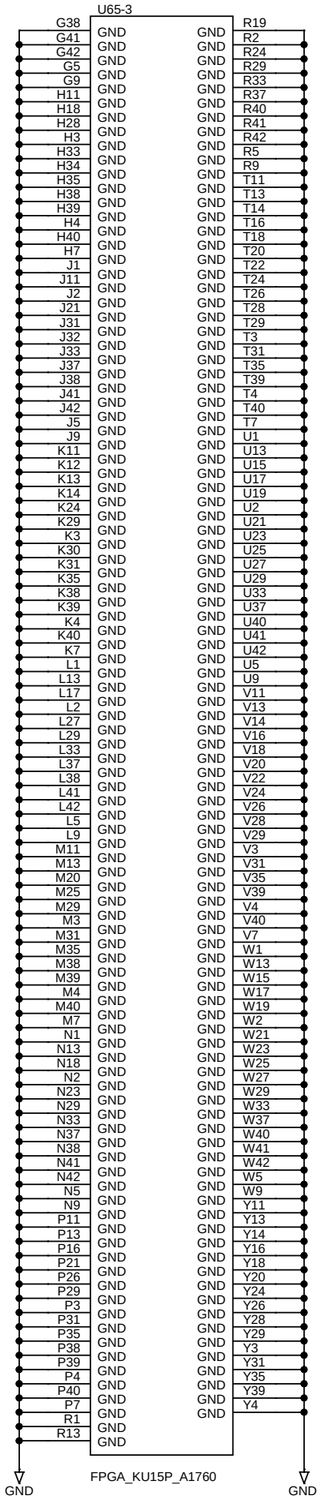
INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

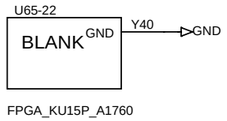
OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

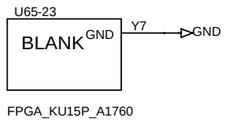
ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 4.06: I2C VU7P OPTICS			
Size	Document Number: 6089-103		Rev: A
Date: Thursday, March 07, 2019	Sheet 30 of 74		









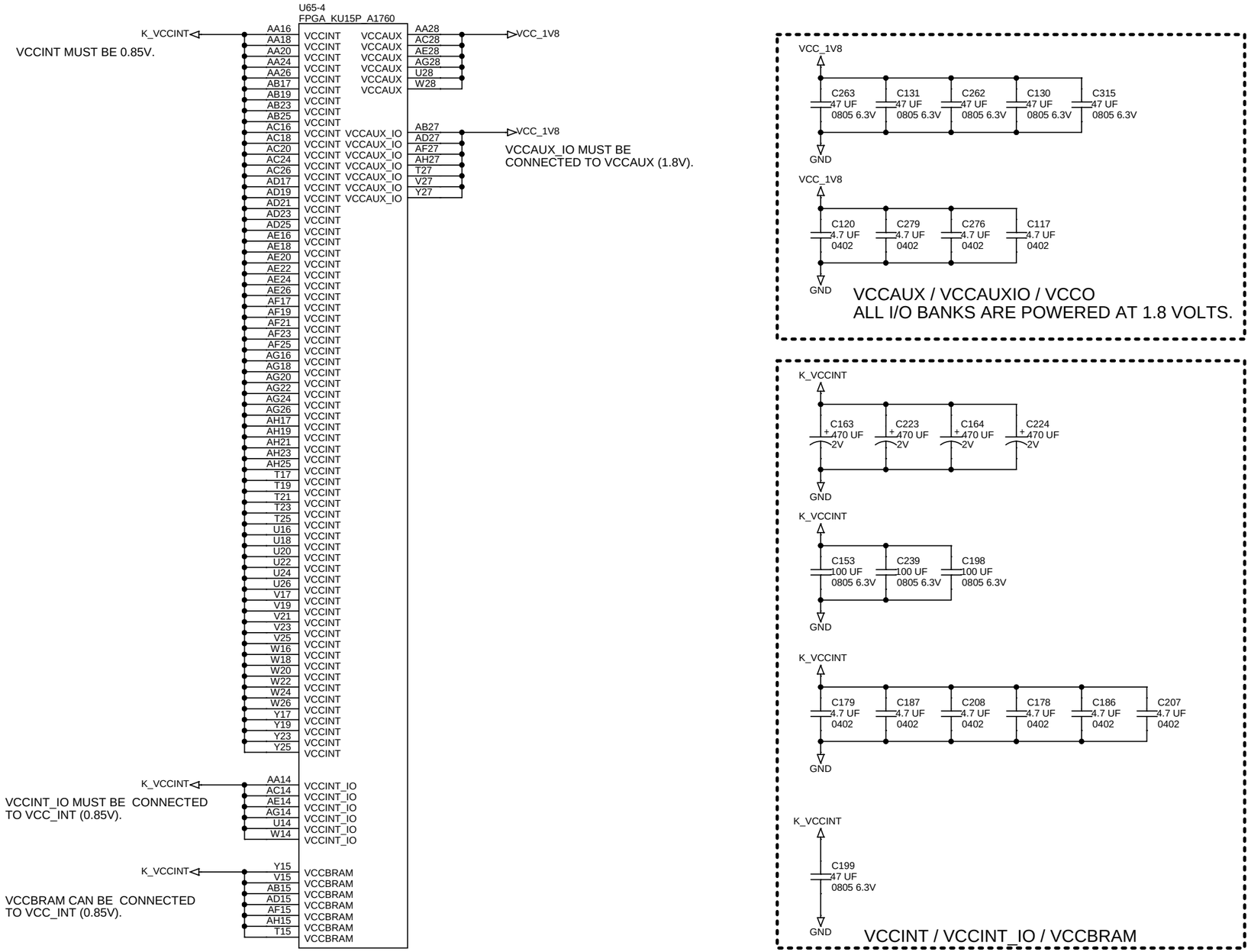


ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.01: KU15P FPGA GND

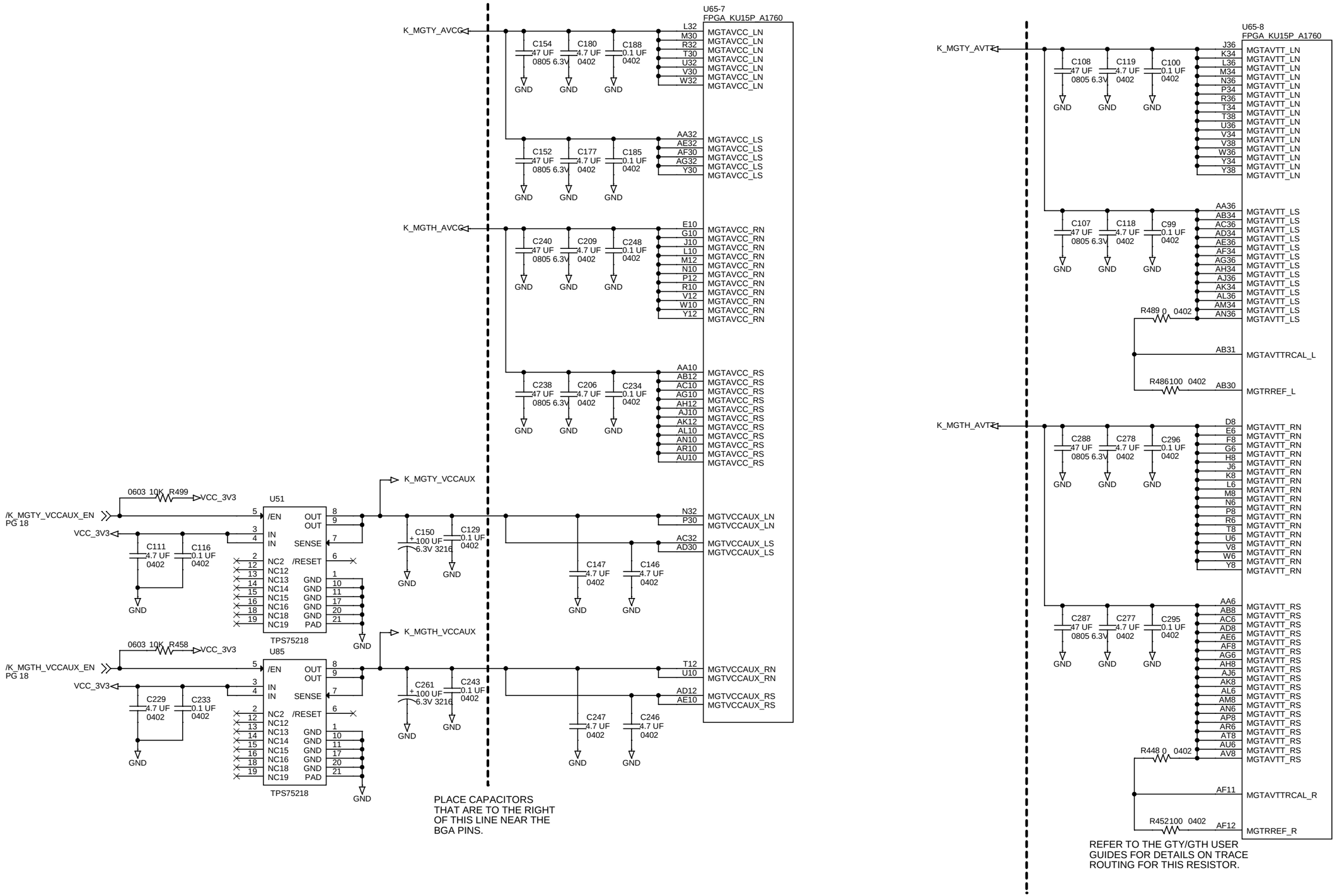
Size	Document Number	Rev
	6089-103	A

Date: Tuesday, February 26, 2019 Sheet 31 of 74



BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"xtp427-ultrascale-plus-schematic-review-checklist.xls"

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.02: KU15P FPGA INTERNAL POWER		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 32 of 74	



ON MIXED TRANSCEIVER DEVICES, REGIONS "LN" AND "LS" ARE GTY TRANSCEIVERS. REGIONS "RN" AND "RS" ARE GTH TRANSCEIVERS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.03: KU15P GTH/GTY TRANSCEIVER POWER

Size	Document Number	Rev
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Date: Tuesday, February 26, 2019 Sheet 33 of 74

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

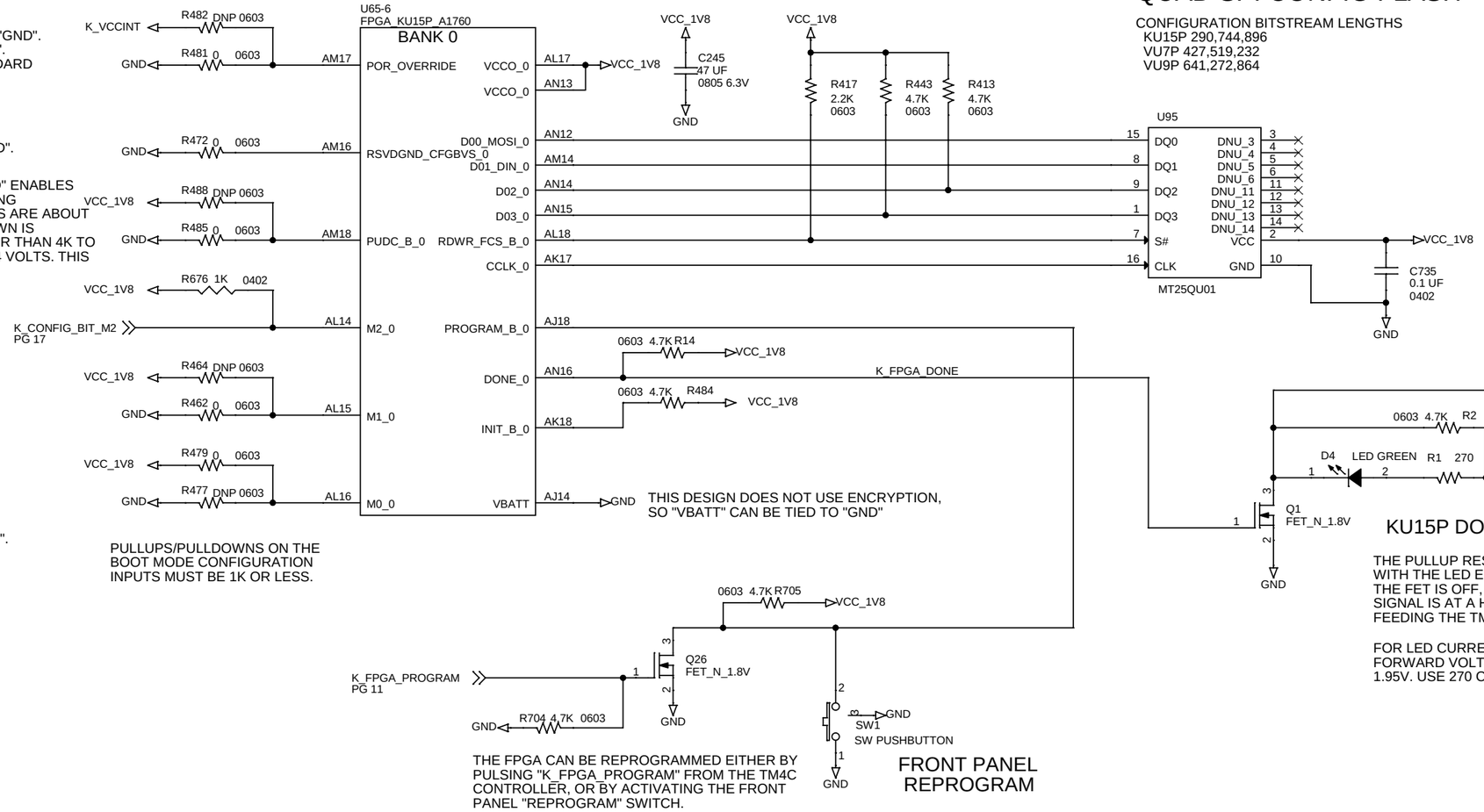
THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

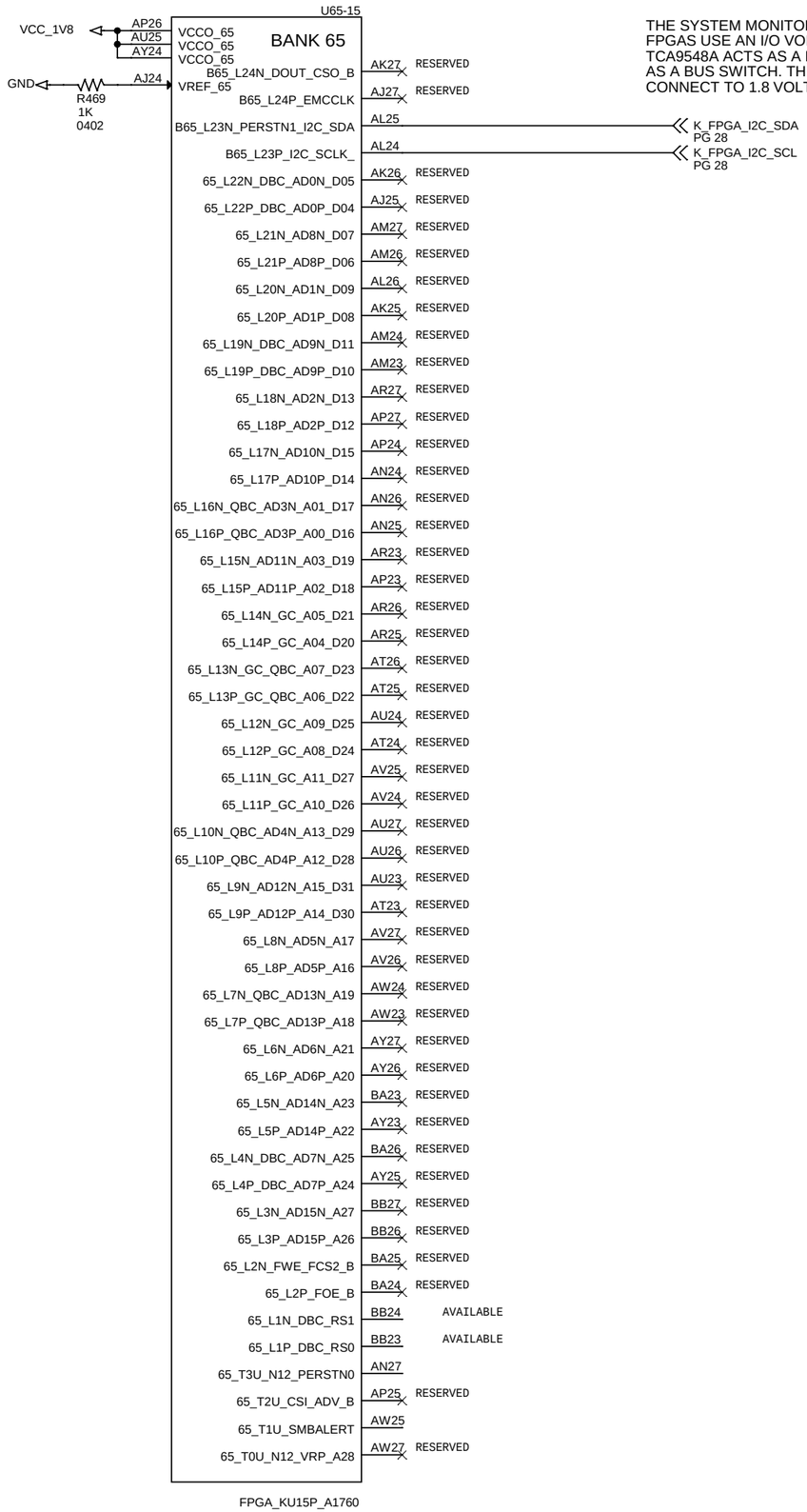
M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

PULLUPS/PULLDOWNS ON THE
BOOT MODE CONFIGURATION
INPUTS MUST BE 1K OR LESS.



ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 5.04: KU15P FPGA CONFIGURATION			
Size	Document Number: 6089-103		Rev: A
Date: Wednesday, March 06, 2019	Sheet 34 of 74		



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

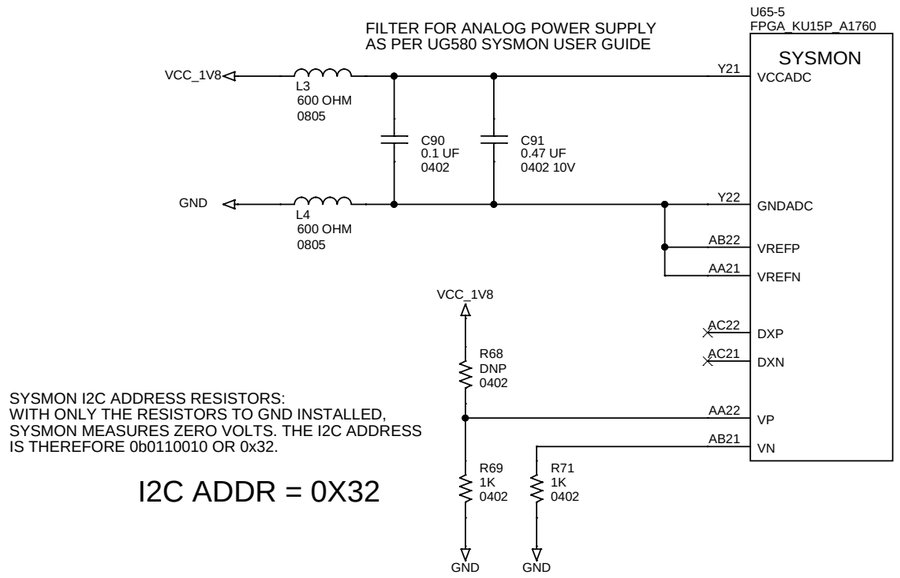
BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.05: KU15P BANK 65

Size	Document Number	Rev
	6089-103	A

Date: Tuesday, February 26, 2019 Sheet 35 of 74



SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

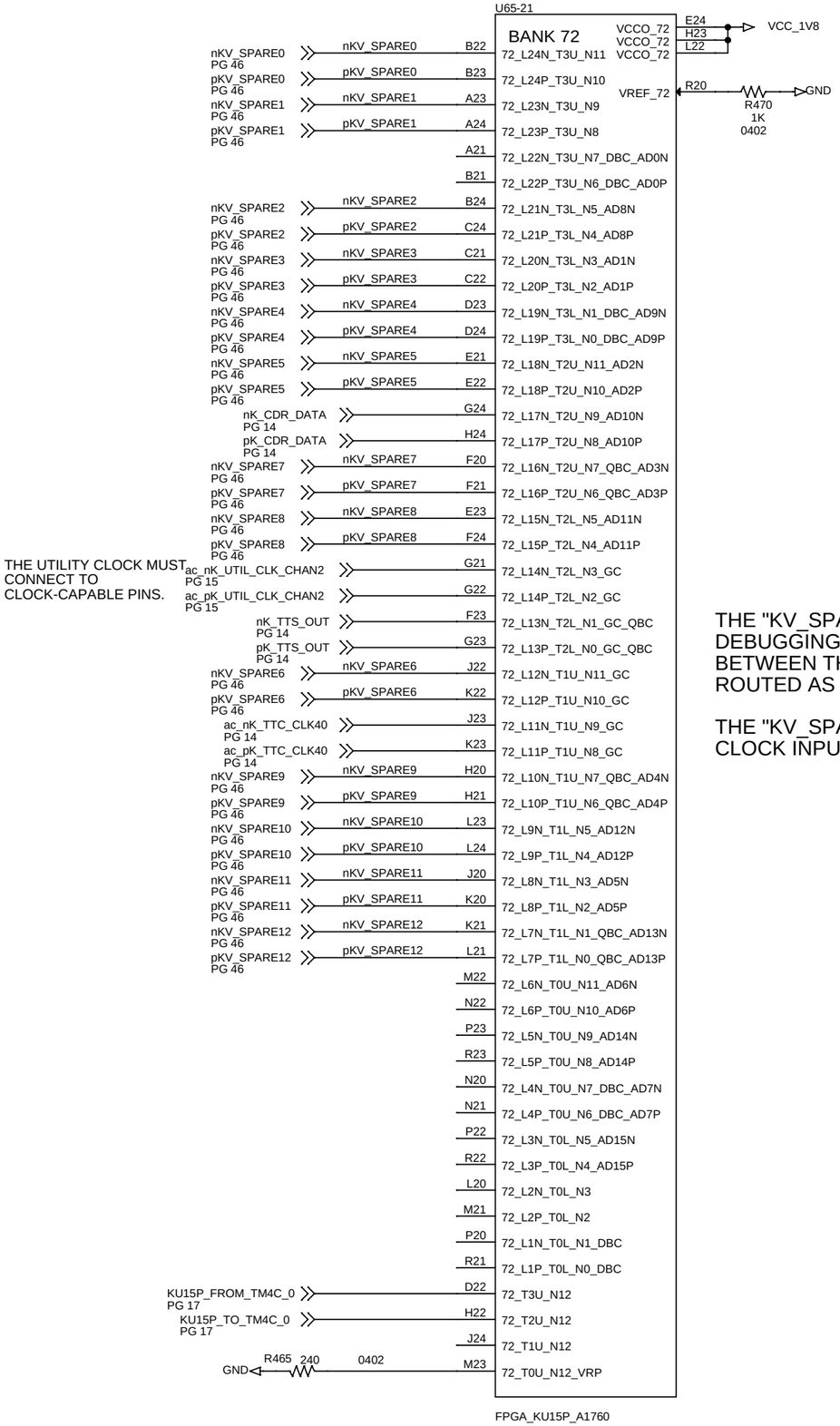
I2C ADDR = 0X32

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.06: KU15P SYSTEM MONITOR

Size | Document Number: 6089-103 | Rev: A

Date: Friday, March 08, 2019 | Sheet 36 of 74

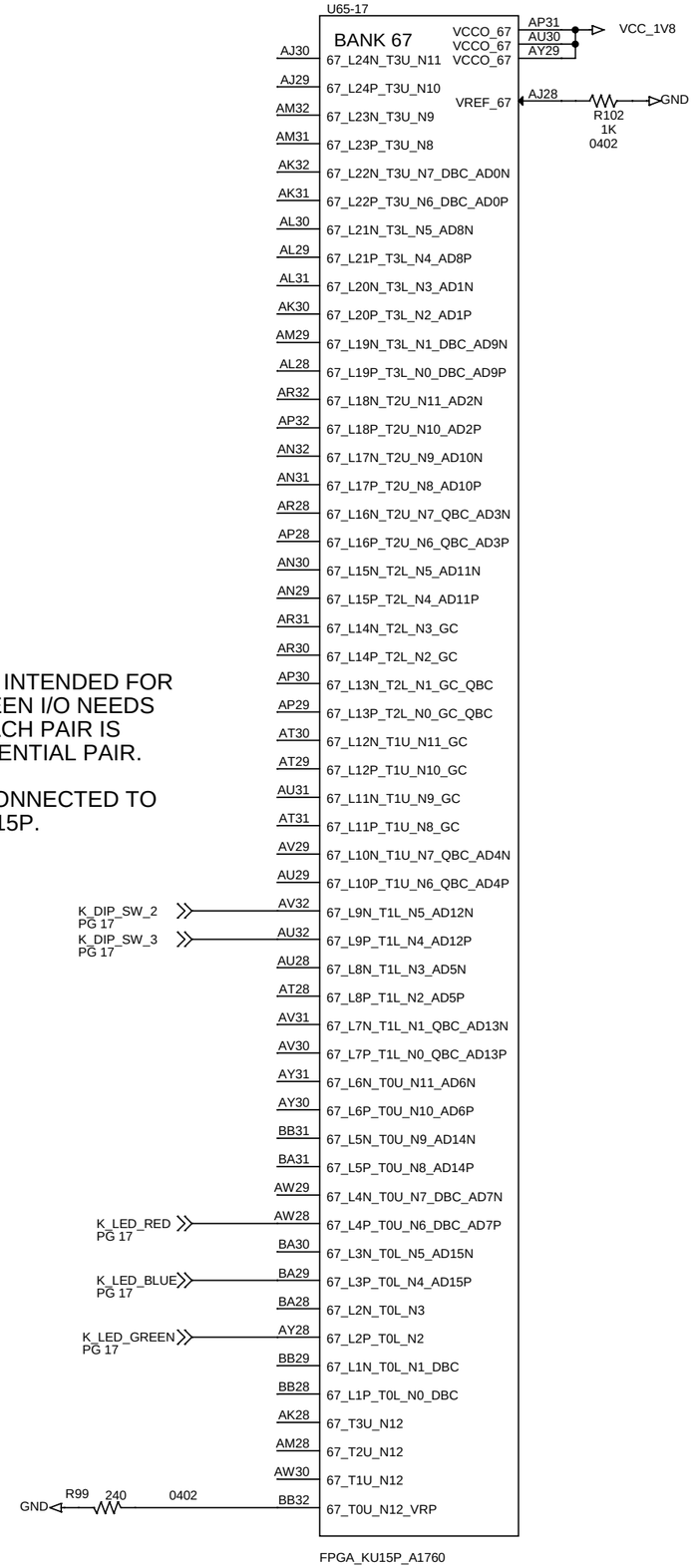


FPGA_KU15P_A1760

THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

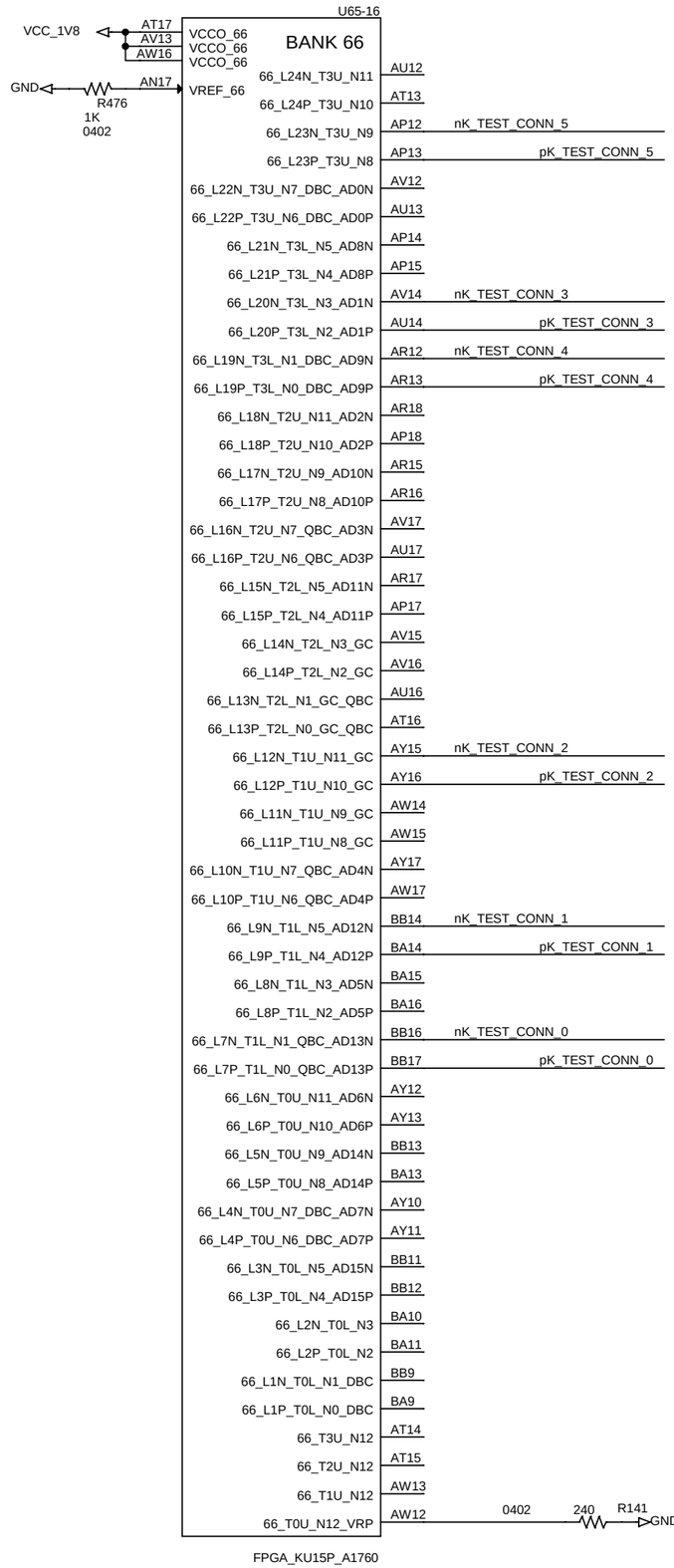
THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

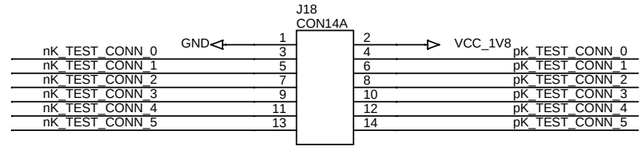
THE "KV_SPARE6" SIGNAL IS CONNECTED TO CLOCK INPUT PINS ON THE KU15P.



FPGA_KU15P_A1760

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.07: KU15P UTILITY BANKS		
Size	Document Number: 6089-103	Rev: A
Date: Friday, August 30, 2019	Sheet 37 of 74	





THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "K_TEST_CONN_2" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.08 KU15P TEST CONNECTOR

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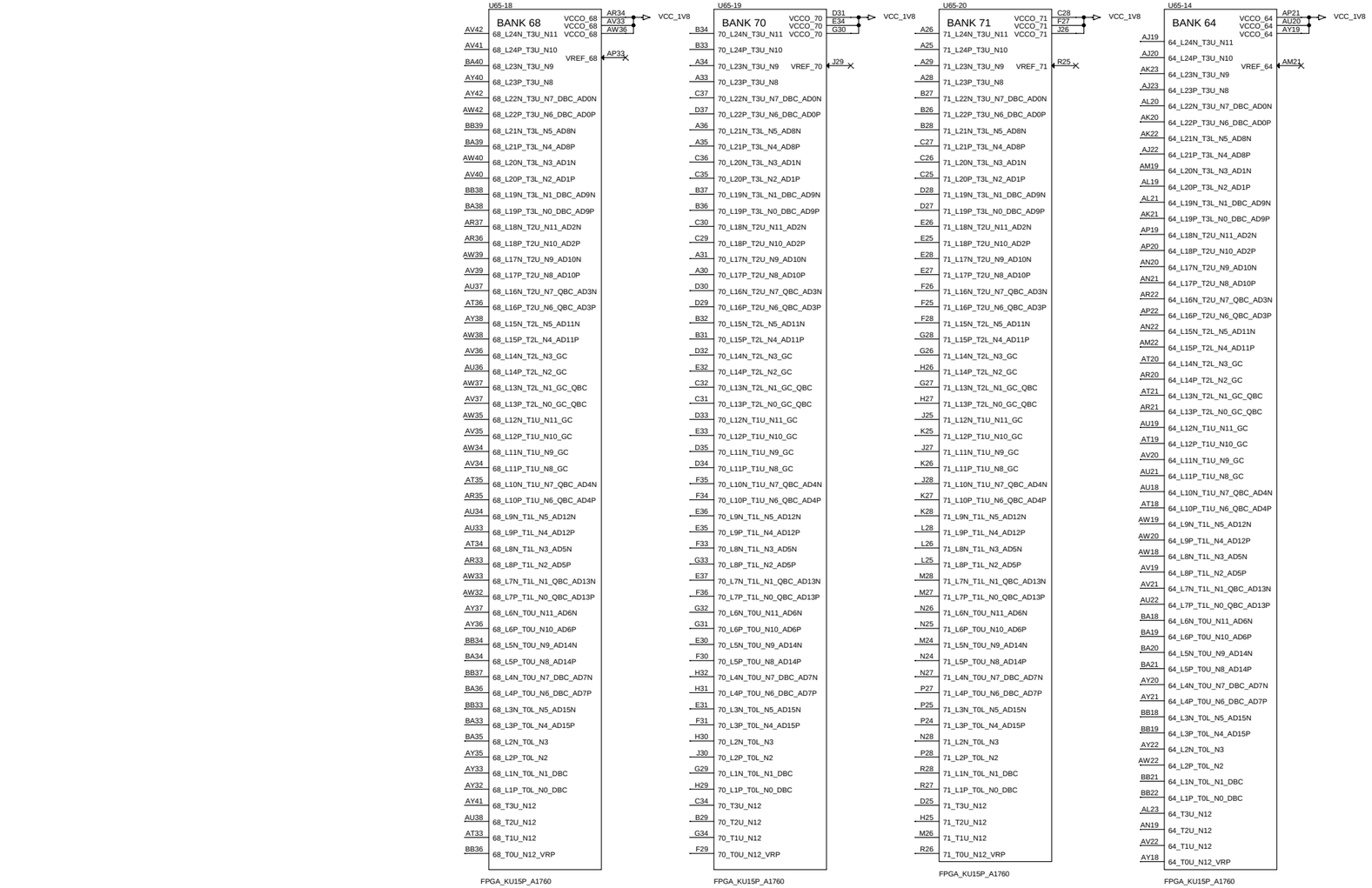

KU15P UNUSED BLOCKS

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.99: KU15P UNUSED BLOCKS

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U66-1
FPGA_VU7P_B2104

A10	GND	GND	AF28
A12	GND	GND	AF3
A21	GND	GND	AF35
A3	GND	GND	AF36
A31	GND	GND	AF4
A41	GND	GND	AF40
A44	GND	GND	AF42
A6	GND	GND	AF45
AA1	GND	GND	AF46
AA10	GND	GND	AF5
AA13	GND	GND	AF8
AA15	GND	GND	AG1
AA17	GND	GND	AG11
AA19	GND	GND	AG17
AA2	GND	GND	AG2
AA21	GND	GND	AG21
AA23	GND	GND	AG23
AA25	GND	GND	AG25
AA27	GND	GND	AG27
AA29	GND	GND	AG33
AA31	GND	GND	AG35
AA35	GND	GND	AG39
AA38	GND	GND	AG42
AA42	GND	GND	AG43
AA43	GND	GND	AG44
AA44	GND	GND	AG5
AA5	GND	GND	AG7
AA6	GND	GND	AH14
AA7	GND	GND	AH16
AB12	GND	GND	AH20
AB14	GND	GND	AH22
AB16	GND	GND	AH24
AB18	GND	GND	AH26
AB20	GND	GND	AH3
AB22	GND	GND	AH30
AB24	GND	GND	AH35
AB26	GND	GND	AH37
AB28	GND	GND	AH4
AB3	GND	GND	AH41
AB30	GND	GND	AH42
AB35	GND	GND	AH45
AB37	GND	GND	AH46
AB4	GND	GND	AH5
AB40	GND	GND	AH9
AB42	GND	GND	AJ1
AB45	GND	GND	AJ10
AB46	GND	GND	AJ13
AB5	GND	GND	AJ15
AB8	GND	GND	AJ17
AC1	GND	GND	AJ2
AC10	GND	GND	AJ21
AC15	GND	GND	AJ23
AC17	GND	GND	AJ25
AC19	GND	GND	AJ35
AC2	GND	GND	AJ38
AC21	GND	GND	AJ42
AC23	GND	GND	AJ43
AC25	GND	GND	AJ44
AC27	GND	GND	AJ5
AC29	GND	GND	AJ6
AC35	GND	GND	AK14
AC39	GND	GND	AK16
AC42	GND	GND	AK18
AC43	GND	GND	AK20
AC44	GND	GND	AK22
AC5	GND	GND	AK24
AC7	GND	GND	AK3
AD14	GND	GND	AK34
AD16	GND	GND	AK35
AD18	GND	GND	AK37
AD20	GND	GND	AK4
AD22	GND	GND	AK40
AD24	GND	GND	AK42
AD26	GND	GND	AK45
AD28	GND	GND	AK46
AD3	GND	GND	AK5
AD32	GND	GND	AK8
AD35	GND	GND	AL1
AD37	GND	GND	AL11
AD4	GND	GND	AL2
AD41	GND	GND	AL31
AD42	GND	GND	AL35
AD45	GND	GND	AL39
AD46	GND	GND	AL42
AD5	GND	GND	AL43
AD9	GND	GND	AL44
AE1	GND	GND	AL5
AE10	GND	GND	AL7
AE17	GND	GND	AM18
AE19	GND	GND	AM28
AE2	GND	GND	AM3
AE21	GND	GND	AM35
AE23	GND	GND	AM37
AE25	GND	GND	AM4
AE27	GND	GND	AM41
AE29	GND	GND	AM42
AE35	GND	GND	AM45
AE38	GND	GND	AM46
AE42	GND	GND	AM5
AE43	GND	GND	AM9
AE44	GND	GND	AN1
AE5	GND	GND	AN10
AE6	GND	GND	AN12
AF12	GND	GND	AN15
AF14	GND	GND	AN2
AF16	GND	GND	AN25
AF20	GND	GND	AN35
AF22	GND	GND	AN38
AF24	GND	GND	AN42
AF26	GND	GND	AN43

GND

U66-2
FPGA_VU7P_B2104

AN44	GND	GND	B44
AN5	GND	GND	B45
AN6	GND	GND	B5
AP12	GND	GND	B6
AP22	GND	GND	B7
AP3	GND	GND	B8
AP32	GND	GND	BA11
AP35	GND	GND	BA21
AP36	GND	GND	BA3
AP4	GND	GND	BA31
AP40	GND	GND	BA37
AP42	GND	GND	BA38
AP45	GND	GND	BA39
AP46	GND	GND	BA44
AP5	GND	GND	BA6
AP8	GND	GND	BB1
AR1	GND	GND	BB18
AR11	GND	GND	BB2
AR12	GND	GND	BB28
AR19	GND	GND	BB3
AR2	GND	GND	BB39
AR29	GND	GND	BB40
AR35	GND	GND	BB41
AR39	GND	GND	BB44
AR42	GND	GND	BB45
AR43	GND	GND	BB46
AR44	GND	GND	BB6
AR5	GND	GND	BB8
AR7	GND	GND	BC15
AT12	GND	GND	BC25
AT16	GND	GND	BC3
AT26	GND	GND	BC35
AT3	GND	GND	BC4
AT35	GND	GND	BC41
AT37	GND	GND	BC42
AT4	GND	GND	BC44
AT41	GND	GND	BC6
AT42	GND	GND	BD1
AT45	GND	GND	BD12
AT46	GND	GND	BD22
AT5	GND	GND	BD3
AT9	GND	GND	BD32
AU1	GND	GND	BD41
AU10	GND	GND	BD44
AU12	GND	GND	BD46
AU2	GND	GND	BD6
AU23	GND	GND	BE19
AU33	GND	GND	BE2
AU35	GND	GND	BE29
AU38	GND	GND	BE3
AU42	GND	GND	BE39
AU43	GND	GND	BE41
AU44	GND	GND	BE45
AU5	GND	GND	BE5
AU6	GND	GND	BE6
AV12	GND	GND	BE9
AV20	GND	GND	BF16
AV3	GND	GND	BF26
AV30	GND	GND	BF3
AV35	GND	GND	BF36
AV36	GND	GND	BF41
AV37	GND	GND	BF44
AV4	GND	GND	BF6
AV40	GND	GND	C1
AV42	GND	GND	C11
AV45	GND	GND	C12
AV46	GND	GND	C15
AV5	GND	GND	C2
AV8	GND	GND	C25
AW1	GND	GND	C35
AW10	GND	GND	C41
AW11	GND	GND	C44
AW12	GND	GND	C46
AW17	GND	GND	C5
AW2	GND	GND	D12
AW27	GND	GND	D22
AW37	GND	GND	D3
AW39	GND	GND	D32
AW42	GND	GND	D4
AW43	GND	GND	D41
AW44	GND	GND	D42
AW5	GND	GND	D44
AW6	GND	GND	D5
AY1	GND	GND	D9
AY10	GND	GND	E1
AY14	GND	GND	E10
AY2	GND	GND	E12
AY24	GND	GND	E19
AY3	GND	GND	E2
AY34	GND	GND	E29
AY37	GND	GND	E41
AY4	GND	GND	E44
AY41	GND	GND	E45
AY42	GND	GND	E46
AY43	GND	GND	E5
AY44	GND	GND	E6
AY45	GND	GND	F12
AY46	GND	GND	F16
AY5	GND	GND	F26
AY6	GND	GND	F3
AY7	GND	GND	F36
AY8	GND	GND	F39
AY9	GND	GND	F4
B12	GND	GND	F40
B18	GND	GND	F41
B2	GND	GND	F44
B28	GND	GND	F5
B38	GND	GND	F8
B4	GND	GND	G1
B41	GND	GND	G11

GND

U66-3
FPGA_VU7P_B2104

G12	GND	GND	R35
G13	GND	GND	R39
G2	GND	GND	R42
G23	GND	GND	R43
G33	GND	GND	R44
G39	GND	GND	R5
G42	GND	GND	R7
G43	GND	GND	T12
G44	GND	GND	T14
G45	GND	GND	T16
G46	GND	GND	T18
G5	GND	GND	T20
G7	GND	GND	T22
H12	GND	GND	T24
H20	GND	GND	T3
H3	GND	GND	T35
H30	GND	GND	T37
H39	GND	GND	T4
H4	GND	GND	T41
H41	GND	GND	T42
H42	GND	GND	T45
H45	GND	GND	T46
H46	GND	GND	T5
H5	GND	GND	T9
H9	GND	GND	U1
J1	GND	GND	U10
J10	GND	GND	U13
J12	GND	GND	U15
J17	GND	GND	U17
J2	GND	GND	U19
J27	GND	GND	U2
J37	GND	GND	U21
J38	GND	GND	U23
J39	GND	GND	U25
J42	GND	GND	U27
J43	GND	GND	U33
J44	GND	GND	U35
J5	GND	GND	U38
J6	GND	GND	U42
K12	GND	GND	U43
K14	GND	GND	U44
K24	GND	GND	U5
K3	GND	GND	U6
K35	GND	GND	V14
K36	GND	GND	V16
K37	GND	GND	V18
K4	GND	GND	V20
K40	GND	GND	V22
K42	GND	GND	V24
K45	GND	GND	V26
K46	GND	GND	V28
K5	GND	GND	V3
K8	GND	GND	V30
L1	GND	GND	V35
L11	GND	GND	V36
L12	GND	GND	V4
L2	GND	GND	V40
L21	GND	GND	V42
L31	GND	GND	V45
L35	GND	GND	V46
L39	GND	GND	V5
L42	GND	GND	V8
L43	GND	GND	W1
L44	GND	GND	W11
L5	GND	GND	W13
L7	GND	GND	W15
M12	GND	GND	W17
M18	GND	GND	W19
M28	GND	GND	W2
M3	GND	GND	W21
M35	GND	GND	W23
M37	GND	GND	W25
M4	GND	GND	W27
M41	GND	GND	W29
M42	GND	GND	W35
M45	GND	GND	W39
M46	GND	GND	W42
M5	GND	GND	W43
M9	GND	GND	W44
N1	GND	GND	W5
N10	GND	GND	W7
N12	GND	GND	Y14
N15	GND	GND	Y16
N2	GND	GND	Y18
N25	GND	GND	Y20
N35	GND	GND	Y22
N38	GND	GND	Y24
N42	GND	GND	Y26
N43	GND	GND	Y28
N44	GND	GND	Y3
N5	GND	GND	Y34
N6	GND	GND	Y35
P12	GND	GND	Y37
P22	GND	GND	Y4
P3	GND	GND	Y41
P32	GND	GND	Y42
P35	GND	GND	Y45
P36	GND	GND	Y46
P4	GND	GND	Y5
P40	GND	GND	Y9
P42	GND		
P45	GND		
P46	GND		
P5	GND		
P8	GND		
R1	GND		
R10	GND		
R19	GND		
R2	GND		
R29	GND		

GND

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title
6.01: VU7P FPGA GND

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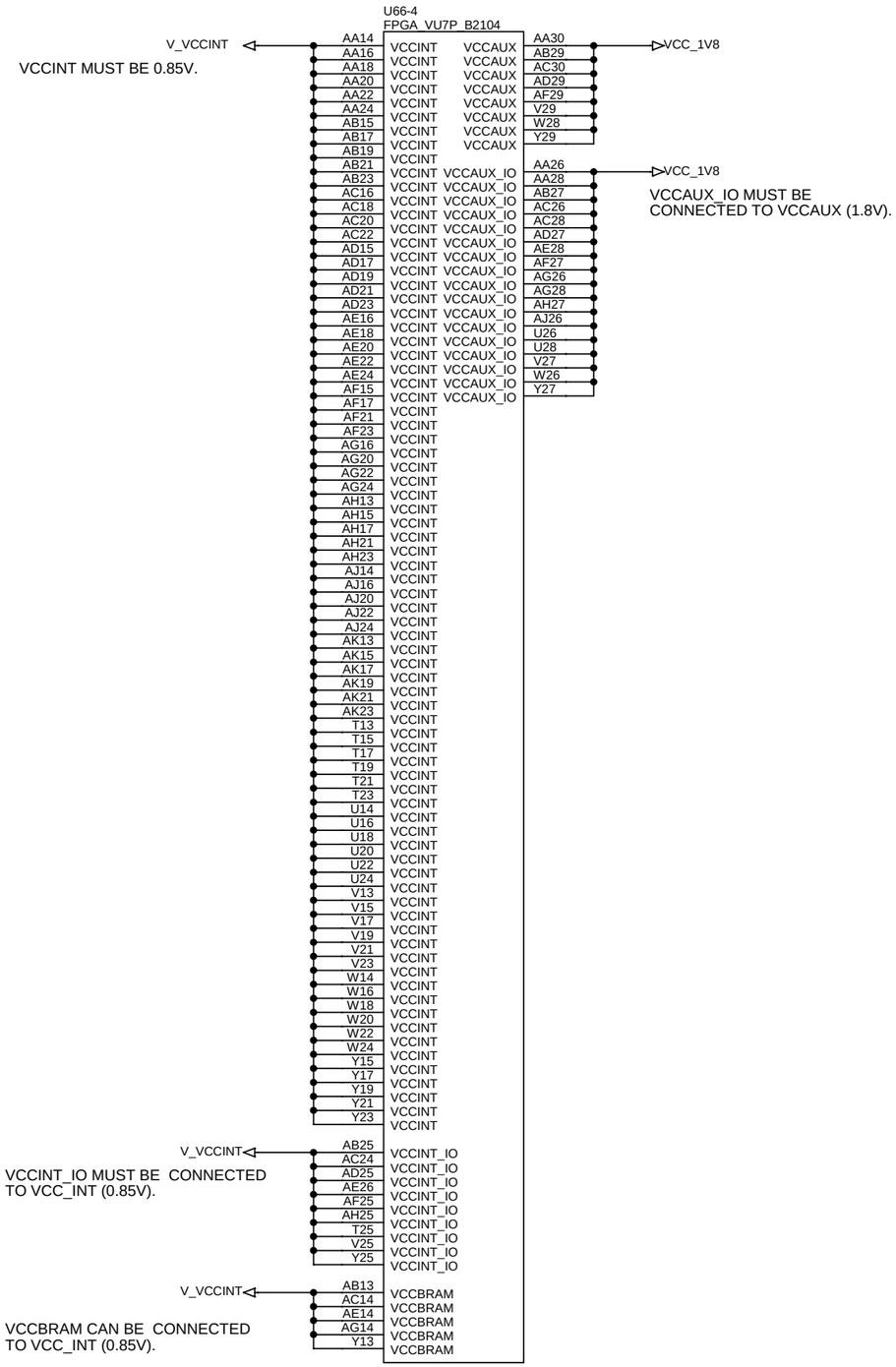

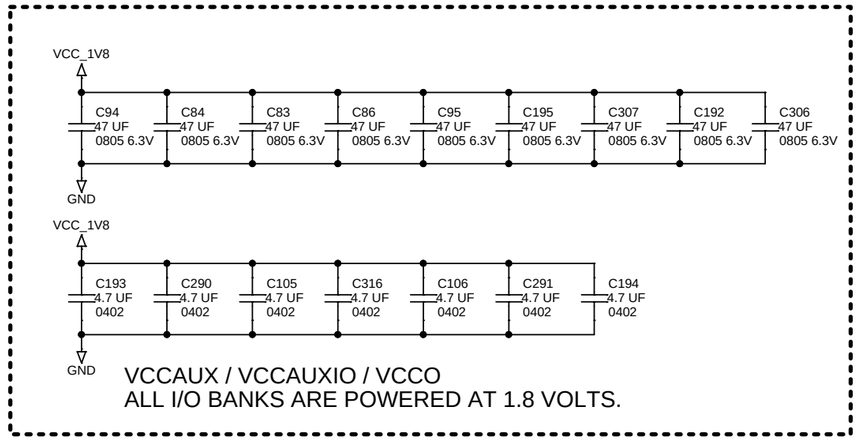

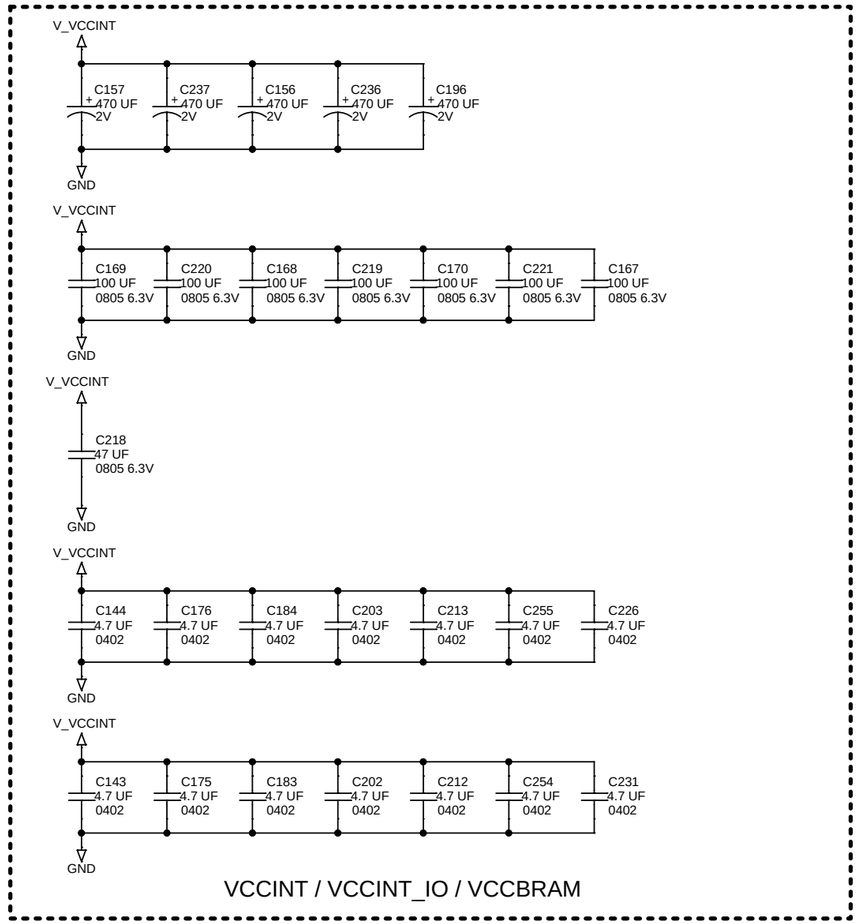

BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"xtp427-ultrascale-plus-schematic-review-checklist.xls"

QUANTITIES BASE ON POSSIBLE UPGRADE TO VU9P

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.02: VU7P FPGA INTERNAL POWER		
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U66-7
FPGA_VU7P_B2104

V_MGTY1_AVCC
C139 47 UF 0805 6.3V
C145 4.7 UF 0402
C136 0.1 UF 0402
GND
AD36 MGTAVCC_LN
AF37 MGTAVCC_LN
L38 MGTAVCC_LN
M36 MGTAVCC_LN
N39 MGTAVCC_LN
P37 MGTAVCC_LN
R38 MGTAVCC_LN
T36 MGTAVCC_LN
U39 MGTAVCC_LN
V37 MGTAVCC_LN

C138 47 UF 0805 6.3V
C142 4.7 UF 0402
C133 0.1 UF 0402
AG38 MGTAVCC_LS
AL38 MGTAVCC_LS
AM36 MGTAVCC_LS
AP37 MGTAVCC_LS
AR38 MGTAVCC_LS
AT36 MGTAVCC_LS
AW38 MGTAVCC_LS
AY40 MGTAVCC_LS

V_MGTY2_AVCC
C259 47 UF 0805 6.3V
C256 4.7 UF 0402
C268 0.1 UF 0402
A11 MGTAVCC_RN
A7 MGTAVCC_RN
B9 MGTAVCC_RN
C10 MGTAVCC_RN
E11 MGTAVCC_RN
G10 MGTAVCC_RN
J11 MGTAVCC_RN
L10 MGTAVCC_RN
N11 MGTAVCC_RN
W10 MGTAVCC_RN

C258 47 UF 0805 6.3V
C253 4.7 UF 0402
C265 0.1 UF 0402
AA11 MGTAVCC_RS
AG10 MGTAVCC_RS
AJ11 MGTAVCC_RS
AL10 MGTAVCC_RS
AN11 MGTAVCC_RS
AP9 MGTAVCC_RS
AR10 MGTAVCC_RS
AU11 MGTAVCC_RS
AV9 MGTAVCC_RS
AW7 MGTAVCC_RS

0603 10K R495
VCC_3V3
/V_MGTY1_VCCAUX_EN
PG 18
U54
/EN
IN
IN
NC2
NC12
NC13
NC14
NC15
NC16
NC18
NC19
OUT
OUT
SENSE
/RESET
GND
PAD
TPS75218
V_MGTY1_VCCAUX
C776 4.7 UF 0402
C777 0.1 UF 0402
C114 100 UF 6.3V 3216
C126 0.1 UF 0402
GND
AB36 MGTVCCAUX_LN
Y36 MGTVCCAUX_LN
AH36 MGTVCCAUX_LS
AK36 MGTVCCAUX_LS
C135 4.7 UF 0402
C134 4.7 UF 0402

0603 10K R408
VCC_3V3
/V_MGTY2_VCCAUX_EN
PG 18
U99
TPS75218
V_MGTY2_VCCAUX
C727 4.7 UF 0402
C728 0.1 UF 0402
C299 100 UF 6.3V 3216
C302 0.1 UF 0402
R11 MGTVCCAUX_RN
U11 MGTVCCAUX_RN
AC11 MGTVCCAUX_RS
AE11 MGTVCCAUX_RS
C267 4.7 UF 0402
C266 4.7 UF 0402

PLACE CAPACITORS
THAT ARE TO THE RIGHT
OF THIS LINE NEAR THE
BGA PINS.

U66-8
FPGA_VU7P_B2104

V_MGTY1_AVTT
C123 47 UF 0805 6.3V
C125 4.7 UF 0402
C113 0.1 UF 0402
GND
AA39 MGTAVTT_LN
AB41 MGTAVTT_LN
AC38 MGTAVTT_LN
AD40 MGTAVTT_LN
AE39 MGTAVTT_LN
AF41 MGTAVTT_LN
C45 MGTAVTT_LN
D43 MGTAVTT_LN
F42 MGTAVTT_LN
F43 MGTAVTT_LN
H40 MGTAVTT_LN
K41 MGTAVTT_LN
M40 MGTAVTT_LN
P41 MGTAVTT_LN
T40 MGTAVTT_LN
V41 MGTAVTT_LN
W38 MGTAVTT_LN
Y40 MGTAVTT_LN
R91 0 0402
B42 MGTAVTTRCAL_LN
R88 100 0402
B43 MGTRREF_LN

C122 47 UF 0805 6.3V
C112 4.7 UF 0402
C124 0.1 UF 0402
AH40 MGTAVTT_LS
AJ39 MGTAVTT_LS
AK41 MGTAVTT_LS
AM40 MGTAVTT_LS
AN39 MGTAVTT_LS
AP41 MGTAVTT_LS
AT40 MGTAVTT_LS
AU39 MGTAVTT_LS
AV41 MGTAVTT_LS
BA42 MGTAVTT_LS
BA43 MGTAVTT_LS
BC43 MGTAVTT_LS
BD45 MGTAVTT_LS
BE44 MGTAVTT_LS
R90 0 0402
BE42 MGTAVTTRCAL_LS
R87 100 0402
BE43 MGTRREF_LS

V_MGTY2_AVTT
C280 47 UF 0805 6.3V
C275 4.7 UF 0402
C285 0.1 UF 0402
B3 MGTAVTT_RN
D8 MGTAVTT_RN
E7 MGTAVTT_RN
F9 MGTAVTT_RN
G6 MGTAVTT_RN
H8 MGTAVTT_RN
J7 MGTAVTT_RN
K9 MGTAVTT_RN
L6 MGTAVTT_RN
M8 MGTAVTT_RN
N7 MGTAVTT_RN
P9 MGTAVTT_RN
R6 MGTAVTT_RN
T8 MGTAVTT_RN
U7 MGTAVTT_RN
V9 MGTAVTT_RN
W6 MGTAVTT_RN
Y8 MGTAVTT_RN
R146 0 0402
C7 MGTAVTTRCAL_RN
R151 100 0402
C6 MGTRREF_RN

C282 47 UF 0805 6.3V
C274 4.7 UF 0402
C284 0.1 UF 0402
AB9 MGTAVTT_RS
AC6 MGTAVTT_RS
AD8 MGTAVTT_RS
AE7 MGTAVTT_RS
AF9 MGTAVTT_RS
AG6 MGTAVTT_RS
AH8 MGTAVTT_RS
AJ7 MGTAVTT_RS
AK9 MGTAVTT_RS
AL6 MGTAVTT_RS
AM8 MGTAVTT_RS
AN7 MGTAVTT_RS
AR6 MGTAVTT_RS
AT8 MGTAVTT_RS
AU7 MGTAVTT_RS
BC5 MGTAVTT_RS
BD2 MGTAVTT_RS
BE4 MGTAVTT_RS
R145 0 0402
BA5 MGTAVTTRCAL_RS
R150 100 0402
BA4 MGTRREF_RS

REFER TO THE GTY/GTH USER
GUIDES FOR DETAILS ON TRACE
ROUTING FOR THIS RESISTOR.

PLACE CAPACITORS AND RESISTORS
THAT ARE TO THE RIGHT OF THIS LINE
NEAR THE BGA PINS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title
6.03: VU7P GTY TRANSCEIVER POWER

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MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

V_VCCINT
R478 DNP 0603
GND
R480 0 0603
AD12 POR_OVERRIDE

GND
R449 0 0603
W12 RSVDGND

VCC_1V8
R463 DNP 0603
GND
R474 0 0603
AA12 PUDC_B_0

VCC_1V8
R682 1K 0402
V_CONFIG_BIT_M2
PG 17
R12 M2_0

VCC_1V8
R459 DNP 0603
GND
R461 0 0603
U12 M1_0

VCC_1V8
R450 0 0603
GND
R451 DNP 0603
V12 M0_0

U66-6
FPGA_VU7P_B2104
BANK 0

VCCO_0 AD13 VCC_1V8
VCCO_0 AF13
D00_MOSI_0 AK12
D01_DIN_0 AJ12
D02_0 AL12
D03_0 AH12
RDWR_FCS_B_0 AG12
CCLK_0 AG13
PROGRAM_B_0 AE12
DONE_0 AC12
INIT_B_0 Y12
VBATT AM12 GND

VCC_1V8
C292
47 UF
0805 6.3V
GND

VCC_1V8
R406 2.2K 0603
R409 4.7K 0603
R407 4.7K 0603

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

U98
MT25QU01
15 DQ0
8 DQ1
9 DQ2
1 DQ3
7 S#
16 CLK
DNU_3 3
DNU_4 4
DNU_5 5
DNU_6 6
DNU_11 11
DNU_12 12
DNU_13 13
DNU_14 14
VCC 2
GND 10

VCC_1V8
C729
0.1 UF
0402
GND

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

PULLUPS/PULLDOWNS ON THE
BOOT MODE CONFIGURATION
INPUTS MUST BE 1K OR LESS.

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

0603 4.7K R21
VCC_1V8
V_FPGA_DONE
0603 4.7K R453
VCC_1V8

/V_FPGA_DONE
PG 11
0603 4.7K R7
D7 LED GREEN R6 270
VCC_3V3
Q5
FET_N_1.8V
GND

VU7P DONE LED

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/V_FPGA_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE TM4C CONTROLLER.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

0603 4.7K R713
VCC_1V8
V_FPGA_PROGRAM
PG 11
Q27
FET_N_1.8V
R712 4.7K 0603
GND
SW3
SW PUSHBUTTON

THE FPGA CAN BE REPROGRAMMED EITHER BY PULSING "V_FPGA_PROGRAM" FROM THE TM4C CONTROLLER, OR BY ACTIVATING THE FRONT PANEL "REPROGRAM" SWITCH.

FRONT PANEL REPROGRAM

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title
6.04: VU7P FPGA CONFIGURATION

Size	Document Number	Rev
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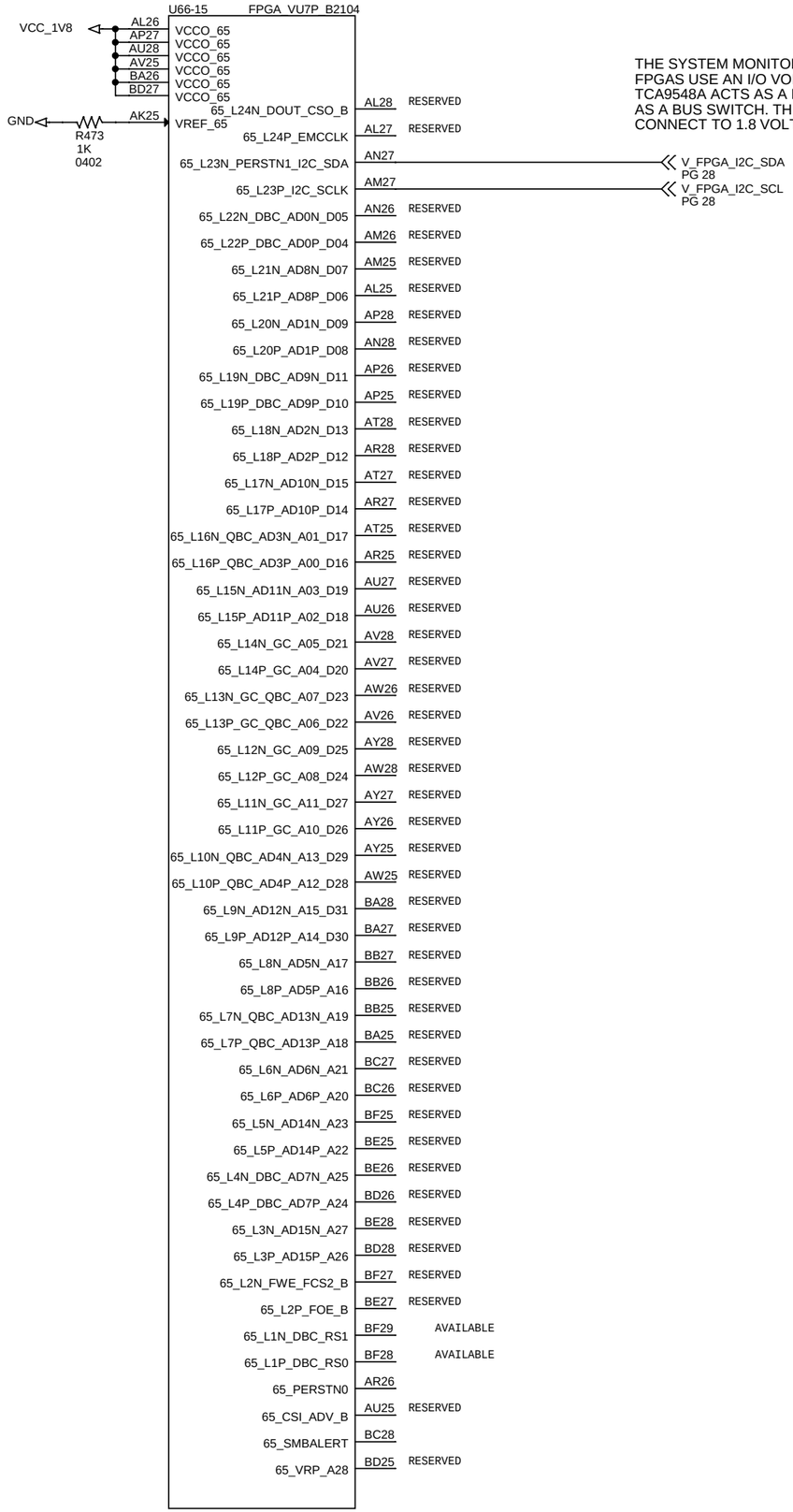
Date: Wednesday, March 06, 2019 Sheet 43 of 74



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

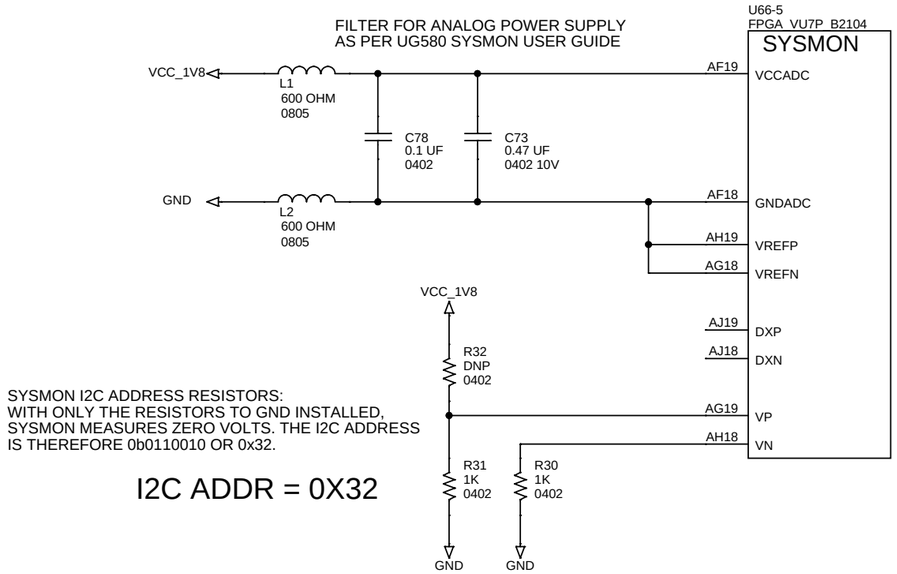
BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.05: VU7P BANK 65

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 44 of 74



SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

I2C ADDR = 0X32

ATCA FPGA BOARD, KU15P AND VU7P, MK1

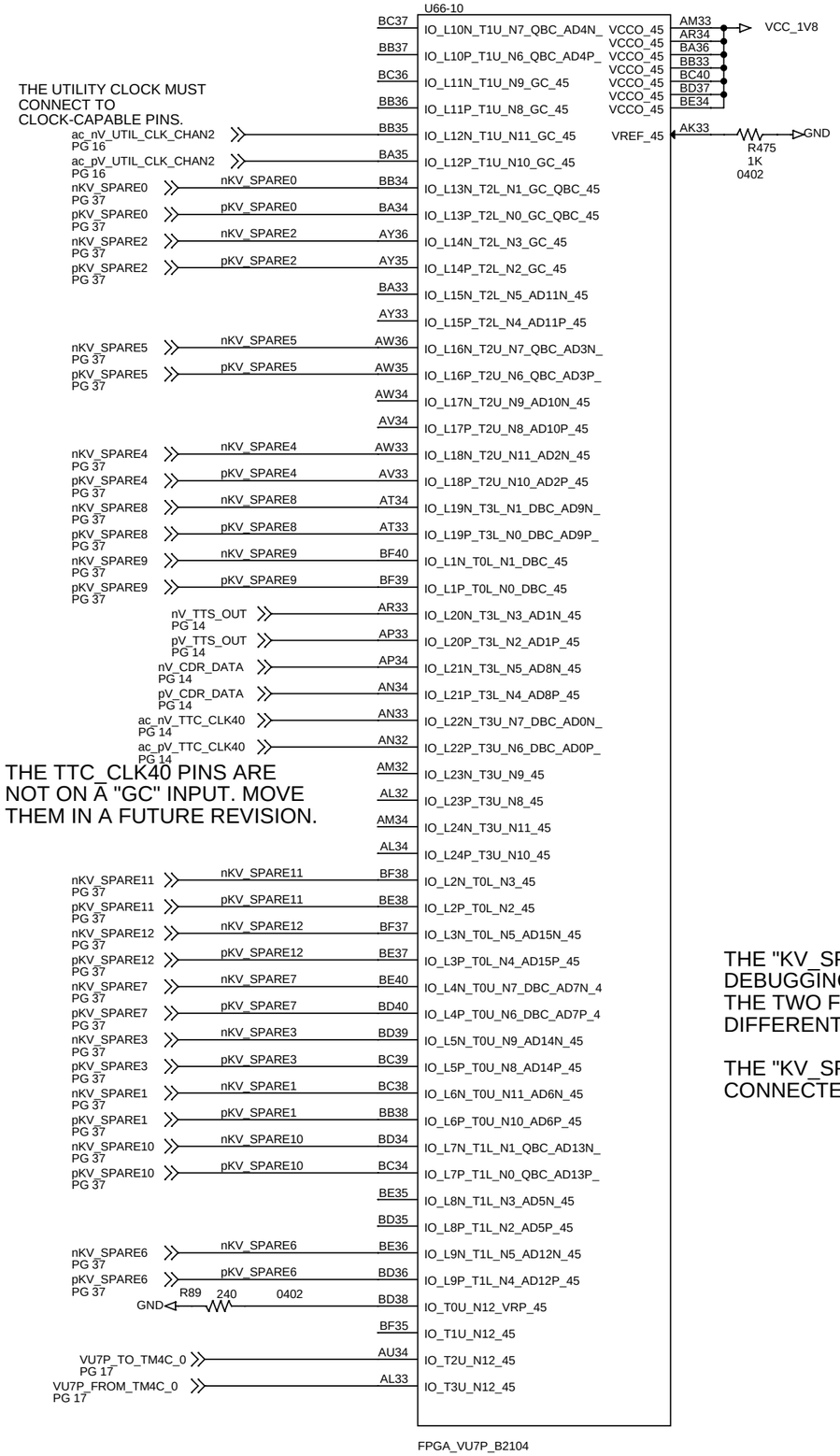
Title: 6.06: VU7P SYSTEM MONITOR

Size	Document Number	Rev
	6089-103	A

Date: Friday, March 08, 2019 Sheet 45 of 74

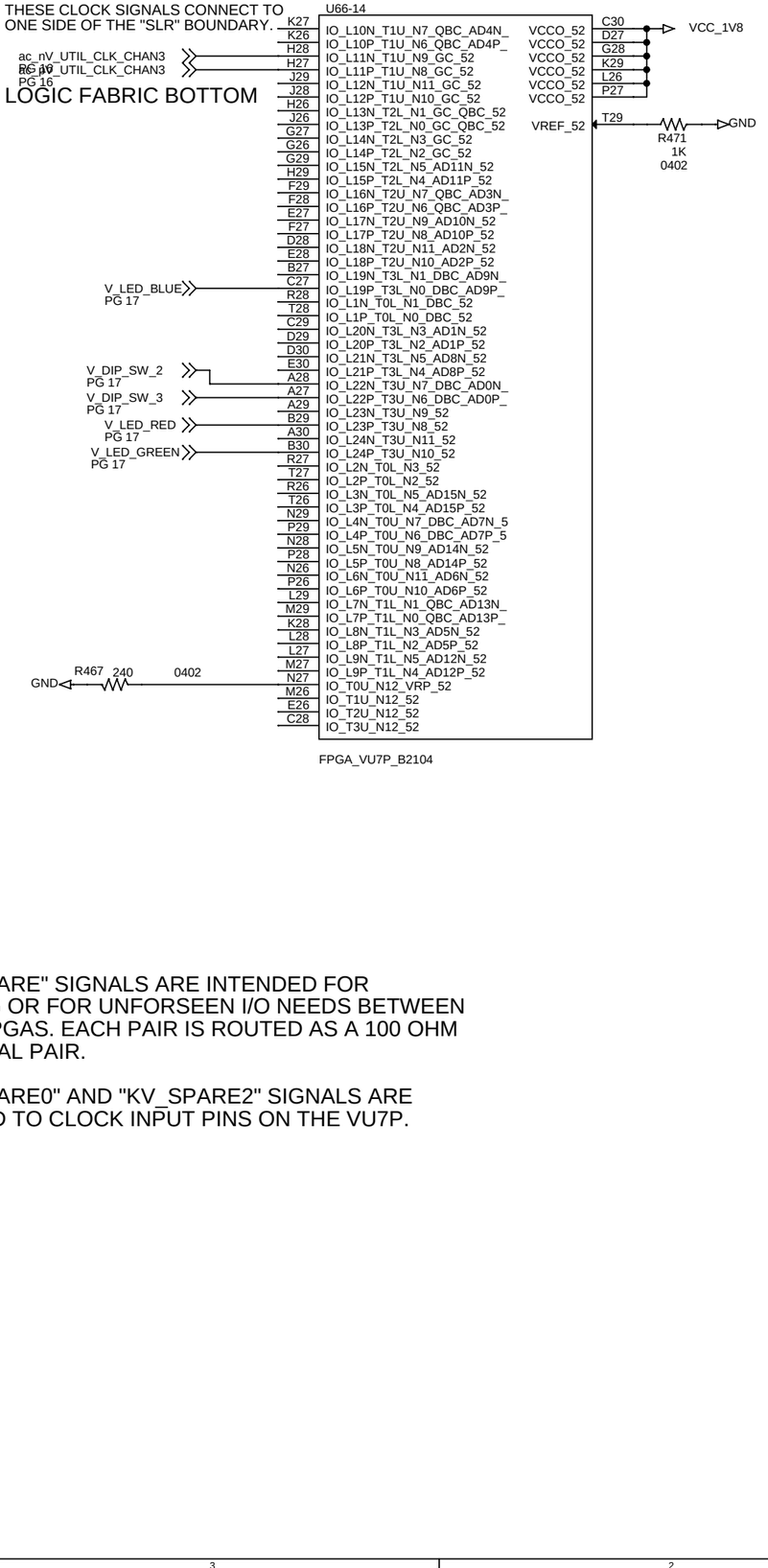
THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

THE TTC_CLK40 PINS ARE NOT ON A "GC" INPUT. MOVE THEM IN A FUTURE REVISION.



THESE CLOCK SIGNALS CONNECT TO ONE SIDE OF THE "SLR" BOUNDARY.

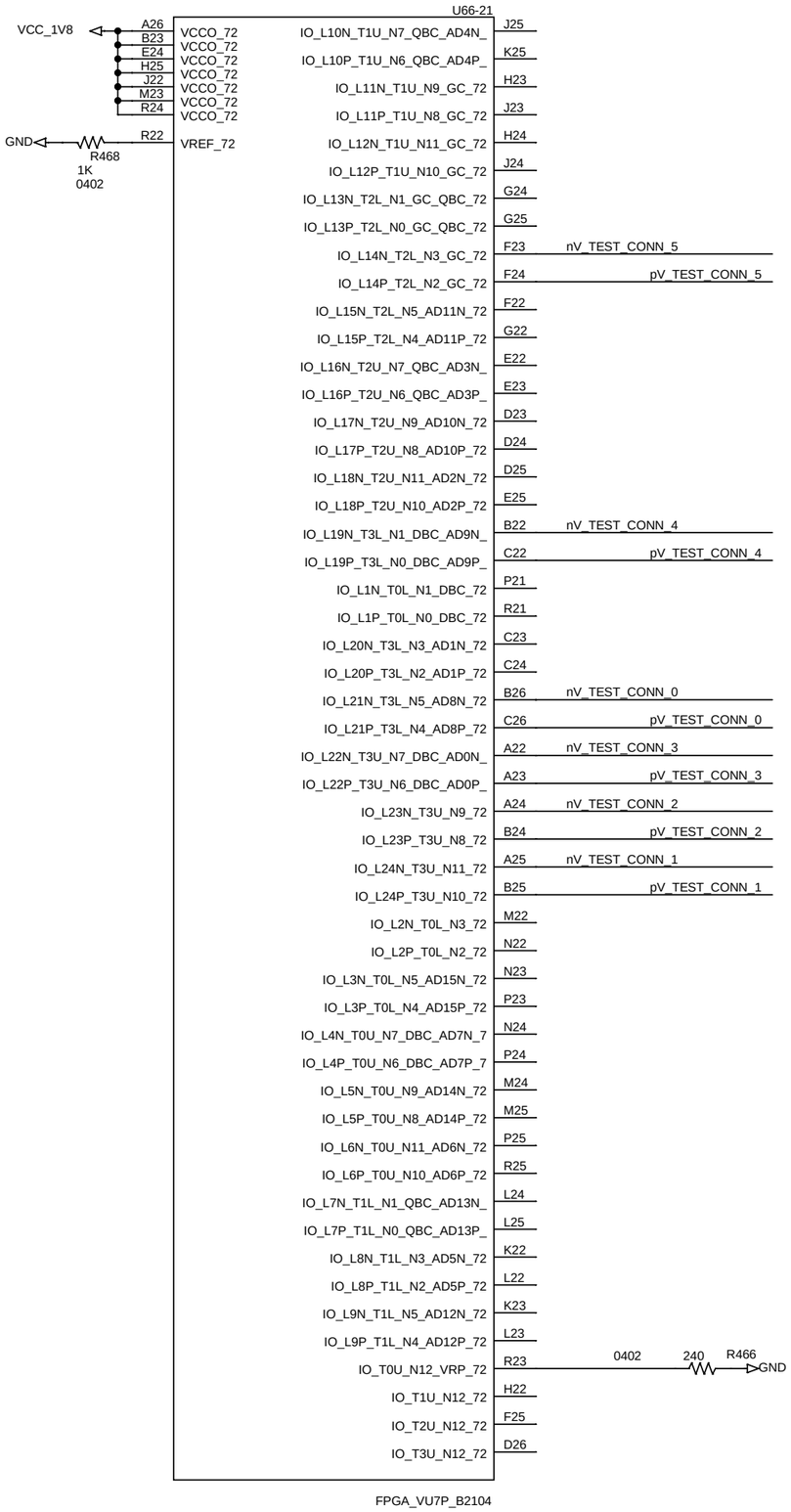
LOGIC FABRIC BOTTOM

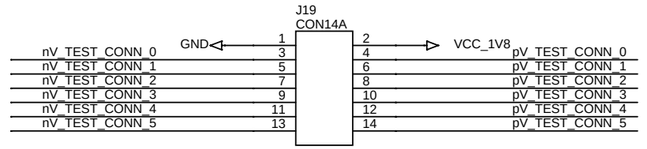


THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "KV_SPARE0" AND "KV_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE VU7P.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.07 VU7P UTILITY BANKS		
Size	Document Number: 6089-103	Rev: A
Date: Friday, August 30, 2019	Sheet 46 of 74	





THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

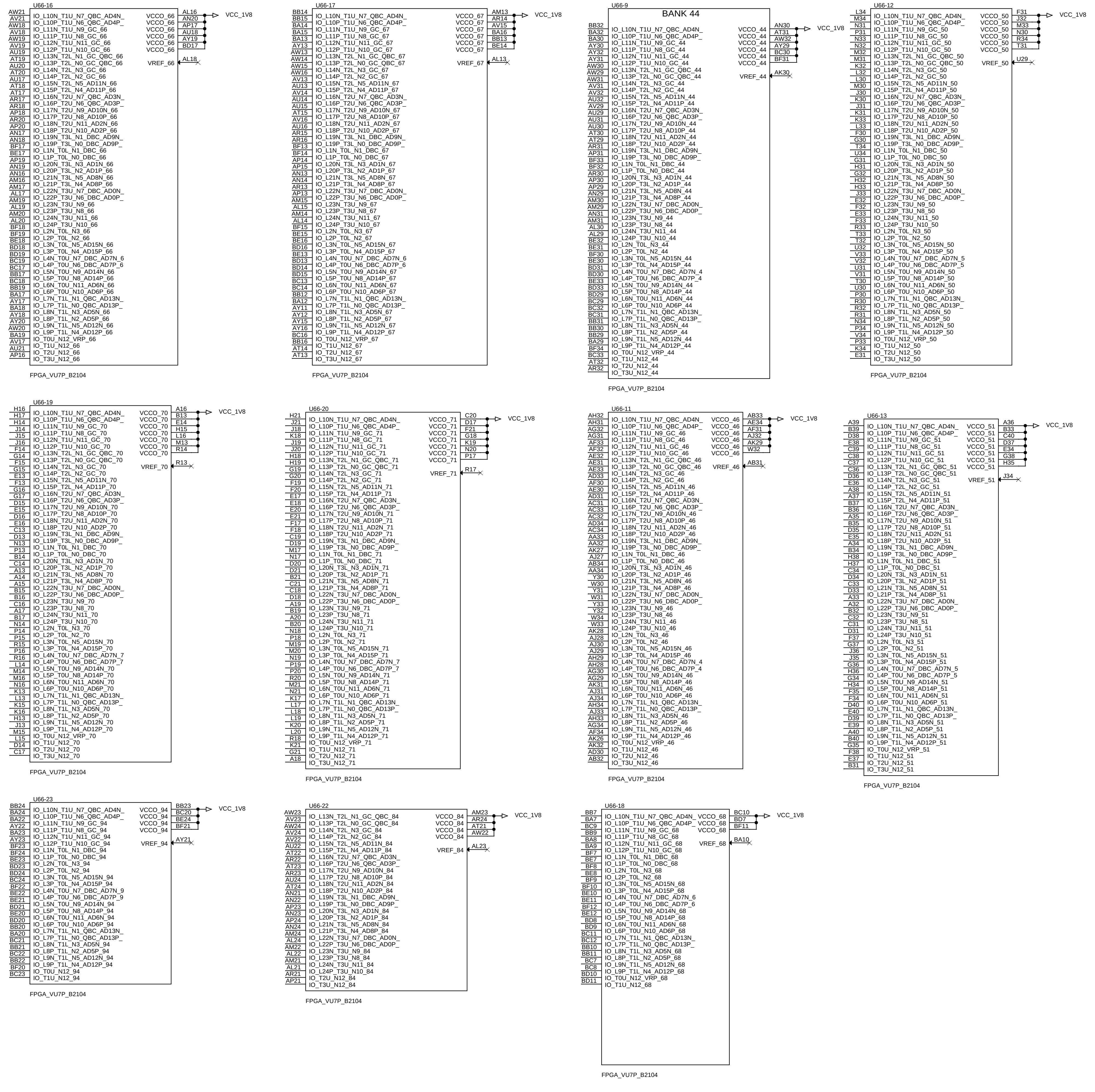
THE "V_TEST_CONN_5" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.08 VU7P TEST CONNECTOR

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 47 of 74



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title

6.99: VU7P UNUSED BLOCKS

Size	Document Number	Rev
	6089-103	A

Date: Tuesday, February 26, 2019 Sheet 48 of 74

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.

U65-33

FPGA_KU15P_A1760

UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.01: KU15P QUAD A UTILITY #1

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 49 of 74

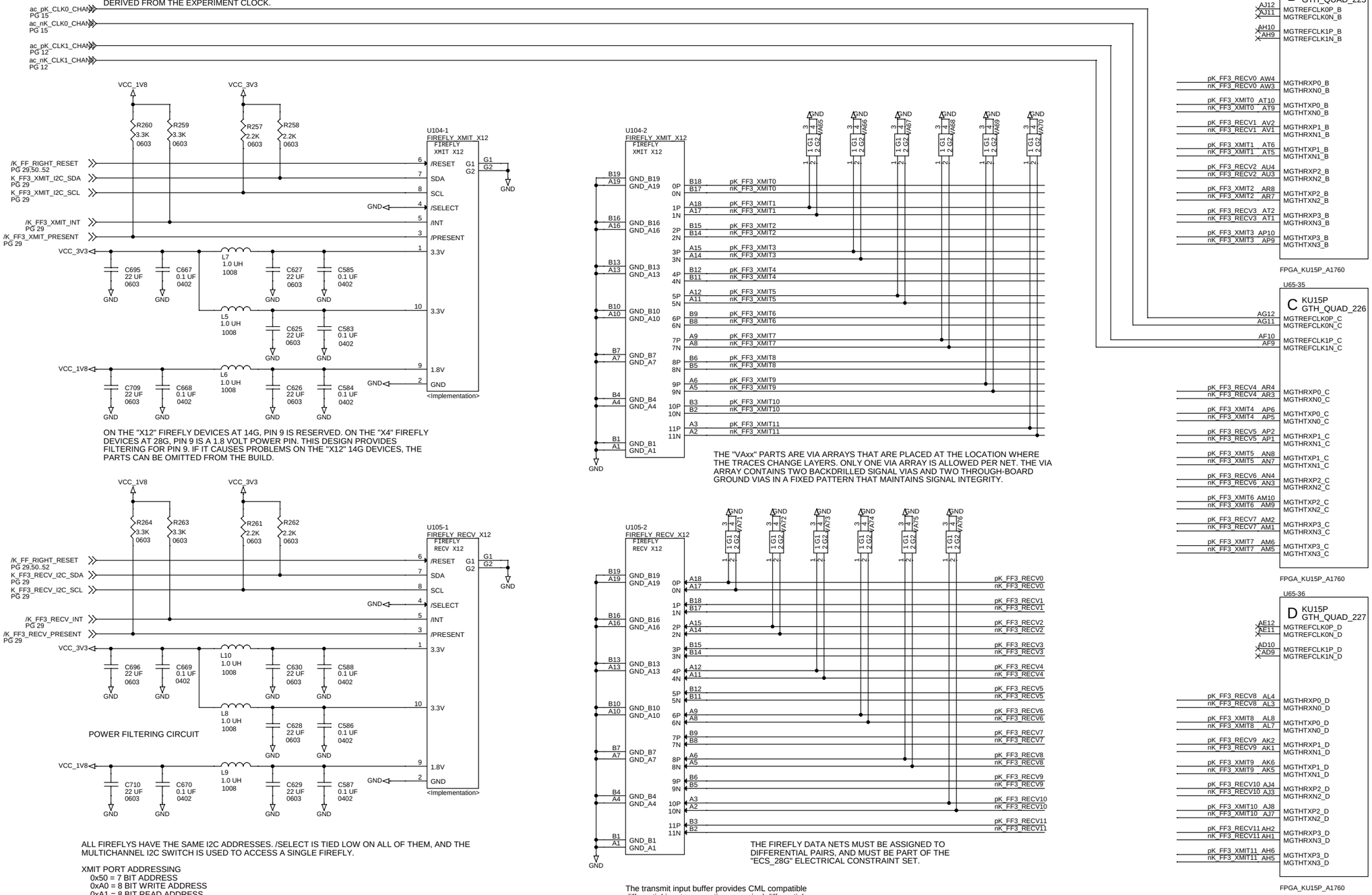
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "B" AND "D" ARE CLOCKED FROM QUAD "C"

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 7.02: KU15P QUADS BCD FIREFLY X12 #3			
Size	Document Number: 6089-103		Rev: A
Date: Tuesday, February 26, 2019	Sheet 50 of 74		

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "E" AND "G" ARE CLOCKED FROM QUAD "F"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN PG 15
ac_nK_CLK0_CHAN PG 15
ac_pK_CLK1_CHAN PG 12
ac_nK_CLK1_CHAN PG 12

U65-37
E KU15P GTH_QUAD_228
AC12 MGTREFCLK0P_E
AC11 MGTREFCLK0N_E
AB10 MGTREFCLK1P_E
AB9 MGTREFCLK1N_E

pK_FF2_RECV0 AG4 MGTHRXP0_E
nK_FF2_RECV0 AG3 MGTHRXN0_E
pK_FF2_XMIT0 AG8 MGTHTXP0_E
nK_FF2_XMIT0 AG7 MGTHTXN0_E
pK_FF2_RECV1 AF2 MGTHRXP1_E
nK_FF2_RECV1 AF1 MGTHRXN1_E
pK_FF2_XMIT1 AF6 MGTHTXP1_E
nK_FF2_XMIT1 AF5 MGTHTXN1_E
pK_FF2_RECV2 AE4 MGTHRXP2_E
nK_FF2_RECV2 AE3 MGTHRXN2_E
pK_FF2_XMIT2 AE8 MGTHTXP2_E
nK_FF2_XMIT2 AE7 MGTHTXN2_E
pK_FF2_RECV3 AD2 MGTHRXP3_E
nK_FF2_RECV3 AD1 MGTHRXN3_E
pK_FF2_XMIT3 AD6 MGTHTXP3_E
nK_FF2_XMIT3 AD5 MGTHTXN3_E

FPGA_KU15P_A1760

U65-38
F KU15P GTH_QUAD_229
AA12 MGTREFCLK0P_F
AA11 MGTREFCLK0N_F
Y10 MGTREFCLK1P_F
Y9 MGTREFCLK1N_F

pK_FF2_RECV4 AC4 MGTHRXP0_F
nK_FF2_RECV4 AC3 MGTHRXN0_F
pK_FF2_XMIT4 AC8 MGTHTXP0_F
nK_FF2_XMIT4 AC7 MGTHTXN0_F
pK_FF2_RECV5 AB2 MGTHRXP1_F
nK_FF2_RECV5 AB1 MGTHRXN1_F
pK_FF2_XMIT5 AB6 MGTHTXP1_F
nK_FF2_XMIT5 AB5 MGTHTXN1_F
pK_FF2_RECV6 AA4 MGTHRXP2_F
nK_FF2_RECV6 AA3 MGTHRXN2_F
pK_FF2_XMIT6 AA8 MGTHTXP2_F
nK_FF2_XMIT6 AA7 MGTHTXN2_F
pK_FF2_RECV7 Y2 MGTHRXP3_F
nK_FF2_RECV7 Y1 MGTHRXN3_F
pK_FF2_XMIT7 Y6 MGTHTXP3_F
nK_FF2_XMIT7 Y5 MGTHTXN3_F

FPGA_KU15P_A1760

U65-39
G KU15P GTH_QUAD_230
W12 MGTREFCLK0P_G
W11 MGTREFCLK0N_G
V10 MGTREFCLK1P_G
V9 MGTREFCLK1N_G

pK_FF2_RECV8 W4 MGTHRXP0_G
nK_FF2_RECV8 W3 MGTHRXN0_G
pK_FF2_XMIT8 W8 MGTHTXP0_G
nK_FF2_XMIT8 W7 MGTHTXN0_G
pK_FF2_RECV9 V2 MGTHRXP1_G
nK_FF2_RECV9 V1 MGTHRXN1_G
pK_FF2_XMIT9 V6 MGTHTXP1_G
nK_FF2_XMIT9 V5 MGTHTXN1_G
pK_FF2_RECV10 U4 MGTHRXP2_G
nK_FF2_RECV10 U3 MGTHRXN2_G
pK_FF2_XMIT10 U8 MGTHTXP2_G
nK_FF2_XMIT10 U7 MGTHTXN2_G
pK_FF2_RECV11 T2 MGTHRXP3_G
nK_FF2_RECV11 T1 MGTHRXN3_G
pK_FF2_XMIT11 T6 MGTHTXP3_G
nK_FF2_XMIT11 T5 MGTHTXN3_G

FPGA_KU15P_A1760

VCC_1V8, VCC_3V3
R268 3.3K 0603, R267 3.3K 0603, R265 2.2K 0603, R266 2.2K 0603

U106-1
FIREFLY_XMIT_X12
FIREFLY XMIT X12

/K_FF_RIGHT_RESET PG 29,50..52
K_FF2_XMIT_I2C_SDA PG 29
K_FF2_XMIT_I2C_SCL PG 29
/K_FF2_XMIT_INT PG 29
/K_FF2_XMIT_PRESENT PG 29

6 /RESET, 7 SDA, 8 SCL, 4 /SELECT, 5 /INT, 3 /PRESENT, G1 G2 GND
1 3.3V, 10 3.3V, 9 1.8V, 2 GND
<implementation>

L13 1.0 UH 1008, L11 1.0 UH 1008, L12 1.0 UH 1008
C697 22 UF 0603, C671 0.1 UF 0402, C633 22 UF 0603, C591 0.1 UF 0402
C631 22 UF 0603, C589 0.1 UF 0402
C711 22 UF 0603, C672 0.1 UF 0402, C632 22 UF 0603, C590 0.1 UF 0402

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U106-2
FIREFLY_XMIT_X12
FIREFLY XMIT X12

GND_B19 A19, GND_A19 A19
GND_B16 B16, GND_A16 A16
GND_B13 B13, GND_A13 A13
GND_B10 B10, GND_A10 A10
GND_B7 B7, GND_A7 A7
GND_B4 B4, GND_A4 A4
GND_B1 B1, GND_A1 A1

0P pK_FF2_XMIT0 B18
0N nK_FF2_XMIT0 B17
1P pK_FF2_XMIT1 A18
1N nK_FF2_XMIT1 A17
2P pK_FF2_XMIT2 B15
2N nK_FF2_XMIT2 B14
3P pK_FF2_XMIT3 A15
3N nK_FF2_XMIT3 A14
4P pK_FF2_XMIT4 B12
4N nK_FF2_XMIT4 B11
5P pK_FF2_XMIT5 A12
5N nK_FF2_XMIT5 A11
6P pK_FF2_XMIT6 B9
6N nK_FF2_XMIT6 B8
7P pK_FF2_XMIT7 A9
7N nK_FF2_XMIT7 A8
8P pK_FF2_XMIT8 B6
8N nK_FF2_XMIT8 B5
9P pK_FF2_XMIT9 A6
9N nK_FF2_XMIT9 A5
10P pK_FF2_XMIT10 B3
10N nK_FF2_XMIT10 B2
11P pK_FF2_XMIT11 A3
11N nK_FF2_XMIT11 A2

GND /A77, GND /A78, GND /A79, GND /A80, GND /A81, GND /A82

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

VCC_1V8, VCC_3V3
R272 3.3K 0603, R271 3.3K 0603, R269 2.2K 0603, R270 2.2K 0603

U107-1
FIREFLY_RECV_X12
FIREFLY RECV X12

/K_FF_RIGHT_RESET PG 29,50..52
K_FF2_RECV_I2C_SDA PG 29
K_FF2_RECV_I2C_SCL PG 29
/K_FF2_RECV_INT PG 29
/K_FF2_RECV_PRESENT PG 29

6 /RESET, 7 SDA, 8 SCL, 4 /SELECT, 5 /INT, 3 /PRESENT, G1 G2 GND
1 3.3V, 10 3.3V, 9 1.8V, 2 GND
<implementation>

L16 1.0 UH 1008, L14 1.0 UH 1008, L15 1.0 UH 1008
C706 22 UF 0603, C673 0.1 UF 0402, C636 22 UF 0603, C594 0.1 UF 0402
C634 22 UF 0603, C592 0.1 UF 0402
C712 22 UF 0603, C674 0.1 UF 0402, C635 22 UF 0603, C593 0.1 UF 0402

POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
0x54 = 7 BIT ADDRESS
0xA8 = 8 BIT WRITE ADDRESS
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

U107-2
FIREFLY_RECV_X12
FIREFLY RECV X12

GND_B19 A19, GND_A19 A19
GND_B16 B16, GND_A16 A16
GND_B13 B13, GND_A13 A13
GND_B10 B10, GND_A10 A10
GND_B7 B7, GND_A7 A7
GND_B4 B4, GND_A4 A4
GND_B1 B1, GND_A1 A1

0P pK_FF2_RECV0 A18
0N nK_FF2_RECV0 A17
1P pK_FF2_RECV1 B18
1N nK_FF2_RECV1 B17
2P pK_FF2_RECV2 A15
2N nK_FF2_RECV2 A14
3P pK_FF2_RECV3 B15
3N nK_FF2_RECV3 B14
4P pK_FF2_RECV4 A12
4N nK_FF2_RECV4 A11
5P pK_FF2_RECV5 B12
5N nK_FF2_RECV5 B11
6P pK_FF2_RECV6 A9
6N nK_FF2_RECV6 A8
7P pK_FF2_RECV7 B9
7N nK_FF2_RECV7 B8
8P pK_FF2_RECV8 A6
8N nK_FF2_RECV8 A5
9P pK_FF2_RECV9 B6
9N nK_FF2_RECV9 B5
10P pK_FF2_RECV10 A3
10N nK_FF2_RECV10 A2
11P pK_FF2_RECV11 B3
11N nK_FF2_RECV11 B2

GND /A83, GND /A84, GND /A85, GND /A86, GND /A87, GND /A88

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.03: KU15P QUADS EFG FIREFLY X12 #2		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 51 of 74	

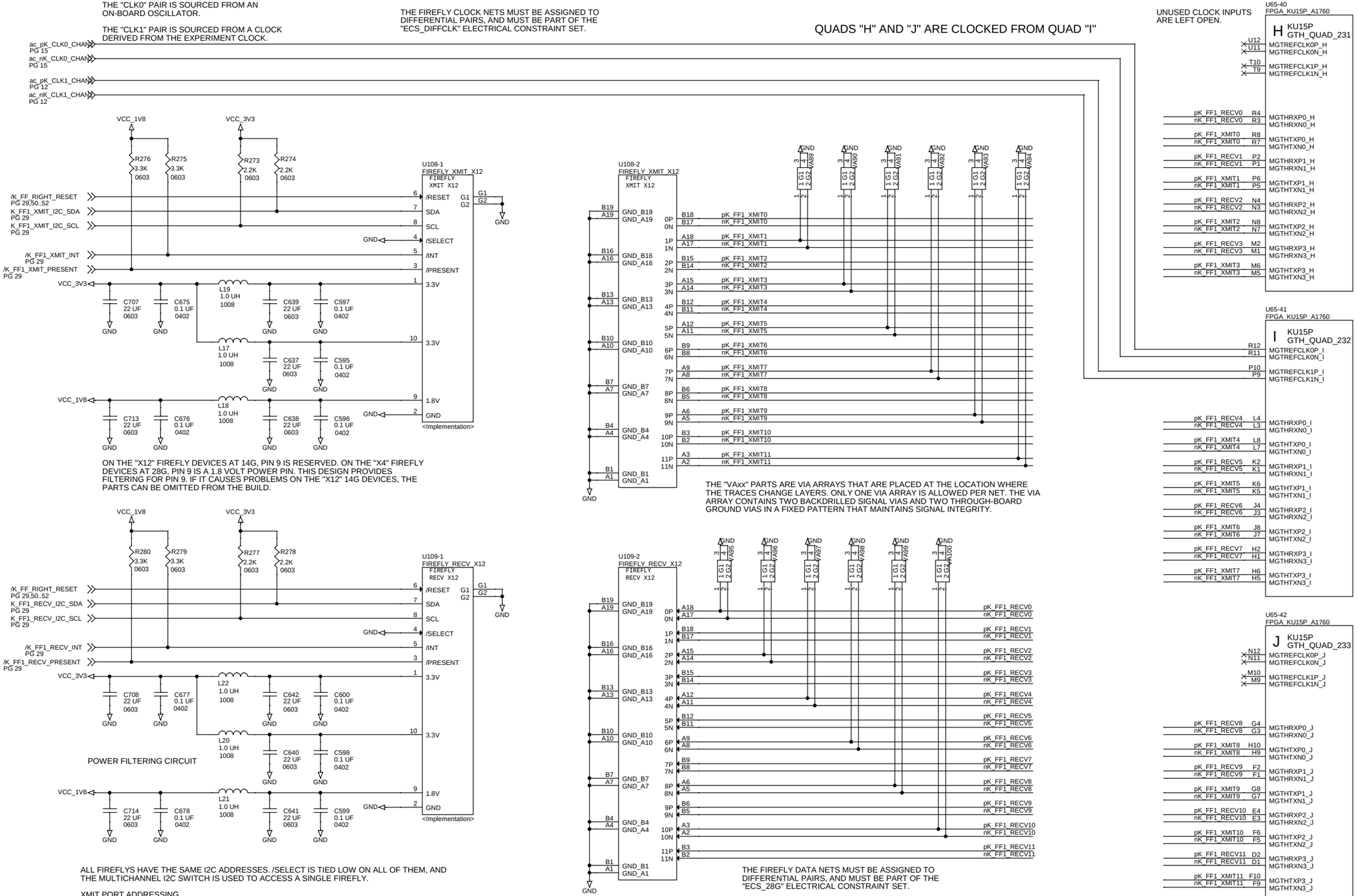
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.04: KU15P QUADS HIJ FIREFLY X12 #1		
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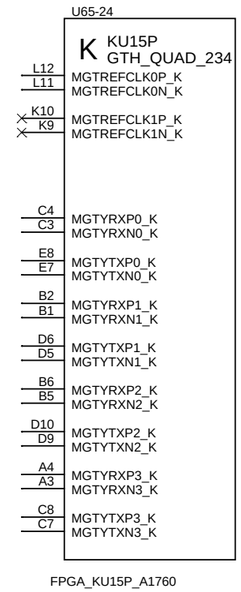
QUAD "K" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.05: KU15P QUAD K UNUSED

Size	Document Number	Rev
	6089-103	A

Date: Tuesday, February 26, 2019 Sheet 53 of 74

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "L" AND "N" ARE CLOCKED FROM QUAD "M"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN4 PG 15
ac_nK_CLK0_CHAN4 PG 15
ac_pK_CLK1_CHAN4 PG 12
ac_nK_CLK1_CHAN4 PG 12

U65-25 L KU15P GTY_QUAD_127

AG30 MGTREFCLK0P_L
AG31 MGTREFCLK0N_L
AE30 MGTREFCLK1P_L
AE31 MGTREFCLK1N_L

pK_FF7_RECV11 AT41 MGTYRXP0_L
nK_FF7_RECV11 AT42 MGTYRXN0_L
pK_FF7_XMIT11 AM36 MGTYTXP0_L
nK_FF7_XMIT11 AM37 MGTYTXN0_L
pK_FF7_RECV10 AR39 MGTYRXP1_L
nK_FF7_RECV10 AR40 MGTYRXN1_L
pK_FF7_XMIT10 AL34 MGTYTXP1_L
nK_FF7_XMIT10 AL35 MGTYTXN1_L
pK_FF7_RECV9 AP41 MGTYRXP2_L
nK_FF7_RECV9 AP42 MGTYRXN2_L
pK_FF7_XMIT9 AK36 MGTYTXP2_L
nK_FF7_XMIT9 AK37 MGTYTXN2_L
pK_FF7_RECV8 AN39 MGTYRXP3_L
nK_FF7_RECV8 AN40 MGTYRXN3_L
pK_FF7_XMIT8 AJ34 MGTYTXP3_L
nK_FF7_XMIT8 AJ35 MGTYTXN3_L

FPGA_KU15P_A1760

U65-26 M KU15P GTY_QUAD_128

AD32 MGTREFCLK0P_M
AD33 MGTREFCLK0N_M
AC30 MGTREFCLK1P_M
AC31 MGTREFCLK1N_M

pK_FF7_RECV7 AM41 MGTYRXP0_M
nK_FF7_RECV7 AM42 MGTYRXN0_M
pK_FF7_XMIT7 AH32 MGTYTXP0_M
nK_FF7_XMIT7 AH33 MGTYTXN0_M
pK_FF7_RECV6 AL39 MGTYRXP1_M
nK_FF7_RECV6 AL40 MGTYRXN1_M
pK_FF7_XMIT6 AH36 MGTYTXP1_M
nK_FF7_XMIT6 AH37 MGTYTXN1_M
pK_FF7_RECV5 AK41 MGTYRXP2_M
nK_FF7_RECV5 AK42 MGTYRXN2_M
pK_FF7_XMIT5 AG34 MGTYTXP2_M
nK_FF7_XMIT5 AG35 MGTYTXN2_M
pK_FF7_RECV4 AJ39 MGTYRXP3_M
nK_FF7_RECV4 AJ40 MGTYRXN3_M
pK_FF7_XMIT4 AF32 MGTYTXP3_M
nK_FF7_XMIT4 AF33 MGTYTXN3_M

FPGA_KU15P_A1760

U65-27 N KU15P GTY_QUAD_129

AB32 MGTREFCLK0P_N
AB33 MGTREFCLK0N_N
AA30 MGTREFCLK1P_N
AA31 MGTREFCLK1N_N

pK_FF7_RECV3 AH41 MGTYRXP0_N
nK_FF7_RECV3 AH42 MGTYRXN0_N
pK_FF7_XMIT3 AF36 MGTYTXP0_N
nK_FF7_XMIT3 AF37 MGTYTXN0_N
pK_FF7_RECV2 AG39 MGTYRXP1_N
nK_FF7_RECV2 AG40 MGTYRXN1_N
pK_FF7_XMIT2 AE34 MGTYTXP1_N
nK_FF7_XMIT2 AE35 MGTYTXN1_N
pK_FF7_RECV1 AF41 MGTYRXP2_N
nK_FF7_RECV1 AF42 MGTYRXN2_N
pK_FF7_XMIT1 AD36 MGTYTXP2_N
nK_FF7_XMIT1 AD37 MGTYTXN2_N
pK_FF7_RECV0 AE39 MGTYRXP3_N
nK_FF7_RECV0 AE40 MGTYRXN3_N
pK_FF7_XMIT0 AC34 MGTYTXP3_N
nK_FF7_XMIT0 AC35 MGTYTXN3_N

FPGA_KU15P_A1760

/K_FF_LEFT_RESET PG 29,54,56..58
K_FF7_XMIT_I2C_SDA PG 29
K_FF7_XMIT_I2C_SCL PG 29
/K_FF7_XMIT_INT PG 29
/K_FF7_XMIT_PRESENT PG 29

VCC_1V8: R601 3.3K 0603, R602 3.3K 0603
VCC_3V3: R604 2.2K 0603, R603 2.2K 0603

U20-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, 1.8V, GND, G1, G2

VCC_3V3: L47 1.0 UH 1008; C847 22 UF 0603; C860 0.1 UF 0402; C884 22 UF 0603; C920 0.1 UF 0402
L49 1.0 UH 1008; C886 22 UF 0603; C922 0.1 UF 0402
VCC_1V8: L48 1.0 UH 1008; C836 22 UF 0603; C859 0.1 UF 0402; C885 22 UF 0603; C921 0.1 UF 0402

<implementation>

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U20-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

pK_FF7_XMIT0 B18 / nK_FF7_XMIT0 B17
pK_FF7_XMIT1 A18 / nK_FF7_XMIT1 A17
pK_FF7_XMIT2 B15 / nK_FF7_XMIT2 B14
pK_FF7_XMIT3 A15 / nK_FF7_XMIT3 A14
pK_FF7_XMIT4 B12 / nK_FF7_XMIT4 B11
pK_FF7_XMIT5 A12 / nK_FF7_XMIT5 A11
pK_FF7_XMIT6 B9 / nK_FF7_XMIT6 B8
pK_FF7_XMIT7 A9 / nK_FF7_XMIT7 A8
pK_FF7_XMIT8 B6 / nK_FF7_XMIT8 B5
pK_FF7_XMIT9 A6 / nK_FF7_XMIT9 A5
pK_FF7_XMIT10 B3 / nK_FF7_XMIT10 B2
pK_FF7_XMIT11 A3 / nK_FF7_XMIT11 A2

GND VA3, GND VA4, GND VA3, GND VA3, GND VA1, GND VA2

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

/K_FF_LEFT_RESET PG 29,54,56..58
K_FF7_RECV_I2C_SDA PG 29
K_FF7_RECV_I2C_SCL PG 29
/K_FF7_RECV_INT PG 29
/K_FF7_RECV_PRESENT PG 29

VCC_1V8: R605 3.3K 0603, R606 3.3K 0603
VCC_3V3: R608 2.2K 0603, R607 2.2K 0603

U21-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/RESET, SDA, SCL, /SELECT, /INT, /PRESENT, 3.3V, 3.3V, 1.8V, GND, G1, G2

VCC_3V3: L50 1.0 UH 1008; C848 22 UF 0603; C862 0.1 UF 0402; C887 22 UF 0603; C923 0.1 UF 0402
L52 1.0 UH 1008; C889 22 UF 0603; C925 0.1 UF 0402
VCC_1V8: L51 1.0 UH 1008; C837 22 UF 0603; C861 0.1 UF 0402; C888 22 UF 0603; C924 0.1 UF 0402

<implementation>

POWER FILTERING CIRCUIT

U21-2 FIREFLY_RECV_X12 FIREFLY RECV X12

pK_FF7_RECV0 A18 / nK_FF7_RECV0 A17
pK_FF7_RECV1 B18 / nK_FF7_RECV1 B17
pK_FF7_RECV2 A15 / nK_FF7_RECV2 A14
pK_FF7_RECV3 B15 / nK_FF7_RECV3 B14
pK_FF7_RECV4 A12 / nK_FF7_RECV4 A11
pK_FF7_RECV5 B12 / nK_FF7_RECV5 B11
pK_FF7_RECV6 A9 / nK_FF7_RECV6 A8
pK_FF7_RECV7 B9 / nK_FF7_RECV7 B8
pK_FF7_RECV8 A6 / nK_FF7_RECV8 A5
pK_FF7_RECV9 B6 / nK_FF7_RECV9 B5
pK_FF7_RECV10 A3 / nK_FF7_RECV10 A2
pK_FF7_RECV11 B3 / nK_FF7_RECV11 B2

GND VA11, GND VA10, GND VA9, GND VA8, GND VA7, GND VA6

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.06: KU15P QUADS LMN FIREFLY X12 #7

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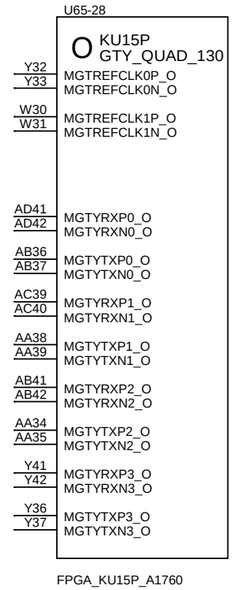
QUAD "O" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.07: KU15P QUAD O UNUSED

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	6089-103	A

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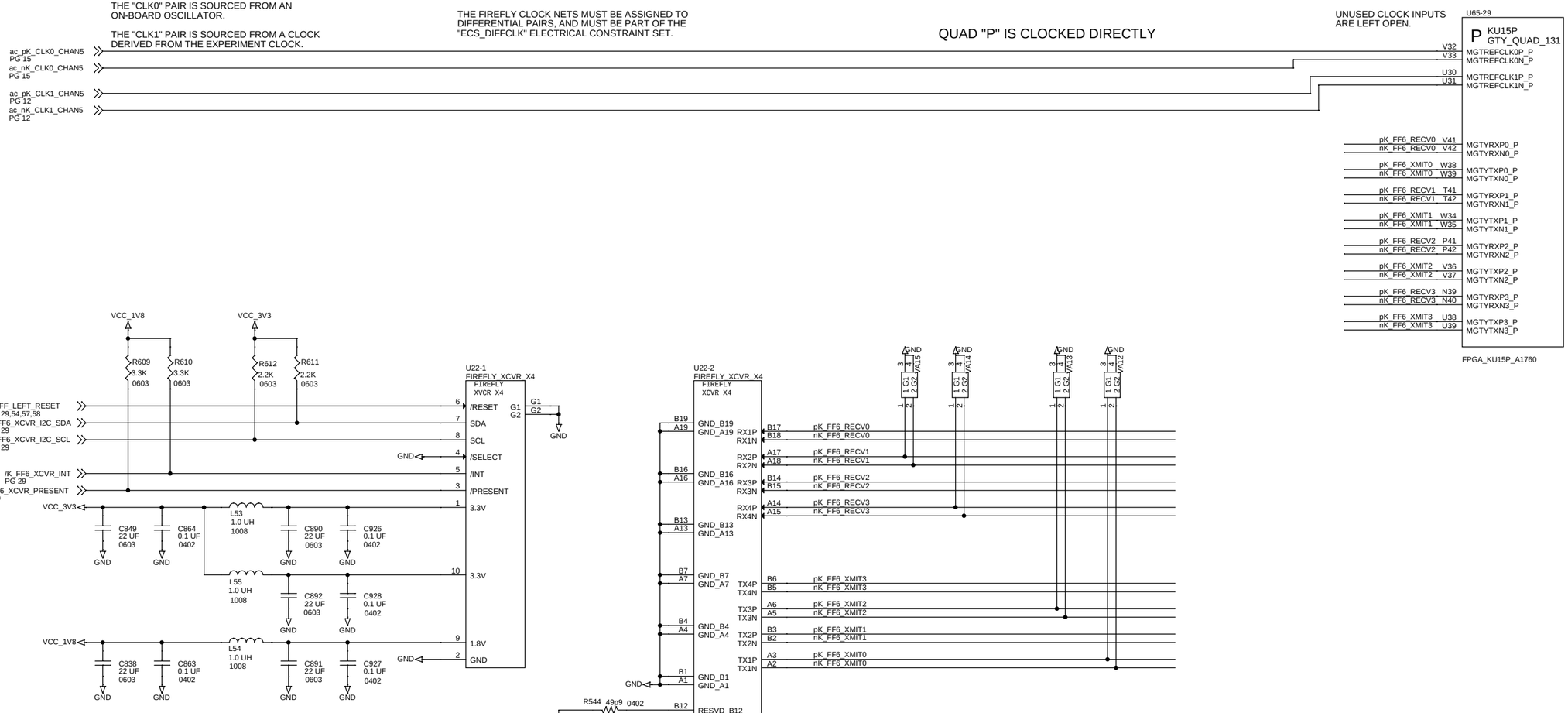
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 7.08: KU15P QUAD P FIREFLY X4 #6			
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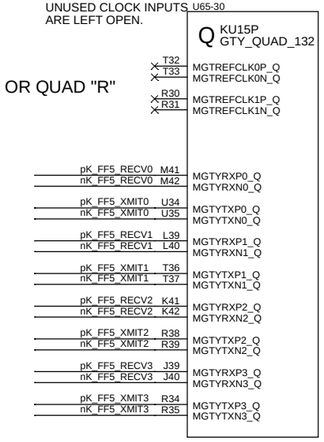
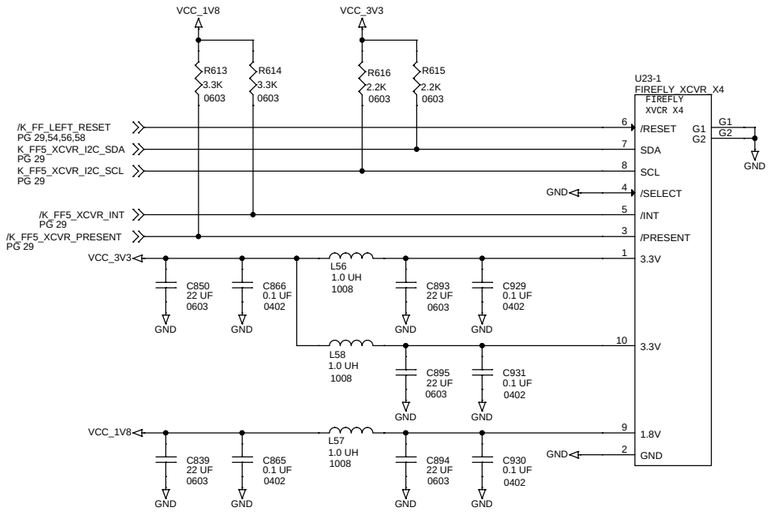
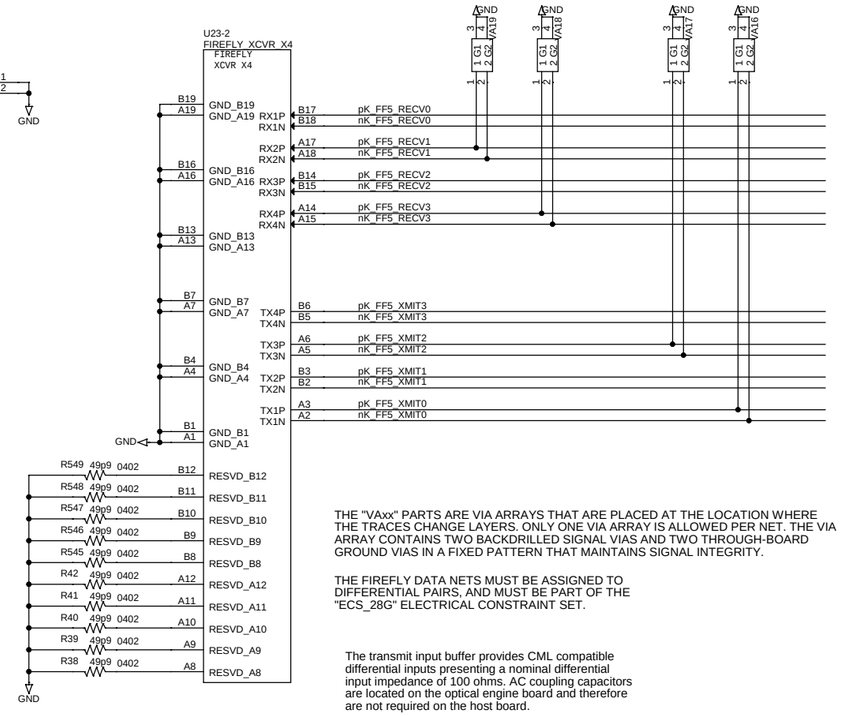
UNUSED CLOCK INPUTS U65-30
ARE LEFT OPEN.

QUAD "Q" CAN BE CLOCKED FROM QUAD "P" OR QUAD "R"



FPGA_KU15P_A1760





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.09: KU15P QUAD R FIREFLY X4 #5

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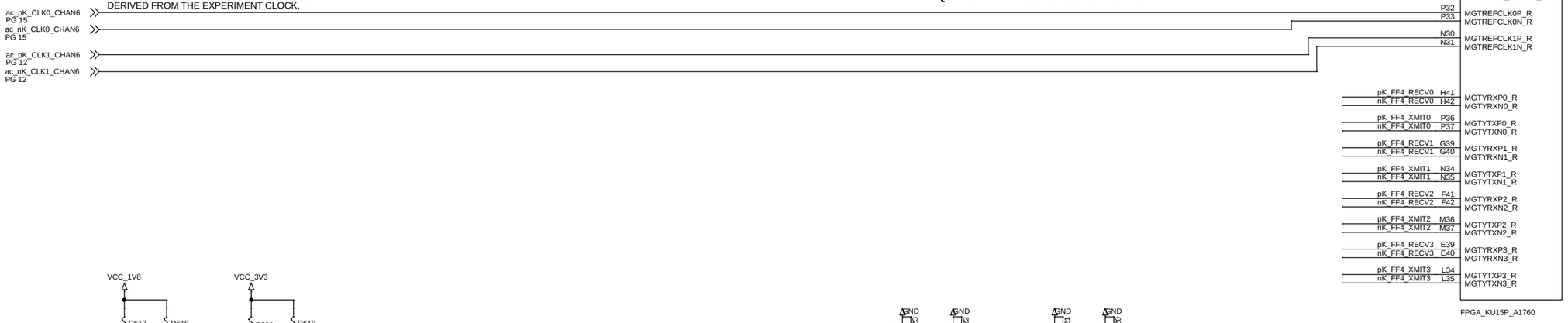
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

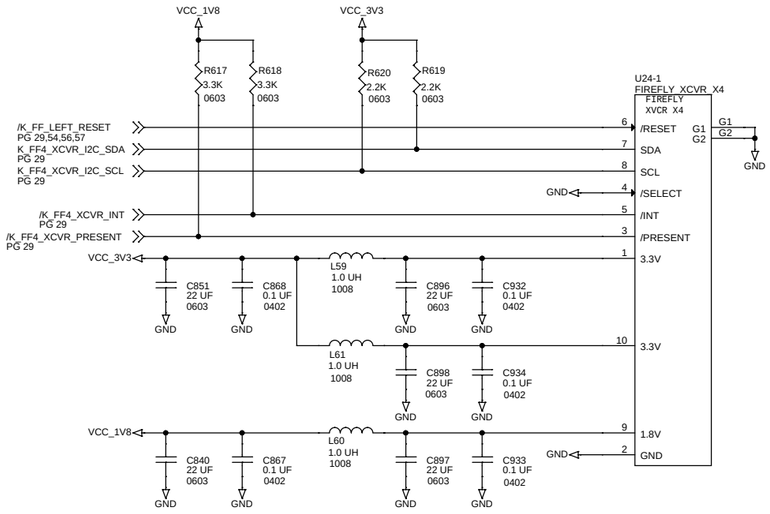
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

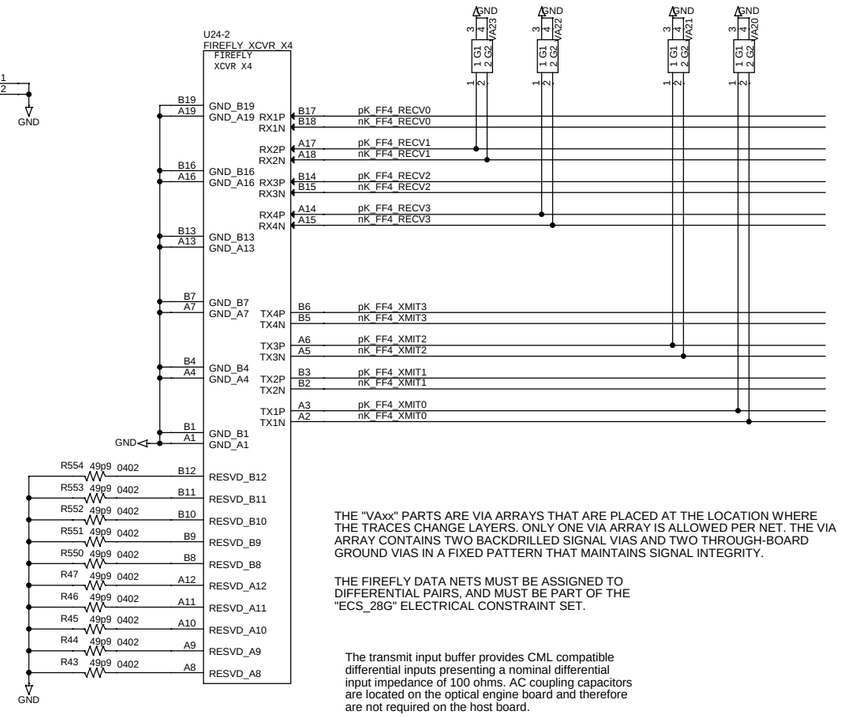
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "R" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.10: KU15P QUAD R FIREFLY X4 #4		
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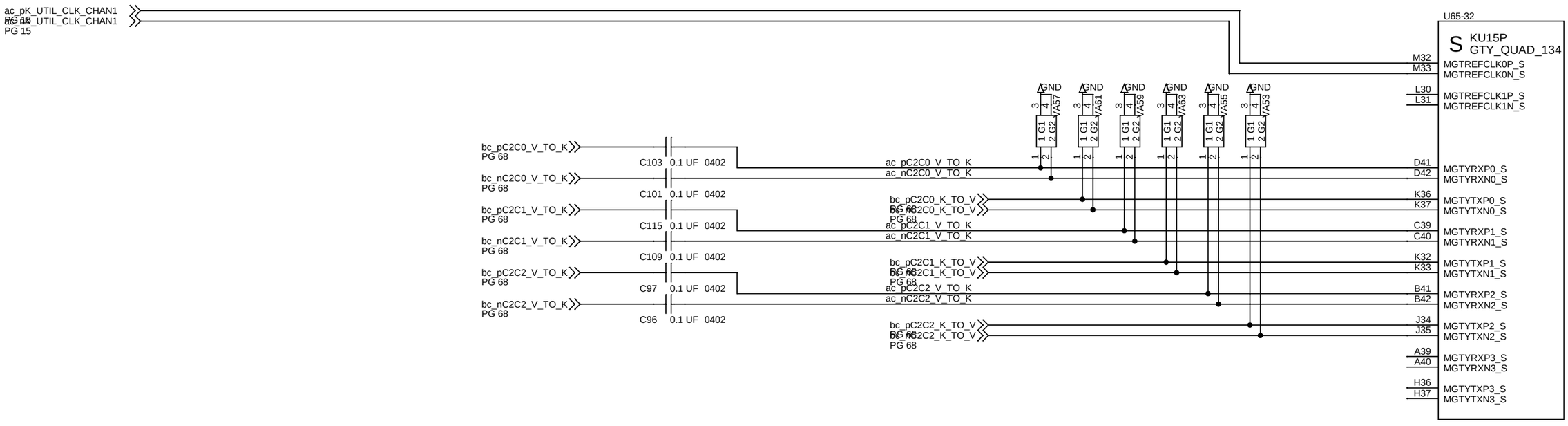
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "S" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

CONNECT UTILITY NETS HERE

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.11: KU15P QUAD S CHIP-TO-CHIP

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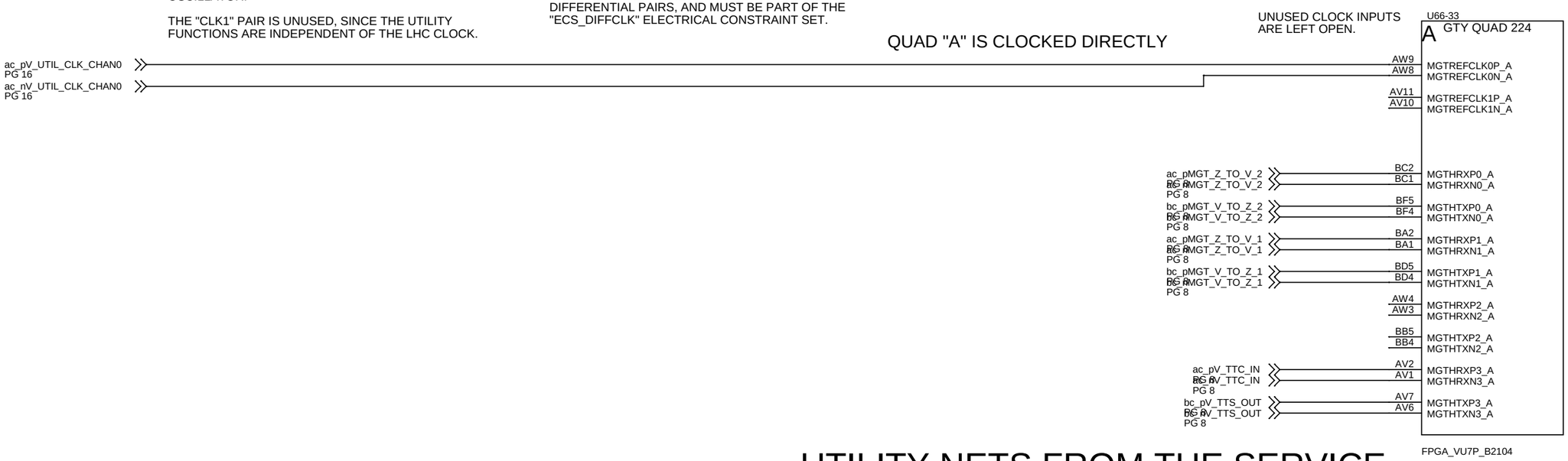
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.01: VU7P QUAD A UTILITY #1		
Size	Document Number: 6089-103	Rev: A
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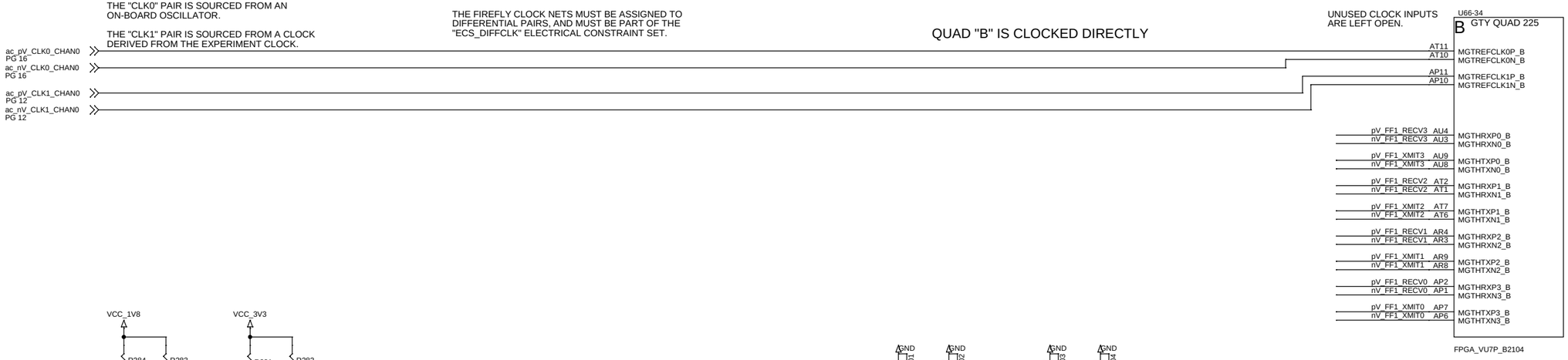
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

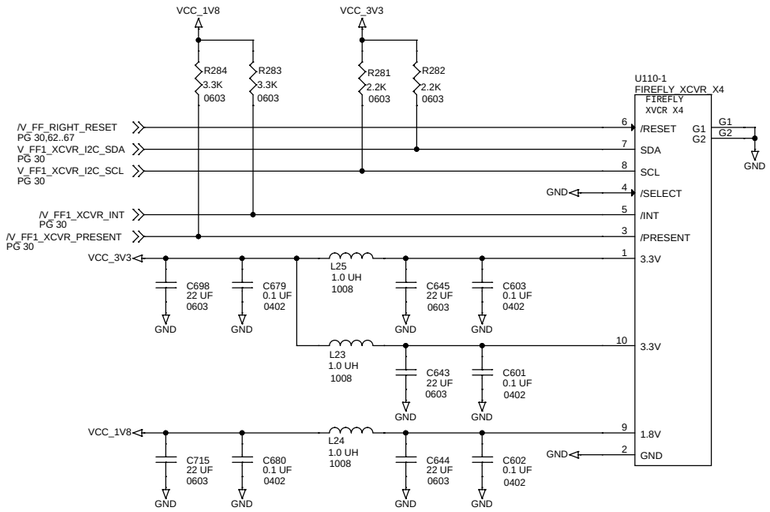
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

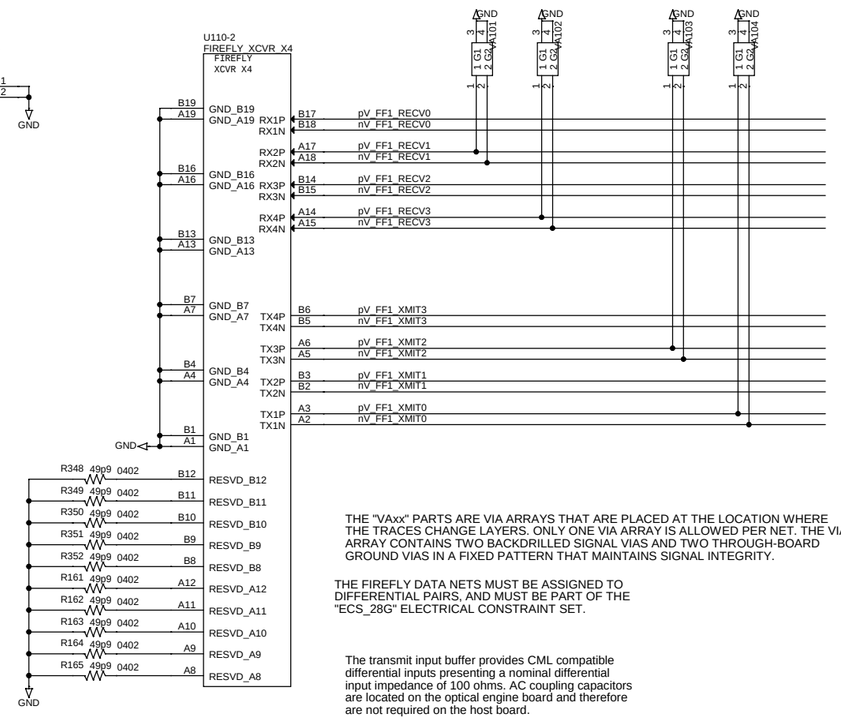
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "B" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.02: VU7P QUAD B FIREFLY X4 #1

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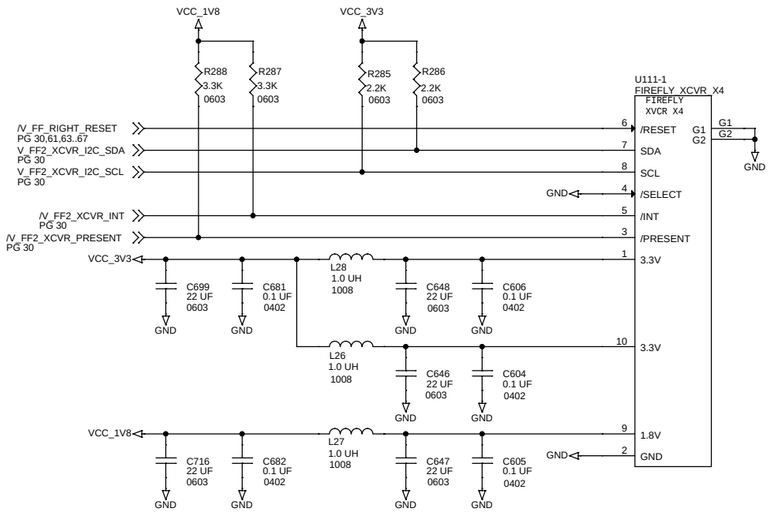
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

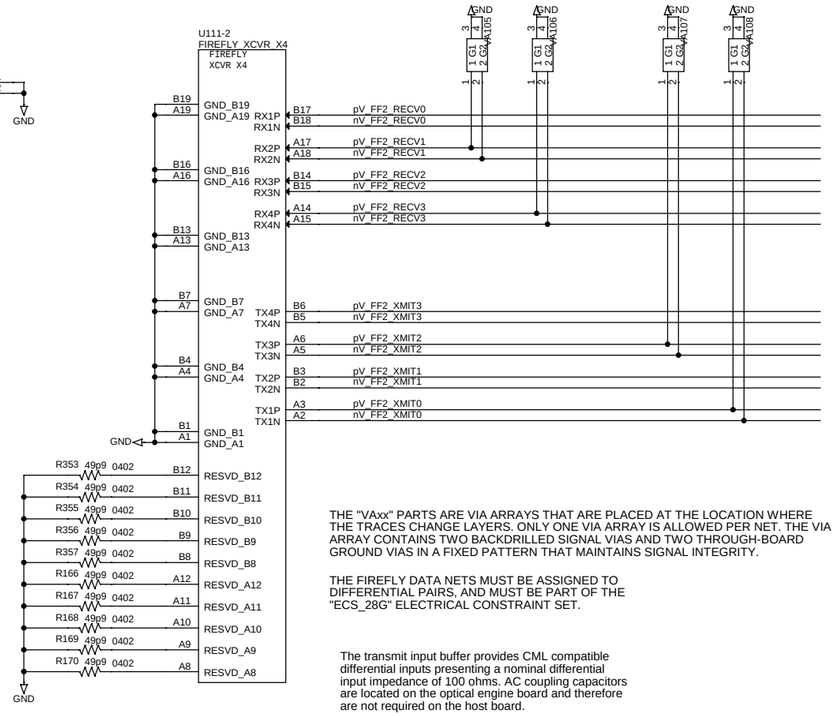
U66-35_FPGA_VU7P_B2104
GTY QUAD 226

AM11
AM10
MGTREFCLK0P_C
MGTREFCLK0N_C
AK11
AK10
MGTREFCLK1P_C
MGTREFCLK1N_C

QUAD "C" IS CLOCKED FROM EITHER QUAD "B" OR "D"

pV_FF2_RECV3 AN4
nV_FF2_RECV3 AN3
MGTHRXP0_C
MGTHRXN0_C
pV_FF2_XMIT3 AN9
nV_FF2_XMIT3 AN8
MGTHTXP0_C
MGTHTXN0_C
pV_FF2_RECV2 AM2
nV_FF2_RECV2 AM1
MGTHRXP1_C
MGTHRXN1_C
pV_FF2_XMIT2 AM7
nV_FF2_XMIT2 AM6
MGTHTXP1_C
MGTHTXN1_C
pV_FF2_RECV1 AL4
nV_FF2_RECV1 AL3
MGTHRXP2_C
MGTHRXN2_C
pV_FF2_XMIT1 AL9
nV_FF2_XMIT1 AL8
MGTHTXP2_C
MGTHTXN2_C
pV_FF2_RECV0 AK2
nV_FF2_RECV0 AK1
MGTHRXP3_C
MGTHRXN3_C
pV_FF2_XMIT0 AK7
nV_FF2_XMIT0 AK6
MGTHTXP3_C
MGTHTXN3_C





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.03: VU7P QUAD C FIREFLY X4 #2

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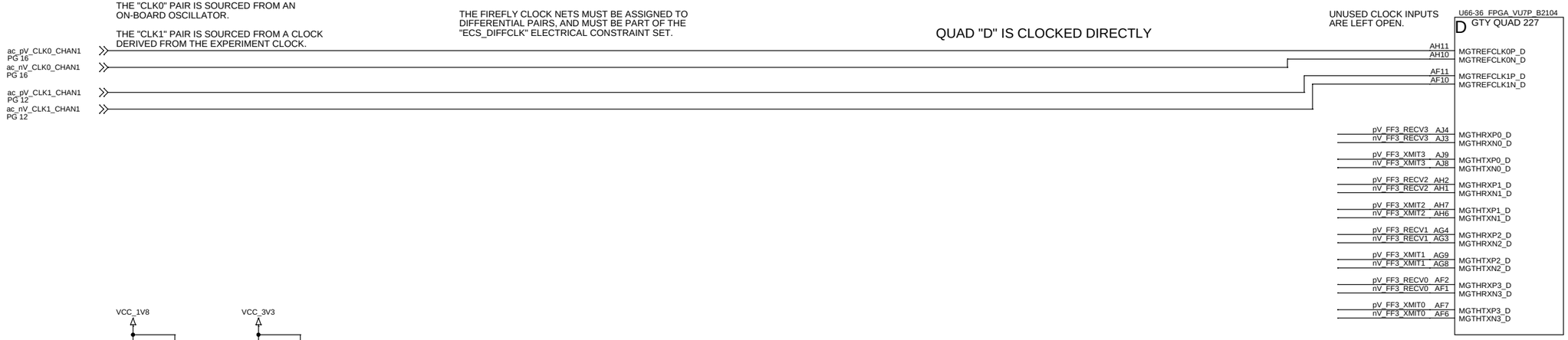
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

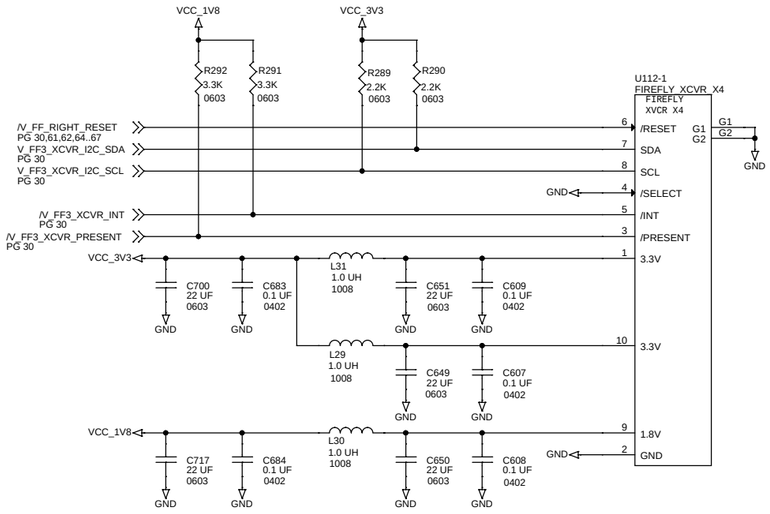
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

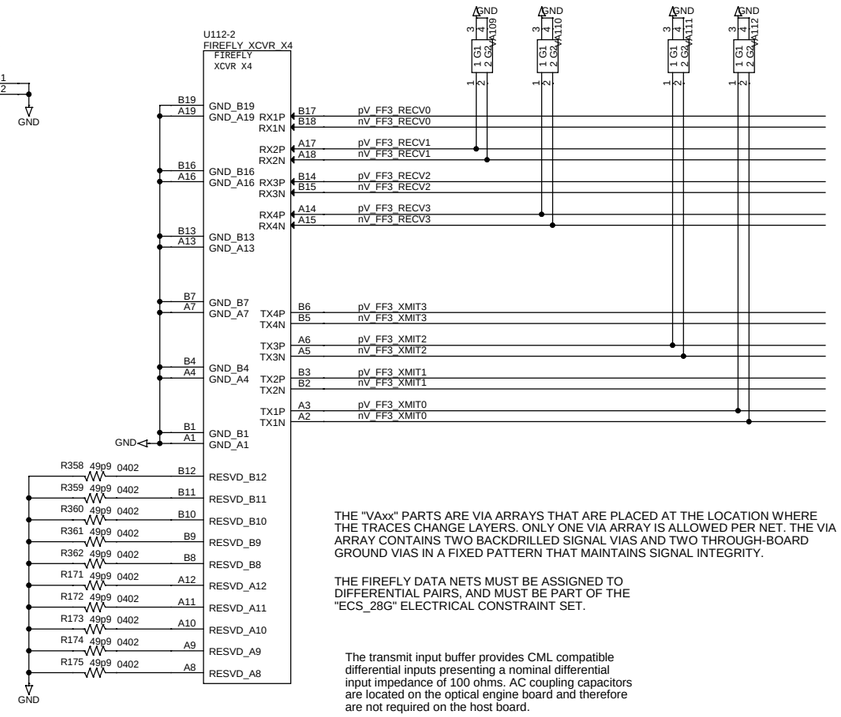
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "D" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.04: VU7P QUAD D FIREFLY X4 #3		
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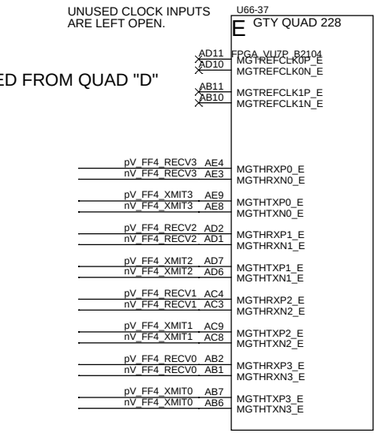
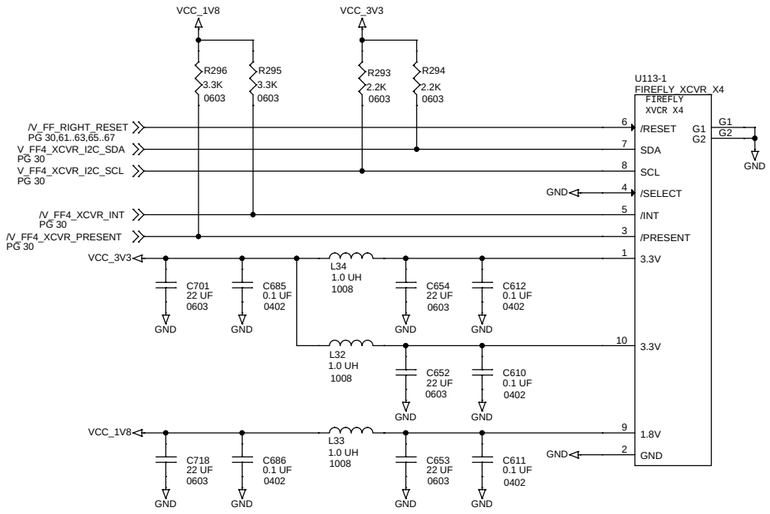
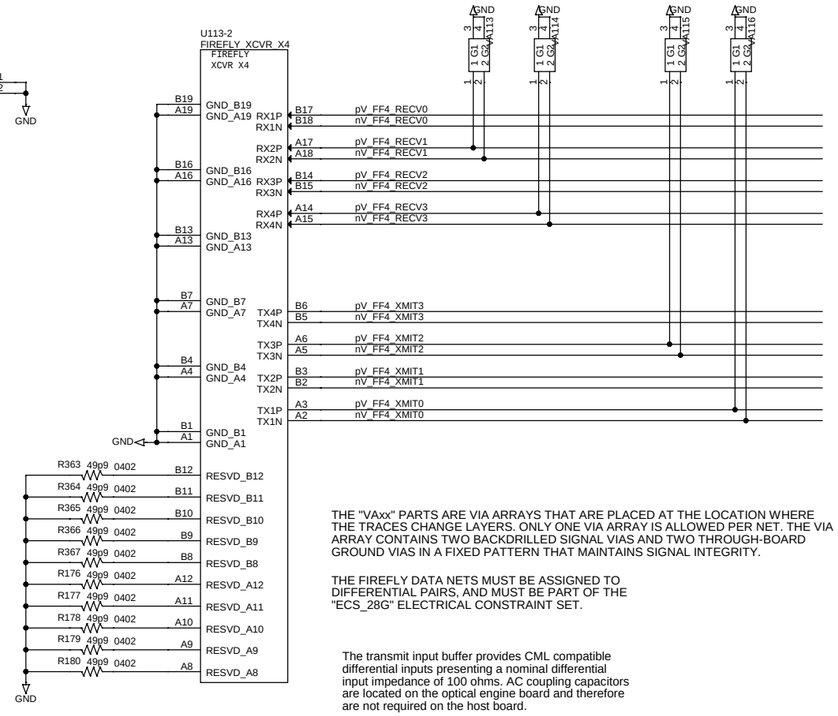
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "E" IS CLOCKED FROM QUAD "D"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.05: VU7P QUAD E FIREFLY X4 #4		
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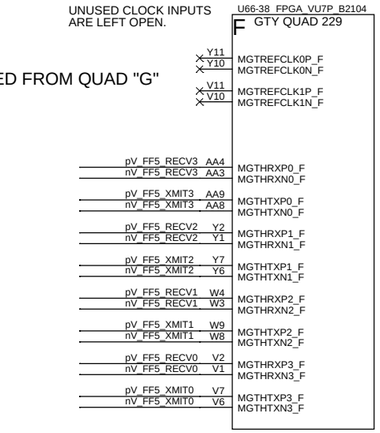
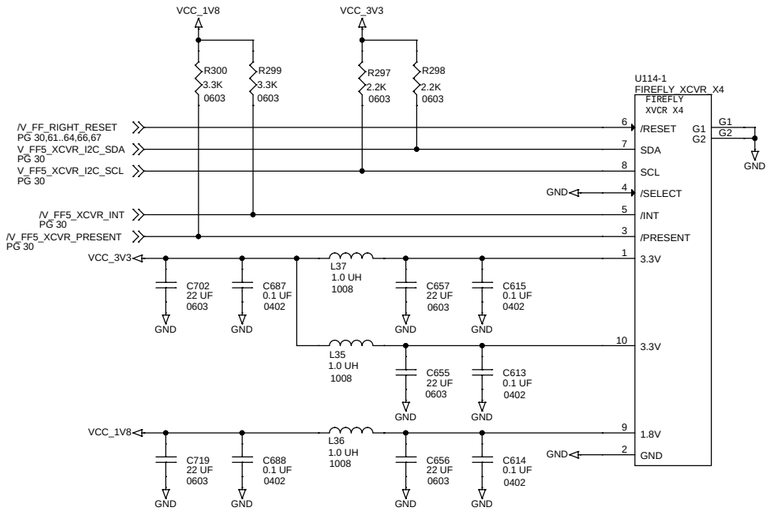
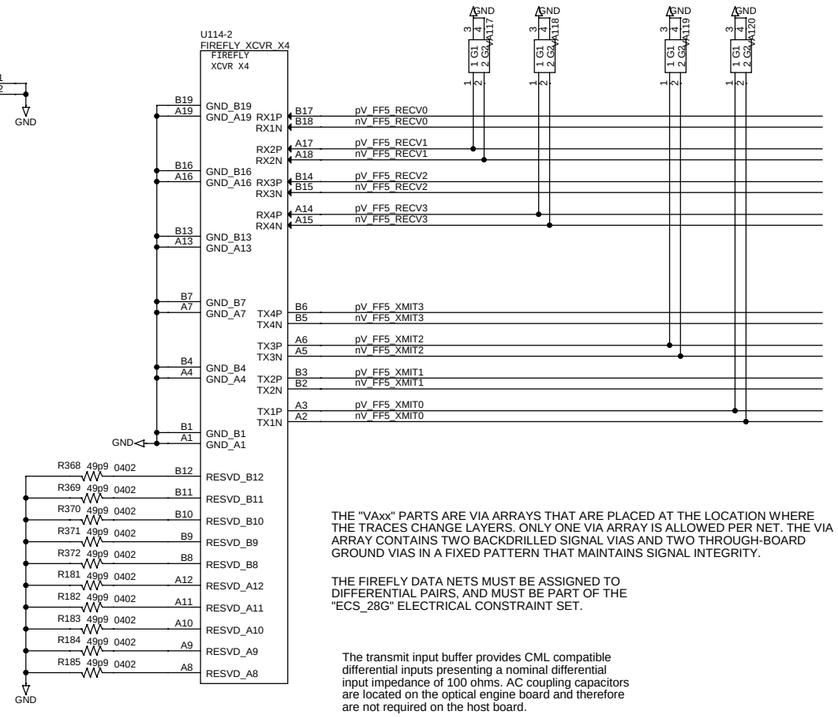
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "F" IS CLOCKED FROM QUAD "G"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.06: VU7P QUAD F FIREFLY X4 #5		
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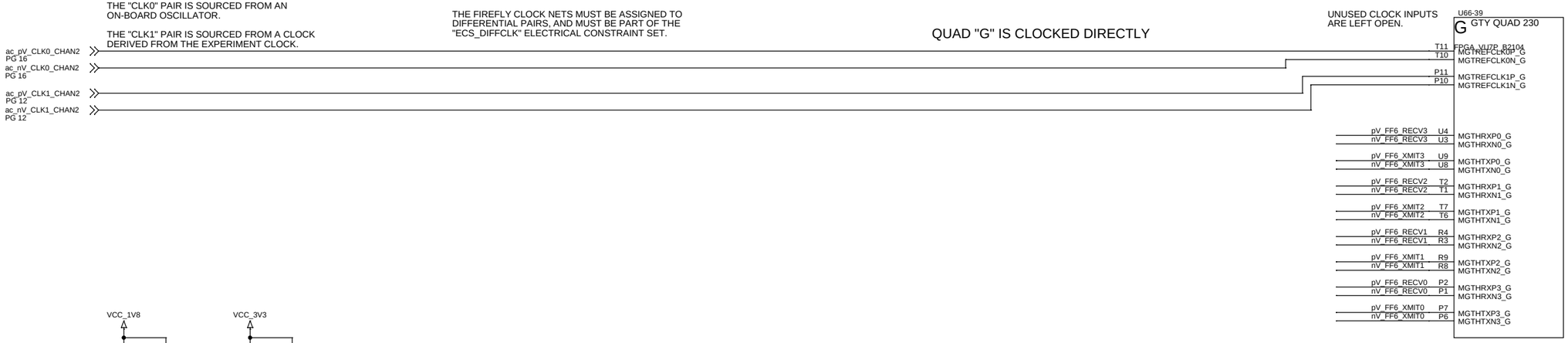
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

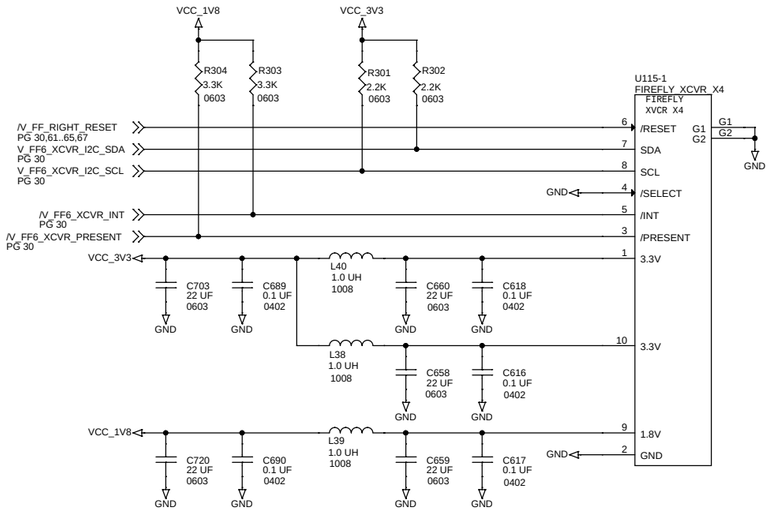
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

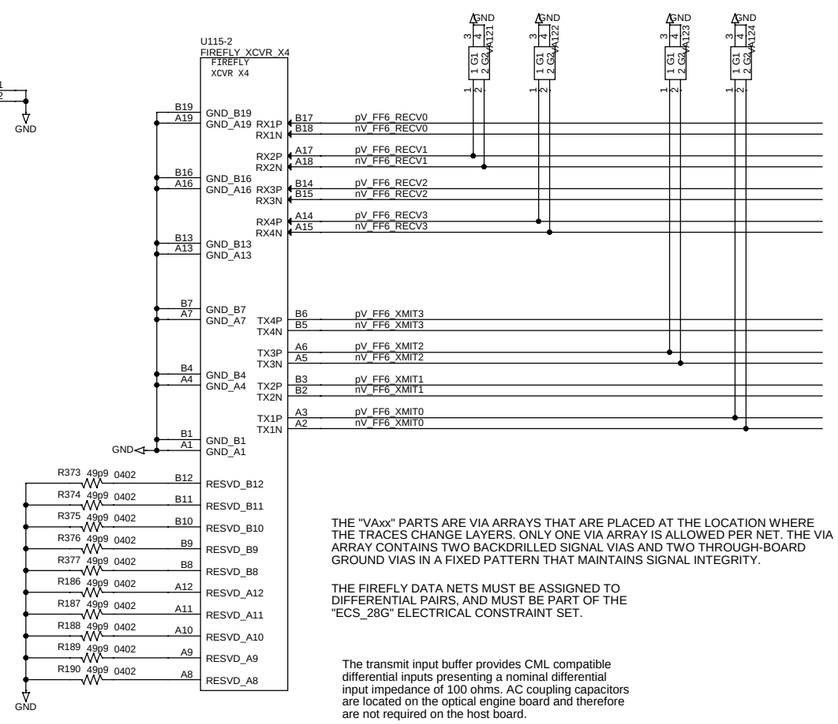
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "G" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.07: VU7P QUAD G FIREFLY X4 #6		
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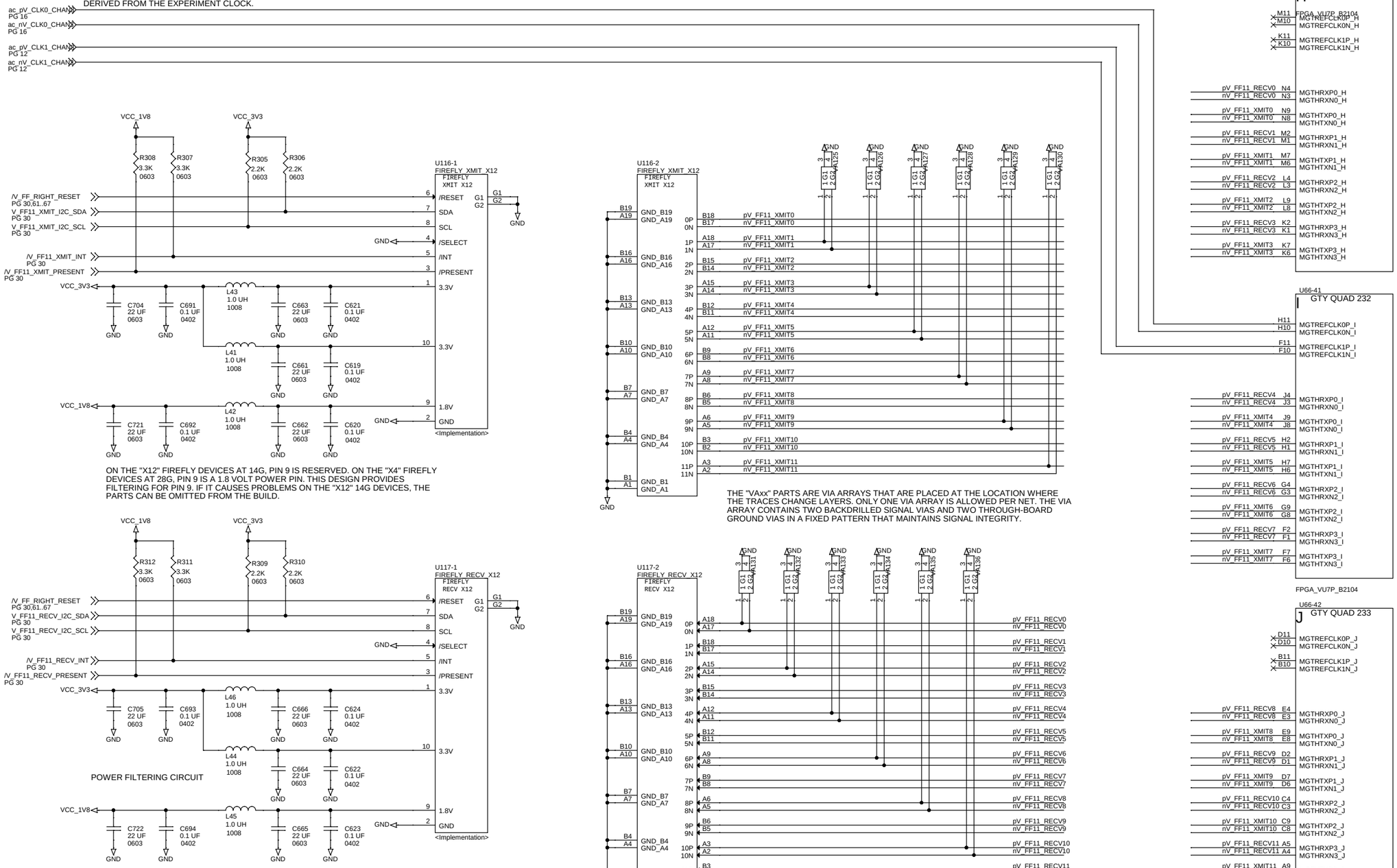
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

POWER FILTERING CIRCUIT

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

Title	ATCA FPGA BOARD, KU15P AND VU7P, MK1
	8.08: VU7P QUADS HIJ FIREFLY X12 #11
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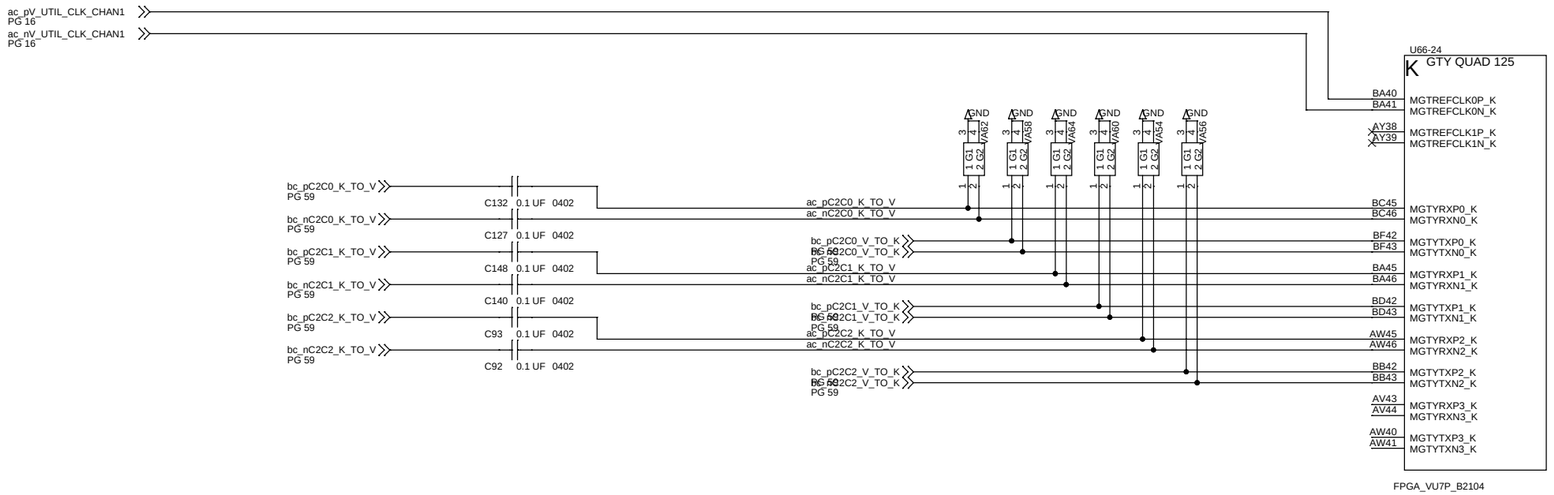
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

QUAD "K" IS CLOCKED DIRECTLY



THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.09: VU7P QUAD K CHIP TO CHIP		
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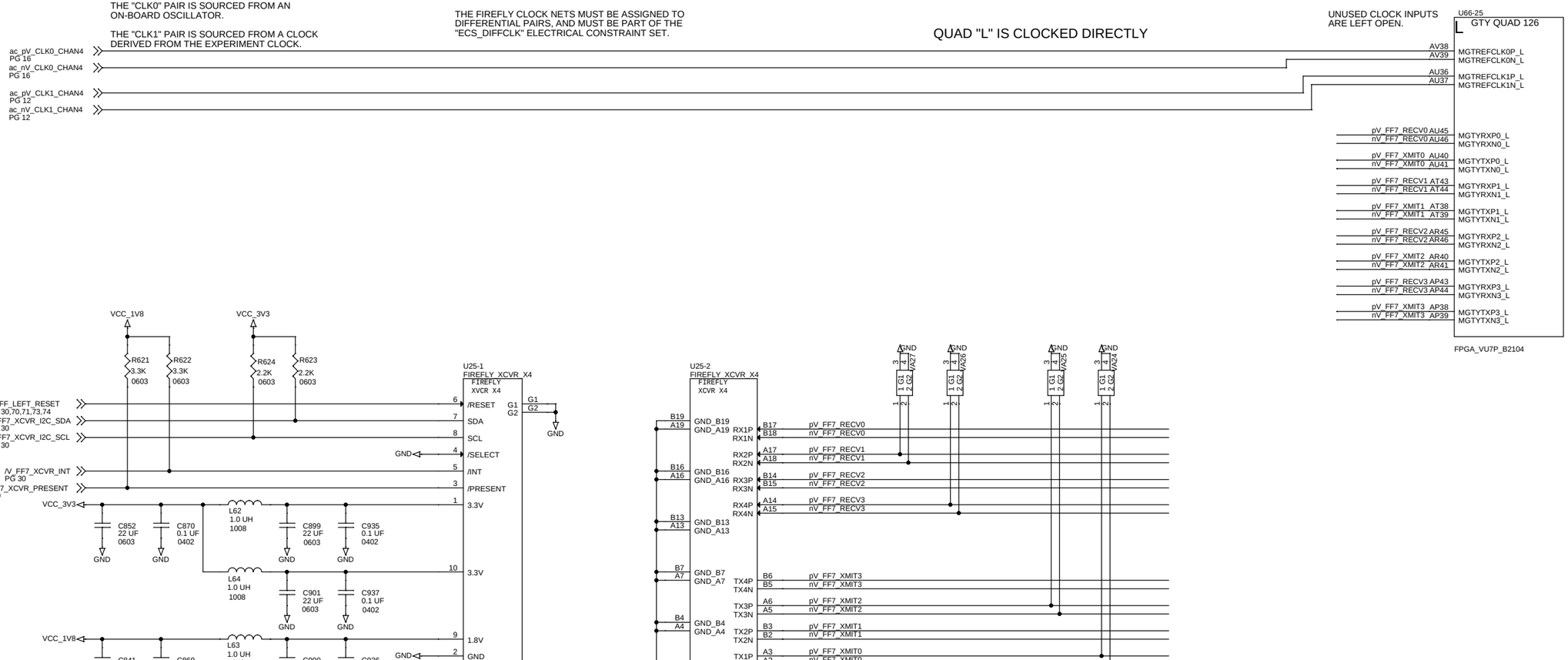
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "L" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.10: VU7P QUAD L FIREFLY X4 #7

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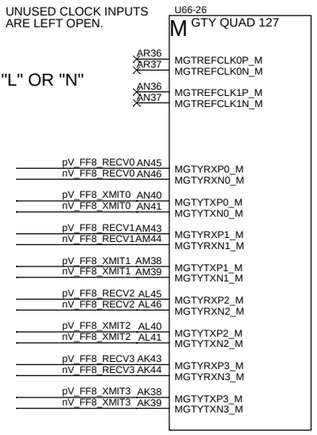
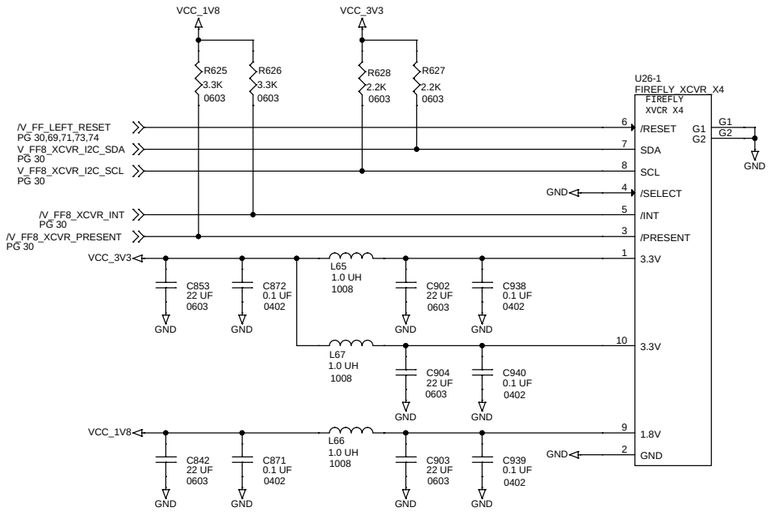
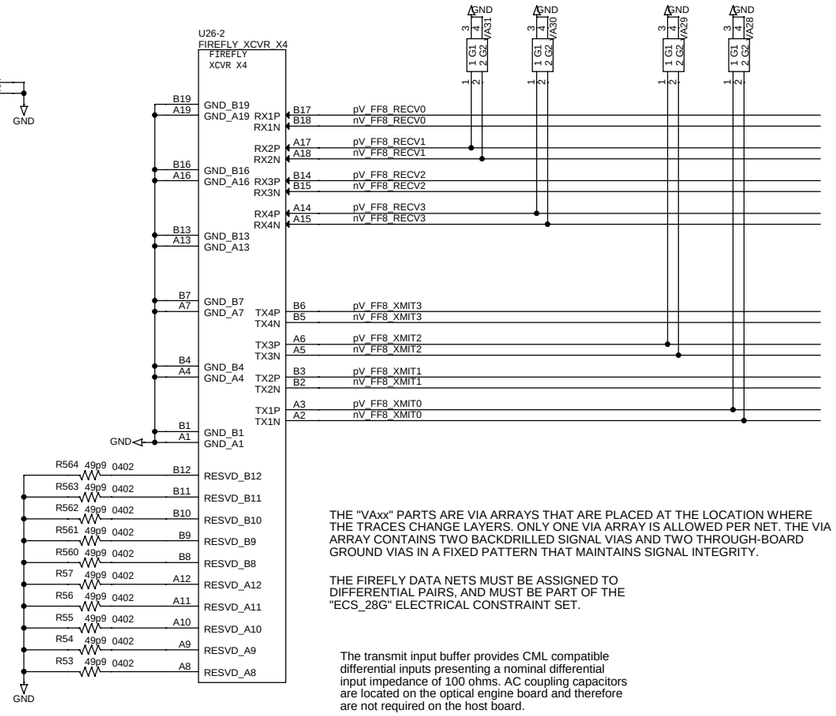
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "M" IS CLOCKED FROM EITHER QUAD "L" OR "N"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.11: VU7P QUAD M FIREFLY X4 #8		
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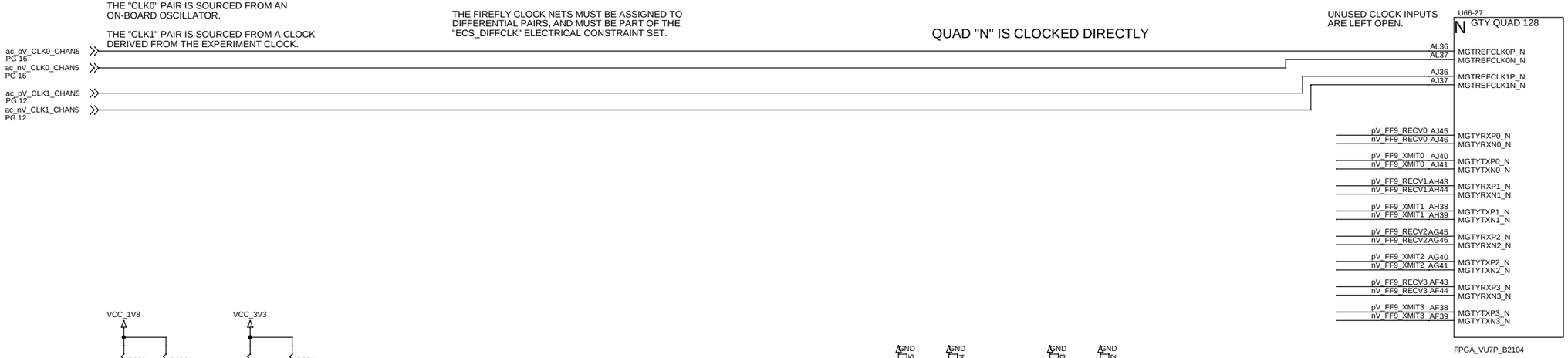
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

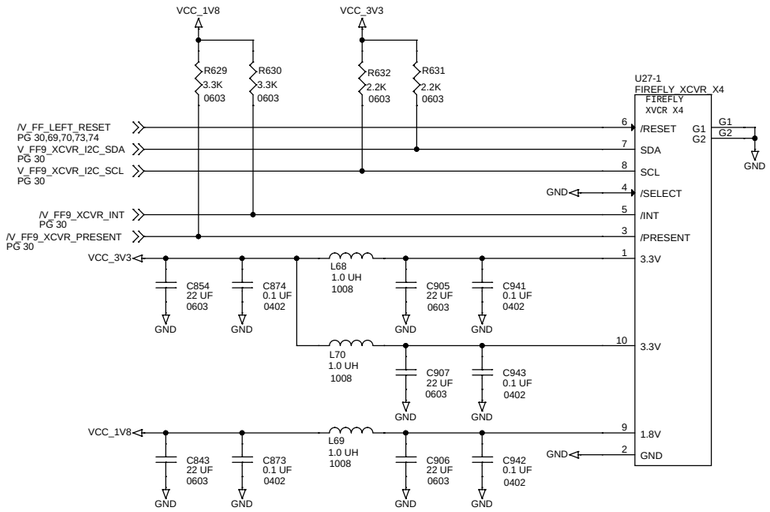
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

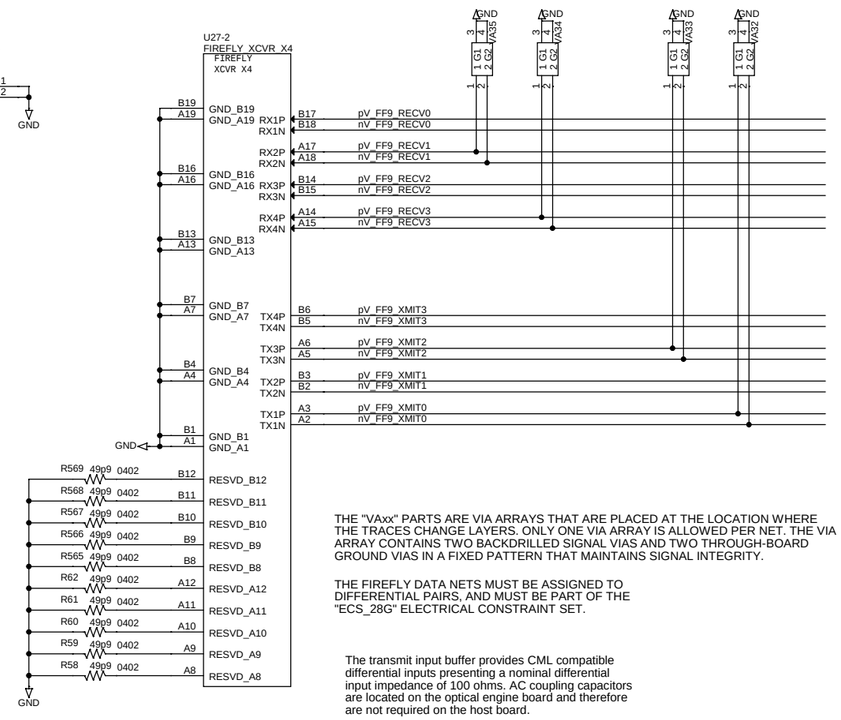
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "N" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.12: VU7P QUAD N FIREFLY X4 #9		
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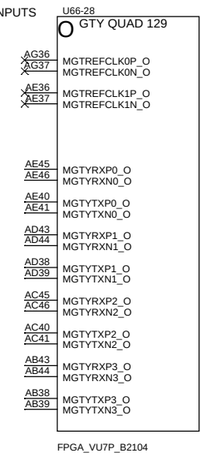
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "O" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.13: VU7P QUAD O UNUSED

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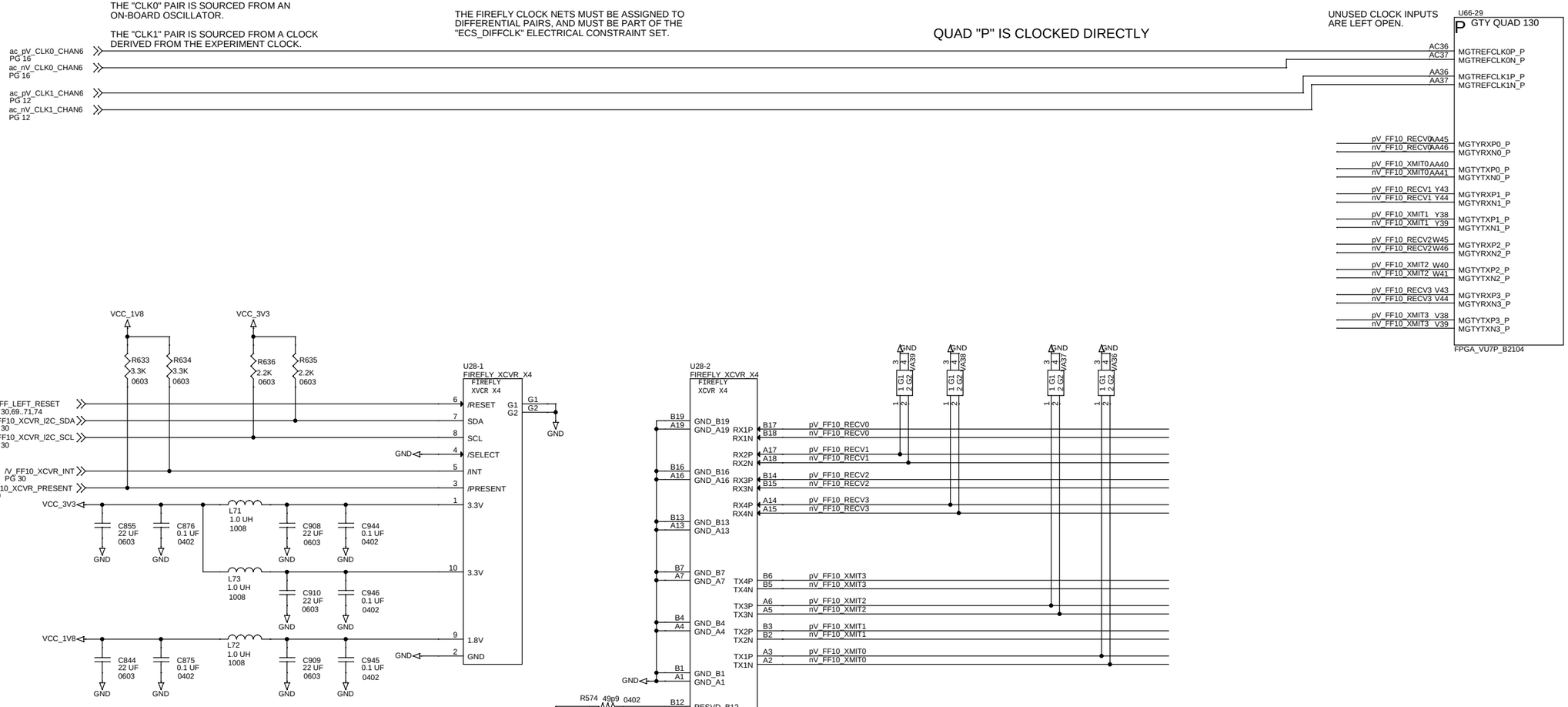
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.14: VU7P QUAD P FIREFLY X4 #10		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 73 of 74	

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

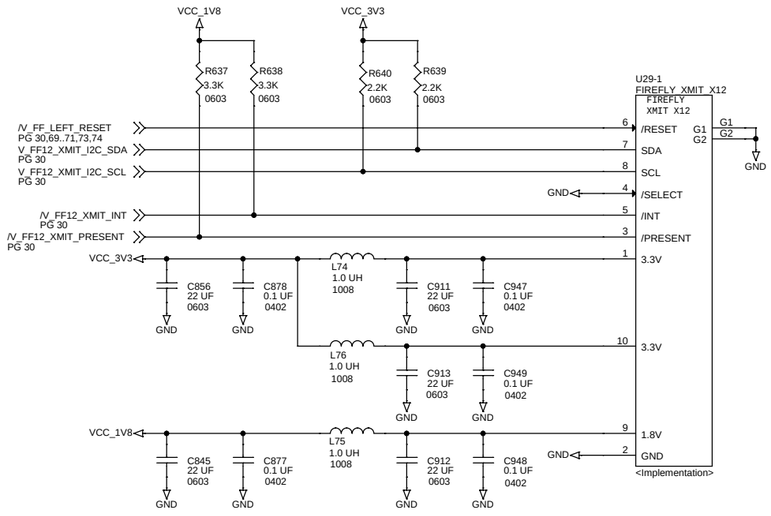
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

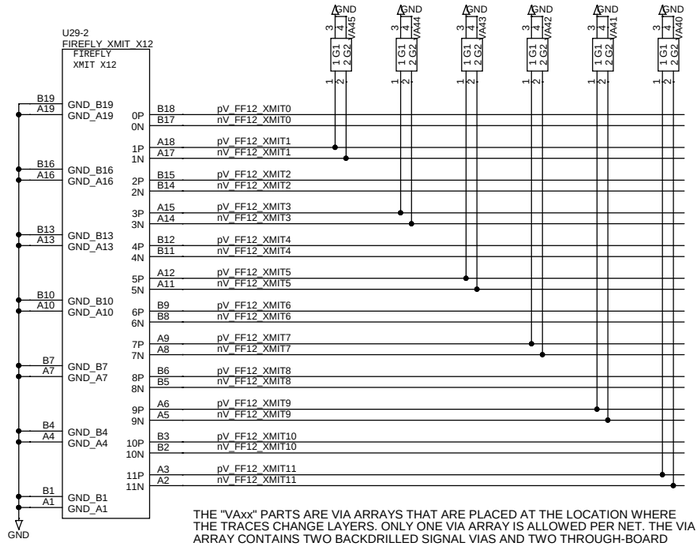
QUADS "Q" AND "S" ARE CLOCKED FROM QUAD "R"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

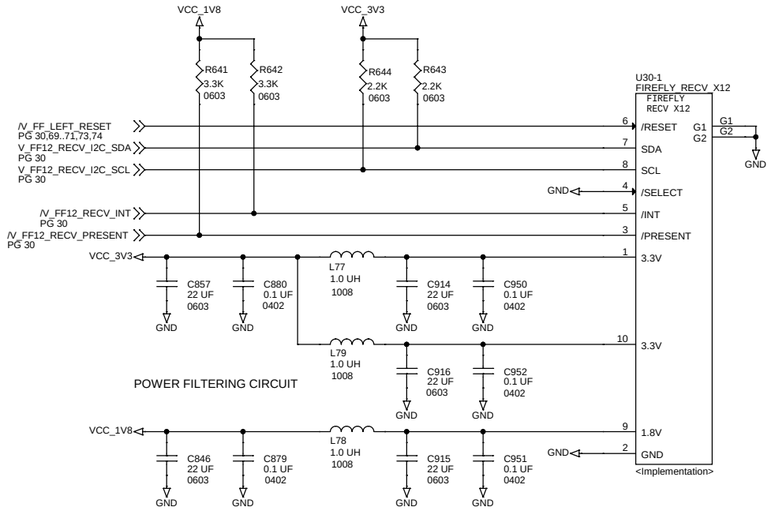
ac_pV_CLK0_CHAN7 PG 16
ac_nV_CLK0_CHAN7 PG 16
ac_pV_CLK1_CHAN7 PG 12
ac_nV_CLK1_CHAN7 PG 12



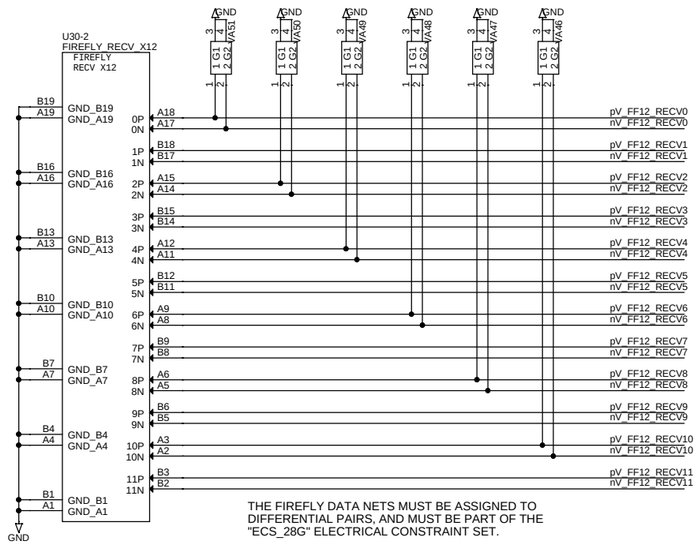
ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



POWER FILTERING CIRCUIT



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.15: VU7P QUADS QRS FIREFLY X12 #12		
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