Hornet: Non-Isolated DC-DC Voltage Regulator Modules

Guidelines for selecting and designing in Hornet Series of Regulator Modules

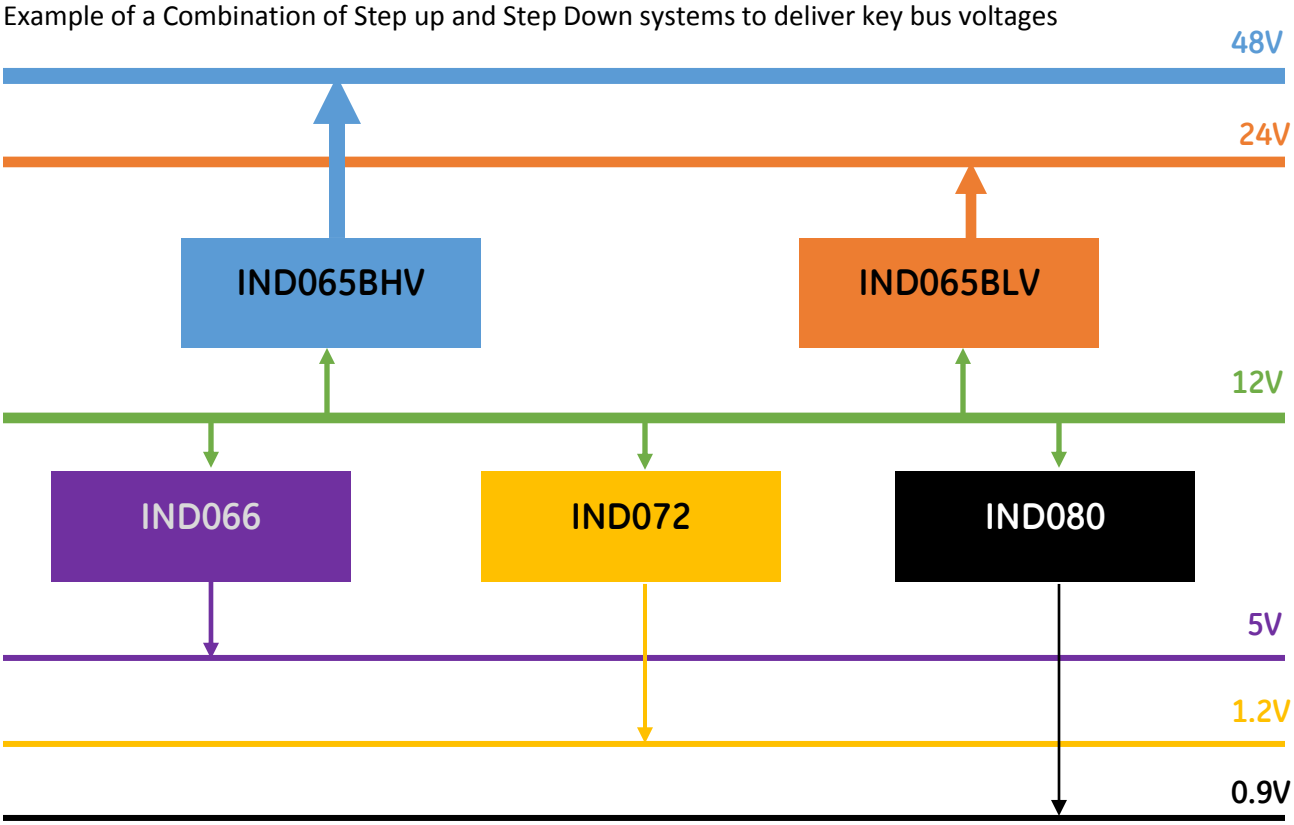
The Hornet series of voltage regulators has been developed for easy selection, design and proven performance and reliability. They are available in a wide range of output voltages, power levels, form-factors and the combination of buck and boost converters frees customers to choose their own intermediate bus voltages for multi-rail designs.

Step 1 – Choose the appropriate power module

Using the existing available primary bus voltage (B), the required output voltage (C) and output power (D), consider the appropriate modules from the list below. Then use the data in columns E and F and, if required, the datasheets to determine the module(s) best suited for the design.

A	B	C	D	E	F
MODEL	INPUT VOLTAGE (Volts)	OUTPUT VOLTAGE (Volts)	OUTPUT POWER (Watts)	INTERCONNECT TYPE	FOOTPRINT (mm x mm)
Step Down / Buck Modules					
IND016	12V±20%	0.6-5.5	16.5	Surface Mount	12.2x12.2
IND033	12V±20%	0.6-5.5	33	Surface Mount	12.2x12.2
IND066	12V±20%	0.6-5.5	66	Surface Mount	12.2x12.2
IND072	12V±20%	0.6-3.3	72.6	Surface Mount	12.2x12.2
IND080	12V±20%	0.6-2.0	80	Surface Mount	13.5x33
IND027W	12V±20%	3.0-9.0	27	Surface Mount	11.4x20.3
IND045W	12V±20%	3.0-9.0	45	Surface Mount	11.4x20.3
IND108W	12V±20%	3.0-9.0	108	Surface Mount	13.5x33
IND027XW	24V±20%	3.0-18.0	27	Surface Mount	11.4x20.3
IND045XW	24V±20%	3.0-18.0	45	Surface Mount	11.4x20.3
IND108XW	24V±20%	3.0-18.0	108	Surface Mount	13.5x33
All the above Surface Mount modules support an operating temperature range of -40 to 105°C (derated output at higher temperatures) and can withstand 40G shock and vibration. Further details are provided in the datasheets.					
IND011SIP	12V±15%	0.6-5.5	11	Through Hole	8.1x10.4
IND060SIP	12V±15%	0.6-5.5	60	Through Hole	8.4x10.4
The above SIP/Through hole modules support an operating temperature range of -40 to 85°C (derated output at higher temperatures)					
Step Up / Boost Modules					
IND065BHV	12V±20%	32-54	65	Surface Mount	11.4x27.9
IND065BLV	12V±20%	16-34	65	Surface Mount	11.4x27.9
The above Surface Mount modules support an operating temperature range of -40 to 85°C (derated output at higher temperatures)					

Example of a Combination of Step up and Step Down systems to deliver key bus voltages



Step 2 – Select the module and load support components

The datasheet provides a list of components needed to directly support the module operation. There are other components that may be needed to ensure smooth operation of both the module and load. These components can be categorized as:

- Input Capacitors – These are used to provide a stiff input source to the module and reduce the input ripple noise to keep the source power clean for other power devices connected to the input bus. Typically at least 1x22uF @16V are used for every 10A output from the module. Additional caps can be used on the input side to further lower the amount of input ripple and noise. A 1x0.047uf, 0402, 16V and a 0.1uF, 0402, 16V ceramic cap are always used to filter high frequency noise. It is also recommended to use a surface mount bulk cap to prevent the voltage from dipping below operational range during surge loading.

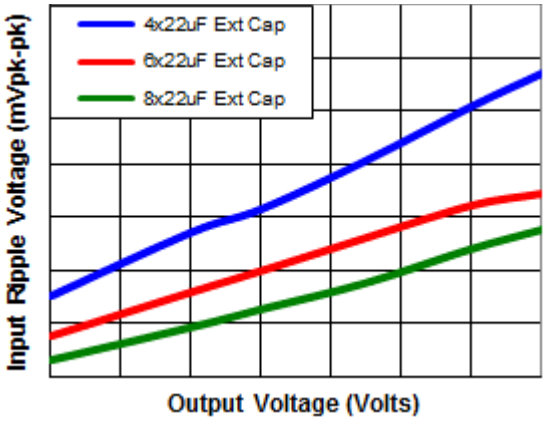


Figure 1. Proportional reduction in Input Ripple Voltage (20MHz BW) with sequential increase of external caps for various output voltages and a fixed input of 12Vin.

Module Output Current (A)	Recommended Input Capacitor Values
0-10A	Ceramics - 1x0.047uf, 0402, 16V; 1x0.1uF, 0402, 16V; 1x22uF, 1210, 16V; 47uF Bulk cap
11-20A	Ceramics - 1x0.047uf, 0402, 16V; 1x0.1uF, 0402, 16V; 2x22uF, 1210, 16V; 100uF Bulk cap
21-30A	Ceramics - 1x0.047uf, 0402, 16V; 1x0.1uF, 0402, 16V; 3x22uF, 1210, 16V; 100uF Bulk cap
31-40A	Ceramics - 1x0.047uf, 0402, 16V; 1x0.1uF, 0402, 16V; 4x22uF, 1210, 16V; 470uF Bulk cap

- Trim Resistor – The modules need an external trim resistor to provide the desired output voltage. Each datasheet has a trim equation and a table of resistor values corresponding to commonly used output voltage. For example, the IND066 has the following trim equation and corresponding table of trim resistor values. For some modules, the Trim Resistor is connected between the Trim Pin and Signal Ground instead of analog ground (the recommended connections are always shown in the datasheets).

Vo (V)	0.9	1.0	1.2	1.5	1.8	2.5	3.3	5.0	$Rtrim = \left[\frac{12}{(Vo - 0.6)}\right] k\Omega$
Rtrim (kΩ)	40	30	20	13.3	10	6.316	4.4	2.727	

- Output Capacitors – These are used to provide low noise, jitter free, tightly regulated output voltage to the load. Each module has a specification of minimum required output capacitance for stable operation of the module. However based on loading dynamics more additional capacitors may be required to keep the total voltage variation within a tight limit. Total Voltage variation is determined by 3 factors:
  - Static Variation – This is the variation due to the internal voltage reference within the module, line regulation and load regulation and is specified in the datasheet
  - Output Ripple and jitter – this is dependent on the amount of external output capacitance and the datasheet provides curves showing the reduction in ripple as capacitance is increased
  - Dynamic loads – Transient loads can perturb the output voltage and additional capacitance can be required to stiffen the output bus to minimize the effect of dynamic loads on the voltage bus. The Tunable Loop feature available in GE modules helps with this issue.

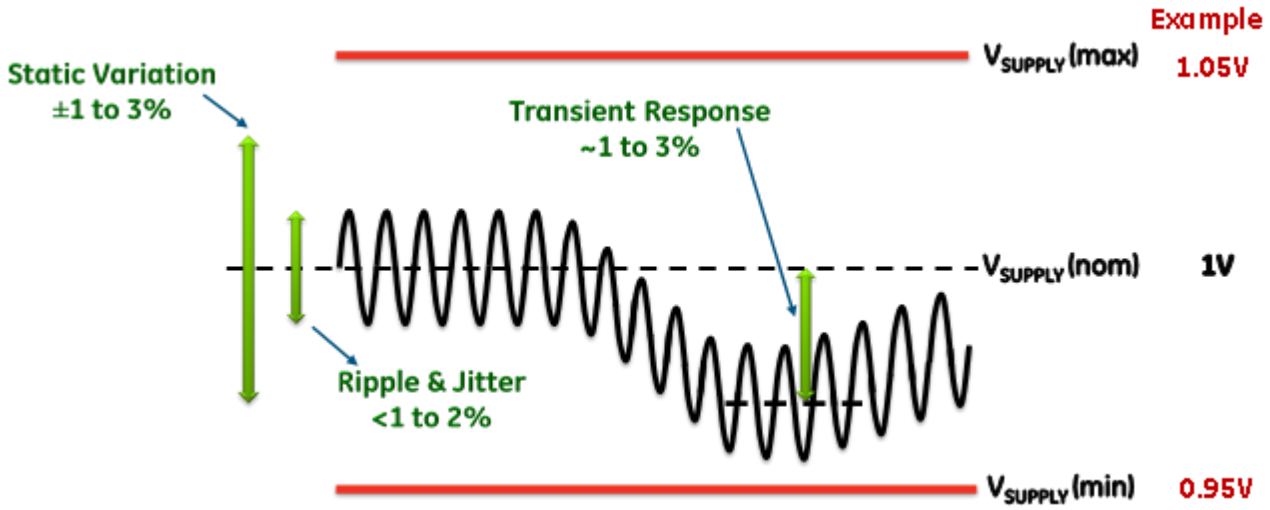


Figure 2 Components of voltage deviation that voltage regulators must address in order to meet IC powering requirements: Static Variation, Ripple and Jitter, and, Transient Response.

As with Input Capacitors, the output side also needs at least 1x0.047uf, 0402, 16V and a 0.1uF, 0402, 16V for filtering high frequency noise. The number of higher rated ceramic caps will depend on the desired output ripple and the number of bulk caps will depend on the presence of dynamic loads.

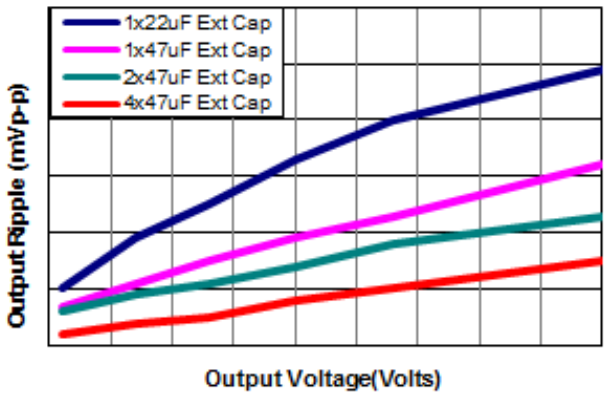


Figure 3. Proportional reduction in Output Ripple Voltage (20MHz BW) with sequential increase of external caps for various output voltages and a fixed input of 12Vin.

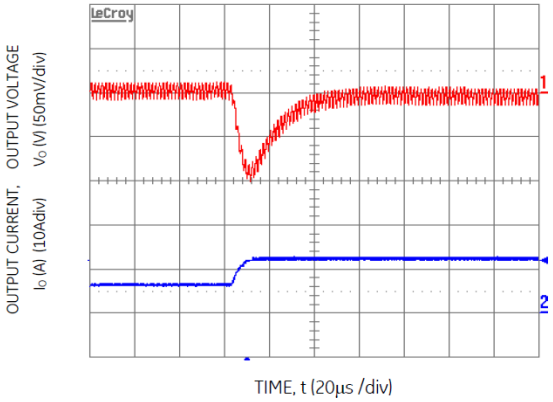


Figure 4. Dynamic Load Change from 50% to 100% at 12Vin, Cout-1x0.047uF, 5x47uF, CTune-1500pF & RTune-330ohms for IND066

- Tunable Loop – The output voltage response by Voltage Regulators is a function of two parameters: (1) the external capacitance and (2) the control bandwidth of the Regulator+load. Due to the Voltage Regulator's limited bandwidth (typically the control loop gain crosses through the 0dB point at no more than 1/10th of the switching frequency), the initial surge of current is provided by the external capacitors. Once the Regulator control loop is able to come into play, the new level of load current is provided by the Voltage Regulator and the current from the external capacitors goes to nearly zero. Hence external capacitors improve transient voltage response by providing additional energy during the transitions between load current levels. As external capacitance is added, the initial deviation due to a load transient is reduced further, leading to the conclusion that lower transient voltage deviations are achieved simply by adding more capacitance.

  While increasing control bandwidth and increasing the external capacitance both improve transient response, these parameters are not independent. In fact, there is a strong interaction between them, as increasing the external capacitance degrades the control bandwidth of the system. Therefore, the full benefits of the external capacitance cannot be realized unless this degradation in counteracted. This is the function of the Tunable Loop feature. It allows the designer to re-tune the control loop to compensate for the additional external capacitance resulting in an optimum balance of capacitance and bandwidth yielding the best transient response possible for a given set of application requirements while minimizing the bulk capacitors.

  The power of the Tunable Loop™ is in its simple implementation. As shown in Figure 5, an external network consisting of a resistor and capacitor in series is connected across the TRIM and Vout (or SENSE) pins of the REGULATOR module. These are typically very small, inexpensive passive devices: The resistor may an 0805, 0603, or 0402 SMT component ranging in resistance from a few Ω to a few kΩ. Likewise, the capacitor is similar in size ranging from a few hundred pF to a few hundred nF. Fundamentally, this allows a single REGULATOR module to be externally optimized across multiple applications of significantly varying demands with minimal effort yielding the optimum board area, cost, response, and reliability. This additional benefit of module consolidation through a simple programmable feature yields significant dividends on both technical and commercial levels.

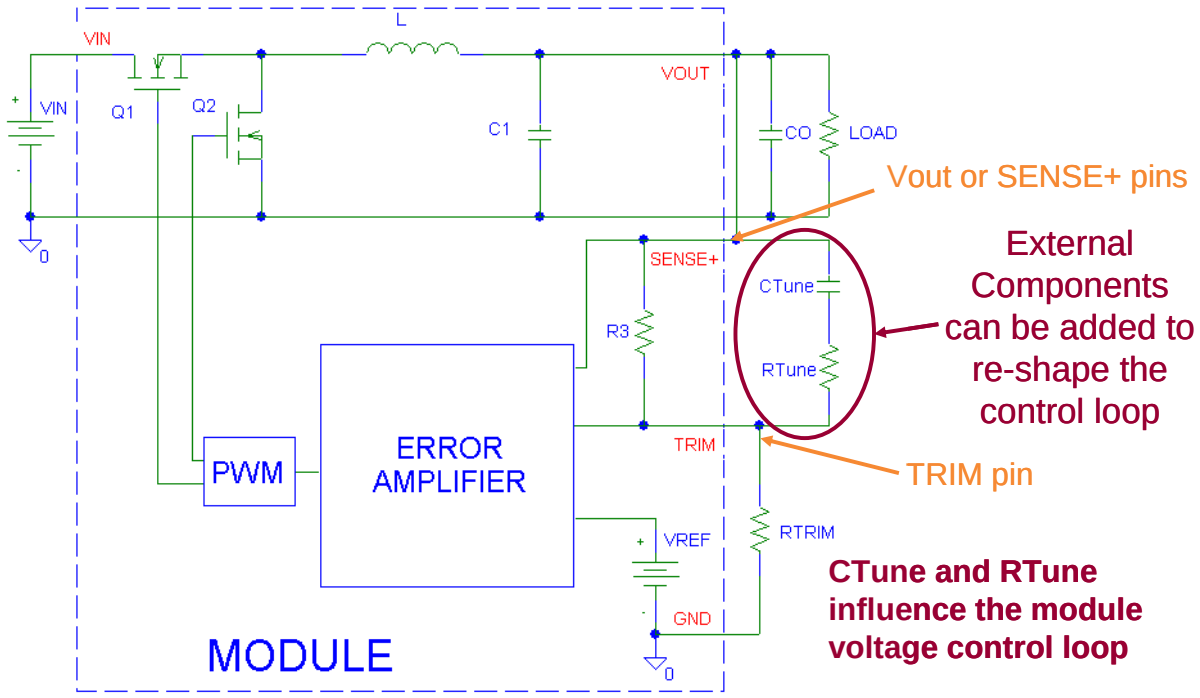


Figure 5. Diagram showing how the Tunable Loop™ feature can be implemented by adding two inexpensive components CTune and RTune to re-shape the voltage regulator voltage control loop

Each of the IND codes has a unique Tunable Loop Look-up Table that provides the value of Rtune and Ctune for a fixed set of output capacitors. This avoids the need for the user to do any simulation work. An example of the table shown in the IND066 datasheet is shown below:

Co	2x47µF	4x47µF	6x47µF	10x47µF	20x47µF
R_{TUNE}	330	330	330	270	180
C_{TUNE}	560pF	1500pF	2200pF	3900pF	6800pF

- On/Off Connections – Most regulators support a negative logic architecture where the Module turns ON when the On/Off pin is held at a Logic low level. Check the individual regulator datasheet for more information regarding On/Off operations. Most regulators will also turn-on if On/Off pin is left floating with exception of IND027W, IND045W, INDO27XW and INDO45XW where the ON/Off pin must be connected to ground for the module to turn on.

- PGOOD – Some regulators provide a PGood terminal. This is an Open Drain terminal that indicates the regulator output voltage is within regulation limits. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going ±10% outside the setpoint value. The PGOOD terminal can be typically connected through a pullup resistor (suggested value 10 to 100KΩ) to a source of 5VDC or lower. The current through the PGOOD terminal is usually restricted to less than 5mA.

- SYNC – Some regulators provide a Sync terminal. The regulator switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external

signal applied to the SYNC pin of the module as shown in Fig. 6, with the converter being synchronized by the rising edge of the external signal. The IND072 regulator switches at half the SYNC frequency. Other regulators switch at the applied frequency. If the SYNC pin is not used, the module will free run at the default switching frequency. **If synchronization is not being used, connect the SYNC pin directly to SIG_GND** (or GND in some codes, see datasheet)

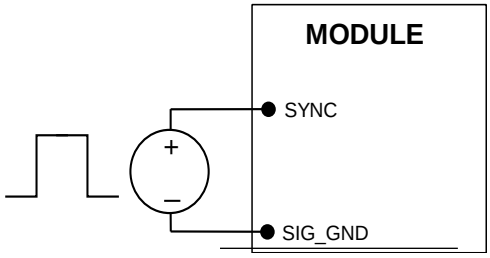


Figure 6. External source connections to synchronize switching frequency of the module

Step 3 – Layout guidelines

- Location of the regulator should be carefully considered to minimize the effects of noise. Voltage regulators are typically located as close as possible to the load. When multiple loads are powered from one unit, it should be located closest to the most voltage sensitive load. If a trade-off between the length of the input and output traces needs to be made, the output trace should be made as small as possible. Suggested layout of the traces used to connect the regulators and locations of external components are provided later in this application note. These considerations, along with good analog design layout practices are sufficient to achieve optimal performance when using these modules.
- Minimize loop area - To provide the most effective filtering and avoid noise coupling from a regulator to other parts of the circuit, it is recommended that the loop area for both power and signal traces to the regulator be minimized. To minimize input noise, it is necessary to reduce the parasitic inductance of the input loop significantly, by reducing the loop area. Using a high frequency, low ESR and ESL bypass capacitor, close to the regulator module input pins reduces the area of this loop significantly.
  Figure7 shows a typical application circuit incorporating these recommendations. For reducing high-frequency switching noise at the input and output of the module, 0.047µF (0402), 0.1µF (0402), etc. small package ceramic capacitors (CI1 and CO1 in schematic) should be placed at the input and output of the module. Capacitors used for minimizing the ripple component (CI2, CI3, CO2 & CO3) are termed as bulk capacitors with capacitance needed being in the order of tens or hundreds of µF.

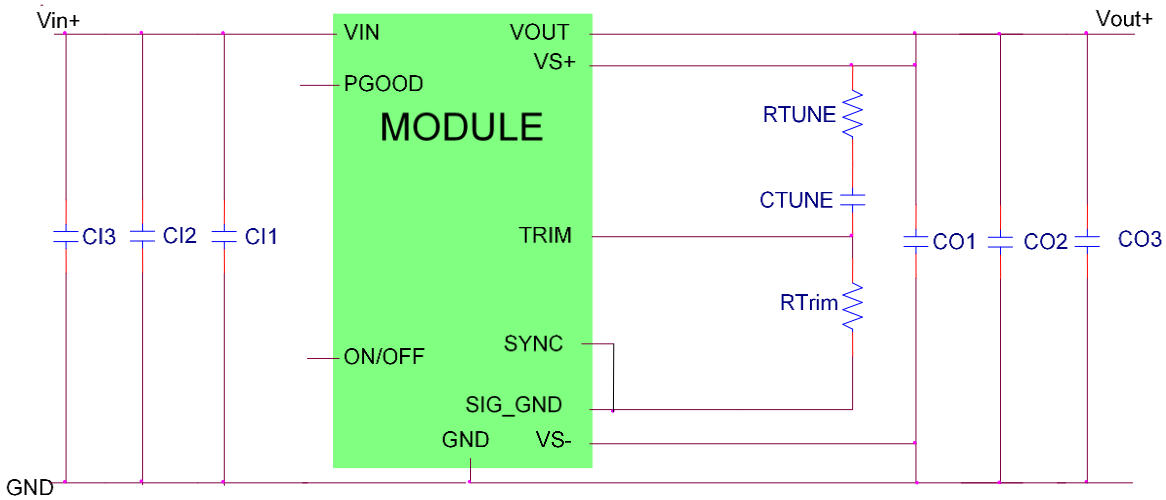


Figure 7. Typical Application Circuit of the IND072 regulator.

Figure 8 shows an example layout for the IND016,033,066 and 072 modules. This example details the key guidelines to be followed when designing the module on to your board. For simplicity, all three power traces (input, output and ground) are assumed to be on the top layer of the PWB – where the regulator is placed.

The guidelines are:

1. Extend the ground plane to the area underneath the module. It is not recommended that this space be utilized for routing signal traces unless they are in inner layers underneath the ground plane. Observe any keepout areas specified for the module.
2. The V_{OUT} and ground planes are placed close together to minimize interconnect inductance on the output side. Similarly on the input side, interconnect inductance is minimized by placing the V_{IN} and ground planes close together
3. Output capacitors (C_{OUT}) are connected as close to the output/ground pins as possible to provide the most effective output filtering. Similarly the input capacitors are placed as close to the input/pins as possible.

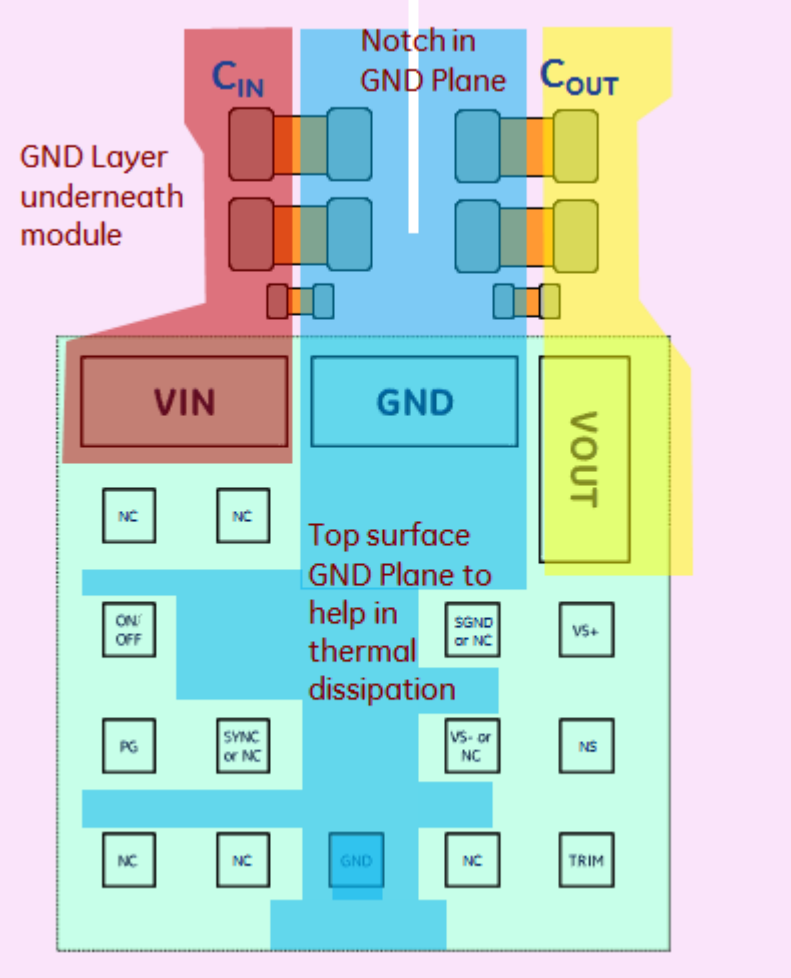


Figure 8. An example layout for a few of the IND modules

4. Pinch traces slightly in the areas where filtering capacitors are placed to force current to flow near the capacitors.
5. Insert a notch in the GND Plane to separate GND currents flowing into the input and output pins. The length of the notch should be determined depending on current rating and cooling of modules. If the module is not force cooled, then the notch should not be too close to the Ground pin to allow for longer unbroken ground plane surface to conduct heat from the module ground pads. The same criteria should be applied for notch sizes among different current rating modules – the higher the module rating the further the separation of the notch from the ground pad.
6. The high frequency low ESR and ESL capacitors (usually 0.01µF or 0.0047µF capacitor in 0402 package should suffice) must be placed closest to the input and output terminals to provide the shortest loop for noise attenuation. The placement of these capacitors should take priority in terms of proximity to the module as compared to other higher value capacitors on both input and output terminals.

- Location of filtering components- It is desirable to have the regulator, filter capacitors and input and output traces all on the same layer. However, practical considerations may require the use of multiple vias to either connect to the input and/or output to a different board layer. There are 2 possible layouts with the use of vias.

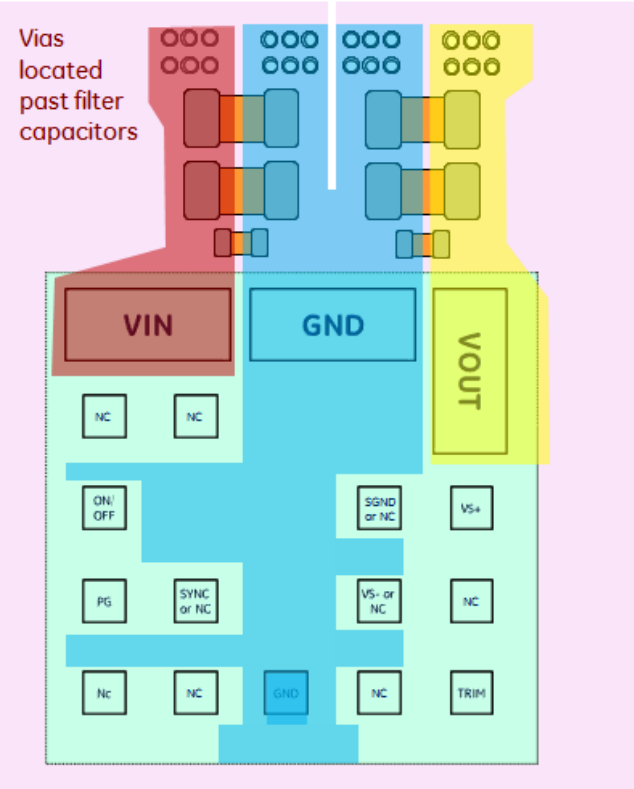


Figure 9. An example Layout for some of the IND series module with vias for output and input power connections.

In the first and preferred layout arrangement both input and output capacitors are on the same layer as the module. Connections are then made vias to inner layers if needed. The high frequency capacitors are placed closest to the module before the vias are placed. A rule of thumb is to have 3A/per via. The recommended via size is 22 mils (0.022" or 560µm) plated-through hole. For control pins, one via per pin is sufficient. Vias should be located in the direction of current flow for optimum performance. For signal traces, the recommended trace width for signal traces is 7 – 10 mils (180 - 250µm). For bulk capacitors, 1-2 vias per capacitor connection are recommended. It is important that the vias be located past the input/output filter caps. Figure 9 shows a layout of the Regulator module showing vias located one the output, input and ground traces for carrying current to the inner layers.

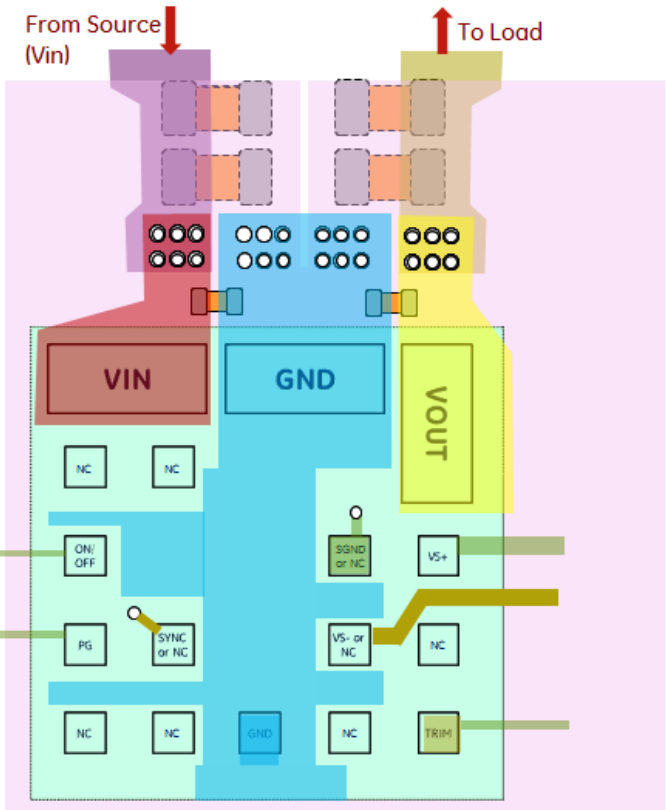
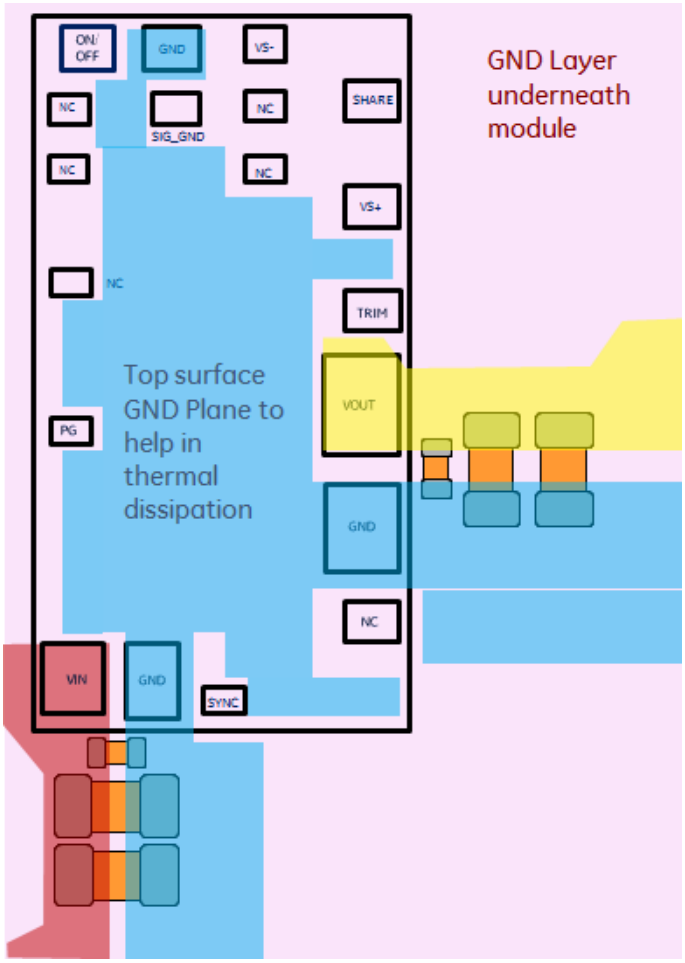


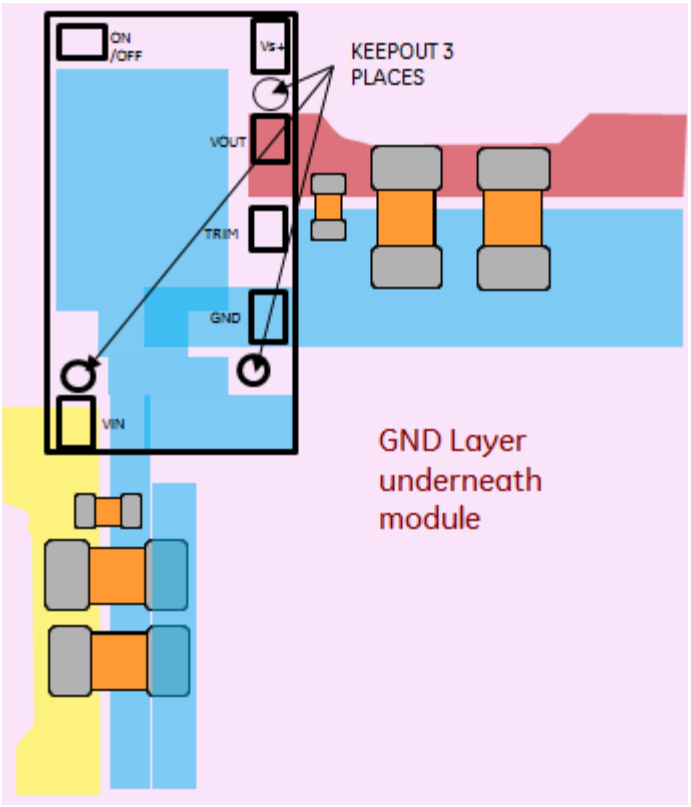
Figure 10. An example Layout with vias for bulk caps, input-output power and suggested control connections.

The second example, shown in Fig. 10, is where the bulk filter capacitors are located on the opposite layer from the module (module on top layer and filter capacitors on bottom layer or vice-versa). It is important that the high frequency filtering capacitors still be located on the same layer as the module and only the bulk capacitors be located on the opposite layer. If the Voltage Sense+ (VS+) and Voltage Sense- (VS-) connection also need to be routed through vias to the opposite layer, they should connect through a 0 ohm resistor on the module layer. TRIM and SGND are sensitive, high-impedance analog terminals. Isolate them from noisy board areas. The trim resistor and tunable loop components should be on the same layer (preferably on top) and close to the module. If the return path for the TRIM is being connected to a SGND, Vs- or GND do not connect that return path to any other trace on the board. These should terminate directly back to the module pin and not be tied to a common return/ground path.

- Clearances around the regulator - Signal traces should not be routed underneath the module, unless sandwiched between ground planes, to avoid noise coupling. Also, components should not be placed under the module to prevent any coupling. The ground plane can be placed under the module. For repair and removal of the SMT module from the PWB, 4.0 mm (0.16 inches) of clearance is recommended around the module outline. This clearance provides and isolates adjacent components from exposure to heat during the removal process.

- Example Layouts of other IND modules





Summary

GE Hornet series Voltage Regulators has been designed for easy design and integrations into challenging applications. A concise list of modules assists in quickly arriving on a suitable part. This application note has covered the process of selection of additional passive components to achieve a stable, low-noise design. Low ESR, surface mount multi-layer ceramic capacitors are the best choice for filtering high-frequency ripple voltage. Several graphs to aid the circuit designer in selecting the right input filter capacitors to use with REGULATORs have been provided. If other capacitor technologies such as aluminum electrolytics are utilized for load transient suppression on the input bus, they should always be used in parallel with ceramic capacitors.

Finally, several example layouts for the Hornet series of regulators have been presented to illustrate the important principles involved in designing GE regulators into an application circuit. In addition, guidelines for via sizing,

number of vias and their placement have been provided. For specific questions in specialized applications and board layout, please consult your local GE Technical Representative for additional information.

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