THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY.
THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: GLOBAL SIGNALS
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: KU15P POWER AND SIGNAL (NON-MGT)
6: VU7P POWER AND SIGNAL (NON-MGT)
7: KU15P MGT TRANSCEIVERS
8: VU7P MGT TRANSCEIVERS

TO DO:

CHECK "bc" AND "ac" PREFIXES ON AC-COUPLED SIGNALS

ON VU7P QUAD "S', CHANGE "...133" TO "...S" IN PIN NAMES

ON VU7P QUAD "A-J', CHANGE "...GTH" TO "...GTY" IN PIN NAMES

ASSIGN AND LABEL I2C ADDRESSES

SOLDERPASTE PATTERNS FOR UEC5_UCCE FOOTPRINT

NETS TO STUDY / DOCUMENT

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 1.01: NOTES

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Firefly #V1
4 Ch XCVR
4 GTY I/O
Firefly #V2
4 Ch XCVR
4 GTY I/O
Firefly #V3
4 Ch XCVR
4 GTY I/O
Firefly #V4
4 Ch XCVR
4 GTY I/O
Firefly #V5
4 Ch XCVR
4 GTY I/O
Firefly #V6
4 Ch XCVR
4 GTY I/O
Firefly #V7
4 Ch XCVR
4 GTY I/O
Firefly #V8
4 Ch XCVR
4 GTY I/O
Firefly #V9
4 Ch XCVR
4 GTY I/O
Firefly #V10
4 Ch XCVR
4 GTY I/O
Firefly #V11
12 Ch
XMIT/RECV
4 GTY I/O
4 GTY I/O
4 GTY I/O
Firefly #V12
12 Ch
XMIT/RECV
4 GTY I/O
4 GTY I/O
4 GTY I/O

UltraScale+
FPGA
B2104 Package
76 GTY

VU5P
VU7P*
VU9P
VU11P

***=Initial Target**

CONFIG
FLASH
CONFIG
FLASH
3 GTY I/O
UTILITY I/O
POWER & I2C
CONTROLLER
POWER
REGULATORS
CLOCK &
TIMING
UTILITY I/O
JTAG
2 GTY I/O
ZYNQ PCIe / AXI C2C
BLADE
CONNECTORS
2 GTH I/O
ZYNQ PCIe / AXI C2C

Kintex
UltraScale+
FPGA
A1760 Package
44 GTH
32 GTY

KU15P*

***=Only choice in this package**

4 GTH I/O
4 GTH I/O
4 GTH I/O
Firefly #K1
12 Ch
XMIT/RECV
4 GTH I/O
4 GTH I/O
4 GTH I/O
Firefly #K2
12 Ch
XMIT/RECV
4 GTH I/O
4 GTH I/O
4 GTH I/O
Firefly #K3
12 Ch
XMIT/RECV
4 GTY I/O
Firefly #K4
4 Ch XCVR
4 GTY I/O
Firefly #K5
4 Ch XCVR
4 GTY I/O
Firefly #K6
4 Ch XCVR
4 GTY I/O
4 GTY I/O
4 GTY I/O
Firefly #K7
12 Ch
XMIT/RECV

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title: 1.02: BLOCK DIAGRAM
Size: | Document Number: 6089-103 | Rev: A
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KU15P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

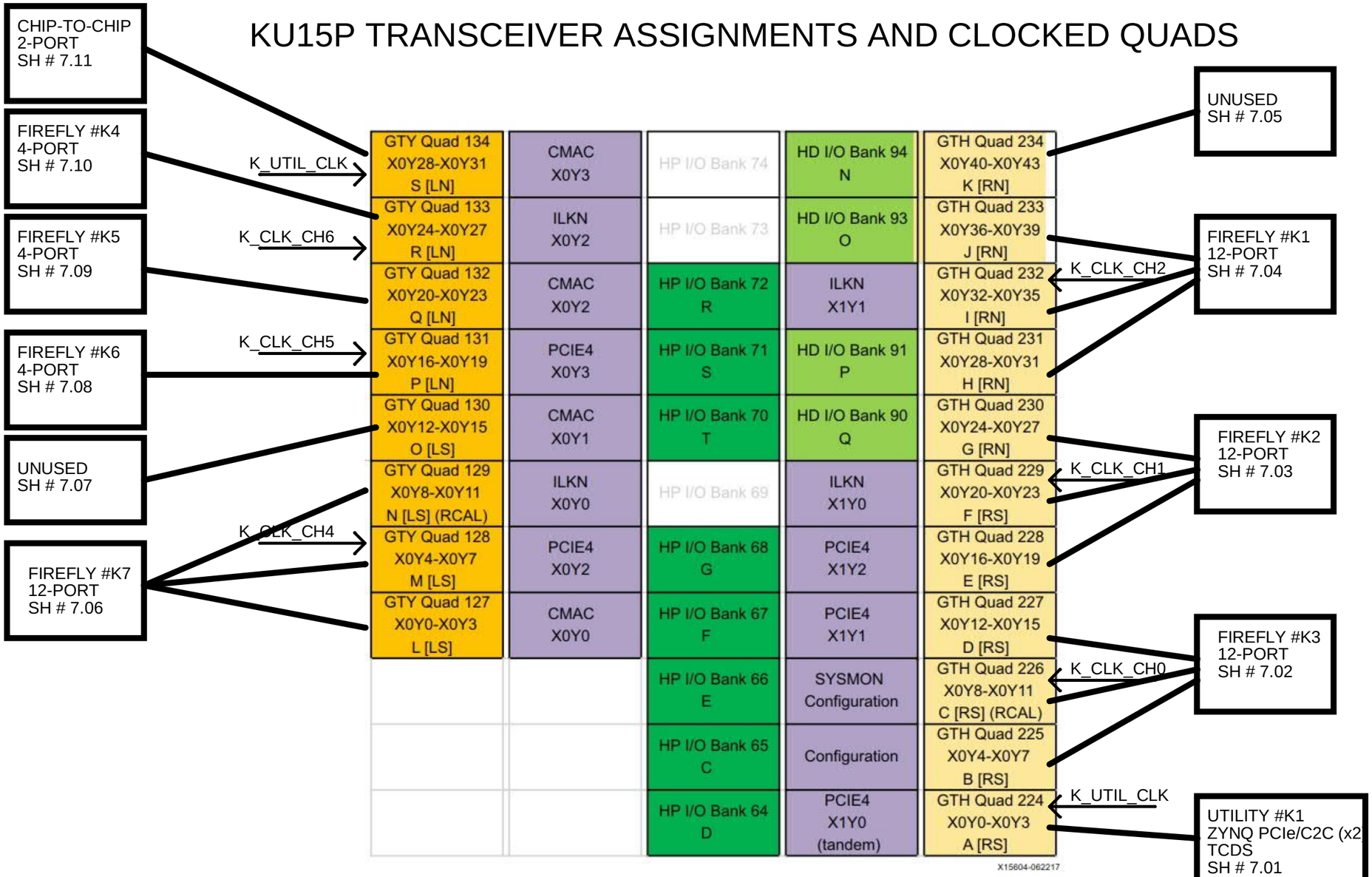

Figure 1-86: **XCKU15P Banks in FFVA1760 Package**

EACK "K_CLK_CHn" CONSISTS OF TWO CLOCKS.
ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.03: KU15P TRANSCEIVERS		
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VU7P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

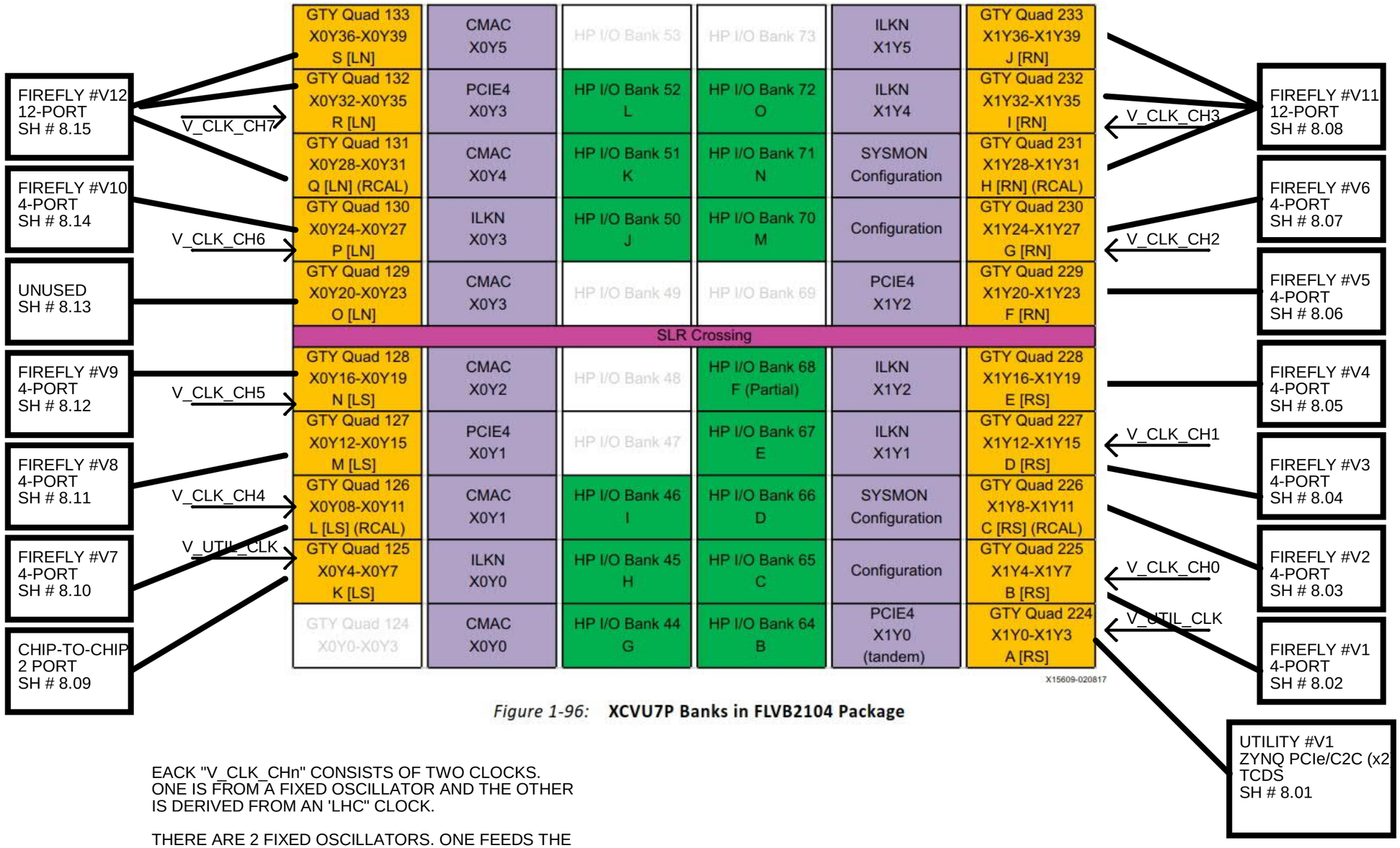

Figure 1-96: **XCVU7P Banks in FLVB2104 Package**

EACK "V_CLK_CHn" CONSISTS OF TWO CLOCKS.
ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.04: VU7P TRANSCEIVERS		
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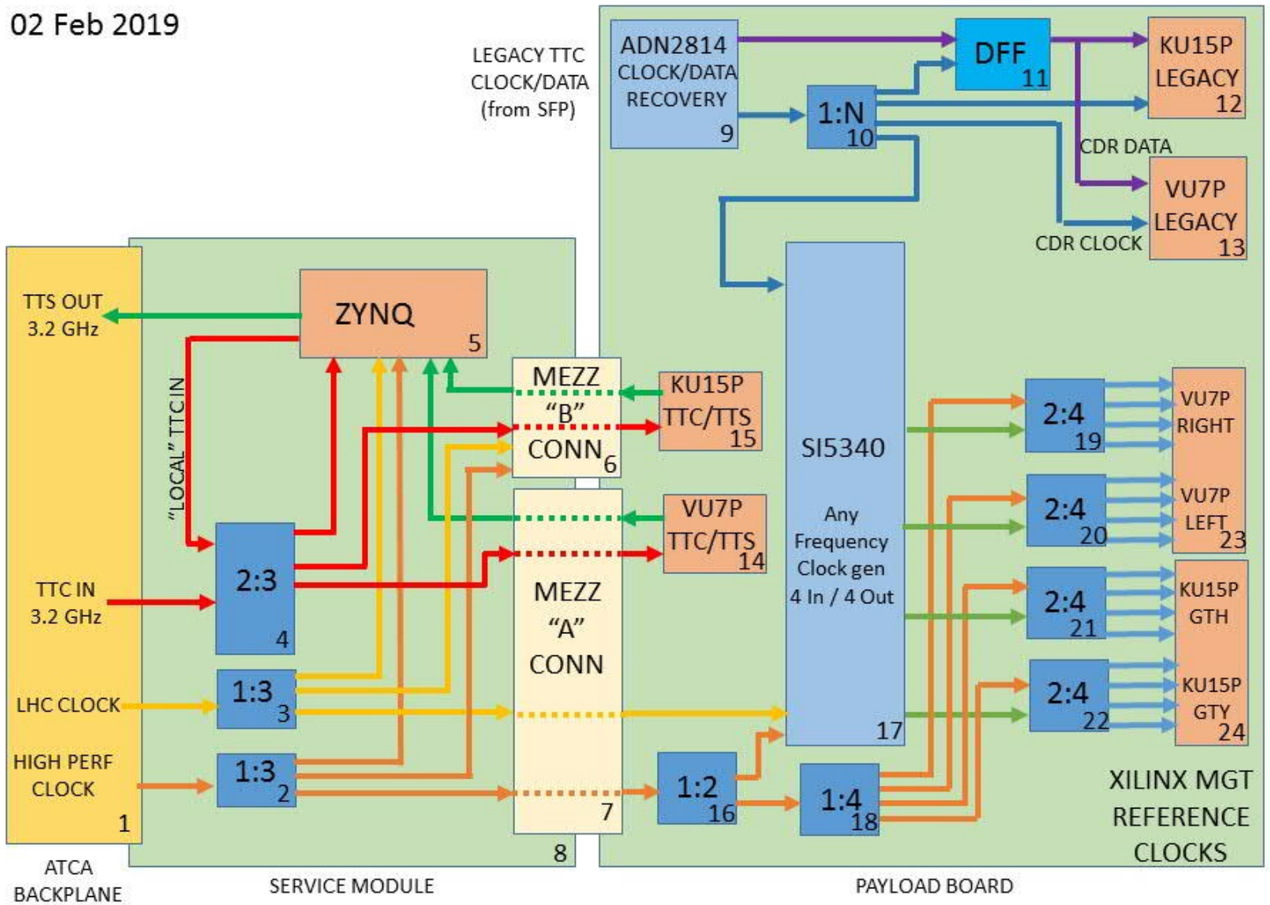
BU/CU Apollo ATCA Backplane Signal Distribution

02 Feb 2019



Charlie Strohman crs5@cornell.edu

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.05: LHC SIGNAL DISTRIBUTION		
Size	Document Number: 6089-103	Rev: A
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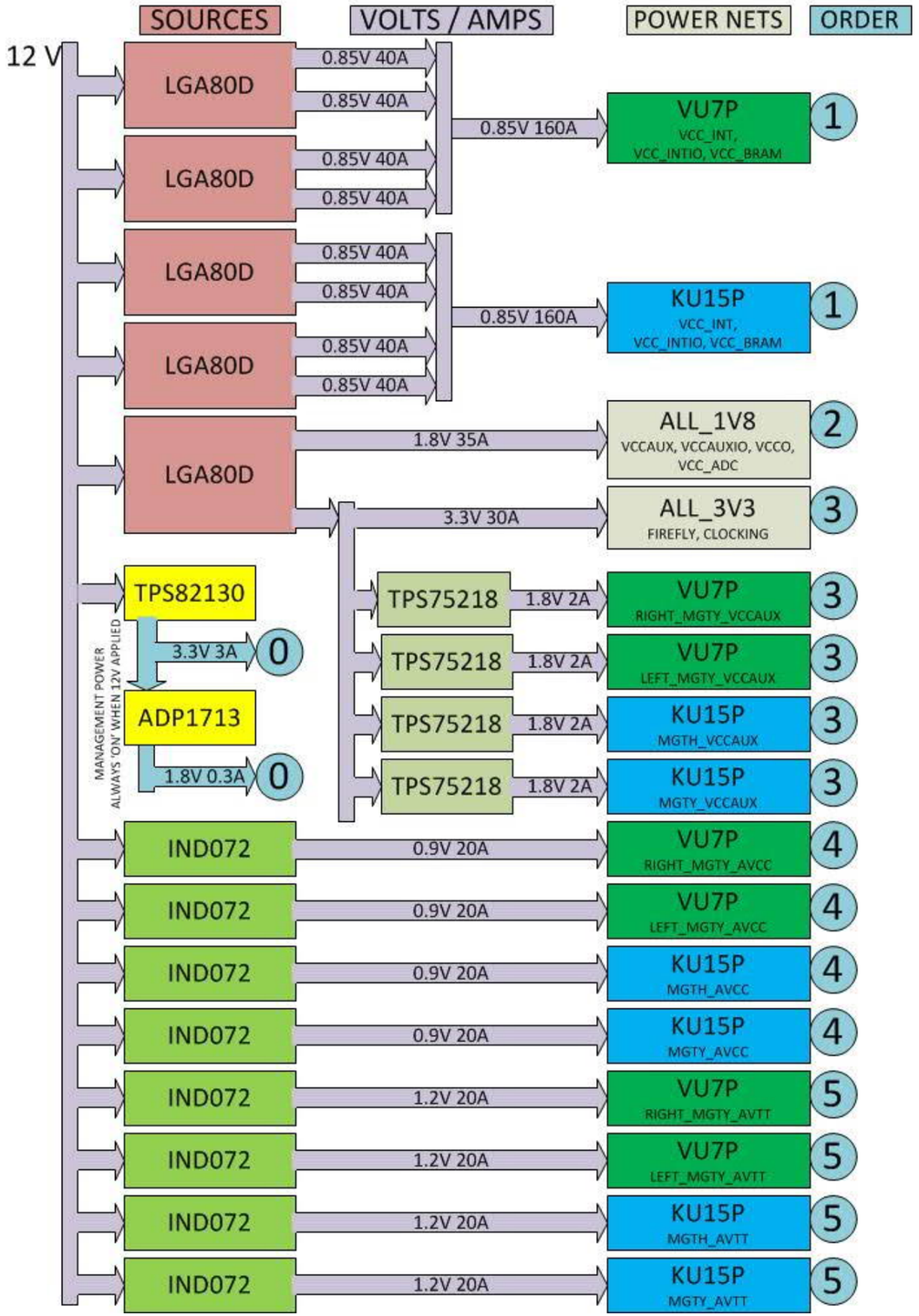

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 1.06: POWER DISTRIBUTION

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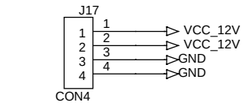
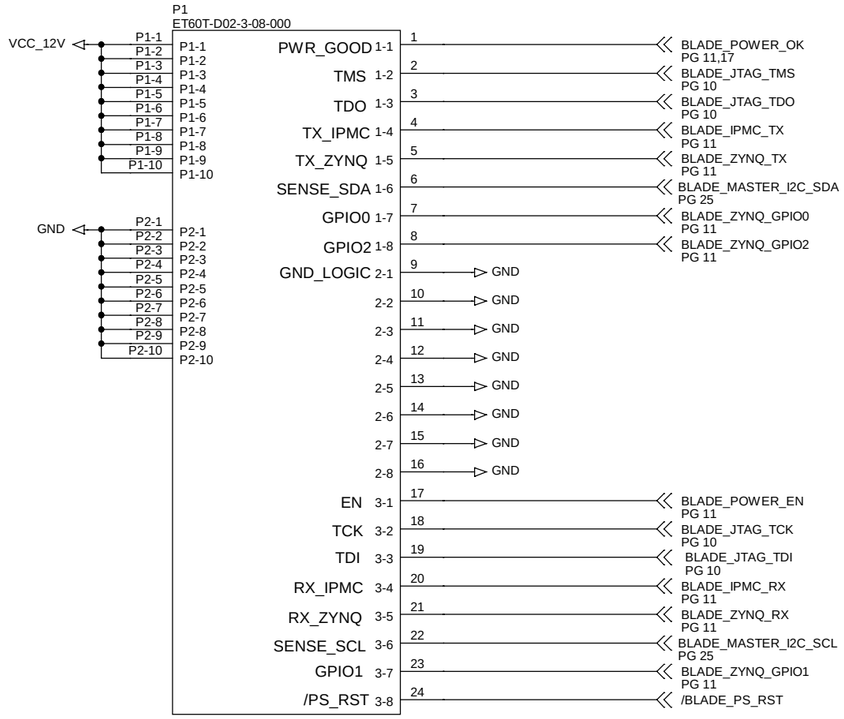
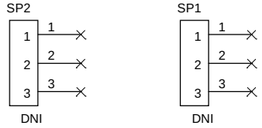


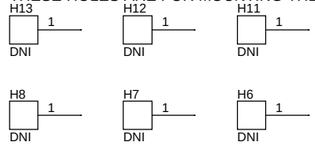
Bench Top Power Inlet



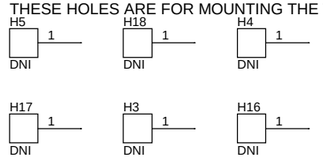
THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.



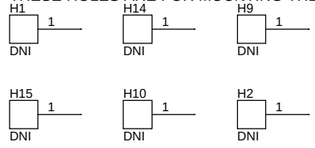
THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINKS

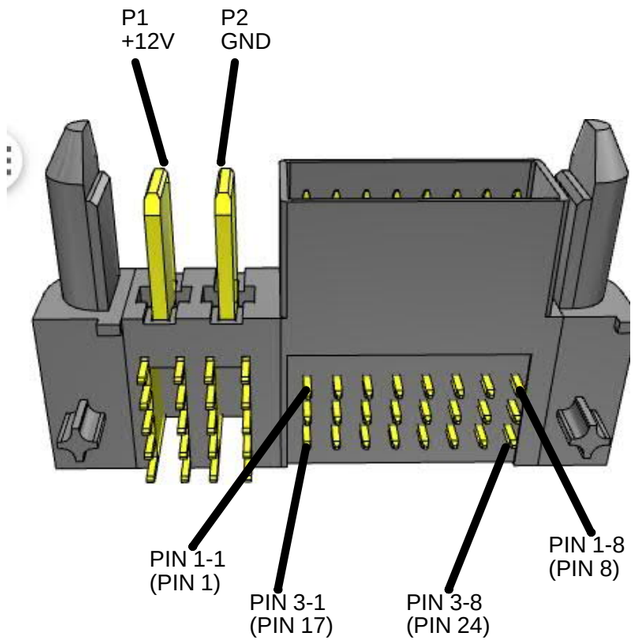


THESE HOLES ARE FOR MOUNTING THE TOP COVER



THESE HOLES ARE FOR MOUNTING THE BOTTOM COVER





ET60T-D02-3-08-000

THESE SHAPES DEFINE MECHANICAL OBJECTS THAT SHOULD BE IN THE BILL OF MATERIALS.

M1 KU15P HEATSINK
M23 HEATSINK PLATE
M3 M3 STANDOFF
M4 M3 STANDOFF
M5 M3 STANDOFF
M6 M3 STANDOFF
M7 M3 STANDOFF
M8 M3 STANDOFF
M2 VU7P HEATSINK
M24 HEATSINK PLATE
M9 M3 STANDOFF
M10 M3 STANDOFF
M11 M3 STANDOFF
M12 M3 STANDOFF
M13 M3 STANDOFF
M14 M3 STANDOFF
M15 FIREFLY HEATSINK (LEFT SIDE)
M16 M2.5 STANDOFF
M17 M2.5 STANDOFF
M18 M2.5 STANDOFF
M19 FIREFLY HEATSINK (RIGHT SIDE)
M20 M2.5 STANDOFF
M21 M2.5 STANDOFF
M22 M2.5 STANDOFF

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.01: BLADE POWER CONNECTOR		
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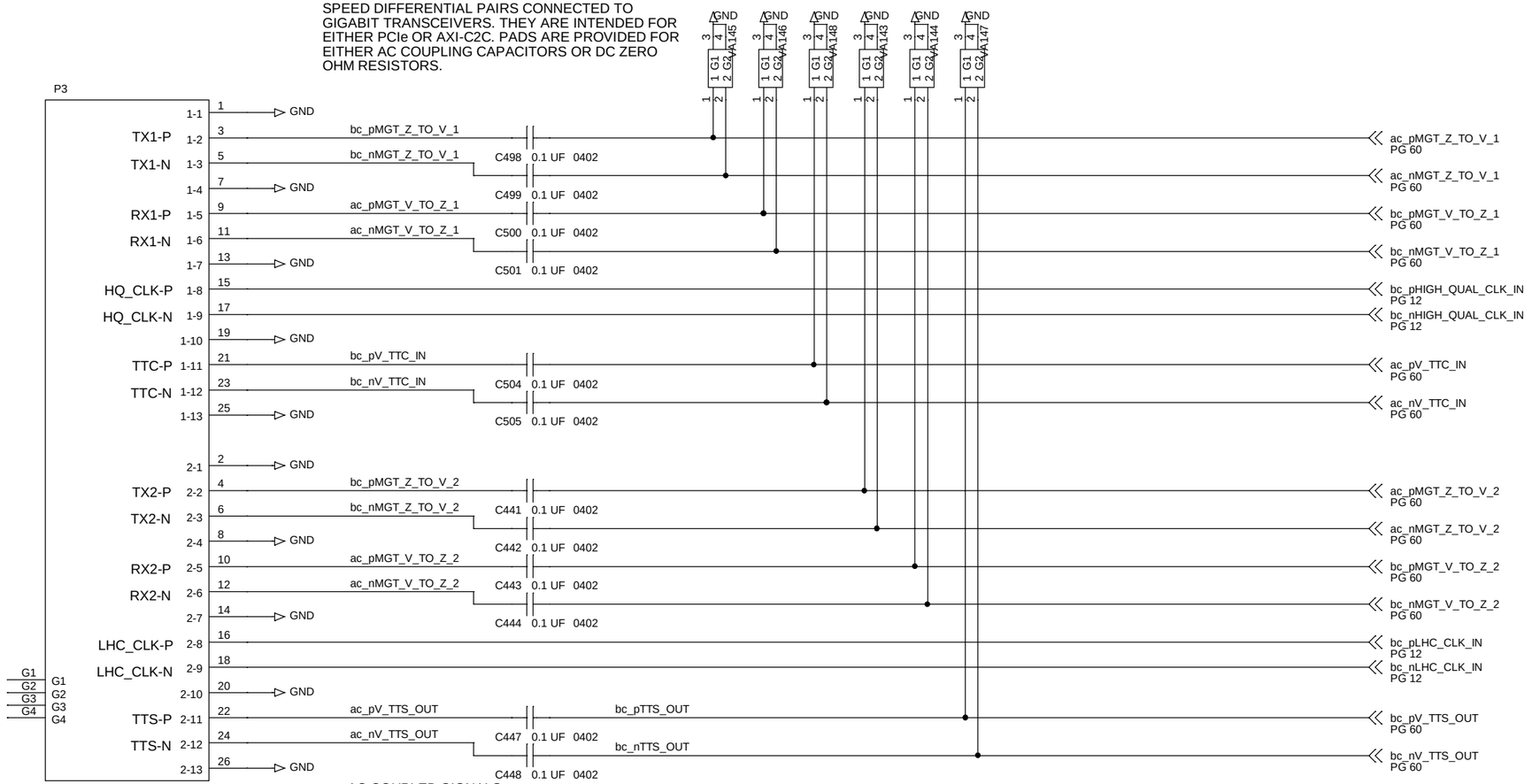
THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.

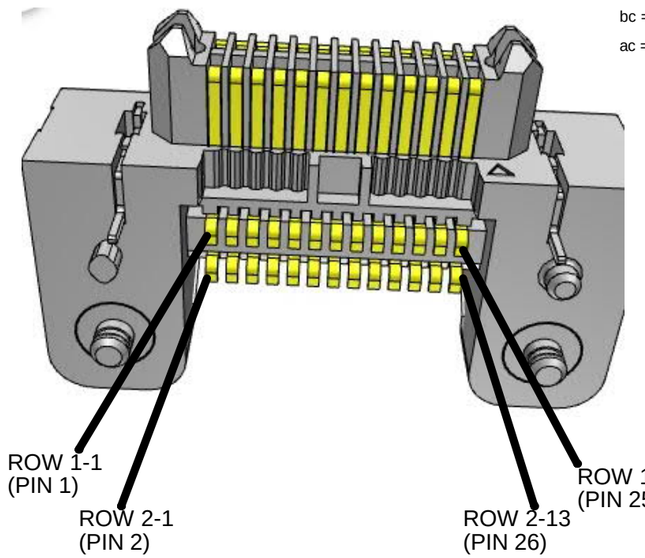


AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

VU7P AND BACKPLANE CLOCK SIGNALS ONLY



ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.02: BLADE HS CONNECTOR #1		
Size	Document Number: 6089-103	Rev: A
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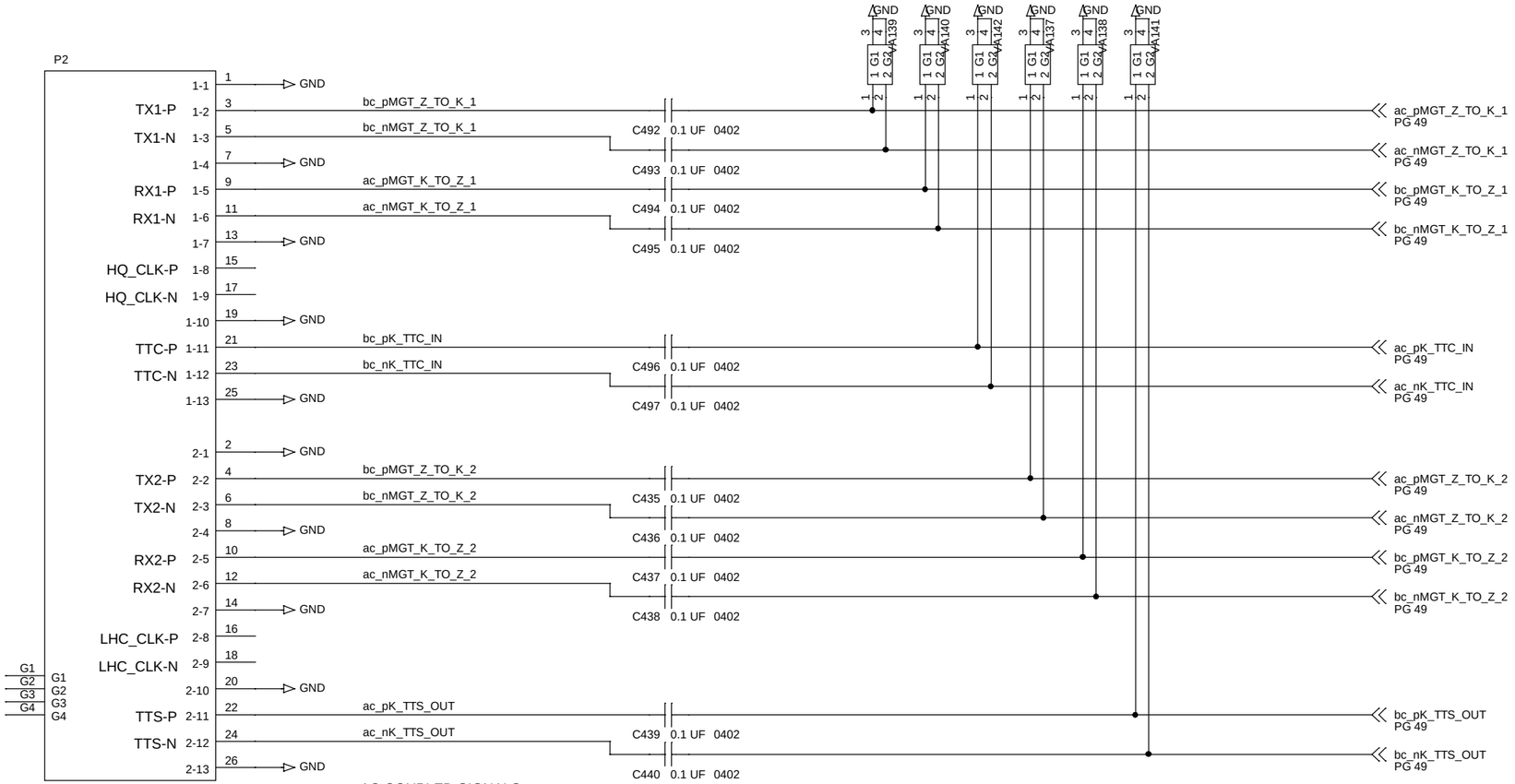
THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.

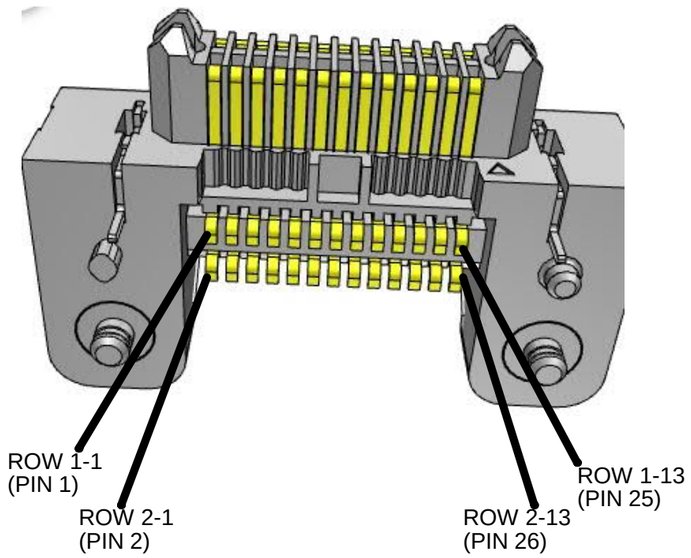


AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

KU15P SIGNALS ONLY



ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.03: BLADE HS CONNECTOR #2		
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TO BYPASS A DEVICE, CONNECT A JUMPER FROM 1 TO 3.
TO INCLUDE A DEVICE IN THE CHAIN, CONNECT A JUMPER FROM 1 TO 2 AND FROM 3 TO 4.
AS ILLUSTRATED, THE CONTROLLER AND THE VU7P ARE PART OF THE CHAIN, AND THE KU15P IS BYPASSED.

BLADE JTAG

BLADE_JTAG_TMS PG 7

VCC_M3V3 — R108 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

U49 74LVC1G126 — R92 33 0603 — V_TMS_1V8
U53 74LVC1G126 — R98 33 0603 — K_TMS_1V8
U57 74LVC1G126 — R107 33 0603 — C_TMS_3V3
U50 74LVC1G125 — R95 33 0603
U55 74LVC1G125 — R101 33 0603
U60 74LVC1G125 — R109 33 0603
U62 74LVC1G126 — R113 33 0603 — V_TCK_1V8
U77 74LVC1G126 — R123 33 0603 — K_TCK_1V8
U84 74LVC1G126 — R133 33 0603 — C_TCK_3V3
U67 74LVC1G125 — R116 33 0603
U78 74LVC1G125 — R130 33 0603
U86 74LVC1G125 — R136 33 0603

VCC_M3V3 — R94 10K 0603

BLADE JTAG

BLADE_JTAG_TCK PG 7

VCC_M3V3 — R134 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

VCC_M3V3 — R115 10K 0603

FORCE JTAG CABLE

IF EITHER THE JUMPER IS IN PLACE, OR THE PROGRAMMING CABLE IS PLUGGED IN, THE OUTPUT OF THIS BUFFER WILL BE LOW. THIS WILL ENABLE ALL OF THE DRIVERS RELATED TO THE CABLE SIGNALS, AND DISABLE ALL OF THE DRIVERS RELATED TO THE MAIN BLADE.

VCC_M3V3 — R70 10K 0603 — J12 JUMPER — GND

U37 74LVC1G125

THE JTAG REFERENCE IS 3.3 VOLTS.

J1 CON_2X7_RA
CONN_JTAG_TMS
CONN_JTAG_TCK
CONN_JTAG_TDO
CONN_JTAG_TDI

USE THE JUMPER IF PIN 13 IS NOT AUTOMATICALLY PULLED LOW WHEN THE CABLE IS PLUGGED IN.

PIN 13 SHOULD BE PULLED LOW WHEN THE CABLE IS PLUGGED IN.

FRONT PANEL JTAG

BLADE JTAG

BLADE_JTAG_TDI PG 7

VCC_M3V3 — R86 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

VCC_M3V3 — R82 10K 0603

U42 74LVC1G126 — R85 33 0603
U41 74LVC1G125 — R83 33 0603

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE MAIN BLADE OR THE EXTERNAL PROGRAMMER.

U38 74AUP1T34 — R72 33 0603
VCC_M1V8 — VCC_M3V3

BLADE JTAG

U40 74AUP1T34 — R81 33 0603 — BLADE_JTAG_TDO PG 7
VCC_M1V8 — VCC_M3V3

U66-43 FPGA_VU7P_B2104

JTAG

V_TDO — AC13 — TDO_0
V_TDI — AE15 — TDI_0

JUMPER_2X2 J13

BYPASS JUMPER

V_TMS_1V8 — AG15 — TMS_0
V_TCK_1V8 — AE13 — TCK_0

VU7P

U7 74LVC1G125 — R11 33 0603

VCC_M3V3 — C771 C766 C752 C747 C825 0.1 UF 0402 — GND
VCC_M3V3 — C812 C809 C803 C826 0.1 UF 0402 — GND

U65-11 FPGA_KU15P_A1760

JTAG

K_TDO — AK16 — TDO_0
K_TDI — AJ15 — TDI_0

JUMPER_2X2 J14

BYPASS JUMPER

K_TMS_1V8 — AJ17 — TMS_0
K_TCK_1V8 — AK15 — TCK_0

KU15P

VCC_M1V8 — C794 C786 C781 C778 C762 0.1 UF 0402 — GND
VCC_M1V8 — C761 C758 C755 C969 C971 0.1 UF 0402 — GND

TDI_1V8

U9 74LVC1G125 — R25 33 0603

U52-1 TM4C1290NCPDT

C_TDO — 97 — JTAG_TDO
C_TDI — 98 — JTAG_TDI

JUMPER_2X2 J15

BYPASS JUMPER

C_TMS_3V3 — 99 — JTAG_TMS
C_TCK_3V3 — 100 — JTAG_TCK

CONTROLLER

TDI_3V3

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.04: JTAG CHAIN		
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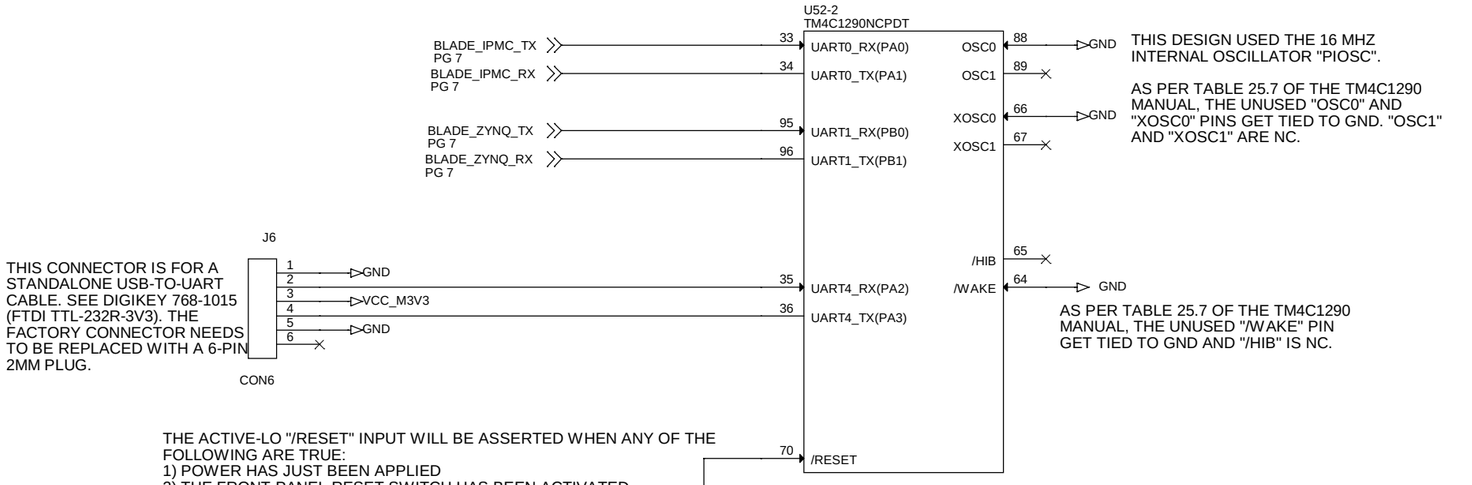

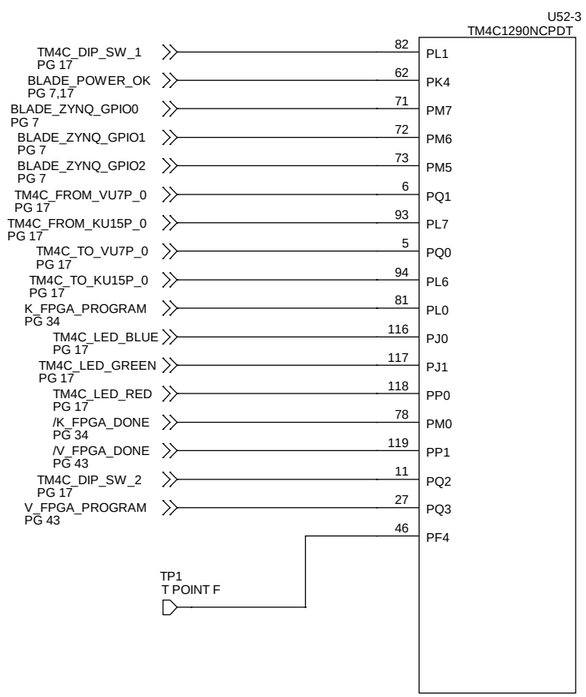

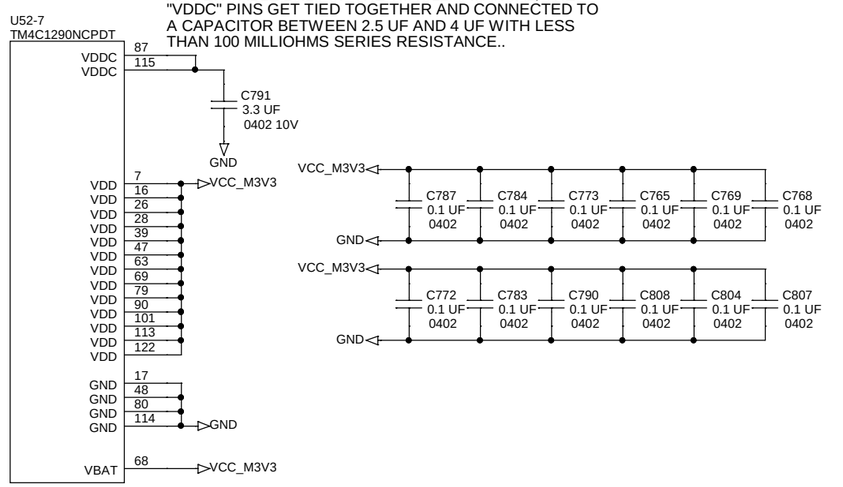

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.05 CONTROLLER		
Size	Document Number: 6089-103	Rev: A
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DO WE NEED TO ADD A BUFFER TO GET AN LHC-BASED CLOCK INTO THE FPGA LOGIC SECTION? WILL USING THE "TXOUTCLK" FROM A GTH/GTY BLOCK BE ADEQUATE?

U81-1
SI5340

bc_pLEGACY_CLK PG 14 — C1 0.1 UF 0402 — ac_pLEGACY_CLK
bc_nLEGACY_CLK PG 14 — C2 0.1 UF 0402 — ac_nLEGACY_CLK
R129 49.9 0402, R131 49.9 0402, C216 0.1 UF 0402 GND
bc_pLHC_CLK_IN PG 8 — C445 0.1 UF 0402 — ac_pLHC_CLK_IN
bc_nLHC_CLK_IN PG 8 — C446 0.1 UF 0402 — ac_nLHC_CLK_IN
R120 49.9 0402, R119 49.9 0402, C205 0.1 UF 0402 GND
bc_pHIGH_QUAL_CLK_IN PG 8 — C502 0.1 UF 0402 — ac_pHIGH_PERF_CLK_IN
bc_nHIGH_QUAL_CLK_IN PG 8 — C503 0.1 UF 0402 — ac_nHIGH_PERF_CLK_IN
R138 49.9 0402, R139 49.9 0402, C250 0.1 UF 0402 GND

pXTAL, X1, 48 MHz, nXTAL
XA, X1_SHIELD, X2_SHIELD, XB
FB_IN /FB_IN
IN_0 /IN_0, IN_1 /IN_1, IN_2 /IN_2
OUT_0 /OUT_0 — pSYNTH_CLK0 / nSYNTH_CLK0
OUT_1 /OUT_1 — pSYNTH_CLK1 / nSYNTH_CLK1
OUT_2 /OUT_2 — pSYNTH_CLK2 / nSYNTH_CLK2
OUT_3 /OUT_3 — pSYNTH_CLK3 / nSYNTH_CLK3

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

WE DO NOT HAVE AN UNUSED OUTPUT, SO WE CAN NOT USE FEEDBACK. ZERO-DELAY BUFFERING IS NOT A REQUIREMENT, NOR IS FIXED PHASE BETWEEN OUTPUTS.

U80
SI53340 1:2
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — pHIGH_PERF_CLK_BUF1 / nHIGH_PERF_CLK_BUF1
Q1 /Q1 — pHIGH_PERF_CLK_BUF0 / nHIGH_PERF_CLK_BUF0
Q2 /Q2, Q3 /QE
VDD — VCC_3V3
GND PAD — GND
R126 4.7K 0603 GND
C751 1 UF 0402 10v
<Implementation>

DC COUPLED LVDS
R121 100 0402
R110 100 0402

THE SPLIT TERMINATOR WITH A CAPACITOR TO GND IS USED FOR CLOCKS COMING FROM OFF THE BOARD. CLOCKS THAT ARE STRICTLY WITHIN THE BOARD USE SIMPLE 100 OHM TERMINATORS.

U61
SI53340 1:4
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — pHIGH_PERF_CLK0 / nHIGH_PERF_CLK0
Q1 /Q1 — pHIGH_PERF_CLK1 / nHIGH_PERF_CLK1
Q2 /Q2 — pHIGH_PERF_CLK2 / nHIGH_PERF_CLK2
Q3 /QE — pHIGH_PERF_CLK3 / nHIGH_PERF_CLK3
VDD — VCC_3V3
GND PAD — GND
R105 4.7K 0603 GND
C767 1 UF 0402 10v
<Implementation>

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

QUAD B

U83
SI53340 2:4
pHIGH_PERF_CLK0 / nHIGH_PERF_CLK0
pSYNTH_CLK0 / nSYNTH_CLK0
R127 100 0402, R132 100 0402
DC COUPLED LVDS
R135 4.7K 0603 GND
V_GTY1_SEL_SYNTH PG 27
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — bc_pV_CLK1_CHAN0 / bc_nV_CLK1_CHAN0
Q1 /Q1 — bc_pV_CLK1_CHAN1 / bc_nV_CLK1_CHAN1
Q2 /Q2 — bc_pV_CLK1_CHAN2 / bc_nV_CLK1_CHAN2
Q3 /QE — bc_pV_CLK1_CHAN3 / bc_nV_CLK1_CHAN3
VDD — VCC_3V3
GND PAD — GND
C754 1 UF 0402 10v
<Implementation>

AC COUPLED LVDS

C228 0.1 UF 0402	bc_pV_CLK1_CHAN0	ac_pV_CLK1_CHAN0 PG 61
C232 0.1 UF 0402	bc_nV_CLK1_CHAN0	ac_nV_CLK1_CHAN0 PG 61
C241 0.1 UF 0402	bc_pV_CLK1_CHAN1	ac_pV_CLK1_CHAN1 PG 63
C244 0.1 UF 0402	bc_nV_CLK1_CHAN1	ac_nV_CLK1_CHAN1 PG 63
C251 0.1 UF 0402	bc_pV_CLK1_CHAN2	ac_pV_CLK1_CHAN2 PG 66
C257 0.1 UF 0402	bc_nV_CLK1_CHAN2	ac_nV_CLK1_CHAN2 PG 66
C269 0.1 UF 0402	bc_pV_CLK1_CHAN3	ac_pV_CLK1_CHAN3 PG 67
C273 0.1 UF 0402	bc_nV_CLK1_CHAN3	ac_nV_CLK1_CHAN3 PG 67

QUAD D

QUAD G

QUAD I

THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.

QUAD L

U56
SI53340 2:4
pHIGH_PERF_CLK1 / nHIGH_PERF_CLK1
pSYNTH_CLK1 / nSYNTH_CLK1
R97 100 0402, R100 100 0402
DC COUPLED LVDS
R106 4.7K 0603 GND
V_GTY2_SEL_SYNTH PG 27
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — bc_pV_CLK1_CHAN4 / bc_nV_CLK1_CHAN4
Q1 /Q1 — bc_pV_CLK1_CHAN5 / bc_nV_CLK1_CHAN5
Q2 /Q2 — bc_pV_CLK1_CHAN6 / bc_nV_CLK1_CHAN6
Q3 /QE — bc_pV_CLK1_CHAN7 / bc_nV_CLK1_CHAN7
VDD — VCC_3V3
GND PAD — GND
C780 1 UF 0402 10v
<Implementation>

C149 0.1 UF 0402	bc_pV_CLK1_CHAN4	ac_pV_CLK1_CHAN4 PG 69
C151 0.1 UF 0402	bc_nV_CLK1_CHAN4	ac_nV_CLK1_CHAN4 PG 69
C158 0.1 UF 0402	bc_pV_CLK1_CHAN5	ac_pV_CLK1_CHAN5 PG 71
C160 0.1 UF 0402	bc_nV_CLK1_CHAN5	ac_nV_CLK1_CHAN5 PG 71
C162 0.1 UF 0402	bc_pV_CLK1_CHAN6	ac_pV_CLK1_CHAN6 PG 73
C166 0.1 UF 0402	bc_nV_CLK1_CHAN6	ac_nV_CLK1_CHAN6 PG 73
C172 0.1 UF 0402	bc_pV_CLK1_CHAN7	ac_pV_CLK1_CHAN7 PG 74
C174 0.1 UF 0402	bc_nV_CLK1_CHAN7	ac_nV_CLK1_CHAN7 PG 74

QUAD N

QUAD P

QUAD R

THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.

QUAD C

U87
SI53340 2:4
pHIGH_PERF_CLK2 / nHIGH_PERF_CLK2
pSYNTH_CLK2 / nSYNTH_CLK2
R147 100 0402, R143 100 0402
DC COUPLED LVDS
R140 4.7K 0603 GND
K_GTH_SEL_SYNTH PG 27
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — bc_pK_CLK1_CHAN0 / bc_nK_CLK1_CHAN0
Q1 /Q1 — bc_pK_CLK1_CHAN1 / bc_nK_CLK1_CHAN1
Q2 /Q2 — bc_pK_CLK1_CHAN2 / bc_nK_CLK1_CHAN2
Q3 /QE — SPARE
VDD — VCC_3V3
GND PAD — GND
C736 1 UF 0402 10v
<Implementation>

AC COUPLED LVDS

C286 0.1 UF 0402	bc_pK_CLK1_CHAN0	ac_pK_CLK1_CHAN0 PG 50
C281 0.1 UF 0402	bc_nK_CLK1_CHAN0	ac_nK_CLK1_CHAN0 PG 50
C270 0.1 UF 0402	bc_pK_CLK1_CHAN1	ac_pK_CLK1_CHAN1 PG 51
C264 0.1 UF 0402	bc_nK_CLK1_CHAN1	ac_nK_CLK1_CHAN1 PG 51
C252 0.1 UF 0402	bc_pK_CLK1_CHAN2	ac_pK_CLK1_CHAN2 PG 52
C249 0.1 UF 0402	bc_nK_CLK1_CHAN2	ac_nK_CLK1_CHAN2 PG 52

QUAD F

QUAD I

THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.

U68
SI53340 2:4
pHIGH_PERF_CLK3 / nHIGH_PERF_CLK3
pSYNTH_CLK3 / nSYNTH_CLK3
R125 100 0402, R117 100 0402
DC COUPLED LVDS
R114 4.7K 0603 GND
K_GTY_SEL_SYNTH PG 27
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — bc_pK_CLK1_CHAN4 / bc_nK_CLK1_CHAN4
Q1 /Q1 — bc_pK_CLK1_CHAN5 / bc_nK_CLK1_CHAN5
Q2 /Q2 — bc_pK_CLK1_CHAN6 / bc_nK_CLK1_CHAN6
Q3 /QE
VDD — VCC_3V3
GND PAD — GND
C759 1 UF 0402 10v
<Implementation>

C211 0.1 UF 0402	bc_pK_CLK1_CHAN4	ac_pK_CLK1_CHAN4 PG 54
C204 0.1 UF 0402	bc_nK_CLK1_CHAN4	ac_nK_CLK1_CHAN4 PG 54
C200 0.1 UF 0402	bc_pK_CLK1_CHAN5	ac_pK_CLK1_CHAN5 PG 56
C191 0.1 UF 0402	bc_nK_CLK1_CHAN5	ac_nK_CLK1_CHAN5 PG 56
C189 0.1 UF 0402	bc_pK_CLK1_CHAN6	ac_pK_CLK1_CHAN6 PG 58
C181 0.1 UF 0402	bc_nK_CLK1_CHAN6	ac_nK_CLK1_CHAN6 PG 58

QUAD M

QUAD P

QUAD R

THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.

AC COUPLED LVDS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.06: LHC CLOCKING

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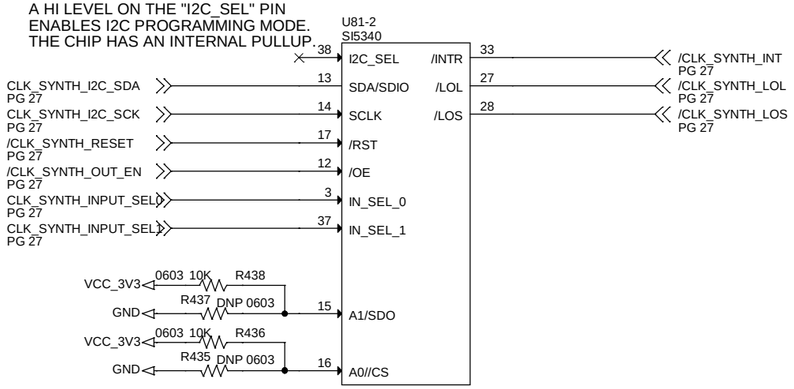
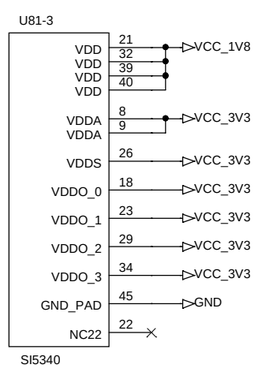
A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

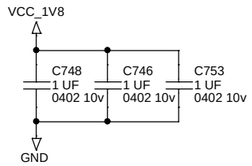


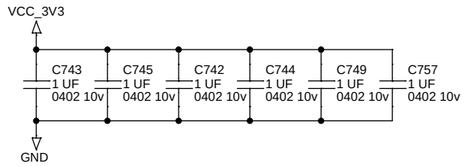
SI5340 I2C ADDRESS:
READ OR WRITE
1 1 1 0 1 A1 A0
RANGE: 0X74 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.







ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.07: LHC CLOCKING SUPPORT		
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THIS CIRCUIT ON THIS PAGE IS FOR USE IN THE PROTOTYPE ONLY. IT ALLOWS US TO FEED LEGACY TTC SIGNALS INTO THE SYSTEM.

U13-2
SFP_CONN_WITH_CAGE

U13-1
SFP_CONN_WITH_CAGE

THE SFP I2C SIGNALS AND CONTROL LINES ARE WIRED TO THE CHIPS THAT SUPPORT ACCESS TO THE KU15P OPTICS. THEY CAN BE CONNECTED ELSEWHERE IF DESIRED.

SFP+ CONNECTOR TO RECEIVE ENCODED TTC CLOCK/DATA STREAM.

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTS_OUT" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS WILL GENERATE THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

J11
JUMPER_DIFF

THESE RESISTORS MUST BE NEAR THE 65LVDS100 INPUT PINS.

U12
NB7V52M

U8
65LVDS100

DC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J10
JUMPER_DIFF

THIS JUMPER ALLOWS DIRECT CONNECTION OF "CDR_DATA" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

THIS BUFFER CONVERTS 2.5V CML SIGNALS TO LVDS LEVELS THAT ARE COMPATABLE WITH ULTRASCALE "HP" BANK INPUTS.

U14
ADN2814

THE CLOCK POLARITY IS INVERTED.

U11
SY89832U

THIS DIVIDER NETWORK PROVIDES A DIFFERENTIAL VOLTAGE OF 0.83 VOLTS. IT HOLDS THE RESET INPUT AT A "FALSE" VALUE.

U10
SY89872

S1=0, S0=1 -> B=INPUT/4

AC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J9
JUMPER_DIFF

AC COUPLED LVDS

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTC_CLK40" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS CLOCK, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

PLACE ONE OF EACH VALUE NEAR PINS 2, 12, 18, 24, AND 31.

THIS DESIGN ONLY USES 2,5 VOLTS FOR LEGACY TTC SUPPORT. IT DOES NOT NEED A DC-DC CONVERTER SUPPLY.

U19
LT1963A

Title	ATCA FPGA BOARD, KU15P AND VU7P, MK1
	2.08: LEGACY TTC
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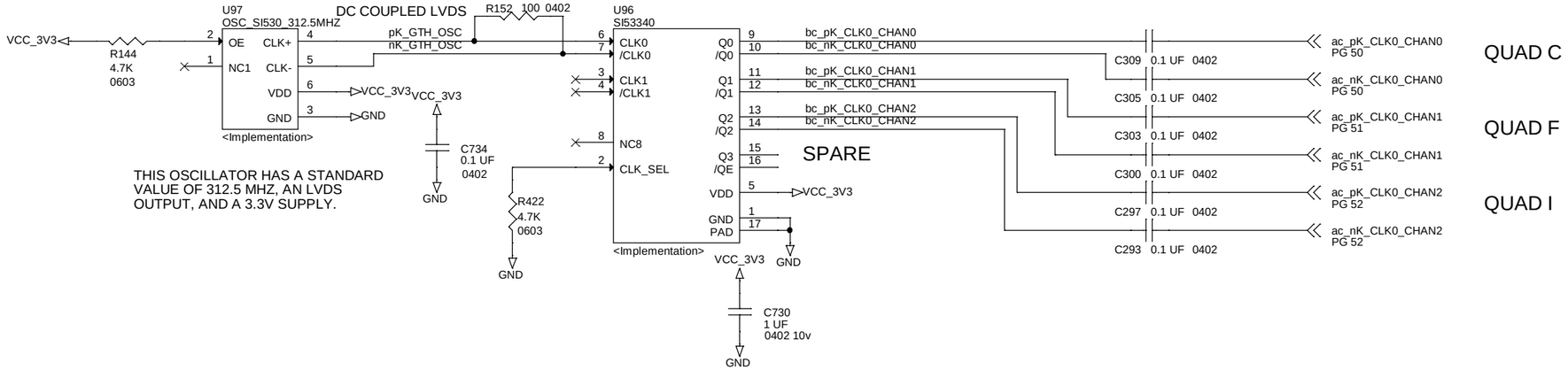
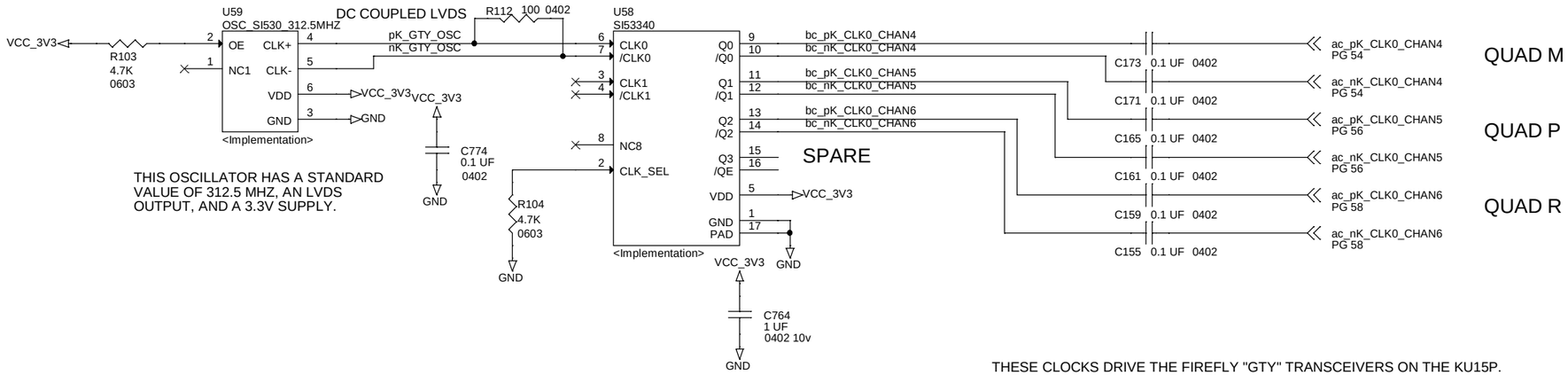
AC COUPLED LVDS

bc = BEFORE CAPACITOR

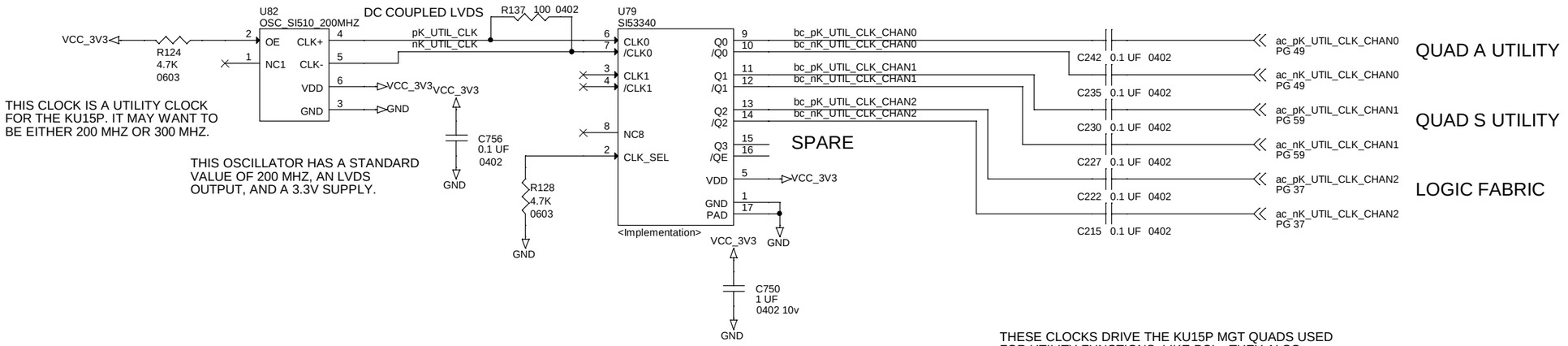
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.



THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.



THESE CLOCKS DRIVE THE KU15P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.09: KU15P OSCILLATOR CLOCKING

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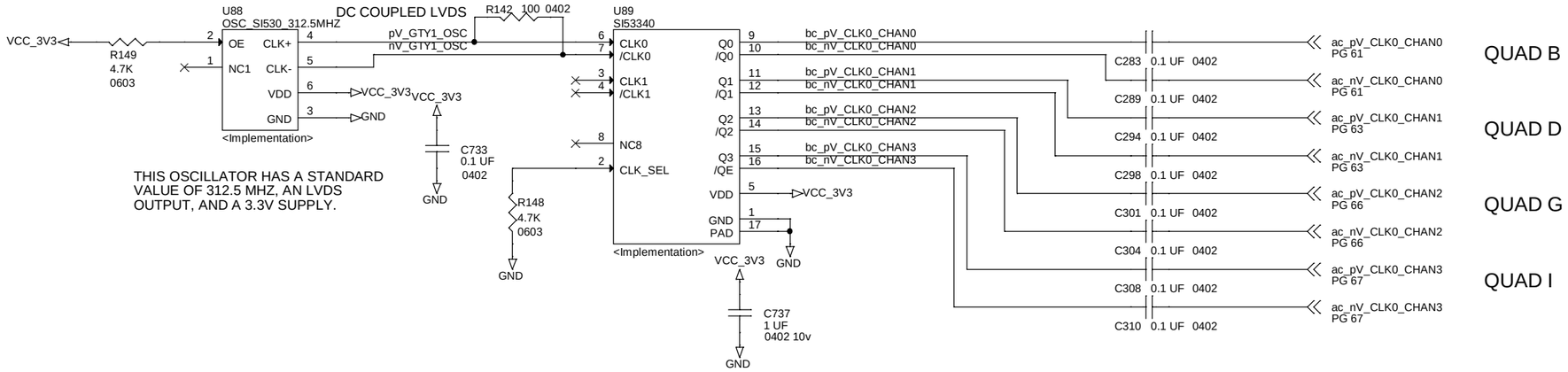
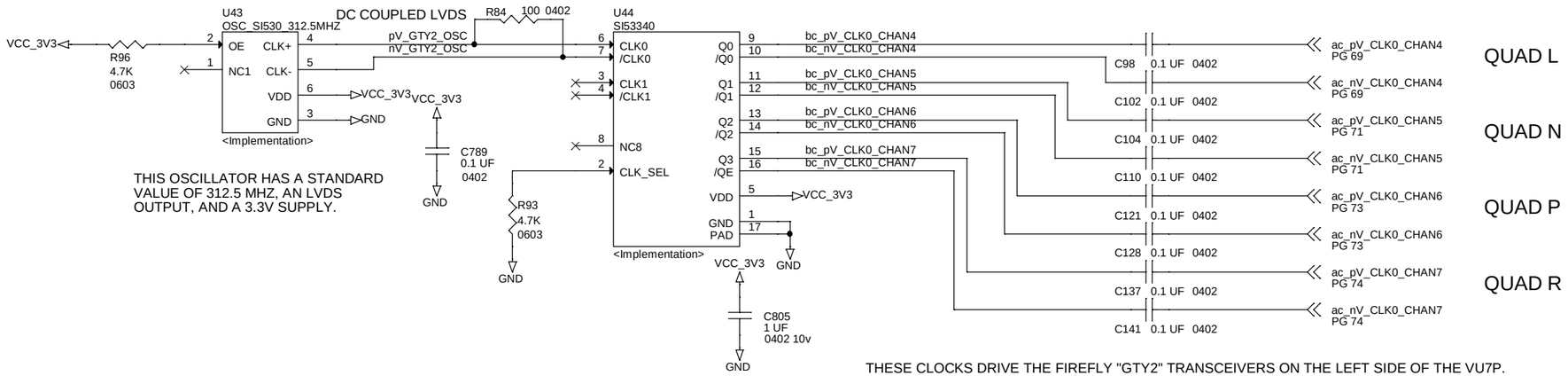
AC COUPLED LVDS

bc = BEFORE CAPACITOR

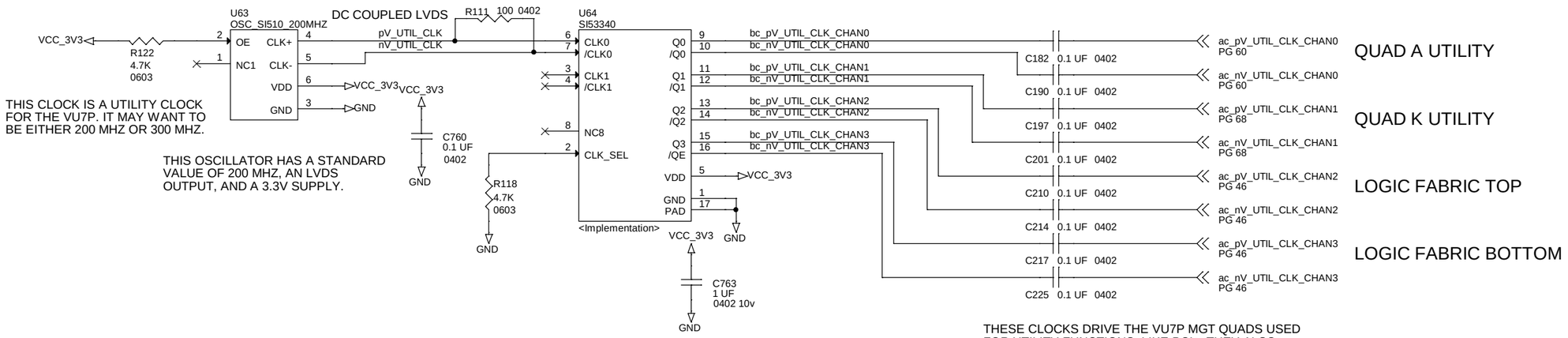
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.



THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.



THESE CLOCKS DRIVE THE VU7P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.10: VU7P OSCILLATOR CLOCKING		
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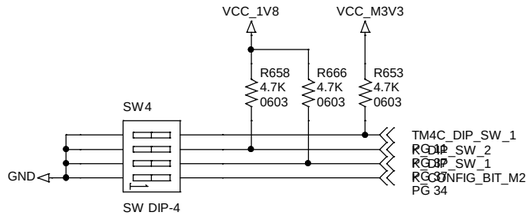
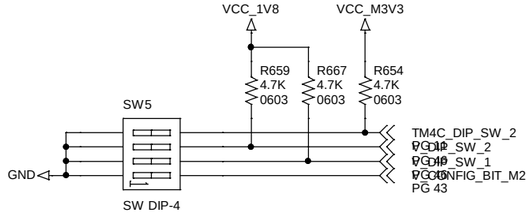
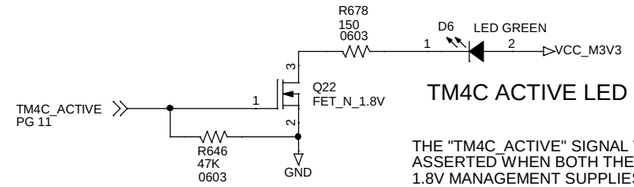


KU15P DIP SWITCH

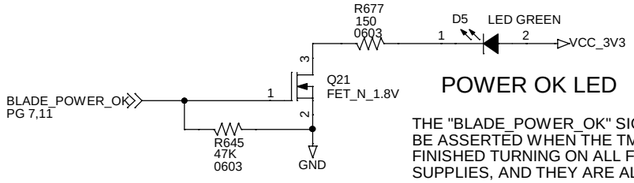


VU7P DIP SWITCH



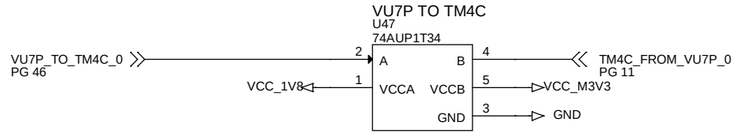
TM4C ACTIVE LED

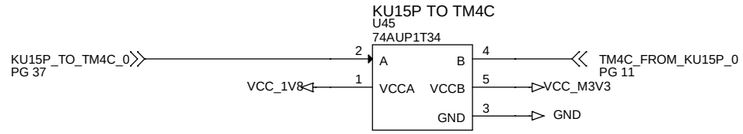
THE "TM4C_ACTIVE" SIGNAL WILL BE ASSERTED WHEN BOTH THE 3.3V AND 1.8V MANAGEMENT SUPPLIES ARE GOOD, THE "ENABLE" SIGNAL FROM THE SERVICE BLADE IS HIGH, AND THE "RESET" SWITCH IS NOT ACTIVATED.

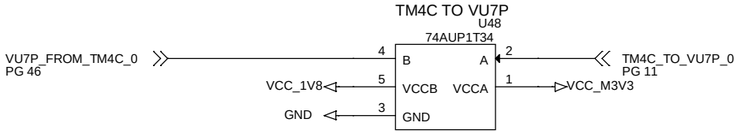


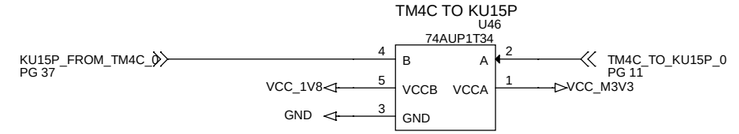
POWER OK LED

THE "BLADE_POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE TM4C HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

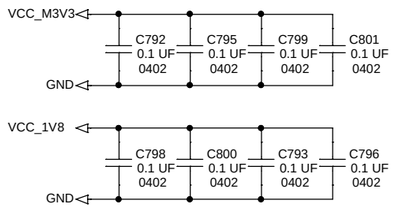




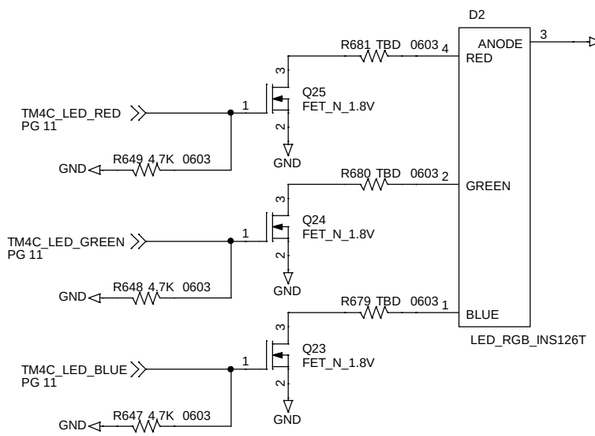




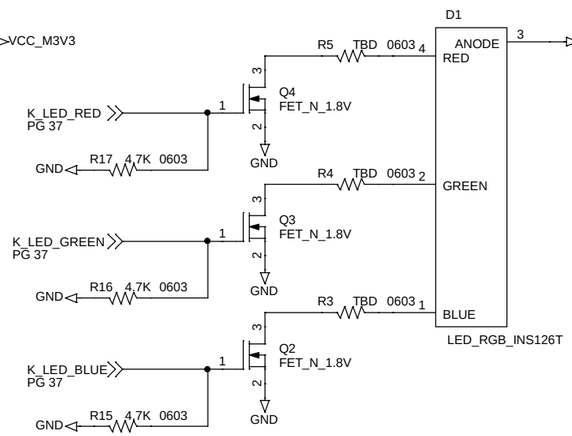
UTILITY CONNECTIONS BETWEEN THE TM4C CONTROLLER AND THE FPGAS. THE LEVEL TRANSLATORS ARE UNI-DIRECTIONAL.



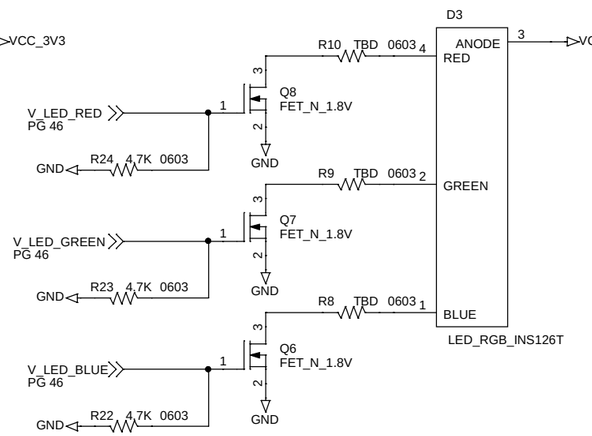
TM4C CONTROLLER LED



KU15P LED



VU7P LED



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.11: LEDS, SWITCHES, LEVEL SHIFTERS		
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U69
K_VCCINT_PG_A_1 PG 20
K_VCCINT_PG_A_2 PG 20
K_VCCINT_PG_A
VCC_M3V3
GND
74LVC1G08

U70
K_VCCINT_PG_B_1 PG 20
K_VCCINT_PG_B_2 PG 20
K_VCCINT_PG_B
74LVC1G08

U75
V_VCCINT_PG_A_1 PG 22
V_VCCINT_PG_A_2 PG 22
V_VCCINT_PG_A
74LVC1G08

U76
V_VCCINT_PG_B_1 PG 22
V_VCCINT_PG_B_2 PG 22
V_VCCINT_PG_B
74LVC1G08

USE 2-INPUT "AND" GATES TO COMBINE "PG" PINS FROM THE SAME MODULE AND SAVE CONTROLLER PINS

U52-6
TM4C1290NCPDT

K_VCCINT_PG_A	61	PK5	PF2	44	CTRL_K_VCCINT_PWR_EN
K_VCCINT_PG_B	60	PK6			
V_VCCINT_PG_A	32	PH3	PA4	37	CTRL_V_VCCINT_PWR_EN
V_VCCINT_PG_B	31	PH2	PP4	105	TP3 T POINT F
			PP3	104	TP2 T POINT F
VCC_3V3_PG PG 19	30	PH1	PF1	43	CTRL_VCC_3V3_PWR_EN
VCC_1V8_PG PG 19	29	PH0	PA5	38	CTRL_VCC_1V8_PWR_EN
			PN5	112	CTRL_V_MGTY1_VCCAUX_EN
			PN4	111	CTRL_V_MGTY2_VCCAUX_EN
			PL2	83	CTRL_K_MGTY_VCCAUX_EN
			PL3	84	CTRL_K_MGTH_VCCAUX_EN
K_MGTY_AVCC_OK PG 21	76	PM2	PL4	85	CTRL_K_MGTY_AVCC_PWR_EN
K_MGTH_AVCC_OK PG 21	75	PM3	PL5	86	CTRL_K_MGTH_AVCC_PWR_EN
K_MGTY_AVTT_OK PG 21	77	PM1	PQ4	102	CTRL_K_MGTY_AVTT_PWR_EN
K_MGTH_AVTT_OK PG 21	74	PM4	PP2	103	CTRL_K_MGTH_AVTT_PWR_EN
V_MGTY2_AVTT_OK PG 23	25	PC4	PN0	107	CTRL_V_MGTY2_AVTT_PWR_EN
V_MGTY1_AVTT_OK PG 23	22	PC7	PN1	108	CTRL_V_MGTY1_AVTT_PWR_EN
V_MGTY2_AVCC_OK PG 23	24	PC5	PN2	109	CTRL_V_MGTY2_AVCC_PWR_EN
V_MGTY1_AVCC_OK PG 23	23	PC6	PN3	110	CTRL_V_MGTY1_AVCC_PWR_EN

U71
CTRL_K_VCCINT_PWR_EN
R454 4.7K 0603
K_VCCINT_PWR_EN PG 20
74LVC1G08

U74
CTRL_V_VCCINT_PWR_EN
R457 4.7K 0603
V_VCCINT_PWR_EN PG 22
74LVC1G08

U72
CTRL_VCC_3V3_PWR_EN
R455 4.7K 0603
VCC_3V3_PWR_EN PG 19
74LVC1G08

U73
CTRL_VCC_1V8_PWR_EN
R456 4.7K 0603
VCC_1V8_PWR_EN PG 19
74LVC1G08

Q15
CTRL_V_MGTY1_VCCAUX_EN
R498 4.7K 0603
/V_MGTY1_VCCAUX_EN PG 42

Q13
CTRL_V_MGTY2_VCCAUX_EN
R405 4.7K 0603
/V_MGTY2_VCCAUX_EN PG 42

Q16
CTRL_K_MGTY_VCCAUX_EN
R501 4.7K 0603
/K_MGTY_VCCAUX_EN PG 33

Q14
CTRL_K_MGTH_VCCAUX_EN
R460 4.7K 0603
/K_MGTH_VCCAUX_EN PG 33

THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN VCC_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

Q17
CTRL_K_MGTY_AVCC_PWR_EN
R591 4.7K 0603
/K_MGTY_AVCC_PWR_EN PG 21

Q9
CTRL_K_MGTH_AVCC_PWR_EN
R313 4.7K 0603
/K_MGTH_AVCC_PWR_EN PG 21

Q18
CTRL_K_MGTY_AVTT_PWR_EN
R594 4.7K 0603
/K_MGTY_AVTT_PWR_EN PG 21

Q10
CTRL_K_MGTH_AVTT_PWR_EN
R316 4.7K 0603
/K_MGTH_AVTT_PWR_EN PG 21

Q12
CTRL_V_MGTY2_AVTT_PWR_EN
R322 4.7K 0603
/V_MGTY2_AVTT_PWR_EN PG 23

Q20
CTRL_V_MGTY1_AVTT_PWR_EN
R600 4.7K 0603
/V_MGTY1_AVTT_PWR_EN PG 23

Q11
CTRL_V_MGTY2_AVCC_PWR_EN
R319 4.7K 0603
/V_MGTY2_AVCC_PWR_EN PG 23

Q19
CTRL_V_MGTY1_AVCC_PWR_EN
R597 4.7K 0603
/V_MGTY1_AVCC_PWR_EN PG 23

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. A VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

SPREAD THESE CAPACITORS AROUND THE BOARD

VCC_M3V3
C960 22 UF 6.3V 0603
C858 22 UF 6.3V 0603
C479 22 UF 6.3V 0603
C548 22 UF 6.3V 0603
GND

VCC_M1V8
C829 22 UF 6.3V 0603
C968 22 UF 6.3V 0603
GND

U31
TPS82130
VCC_12V
C15 10 UF 16V 0805
C834 3.3 NF 50V 0603
VIN
EN
SS/TR
VOUT
VOUT
FB
PG
GND
PAD
R28 110K 0603 0.1%
R29 34.8K 0603 0.1%
C52 22 UF 6.3V 0603
VCC_M3V3

THE VOLTAGE IS 3.33 VOLTS WITH RESISTORS OF 110K AND 34.8K.

VCC_M3V3 AND VCC_M1V8 ARE THE "MANAGEMENT" POWER. THEY PROVIDE POWER TO THE POWER SEQUENCING CIRCUIT. THEY ARE ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

U90
ADP1713_1V8
EN
IN
OUT
BYP
GND
C731 4.7 UF 0402
C732 0.1 UF 0402
C271 0.01 UF 0402
C272 4.7 UF 0402
C260 0.1 UF 0402
VCC_M1V8

Title	ATCA FPGA BOARD, KU15P AND VU7P, MK1
	3.01: POWER CONTROL
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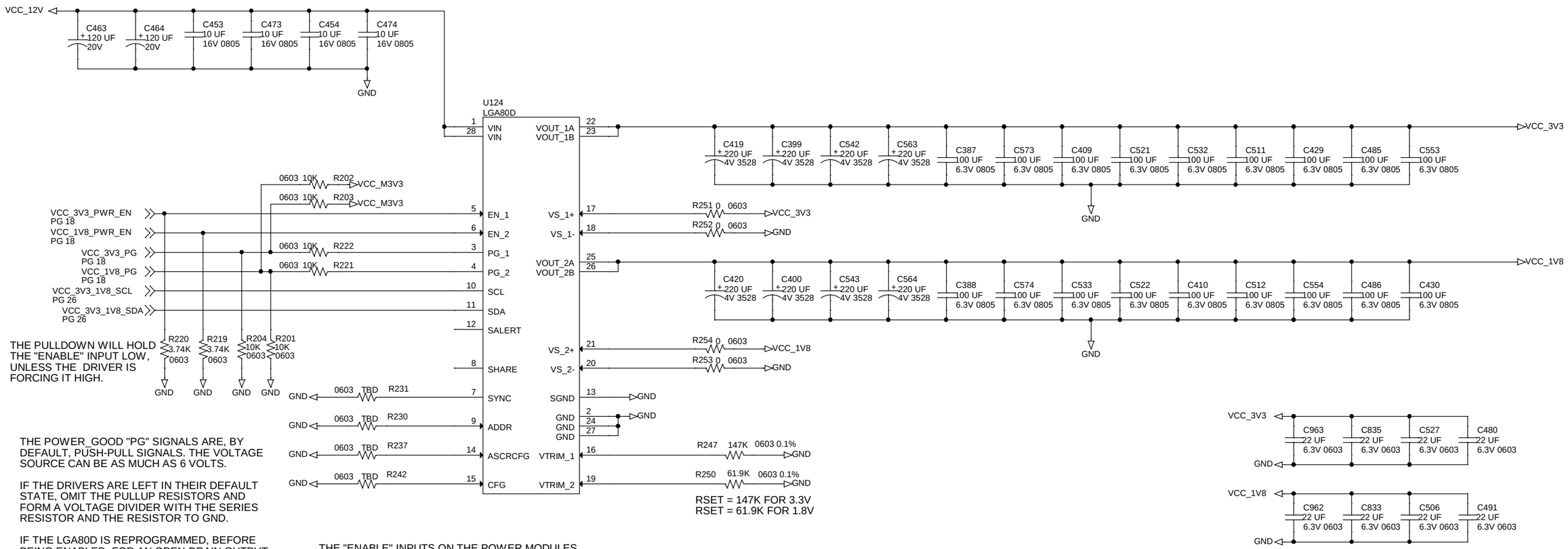

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.02: POWER GLOBAL 3.3V AND 1.8V

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KU15P VCCINT MUST BE 0.85V.

U122
LGA80D

VCC_12V

C459 +120 UF 20V
C460 +120 UF 20V
C449 10 UF 16V 0805
C469 10 UF 16V 0805
C450 10 UF 16V 0805
C470 10 UF 16V 0805

GND

1 VIN
28 VIN
A
22 VOUT_1A
23 VOUT_1B

C415 +330 UF 2.5V 3528
C393 +330 UF 2.5V 3528
C538 +330 UF 2.5V 3528
C559 +330 UF 2.5V 3528
C425 100 UF 4V 0805
C405 100 UF 4V 0805
C528 100 UF 4V 0805
C550 100 UF 4V 0805
C383 100 UF 4V 0805
C569 100 UF 4V 0805
C481 100 UF 4V 0805
C507 100 UF 4V 0805
C517 100 UF 4V 0805

GND

K_VCCINT

5 EN_1
0603 10K R194 VCC_M3V3
6 EN_2
0603 10K R195 VCC_M3V3
3 PG_1
0603 10K R216 K_VCCINT_PG_A_1 PG 18
4 PG_2
0603 10K R215 K_VCCINT_PG_A_2 PG 18
10 SCL
K_VCCINT_A_SCL PG 26
11 SDA
K_VCCINT_A_SDA PG 26
12 SALERT
R196 10K 0603
R193 10K 0603
GND GND
8 SHARE
7 SYNC
K_VCCINT_PWR_EN PG 18
9 ADDR
R213 3.74K 0603
GND
14 ASCRCFG
15 CFG

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

0603 TBD R227 GND
0603 TBD R235 GND
0603 TBD R240 GND

17 VS_1+
R191 0 0603 K_VCCINT
18 VS_1-
R192 0 0603 GND
25 VOUT_2A
26 VOUT_2B

C416 +330 UF 2.5V 3528
C394 +330 UF 2.5V 3528
C539 +330 UF 2.5V 3528
C560 +330 UF 2.5V 3528
C426 100 UF 4V 0805
C406 100 UF 4V 0805
C529 100 UF 4V 0805
C551 100 UF 4V 0805
C384 100 UF 4V 0805
C570 100 UF 4V 0805
C482 100 UF 4V 0805
C508 100 UF 4V 0805
C518 100 UF 4V 0805

GND

21 VS_2+
20 VS_2-
13 SGND GND
2 GND
24 GND
27 GND
GND
16 VTRIM_1
R245 16.2K 0603 0.1% GND
19 VTRIM_2

RSET = 16.2K FOR 0.85V

U123
LGA80D

C461 +120 UF 20V
C462 +120 UF 20V
C451 10 UF 16V 0805
C471 10 UF 16V 0805
C452 10 UF 16V 0805
C472 10 UF 16V 0805

GND

1 VIN
28 VIN
B
22 VOUT_1A
23 VOUT_1B

C417 +330 UF 2.5V 3528
C396 +330 UF 2.5V 3528
C540 +330 UF 2.5V 3528
C561 +330 UF 2.5V 3528
C427 100 UF 4V 0805
C407 100 UF 4V 0805
C530 100 UF 4V 0805
C552 100 UF 4V 0805
C385 100 UF 4V 0805
C571 100 UF 4V 0805
C519 100 UF 4V 0805
C509 100 UF 4V 0805
C483 100 UF 4V 0805

GND

5 EN_1
0603 10K R198 VCC_M3V3
6 EN_2
0603 10K R199 VCC_M3V3
3 PG_1
0603 10K R218 K_VCCINT_PG_B_1 PG 18
4 PG_2
0603 10K R217 K_VCCINT_PG_B_2 PG 18
10 SCL
K_VCCINT_B_SCL PG 26
11 SDA
K_VCCINT_B_SDA PG 26
12 SALERT
R200 10K 0603
R197 10K 0603
GND GND
8 SHARE
7 SYNC
9 ADDR
14 ASCRCFG
15 CFG

0603 TBD R229 GND
0603 TBD R228 GND
0603 TBD R236 GND
0603 TBD R241 GND

17 VS_1+
18 VS_1-
25 VOUT_2A
26 VOUT_2B

C418 +330 UF 2.5V 3528
C397 +330 UF 2.5V 3528
C541 +330 UF 2.5V 3528
C562 +330 UF 2.5V 3528
C428 100 UF 4V 0805
C408 100 UF 4V 0805
C531 100 UF 4V 0805
C549 100 UF 4V 0805
C386 100 UF 4V 0805
C572 100 UF 4V 0805
C520 100 UF 4V 0805
C510 100 UF 4V 0805
C484 100 UF 4V 0805

GND

21 VS_2+
20 VS_2-
13 SGND GND
2 GND
24 GND
27 GND
GND
16 VTRIM_1
R246 16.2K 0603 0.1% GND
19 VTRIM_2

RSET = 16.2K FOR 0.85V

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.03: POWER SOURCE KU15P INTERNAL

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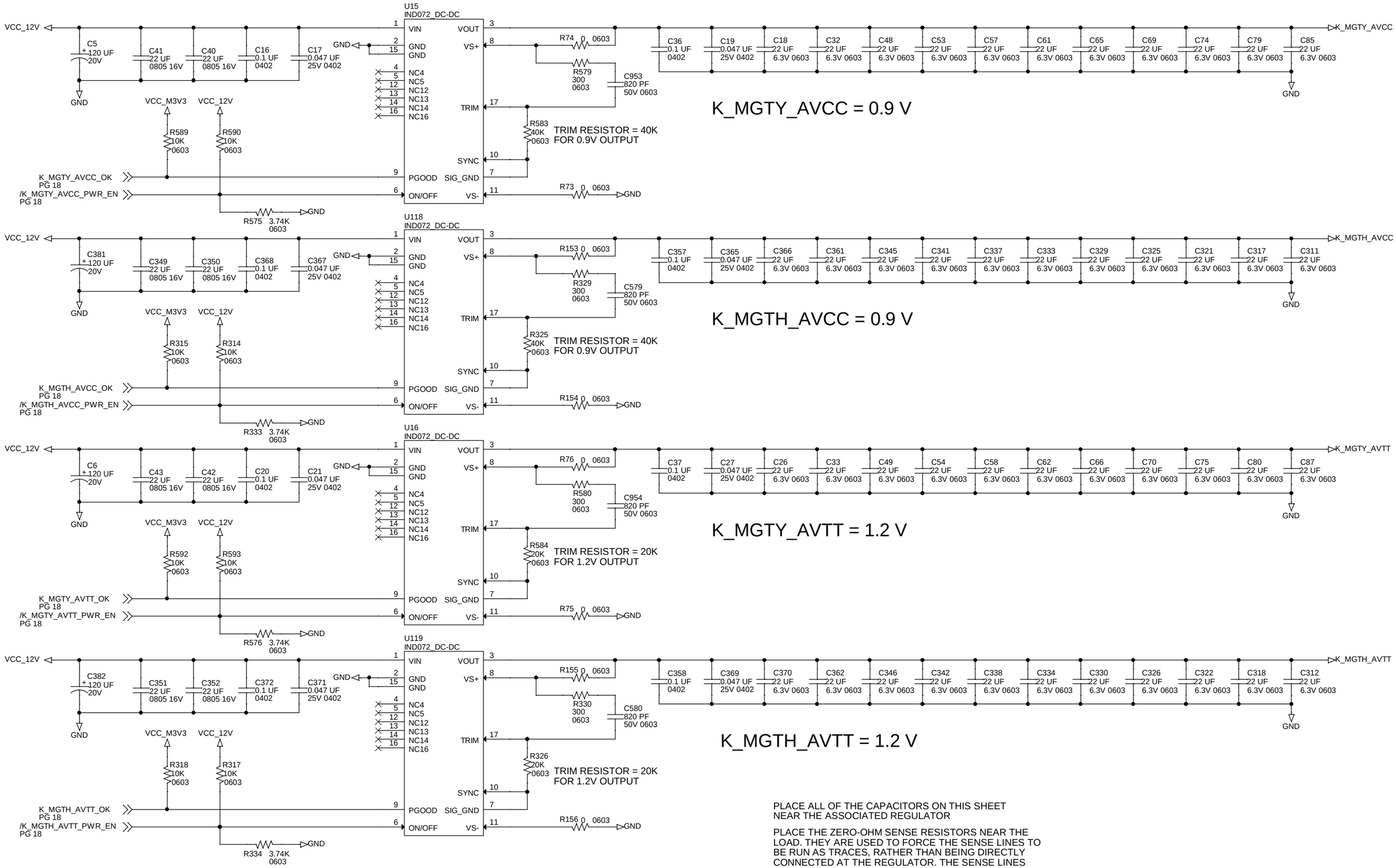

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.04: POWER SOURCE KU15P MGT XCVR

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VU7P VCCINT MUST BE 0.85V.

VCC_12V

C465 120 UF 20V, C466 120 UF 20V, C455 10 UF 16V 0805, C475 10 UF 16V 0805, C456 10 UF 16V 0805, C476 10 UF 16V 0805

GND

U125
LGA80D

A

1	VIN	VOUT_1A	22
28	VIN	VOUT_1B	23
5	EN_1	VS_1+	17
6	EN_2	VS_1-	18
3	PG_1		
4	PG_2	VOUT_2A	25
		VOUT_2B	26
10	SCL		
11	SDA		
12	SALERT		
		VS_2+	21
8	SHARE	VS_2-	20
7	SYNC	SGND	13
9	ADDR	GND	2
		GND	24
		GND	27
14	ASCRCFG	VTRIM_1	16
15	CFG	VTRIM_2	19

C421 330 UF 2.5V 3528, C401 330 UF 2.5V 3528, C544 330 UF 2.5V 3528, C565 330 UF 2.5V 3528, C431 100 UF 6.3V 0805, C411 100 UF 6.3V 0805, C534 100 UF 6.3V 0805, C555 100 UF 6.3V 0805, C389 100 UF 6.3V 0805, C575 100 UF 6.3V 0805, C523 100 UF 6.3V 0805, C513 100 UF 6.3V 0805, C487 100 UF 6.3V 0805

GND

V_VCCINT

0603 10K R206 VCC_M3V3
0603 10K R207 VCC_M3V3
0603 10K R224
0603 10K R223

R256 0 0603 V_VCCINT
R255 0 0603 GND

V_VCCINT_PG_A_1 PG 18
V_VCCINT_PG_A_2 PG 18
V_VCCINT_A_SCL PG 26
V_VCCINT_A_SDA PG 26

R208 10K 0603, R205 10K 0603

GND GND

C402 330 UF 2.5V 3528, C422 330 UF 2.5V 3528, C566 330 UF 2.5V 3528, C545 330 UF 2.5V 3528, C432 100 UF 6.3V 0805, C412 100 UF 6.3V 0805, C535 100 UF 6.3V 0805, C556 100 UF 6.3V 0805, C390 100 UF 6.3V 0805, C576 100 UF 6.3V 0805, C524 100 UF 6.3V 0805, C514 100 UF 6.3V 0805, C488 100 UF 6.3V 0805

GND

V_VCCINT_PWR_EN PG 18

R214 3.74K 0603

GND

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

GND 0603 TBD R232
GND 0603 TBD R238
GND 0603 TBD R243

R248 16.2K 0603 0.1% GND

RSET = 16.2K FOR 0.85V

U126
LGA80D

B

1	VIN	VOUT_1A	22
28	VIN	VOUT_1B	23
5	EN_1	VS_1+	17
6	EN_2	VS_1-	18
3	PG_1		
4	PG_2	VOUT_2A	25
		VOUT_2B	26
10	SCL		
11	SDA		
12	SALERT		
		VS_2+	21
8	SHARE	VS_2-	20
7	SYNC	SGND	13
9	ADDR	GND	2
		GND	24
		GND	27
14	ASCRCFG	VTRIM_1	16
15	CFG	VTRIM_2	19

C467 120 UF 20V, C468 120 UF 20V, C457 10 UF 16V 0805, C477 10 UF 16V 0805, C458 10 UF 16V 0805, C478 10 UF 16V 0805

GND

C423 330 UF 2.5V 3528, C403 330 UF 2.5V 3528, C546 330 UF 2.5V 3528, C567 330 UF 2.5V 3528, C433 100 UF 6.3V 0805, C413 100 UF 6.3V 0805, C536 100 UF 6.3V 0805, C557 100 UF 6.3V 0805, C391 100 UF 6.3V 0805, C577 100 UF 6.3V 0805, C525 100 UF 6.3V 0805, C515 100 UF 6.3V 0805, C489 100 UF 6.3V 0805

GND

0603 10K R210 VCC_M3V3
0603 10K R211 VCC_M3V3
0603 10K R226
0603 10K R225

V_VCCINT_PG_B_1 PG 18
V_VCCINT_PG_B_2 PG 18
V_VCCINT_B_SCL PG 26
V_VCCINT_B_SDA PG 26

R212 10K 0603, R209 10K 0603

GND GND

C424 330 UF 2.5V 3528, C404 330 UF 2.5V 3528, C568 330 UF 2.5V 3528, C547 330 UF 2.5V 3528, C434 100 UF 6.3V 0805, C414 100 UF 6.3V 0805, C537 100 UF 6.3V 0805, C558 100 UF 6.3V 0805, C392 100 UF 6.3V 0805, C578 100 UF 6.3V 0805, C490 100 UF 6.3V 0805, C516 100 UF 6.3V 0805, C526 100 UF 6.3V 0805

GND

GND 0603 TBD R234
GND 0603 TBD R233
GND 0603 TBD R239
GND 0603 TBD R244

R249 16.2K 0603 0.1% GND

RSET = 16.2K FOR 0.85V

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.05: POWER SOURCE VU7P INTERNAL

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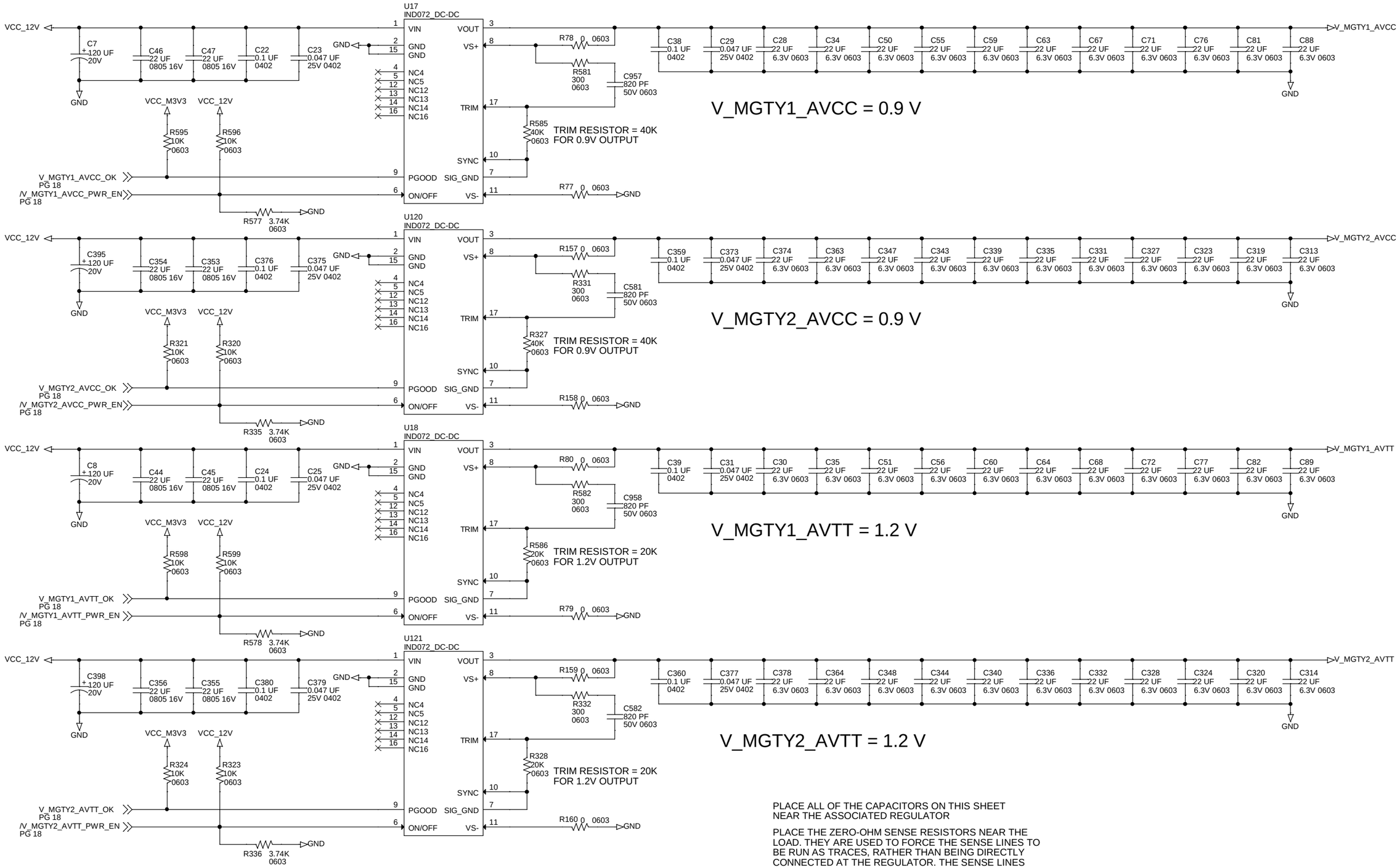

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 3.06: POWER SOURCE VU7P MGT XCVR		
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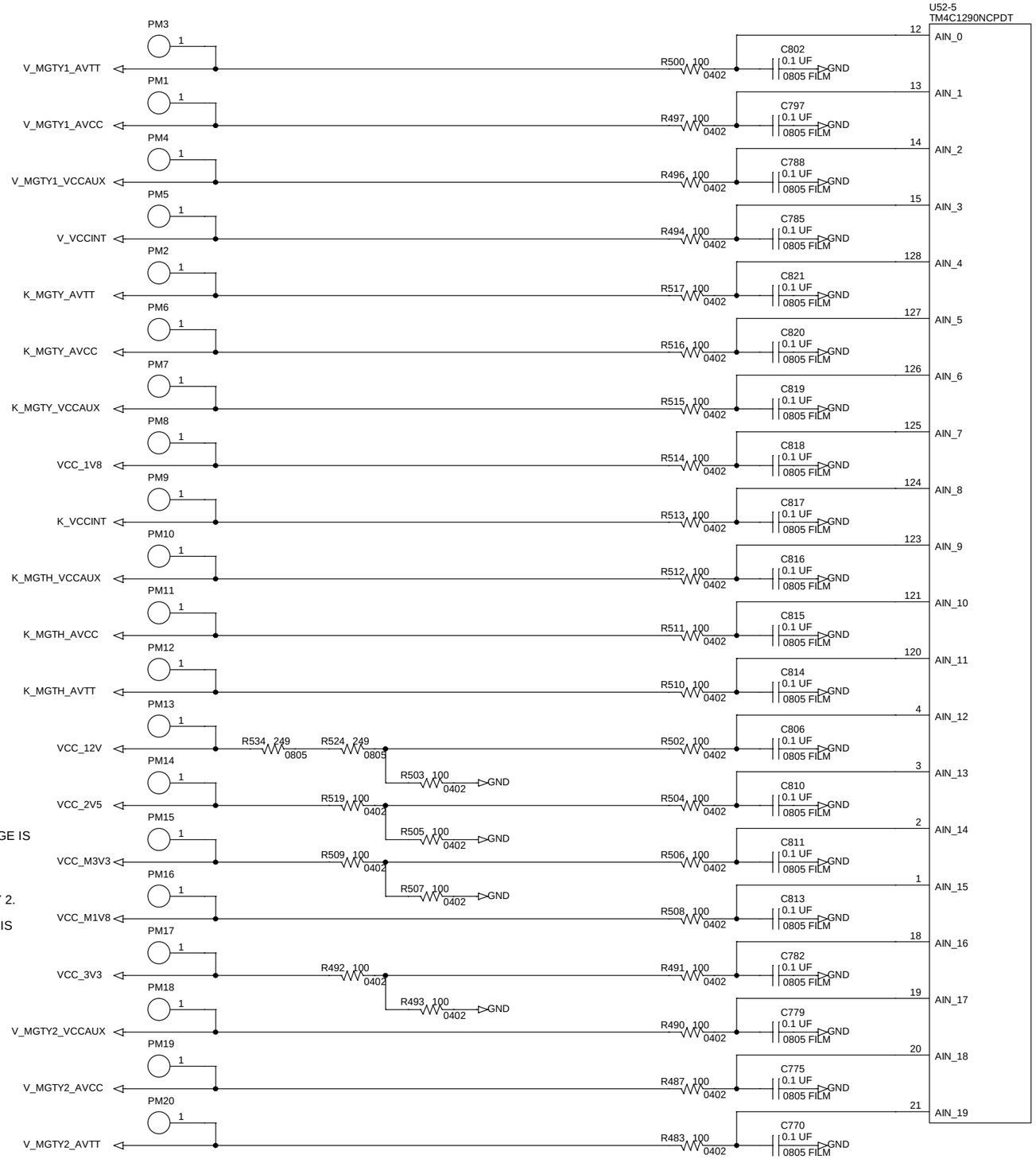

THE FULL SCALE ADC VOLTAGE IS 2.5 VOLTS, AS SET BY THE VOLTAGE REFERENCE.

THE 2.5 VOLT AND 3.3 VOLT SUPPLY LEVEL IS DIVIDED BY 2.

THE 12 VOLT SUPPLY LEVEL IS DIVIDED BY 6.

TEST POINTS TO MEASURE VOLTAGES

PM21 PM22 PM23 PM24 PM25 PM26 — 1 — GND

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.07: POWER MEASUREMENT

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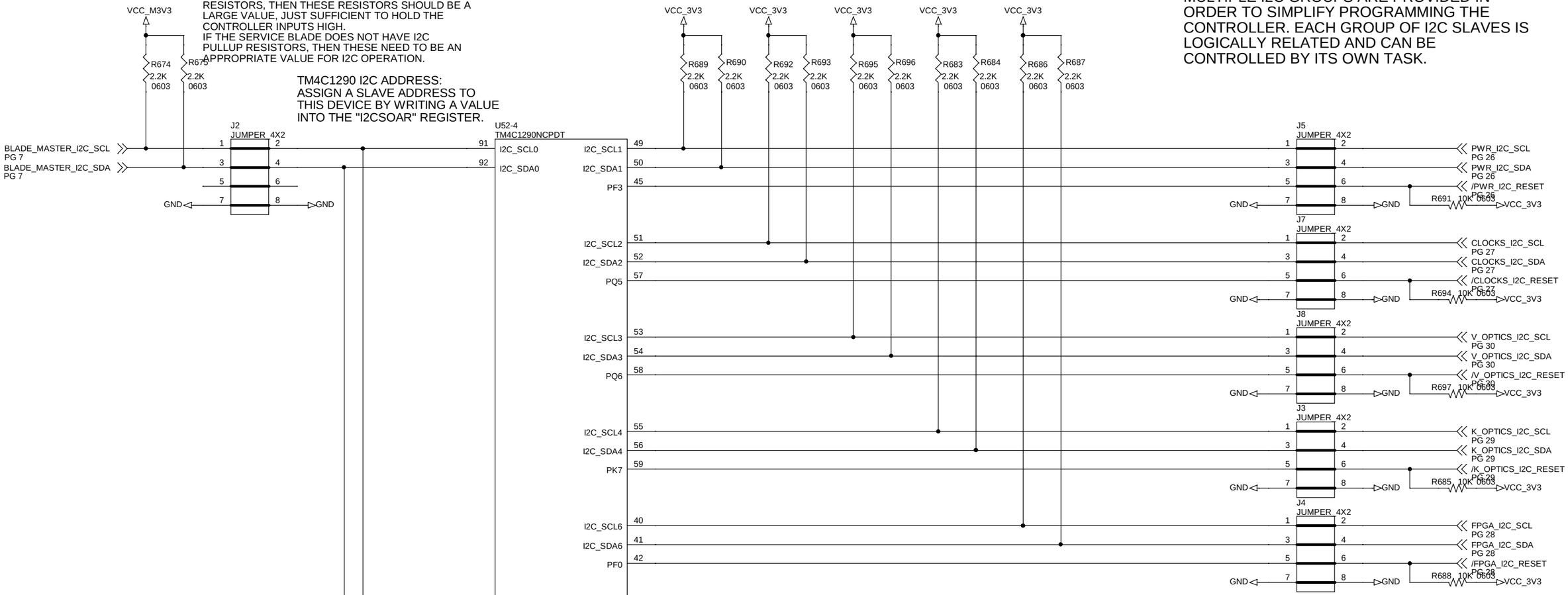
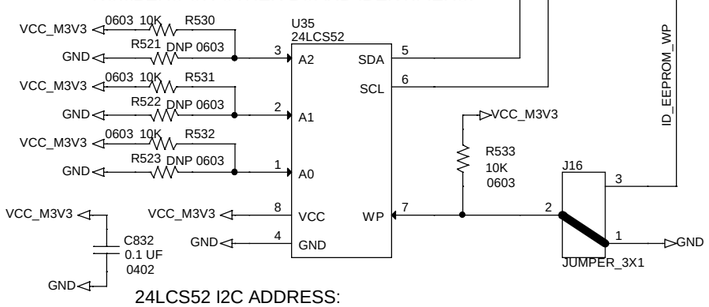
IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH.
IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.



THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.



24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

THIS JUMPER CONFIGURES THE HARDWARE WRITE-PROTECT PIN.

IF NO JUMPER IS IN PLACE, THE HARDWARE WRITE PROTECTION IS ALWAYS ENABLED.

IF THE JUMPER CONNECTS PINS 1 AND 2, THE HARDWARE WRITE PROTECTION IS ALWAYS DISABLED.

IF THE JUMPER CONNECTS PINS 2 AND 3, THE HARDWARE PROTECTION IS CONTROLLED BY A GPIO PIN ON THE CONTROLLER.

REFER TO THE DATA SHEET FOR DETAILS ABOUT CONNECTING AN EXTERNAL HIGH VOLTAGE TO RESET THE SOFTWARE WRITE PROTECT FUSE.

I2C MODULE 7 IN UNCOMMITTED. THE PINS CAN BE REPURPOSED IF NEEDED. I2C MODULE 8 ON PINS 35 AND 36 HAS BEEN REPURPOSED AS UART MODULE 4.

HEADERS ARE PROVIDED TO SUPPORT DRIVING ANY I2C BUS WITH A STAND-ALONE USB-TO-I2C CONTROLLER.

NORMALLY, JUMPERS WILL CONNECT THE ON-BOARD "SCL", "SDA", AND "/RESET" SIGNALS STRAIGHT THROUGH THE HEADERS.

TO CONNECT THE STAND-ALONE CONTROLLER, PULL THE JUMPERS FROM THE HEADER AND CONNECT THE CONTROLLER'S SIGNALS TO PINS 2, 4, AND 6, AND CONNECT GND TO PIN 8.

CONFIGURE THE "SPI MISO" PIN ON THE AARDVARK CONTROLLER AS A "GPIO OUTPUT" TO CONTROL THE "RESET" SIGNAL.

THIS LAYOUT ASSUMES THAT THE STAND-ALONE CONTROLLER PROVIDES PULL-UP RESISTORS ON THE I2C SIGNALS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.01: I2C CONTROLLER		
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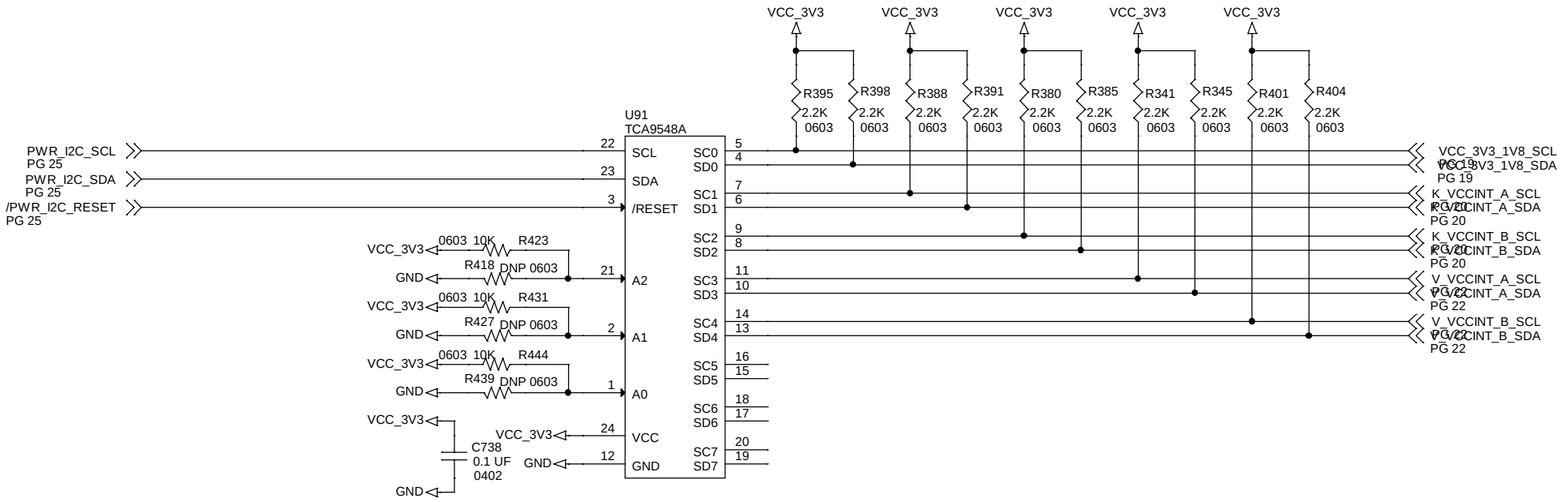

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.02: I2C POWER CONTROL		
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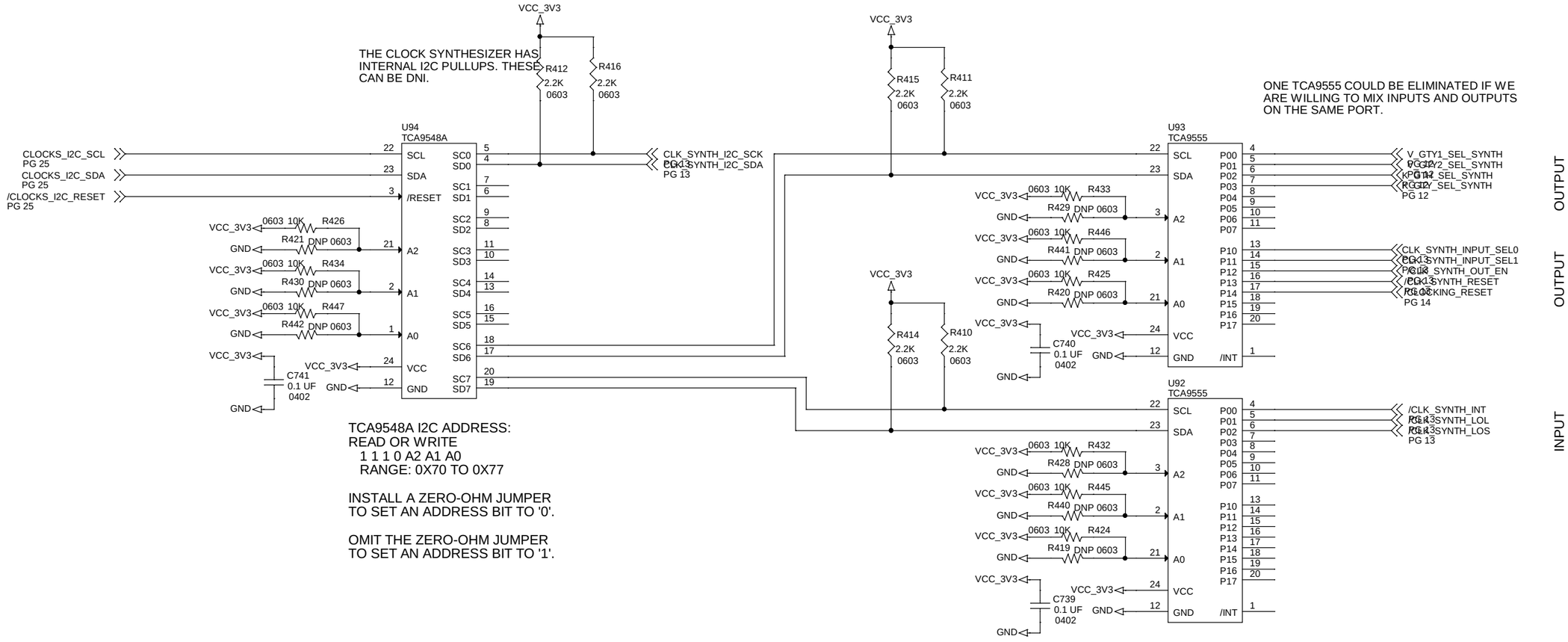
Date: Tuesday, February 26, 2019	Sheet 26 of 74	



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.03: I2C CLOCK SOURCE CONTROL		
Size	Document Number: 6089-103	Rev: A
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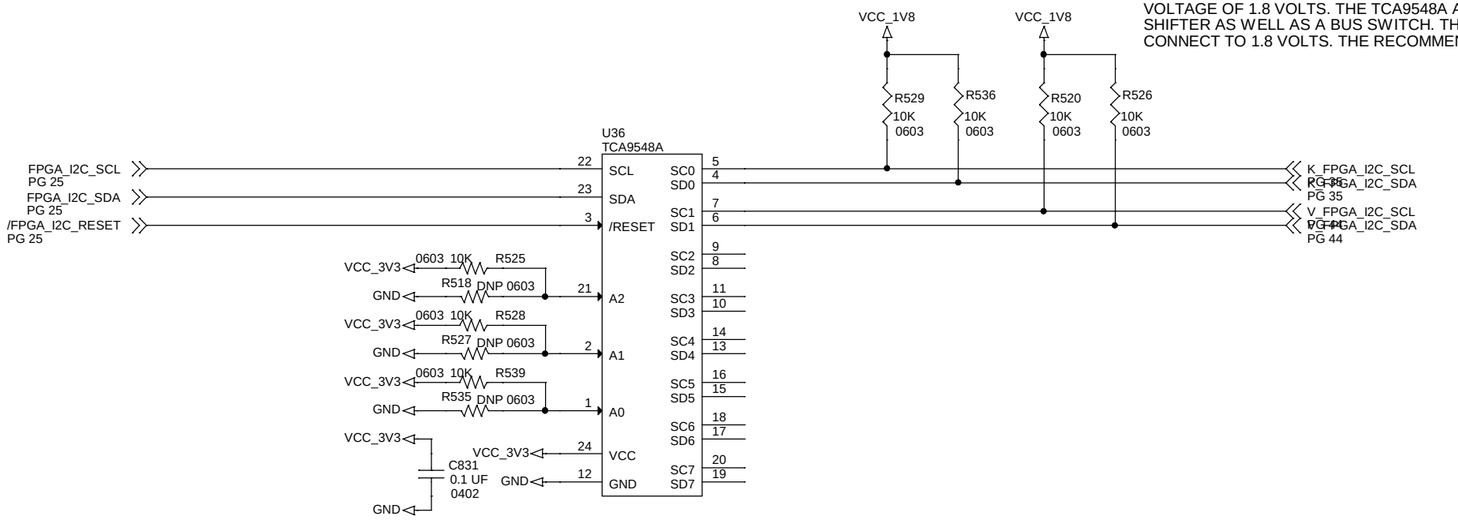
THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.04: I2C FPGA SYSMON

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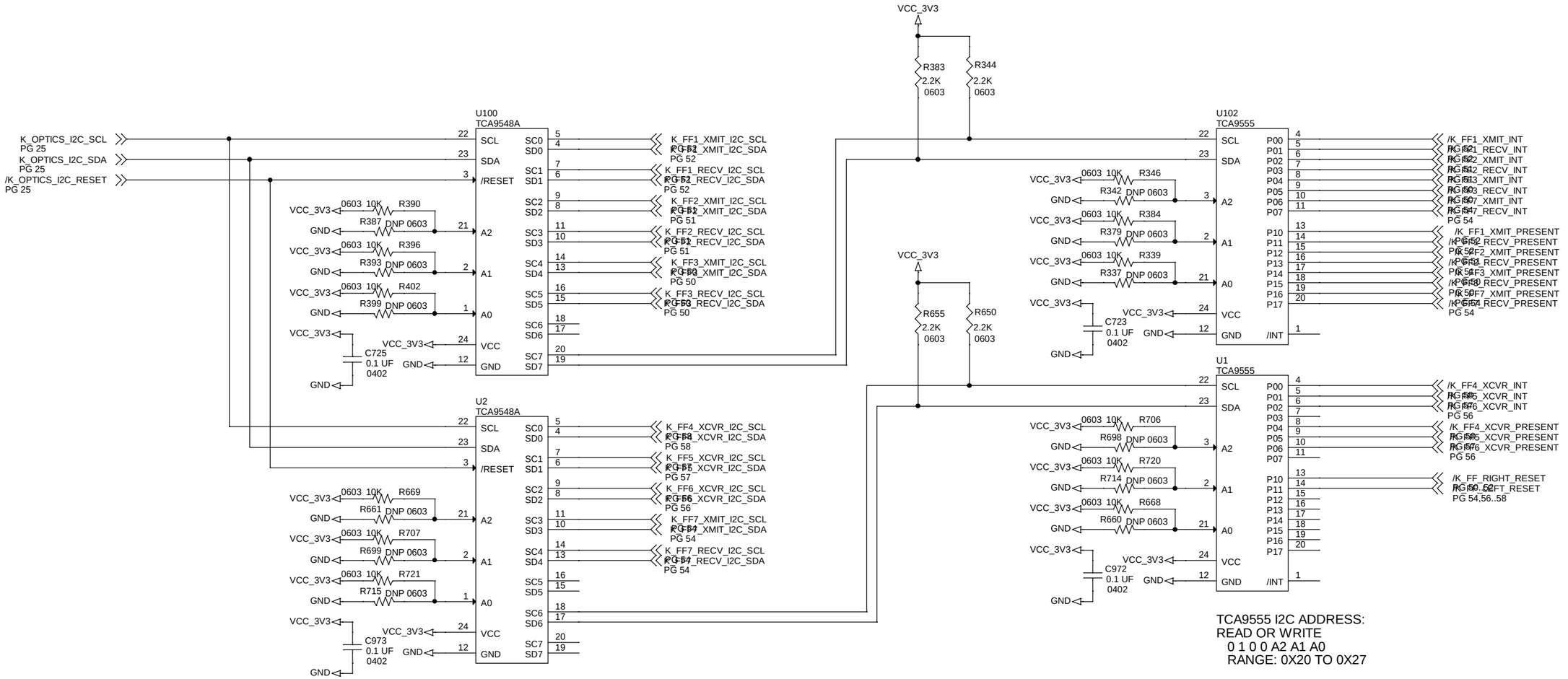

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.05: I2C KU15P OPTICS		
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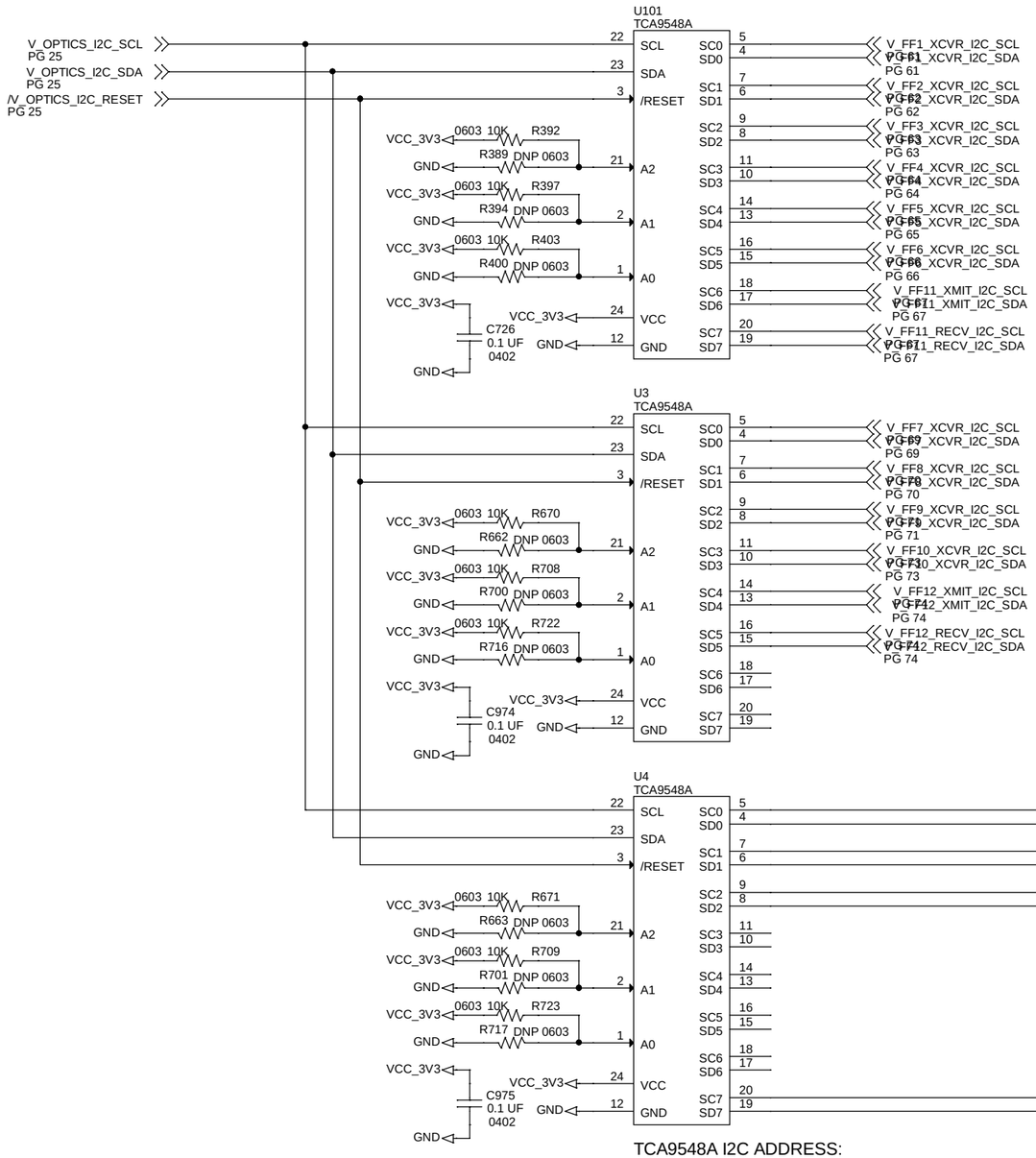
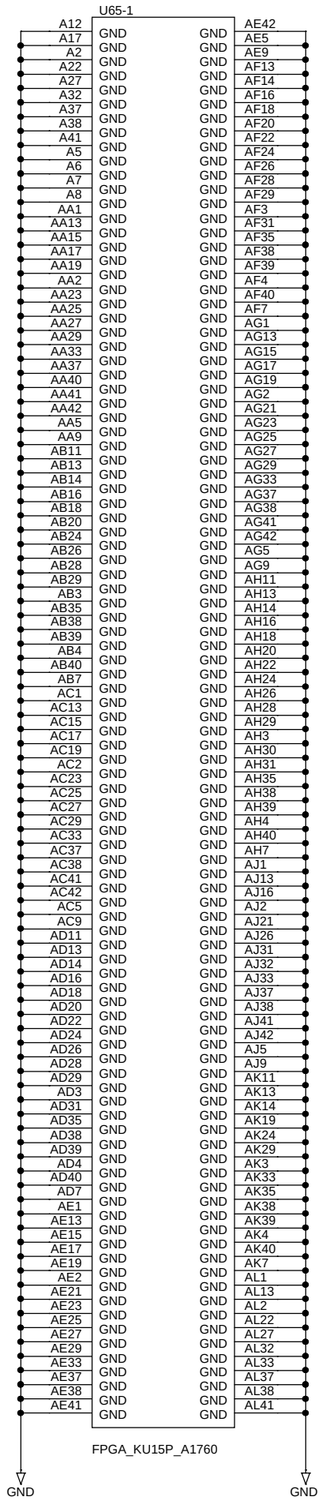
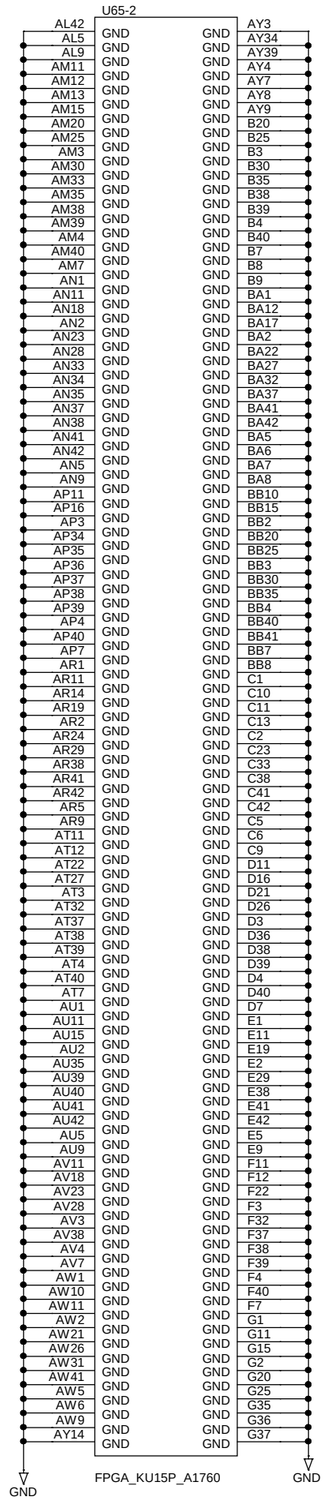
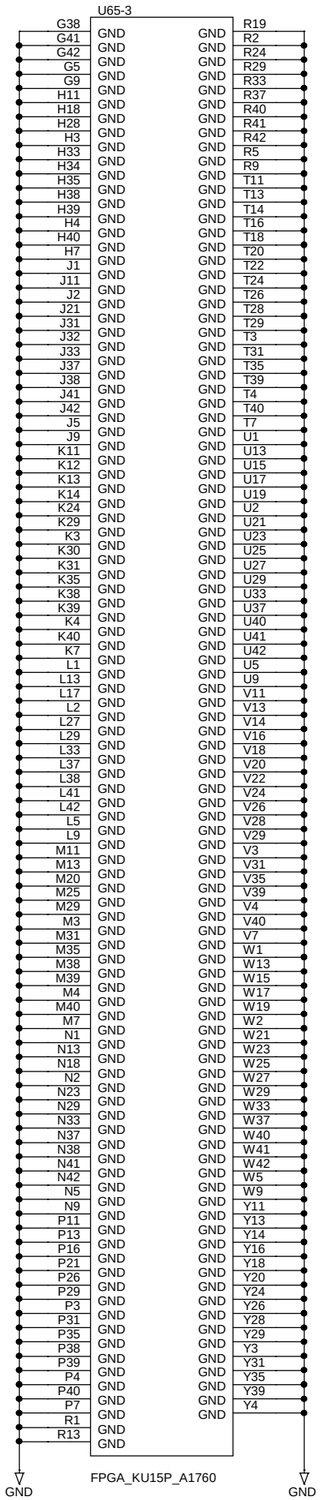
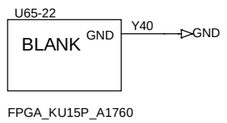


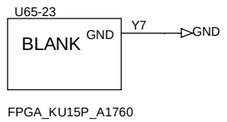
ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.06: I2C VU7P OPTICS		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 30 of 74	











ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.01: KU15P FPGA GND

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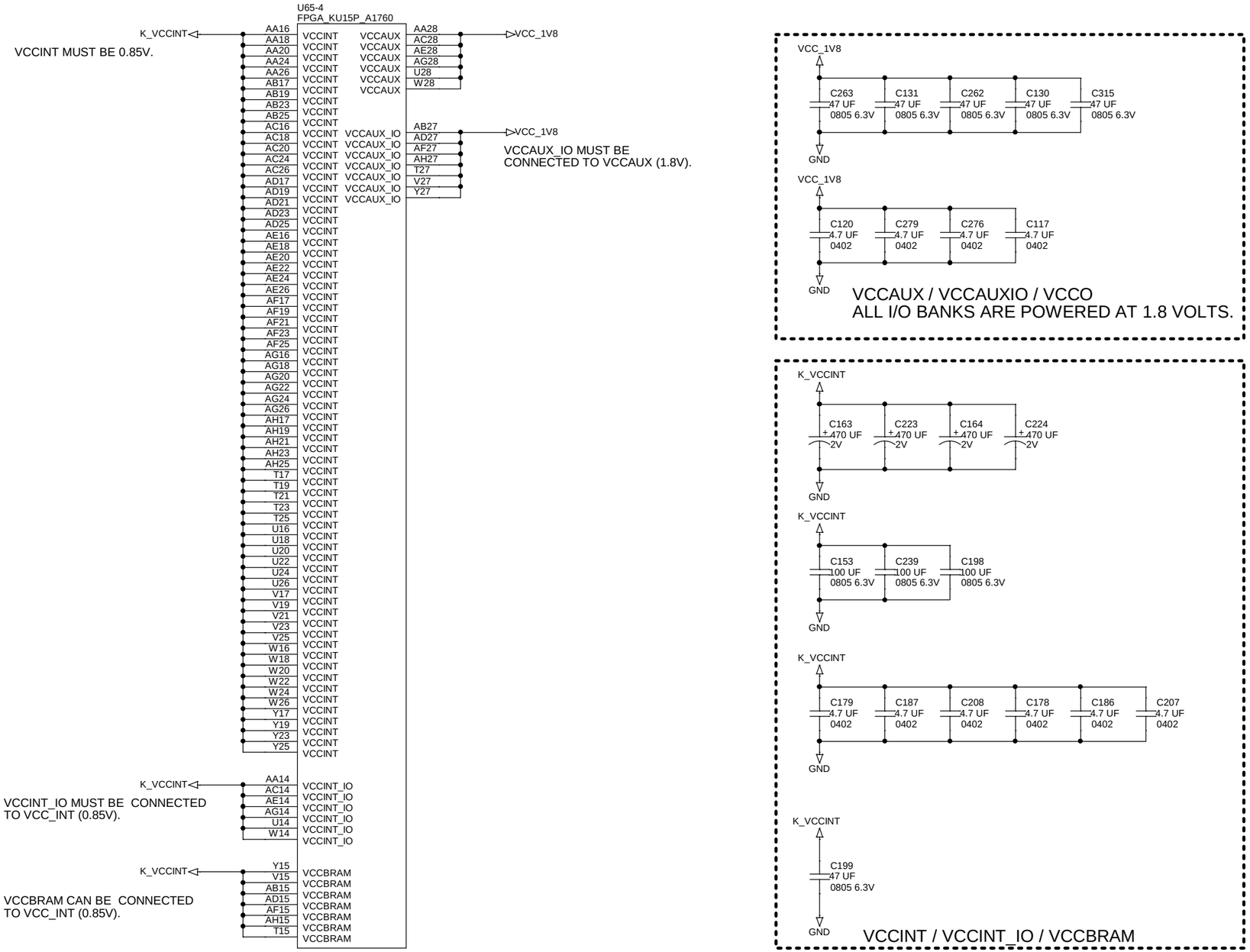
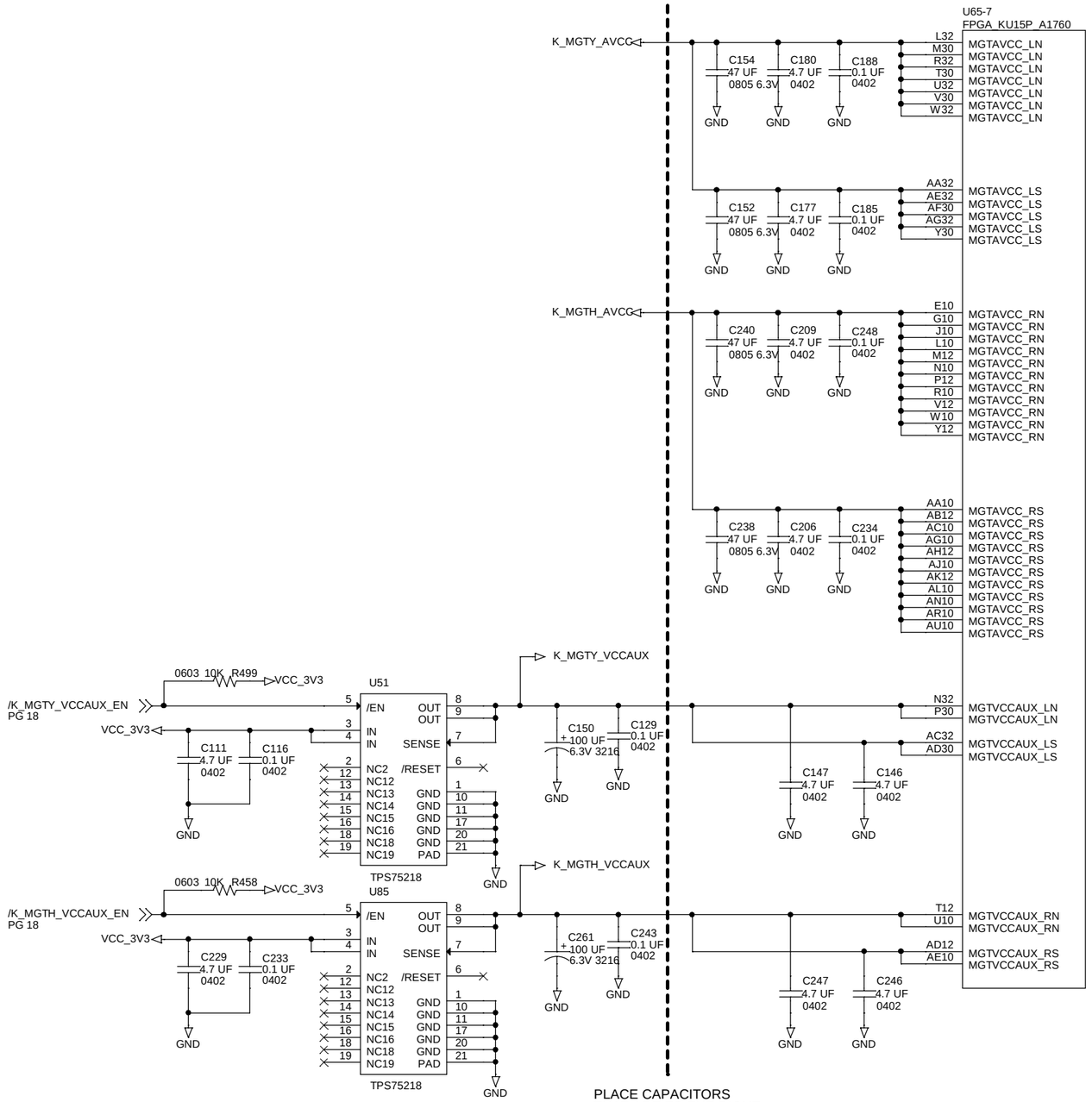
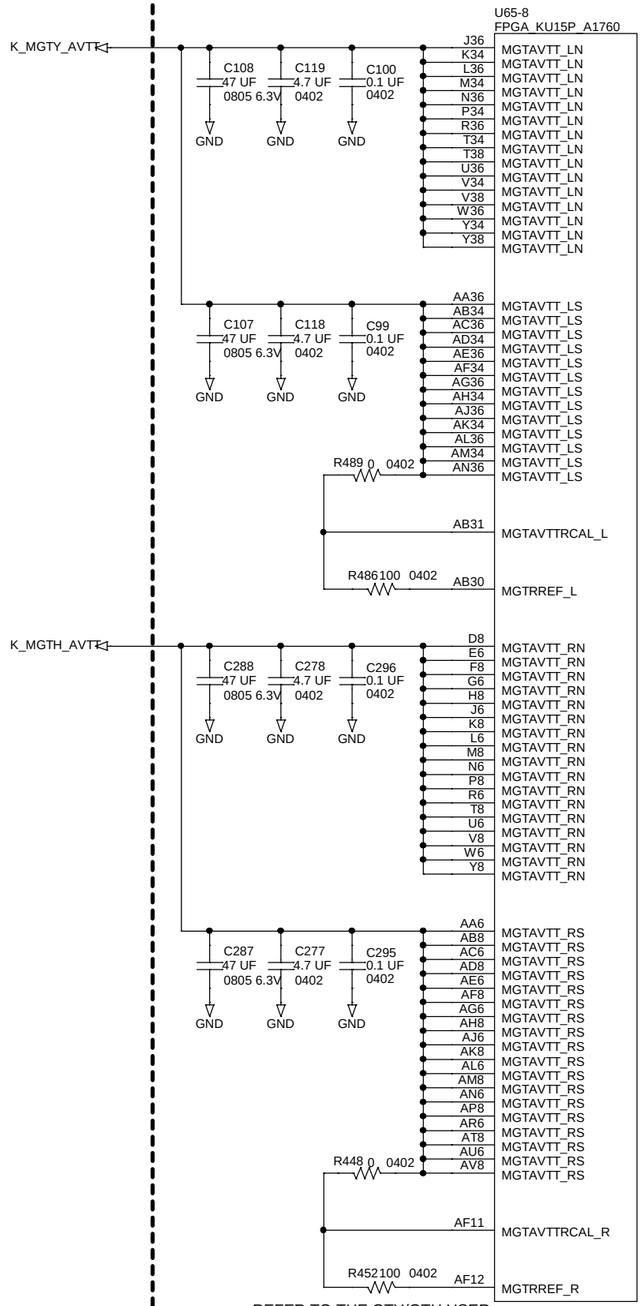


BYPASS CAPACITOR VALUES AND QUANTITIES FROM "xtp427-ultrascale-plus-schematic-review-checklist.xls"

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.02: KU15P FPGA INTERNAL POWER		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 32 of 74	





ON MIXED TRANSCEIVER DEVICES, REGIONS "LN" AND "LS" ARE GTY TRANSCEIVERS. REGIONS "RN" AND "RS" ARE GTH TRANSCEIVERS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.03: KU15P GTH/GTY TRANSCEIVER POWER		
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MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES
PULLUPS ON ALL I/O PINS DURING
CONFIGURATION. THE PULLUPS ARE ABOUT
15K AT 1.8 VOLTS. IF A PULLDOWN IS
REQUIRED, IT MUST BE SMALLER THAN 4K TO
DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS
PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

PULLUPS/PULLDOWNS ON THE
BOOT MODE CONFIGURATION
INPUTS MUST BE 1K OR LESS.

U65-6
FPGA_KU15P_A1760
BANK 0

K_VCCINT — R482 DNP 0603 — AM17 POR_OVERRIDE
GND — R481 0 0603 — AM17
GND — R472 0 0603 — AM16 RSVDGND_CFGBVS_0
VCC_1V8 — R488 DNP 0603 — AM18 PUDC_B_0
GND — R485 0 0603 — AM18
VCC_1V8 — R676 1K 0402 — AL14 M2_0
K_CONFIG_BIT_M2 PG 17 — AL14
VCC_1V8 — R464 DNP 0603 — AL15 M1_0
GND — R462 0 0603 — AL15
VCC_1V8 — R479 0 0603 — AL16 M0_0
GND — R477 DNP 0603 — AL16

VCCO_0: AL17, AN13 → VCC_1V8
C245 47 UF 0805 6.3V
VCC_1V8 — R417 2.2K 0603
VCC_1V8 — R443 4.7K 0603
R413 4.7K 0603

D00_MOSI_0 AN12
D01_DIN_0 AM14
D02_0 AN14
D03_0 AN15
RDWR_FCS_B_0 AL18
CCLK_0 AK17
PROGRAM_B_0 AJ18
DONE_0 AN16
INIT_B_0 AK18
VBATT AJ14 → GND

THIS DESIGN DOES NOT USE ENCRYPTION,
SO "VBATT" CAN BE TIED TO "GND"

0603 4.7K R14 VCC_1V8
0603 4.7K R484 VCC_1V8
K_FPGA_INIT_B

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

U95
MT25QU01
15 DQ0
8 DQ1
9 DQ2
1 DQ3
7 S#
16 CLK
VCC 2
GND 10
DNU_3 3
DNU_4 4
DNU_5 5
DNU_6 6
DNU_11 11
DNU_12 12
DNU_13 13
DNU_14 14
VCC_1V8
C735 0.1 UF 0402
GND

K_FPGA_DONE

/K_FPGA_DONE
PG 11
0603 4.7K R2
D4 LED GREEN R1 150
VCC_3V3
Q1 FET_N_1.8V
GND

KU15P DONE LED

THE PULLUP RESISTOR IN PARALLEL
WITH THE LED ENSURES THAT, WHEN
THE FET IS OFF, THE "/K_FPGA_DONE"
SIGNAL IS AT A HIGH LEVEL FOR
FEEDING THE TM4C CONTROLLER.

0603 4.7K R705 VCC_1V8
K_FPGA_PROGRAM
PG 11
Q26 FET_N_1.8V
R704 4.7K 0603 GND
GND
SW1
SW PUSHBUTTON
GND

THE FPGA CAN BE REPROGRAMMED EITHER BY
PULSING "K_FPGA_PROGRAM" FROM THE TM4C
CONTROLLER, OR BY ACTIVATING THE FRONT
PANEL "REPROGRAM" SWITCH.

FRONT PANEL REPROGRAM

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title
5.04: KU15P FPGA CONFIGURATION
Size | Document Number 6089-103 | Rev A
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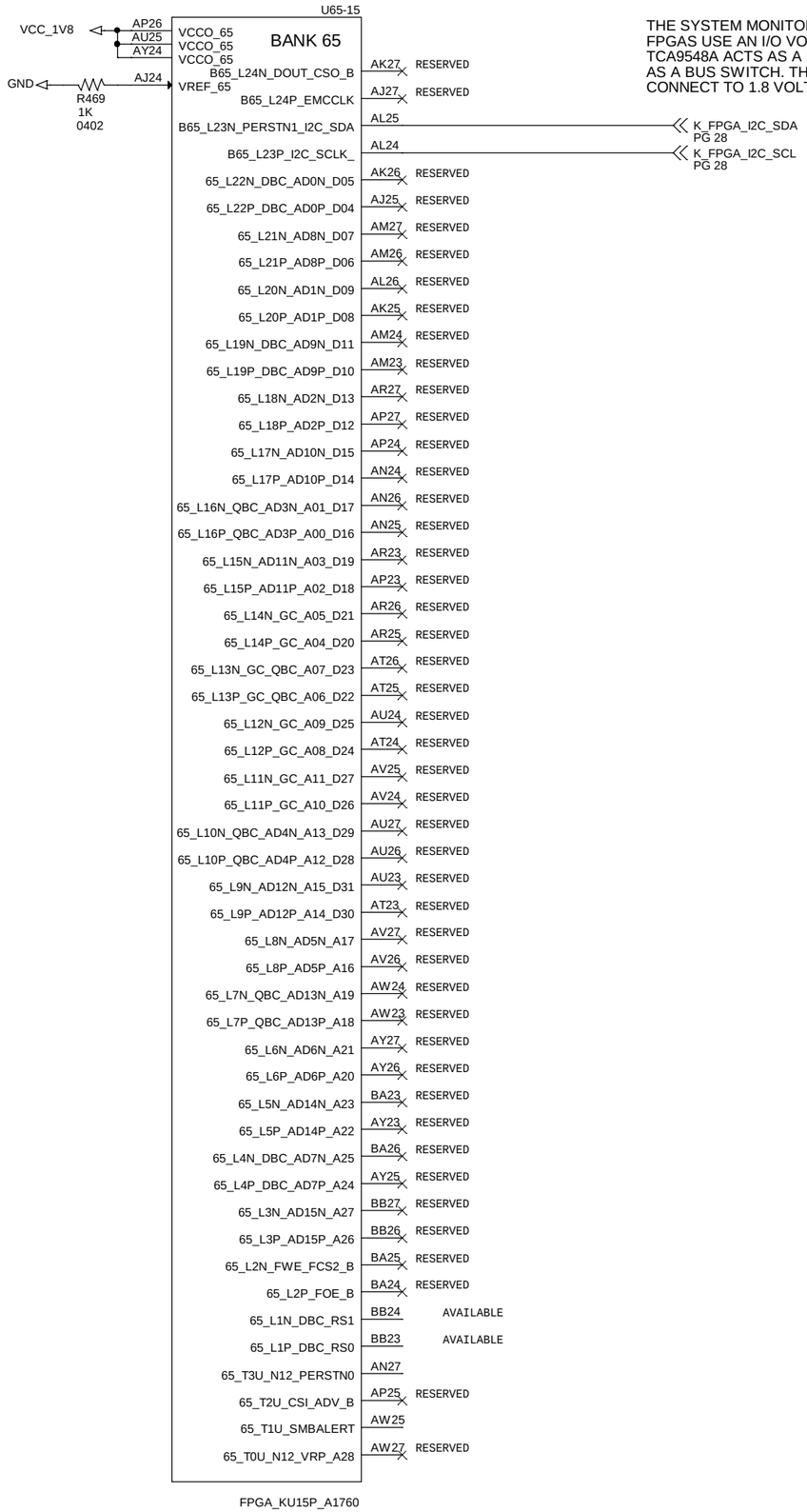

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.05: KU15P BANK 65

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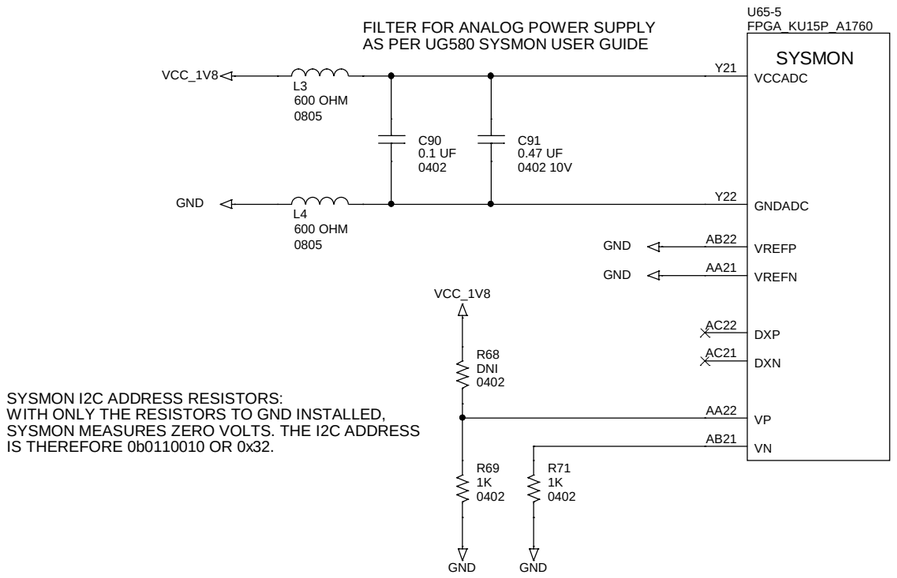

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.06: KU15P SYSTEM MONITOR

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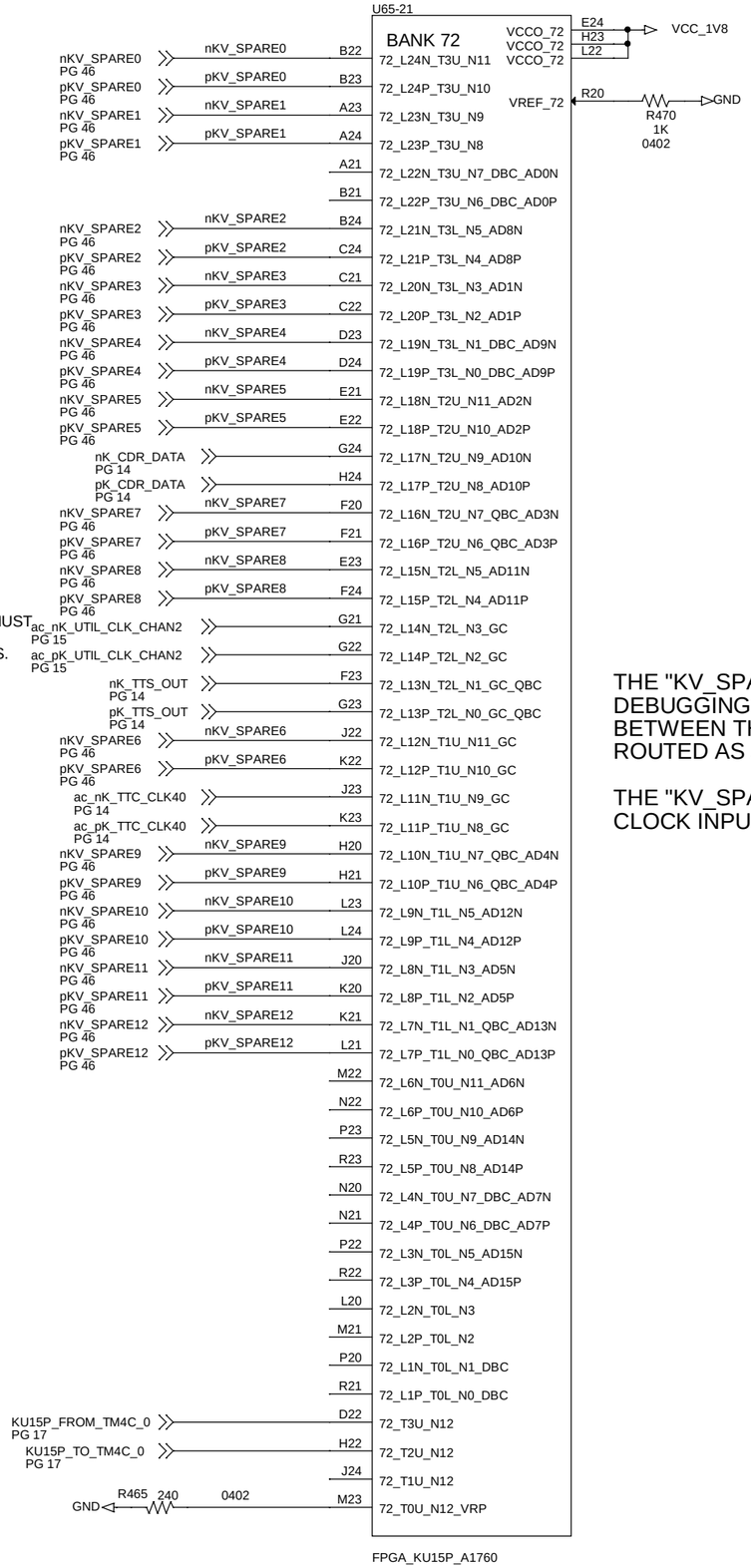
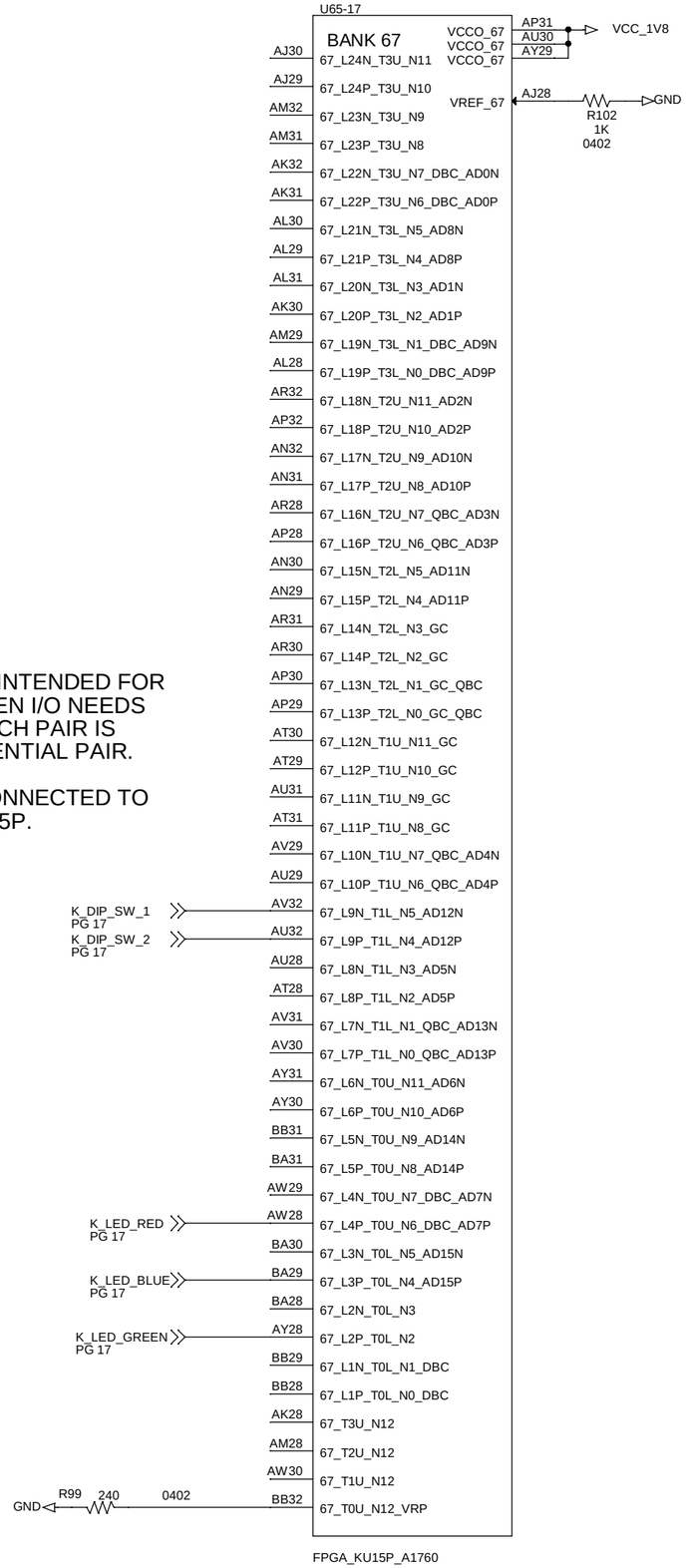


THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "KV_SPARE6" SIGNAL IS CONNECTED TO CLOCK INPUT PINS ON THE KU15P.



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.07: KU15P UTILITY BANKS		
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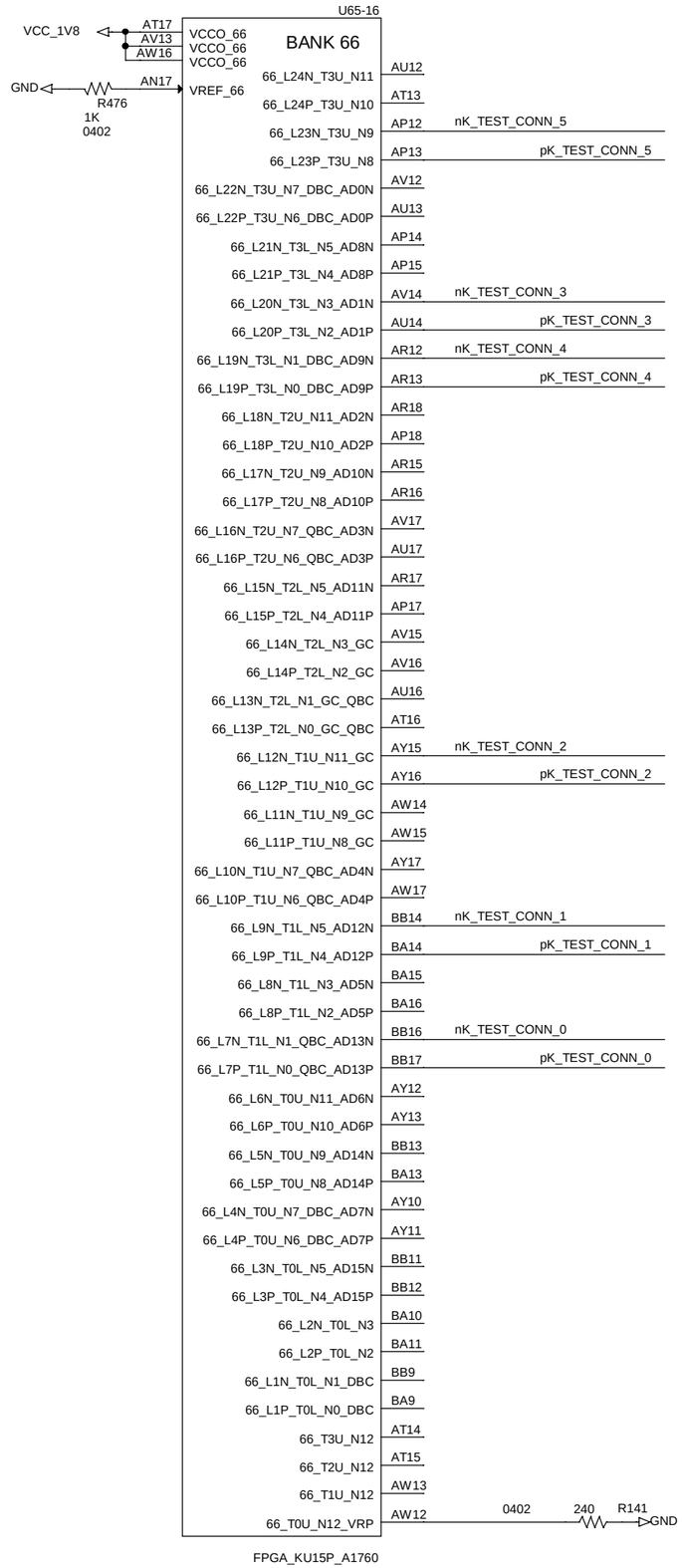

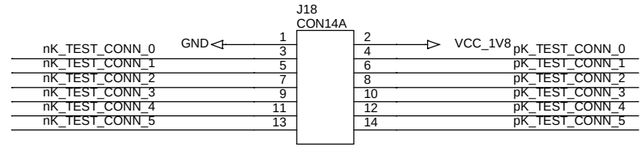

THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "K_TEST_CONN_2" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.08 KU15P TEST CONNECTOR

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U65-18

BANK 68

AV42	68_L24N_T3U_N11	VCCO_68
AV41	68_L24P_T3U_N10	VCCO_68
BA40	68_L23N_T3U_N9	VREF_68
AY40	68_L23P_T3U_N8	
AY42	68_L22N_T3U_N7_DBC_AD0N	
AW42	68_L22P_T3U_N6_DBC_AD0P	
BB39	68_L21N_T3L_N5_AD8N	
BA39	68_L21P_T3L_N4_AD8P	
AW40	68_L20N_T3L_N3_AD1N	
AV40	68_L20P_T3L_N2_AD1P	
BB38	68_L19N_T3L_N1_DBC_AD9N	
BA38	68_L19P_T3L_N0_DBC_AD9P	
AR37	68_L18N_T2U_N11_AD2N	
AR36	68_L18P_T2U_N10_AD2P	
AW39	68_L17N_T2U_N9_AD10N	
AV39	68_L17P_T2U_N8_AD10P	
AU37	68_L16N_T2U_N7_QBC_AD3N	
AT36	68_L16P_T2U_N6_QBC_AD3P	
AY38	68_L15N_T2L_N5_AD11N	
AW38	68_L15P_T2L_N4_AD11P	
AV36	68_L14N_T2L_N3_GC	
AU36	68_L14P_T2L_N2_GC	
AW37	68_L13N_T2L_N1_GC_QBC	
AV37	68_L13P_T2L_N0_GC_QBC	
AW35	68_L12N_T1U_N11_GC	
AV35	68_L12P_T1U_N10_GC	
AW34	68_L11N_T1U_N9_GC	
AV34	68_L11P_T1U_N8_GC	
AT35	68_L10N_T1U_N7_QBC_AD4N	
AR35	68_L10P_T1U_N6_QBC_AD4P	
AU34	68_L9N_T1L_N5_AD12N	
AU33	68_L9P_T1L_N4_AD12P	
AT34	68_L8N_T1L_N3_AD5N	
AR33	68_L8P_T1L_N2_AD5P	
AW33	68_L7N_T1L_N1_QBC_AD13N	
AW32	68_L7P_T1L_N0_QBC_AD13P	
AY37	68_L6N_T0U_N11_AD6N	
AY36	68_L6P_T0U_N10_AD6P	
BB34	68_L5N_T0U_N9_AD14N	
BA34	68_L5P_T0U_N8_AD14P	
BB37	68_L4N_T0U_N7_DBC_AD7N	
BA36	68_L4P_T0U_N6_DBC_AD7P	
BB33	68_L3N_T0L_N5_AD15N	
BA33	68_L3P_T0L_N4_AD15P	
BA35	68_L2N_T0L_N3	
AY35	68_L2P_T0L_N2	
AY33	68_L1N_T0L_N1_DBC	
AY32	68_L1P_T0L_N0_DBC	
AY41	68_T3U_N12	
AU38	68_T2U_N12	
AT33	68_T1U_N12	
BB36	68_T0U_N12_VRP	

VCCO_68 VCCO_68 — AR34 AV33 AW36 — VCC_1V8

VREF_68 — AP33

FPGA_KU15P_A1760

U65-19

BANK 70

B34	70_L24N_T3U_N11	VCCO_70
B33	70_L24P_T3U_N10	VCCO_70
A34	70_L23N_T3U_N9	VREF_70
A33	70_L23P_T3U_N8	
C37	70_L22N_T3U_N7_DBC_AD0N	
D37	70_L22P_T3U_N6_DBC_AD0P	
A36	70_L21N_T3L_N5_AD8N	
A35	70_L21P_T3L_N4_AD8P	
C36	70_L20N_T3L_N3_AD1N	
C35	70_L20P_T3L_N2_AD1P	
B37	70_L19N_T3L_N1_DBC_AD9N	
B36	70_L19P_T3L_N0_DBC_AD9P	
C30	70_L18N_T2U_N11_AD2N	
C29	70_L18P_T2U_N10_AD2P	
A31	70_L17N_T2U_N9_AD10N	
A30	70_L17P_T2U_N8_AD10P	
D30	70_L16N_T2U_N7_QBC_AD3N	
D29	70_L16P_T2U_N6_QBC_AD3P	
B32	70_L15N_T2L_N5_AD11N	
B31	70_L15P_T2L_N4_AD11P	
D32	70_L14N_T2L_N3_GC	
E32	70_L14P_T2L_N2_GC	
C32	70_L13N_T2L_N1_GC_QBC	
C31	70_L13P_T2L_N0_GC_QBC	
D33	70_L12N_T1U_N11_GC	
E33	70_L12P_T1U_N10_GC	
D35	70_L11N_T1U_N9_GC	
D34	70_L11P_T1U_N8_GC	
F35	70_L10N_T1U_N7_QBC_AD4N	
F34	70_L10P_T1U_N6_QBC_AD4P	
E36	70_L9N_T1L_N5_AD12N	
E35	70_L9P_T1L_N4_AD12P	
F33	70_L8N_T1L_N3_AD5N	
G33	70_L8P_T1L_N2_AD5P	
E37	70_L7N_T1L_N1_QBC_AD13N	
F36	70_L7P_T1L_N0_QBC_AD13P	
G32	70_L6N_T0U_N11_AD6N	
G31	70_L6P_T0U_N10_AD6P	
E30	70_L5N_T0U_N9_AD14N	
F30	70_L5P_T0U_N8_AD14P	
H32	70_L4N_T0U_N7_DBC_AD7N	
H31	70_L4P_T0U_N6_DBC_AD7P	
E31	70_L3N_T0L_N5_AD15N	
F31	70_L3P_T0L_N4_AD15P	
H30	70_L2N_T0L_N3	
J30	70_L2P_T0L_N2	
G29	70_L1N_T0L_N1_DBC	
H29	70_L1P_T0L_N0_DBC	
C34	70_T3U_N12	
B29	70_T2U_N12	
G34	70_T1U_N12	
F29	70_T0U_N12_VRP	

VCCO_70 VCCO_70 — D31 E34 G30 — VCC_1V8

VREF_70 — J29

FPGA_KU15P_A1760

U65-20

BANK 71

A26	71_L24N_T3U_N11	VCCO_71
A25	71_L24P_T3U_N10	VCCO_71
A29	71_L23N_T3U_N9	VREF_71
A28	71_L23P_T3U_N8	
B27	71_L22N_T3U_N7_DBC_AD0N	
B26	71_L22P_T3U_N6_DBC_AD0P	
B28	71_L21N_T3L_N5_AD8N	
C27	71_L21P_T3L_N4_AD8P	
C26	71_L20N_T3L_N3_AD1N	
C25	71_L20P_T3L_N2_AD1P	
D28	71_L19N_T3L_N1_DBC_AD9N	
D27	71_L19P_T3L_N0_DBC_AD9P	
E26	71_L18N_T2U_N11_AD2N	
E25	71_L18P_T2U_N10_AD2P	
E28	71_L17N_T2U_N9_AD10N	
E27	71_L17P_T2U_N8_AD10P	
F26	71_L16N_T2U_N7_QBC_AD3N	
F25	71_L16P_T2U_N6_QBC_AD3P	
F28	71_L15N_T2L_N5_AD11N	
G28	71_L15P_T2L_N4_AD11P	
G26	71_L14N_T2L_N3_GC	
H26	71_L14P_T2L_N2_GC	
G27	71_L13N_T2L_N1_GC_QBC	
H27	71_L13P_T2L_N0_GC_QBC	
J25	71_L12N_T1U_N11_GC	
K25	71_L12P_T1U_N10_GC	
J27	71_L11N_T1U_N9_GC	
K26	71_L11P_T1U_N8_GC	
J28	71_L10N_T1U_N7_QBC_AD4N	
K27	71_L10P_T1U_N6_QBC_AD4P	
K28	71_L9N_T1L_N5_AD12N	
L28	71_L9P_T1L_N4_AD12P	
L26	71_L8N_T1L_N3_AD5N	
L25	71_L8P_T1L_N2_AD5P	
M28	71_L7N_T1L_N1_QBC_AD13N	
M27	71_L7P_T1L_N0_QBC_AD13P	
N26	71_L6N_T0U_N11_AD6N	
N25	71_L6P_T0U_N10_AD6P	
M24	71_L5N_T0U_N9_AD14N	
N24	71_L5P_T0U_N8_AD14P	
N27	71_L4N_T0U_N7_DBC_AD7N	
P27	71_L4P_T0U_N6_DBC_AD7P	
P25	71_L3N_T0L_N5_AD15N	
P24	71_L3P_T0L_N4_AD15P	
N28	71_L2N_T0L_N3	
P28	71_L2P_T0L_N2	
R28	71_L1N_T0L_N1_DBC	
R27	71_L1P_T0L_N0_DBC	
D25	71_T3U_N12	
H25	71_T2U_N12	
M26	71_T1U_N12	
R26	71_T0U_N12_VRP	

VCCO_71 VCCO_71 — C28 F27 J26 — VCC_1V8

VREF_71 — R25

FPGA_KU15P_A1760

U65-14

BANK 64

AJ19	64_L24N_T3U_N11	VCCO_64
AJ20	64_L24P_T3U_N10	VCCO_64
AK23	64_L23N_T3U_N9	VCCO_64
AJ23	64_L23P_T3U_N8	
AL20	64_L22N_T3U_N7_DBC_AD0N	
AK20	64_L22P_T3U_N6_DBC_AD0P	
AK22	64_L21N_T3L_N5_AD8N	
AJ22	64_L21P_T3L_N4_AD8P	
AM19	64_L20N_T3L_N3_AD1N	
AL19	64_L20P_T3L_N2_AD1P	
AL21	64_L19N_T3L_N1_DBC_AD9N	
AK21	64_L19P_T3L_N0_DBC_AD9P	
AP19	64_L18N_T2U_N11_AD2N	
AP20	64_L18P_T2U_N10_AD2P	
AN20	64_L17N_T2U_N9_AD10N	
AN21	64_L17P_T2U_N8_AD10P	
AR22	64_L16N_T2U_N7_QBC_AD3N	
AP22	64_L16P_T2U_N6_QBC_AD3P	
AN22	64_L15N_T2L_N5_AD11N	
AM22	64_L15P_T2L_N4_AD11P	
AT20	64_L14N_T2L_N3_GC	
AR20	64_L14P_T2L_N2_GC	
AT21	64_L13N_T2L_N1_GC_QBC	
AR21	64_L13P_T2L_N0_GC_QBC	
AU19	64_L12N_T1U_N11_GC	
AT19	64_L12P_T1U_N10_GC	
AV20	64_L11N_T1U_N9_GC	
AU21	64_L11P_T1U_N8_GC	
AU18	64_L10N_T1U_N7_QBC_AD4N	
AT18	64_L10P_T1U_N6_QBC_AD4P	
AW19	64_L9N_T1L_N5_AD12N	
AW20	64_L9P_T1L_N4_AD12P	
AW18	64_L8N_T1L_N3_AD5N	
AV19	64_L8P_T1L_N2_AD5P	
AV21	64_L7N_T1L_N1_QBC_AD13N	
AU22	64_L7P_T1L_N0_QBC_AD13P	
BA18	64_L6N_T0U_N11_AD6N	
BA19	64_L6P_T0U_N10_AD6P	
BA20	64_L5N_T0U_N9_AD14N	
BA21	64_L5P_T0U_N8_AD14P	
AY20	64_L4N_T0U_N7_DBC_AD7N	
AY21	64_L4P_T0U_N6_DBC_AD7P	
BB18	64_L3N_T0L_N5_AD15N	
BB19	64_L3P_T0L_N4_AD15P	
AY22	64_L2N_T0L_N3	
AW22	64_L2P_T0L_N2	
BB21	64_L1N_T0L_N1_DBC	
BB22	64_L1P_T0L_N0_DBC	
AL23	64_T3U_N12	
AN19	64_T2U_N12	
AV22	64_T1U_N12	
AY18	64_T0U_N12_VRP	

VCCO_64 VCCO_64 VCCO_64 — AP21 AU20 AY19 — VCC_1V8

VREF_64 — AM21

FPGA_KU15P_A1760

U65-9

BANK 90

P17	90_L12N_AD0N	VCCO_90
R17	90_L12P_AD0P	VCCO_90
M17	90_L11N_AD1N	
N17	90_L11P_AD1P	
P18	90_L10N_AD2N	
R18	90_L10P_AD2P	
N19	90_L9N_AD3N	
P19	90_L9P_AD3P	
L18	90_L8N_HDGC_AD4N	
M18	90_L8P_HDGC_AD4P	
L19	90_L7N_HDGC_AD5N	
M19	90_L7P_HDGC_AD5P	
K16	90_L6N_HDGC_AD6N	
K17	90_L6P_HDGC_AD6P	
J18	90_L5N_HDGC_AD7N	
K18	90_L5N_HDGC_AD7P	
H16	90_L4N_AD8N	
J17	90_L4P_AD8P	
G17	90_L3N_AD9N	
H17	90_L3P_AD9P	
H19	90_L2N_AD10N	
J19	90_L2P_AD10P	
G18	90_L1N_AD11N	
G19	90_L1P_AD11P	

VCCO_90 VCCO_90 — J16 K19 — VCC_1V8

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U65-10

BANK 91

F16	91_L12N_AD8N	VCCO_91
G16	91_L12P_AD8P	VCCO_91
E16	91_L11N_AD9N	
E17	91_L11P_AD9P	
D17	91_L10N_AD10N	
E18	91_L10P_AD10P	
F18	91_L9N_AD11N	
F19	91_L9P_AD11P	
D18	91_L8N_HDGC	
D19	91_L8P_HDGC	
D20	91_L7N_HDGC	
E20	91_L7P_HDGC	
C16	91_L6N_HDGC	
C17	91_L6P_HDGC	
C19	91_L5N_HDGC	
C20	91_L5P_HDGC	
A16	91_L4N_AD12N	
B16	91_L4P_AD12P	
B17	91_L3N_AD13N	
B18	91_L3P_AD13P	
A18	91_L2N_AD14N	
B19	91_L2P_AD14P	
A19	91_L1N_AD15N	
A20	91_L1P_AD15P	

VCCO_91 VCCO_91 — C18 F17 — VCC_1V8

FPGA_KU15P_A1760

U65-12

BANK 93

G13	93_L12N_AD0N	VCCO_93
G14	93_L12P_AD0P	VCCO_93
H14	93_L11N_AD1N	
H15	93_L11P_AD1P	
G12	93_L10N_AD2N	
H12	93_L10P_AD2P	
J12	93_L9N_AD3N	
J13	93_L9P_AD3P	
J14	93_L8N_HDGC_AD4N	
J15	93_L8P_HDGC_AD4P	
K15	93_L7N_HDGC_AD5N	
L15	93_L7P_HDGC_AD5P	
L16	93_L6N_HDGC_AD6N	
M16	93_L6P_HDGC_AD6P	
L14	93_L5N_HDGC_AD7N	
M14	93_L5P_HDGC_AD7P	
N15	93_L4N_AD8N	
N16	93_L4P_AD8P	
N14	93_L3N_AD9N	
P15	93_L3P_AD9P	
P14	93_L2N_AD10N	
R14	93_L2P_AD10P	
R15	93_L1N_AD11N	
R16	93_L1P_AD11P	

VCCO_93 VCCO_93 — H13 M15 — VCC_1V8

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U65-13

BANK 94

A14	94_L12N_AD8N	VCCO_94
A15	94_L12P_AD8P	VCCO_94
A13	94_L11N_AD9N	
B14	94_L11P_AD9P	
C14	94_L10N_AD10N	
C15	94_L10P_AD10P	
D14	94_L9N_AD11N	
D15	94_L9P_AD11P	
E15	94_L8N_HDGC	
F15	94_L8P_HDGC	
F13	94_L7N_HDGC	
F14	94_L7P_HDGC	
D13	94_L6N_HDGC	
E13	94_L6P_HDGC	
D12	94_L5N_HDGC	
E12	94_L5P_HDGC	
B12	94_L4N_AD12N	
B13	94_L4P_AD12P	
B11	94_L3N_AD13N	
C12	94_L3P_AD13P	
A10	94_L2N_AD14N	
A11	94_L2P_AD14P	
A9	94_L1N_AD15N	
B10	94_L11P_AD15P	

VCCO_94 VCCO_94 — B15 E14 — VCC_1V8

FPGA_KU15P_A1760

KU15P UNUSED BLOCKS

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.99: KU15P UNUSED BLOCKS		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 39 of 74	

U66-1
FPGA_VU7P_B2104

A10	GND	GND	AF28
A12	GND	GND	AF3
A21	GND	GND	AF35
A3	GND	GND	AF36
A31	GND	GND	AF4
A41	GND	GND	AF40
A44	GND	GND	AF42
A6	GND	GND	AF45
AA1	GND	GND	AF46
AA10	GND	GND	AF5
AA13	GND	GND	AF8
AA15	GND	GND	AG1
AA17	GND	GND	AG11
AA19	GND	GND	AG17
AA2	GND	GND	AG2
AA21	GND	GND	AG21
AA23	GND	GND	AG23
AA25	GND	GND	AG25
AA27	GND	GND	AG27
AA29	GND	GND	AG33
AA31	GND	GND	AG35
AA35	GND	GND	AG39
AA38	GND	GND	AG42
AA42	GND	GND	AG43
AA43	GND	GND	AG44
AA44	GND	GND	AG5
AA5	GND	GND	AG7
AA6	GND	GND	AH14
AA7	GND	GND	AH16
AB12	GND	GND	AH20
AB14	GND	GND	AH22
AB16	GND	GND	AH24
AB18	GND	GND	AH26
AB20	GND	GND	AH3
AB22	GND	GND	AH30
AB24	GND	GND	AH35
AB26	GND	GND	AH37
AB28	GND	GND	AH4
AB3	GND	GND	AH41
AB30	GND	GND	AH42
AB35	GND	GND	AH45
AB37	GND	GND	AH46
AB4	GND	GND	AH5
AB40	GND	GND	AH9
AB42	GND	GND	AJ1
AB45	GND	GND	AJ10
AB46	GND	GND	AJ13
AB5	GND	GND	AJ15
AB8	GND	GND	AJ17
AC1	GND	GND	AJ2
AC10	GND	GND	AJ21
AC15	GND	GND	AJ23
AC17	GND	GND	AJ25
AC19	GND	GND	AJ35
AC2	GND	GND	AJ38
AC21	GND	GND	AJ42
AC23	GND	GND	AJ43
AC25	GND	GND	AJ44
AC27	GND	GND	AJ5
AC29	GND	GND	AJ6
AC35	GND	GND	AK14
AC39	GND	GND	AK16
AC42	GND	GND	AK18
AC43	GND	GND	AK20
AC44	GND	GND	AK22
AC5	GND	GND	AK24
AC7	GND	GND	AK3
AD14	GND	GND	AK34
AD16	GND	GND	AK35
AD18	GND	GND	AK37
AD20	GND	GND	AK4
AD22	GND	GND	AK40
AD24	GND	GND	AK42
AD26	GND	GND	AK45
AD28	GND	GND	AK46
AD3	GND	GND	AK5
AD32	GND	GND	AK8
AD35	GND	GND	AL1
AD37	GND	GND	AL11
AD4	GND	GND	AL2
AD41	GND	GND	AL31
AD42	GND	GND	AL35
AD45	GND	GND	AL39
AD46	GND	GND	AL42
AD5	GND	GND	AL43
AD9	GND	GND	AL44
AE1	GND	GND	AL5
AE10	GND	GND	AL7
AE17	GND	GND	AM18
AE19	GND	GND	AM28
AE2	GND	GND	AM3
AE21	GND	GND	AM35
AE23	GND	GND	AM37
AE25	GND	GND	AM4
AE27	GND	GND	AM41
AE29	GND	GND	AM42
AE35	GND	GND	AM45
AE38	GND	GND	AM46
AE42	GND	GND	AM5
AE43	GND	GND	AM9
AE44	GND	GND	AN1
AE5	GND	GND	AN10
AE6	GND	GND	AN12
AF12	GND	GND	AN15
AF14	GND	GND	AN2
AF16	GND	GND	AN25
AF20	GND	GND	AN35
AF22	GND	GND	AN38
AF24	GND	GND	AN42
AF26	GND	GND	AN43

GND GND

U66-2
FPGA_VU7P_B2104

AN44	GND	GND	B44
AN5	GND	GND	B45
AN6	GND	GND	B5
AP12	GND	GND	B6
AP22	GND	GND	B7
AP3	GND	GND	B8
AP32	GND	GND	BA11
AP35	GND	GND	BA21
AP36	GND	GND	BA3
AP4	GND	GND	BA31
AP40	GND	GND	BA37
AP42	GND	GND	BA38
AP45	GND	GND	BA39
AP46	GND	GND	BA44
AP5	GND	GND	BA6
AP8	GND	GND	BB1
AR1	GND	GND	BB18
AR11	GND	GND	BB2
AR12	GND	GND	BB28
AR19	GND	GND	BB3
AR2	GND	GND	BB39
AR29	GND	GND	BB40
AR35	GND	GND	BB41
AR39	GND	GND	BB44
AR42	GND	GND	BB45
AR43	GND	GND	BB46
AR44	GND	GND	BB6
AR5	GND	GND	BB8
AR7	GND	GND	BC15
AT12	GND	GND	BC25
AT16	GND	GND	BC3
AT26	GND	GND	BC35
AT3	GND	GND	BC4
AT35	GND	GND	BC41
AT37	GND	GND	BC42
AT4	GND	GND	BC44
AT41	GND	GND	BC6
AT42	GND	GND	BD1
AT45	GND	GND	BD12
AT46	GND	GND	BD22
AT5	GND	GND	BD3
AT9	GND	GND	BD32
AU1	GND	GND	BD41
AU10	GND	GND	BD44
AU12	GND	GND	BD46
AU2	GND	GND	BD6
AU23	GND	GND	BE19
AU33	GND	GND	BE2
AU35	GND	GND	BE29
AU38	GND	GND	BE3
AU42	GND	GND	BE39
AU43	GND	GND	BE41
AU44	GND	GND	BE45
AU5	GND	GND	BE5
AU6	GND	GND	BE6
AV12	GND	GND	BE9
AV20	GND	GND	BF16
AV3	GND	GND	BF26
AV30	GND	GND	BF3
AV35	GND	GND	BF36
AV36	GND	GND	BF41
AV37	GND	GND	BF44
AV4	GND	GND	BF6
AV40	GND	GND	C1
AV42	GND	GND	C11
AV45	GND	GND	C12
AV46	GND	GND	C15
AV5	GND	GND	C2
AV8	GND	GND	C25
AW1	GND	GND	C35
AW10	GND	GND	C41
AW11	GND	GND	C44
AW12	GND	GND	C46
AW17	GND	GND	C5
AW2	GND	GND	D12
AW27	GND	GND	D22
AW37	GND	GND	D3
AW39	GND	GND	D32
AW42	GND	GND	D4
AW43	GND	GND	D41
AW44	GND	GND	D42
AW5	GND	GND	D44
AW6	GND	GND	D5
AY1	GND	GND	D9
AY10	GND	GND	E1
AY14	GND	GND	E10
AY2	GND	GND	E12
AY24	GND	GND	E19
AY3	GND	GND	E2
AY34	GND	GND	E29
AY37	GND	GND	E41
AY4	GND	GND	E44
AY41	GND	GND	E45
AY42	GND	GND	E46
AY43	GND	GND	E5
AY44	GND	GND	E6
AY45	GND	GND	F12
AY46	GND	GND	F16
AY5	GND	GND	F26
AY6	GND	GND	F3
AY7	GND	GND	F36
AY8	GND	GND	F39
AY9	GND	GND	F4
B12	GND	GND	F40
B18	GND	GND	F41
B2	GND	GND	F44
B28	GND	GND	F5
B38	GND	GND	F8
B4	GND	GND	G1
B41	GND	GND	G11

GND GND

U66-3
FPGA_VU7P_B2104

G12	GND	GND	R35
G13	GND	GND	R39
G2	GND	GND	R42
G23	GND	GND	R43
G33	GND	GND	R44
G39	GND	GND	R5
G42	GND	GND	R7
G43	GND	GND	T12
G44	GND	GND	T14
G45	GND	GND	T16
G46	GND	GND	T18
G5	GND	GND	T20
G7	GND	GND	T22
H12	GND	GND	T24
H20	GND	GND	T3
H3	GND	GND	T35
H30	GND	GND	T37
H39	GND	GND	T4
H4	GND	GND	T41
H41	GND	GND	T42
H42	GND	GND	T45
H45	GND	GND	T46
H46	GND	GND	T5
H5	GND	GND	T9
H9	GND	GND	U1
J1	GND	GND	U10
J10	GND	GND	U13
J12	GND	GND	U15
J17	GND	GND	U17
J2	GND	GND	U19
J27	GND	GND	U2
J37	GND	GND	U21
J38	GND	GND	U23
J39	GND	GND	U25
J42	GND	GND	U27
J43	GND	GND	U33
J44	GND	GND	U35
J5	GND	GND	U38
J6	GND	GND	U42
K12	GND	GND	U43
K14	GND	GND	U44
K24	GND	GND	U5
K3	GND	GND	U6
K35	GND	GND	V14
K36	GND	GND	V16
K37	GND	GND	V18
K4	GND	GND	V20
K40	GND	GND	V22
K42	GND	GND	V24
K45	GND	GND	V26
K46	GND	GND	V28
K5	GND	GND	V3
K8	GND	GND	V30
L1	GND	GND	V35
L11	GND	GND	V36
L12	GND	GND	V4
L2	GND	GND	V40
L21	GND	GND	V42
L31	GND	GND	V45
L35	GND	GND	V46
L39	GND	GND	V5
L42	GND	GND	V8
L43	GND	GND	W1
L44	GND	GND	W11
L5	GND	GND	W13
L7	GND	GND	W15
M12	GND	GND	W17
M18	GND	GND	W19
M28	GND	GND	W2
M3	GND	GND	W21
M35	GND	GND	W23
M37	GND	GND	W25
M4	GND	GND	W27
M41	GND	GND	W29
M42	GND	GND	W35
M45	GND	GND	W39
M46	GND	GND	W42
M5	GND	GND	W43
M9	GND	GND	W44
N1	GND	GND	W5
N10	GND	GND	W7
N12	GND	GND	Y14
N15	GND	GND	Y16
N2	GND	GND	Y18
N25	GND	GND	Y20
N35	GND	GND	Y22
N38	GND	GND	Y24
N42	GND	GND	Y26
N43	GND	GND	Y28
N44	GND	GND	Y3
N5	GND	GND	Y34
N6	GND	GND	Y35
P12	GND	GND	Y37
P22	GND	GND	Y4
P3	GND	GND	Y41
P32	GND	GND	Y42
P35	GND	GND	Y45
P36	GND	GND	Y46
P4	GND	GND	Y5
P40	GND	GND	Y9
P42	GND	GND	
P45	GND	GND	
P46	GND	GND	
P5	GND	GND	
P8	GND	GND	
R1	GND	GND	
R10	GND	GND	
R19	GND	GND	
R2	GND	GND	
R29	GND	GND	

GND GND

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title
6.01: VU7P FPGA GND

Size	Document Number	Rev
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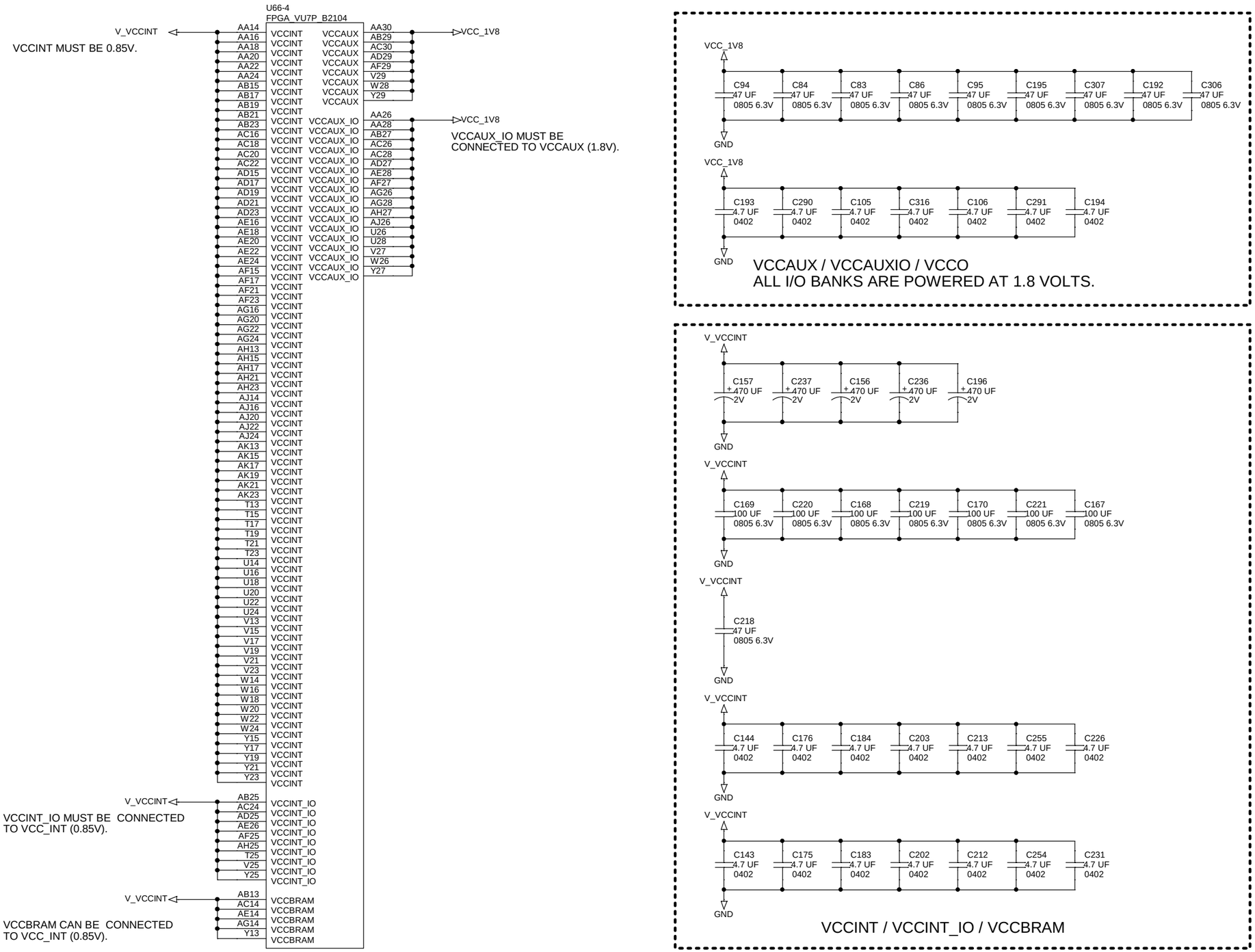

BYPASS CAPACITOR VALUES AND QUANTITIES FROM "xtp427-ultrascale-plus-schematic-review-checklist.xls"

QUANTITIES BASE ON POSSIBLE UPGRADE TO VU9P

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.02: VU7P FPGA INTERNAL POWER		
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U66-7
FPGA_VU7P_B2104

V_MGTY1_AVCC
C139 47 UF 0805 6.3V
C145 4.7 UF 0402
C136 0.1 UF 0402
GND
AD36 MGTAVCC_LN
AF37 MGTAVCC_LN
L38 MGTAVCC_LN
M36 MGTAVCC_LN
N39 MGTAVCC_LN
P37 MGTAVCC_LN
R38 MGTAVCC_LN
T36 MGTAVCC_LN
U39 MGTAVCC_LN
V37 MGTAVCC_LN

C138 47 UF 0805 6.3V
C142 4.7 UF 0402
C133 0.1 UF 0402
AG38 MGTAVCC_LS
AL38 MGTAVCC_LS
AM36 MGTAVCC_LS
AP37 MGTAVCC_LS
AR38 MGTAVCC_LS
AT36 MGTAVCC_LS
AW38 MGTAVCC_LS
AY40 MGTAVCC_LS

V_MGTY2_AVCC
C259 47 UF 0805 6.3V
C256 4.7 UF 0402
C268 0.1 UF 0402
A11 MGTAVCC_RN
A7 MGTAVCC_RN
B9 MGTAVCC_RN
C10 MGTAVCC_RN
E11 MGTAVCC_RN
G10 MGTAVCC_RN
J11 MGTAVCC_RN
L10 MGTAVCC_RN
N11 MGTAVCC_RN
W10 MGTAVCC_RN

C258 47 UF 0805 6.3V
C253 4.7 UF 0402
C265 0.1 UF 0402
AA11 MGTAVCC_RS
AG10 MGTAVCC_RS
AJ11 MGTAVCC_RS
AL10 MGTAVCC_RS
AN11 MGTAVCC_RS
AP9 MGTAVCC_RS
AR10 MGTAVCC_RS
AU11 MGTAVCC_RS
AV9 MGTAVCC_RS
AW7 MGTAVCC_RS

0603 10K R495
VCC_3V3
/V_MGTY1_VCCAUX_EN
PG 18
U54
/EN OUT 8,9
IN IN 3,4
SENSE 7
/RESET 6
NC2 2
NC12 12
NC13 13
NC14 14
NC15 15
NC16 16
NC18 18
NC19 19
GND 1,10,11,17,20,21
PAD
TPS75218
C776 4.7 UF 0402
C777 0.1 UF 0402
V_MGTY1_VCCAUX
C114 100 UF 6.3V 3216
C126 0.1 UF 0402
GND
AB36 MGTVCCAUX_LN
Y36 MGTVCCAUX_LN
AH36 MGTVCCAUX_LS
AK36 MGTVCCAUX_LS
C135 4.7 UF 0402
C134 4.7 UF 0402

0603 10K R408
VCC_3V3
/V_MGTY2_VCCAUX_EN
PG 18
U99
TPS75218
C727 4.7 UF 0402
C728 0.1 UF 0402
V_MGTY2_VCCAUX
C299 100 UF 6.3V 3216
C302 0.1 UF 0402
R11 MGTVCCAUX_RN
U11 MGTVCCAUX_RN
AC11 MGTVCCAUX_RS
AE11 MGTVCCAUX_RS
C267 4.7 UF 0402
C266 4.7 UF 0402

PLACE CAPACITORS
THAT ARE TO THE RIGHT
OF THIS LINE NEAR THE
BGA PINS.

U66-8

V_MGTY1_AVTT
C123 47 UF 0805 6.3V
C125 4.7 UF 0402
C113 0.1 UF 0402
GND
AA39 MGTAVTT_LN
AB41 MGTAVTT_LN
AC38 MGTAVTT_LN
AD40 MGTAVTT_LN
AE39 MGTAVTT_LN
AF41 MGTAVTT_LN
C45 MGTAVTT_LN
D43 MGTAVTT_LN
F42 MGTAVTT_LN
F43 MGTAVTT_LN
H40 MGTAVTT_LN
K41 MGTAVTT_LN
M40 MGTAVTT_LN
P41 MGTAVTT_LN
T40 MGTAVTT_LN
V41 MGTAVTT_LN
W38 MGTAVTT_LN
Y40 MGTAVTT_LN
R91 0 0402
B42 MGTAVTTRCAL_LN
R88 100 0402
B43 MGTRREF_LN

C122 47 UF 0805 6.3V
C112 4.7 UF 0402
C124 0.1 UF 0402
AH40 MGTAVTT_LS
AJ39 MGTAVTT_LS
AK41 MGTAVTT_LS
AM40 MGTAVTT_LS
AN39 MGTAVTT_LS
AP41 MGTAVTT_LS
AT40 MGTAVTT_LS
AU39 MGTAVTT_LS
AV41 MGTAVTT_LS
BA42 MGTAVTT_LS
BA43 MGTAVTT_LS
BC43 MGTAVTT_LS
BD45 MGTAVTT_LS
BE44 MGTAVTT_LS
R90 0 0402
BE42 MGTAVTTRCAL_LS
R87 100 0402
BE43 MGTRREF_LS

V_MGTY2_AVTT
C280 47 UF 0805 6.3V
C275 4.7 UF 0402
C285 0.1 UF 0402
B3 MGTAVTT_RN
D8 MGTAVTT_RN
E7 MGTAVTT_RN
F9 MGTAVTT_RN
G6 MGTAVTT_RN
H8 MGTAVTT_RN
J7 MGTAVTT_RN
K9 MGTAVTT_RN
L6 MGTAVTT_RN
M8 MGTAVTT_RN
N7 MGTAVTT_RN
P9 MGTAVTT_RN
R6 MGTAVTT_RN
T8 MGTAVTT_RN
U7 MGTAVTT_RN
V9 MGTAVTT_RN
W6 MGTAVTT_RN
Y8 MGTAVTT_RN
R146 0 0402
C7 MGTAVTTRCAL_RN
R151 100 0402
C6 MGTRREF_RN

C282 47 UF 0805 6.3V
C274 4.7 UF 0402
C284 0.1 UF 0402
AB9 MGTAVTT_RS
AC6 MGTAVTT_RS
AD8 MGTAVTT_RS
AE7 MGTAVTT_RS
AF9 MGTAVTT_RS
AG6 MGTAVTT_RS
AH8 MGTAVTT_RS
AJ7 MGTAVTT_RS
AK9 MGTAVTT_RS
AL6 MGTAVTT_RS
AM8 MGTAVTT_RS
AN7 MGTAVTT_RS
AR6 MGTAVTT_RS
AT8 MGTAVTT_RS
AU7 MGTAVTT_RS
BC5 MGTAVTT_RS
BD2 MGTAVTT_RS
BE4 MGTAVTT_RS
R145 0 0402
BA5 MGTAVTTRCAL_RS
R150 100 0402
BA4 MGTRREF_RS

FPGA_VU7P_B2104

REFER TO THE GTY/GTH USER
GUIDES FOR DETAILS ON TRACE
ROUTING FOR THIS RESISTOR.

PLACE CAPACITORS AND RESISTORS
THAT ARE TO THE RIGHT OF THIS LINE
NEAR THE BGA PINS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.03: VU7P GTY TRANSCEIVER POWER		
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MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

V_VCCINT — R478 DNP 0603 — AD12
GND — R480 0 0603 — AD12
GND — R449 0 0603 — W12
VCC_1V8 — R463 DNP 0603 — AA12
GND — R474 0 0603 — AA12
VCC_1V8 — R682 1K 0402 — R12
V_CONFIG_BIT_M2 PG 17 — R12
VCC_1V8 — R459 DNP 0603 — U12
GND — R461 0 0603 — U12
VCC_1V8 — R450 0 0603 — V12
GND — R451 DNP 0603 — V12

U66-6
FPGA_VU7P_B2104
BANK 0

POR_OVERRIDE
RSVDGND
PUDC_B_0
M2_0
M1_0
M0_0
VCCO_0 (AD13)
VCCO_0 (AF13) — VCC_1V8 — C292 47 UF 0805 6.3V — GND
D00_MOSI_0 (AK12)
D01_DIN_0 (AJ12)
D02_0 (AL12)
D03_0 (AH12)
RDWR_FCS_B_0 (AG12)
CCLK_0 (AG13)
PROGRAM_B_0 (AE12)
DONE_0 (AC12) — 0603 4.7K R21 — VCC_1V8 — V_FPGA_DONE
INIT_B_0 (Y12) — 0603 4.7K R453 — VCC_1V8 — V_FPGA_INIT_B
VBATT (AM12) — GND

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

VCC_1V8 — R406 2.2K 0603
VCC_1V8 — R409 4.7K 0603
R407 4.7K 0603

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

U98
MT25QU01
15 DQ0
8 DQ1
9 DQ2
1 DQ3
7 S#
16 CLK
DNU_3 3, DNU_4 4, DNU_5 5, DNU_6 6, DNU_11 11, DNU_12 12, DNU_13 13, DNU_14 14
VCC 2 — VCC_1V8
GND 10 — GND
C729 0.1 UF 0402

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

PULLUPS/PULLDOWNS ON THE
BOOT MODE CONFIGURATION
INPUTS MUST BE 1K OR LESS.

/V_FPGA_DONE PG 11
0603 4.7K R7
D7 LED GREEN R6 150 — VCC_3V3
Q5 FET_N_1.8V
GND

VU7P DONE LED

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/V_FPGA_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE TM4C CONTROLLER.

0603 4.7K R713 — VCC_1V8
V_FPGA_PROGRAM PG 11
Q27 FET_N_1.8V
GND — R712 4.7K 0603 — GND
GND
SW3 SW PUSHBUTTON
GND

THE FPGA CAN BE REPROGRAMMED EITHER BY PULSING "V_FPGA_PROGRAM" FROM THE TM4C CONTROLLER, OR BY ACTIVATING THE FRONT PANEL "REPROGRAM" SWITCH.

FRONT PANEL REPROGRAM

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 6.04: VU7P FPGA CONFIGURATION			
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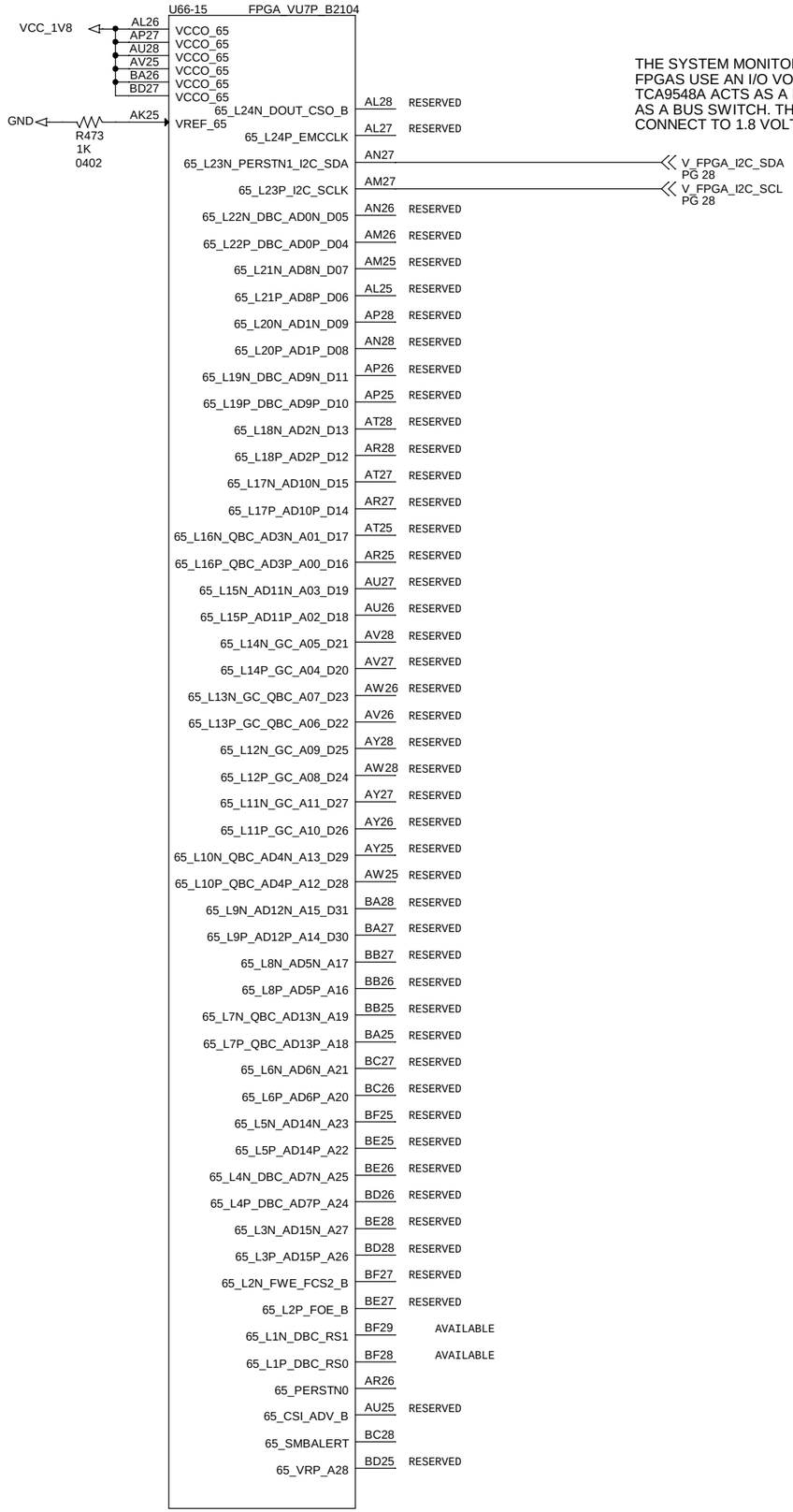

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.05: VU7P BANK 65

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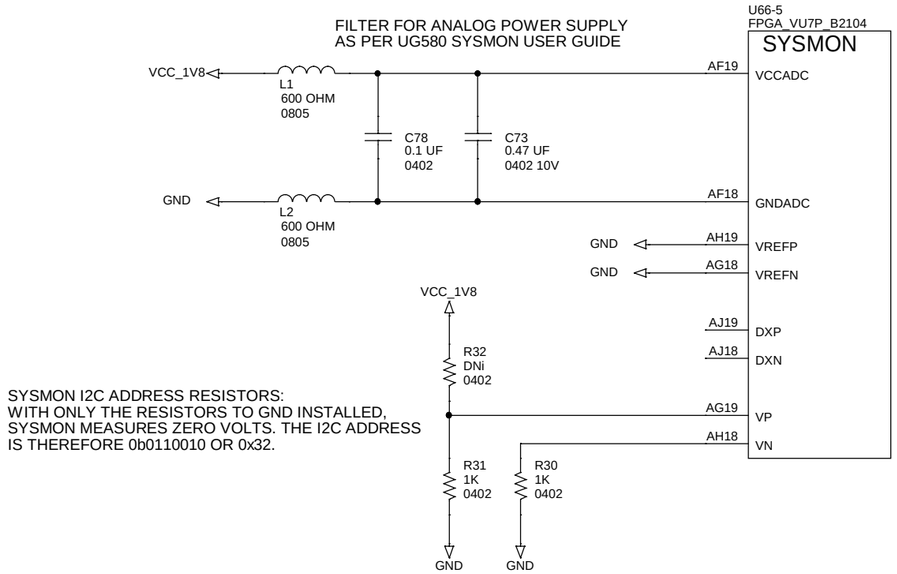

SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.06: VU7P SYSTEM MONITOR		
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THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

U66-10

ac_nV_UTIL_CLK_CHAN2 PG 16		BC37	IO_L10N_T1U_N7_QBC_AD4N_	VCCO_45	AM33
ac_pV_UTIL_CLK_CHAN2 PG 16		BB37	IO_L10P_T1U_N6_QBC_AD4P_	VCCO_45	AR34
nKV_SPARE0 PG 37	nKV_SPARE0	BC36	IO_L11N_T1U_N9_GC_45	VCCO_45	BA36
pKV_SPARE0 PG 37	pKV_SPARE0	BB36	IO_L11P_T1U_N8_GC_45	VCCO_45	BB33
nKV_SPARE2 PG 37	nKV_SPARE2	BB35	IO_L12N_T1U_N11_GC_45	VCCO_45	BC40
pKV_SPARE2 PG 37	pKV_SPARE2	BA35	IO_L12P_T1U_N10_GC_45	VCCO_45	BD37
		BB34	IO_L13N_T2L_N1_GC_QBC_45	VCCO_45	BE34
		BA34	IO_L13P_T2L_N0_GC_QBC_45	VREF_45	AK33
		AY36	IO_L14N_T2L_N3_GC_45		
		AY35	IO_L14P_T2L_N2_GC_45		
		BA33	IO_L15N_T2L_N5_AD11N_45		
		AY33	IO_L15P_T2L_N4_AD11P_45		
nKV_SPARE5 PG 37	nKV_SPARE5	AW36	IO_L16N_T2U_N7_QBC_AD3N_		
pKV_SPARE5 PG 37	pKV_SPARE5	AW35	IO_L16P_T2U_N6_QBC_AD3P_		
		AW34	IO_L17N_T2U_N9_AD10N_45		
		AV34	IO_L17P_T2U_N8_AD10P_45		
nKV_SPARE4 PG 37	nKV_SPARE4	AW33	IO_L18N_T2U_N11_AD2N_45		
pKV_SPARE4 PG 37	pKV_SPARE4	AV33	IO_L18P_T2U_N10_AD2P_45		
nKV_SPARE8 PG 37	nKV_SPARE8	AT34	IO_L19N_T3L_N1_DBC_AD9N_		
pKV_SPARE8 PG 37	pKV_SPARE8	AT33	IO_L19P_T3L_N0_DBC_AD9P_		
nKV_SPARE9 PG 37	nKV_SPARE9	BF40	IO_L1N_T0L_N1_DBC_45		
pKV_SPARE9 PG 37	pKV_SPARE9	BF39	IO_L1P_T0L_N0_DBC_45		
nV_TTS_OUT PG 14		AR33	IO_L20N_T3L_N3_AD1N_45		
pV_TTS_OUT PG 14		AP33	IO_L20P_T3L_N2_AD1P_45		
nV_CDR_DATA PG 14		AP34	IO_L21N_T3L_N5_AD8N_45		
pV_CDR_DATA PG 14		AN34	IO_L21P_T3L_N4_AD8P_45		
ac_nV_TTC_CLK40 PG 14		AN33	IO_L22N_T3U_N7_DBC_AD0N_		
ac_pV_TTC_CLK40 PG 14		AN32	IO_L22P_T3U_N6_DBC_AD0P_		
		AM32	IO_L23N_T3U_N9_45		
		AL32	IO_L23P_T3U_N8_45		
		AM34	IO_L24N_T3U_N11_45		
		AL34	IO_L24P_T3U_N10_45		
nKV_SPARE11 PG 37	nKV_SPARE11	BF38	IO_L2N_T0L_N3_45		
pKV_SPARE11 PG 37	pKV_SPARE11	BE38	IO_L2P_T0L_N2_45		
nKV_SPARE12 PG 37	nKV_SPARE12	BF37	IO_L3N_T0L_N5_AD15N_45		
pKV_SPARE12 PG 37	pKV_SPARE12	BE37	IO_L3P_T0L_N4_AD15P_45		
nKV_SPARE7 PG 37	nKV_SPARE7	BE40	IO_L4N_T0U_N7_DBC_AD7N_4		
pKV_SPARE7 PG 37	pKV_SPARE7	BD40	IO_L4P_T0U_N6_DBC_AD7P_4		
nKV_SPARE3 PG 37	nKV_SPARE3	BD39	IO_L5N_T0U_N9_AD14N_45		
pKV_SPARE3 PG 37	pKV_SPARE3	BC39	IO_L5P_T0U_N8_AD14P_45		
nKV_SPARE1 PG 37	nKV_SPARE1	BC38	IO_L6N_T0U_N11_AD6N_45		
pKV_SPARE1 PG 37	pKV_SPARE1	BB38	IO_L6P_T0U_N10_AD6P_45		
nKV_SPARE10 PG 37	nKV_SPARE10	BD34	IO_L7N_T1L_N1_QBC_AD13N_		
pKV_SPARE10 PG 37	pKV_SPARE10	BC34	IO_L7P_T1L_N0_QBC_AD13P_		
		BE35	IO_L8N_T1L_N3_AD5N_45		
		BD35	IO_L8P_T1L_N2_AD5P_45		
nKV_SPARE6 PG 37	nKV_SPARE6	BE36	IO_L9N_T1L_N5_AD12N_45		
pKV_SPARE6 PG 37	pKV_SPARE6	BD36	IO_L9P_T1L_N4_AD12P_45		
GND R89 240 0402		BD38	IO_T0U_N12_VRP_45		
		BF35	IO_T1U_N12_45		
VU7P_TO_TM4C_0 PG 17		AU34	IO_T2U_N12_45		
VU7P_FROM_TM4C_0 PG 17		AL33	IO_T3U_N12_45		

FPGA_VU7P_B2104

VCC_1V8

R475 1K 0402 GND

THESE CLOCK SIGNALS CONNECT TO ONE SIDE OF THE "SLR" BOUNDARY.

ac_nV_UTIL_CLK_CHAN3 PG 16
ac_pV_UTIL_CLK_CHAN3 PG 16

LOGIC FABRIC BOTTOM

U66-14

	K27	IO_L10N_T1U_N7_QBC_AD4N_	VCCO_52	C30	
	K26	IO_L10P_T1U_N6_QBC_AD4P_	VCCO_52	D27	
	H28	IO_L11N_T1U_N9_GC_52	VCCO_52	G28	
	H27	IO_L11P_T1U_N8_GC_52	VCCO_52	K29	
	J29	IO_L12N_T1U_N11_GC_52	VCCO_52	L26	
	J28	IO_L12P_T1U_N10_GC_52	VCCO_52	P27	
	H26	IO_L13N_T2L_N1_GC_QBC_52			
	J26	IO_L13P_T2L_N0_GC_QBC_52	VREF_52	T29	
	G27	IO_L14N_T2L_N3_GC_52			
	G26	IO_L14P_T2L_N2_GC_52			
	G29	IO_L15N_T2L_N5_AD11N_52			
	H29	IO_L15P_T2L_N4_AD11P_52			
	F29	IO_L16N_T2U_N7_QBC_AD3N_			
	F28	IO_L16P_T2U_N6_QBC_AD3P_			
	E27	IO_L17N_T2U_N9_AD10N_52			
	F27	IO_L17P_T2U_N8_AD10P_52			
	D28	IO_L18N_T2U_N11_AD2N_52			
	E28	IO_L18P_T2U_N10_AD2P_52			
V_LED_BLUE PG 17	B27	IO_L19N_T3L_N1_DBC_AD9N_			
	C27	IO_L19P_T3L_N0_DBC_AD9P_			
	R28	IO_L1N_T0L_N1_DBC_52			
	T28	IO_L1P_T0L_N0_DBC_52			
	C29	IO_L20N_T3L_N3_AD1N_52			
	D29	IO_L20P_T3L_N2_AD1P_52			
	D30	IO_L21N_T3L_N5_AD8N_52			
	E30	IO_L21P_T3L_N4_AD8P_52			
V_DIP_SW_1 PG 17	A28	IO_L22N_T3U_N7_DBC_AD0N_			
V_DIP_SW_2 PG 17	A27	IO_L22P_T3U_N6_DBC_AD0P_			
	A29	IO_L23N_T3U_N9_52			
V_LED_RED PG 17	B29	IO_L23P_T3U_N8_52			
V_LED_GREEN PG 17	A30	IO_L24N_T3U_N11_52			
	B30	IO_L24P_T3U_N10_52			
	R27	IO_L2N_T0L_N3_52			
	T27	IO_L2P_T0L_N2_52			
	R26	IO_L3N_T0L_N5_AD15N_52			
	T26	IO_L3P_T0L_N4_AD15P_52			
	N29	IO_L4N_T0U_N7_DBC_AD7N_5			
	P29	IO_L4P_T0U_N6_DBC_AD7P_5			
	N28	IO_L5N_T0U_N9_AD14N_52			
	P28	IO_L5P_T0U_N8_AD14P_52			
	N26	IO_L6N_T0U_N11_AD6N_52			
	P26	IO_L6P_T0U_N10_AD6P_52			
	L29	IO_L7N_T1L_N1_QBC_AD13N_			
	M29	IO_L7P_T1L_N0_QBC_AD13P_			
	K28	IO_L8N_T1L_N3_AD5N_52			
	L28	IO_L8P_T1L_N2_AD5P_52			
	L27	IO_L9N_T1L_N5_AD12N_52			
	M27	IO_L9P_T1L_N4_AD12P_52			
GND R467 240 0402	N27	IO_T0U_N12_VRP_52			
	M26	IO_T1U_N12_52			
	E26	IO_T2U_N12_52			
	C28	IO_T3U_N12_52			

FPGA_VU7P_B2104

VCC_1V8

R471 1K 0402 GND

THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

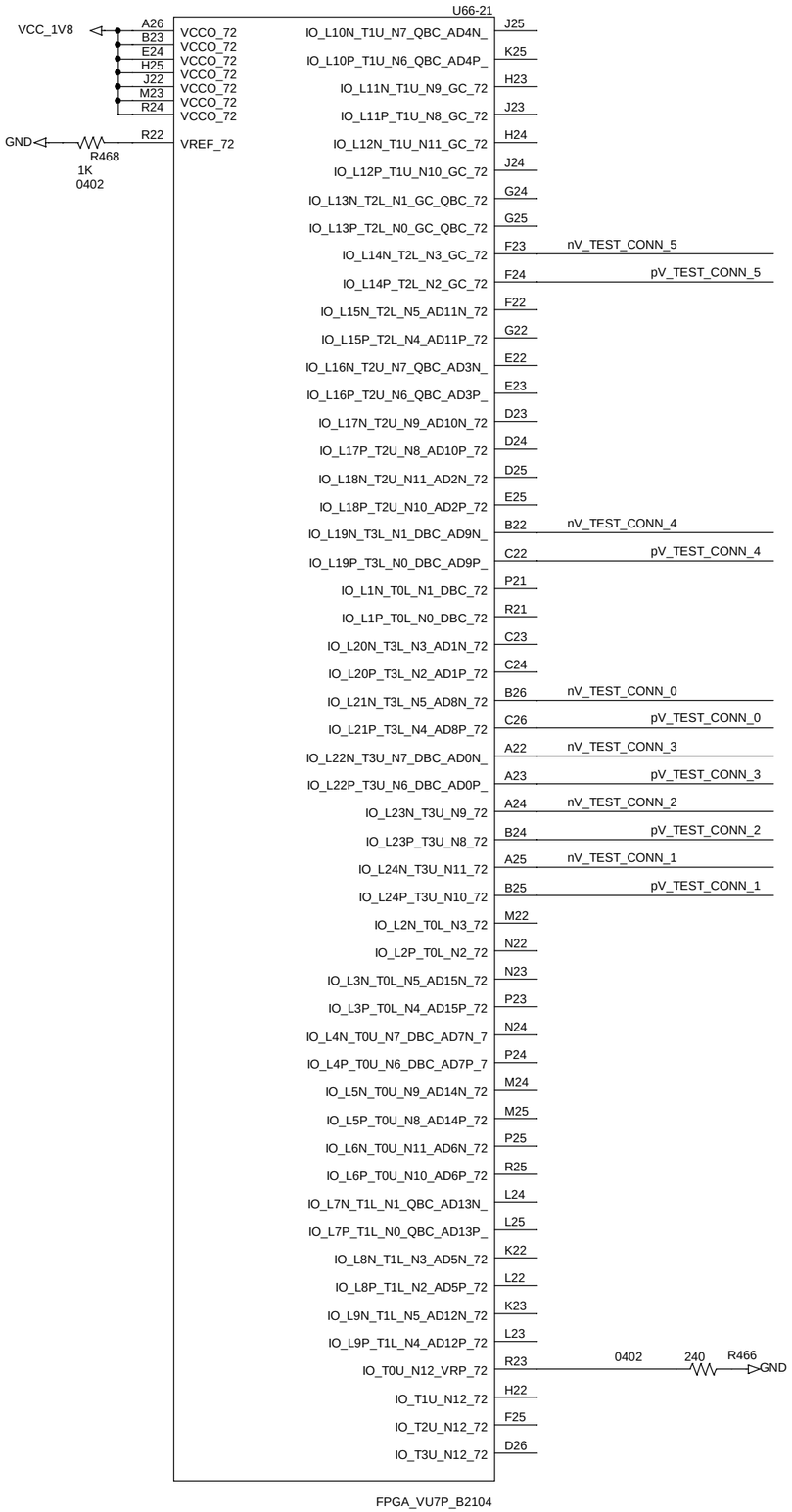
THE "KV_SPARE0" AND "KV_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE VU7P.

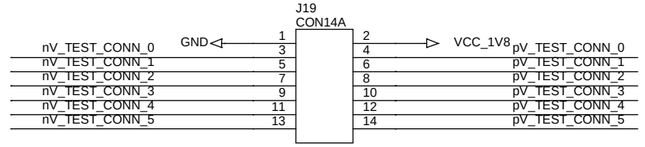
ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.07 VU7P UTILITY BANKS

Size: | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 46 of 74





THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "V_TEST_CONN_5" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.08 VU7P TEST CONNECTOR

Size	Document Number	Rev
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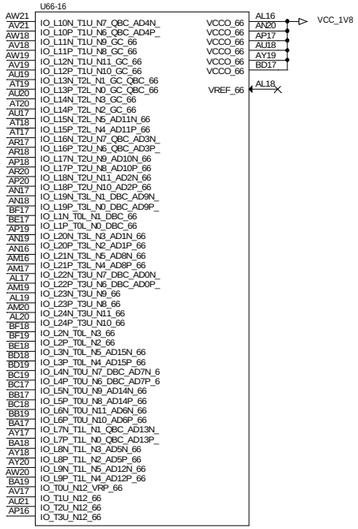
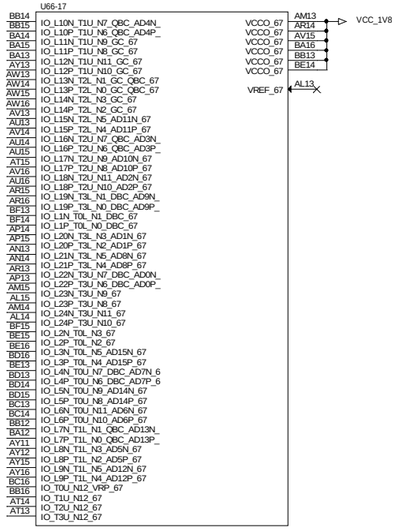
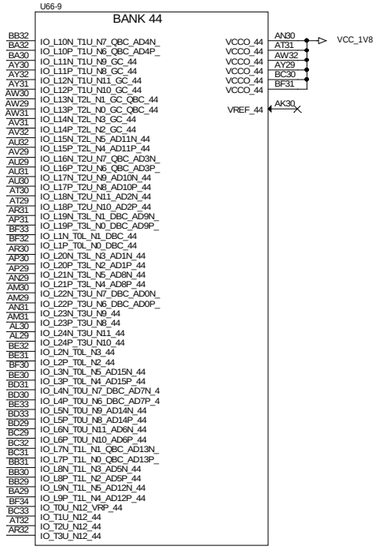
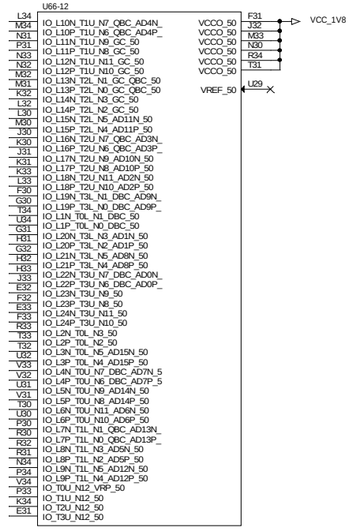
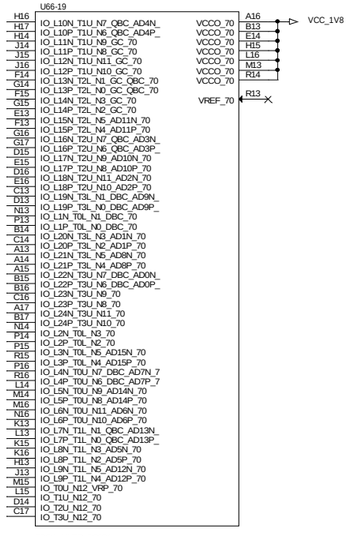
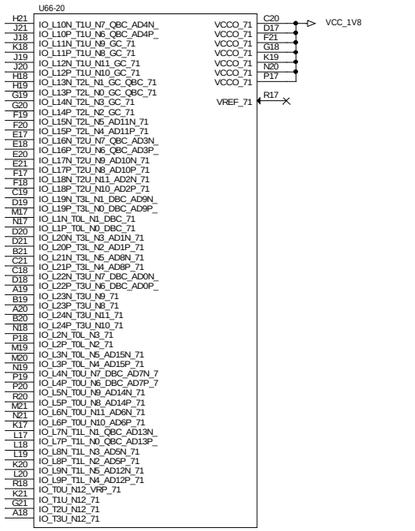


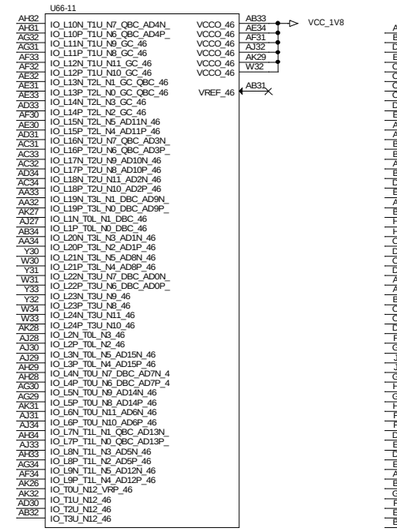


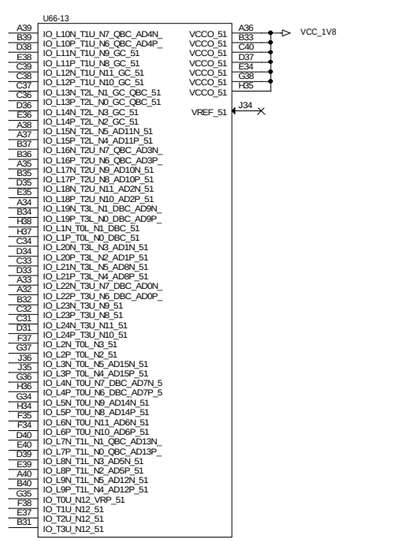


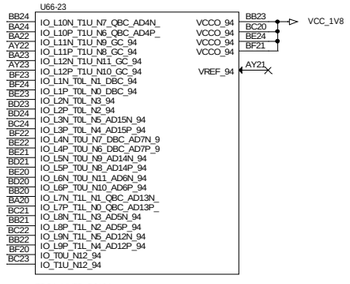


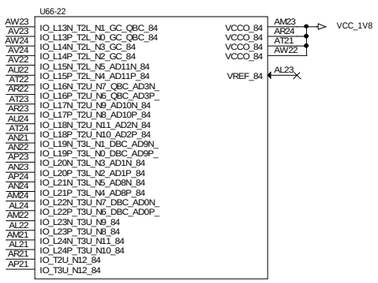


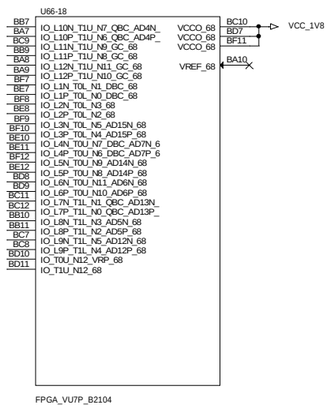












ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.99: VU7P UNUSED BLOCKS

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 48 of 74

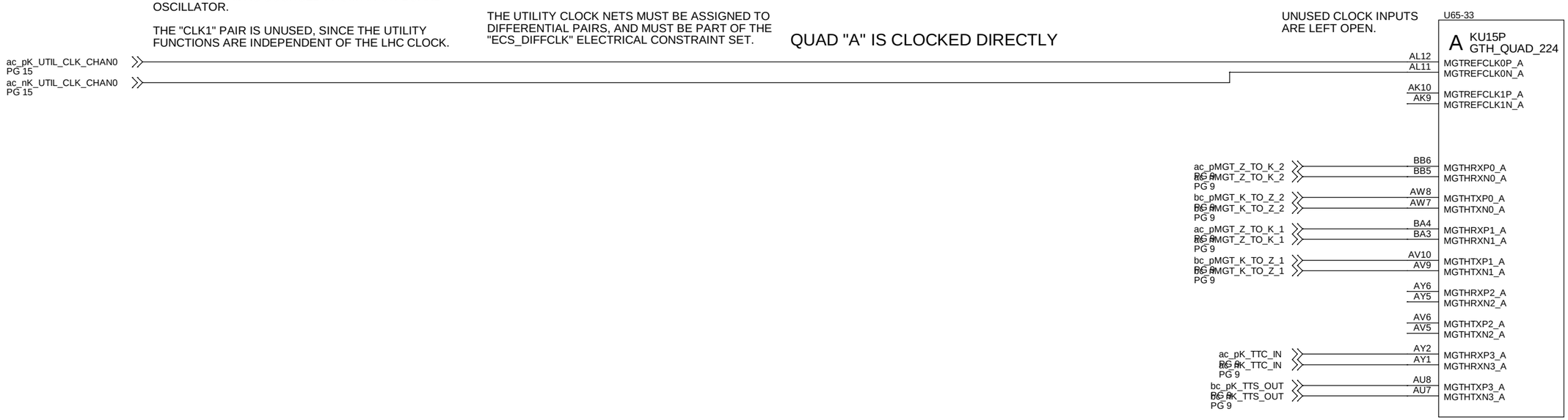
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.01: KU15P QUAD A UTILITY #1		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 49 of 74	

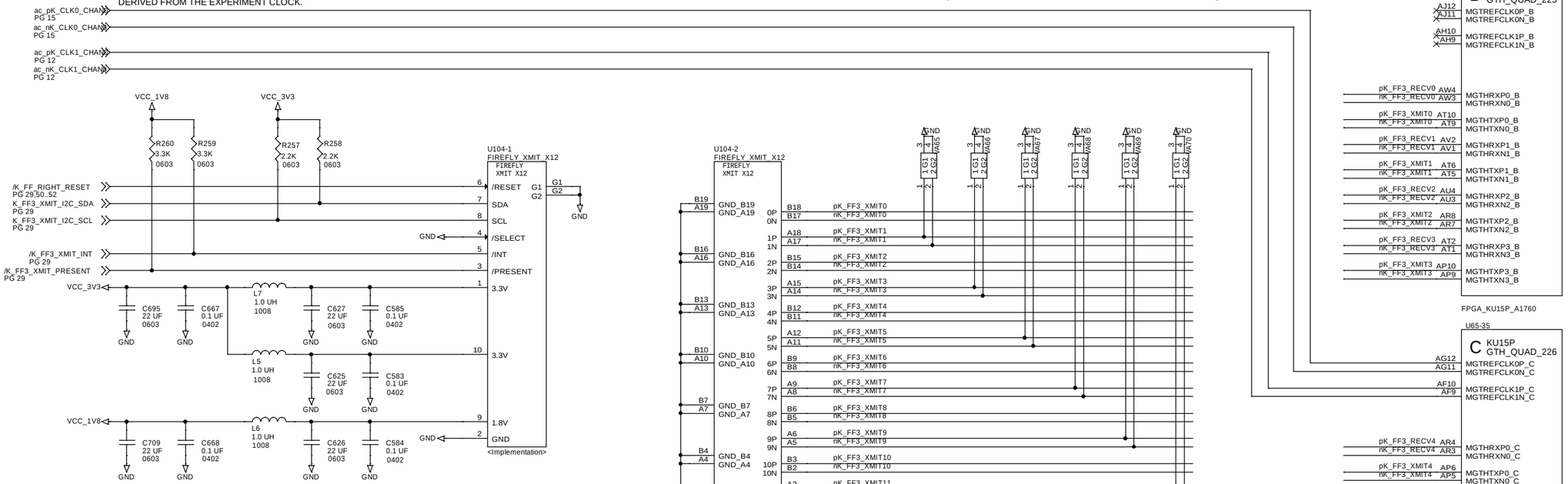
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

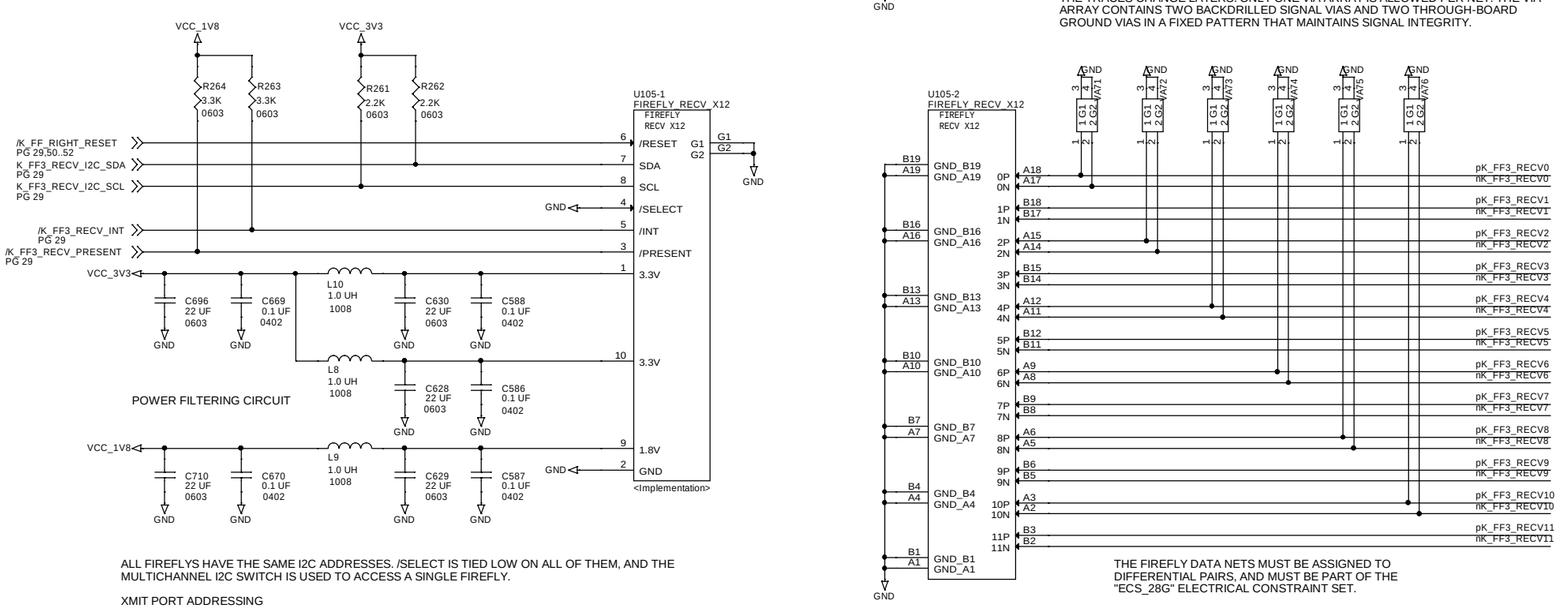
QUADS "B" AND "D" ARE CLOCKED FROM QUAD "C"

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.02: KU15P QUADS BCD FIREFLY X12 #3

Size	Document Number	Rev
	6089-103	A

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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "E" AND "G" ARE CLOCKED FROM QUAD "F"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN PG 15
ac_nK_CLK0_CHAN PG 15
ac_pK_CLK1_CHAN PG 12
ac_nK_CLK1_CHAN PG 12

U65-37
E KU15P GTH_QUAD_228
AC12 MGTREFCLK0P_E
AC11 MGTREFCLK0N_E
AB10 MGTREFCLK1P_E
AB9 MGTREFCLK1N_E

pK_FF2_RECV0 AG4 MGTHRXP0_E
nK_FF2_RECV0 AG3 MGTHRXN0_E
pK_FF2_XMIT0 AG8 MGTHTXP0_E
nK_FF2_XMIT0 AG7 MGTHTXN0_E
pK_FF2_RECV1 AF2 MGTHRXP1_E
nK_FF2_RECV1 AF1 MGTHRXN1_E
pK_FF2_XMIT1 AF6 MGTHTXP1_E
nK_FF2_XMIT1 AF5 MGTHTXN1_E
pK_FF2_RECV2 AE4 MGTHRXP2_E
nK_FF2_RECV2 AE3 MGTHRXN2_E
pK_FF2_XMIT2 AE8 MGTHTXP2_E
nK_FF2_XMIT2 AE7 MGTHTXN2_E
pK_FF2_RECV3 AD2 MGTHRXP3_E
nK_FF2_RECV3 AD1 MGTHRXN3_E
pK_FF2_XMIT3 AD6 MGTHTXP3_E
nK_FF2_XMIT3 AD5 MGTHTXN3_E

FPGA_KU15P_A1760

U65-38
F KU15P GTH_QUAD_229
AA12 MGTREFCLK0P_F
AA11 MGTREFCLK0N_F
Y10 MGTREFCLK1P_F
Y9 MGTREFCLK1N_F

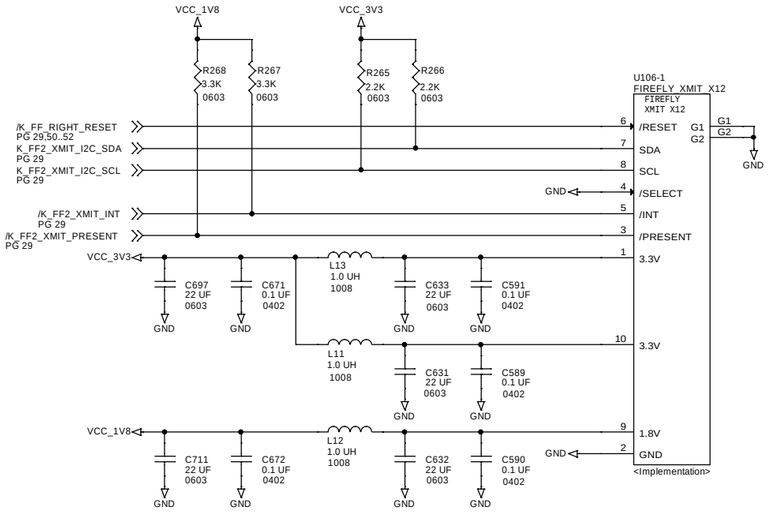
pK_FF2_RECV4 AC4 MGTHRXP0_F
nK_FF2_RECV4 AC3 MGTHRXN0_F
pK_FF2_XMIT4 AC8 MGTHTXP0_F
nK_FF2_XMIT4 AC7 MGTHTXN0_F
pK_FF2_RECV5 AB2 MGTHRXP1_F
nK_FF2_RECV5 AB1 MGTHRXN1_F
pK_FF2_XMIT5 AB6 MGTHTXP1_F
nK_FF2_XMIT5 AB5 MGTHTXN1_F
pK_FF2_RECV6 AA4 MGTHRXP2_F
nK_FF2_RECV6 AA3 MGTHRXN2_F
pK_FF2_XMIT6 AA8 MGTHTXP2_F
nK_FF2_XMIT6 AA7 MGTHTXN2_F
pK_FF2_RECV7 Y2 MGTHRXP3_F
nK_FF2_RECV7 Y1 MGTHRXN3_F
pK_FF2_XMIT7 Y6 MGTHTXP3_F
nK_FF2_XMIT7 Y5 MGTHTXN3_F

FPGA_KU15P_A1760

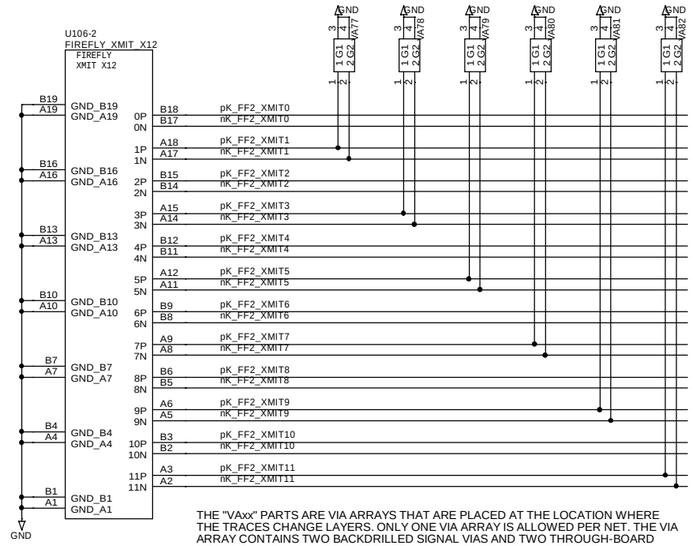
U65-39
G KU15P GTH_QUAD_230
W12 MGTREFCLK0P_G
W11 MGTREFCLK0N_G
V10 MGTREFCLK1P_G
V9 MGTREFCLK1N_G

pK_FF2_RECV8 W4 MGTHRXP0_G
nK_FF2_RECV8 W3 MGTHRXN0_G
pK_FF2_XMIT8 W8 MGTHTXP0_G
nK_FF2_XMIT8 W7 MGTHTXN0_G
pK_FF2_RECV9 V2 MGTHRXP1_G
nK_FF2_RECV9 V1 MGTHRXN1_G
pK_FF2_XMIT9 V6 MGTHTXP1_G
nK_FF2_XMIT9 V5 MGTHTXN1_G
pK_FF2_RECV10 U4 MGTHRXP2_G
nK_FF2_RECV10 U3 MGTHRXN2_G
pK_FF2_XMIT10 U8 MGTHTXP2_G
nK_FF2_XMIT10 U7 MGTHTXN2_G
pK_FF2_RECV11 T2 MGTHRXP3_G
nK_FF2_RECV11 T1 MGTHRXN3_G
pK_FF2_XMIT11 T6 MGTHTXP3_G
nK_FF2_XMIT11 T5 MGTHTXN3_G

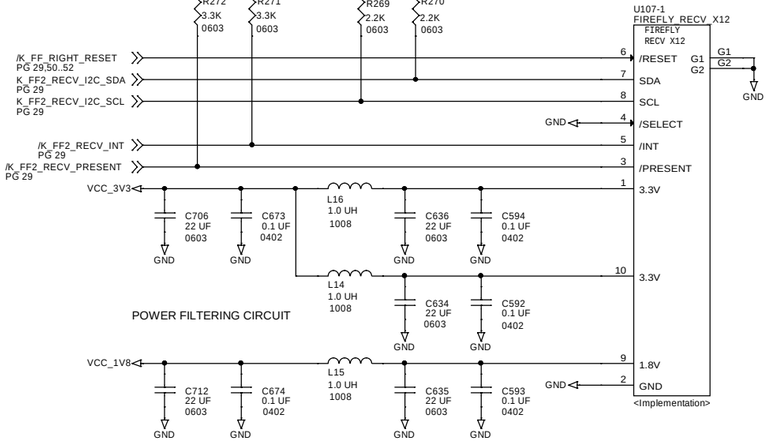
FPGA_KU15P_A1760



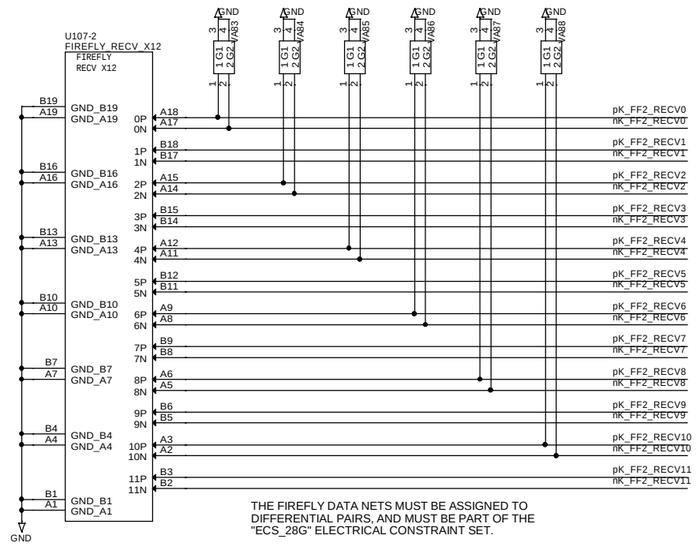
ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



POWER FILTERING CIRCUIT



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.03: KU15P QUADS EFG FIREFLY X12 #2

Size | Document Number: 6089-103 | Rev: A

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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN PG 15
ac_nK_CLK0_CHAN PG 15
ac_pK_CLK1_CHAN PG 12
ac_nK_CLK1_CHAN PG 12

U65-40 FPGA_KU15P_A1760
H KU15P GTH_QUAD_231
U12 MGTREFCLK0P_H
U11 MGTREFCLK0N_H
T10 MGTREFCLK1P_H
T9 MGTREFCLK1N_H

pK_FF1_RECV0 R4 MGTHRXP0_H
nK_FF1_RECV0 R3 MGTHRXN0_H
pK_FF1_XMIT0 R8 MGTHTXP0_H
nK_FF1_XMIT0 R7 MGTHTXN0_H
pK_FF1_RECV1 P2 MGTHRXP1_H
nK_FF1_RECV1 P1 MGTHRXN1_H
pK_FF1_XMIT1 P6 MGTHTXP1_H
nK_FF1_XMIT1 P5 MGTHTXN1_H
pK_FF1_RECV2 N4 MGTHRXP2_H
nK_FF1_RECV2 N3 MGTHRXN2_H
pK_FF1_XMIT2 N8 MGTHTXP2_H
nK_FF1_XMIT2 N7 MGTHTXN2_H
pK_FF1_RECV3 M2 MGTHRXP3_H
nK_FF1_RECV3 M1 MGTHRXN3_H
pK_FF1_XMIT3 M6 MGTHTXP3_H
nK_FF1_XMIT3 M5 MGTHTXN3_H

U65-41 FPGA_KU15P_A1760
I KU15P GTH_QUAD_232
R12 MGTREFCLK0P_I
R11 MGTREFCLK0N_I
P10 MGTREFCLK1P_I
P9 MGTREFCLK1N_I

pK_FF1_RECV4 L4 MGTHRXP0_I
nK_FF1_RECV4 L3 MGTHRXN0_I
pK_FF1_XMIT4 L8 MGTHTXP0_I
nK_FF1_XMIT4 L7 MGTHTXN0_I
pK_FF1_RECV5 K2 MGTHRXP1_I
nK_FF1_RECV5 K1 MGTHRXN1_I
pK_FF1_XMIT5 K6 MGTHTXP1_I
nK_FF1_XMIT5 K5 MGTHTXN1_I
pK_FF1_RECV6 J4 MGTHRXP2_I
nK_FF1_RECV6 J3 MGTHRXN2_I
pK_FF1_XMIT6 J8 MGTHTXP2_I
nK_FF1_XMIT6 J7 MGTHTXN2_I
pK_FF1_RECV7 H2 MGTHRXP3_I
nK_FF1_RECV7 H1 MGTHRXN3_I
pK_FF1_XMIT7 H6 MGTHTXP3_I
nK_FF1_XMIT7 H5 MGTHTXN3_I

U65-42 FPGA_KU15P_A1760
J KU15P GTH_QUAD_233
N12 MGTREFCLK0P_J
N11 MGTREFCLK0N_J
M10 MGTREFCLK1P_J
M9 MGTREFCLK1N_J

pK_FF1_RECV8 G4 MGTHRXP0_J
nK_FF1_RECV8 G3 MGTHRXN0_J
pK_FF1_XMIT8 H10 MGTHTXP0_J
nK_FF1_XMIT8 H9 MGTHTXN0_J
pK_FF1_RECV9 F2 MGTHRXP1_J
nK_FF1_RECV9 F1 MGTHRXN1_J
pK_FF1_XMIT9 G8 MGTHTXP1_J
nK_FF1_XMIT9 G7 MGTHTXN1_J
pK_FF1_RECV10 E4 MGTHRXP2_J
nK_FF1_RECV10 E3 MGTHRXN2_J
pK_FF1_XMIT10 F6 MGTHTXP2_J
nK_FF1_XMIT10 F5 MGTHTXN2_J
pK_FF1_RECV11 D2 MGTHRXP3_J
nK_FF1_RECV11 D1 MGTHRXN3_J
pK_FF1_XMIT11 F10 MGTHTXP3_J
nK_FF1_XMIT11 F9 MGTHTXN3_J

VCC_1V8, VCC_3V3
R276 3.3K 0603, R275 3.3K 0603, R273 2.2K 0603, R274 2.2K 0603

U108-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12
/K_FF_RIGHT_RESET PG 29,50..52 → 6 /RESET
K_FF1_XMIT_I2C_SDA PG 29 → 7 SDA
K_FF1_XMIT_I2C_SCL PG 29 → 8 SCL
GND → 4 /SELECT
/K_FF1_XMIT_INT PG 29 → 5 /INT
/K_FF1_XMIT_PRESENT PG 29 → 3 /PRESENT
G1, G2 → GND
1 → 3.3V
10 → 3.3V
9 → 1.8V
2 → GND
<Implementation>

VCC_3V3 → L19 1.0 UH 1008 → 1
C707 22 UF 0603, C675 0.1 UF 0402, C639 22 UF 0603, C597 0.1 UF 0402
L17 1.0 UH 1008 → 10
C637 22 UF 0603, C595 0.1 UF 0402
VCC_1V8 → L18 1.0 UH 1008 → 9
C713 22 UF 0603, C676 0.1 UF 0402, C638 22 UF 0603, C596 0.1 UF 0402

U108-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 B17
B16 A16	GND_B16 GND_A16	1P 1N	A18 A17
B13 A13	GND_B13 GND_A13	2P 2N	B15 B14
B10 A10	GND_B10 GND_A10	3P 3N	A15 A14
B7 A7	GND_B7 GND_A7	4P 4N	B12 B11
B4 A4	GND_B4 GND_A4	5P 5N	A12 A11
B1 A1	GND_B1 GND_A1	6P 6N	B9 B8
		7P 7N	A9 A8
		8P 8N	B7 B6
		9P 9N	A6 A5
		10P 10N	B3 B2
		11P 11N	A3 A2

pK_FF1_XMIT0 / nK_FF1_XMIT0
pK_FF1_XMIT1 / nK_FF1_XMIT1
pK_FF1_XMIT2 / nK_FF1_XMIT2
pK_FF1_XMIT3 / nK_FF1_XMIT3
pK_FF1_XMIT4 / nK_FF1_XMIT4
pK_FF1_XMIT5 / nK_FF1_XMIT5
pK_FF1_XMIT6 / nK_FF1_XMIT6
pK_FF1_XMIT7 / nK_FF1_XMIT7
pK_FF1_XMIT8 / nK_FF1_XMIT8
pK_FF1_XMIT9 / nK_FF1_XMIT9
pK_FF1_XMIT10 / nK_FF1_XMIT10
pK_FF1_XMIT11 / nK_FF1_XMIT11

GND, 1 G1 2 G2, A85, A90, A91, A92, A93, A94

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

VCC_1V8, VCC_3V3
R280 3.3K 0603, R279 3.3K 0603, R277 2.2K 0603, R278 2.2K 0603

U109-1 FIREFLY_RECV_X12 FIREFLY RECV X12
/K_FF_RIGHT_RESET PG 29,50..52 → 6 /RESET
K_FF1_RECV_I2C_SDA PG 29 → 7 SDA
K_FF1_RECV_I2C_SCL PG 29 → 8 SCL
GND → 4 /SELECT
/K_FF1_RECV_INT PG 29 → 5 /INT
/K_FF1_RECV_PRESENT PG 29 → 3 /PRESENT
G1, G2 → GND
1 → 3.3V
10 → 3.3V
9 → 1.8V
2 → GND
<Implementation>

VCC_3V3 → L22 1.0 UH 1008 → 1
C708 22 UF 0603, C677 0.1 UF 0402, C642 22 UF 0603, C600 0.1 UF 0402
L20 1.0 UH 1008 → 10
C640 22 UF 0603, C598 0.1 UF 0402
VCC_1V8 → L21 1.0 UH 1008 → 9
C714 22 UF 0603, C678 0.1 UF 0402, C641 22 UF 0603, C599 0.1 UF 0402

POWER FILTERING CIRCUIT

U109-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17
B16 A16	GND_B16 GND_A16	1P 1N	B18 B17
B13 A13	GND_B13 GND_A13	2P 2N	A15 A14
B10 A10	GND_B10 GND_A10	3P 3N	B15 B14
B7 A7	GND_B7 GND_A7	4P 4N	A12 A11
B4 A4	GND_B4 GND_A4	5P 5N	B12 B11
B1 A1	GND_B1 GND_A1	6P 6N	A9 A8
		7P 7N	B9 B8
		8P 8N	A6 A5
		9P 9N	B6 B5
		10P 10N	A3 A2
		11P 11N	B3 B2

pK_FF1_RECV0 / nK_FF1_RECV0
pK_FF1_RECV1 / nK_FF1_RECV1
pK_FF1_RECV2 / nK_FF1_RECV2
pK_FF1_RECV3 / nK_FF1_RECV3
pK_FF1_RECV4 / nK_FF1_RECV4
pK_FF1_RECV5 / nK_FF1_RECV5
pK_FF1_RECV6 / nK_FF1_RECV6
pK_FF1_RECV7 / nK_FF1_RECV7
pK_FF1_RECV8 / nK_FF1_RECV8
pK_FF1_RECV9 / nK_FF1_RECV9
pK_FF1_RECV10 / nK_FF1_RECV10
pK_FF1_RECV11 / nK_FF1_RECV11

GND, 1 G1 2 G2, A95, A96, A97, A98, A99, A100

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.04: KU15P QUADS HIJ FIREFLY X12 #1

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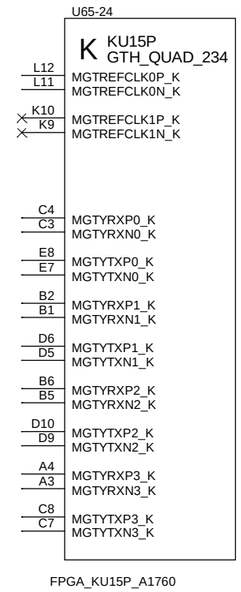
QUAD "K" IS UNUSED



FPGA_KU15P_A1760

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.05: KU15P QUAD K UNUSED

Size	Document Number	Rev
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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

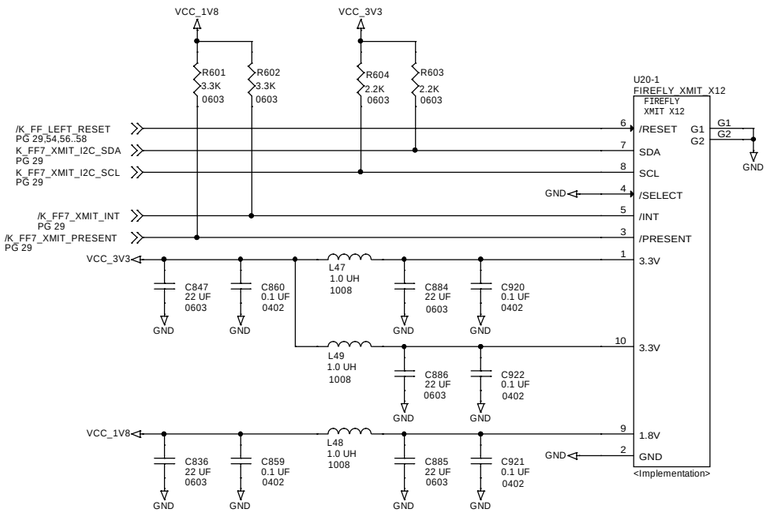
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

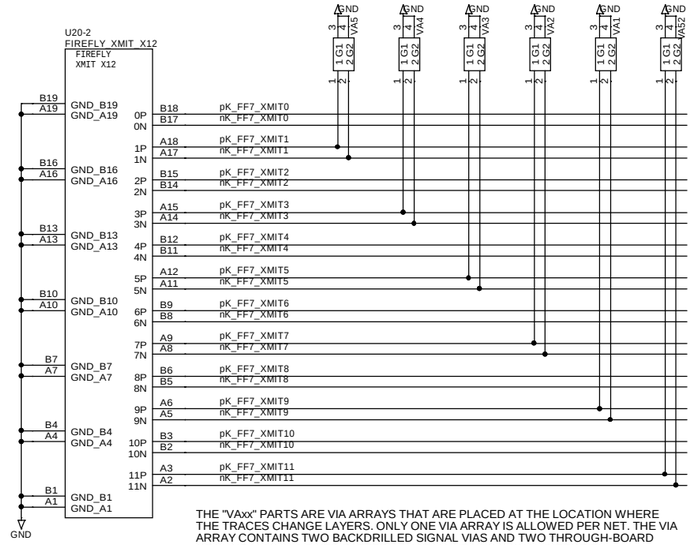
QUADS "L" AND "N" ARE CLOCKED FROM QUAD "M"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

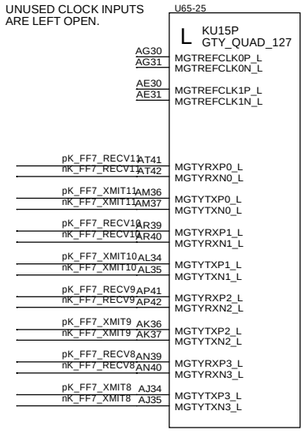
ac_pK_CLK0_CHAN4 PG 15
ac_nK_CLK0_CHAN4 PG 15
ac_pK_CLK1_CHAN4 PG 12
ac_nK_CLK1_CHAN4 PG 12

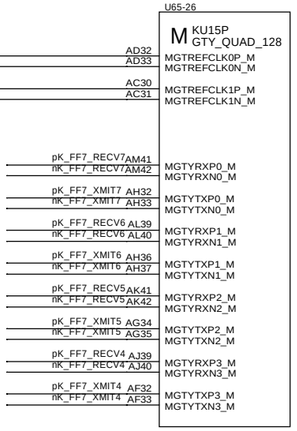


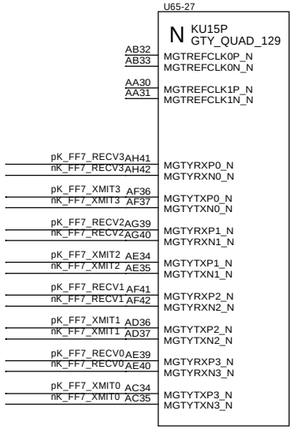
ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

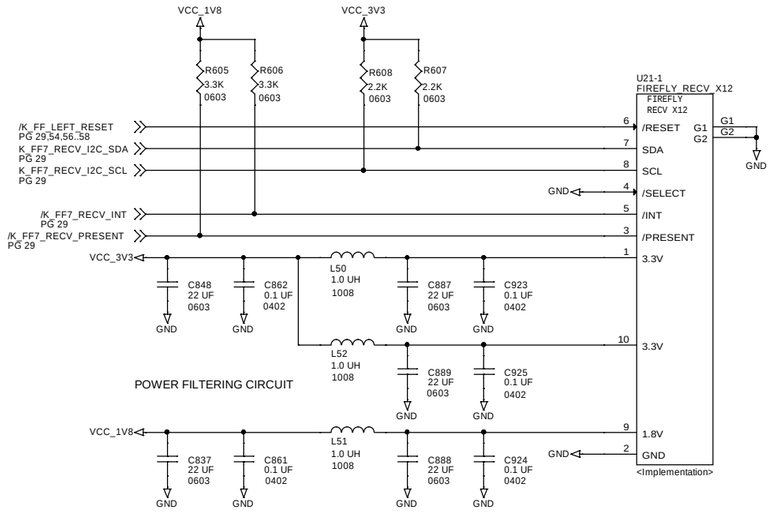


THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

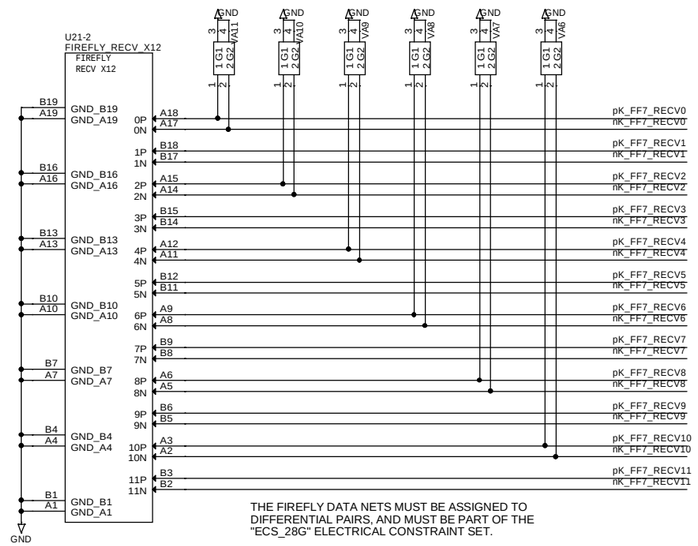








POWER FILTERING CIRCUIT



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.06: KU15P QUADS LMN FIREFLY X12 #7

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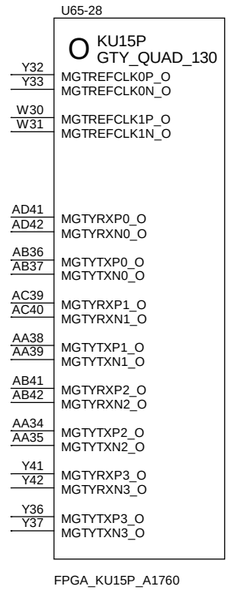
QUAD "O" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.07: KU15P QUAD O UNUSED

Size	Document Number	Rev
	6089-103	A

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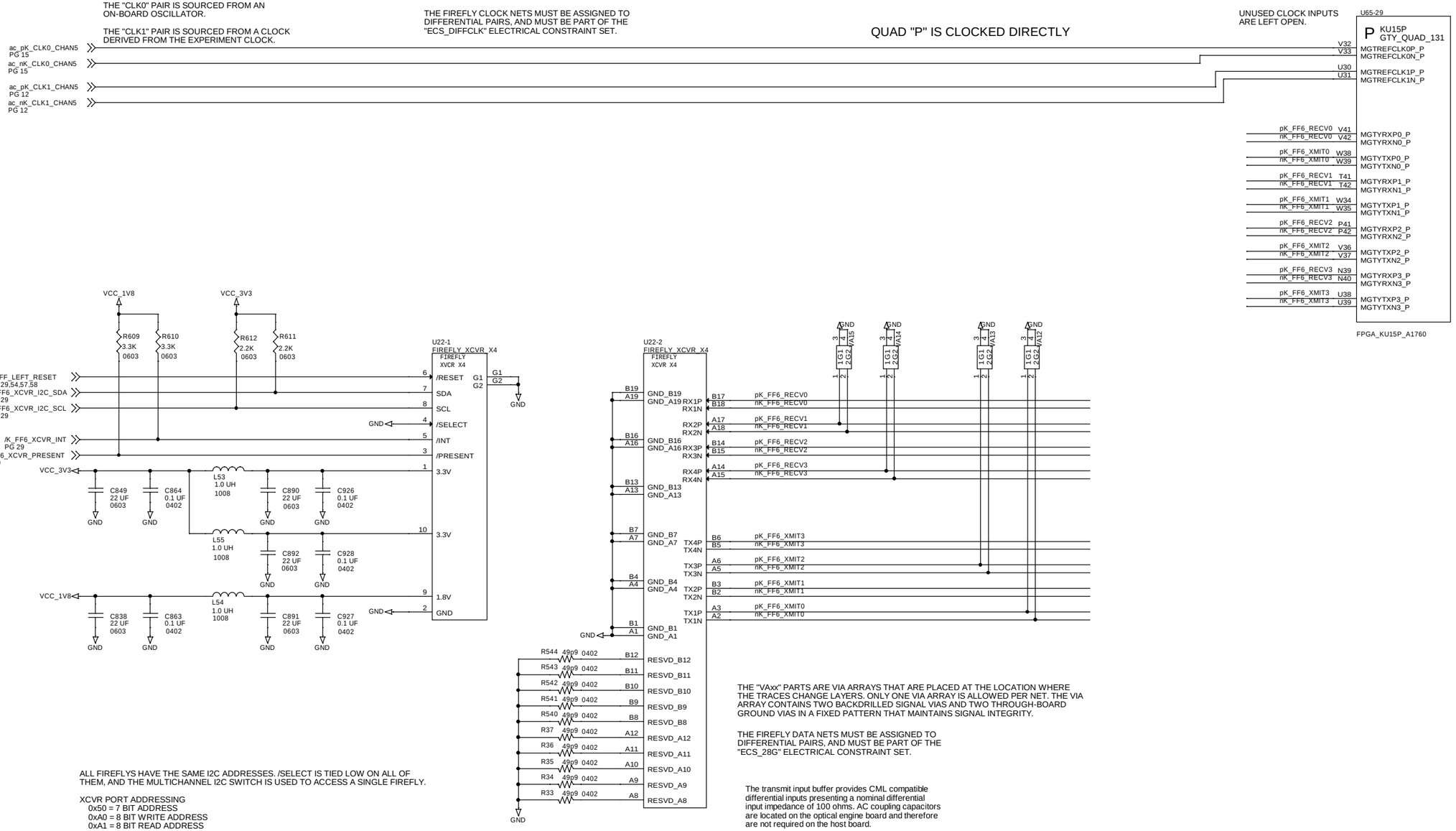
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.08: KU15P QUAD P FIREFLY X4 #6		
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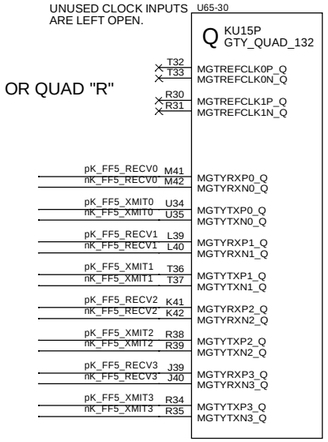
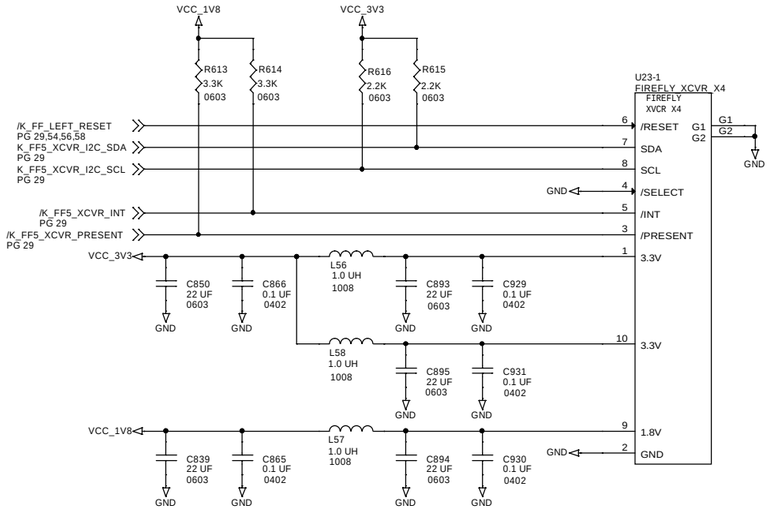
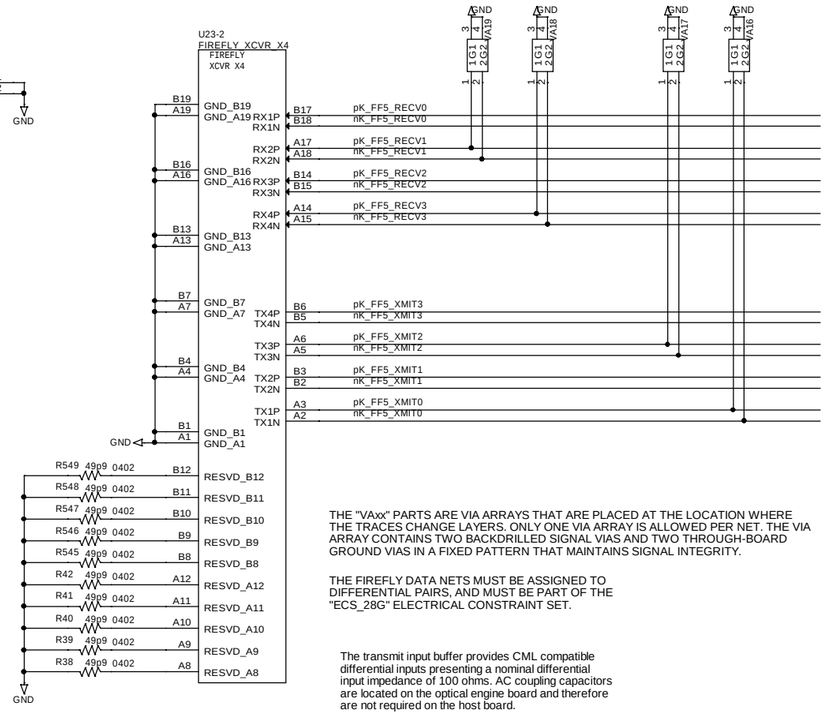
UNUSED CLOCK INPUTS ARE LEFT OPEN.

QUAD "Q" CAN BE CLOCKED FROM QUAD "P" OR QUAD "R"



FPGA_KU15P_A1760





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 7.09: KU15P QUAD R FIREFLY X4 #5			
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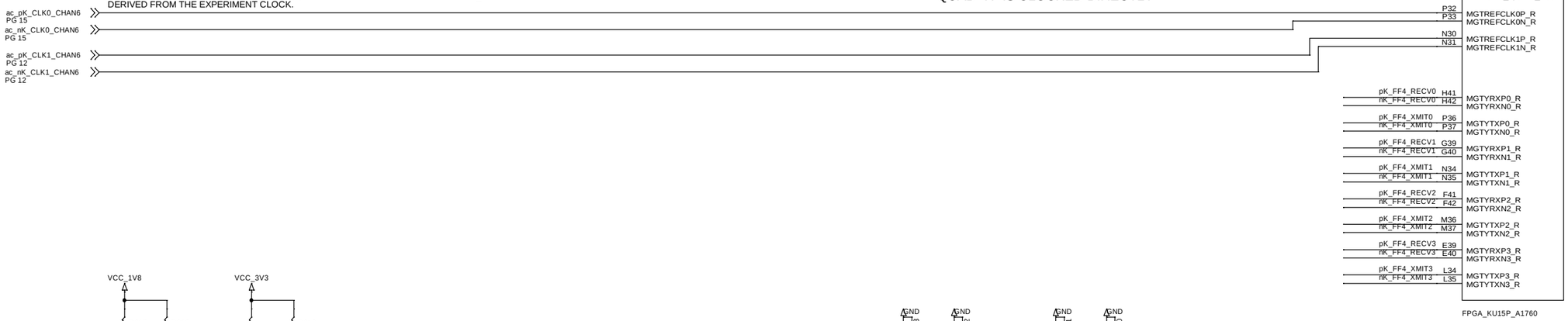
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

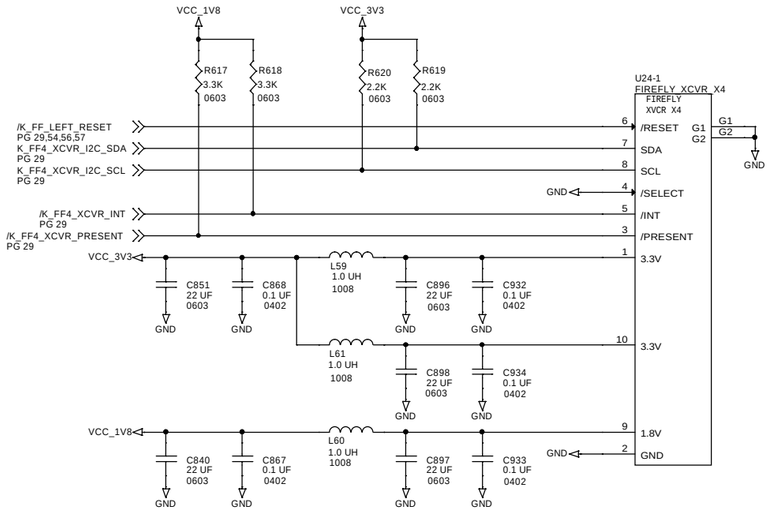
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

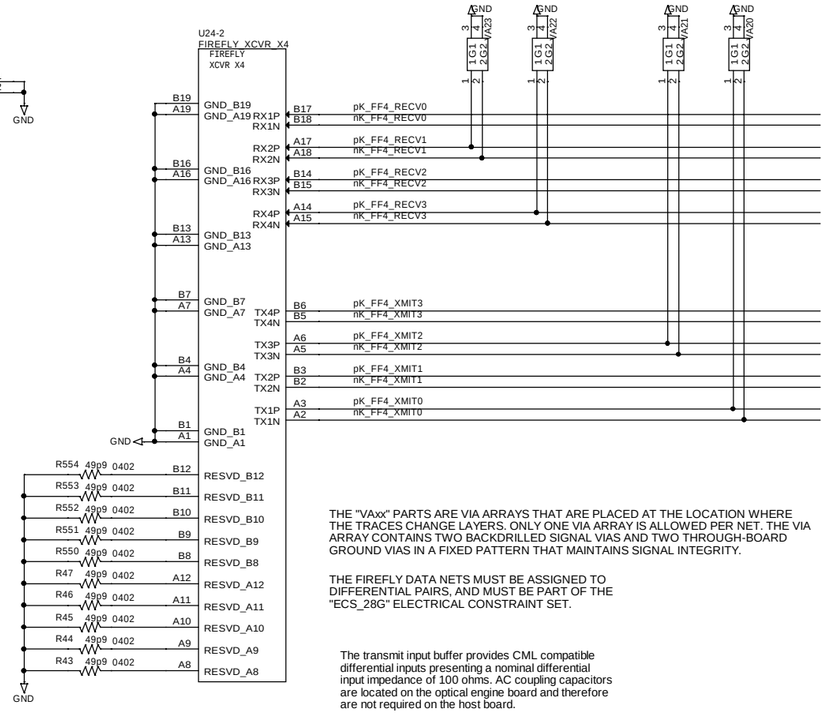
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "R" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.10: KU15P QUAD R FIREFLY X4 #4		
Size	Document Number: 6089-103	Rev: A
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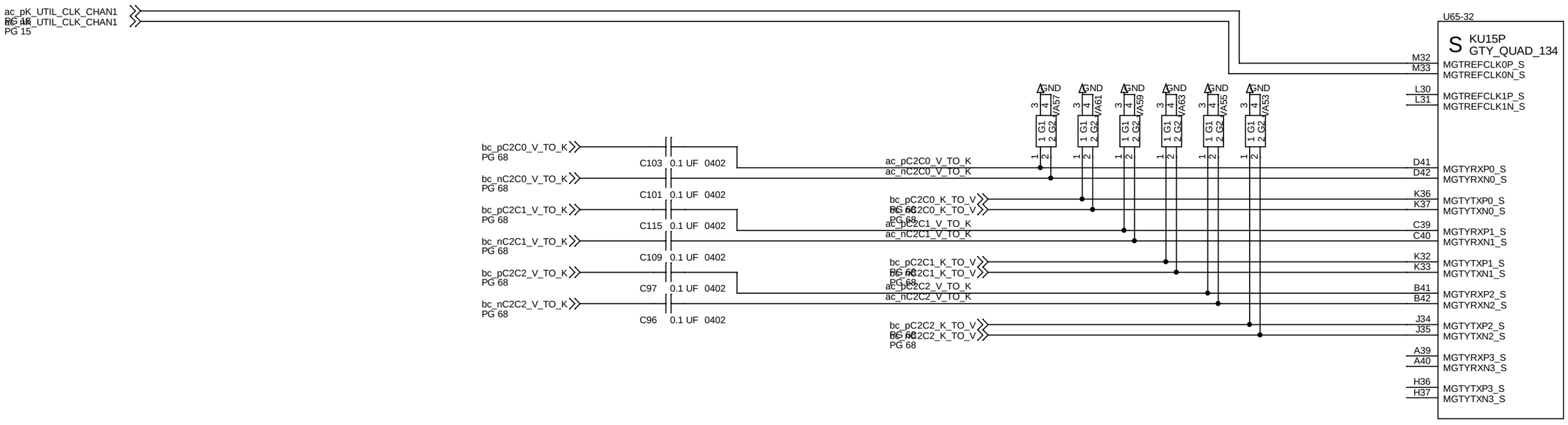
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "S" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

CONNECT UTILITY NETS HERE

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.11: KU15P QUAD S CHIP-TO-CHIP

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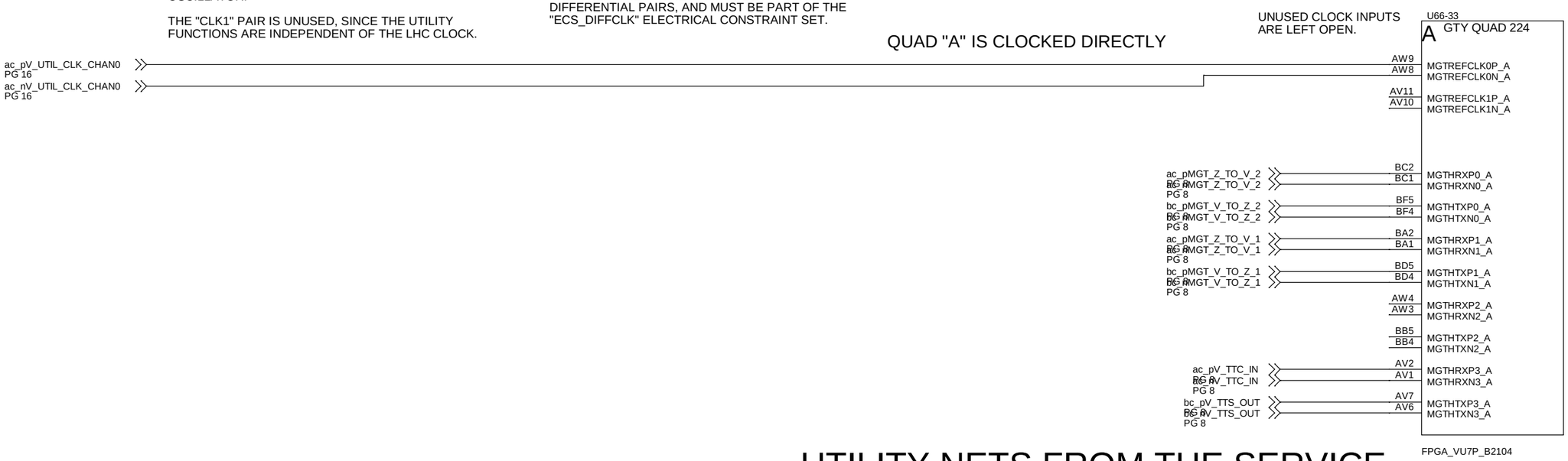
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.01: VU7P QUAD A UTILITY #1		
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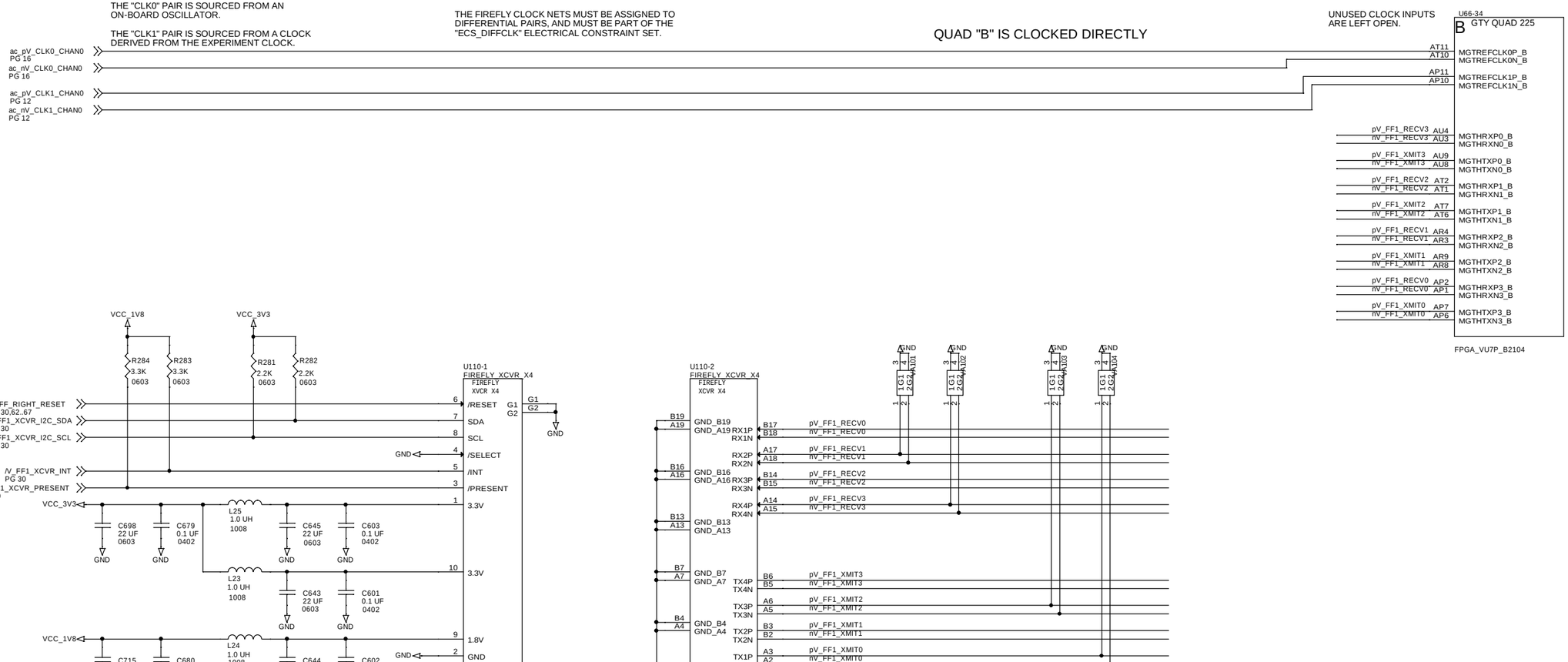
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "B" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.02: VU7P QUAD B FIREFLY X4 #1		
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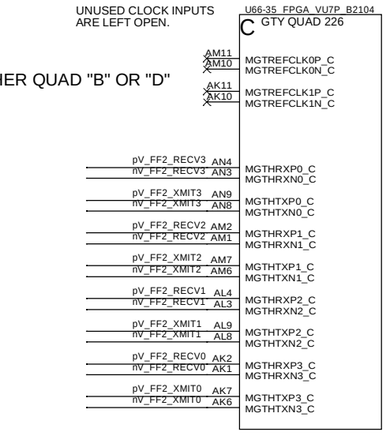
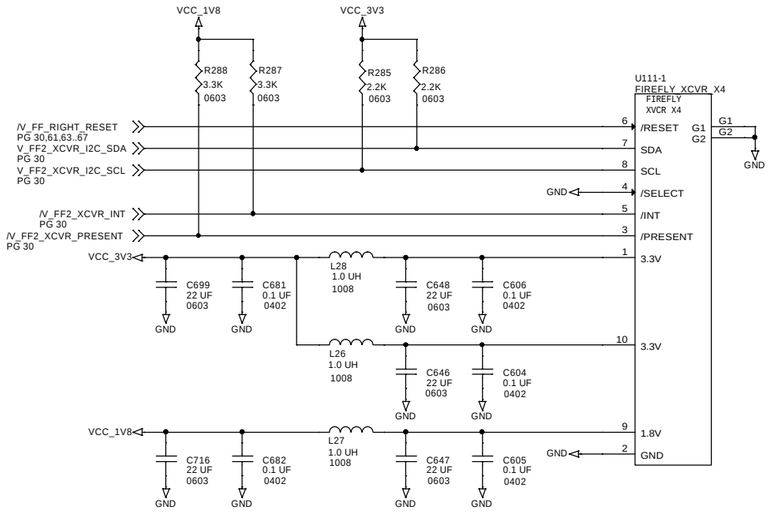
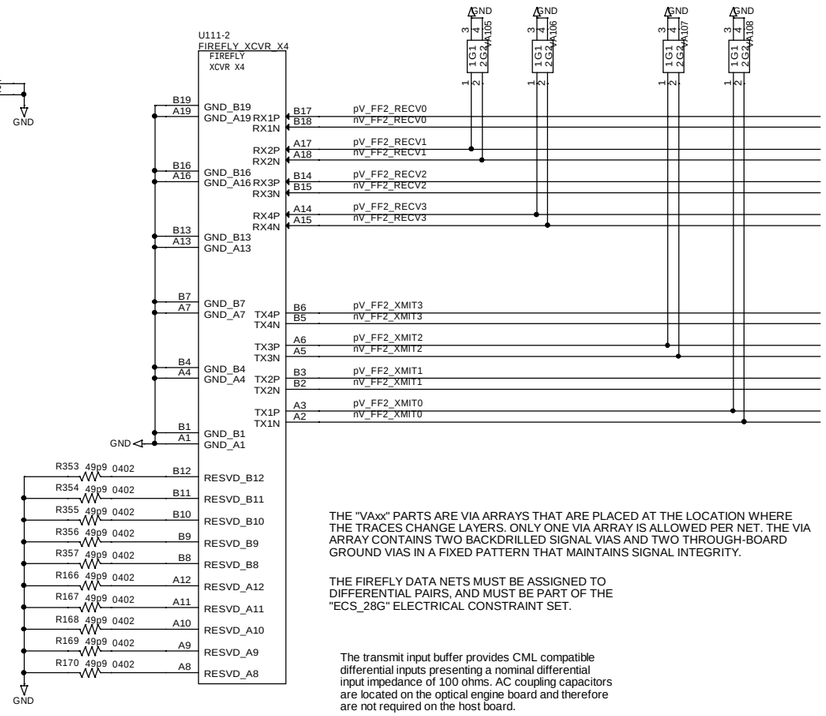
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "C" IS CLOCKED FROM EITHER QUAD "B" OR "D"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.03: VU7P QUAD C FIREFLY X4 #2		
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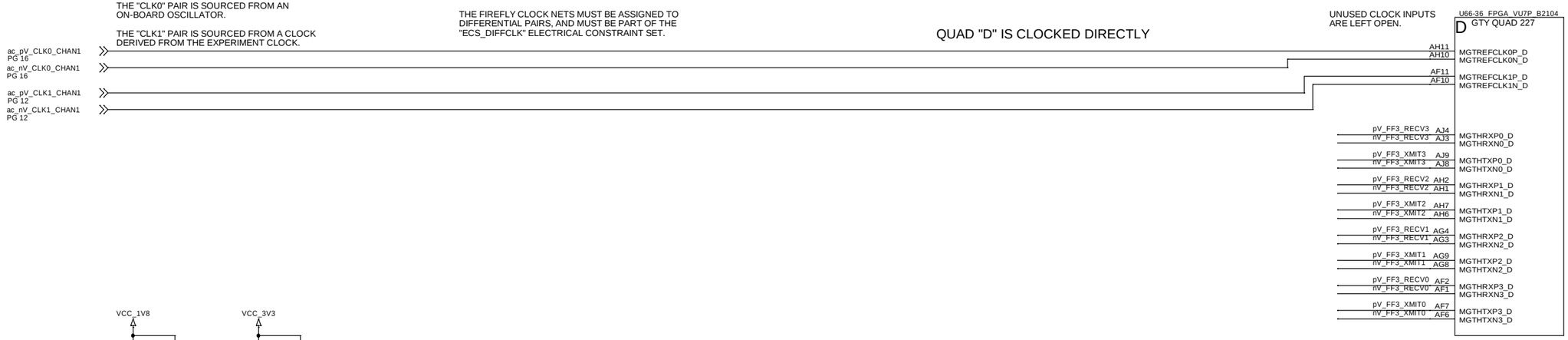
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

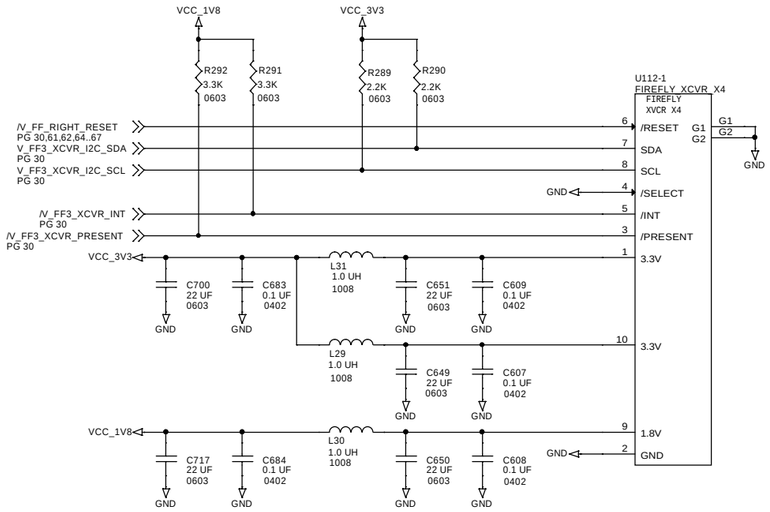
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

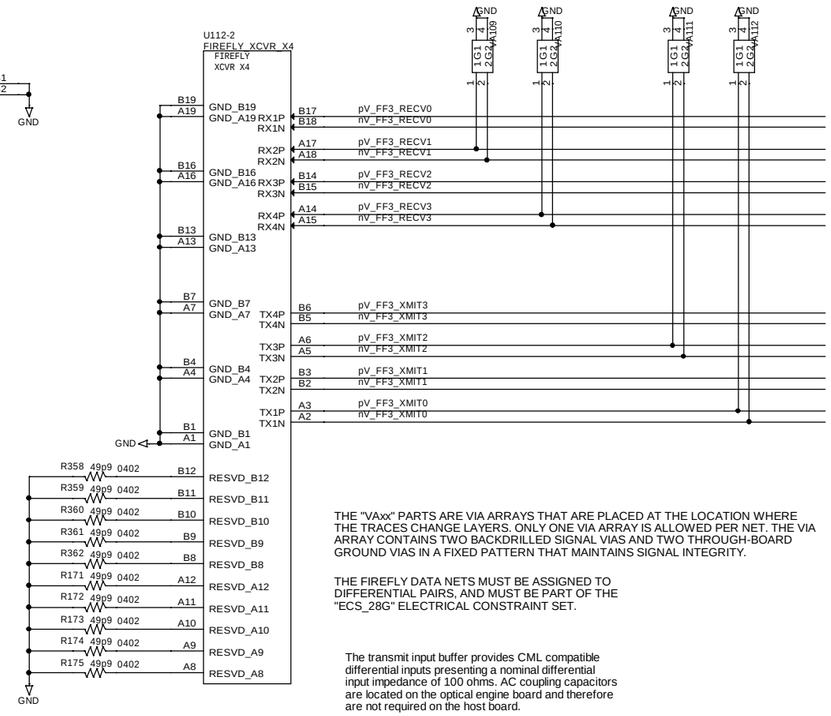
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "D" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.04: VU7P QUAD D FIREFLY X4 #3		
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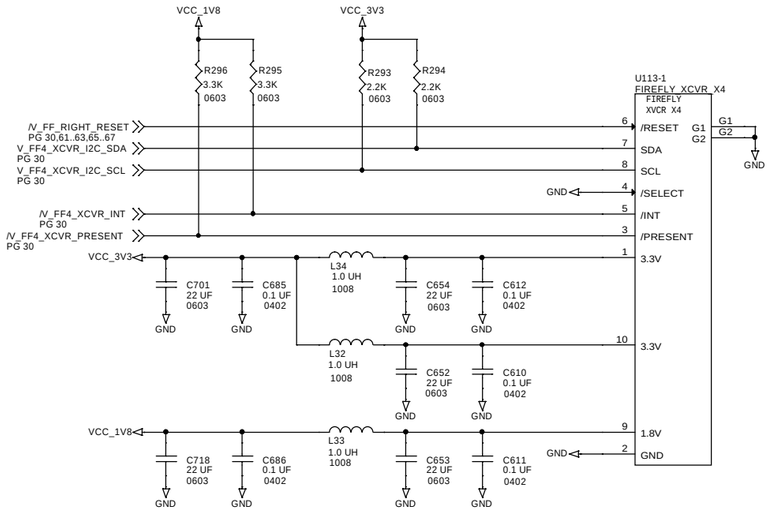
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

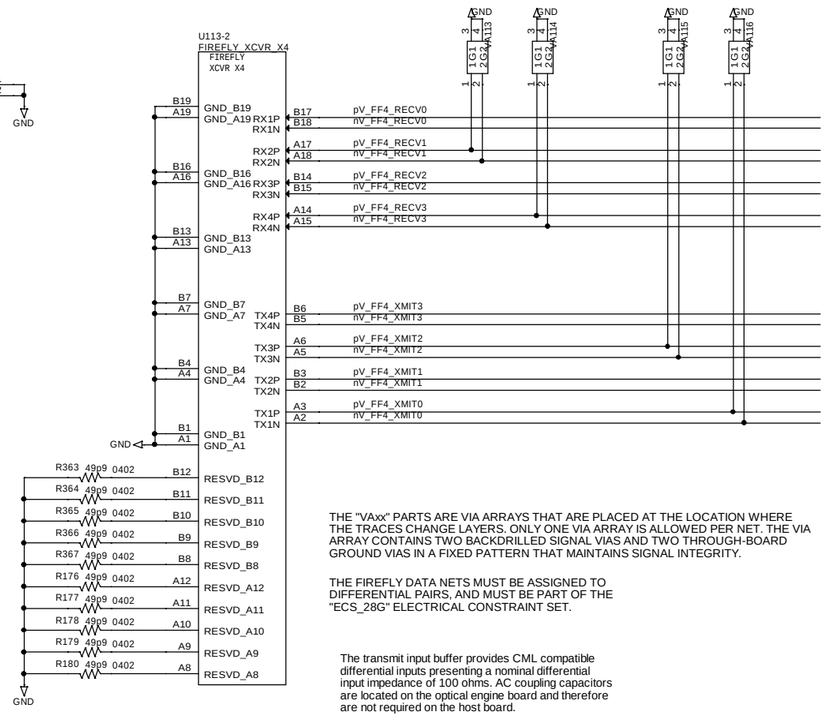
QUAD "E" IS CLOCKED FROM QUAD "D"

U66-37
GTY QUAD 228

AD11 FPGA_VU7P_B2104
AD10 MGTREFCLK0P_E
MGTREFCLK0N_E
AB11 MGTREFCLK1P_E
AB10 MGTREFCLK1N_E

pV_FF4_RECV3 AE4 MGTHRXP0_E
nV_FF4_RECV3 AE3 MGTHRXN0_E
pV_FF4_XMIT3 AE9 MGTHTXP0_E
nV_FF4_XMIT3 AE8 MGTHTXN0_E
pV_FF4_RECV2 AD2 MGTHRXP1_E
nV_FF4_RECV2 AD1 MGTHRXN1_E
pV_FF4_XMIT2 AD7 MGTHTXP1_E
nV_FF4_XMIT2 AD6 MGTHTXN1_E
pV_FF4_RECV1 AC4 MGTHRXP2_E
nV_FF4_RECV1 AC3 MGTHRXN2_E
pV_FF4_XMIT1 AC9 MGTHTXP2_E
nV_FF4_XMIT1 AC8 MGTHTXN2_E
pV_FF4_RECV0 AB2 MGTHRXP3_E
nV_FF4_RECV0 AB1 MGTHRXN3_E
pV_FF4_XMIT0 AB7 MGTHTXP3_E
nV_FF4_XMIT0 AB6 MGTHTXN3_E





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title: 8.05: VU7P QUAD E FIREFLY X4 #4
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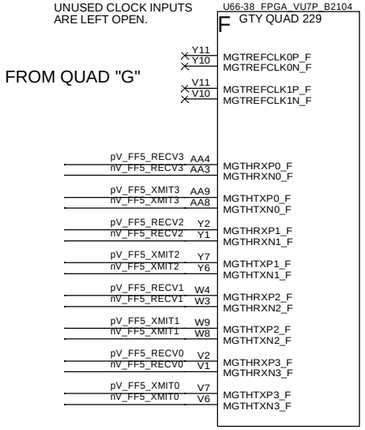
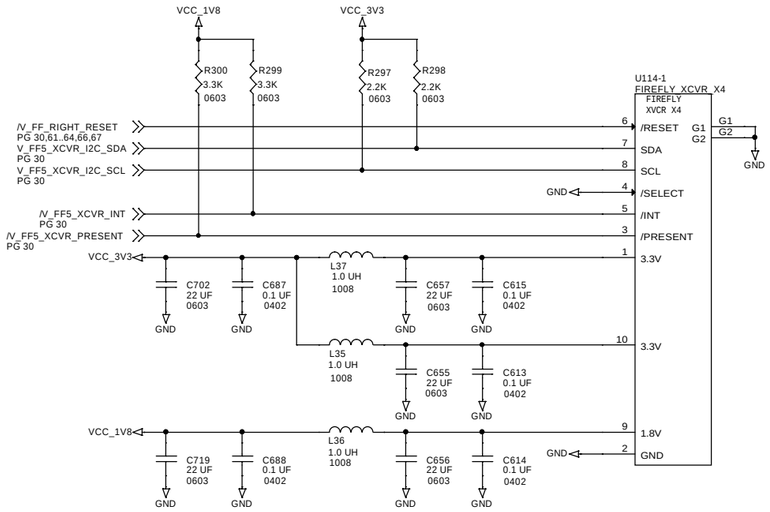
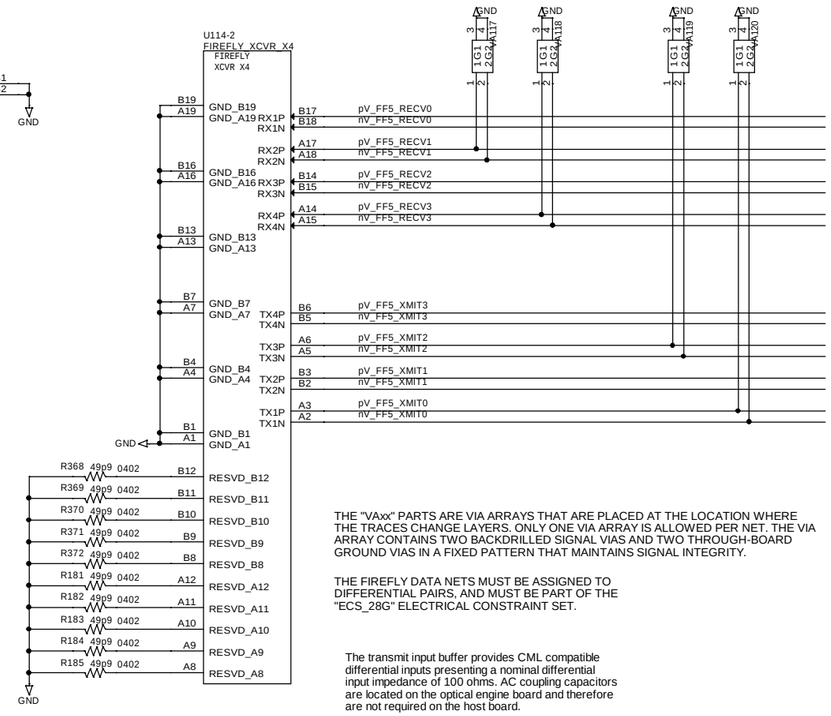
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "F" IS CLOCKED FROM QUAD "G"

U66-38_FPGA_VU7P_B2104
GTY QUAD 229







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.06: VU7P QUAD F FIREFLY X4 #5

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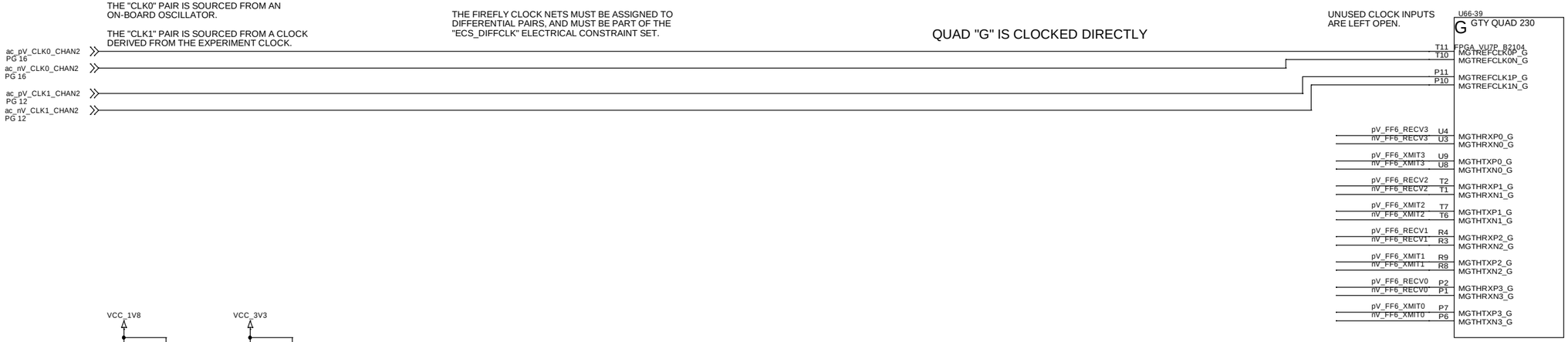
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

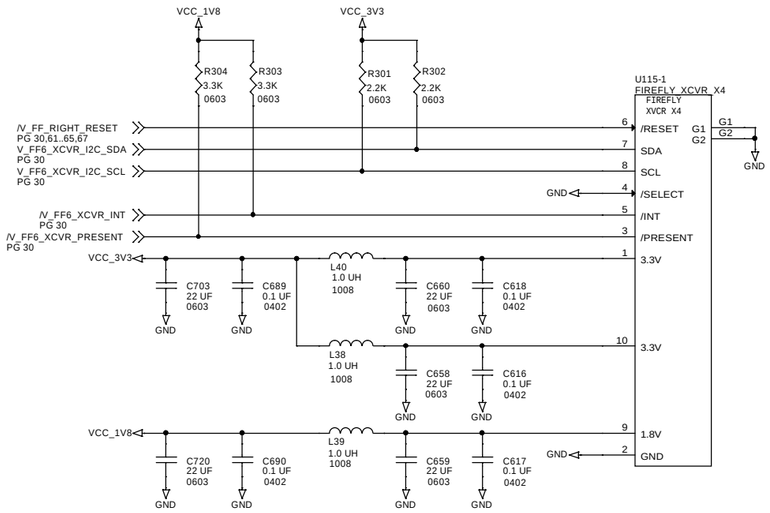
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

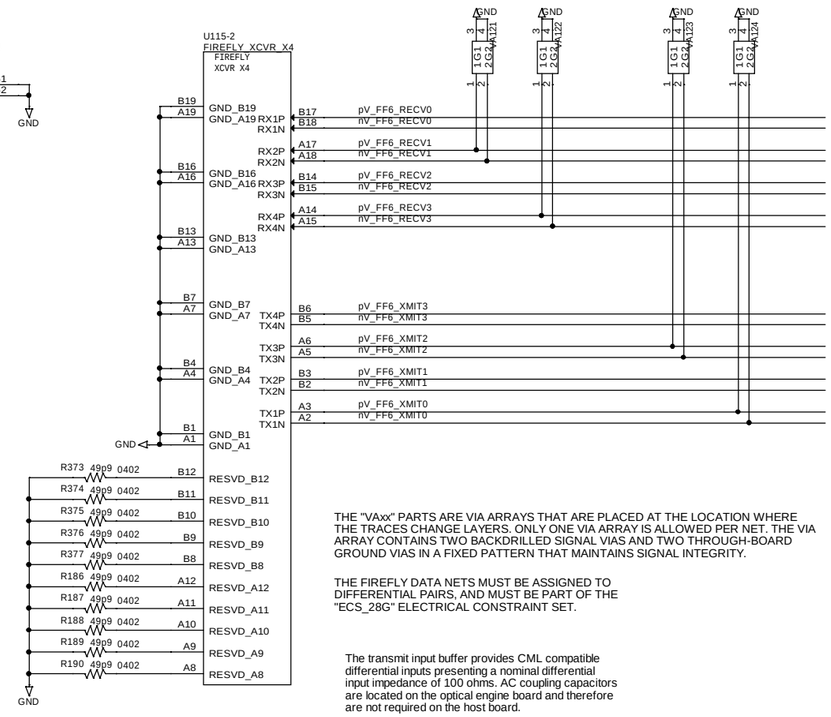
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "G" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.07: VU7P QUAD G FIREFLY X4 #6		
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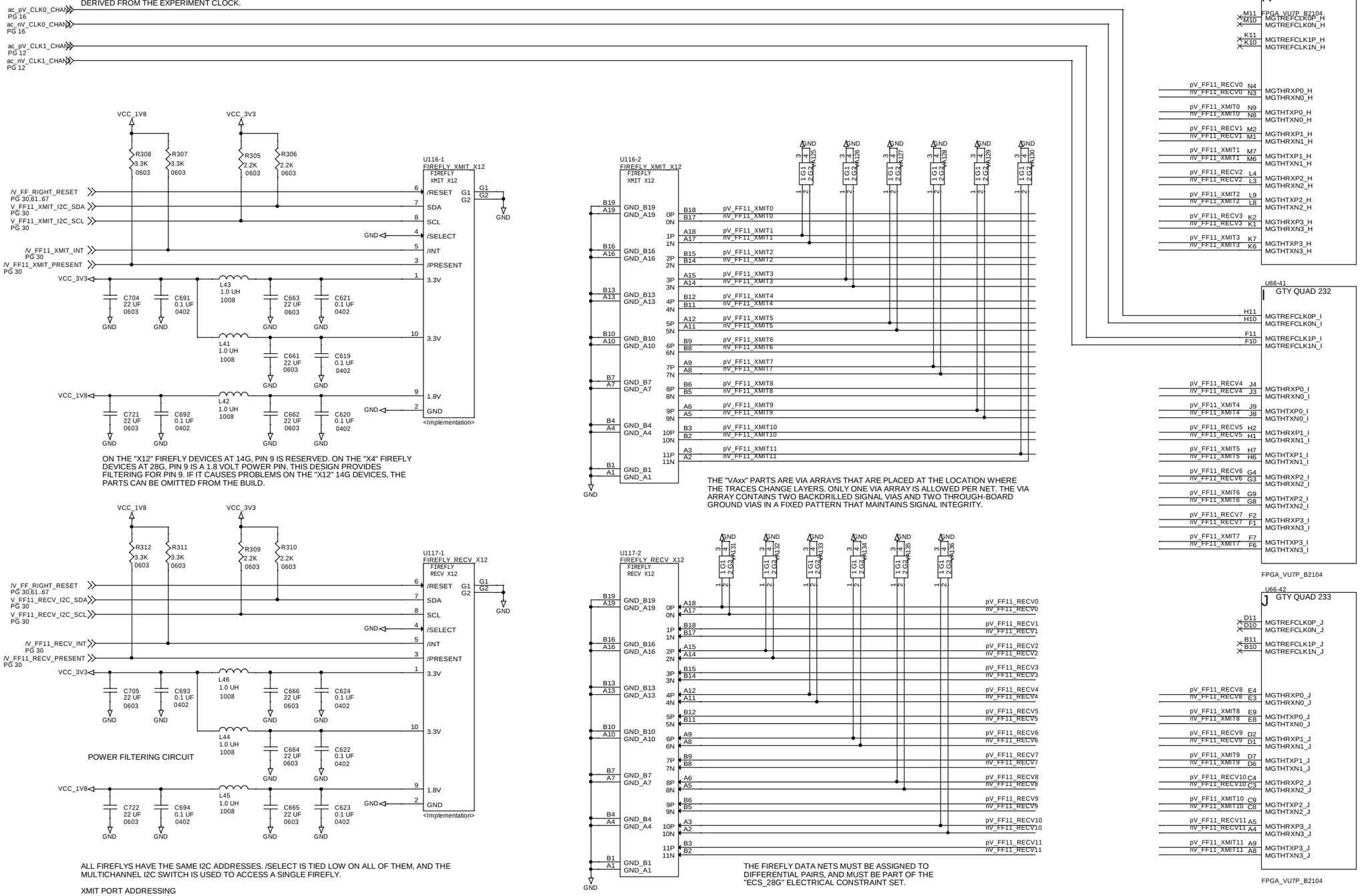
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

POWER FILTERING CIRCUIT

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 8.08: VU7P QUADS HIJ FIREFLY X12 #11			
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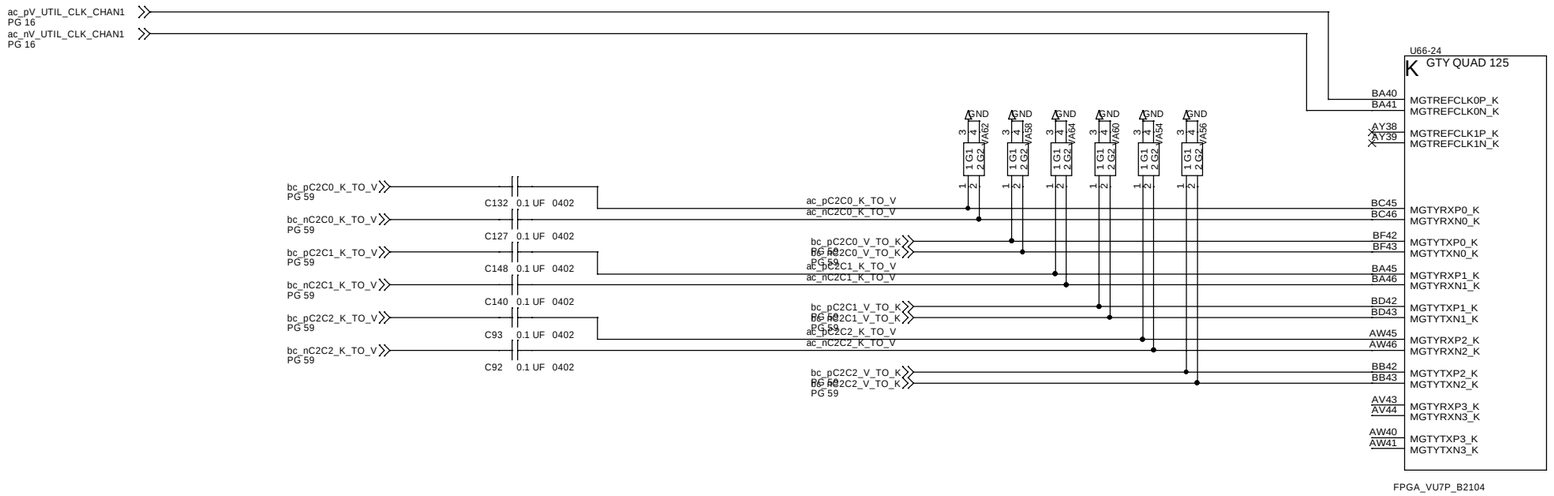
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

QUAD "K" IS CLOCKED DIRECTLY



THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.09: VU7P QUAD K CHIP TO CHIP

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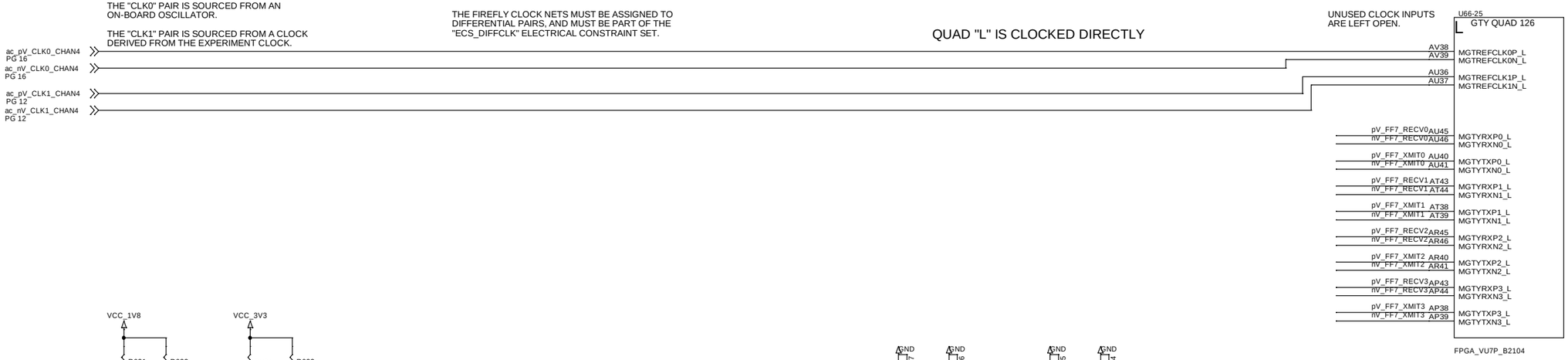
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

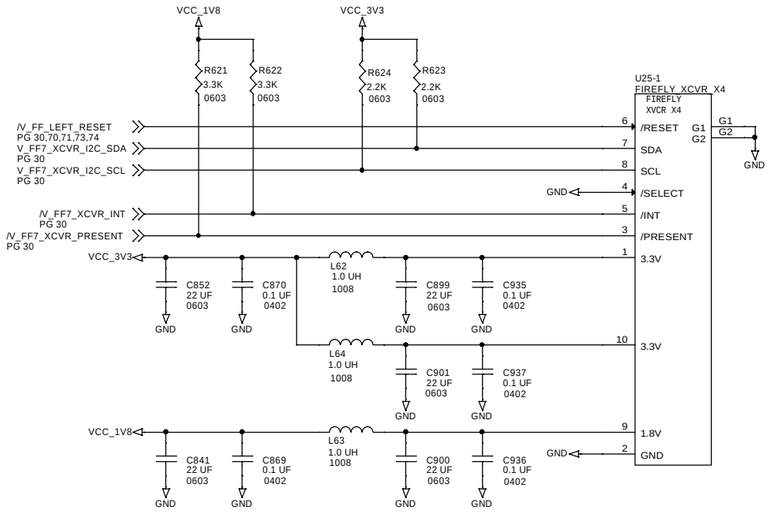
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

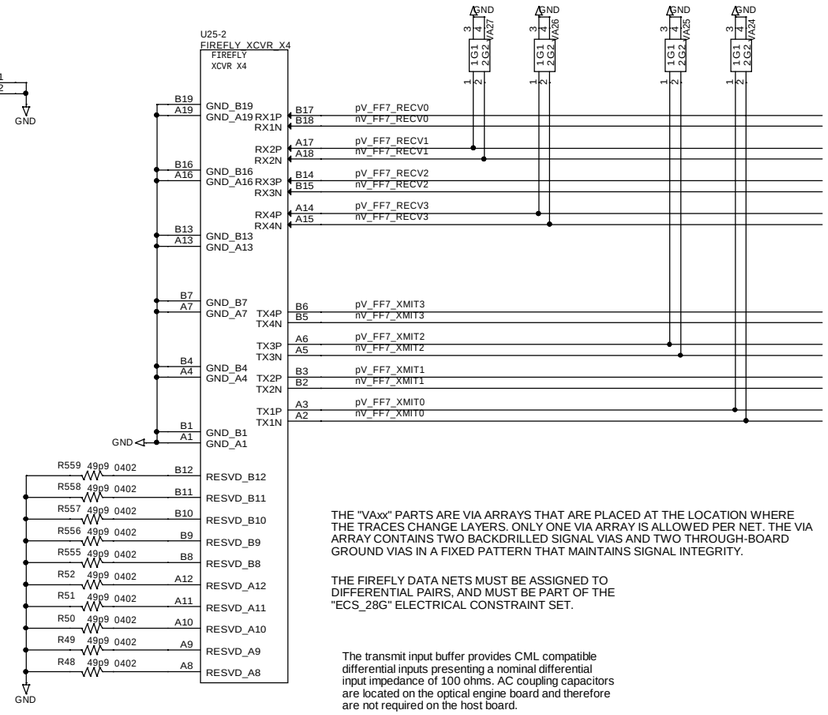
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "L" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.10: VU7P QUAD L FIREFLY X4 #7		
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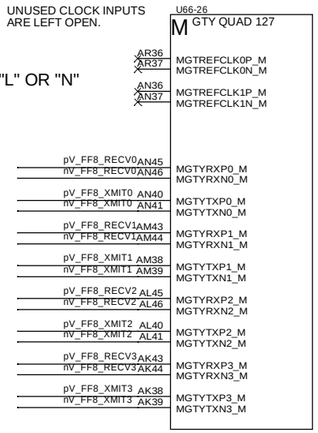
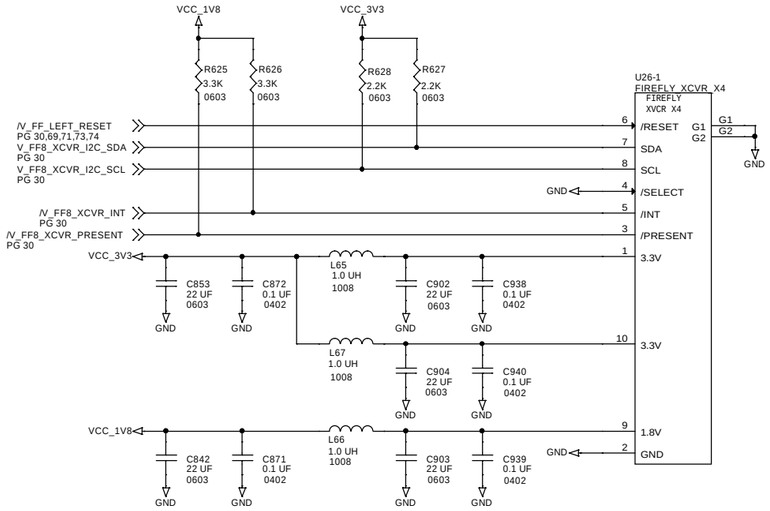
Date: Tuesday, February 26, 2019	Sheet 69 of 74	

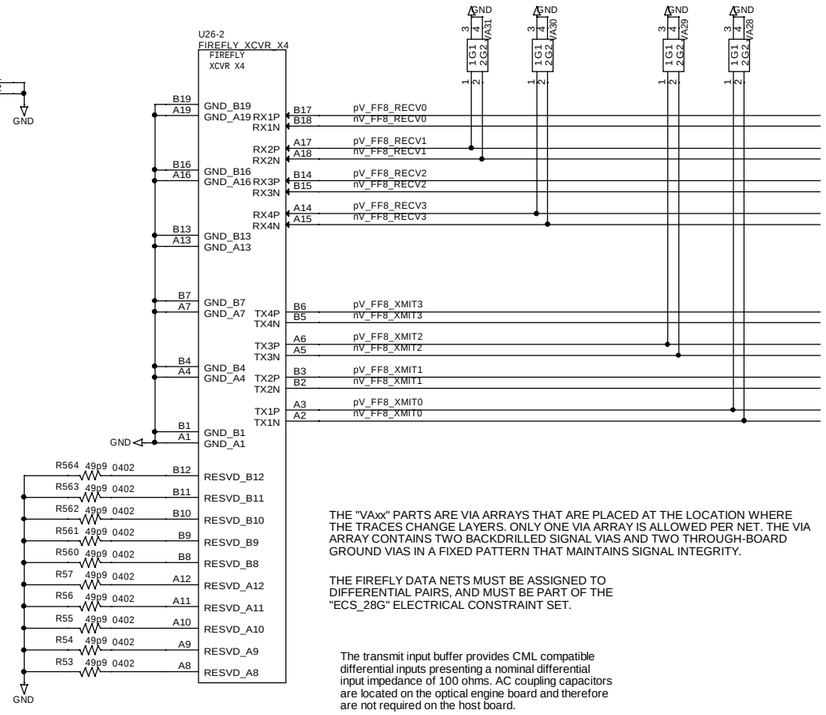
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "M" IS CLOCKED FROM EITHER QUAD "L" OR "N"



FPGA_VU7P_B2104





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.11: VU7P QUAD M FIREFLY X4 #8		
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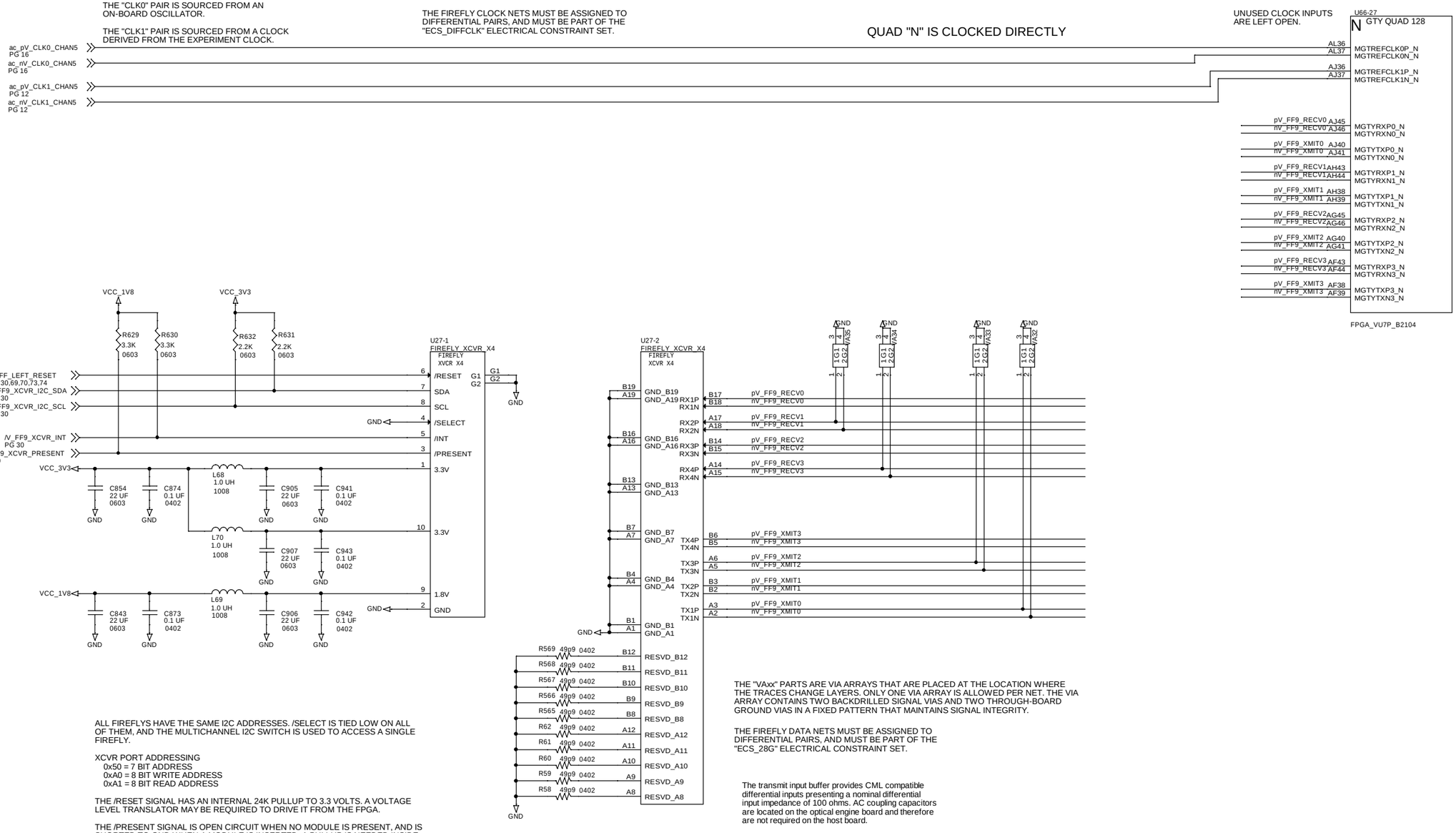
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "N" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

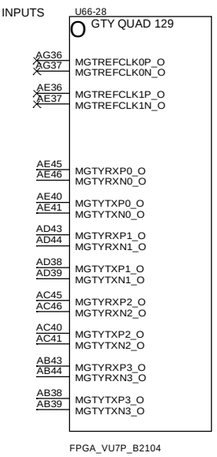
The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.12: VU7P QUAD N FIREFLY X4 #9		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 71 of 74	

UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "O" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.13: VU7P QUAD O UNUSED		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 72 of 74	

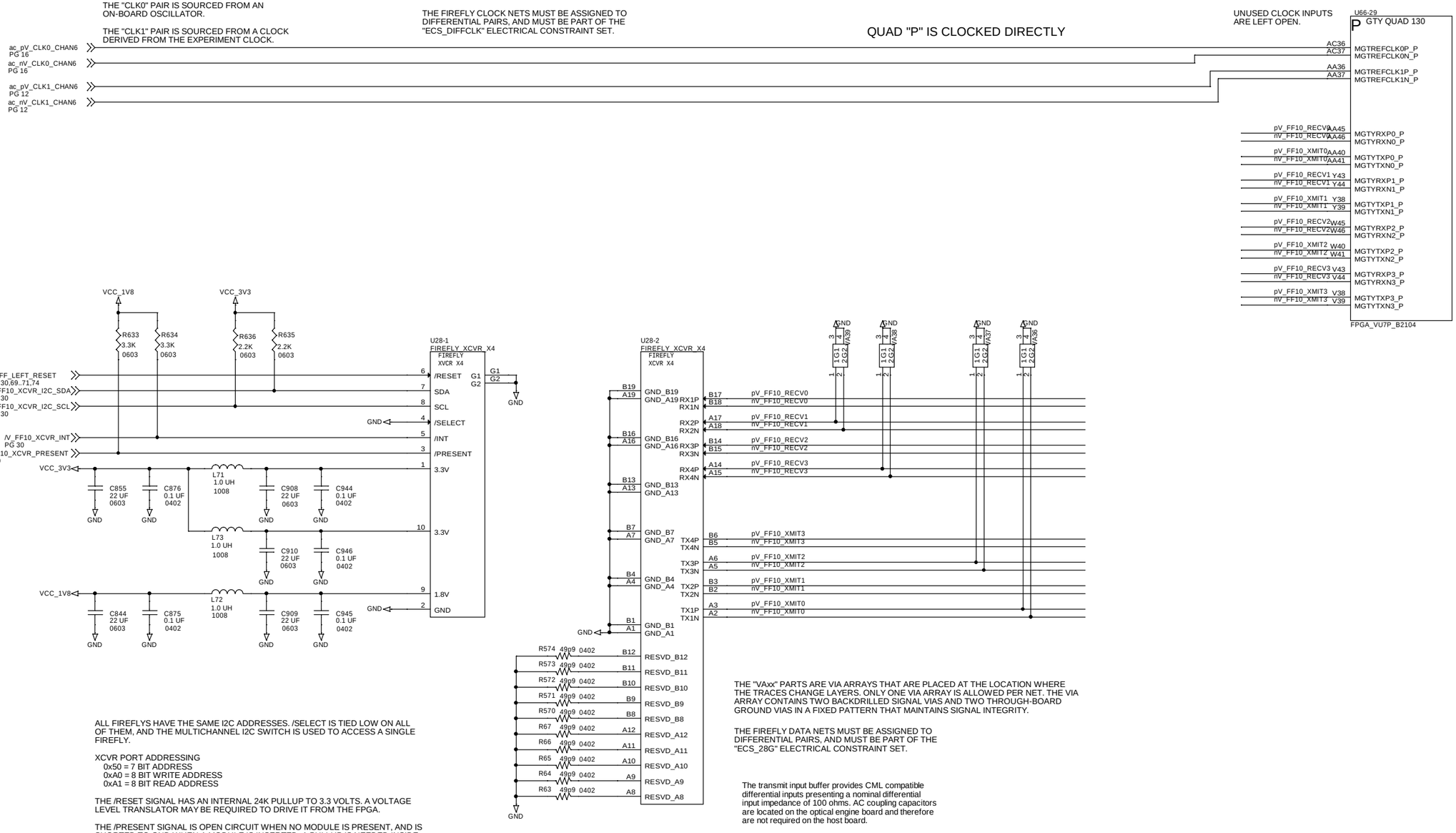
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.14: VU7P QUAD P FIREFLY X4 #10		
Size	Document Number: 6089-103	Rev: A
Date: Tuesday, February 26, 2019	Sheet 73 of 74	

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "Q" AND "S" ARE CLOCKED FROM QUAD "R"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pV_CLK0_CHAN7 PG 16
ac_nV_CLK0_CHAN7 PG 16
ac_pV_CLK1_CHAN7 PG 12
ac_nV_CLK1_CHAN7 PG 12

U66-30 GTY QUAD 131 (Q)
MGTREFCLK0P_Q / MGTREFCLK0N_Q (W36 / W37)
MGTREFCLK1P_Q / MGTREFCLK1N_Q (U36 / U37)
MGTYRXP0_Q / MGTYRXN0_Q (U45 / U46)
MGTYTXP0_Q / MGTYTXN0_Q (U40 / U41)
MGTYRXP1_Q / MGTYRXN1_Q (T43 / T44)
MGTYTXP1_Q / MGTYTXN1_Q (T38 / T39)
MGTYRXP2_Q / MGTYRXN2_Q (R45 / R46)
MGTYTXP2_Q / MGTYTXN2_Q (R40 / R41)
MGTYRXP3_Q / MGTYRXN3_Q (P43 / P44)
MGTYTXP3_Q / MGTYTXN3_Q (P38 / P39)

FPGA_VU7P_B2104

U66-31 GTY QUAD 132 (R)
MGTREFCLK0P_R / MGTREFCLK0N_R (R36 / R37)
MGTREFCLK1P_R / MGTREFCLK1N_R (N36 / N37)
MGTYRXP0_R / MGTYRXN0_R (N45 / N46)
MGTYTXP0_R / MGTYTXN0_R (N40 / N41)
MGTYRXP1_R / MGTYRXN1_R (M43 / M44)
MGTYTXP1_R / MGTYTXN1_R (M38 / M39)
MGTYRXP2_R / MGTYRXN2_R (L45 / L46)
MGTYTXP2_R / MGTYTXN2_R (L40 / L41)
MGTYRXP3_R / MGTYRXN3_R (K43 / K44)
MGTYTXP3_R / MGTYTXN3_R (J40 / J41)

FPGA_VU7P_B2104

U66-32 GTY QUAD 133 (S)
MGTREFCLK0P_133 / MGTREFCLK0N_133 (L36 / L37)
MGTREFCLK1P_133 / MGTREFCLK1N_133 (K38 / K39)
MGTYRXP0_133 / MGTYRXN0_133 (J45 / J46)
MGTYTXP0_133 / MGTYTXN0_133 (G40 / G41)
MGTYRXP1_133 / MGTYRXN1_133 (H43 / H44)
MGTYTXP1_133 / MGTYTXN1_133 (E42 / E43)
MGTYRXP2_133 / MGTYRXN2_133 (F45 / F46)
MGTYTXP2_133 / MGTYTXN2_133 (C42 / C43)
MGTYRXP3_133 / MGTYRXN3_133 (D45 / D46)
MGTYTXP3_133 / MGTYTXN3_133 (A42 / A43)

FPGA_VU7P_B2104

U29-1 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)
/V_FF_LEFT_RESET PG 30,69..71,73,74 → /RESET
V_FF12_XMIT_I2C_SDA PG 30 → SDA
V_FF12_XMIT_I2C_SCL PG 30 → SCL
GND → /SELECT
/V_FF12_XMIT_INT PG 30 → /INT
/V_FF12_XMIT_PRESENT PG 30 → /PRESENT
VCC_1V8: R637 3.3K 0603, R638 3.3K 0603
VCC_3V3: R640 2.2K 0603, R639 2.2K 0603
VCC_3V3 → 3.3V: L74 1.0 UH 1008; C856 22 UF 0603; C878 0.1 UF 0402; C911 22 UF 0603; C947 0.1 UF 0402
VCC_3V3 → 3.3V: L76 1.0 UH 1008; C913 22 UF 0603; C949 0.1 UF 0402
VCC_1V8 → 1.8V: L75 1.0 UH 1008; C845 22 UF 0603; C877 0.1 UF 0402; C912 22 UF 0603; C948 0.1 UF 0402
GND → GND
G1, G2 → GND
<Implementation>

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U29-2 FIREFLY_XMIT_X12 (FIREFLY XMIT X12)
GND_B19/A19, GND_B16/A16, GND_B13/A13, GND_B10/A10, GND_B7/A7, GND_B4/A4, GND_B1/A1
0P/0N: pV_FF12_XMIT0 / nV_FF12_XMIT0 (B18 / B17)
1P/1N: pV_FF12_XMIT1 / nV_FF12_XMIT1 (A18 / A17)
2P/2N: pV_FF12_XMIT2 / nV_FF12_XMIT2 (B15 / B14)
3P/3N: pV_FF12_XMIT3 / nV_FF12_XMIT3 (A15 / A14)
4P/4N: pV_FF12_XMIT4 / nV_FF12_XMIT4 (B12 / B11)
5P/5N: pV_FF12_XMIT5 / nV_FF12_XMIT5 (A12 / A11)
6P/6N: pV_FF12_XMIT6 / nV_FF12_XMIT6 (B9 / B8)
7P/7N: pV_FF12_XMIT7 / nV_FF12_XMIT7 (A9 / A8)
8P/8N: pV_FF12_XMIT8 / nV_FF12_XMIT8 (B6 / B5)
9P/9N: pV_FF12_XMIT9 / nV_FF12_XMIT9 (A6 / A5)
10P/10N: pV_FF12_XMIT10 / nV_FF12_XMIT10 (B3 / B2)
11P/11N: pV_FF12_XMIT11 / nV_FF12_XMIT11 (A3 / A2)
GND → 1 G1 2 G2 /A45, /A44, /A43, /A42, /A41, /A40

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U30-1 FIREFLY_RECV_X12 (FIREFLY RECV X12)
/V_FF_LEFT_RESET PG 30,69..71,73,74 → /RESET
V_FF12_RECV_I2C_SDA PG 30 → SDA
V_FF12_RECV_I2C_SCL PG 30 → SCL
GND → /SELECT
/V_FF12_RECV_INT PG 30 → /INT
/V_FF12_RECV_PRESENT PG 30 → /PRESENT
VCC_1V8: R641 3.3K 0603, R642 3.3K 0603
VCC_3V3: R644 2.2K 0603, R643 2.2K 0603
VCC_3V3 → 3.3V: L77 1.0 UH 1008; C857 22 UF 0603; C880 0.1 UF 0402; C914 22 UF 0603; C950 0.1 UF 0402
VCC_3V3 → 3.3V: L79 1.0 UH 1008; C916 22 UF 0603; C952 0.1 UF 0402
VCC_1V8 → 1.8V: L78 1.0 UH 1008; C846 22 UF 0603; C879 0.1 UF 0402; C915 22 UF 0603; C951 0.1 UF 0402
GND → GND
G1, G2 → GND
<implementation>

POWER FILTERING CIRCUIT

U30-2 FIREFLY_RECV_X12 (FIREFLY RECV X12)
GND_B19/A19, GND_B16/A16, GND_B13/A13, GND_B10/A10, GND_B7/A7, GND_B4/A4, GND_B1/A1
0P/0N: pV_FF12_RECV0 / nV_FF12_RECV0 (A18 / A17)
1P/1N: pV_FF12_RECV1 / nV_FF12_RECV1 (B18 / B17)
2P/2N: pV_FF12_RECV2 / nV_FF12_RECV2 (A15 / A14)
3P/3N: pV_FF12_RECV3 / nV_FF12_RECV3 (B15 / B14)
4P/4N: pV_FF12_RECV4 / nV_FF12_RECV4 (A12 / A11)
5P/5N: pV_FF12_RECV5 / nV_FF12_RECV5 (B12 / B11)
6P/6N: pV_FF12_RECV6 / nV_FF12_RECV6 (A9 / A8)
7P/7N: pV_FF12_RECV7 / nV_FF12_RECV7 (B9 / B8)
8P/8N: pV_FF12_RECV8 / nV_FF12_RECV8 (A6 / A5)
9P/9N: pV_FF12_RECV9 / nV_FF12_RECV9 (B6 / B5)
10P/10N: pV_FF12_RECV10 / nV_FF12_RECV10 (A3 / A2)
11P/11N: pV_FF12_RECV11 / nV_FF12_RECV11 (B3 / B2)
GND → 1 G1 2 G2 /A51, /A50, /A49, /A48, /A47, /A46

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.15: VU7P QUADS QRS FIREFLY X12 #12		
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Date: Tuesday, February 26, 2019	Sheet 74 of 74	