Cornell Laboratory for
Accelerator-based Sciences and Education (CLASSE)

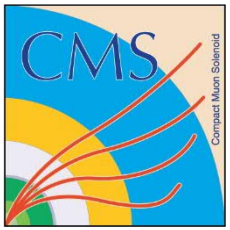
OT-DTC, TF, & IT-DTC Hardware Update and Status

Apollo (Service and Command)
Crystal
Serenity

Charlie Strohman

crs5@cornell.edu

DPS Meeting
March 7, 2019

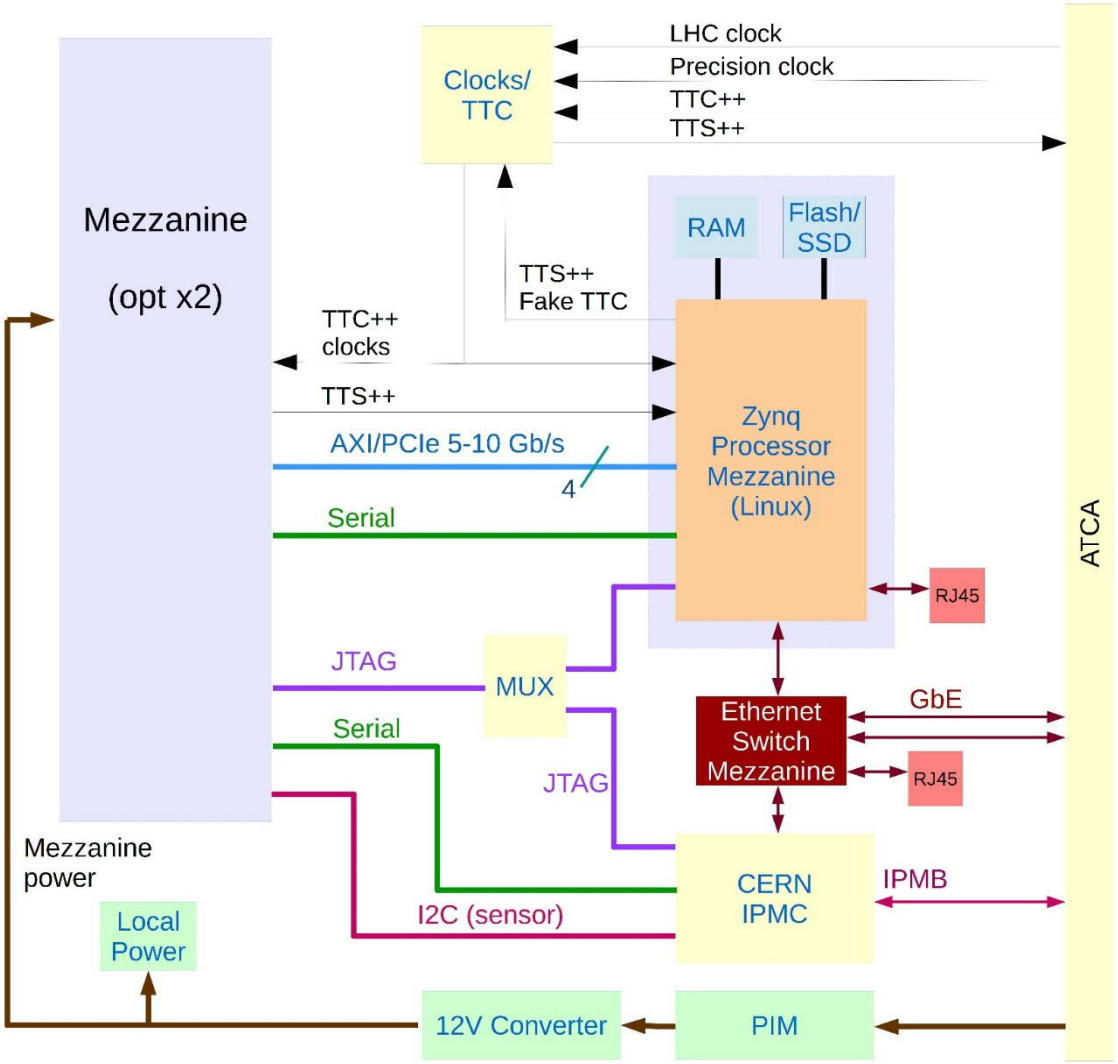


Introduction

- Hardware Update
  - Apollo
    - Service Module (Boston University)
    - Command Module FPGA board (Cornell University)
  - Serenity (Imperial College London)
  - Crystal (Imperial College London)

- Schedule
  - Board Availability
  - Integration Testing

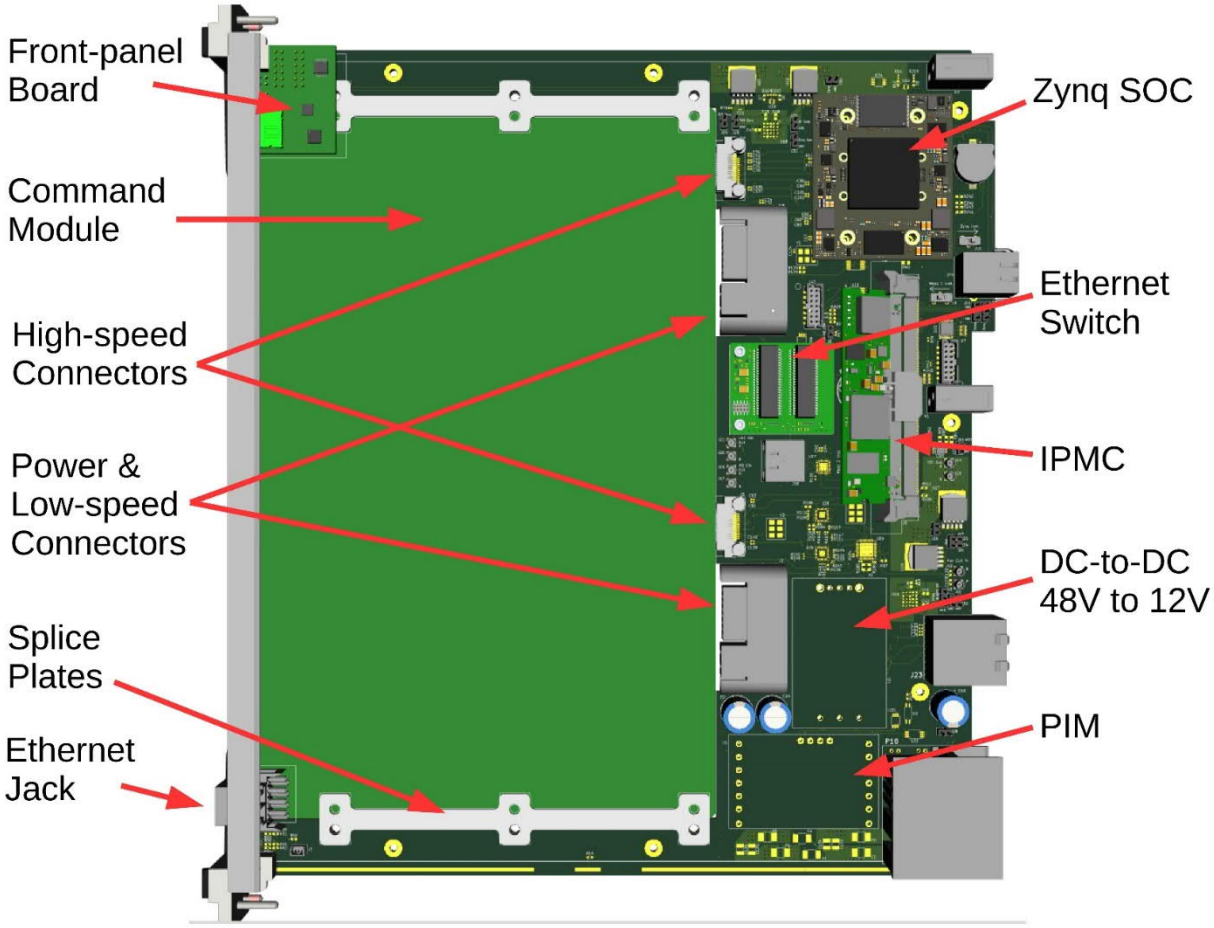
Apollo Service Module



Block Diagram

From Dan Gastler @ BU

Apollo Service Module



Assembled Model

From Dan Gastler @ BU

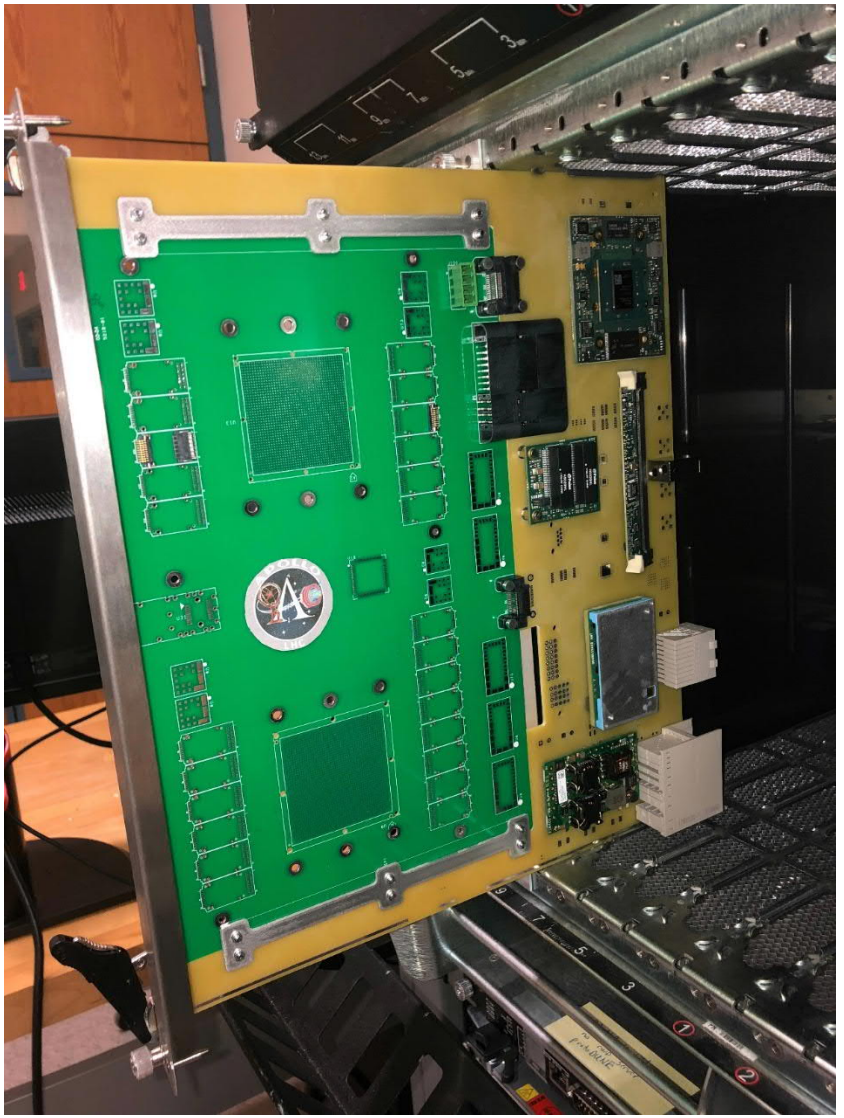
Apollo Service Module

Mechanical Prototypes

- Verify that BU and CU agree on mechanics
- Side 1 of the two boards are co-planar
- Service module can support one large or one/two small command modules

Advantages of independent cards

- Different PCB material
  - Lower speeds on blade (10G max vs. 25G)
- Different PCB processes
  - Could have conventional vs. HDI sequential laminations
  - Different number of layers
  - Different thicknesses
  - Backdrilling
- Minimize cost and risk when changing technology
- Support multiple applications
  - IT-DTC
  - TF
  - ATLAS Level 0 MDT trigger processor



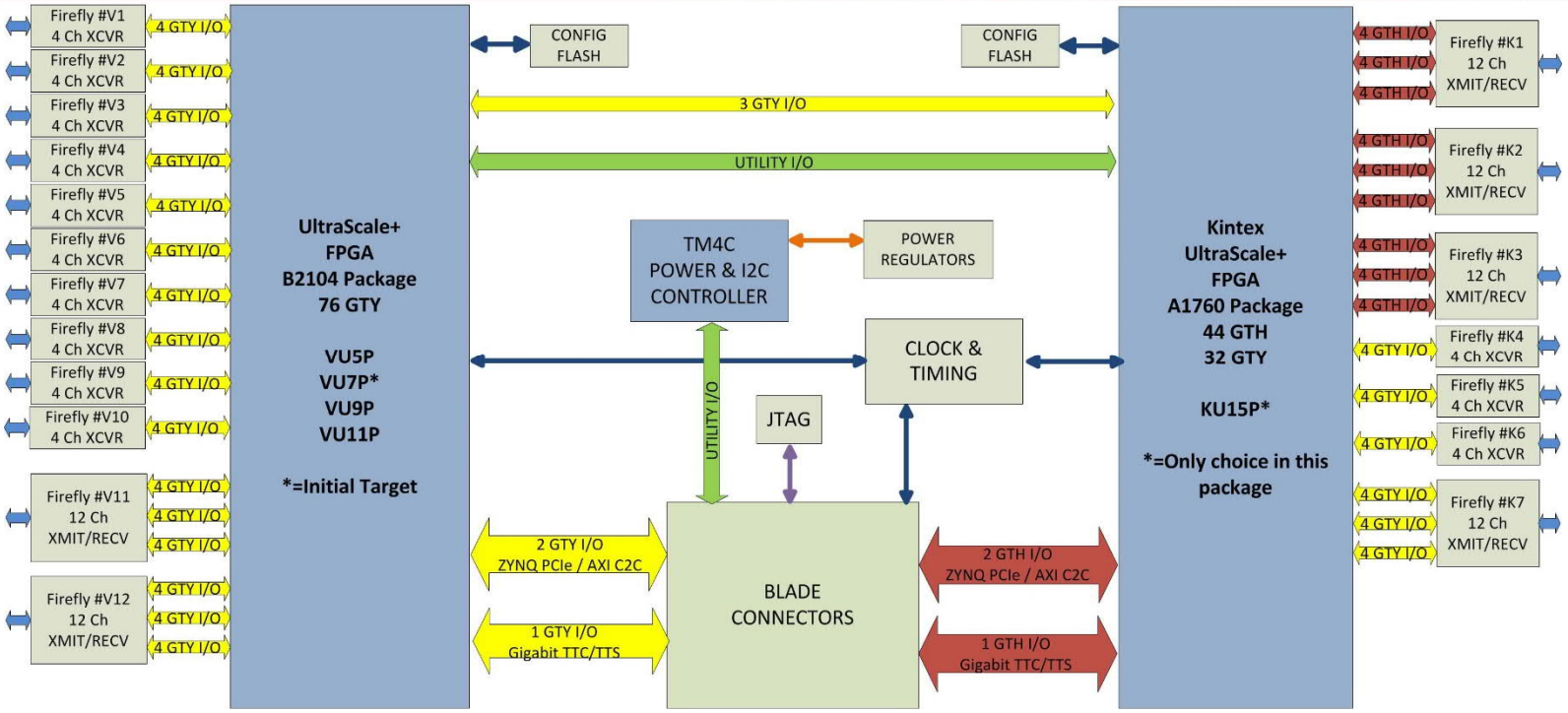
From Dan Gastler @ BU

Apollo Service Module

Status (from Eric Hazen)

- PCBs not yet ordered, final checking underway
- Expect bare PCBs and parts kits by ~ 1 April
- Expect assembled PCBs by ~15 April

Apollo VU7P/KU15P Module



- VU7P (GTY up to 25G with -1 speed grade)
  - 64 GTY Firefly to front panel
    - 10 4-Chan XCVR
    - 2 12-chan XMIT/RECV (25G parts not available yet)
  - 2 GTY to service blade (PCIe or AXI C2C)
  - 3 GTY to KU15P
  - 1 GTY to service blade (TTC/TTS)
    - Other
      - Controller for power sequence and I2C concentration
      - Reference Clock and timing distribution
      - JTAG to both FPGAs and controller

- KU15P (GTH up to 16G, GTY up to 28G with -2 speed grade)
  - 36 GTH Firefly to front panel
    - 3 12-Chan XMIT/RECV
  - 24 GTY Firefly to front panel
    - 3 4-Chan XCVR
    - 1 12-chan XMIT/RECV
  - 2 GTH to service blade (PCIe or AXI C2C)
  - 3 GTY to VU7P
  - 1 GTH to service blade (TTC/TTS)

Block Diagram

From Charlie Strohman @ CU

Apollo VU7P/KU15P Module

Status (from Charlie Strohman)

- Boards currently out for fabrication
  - Scheduled to be shipped to Cornell 3/18
  - FYI: 12 boards, 16 layers, Megtron-6, 180 mm X 278 mm x 1.8 mm, 9590 vias (1076 are backdrilled) -> $1246 each plus $1700 NRE (also $766 each for quantity 300)
- Finishing up BOM for assembly quotes for 10 boards
  - Hoping to start assembly before 3/22
- Ordered:
  - 7 KU15P
    - Also borrowing 2
  - 5 VU7P
    - already have 2 on hand
  - 75 FireFly 4-chan XCVR @ 25G
  - 12 FireFly 12-chan XMIT/RECV @ 14G
    - Already have 9 on hand, but too short to reach front panel from back of board
  - Listening for availability of 12-chan XMIT/RECV @ 25G
- Charlie on vacation 3/22 through 4/5
  - Hiking in Big Bend National Park in Texas

A Minimal Ethernet and Timing Hub

Part of the Serenity Family

From Andy Rose

18 Feb 2019 https://indico.cern.ch/event/799840/

Slide originally shown by Andy Rose on 18 Feb 2019 https://indico.cern.ch/event/799840/

A **Minimal** Ethernet & Timing Hub

- Ethernet distribution
- TTC distribution
- A few experimental features

- Stackup - Keep it simple, 12-layer FR4

- Should be operable within standby power limit
  - No need for IPMC, unless you want it ☺

Charlie's added comment:
The DTH is not available soon enough for testing the OT_DTC and TF systems. The Crystal board provides basic utilities. In the spirt of testing new ideas, it also provides an opportunity to try a few.

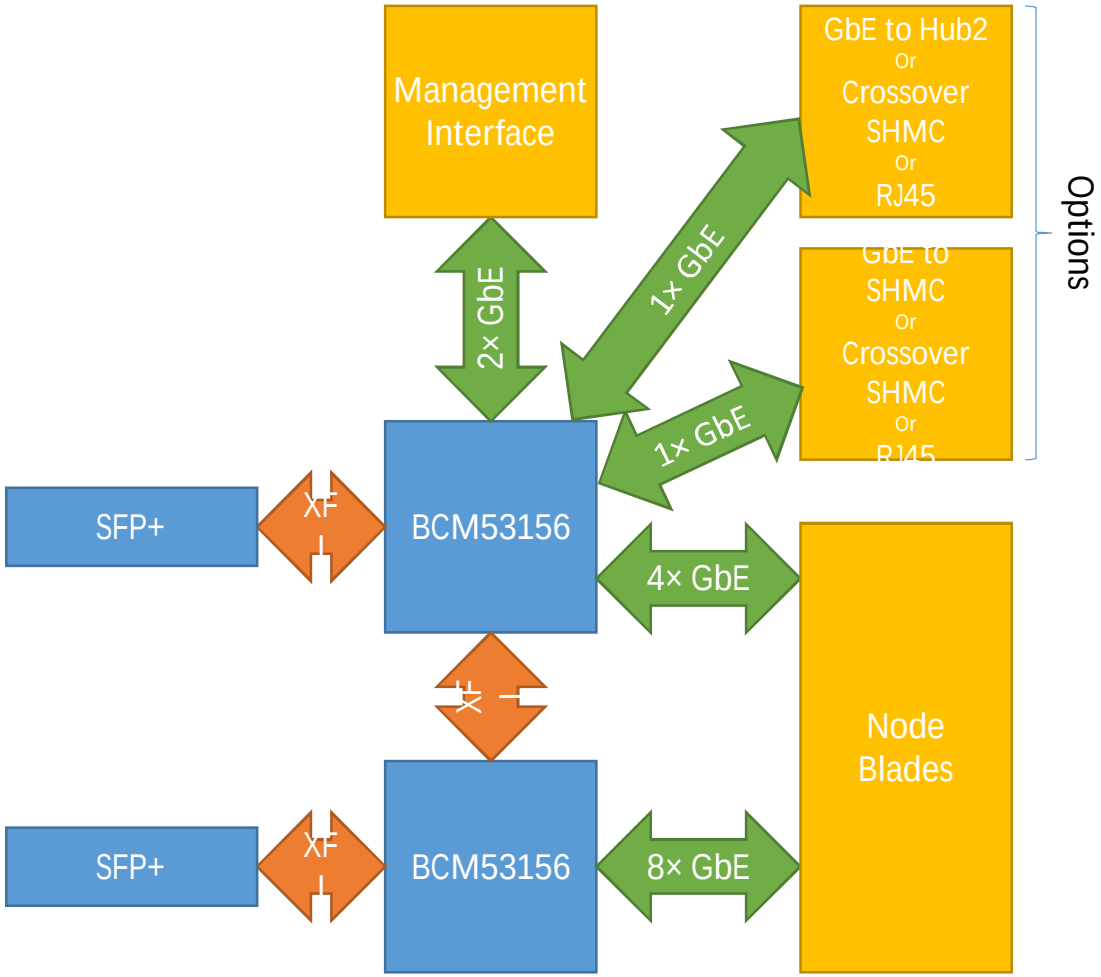
Refer to Andy's slides for details.

From Andy Rose
18 Feb 2019 https://indico.cern.ch/event/799840/

Ethernet

- Capacitively coupled as per Broadcom spec.
- 0402's for easy manipulation
- Options set by selecting which capacitors to fit

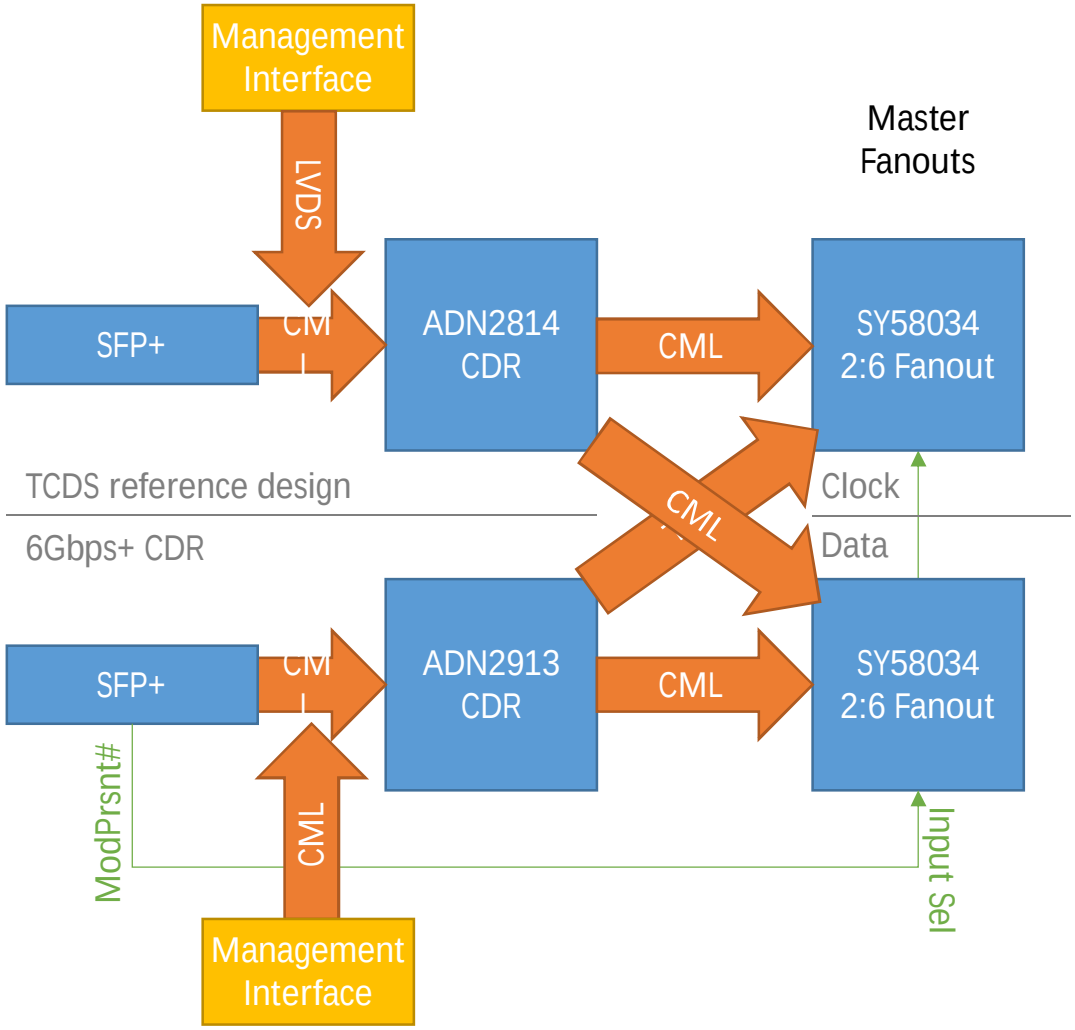
- SPI interface for programming



From Andy Rose
18 Feb 2019 https://indico.cern.ch/event/799840/

TTC CDR

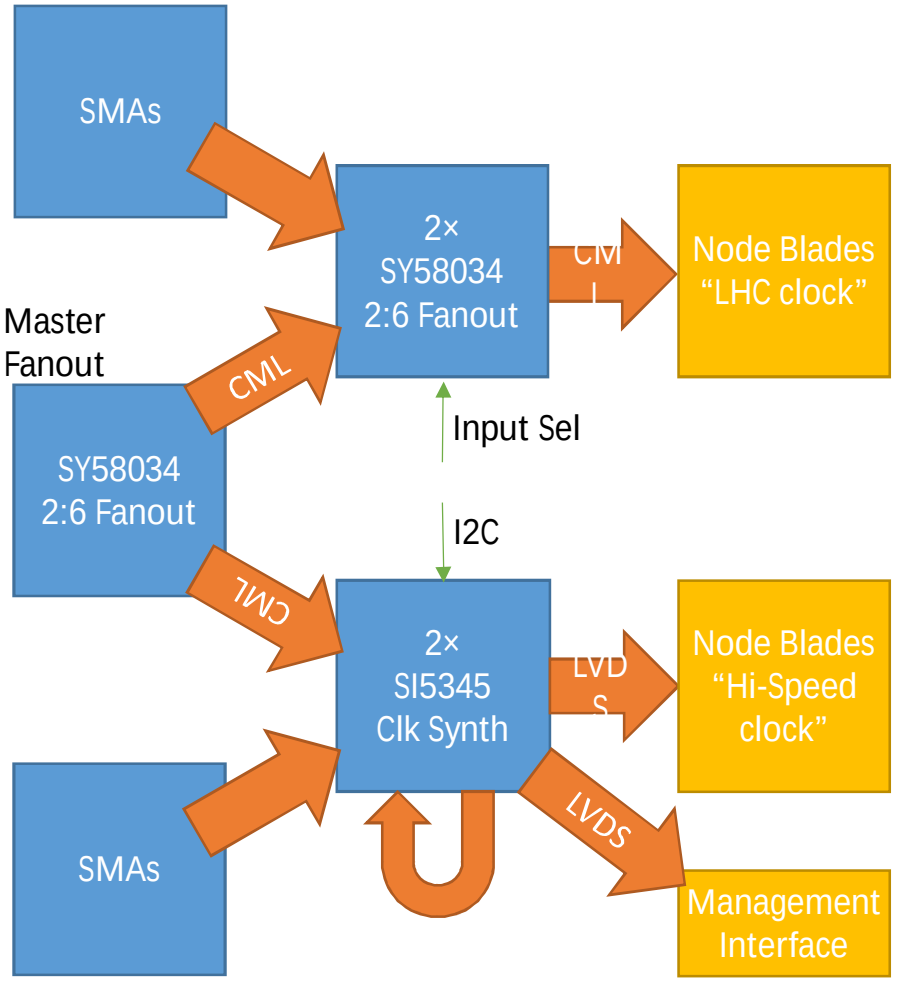
- Two CDR circuits
  - One cloned from TCDS FMC
  - One spec'ed to 8.5Gbps to emulate Gigabit TCDS
- High-performance CML fanout buffers
  - DC to >6GHz
  - 20ps output-to-output skew
  - 60fs RMS jitter
- Fanout inputs selected by either fitting a resistor OR by SFP ModPrsnt# line
- All power supplies filtered
- All traces length-matched to <100µm



From Andy Rose
18 Feb 2019 https://indico.cern.ch/event/799840/

TTC Clock distribution

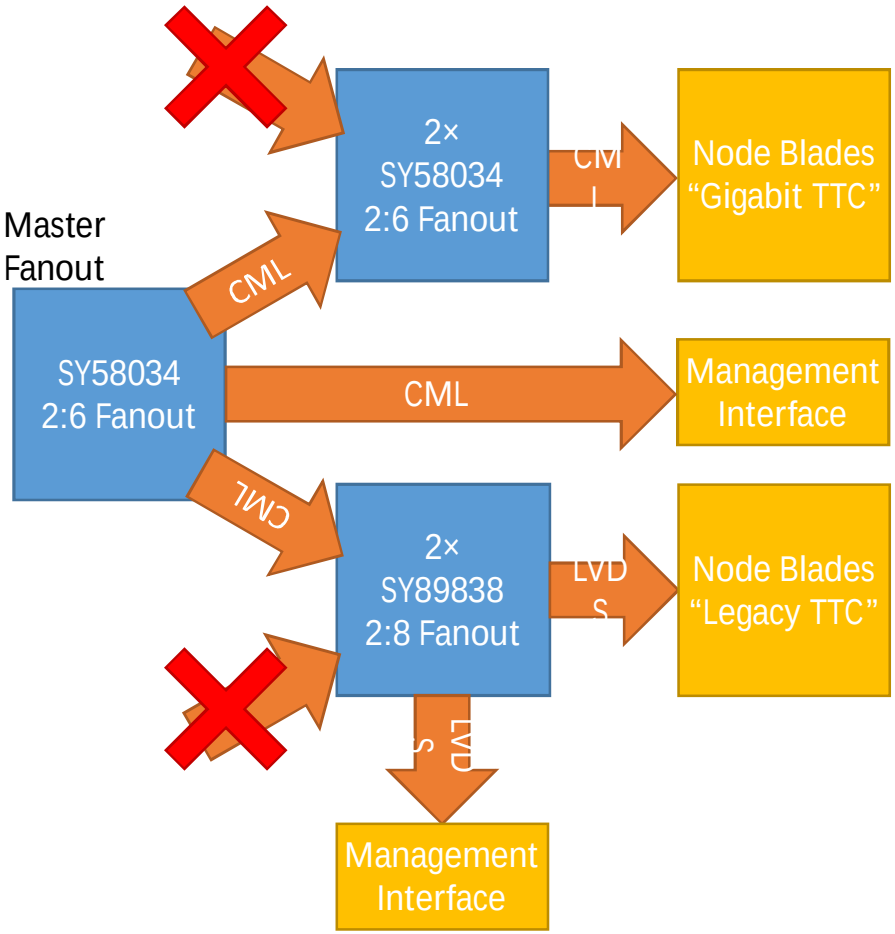
- High-performance CML fanout buffers
  - DC to >6GHz
  - 20ps output-to-output skew
  - 60fs RMS jitter
  - SMA input selected by fitting resistor
- "Hi-Speed" LHC clock provided with SI5345's
  - Includes provision for phase-locked operation
  - SMAs for clock-distribution testing
  - I2C control
- All power supplies filtered
- All traces length-matched to < 100µm



From Andy Rose
18 Feb 2019 https://indico.cern.ch/event/799840/

TTC Data distribution

- High-performance CML fanout buffers for “Gigabit TTC”
  - DC to >6GHz
  - 20ps output-to-output skew
  - 60fs RMS jitter
- High-performance LVDS fanout buffers for “Legacy TTC”
  - DC to >1.5GHz
  - 40ps output-to-output skew
  - 150fs RMS jitter
- All power supplies filtered
- All traces length-matched to < 100µm



From Andy Rose
18 Feb 2019 https://indico.cern.ch/event/799840/

Status (from Greg Iles)

- Expecting ~10 around the end of April


Science & Technology Facilities Council
INFN Istituto Nazionale Fisica Nucleare Sezione di Pisa
Imperial College London
KIT Karlsruher Institut für Technologie
SERENITY
Andy Rose, Imperial College, London
tifr tata institute of fundamental research
CERN
University of BRISTOL
cea SACLAY
UNIVERSITY OF IOANNINA

SERENITY 1.1 STATUS

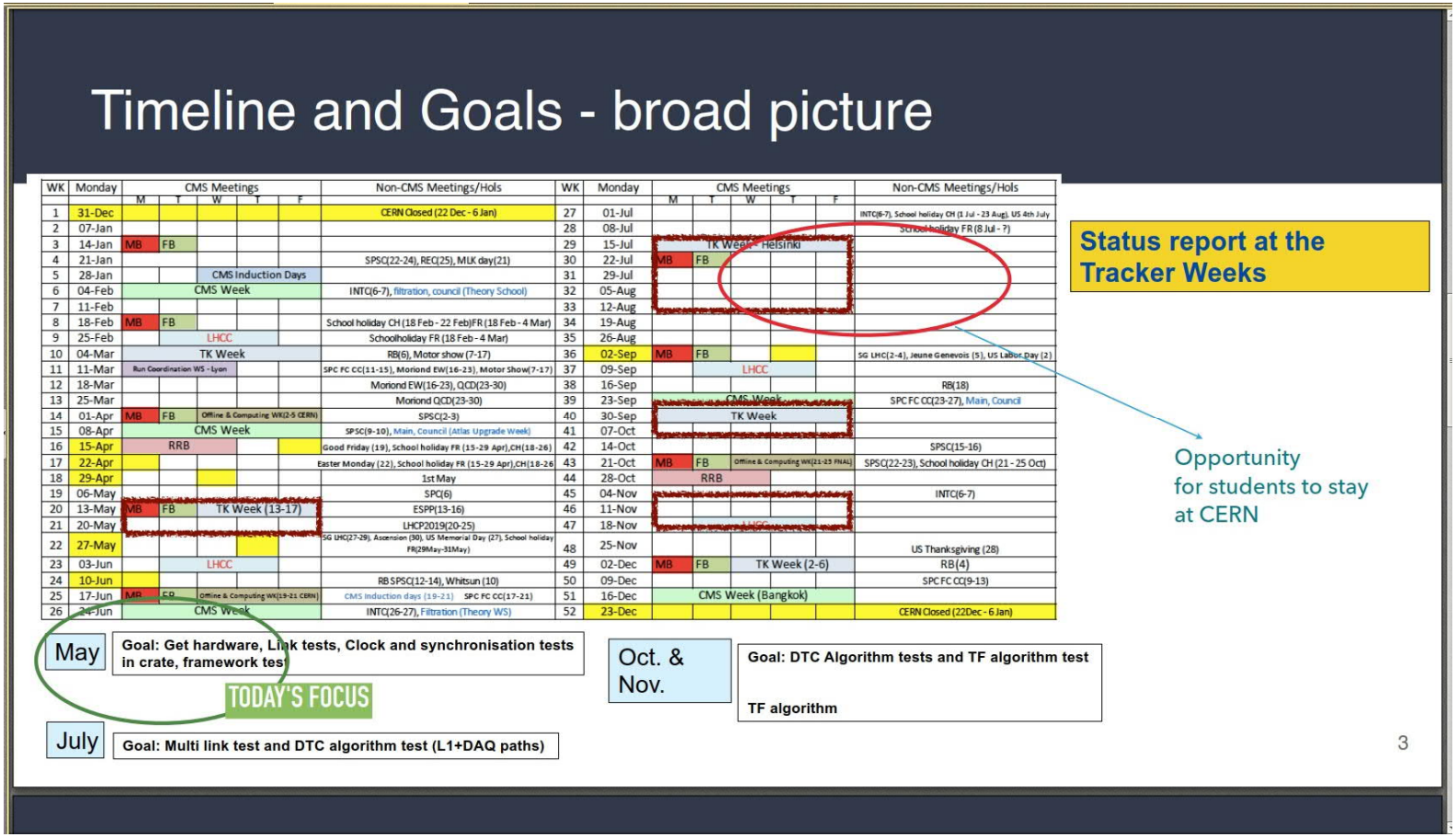
- 5 blades ready for distribution
  - Currently sorting paperwork
- 2 blades in assembly at KIT
- 13 PCBs and components ready for assembly
  - Currently sorting paperwork
  - Want to send out order soon
  - Speak to Greg if you are interested in one
- To do: move standalone software into integrated framework
  - Meeting at RAL next week to discuss

Status (from slides and Greg Iles)

- Looks like 7 already exist?
- Expecting 10 more around the end of March

Integration Testing Goals

- Good to have goals, leads to discussion of home-site procedures and needs
- Goal 1: First test at TIF in mid-May
- Marginal probability of Apollo being ready, would like to test with Crystal at home.



Timeline and Goals - broad picture

WK	Monday	CMS Meetings M	T	W	T	F	Non-CMS Meetings/Hols
1	31-Dec						CERN Closed (22 Dec - 6 Jan)
2	07-Jan						
3	14-Jan	MB	FB				
4	21-Jan						SPSC(22-24), REC(25), MLK day(21)
5	28-Jan			CMS Induction Days			
6	04-Feb	CMS Week					INTC(6-7), filtration, council (Theory School)
7	11-Feb						
8	18-Feb	MB	FB				School holiday CH (18 Feb - 22 Feb)FR (18 Feb - 4 Mar)
9	25-Feb	LHCC					Schoolholiday FR (18 Feb - 4 Mar)
10	04-Mar	TK Week					RB(6), Motor show (7-17)
11	11-Mar	Run Coordination WS - Lyon					SPC FC CC(11-15), Moriond EW(16-23), Motor Show(7-17)
12	18-Mar						Moriond EW(16-23), QCD(23-30)
13	25-Mar						Moriond QCD(23-30)
14	01-Apr	MB	FB	Offline & Computing WK(2-5 CERN)			SPSC(2-3)
15	08-Apr	CMS Week					SPSC(9-10), Main, Council (Atlas Upgrade Week)
16	15-Apr	RRB					Good Friday (19), School holiday FR (15-29 Apr),CH(18-26)
17	22-Apr						Easter Monday (22), School holiday FR (15-29 Apr),CH(18-26
18	29-Apr						1st May
19	06-May						SPC(6)
20	13-May	MB	FB	TK Week (13-17)			ESPP(13-16)
21	20-May						LHCP2019(20-25)
22	27-May						SG LHC(27-29), Ascension (30), US Memorial Day (27), School holiday FR(29May-31May)
23	03-Jun		LHCC				
24	10-Jun						RB SPSC(12-14), Whitsun (10)
25	17-Jun	MB	FB	Offline & Computing WK(19-21 CERN)			CMS Induction days (19-21) SPC FC CC(17-21)
26	24-Jun	CMS Week					INTC(26-27), Filtration (Theory WS)

WK	Monday	CMS Meetings M	T	W	T	F	Non-CMS Meetings/Hols
27	01-Jul						INTC(6-7), School holiday CH (1 Jul - 23 Aug), US 4th July
28	08-Jul						School holiday FR (8 Jul - ?)
29	15-Jul	TK Week - Helsinki					
30	22-Jul	MB	FB				
31	29-Jul						
32	05-Aug						
33	12-Aug						
34	19-Aug						
35	26-Aug						
36	02-Sep	MB	FB				SG LHC(2-4), Jeune Genevois (5), US Labor Day (2)
37	09-Sep		LHCC				
38	16-Sep						RB(18)
39	23-Sep	CMS Week					SPC FC CC(23-27), Main, Council
40	30-Sep	TK Week					
41	07-Oct						
42	14-Oct						SPSC(15-16)
43	21-Oct	MB	FB	Offline & Computing WK(21-25 FNAL)			SPSC(22-23), School holiday CH (21 - 25 Oct)
44	28-Oct	RRB					
45	04-Nov						INTC(6-7)
46	11-Nov						
47	18-Nov						
48	25-Nov						US Thanksgiving (28)
49	02-Dec	MB	FB	TK Week (2-6)			RB(4)
50	09-Dec						SPC FC CC(9-13)
51	16-Dec	CMS Week (Bangkok)					
52	23-Dec						CERN Closed (22Dec - 6 Jan)

Status report at the Tracker Weeks

Opportunity for students to stay at CERN

May Goal: Get hardware, Link tests, Clock and synchronisation tests in crate, framework test

TODAY'S FOCUS

July Goal: Multi link test and DTC algorithm test (L1+DAQ paths)

Oct. & Nov. Goal: DTC Algorithm tests and TF algorithm test

TF algorithm

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From Fabrizio Palla and Thomas Owen James
11 Feb 2019 https://indico.cern.ch/event/797875/