THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY.
THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: GLOBAL SIGNALS
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: KU15P POWER AND SIGNAL (NON-MGT)
6: VU7P POWER AND SIGNAL (NON-MGT)
7: KU15P MGT TRANSCEIVERS
8: VU7P MGT TRANSCEIVERS

TO DO:

CHECK "bc" AND "ac" PREFIXES ON AC-COUPLED SIGNALS

ON VU7P QUAD "S', CHANGE "...133" TO "...S" IN PIN NAMES

ON VU7P QUAD "A-J', CHANGE "...GTH" TO "...GTY" IN PIN NAMES

ADD INTER-SHEET REFERENCES

ASSIGN AND LABEL I2C ADDRESSES

SOLDERPASTE PATTERNS FOR UEC5_UCCE FOOTPRINT

NETS TO STUDY / DOCUMENT

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.01: NOTES		
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Firefly #V1
4 Ch XCVR
4 GTY I/O
Firefly #V2
4 Ch XCVR
4 GTY I/O
Firefly #V3
4 Ch XCVR
4 GTY I/O
Firefly #V4
4 Ch XCVR
4 GTY I/O
Firefly #V5
4 Ch XCVR
4 GTY I/O
Firefly #V6
4 Ch XCVR
4 GTY I/O
Firefly #V7
4 Ch XCVR
4 GTY I/O
Firefly #V8
4 Ch XCVR
4 GTY I/O
Firefly #V9
4 Ch XCVR
4 GTY I/O
Firefly #V10
4 Ch XCVR
4 GTY I/O
Firefly #V11
12 Ch
XMIT/RECV
4 GTY I/O
4 GTY I/O
4 GTY I/O
Firefly #V12
12 Ch
XMIT/RECV
4 GTY I/O
4 GTY I/O
4 GTY I/O

UltraScale+
FPGA
B2104 Package
76 GTY

VU5P
VU7P*
VU9P
VU11P

***=Initial Target**

CONFIG
FLASH
CONFIG
FLASH
3 GTY I/O
UTILITY I/O
POWER & I2C
CONTROLLER
POWER
REGULATORS
CLOCK &
TIMING
UTILITY I/O
JTAG
2 GTY I/O
ZYNQ PCIe / AXI C2C
BLADE
CONNECTORS
2 GTH I/O
ZYNQ PCIe / AXI C2C

Kintex
UltraScale+
FPGA
A1760 Package
44 GTH
32 GTY

KU15P*

***=Only choice in this package**

4 GTH I/O
4 GTH I/O
4 GTH I/O
Firefly #K1
12 Ch
XMIT/RECV
4 GTH I/O
4 GTH I/O
4 GTH I/O
Firefly #K2
12 Ch
XMIT/RECV
4 GTH I/O
4 GTH I/O
4 GTH I/O
Firefly #K3
12 Ch
XMIT/RECV
4 GTY I/O
Firefly #K4
4 Ch XCVR
4 GTY I/O
Firefly #K5
4 Ch XCVR
4 GTY I/O
Firefly #K6
4 Ch XCVR
4 GTY I/O
4 GTY I/O
4 GTY I/O
Firefly #K7
12 Ch
XMIT/RECV

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title
1.02: BLOCK DIAGRAM
Size | Document Number 6089-103 | Rev A
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KU15P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

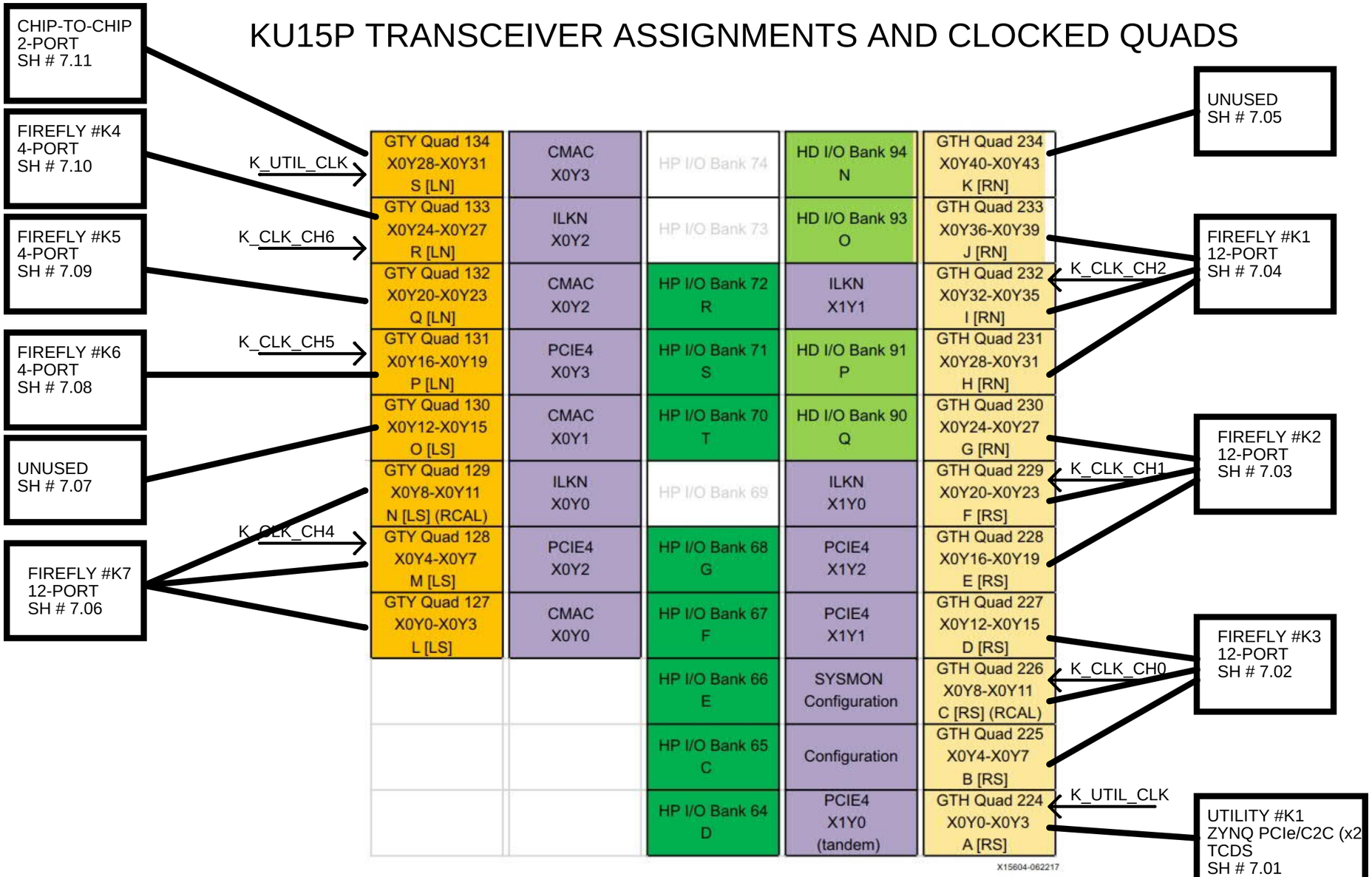

Figure 1-86: **XCKU15P Banks in FFVA1760 Package**

EACK "K_CLK_CHn" CONSISTS OF TWO CLOCKS.
ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.03: KU15P TRANSCEIVERS		
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VU7P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

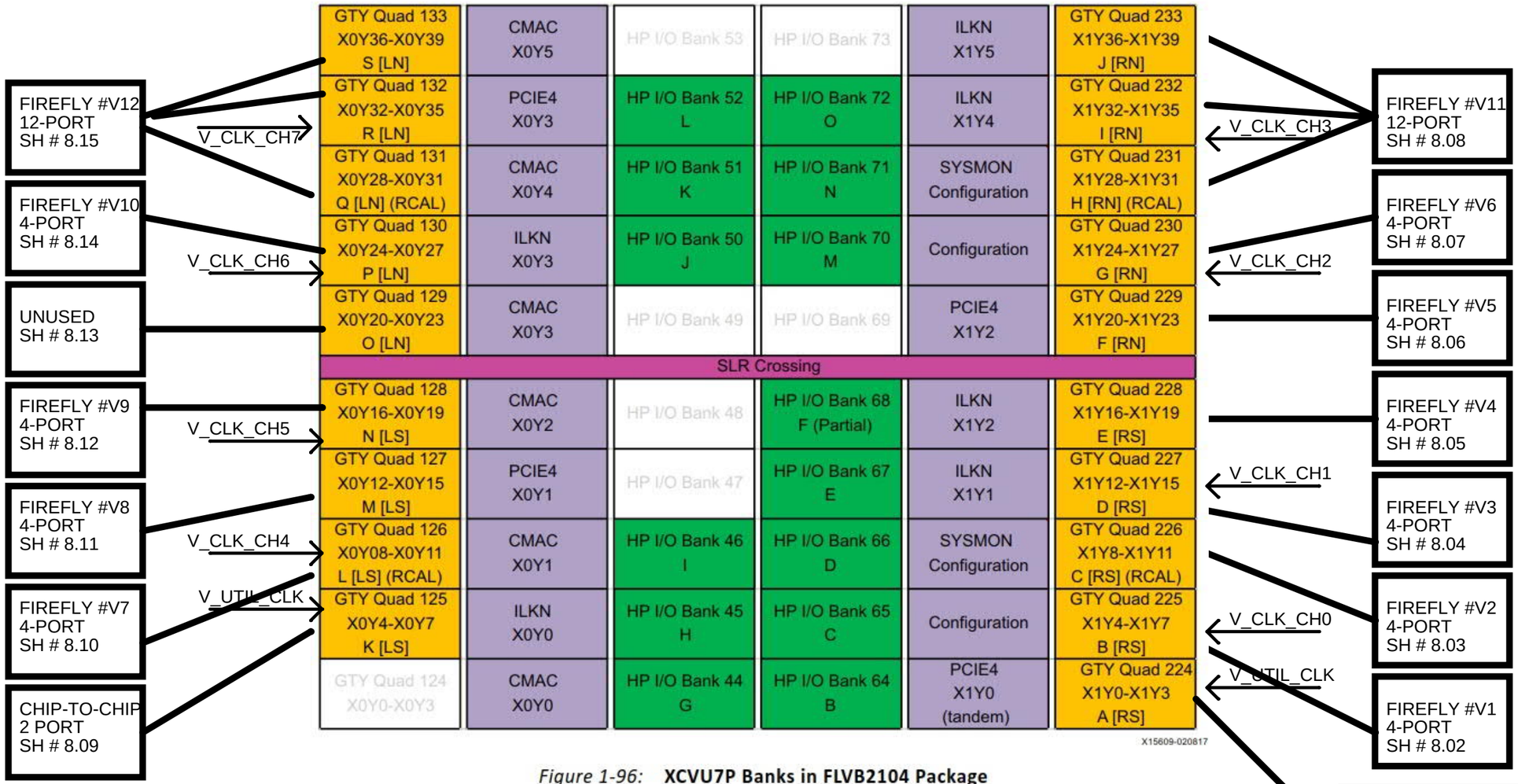

Figure 1-96: **XCVU7P Banks in FLVB2104 Package**

EACK "V_CLK_CHn" CONSISTS OF TWO CLOCKS. ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.04: VU7P TRANSCEIVERS		
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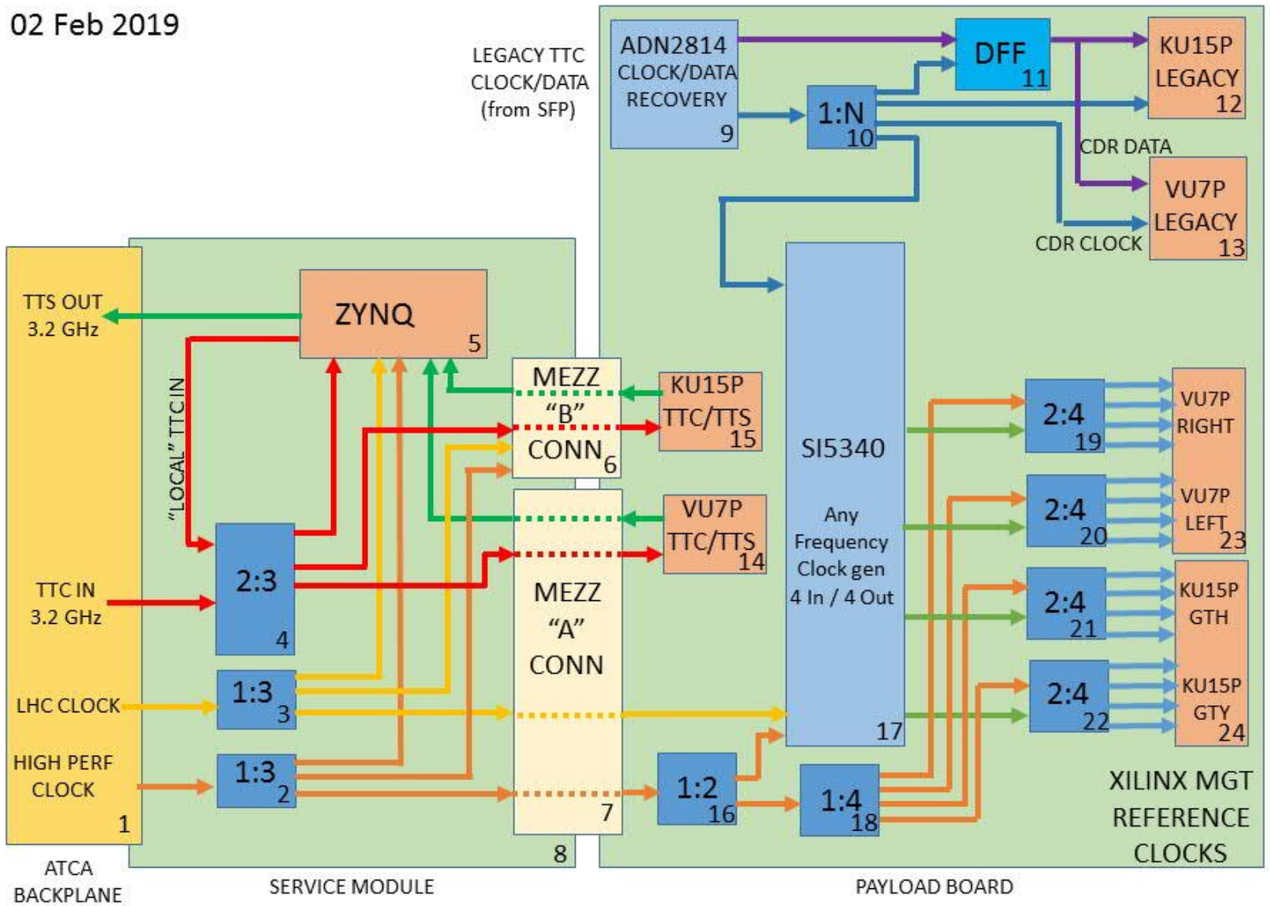
BU/CU Apollo ATCA Backplane Signal Distribution

02 Feb 2019



Charlie Strohman crs5@cornell.edu

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.05: LHC SIGNAL DISTRIBUTION		
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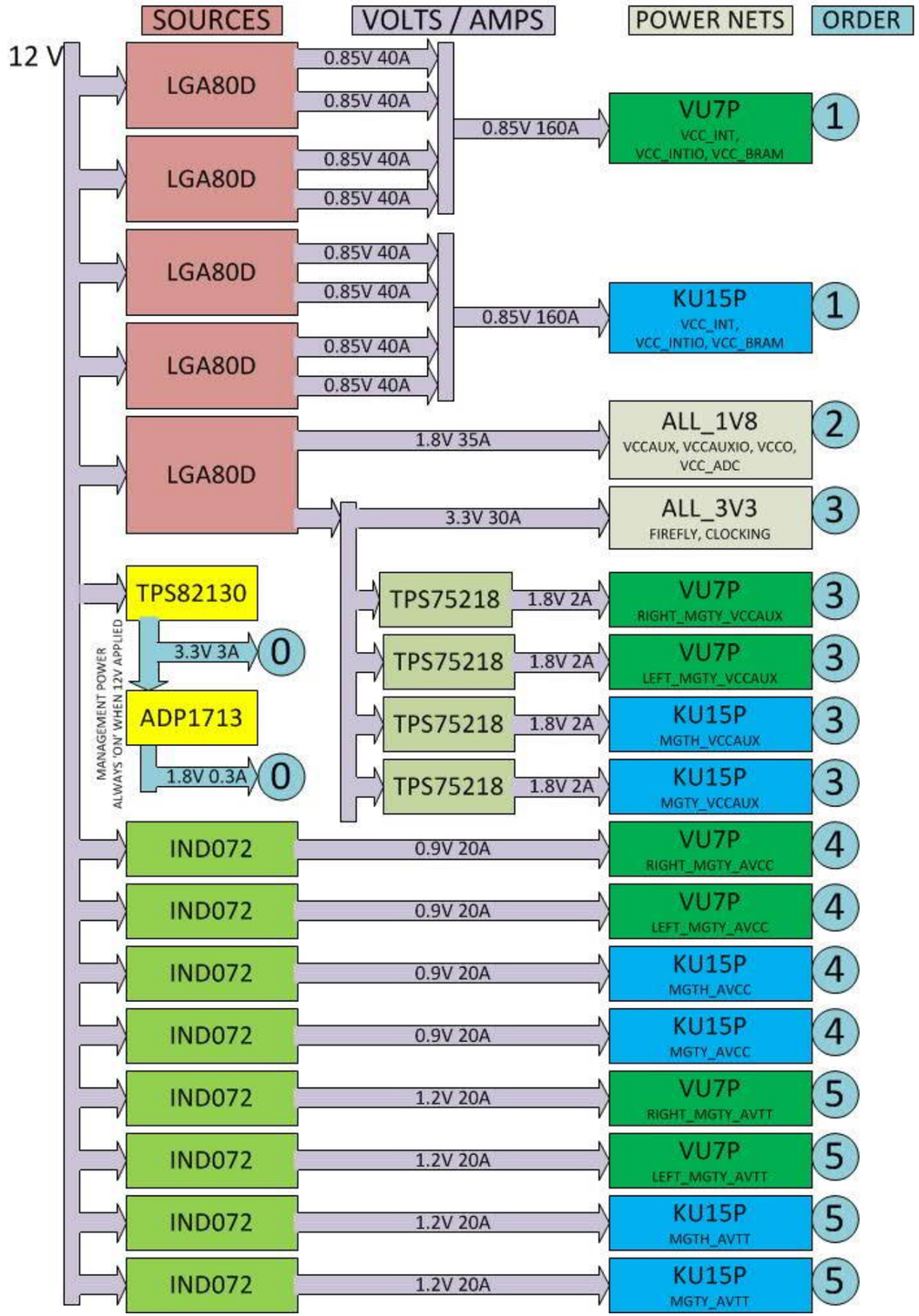

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 1.06: POWER DISTRIBUTION		
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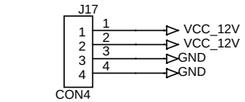
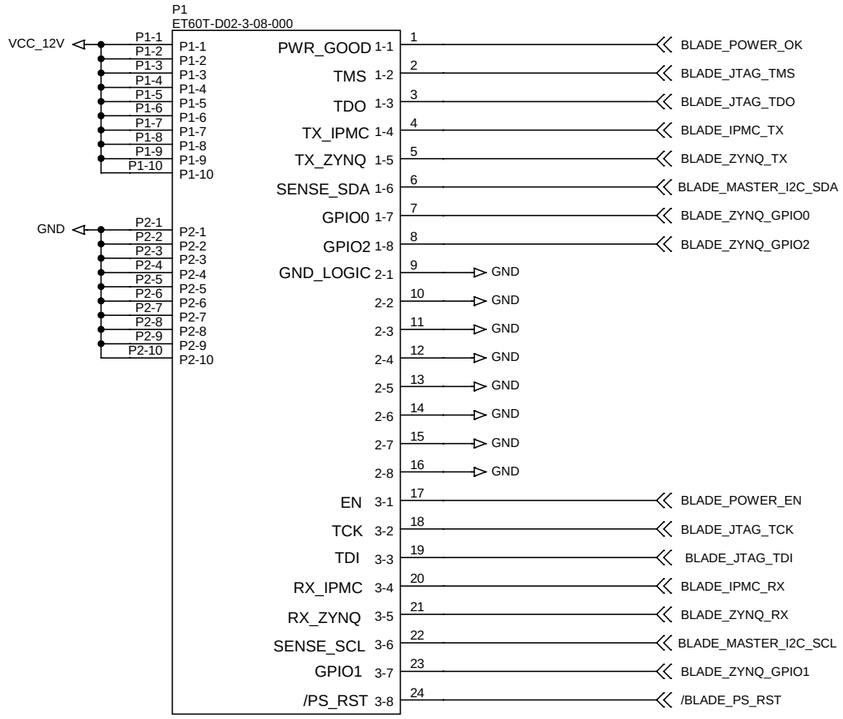


Bench Top Power Inlet



THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.

SP2 DNI

SP1 DNI

THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINKS

H13 DNI, H12 DNI, H11 DNI

H8 DNI, H7 DNI, H6 DNI

THESE HOLES ARE FOR MOUNTING THE TOP COVER

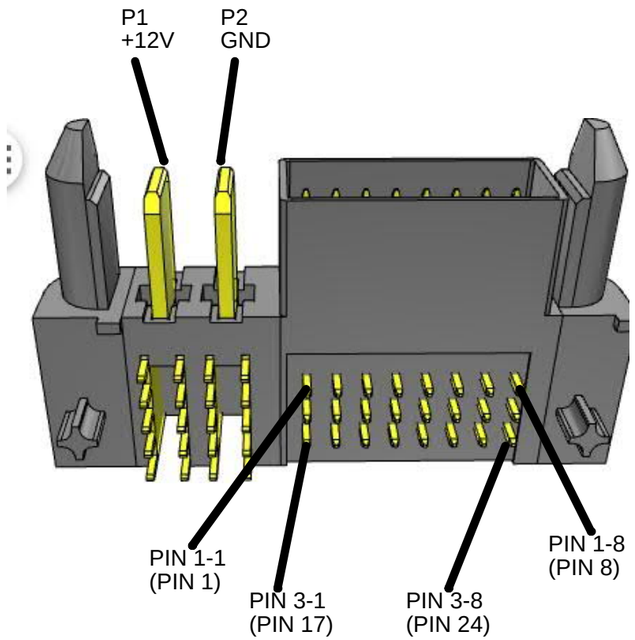
H5 DNI, H18 DNI, H4 DNI

H17 DNI, H3 DNI, H16 DNI

THESE HOLES ARE FOR MOUNTING THE BOTTOM COVER

H1 DNI, H14 DNI, H9 DNI

H15 DNI, H10 DNI, H2 DNI



ET60T-D02-3-08-000

THESE SHAPES DEFINE MECHANICAL OBJECTS THAT SHOULD BE IN THE BILL OF MATERIALS.

M1 KU15P HEATSINK

M23 HEATSINK PLATE

M3 M3 STANDOFF, M4 M3 STANDOFF, M5 M3 STANDOFF, M6 M3 STANDOFF, M7 M3 STANDOFF, M8 M3 STANDOFF

M2 VU7P HEATSINK

M24 HEATSINK PLATE

M9 M3 STANDOFF, M10 M3 STANDOFF, M11 M3 STANDOFF, M12 M3 STANDOFF, M13 M3 STANDOFF, M14 M3 STANDOFF

M15 FIREFLY HEATSINK (LEFT SIDE)

M16 M2.5 STANDOFF, M17 M2.5 STANDOFF, M18 M2.5 STANDOFF

M19 FIREFLY HEATSINK (RIGHT SIDE)

M20 M2.5 STANDOFF, M21 M2.5 STANDOFF, M22 M2.5 STANDOFF

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.01: BLADE POWER CONNECTOR		
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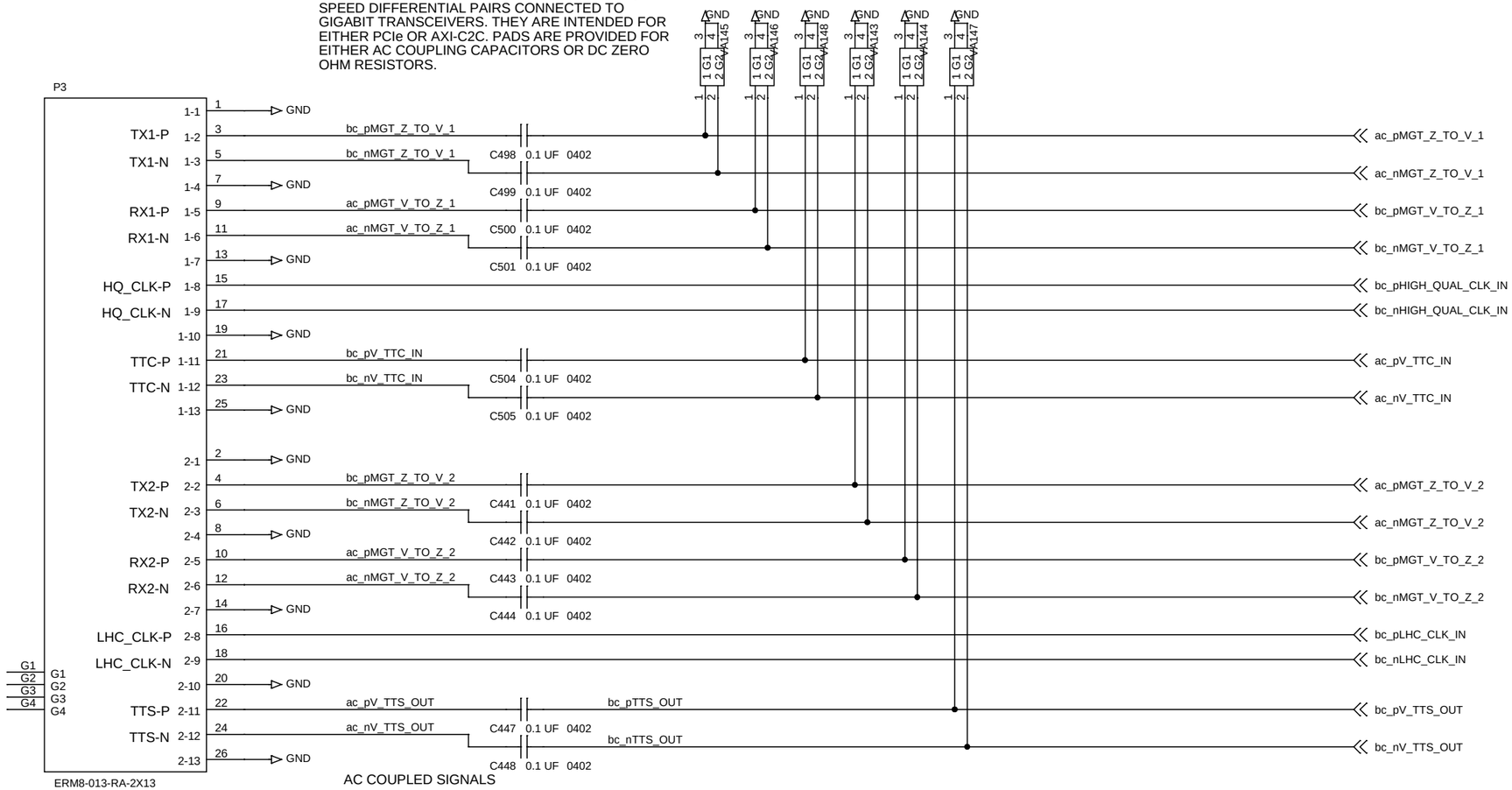
THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.

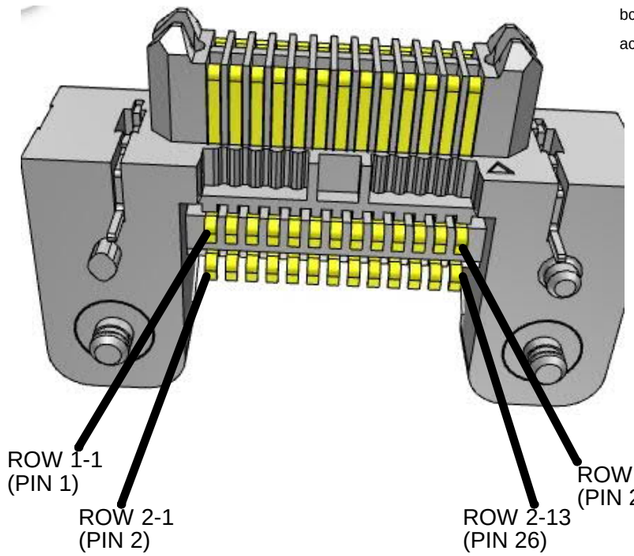


AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

VU7P AND BACKPLANE CLOCK SIGNALS ONLY



ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.02: BLADE HS CONNECTOR #1		
Size	Document Number: 6089-103	Rev: A
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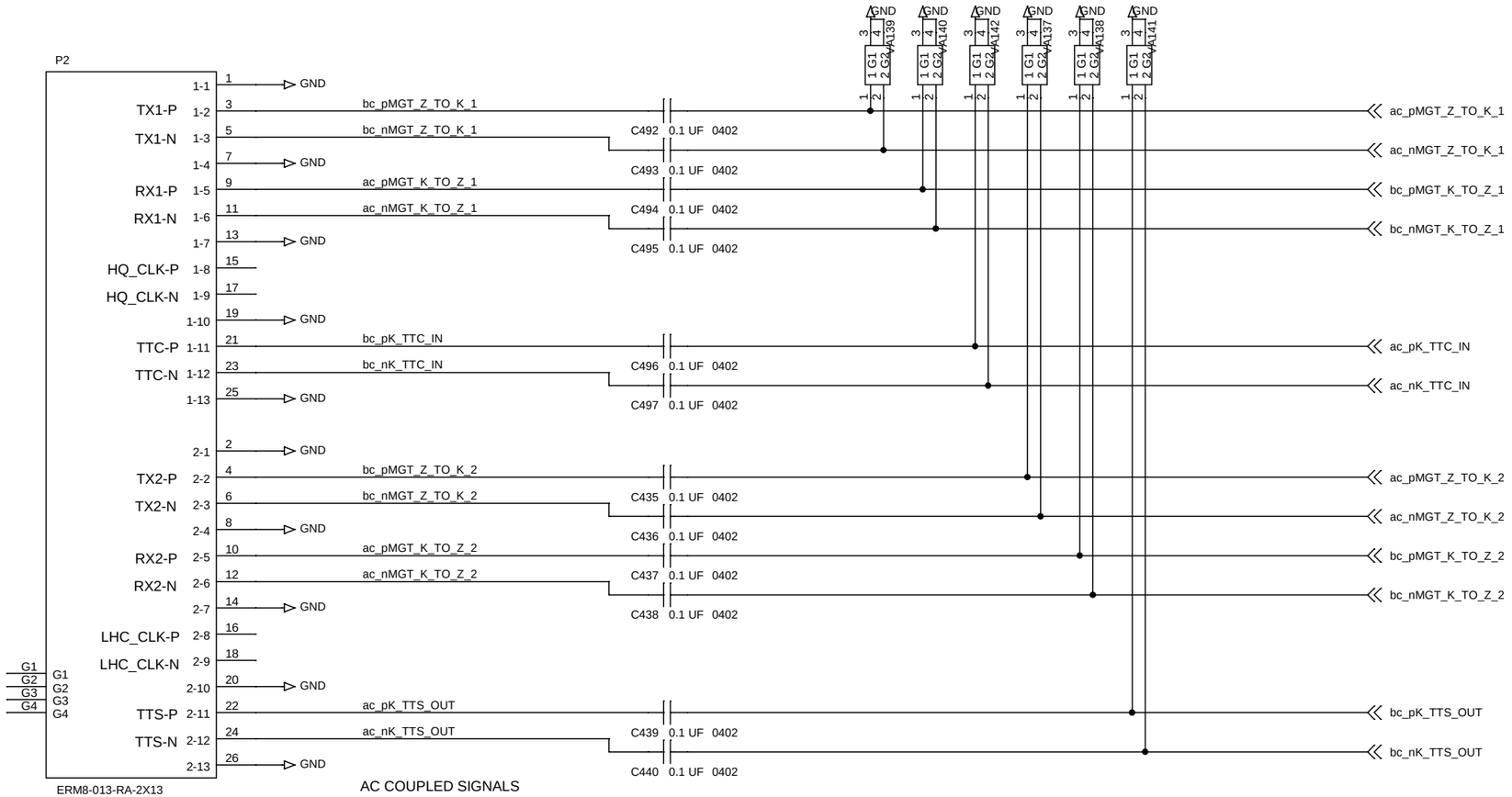
THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.

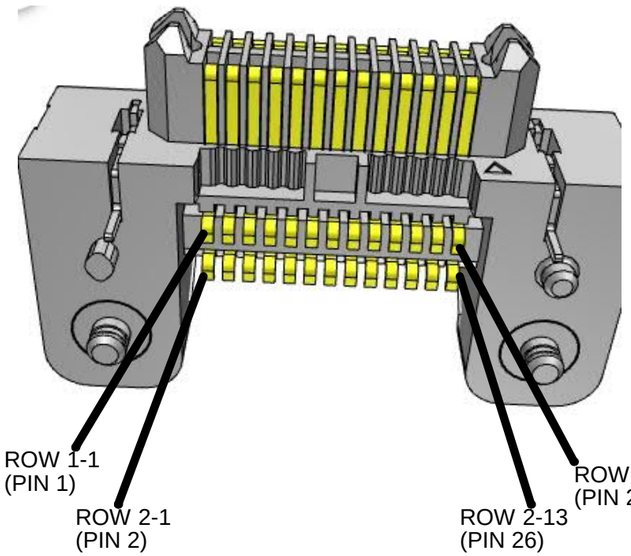


AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

KU15P SIGNALS ONLY



ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 2.03: BLADE HS CONNECTOR #2			
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TO BYPASS A DEVICE, CONNECT A JUMPER FROM 1 TO 3.
TO INCLUDE A DEVICE IN THE CHAIN, CONNECT A JUMPER FROM 1 TO 2 AND FROM 3 TO 4.
AS ILLUSTRATED, THE CONTROLLER AND THE VU7P ARE PART OF THE CHAIN, AND THE KU15P IS BYPASSED.

BLADE JTAG

BLADE_JTAG_TMS

VCC_M3V3 R108 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

U49 74LVC1G126 — R92 33 0603 — V_TMS_1V8
U53 74LVC1G126 — R98 33 0603 — K_TMS_1V8
U57 74LVC1G126 — R107 33 0603 — C_TMS_3V3
U50 74LVC1G125 — R95 33 0603 — VCC_M1V8
U55 74LVC1G125 — R101 33 0603 — VCC_M1V8
U60 74LVC1G125 — R109 33 0603 — VCC_M3V3
U62 74LVC1G126 — R113 33 0603 — V_TCK_1V8
U77 74LVC1G126 — R123 33 0603 — K_TCK_1V8
U84 74LVC1G126 — R133 33 0603 — C_TCK_3V3
U67 74LVC1G125 — R116 33 0603 — VCC_M1V8
U78 74LVC1G125 — R130 33 0603 — VCC_M1V8
U86 74LVC1G125 — R136 33 0603 — VCC_M3V3

VCC_M3V3 R94 10K 0603

VCC_M3V3 R115 10K 0603

BLADE JTAG

BLADE_JTAG_TCK

VCC_M3V3 R134 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

IF EITHER THE JUMPER IS IN PLACE, OR THE PROGRAMMING CABLE IS PLUGGED IN, THE OUTPUT OF THIS BUFFER WILL BE LOW. THIS WILL ENABLE ALL OF THE DRIVERS RELATED TO THE CABLE SIGNALS, AND DISABLE ALL OF THE DRIVERS RELATED TO THE MAIN BLADE.

VCC_M3V3 R70 10K 0603

U37 74LVC1G125 — VCC_M3V3

J12 JUMPER

THE JTAG REFERENCE IS 3.3 VOLTS.

J1 CON_2X7_RA
CONN_JTAG_TMS
CONN_JTAG_TCK
CONN_JTAG_TDO
CONN_JTAG_TDI

USE THE JUMPER IF PIN 13 IS NOT AUTOMATICALLY PULLED LOW WHEN THE CABLE IS PLUGGED IN.

PIN 13 SHOULD BE PULLED LOW WHEN THE CABLE IS PLUGGED IN.

FRONT PANEL JTAG

BLADE JTAG

BLADE_JTAG_TDI

VCC_M3V3 R86 10K 0603

VCC_M3V3 R82 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE MAIN BLADE OR THE EXTERNAL PROGRAMMER.

U38 74AUP1T34 — R72 33 0603 — VCC_M1V8 — VCC_M3V3
U40 74AUP1T34 — R81 33 0603 — VCC_M1V8 — VCC_M3V3 — BLADE_JTAG_TDO

BLADE JTAG

JUMPER_2X2 J13
BYPASS JUMPER

U66-43 FPGA_VU7P_B2104 — JTAG
V_TDO AC13 TDO_0
V_TDI AE15 TDI_0
V_TMS_1V8 AG15 TMS_0
V_TCK_1V8 AE13 TCK_0

VU7P

U7 74LVC1G125 — R11 33 0603 — VCC_M1V8

VCC_M3V3 — C771 C766 C752 C747 C825 0.1 UF 0402 — GND
VCC_M3V3 — C812 C809 C803 C826 0.1 UF 0402 — GND

JUMPER_2X2 J14
BYPASS JUMPER

U65-11 FPGA_KU15P_A1760 — JTAG
K_TDO AK16 TDO_0
K_TDI AJ15 TDI_0
K_TMS_1V8 AJ17 TMS_0
K_TCK_1V8 AK15 TCK_0

KU15P

TDI_1V8

U9 74LVC1G125 — R25 33 0603 — VCC_M1V8

VCC_M1V8 — C794 C786 C781 C778 C762 0.1 UF 0402 — GND
VCC_M1V8 — C761 C758 C755 C969 C971 0.1 UF 0402 — GND

JUMPER_2X2 J15
BYPASS JUMPER

U52-1 TM4C1290NCPDT
C_TDO 97 JTAG_TDO
C_TDI 98 JTAG_TDI
C_TMS_3V3 99 JTAG_TMS
C_TCK_3V3 100 JTAG_TCK

CONTROLLER

TDI_3V3

U42 74LVC1G126 — R85 33 0603 — VCC_M3V3
U41 74LVC1G125 — R83 33 0603 — VCC_M3V3

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.04: JTAG CHAIN		
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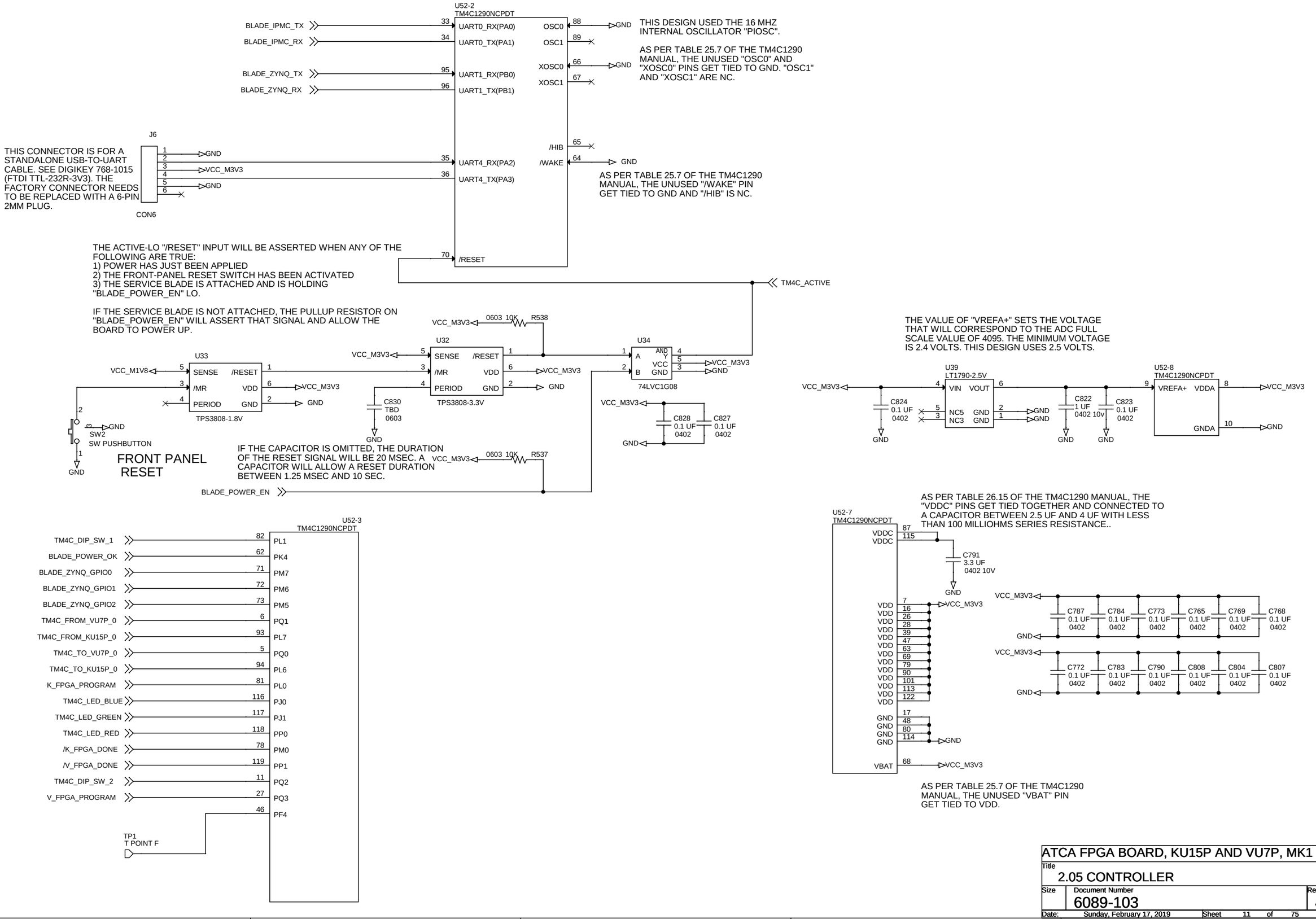

Title	ATCA FPGA BOARD, KU15P AND VU7P, MK1
	2.05 CONTROLLER
Size	
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DO WE NEED TO ADD A BUFFER TO GET AN LHC-BASED CLOCK INTO THE FPGA LOGIC SECTION? WILL USING THE "TXOUTCLK" FROM A GTH/GTY BLOCK BE ADEQUATE?

bc_pLEGACY_CLK — C1 0.1 UF 0402 — ac_pLEGACY_CLK
bc_nLEGACY_CLK — C2 0.1 UF 0402 — ac_nLEGACY_CLK
R129 49.9 0402, R131 49.9 0402, C216 0.1 UF 0402 GND
bc_pLHC_CLK_IN — C445 0.1 UF 0402 — ac_pLHC_CLK_IN
bc_nLHC_CLK_IN — C446 0.1 UF 0402 — ac_nLHC_CLK_IN
R120 49.9 0402, R119 49.9 0402, C205 0.1 UF 0402 GND
bc_pHIGH_QUAL_CLK_IN — C502 0.1 UF 0402 — ac_pHIGH_PERF_CLK_IN
bc_nHIGH_QUAL_CLK_IN — C503 0.1 UF 0402 — ac_nHIGH_PERF_CLK_IN
R138 49.9 0402, R139 49.9 0402, C250 0.1 UF 0402 GND

U81-1 SI5340
pXTAL, X1, 48 MHz, nXTAL
XA, X1_SHIELD, X2_SHIELD, XB
FB_IN /FB_IN
OUT_0 /OUT_0 — pSYNTH_CLK0 / nSYNTH_CLK0
OUT_1 /OUT_1 — pSYNTH_CLK1 / nSYNTH_CLK1
OUT_2 /OUT_2 — pSYNTH_CLK2 / nSYNTH_CLK2
OUT_3 /OUT_3 — pSYNTH_CLK3 / nSYNTH_CLK3
IN_0 /IN_0, IN_1 /IN_1, IN_2 /IN_2

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

WE DO NOT HAVE AN UNUSED OUTPUT, SO WE CAN NOT USE FEEDBACK. ZERO-DELAY BUFFERING IS NOT A REQUIREMENT, NOR IS FIXED PHASE BETWEEN OUTPUTS.

THE SPLIT TERMINATOR WITH A CAPACITOR TO GND IS USED FOR CLOCKS COMING FROM OFF THE BOARD. CLOCKS THAT ARE STRICTLY WITHIN THE BOARD USE SIMPLE 100 OHM TERMINATORS.

U80 SI53340 1:2
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
R126 4.7K 0603 GND
Q0 /Q0 — pHIGH_PERF_CLK_BUF1 / nHIGH_PERF_CLK_BUF1
Q1 /Q1 — pHIGH_PERF_CLK_BUF0 / nHIGH_PERF_CLK_BUF0
Q2 /Q2, Q3 /QE
VDD — VCC_3V3; GND PAD — GND
C751 1 UF 0402 10v
<Implementation>

DC COUPLED LVDS
R121 100 0402, R110 100 0402

U61 SI53340 1:4
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
R105 4.7K 0603 GND
Q0 /Q0 — pHIGH_PERF_CLK0 / nHIGH_PERF_CLK0
Q1 /Q1 — pHIGH_PERF_CLK1 / nHIGH_PERF_CLK1
Q2 /Q2 — pHIGH_PERF_CLK2 / nHIGH_PERF_CLK2
Q3 /QE — pHIGH_PERF_CLK3 / nHIGH_PERF_CLK3
VDD — VCC_3V3; GND PAD — GND
C767 1 UF 0402 10v
<Implementation>

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

AC COUPLED LVDS

U83 SI53340 2:4
pHIGH_PERF_CLK0 / nHIGH_PERF_CLK0 — R127 100 0402, R132 100 0402
pSYNTH_CLK0 / nSYNTH_CLK0
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
R135 4.7K 0603 GND; V_GTY1_SEL_SYNTH
Q0 /Q0 — bc_pV_CLK1_CHAN0 / bc_nV_CLK1_CHAN0 — C228 0.1 UF 0402 — ac_pV_CLK1_CHAN0 / ac_nV_CLK1_CHAN0 — QUAD B
Q1 /Q1 — bc_pV_CLK1_CHAN1 / bc_nV_CLK1_CHAN1 — C232 0.1 UF 0402 — ac_pV_CLK1_CHAN1 / ac_nV_CLK1_CHAN1 — QUAD D
Q2 /Q2 — bc_pV_CLK1_CHAN2 / bc_nV_CLK1_CHAN2 — C241 0.1 UF 0402 — ac_pV_CLK1_CHAN2 / ac_nV_CLK1_CHAN2 — QUAD G
Q3 /QE — bc_pV_CLK1_CHAN3 / bc_nV_CLK1_CHAN3 — C244 0.1 UF 0402 — ac_pV_CLK1_CHAN3 / ac_nV_CLK1_CHAN3 — QUAD I
VDD — VCC_3V3; GND PAD — GND
C754 1 UF 0402 10v
<Implementation>

DC COUPLED LVDS

THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.

U56 SI53340 2:4
pHIGH_PERF_CLK1 / nHIGH_PERF_CLK1 — R97 100 0402, R100 100 0402
pSYNTH_CLK1 / nSYNTH_CLK1
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
R106 4.7K 0603 GND; V_GTY2_SEL_SYNTH
Q0 /Q0 — bc_pV_CLK1_CHAN4 / bc_nV_CLK1_CHAN4 — C149 0.1 UF 0402 — ac_pV_CLK1_CHAN4 / ac_nV_CLK1_CHAN4 — QUAD L
Q1 /Q1 — bc_pV_CLK1_CHAN5 / bc_nV_CLK1_CHAN5 — C151 0.1 UF 0402 — ac_pV_CLK1_CHAN5 / ac_nV_CLK1_CHAN5 — QUAD N
Q2 /Q2 — bc_pV_CLK1_CHAN6 / bc_nV_CLK1_CHAN6 — C158 0.1 UF 0402 — ac_pV_CLK1_CHAN6 / ac_nV_CLK1_CHAN6 — QUAD P
Q3 /QE — bc_pV_CLK1_CHAN7 / bc_nV_CLK1_CHAN7 — C160 0.1 UF 0402 — ac_pV_CLK1_CHAN7 / ac_nV_CLK1_CHAN7 — QUAD R
VDD — VCC_3V3; GND PAD — GND
C780 1 UF 0402 10v
<Implementation>

DC COUPLED LVDS

THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.

AC COUPLED LVDS

U87 SI53340 2:4
pHIGH_PERF_CLK2 / nHIGH_PERF_CLK2 — R147 100 0402, R143 100 0402
pSYNTH_CLK2 / nSYNTH_CLK2
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
R140 4.7K 0603 GND; K_GTH_SEL_SYNTH
Q0 /Q0 — bc_pK_CLK1_CHAN0 / bc_nK_CLK1_CHAN0 — C286 0.1 UF 0402 — ac_pK_CLK1_CHAN0 / ac_nK_CLK1_CHAN0 — QUAD C
Q1 /Q1 — bc_pK_CLK1_CHAN1 / bc_nK_CLK1_CHAN1 — C281 0.1 UF 0402 — ac_pK_CLK1_CHAN1 / ac_nK_CLK1_CHAN1 — QUAD F
Q2 /Q2 — bc_pK_CLK1_CHAN2 / bc_nK_CLK1_CHAN2 — C270 0.1 UF 0402 — ac_pK_CLK1_CHAN2 / ac_nK_CLK1_CHAN2 — QUAD I
Q3 /QE — SPARE — C264 0.1 UF 0402 — QUAD SPARE
VDD — VCC_3V3; GND PAD — GND
C736 1 UF 0402 10v
<Implementation>

DC COUPLED LVDS

THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.

AC COUPLED LVDS

U68 SI53340 2:4
pHIGH_PERF_CLK3 / nHIGH_PERF_CLK3 — R125 100 0402, R117 100 0402
pSYNTH_CLK3 / nSYNTH_CLK3
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
R114 4.7K 0603 GND; K_GTY_SEL_SYNTH
Q0 /Q0 — bc_pK_CLK1_CHAN4 / bc_nK_CLK1_CHAN4 — C211 0.1 UF 0402 — ac_pK_CLK1_CHAN4 / ac_nK_CLK1_CHAN4 — QUAD M
Q1 /Q1 — bc_pK_CLK1_CHAN5 / bc_nK_CLK1_CHAN5 — C204 0.1 UF 0402 — ac_pK_CLK1_CHAN5 / ac_nK_CLK1_CHAN5 — QUAD P
Q2 /Q2 — bc_pK_CLK1_CHAN6 / bc_nK_CLK1_CHAN6 — C200 0.1 UF 0402 — ac_pK_CLK1_CHAN6 / ac_nK_CLK1_CHAN6 — QUAD R
Q3 /QE — C191 0.1 UF 0402 — C189 0.1 UF 0402 — C181 0.1 UF 0402
VDD — VCC_3V3; GND PAD — GND
C759 1 UF 0402 10v
<Implementation>

DC COUPLED LVDS

THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.

AC COUPLED LVDS
bc = BEFORE CAPACITOR
ac = AFTER CAPACITOR

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title: 2.06: LHC CLOCKING
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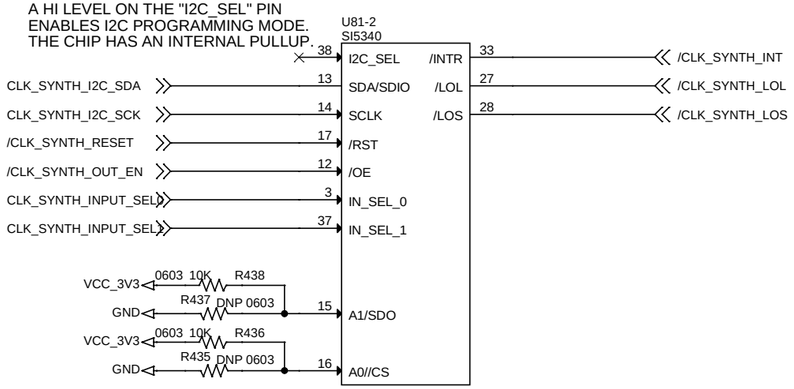
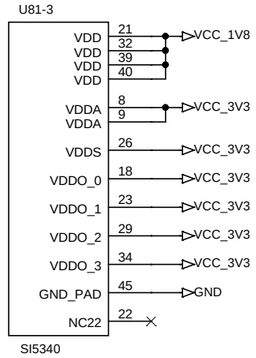
A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

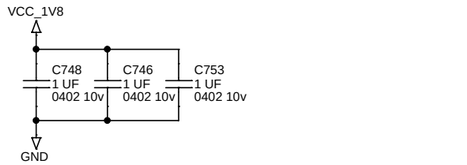


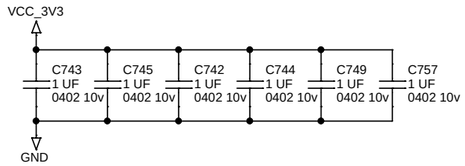
SI5340 I2C ADDRESS:
READ OR WRITE
1 1 1 0 1 A1 A0
RANGE: 0X74 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.







ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.07: LHC CLOCKING SUPPORT		
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THIS CIRCUIT ON THIS PAGE IS FOR USE IN THE PROTOTYPE ONLY. IT ALLOWS US TO FEED LEGACY TTC SIGNALS INTO THE SYSTEM.

U13-2
SFP_CONN_WITH_CAGE

U13-1
SFP_CONN_WITH_CAGE

THE SFP I2C SIGNALS AND CONTROL LINES ARE WIRED TO THE CHIPS THAT SUPPORT ACCESS TO THE KU15P OPTICS. THEY CAN BE CONNECTED ELSEWHERE IF DESIRED.

SFP+ CONNECTOR TO RECEIVE ENCODED TTC CLOCK/DATA STREAM.

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTS_OUT" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS WILL GENERATE THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

J11
JUMPER_DIFF

THESE RESISTORS MUST BE NEAR THE 65LVDS100 INPUT PINS.

VCC_2V5
R12 49.9 0402
R18 49.9 0402

U12
NB7V52M

U8
65LVDS100

DC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J10
JUMPER_DIFF

THIS JUMPER ALLOWS DIRECT CONNECTION OF "CDR_DATA" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

THIS BUFFER CONVERTS 2.5V CML SIGNALS TO LVDS LEVELS THAT ARE COMPATABLE WITH ULTRASCALE "HP" BANK INPUTS.

C964 0.1 UF 0402
C970 0.1 UF 0402

R13 1K 0402
R20 1K 0402
R19 1K 0402

U14
ADN2814

C14 0.47 UF 0402 10V

C9 0.1 UF 0402
C918 1 NF 0402
C882 1 NF 0402
C917 1 NF 0402
C956 1 NF 0402
C959 1 NF 0402

PLACE ONE OF EACH VALUE NEAR PINS 2, 12, 18, 24, AND 31.

THE CLOCK POLARITY IS INVERTED.

U11
SY89832U

C967 0.1 UF 0402
C919 0.1 UF 0402
C881 0.1 UF 0402
C883 0.1 UF 0402
C955 0.1 UF 0402
C961 0.1 UF 0402

THIS DIVIDER NETWORK PROVIDES A DIFFERENTIAL VOLTAGE OF 0.83 VOLTS. IT HOLDS THE RESET INPUT AT A "FALSE" VALUE.

U10
SY89872

S1=0, S0=1 -> B=INPUT/4

C965 0.1 UF 0402
C966 0.1 UF 0402

AC COUPLED LVDS

C3 0.1 UF 0402
C4 0.1 UF 0402
AC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J9
JUMPER_DIFF

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTC_CLK40" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS CLOCK, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

THIS DESIGN ONLY USES 2,5 VOLTS FOR LEGACY TTC SUPPORT. IT DOES NOT NEED A DC-DC CONVERTER SUPPLY.

U19
LT1963A

C12 0.1 UF 0402
C10 10 UF 16V 0805
C11 22 UF 6.3V 0805
C13 0.1 UF 0402

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.08: LEGACY TTC		
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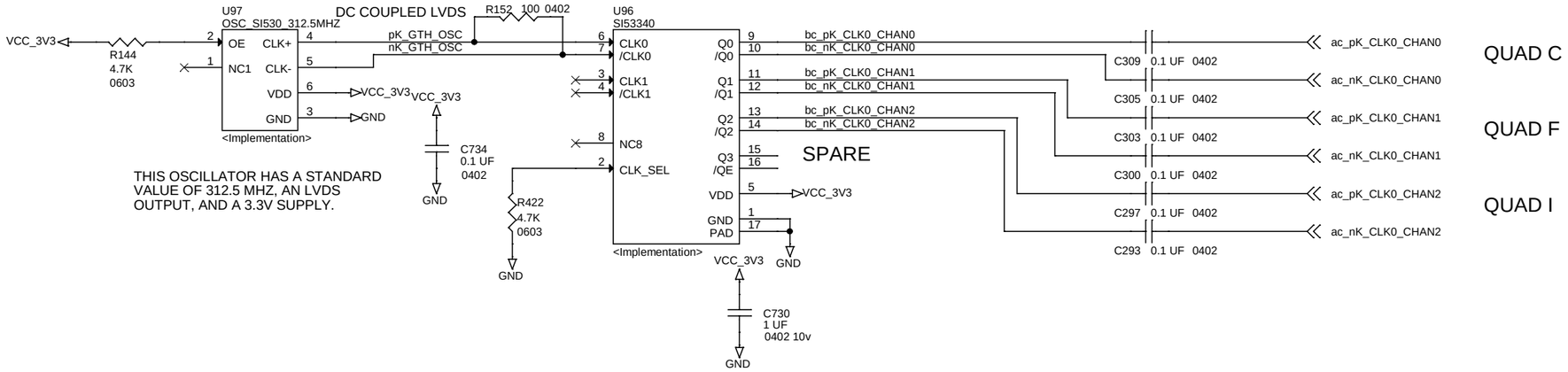
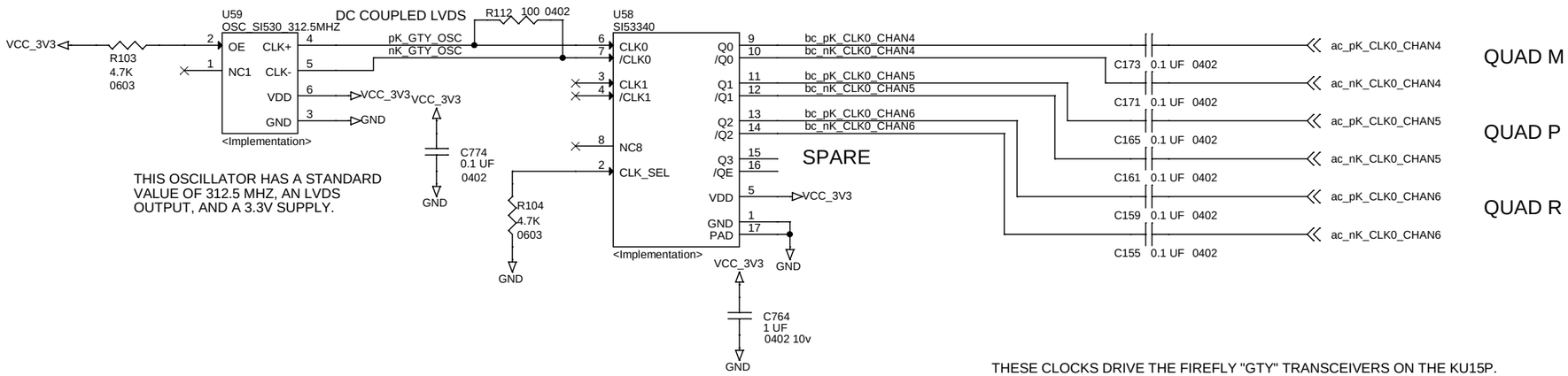
AC COUPLED LVDS

bc = BEFORE CAPACITOR

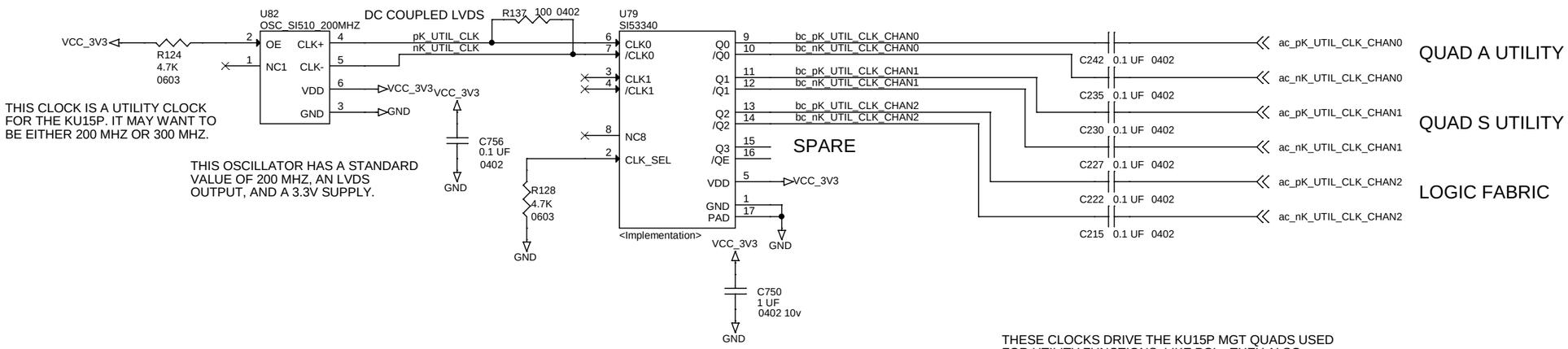
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.



THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.



THESE CLOCKS DRIVE THE KU15P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.09: KU15P OSCILLATOR CLOCKING

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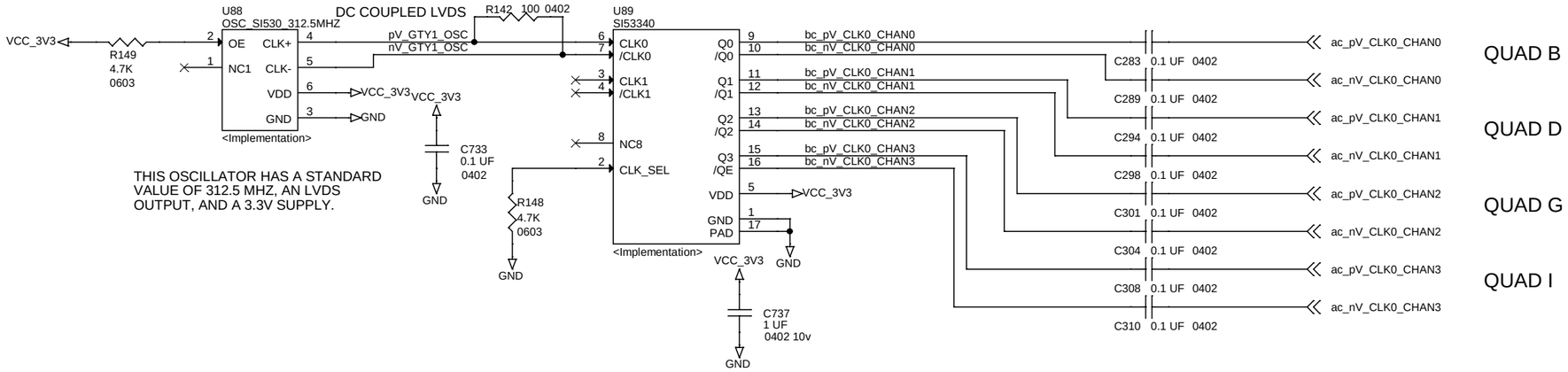
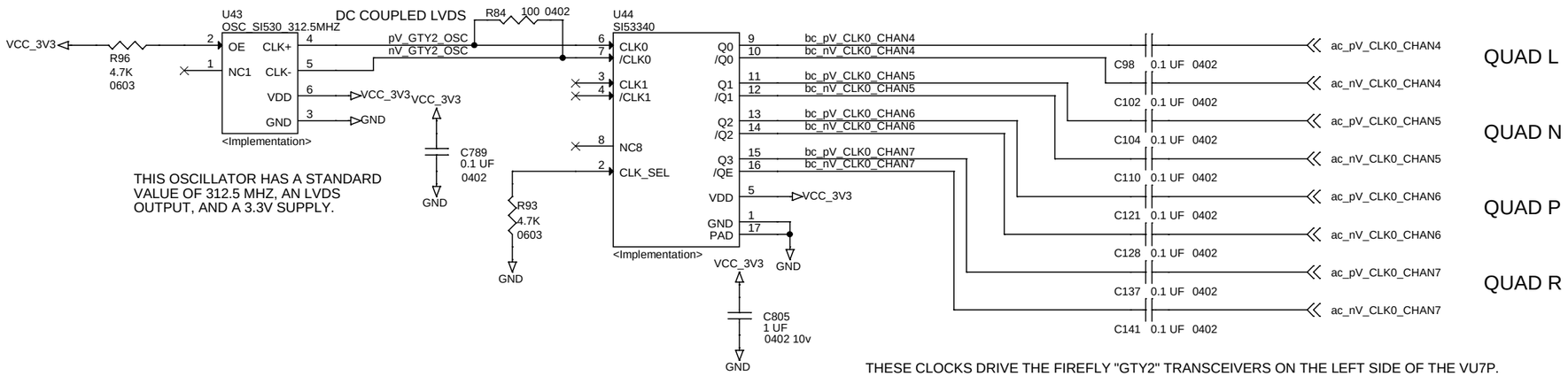
AC COUPLED LVDS

bc = BEFORE CAPACITOR

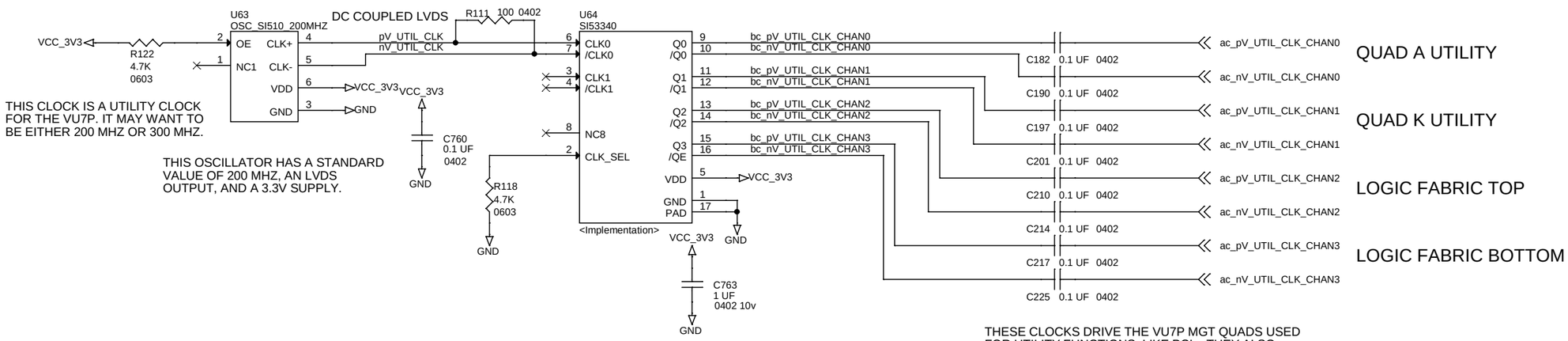
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.



THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.



THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.



THESE CLOCKS DRIVE THE VU7P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title

2.10: VU7P OSCILLATOR CLOCKING

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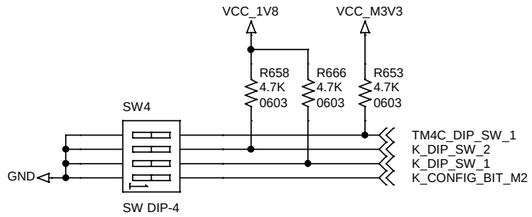
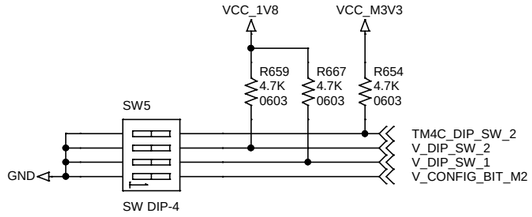
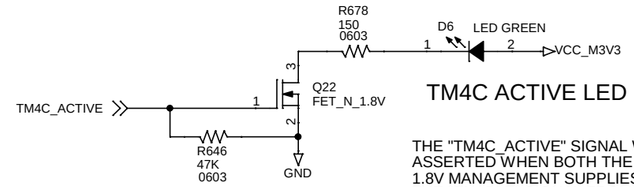
ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.11: BETWEEN FPGA CONNECTIONS		
Size	Document Number: 6089-103	Rev: A
Date: Monday, February 11, 2019	Sheet 17 of 75	



KU15P DIP SWITCH

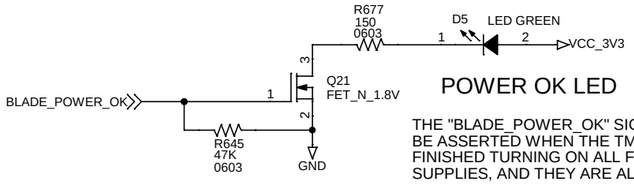


VU7P DIP SWITCH



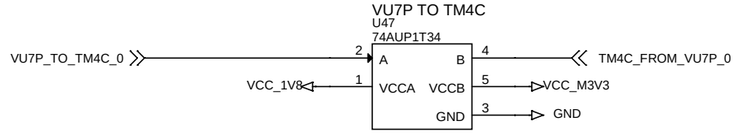
TM4C ACTIVE LED

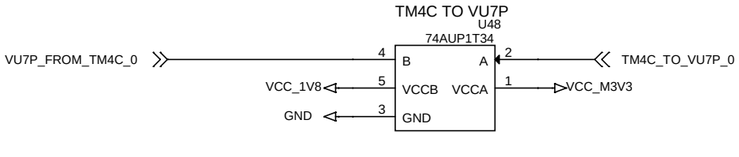
THE "TM4C_ACTIVE" SIGNAL WILL BE ASSERTED WHEN BOTH THE 3.3V AND 1.8V MANAGEMENT SUPPLIES ARE GOOD, THE "ENABLE" SIGNAL FROM THE SERVICE BLADE IS HIGH, AND THE "RESET" SWITCH IS NOT ACTIVATED.



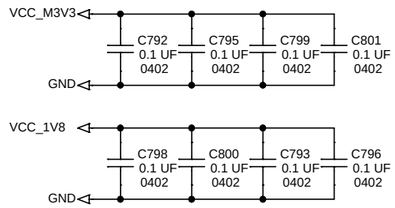
POWER OK LED

THE "BLADE_POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE TM4C HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

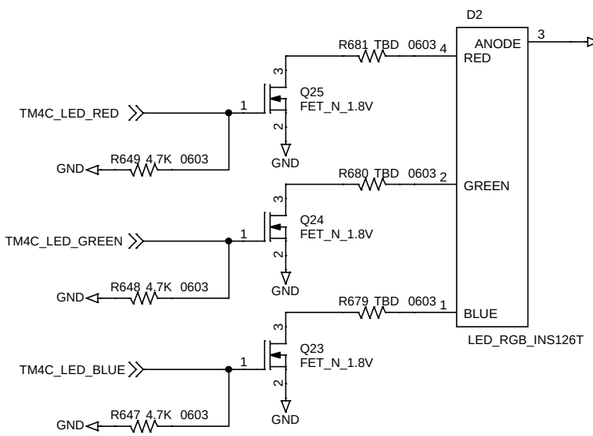




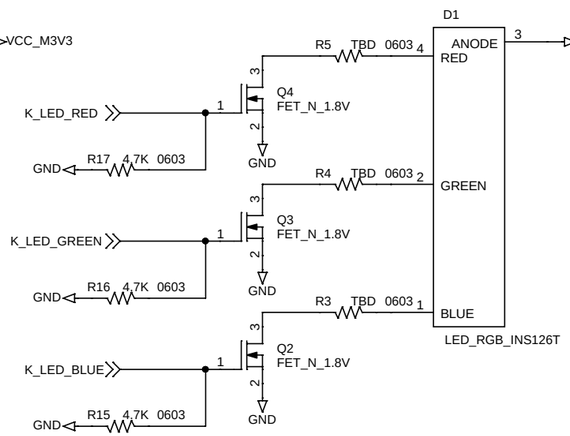
UTILITY CONNECTIONS BETWEEN THE TM4C CONTROLLER AND THE FPGAS. THE LEVEL TRANSLATORS ARE UNI-DIRECTIONAL.



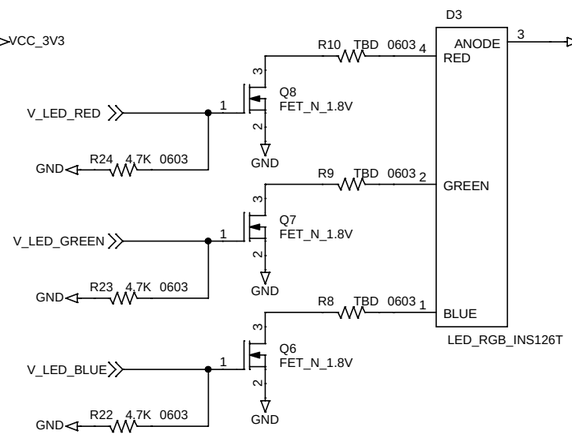
TM4C CONTROLLER LED



KU15P LED



VU7P LED



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 2.12: LEDS, SWITCHES, LEVEL SHIFTERS		
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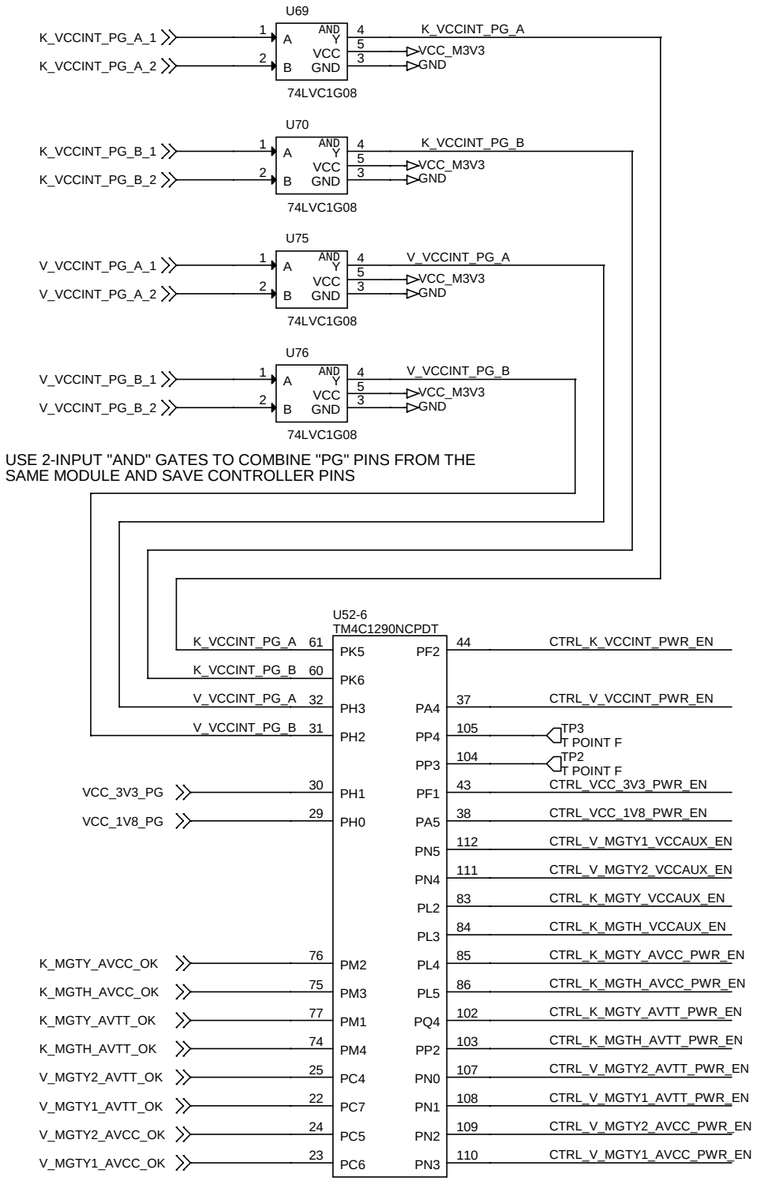
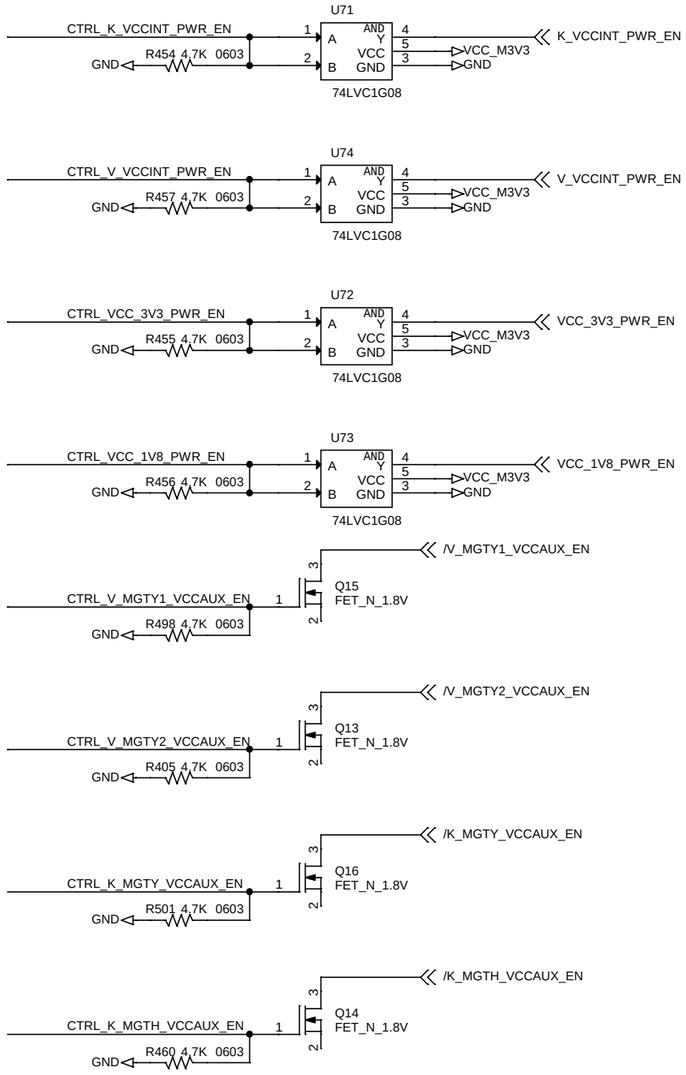
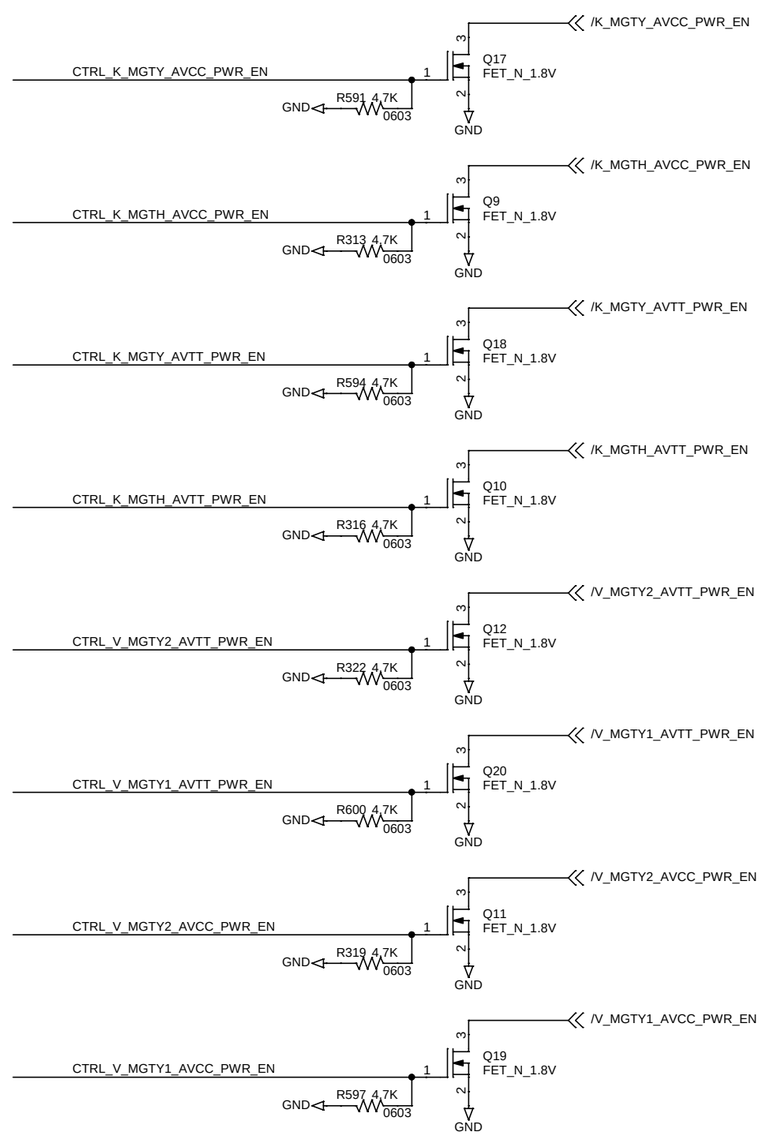


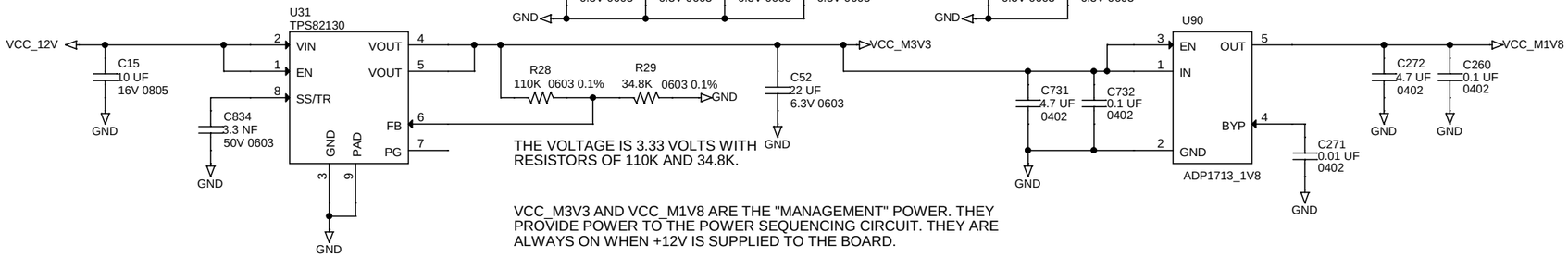




THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN VCC_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. A VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

SPREAD THESE CAPACITORS AROUND THE BOARD



VCC_M3V3 AND VCC_M1V8 ARE THE "MANAGEMENT" POWER. THEY PROVIDE POWER TO THE POWER SEQUENCING CIRCUIT. THEY ARE ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 3.01: POWER CONTROL		
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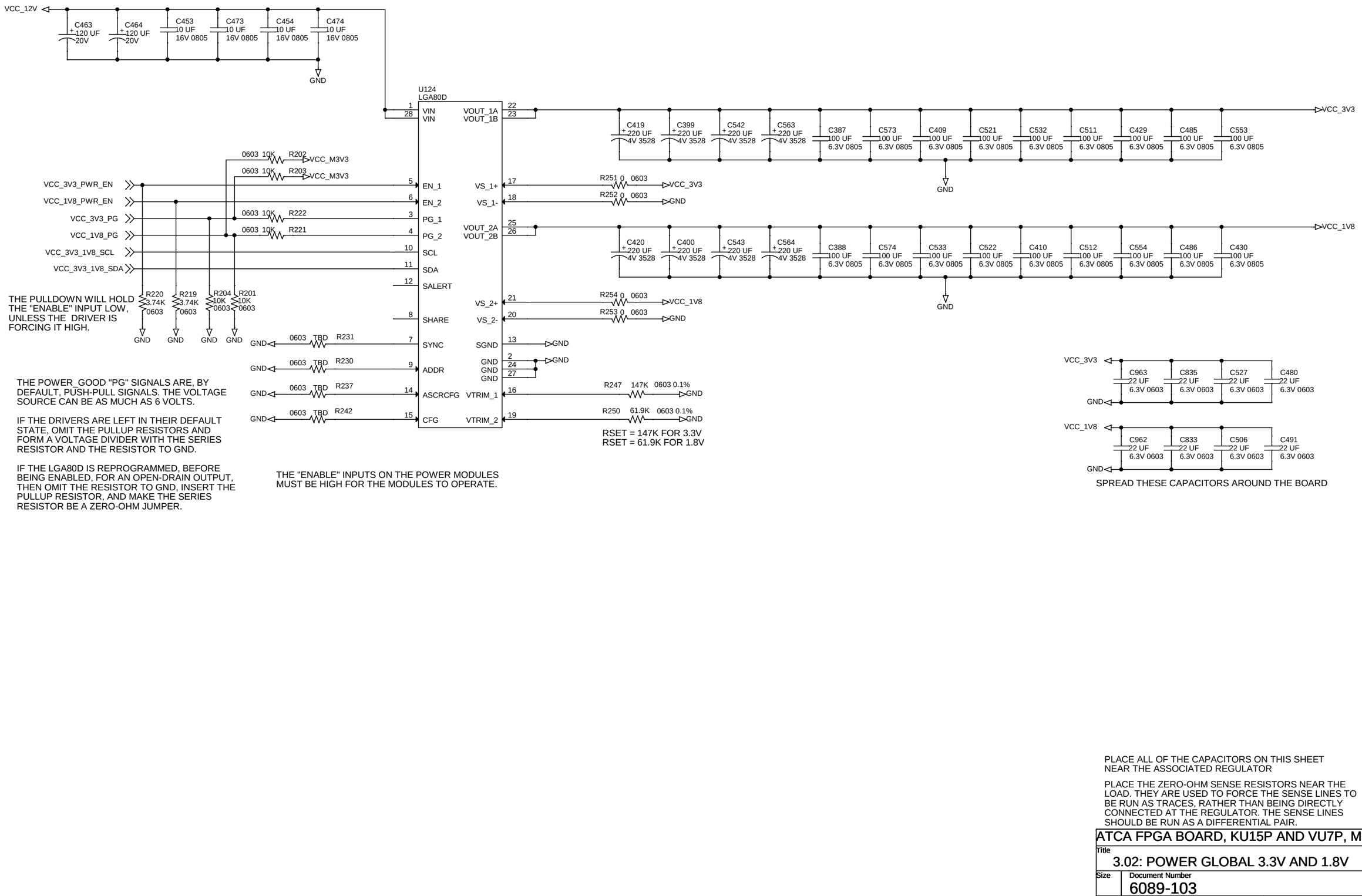

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.02: POWER GLOBAL 3.3V AND 1.8V

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KU15P VCCINT MUST BE 0.85V.

VCC_12V

C459 120 UF 20V, C460 120 UF 20V, C449 10 UF 16V 0805, C469 10 UF 16V 0805, C450 10 UF 16V 0805, C470 10 UF 16V 0805

GND

U122
LGA80D

A

VIN (1, 28)
VOUT_1A (22)
VOUT_1B (23)
EN_1 (5)
EN_2 (6)
PG_1 (3)
PG_2 (4)
SCL (10)
SDA (11)
SALERT (12)
VS_1+ (17)
VS_1- (18)
VOUT_2A (25)
VOUT_2B (26)
VS_2+ (21)
VS_2- (20)
SHARE (8)
SYNC (7)
SGND (13)
GND (2, 24, 27)
ADDR (9)
ASCRCFG (14)
VTRIM_1 (16)
CFG (15)
VTRIM_2 (19)

0603 10K R194 VCC_M3V3
0603 10K R195 VCC_M3V3
0603 10K R216
0603 10K R215

K_VCCINT_PG_A_1
K_VCCINT_PG_A_2
K_VCCINT_A_SCL
K_VCCINT_A_SDA

R196 10K 0603, R193 10K 0603

GND GND

K_VCCINT_PWR_EN

R213 3.74K 0603

GND

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

0603 TBD R227
0603 TBD R235
0603 TBD R240

R191 0 0603 K_VCCINT
R192 0 0603 GND

R245 16.2K 0603 0.1% GND

RSET = 16.2K FOR 0.85V

C415 330 UF 2.5V 3528, C393 330 UF 2.5V 3528, C538 330 UF 2.5V 3528, C559 330 UF 2.5V 3528, C425 100 UF 4V 0805, C405 100 UF 4V 0805, C528 100 UF 4V 0805, C550 100 UF 4V 0805, C383 100 UF 4V 0805, C569 100 UF 4V 0805, C481 100 UF 4V 0805, C507 100 UF 4V 0805, C517 100 UF 4V 0805

GND

C416 330 UF 2.5V 3528, C394 330 UF 2.5V 3528, C539 330 UF 2.5V 3528, C560 330 UF 2.5V 3528, C426 100 UF 4V 0805, C406 100 UF 4V 0805, C529 100 UF 4V 0805, C551 100 UF 4V 0805, C384 100 UF 4V 0805, C570 100 UF 4V 0805, C482 100 UF 4V 0805, C508 100 UF 4V 0805, C518 100 UF 4V 0805

GND

K_VCCINT

C461 120 UF 20V, C462 120 UF 20V, C451 10 UF 16V 0805, C471 10 UF 16V 0805, C452 10 UF 16V 0805, C472 10 UF 16V 0805

GND

U123
LGA80D

B

VIN (1, 28)
VOUT_1A (22)
VOUT_1B (23)
EN_1 (5)
EN_2 (6)
PG_1 (3)
PG_2 (4)
SCL (10)
SDA (11)
SALERT (12)
VS_1+ (17)
VS_1- (18)
VOUT_2A (25)
VOUT_2B (26)
VS_2+ (21)
VS_2- (20)
SHARE (8)
SYNC (7)
SGND (13)
GND (2, 24, 27)
ADDR (9)
ASCRCFG (14)
VTRIM_1 (16)
CFG (15)
VTRIM_2 (19)

0603 10K R198 VCC_M3V3
0603 10K R199 VCC_M3V3
0603 10K R218
0603 10K R217

K_VCCINT_PG_B_1
K_VCCINT_PG_B_2
K_VCCINT_B_SCL
K_VCCINT_B_SDA

R200 10K 0603, R197 10K 0603

GND GND

0603 TBD R229
0603 TBD R228
0603 TBD R236
0603 TBD R241

R246 16.2K 0603 0.1% GND

RSET = 16.2K FOR 0.85V

C417 330 UF 2.5V 3528, C396 330 UF 2.5V 3528, C540 330 UF 2.5V 3528, C561 330 UF 2.5V 3528, C427 100 UF 4V 0805, C407 100 UF 4V 0805, C530 100 UF 4V 0805, C552 100 UF 4V 0805, C385 100 UF 4V 0805, C571 100 UF 4V 0805, C519 100 UF 4V 0805, C509 100 UF 4V 0805, C483 100 UF 4V 0805

GND

C418 330 UF 2.5V 3528, C397 330 UF 2.5V 3528, C541 330 UF 2.5V 3528, C562 330 UF 2.5V 3528, C428 100 UF 4V 0805, C408 100 UF 4V 0805, C531 100 UF 4V 0805, C549 100 UF 4V 0805, C386 100 UF 4V 0805, C572 100 UF 4V 0805, C520 100 UF 4V 0805, C510 100 UF 4V 0805, C484 100 UF 4V 0805

GND

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 3.03: POWER SOURCE KU15P INTERNAL		
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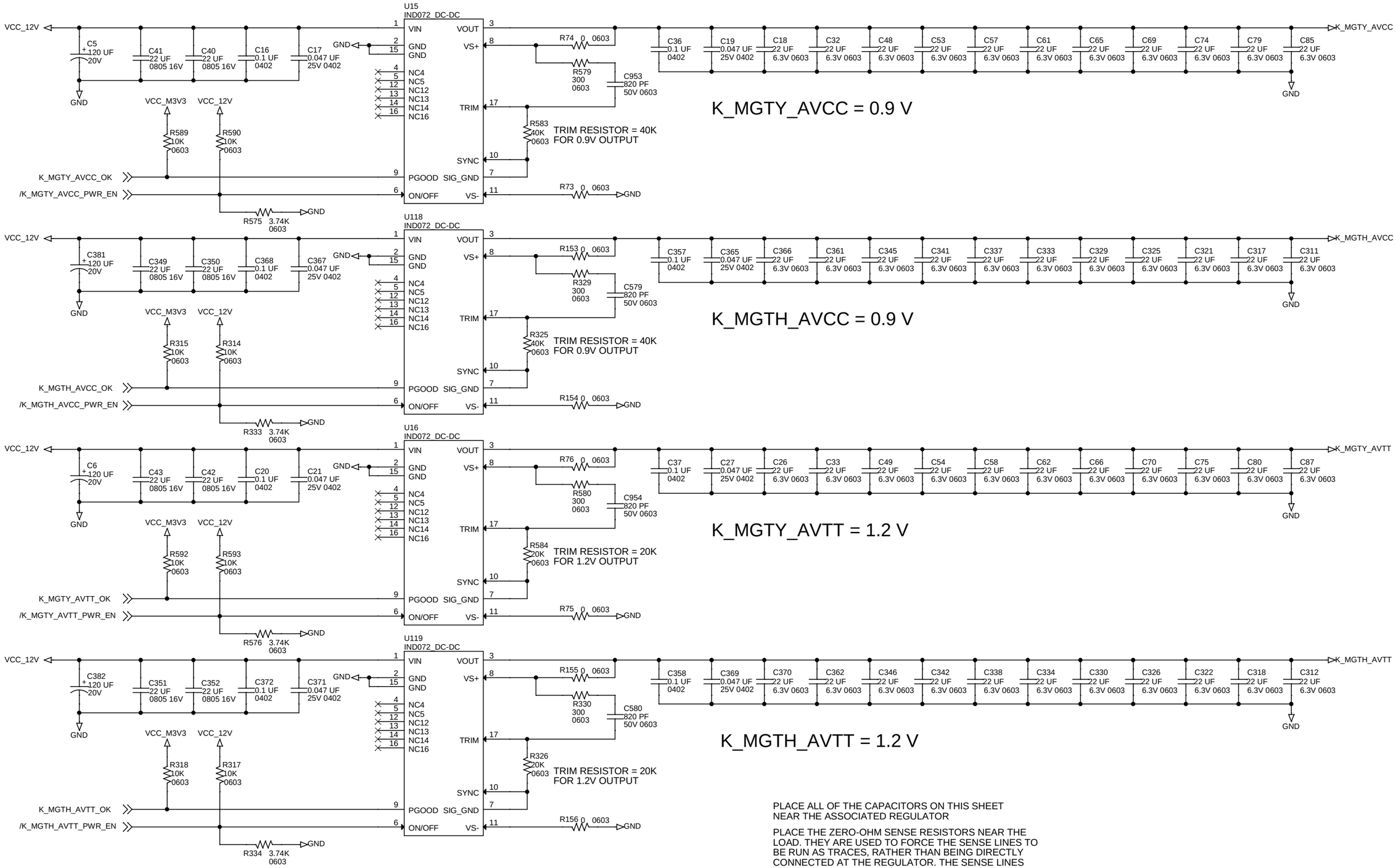

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.04: POWER SOURCE KU15P MGT XCVR

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VU7P VCCINT MUST BE 0.85V.

U125
LGA80D

VCC_12V

C465 120 UF 20V
C466 120 UF 20V
C455 10 UF 16V 0805
C475 10 UF 16V 0805
C456 10 UF 16V 0805
C476 10 UF 16V 0805
GND

1 VIN
28 VIN
A
22 VOUT_1A
23 VOUT_1B

V_VCCINT

C421 330 UF 2.5V 3528
C401 330 UF 2.5V 3528
C544 330 UF 2.5V 3528
C565 330 UF 2.5V 3528
C431 100 UF 6.3V 0805
C411 100 UF 6.3V 0805
C534 100 UF 6.3V 0805
C555 100 UF 6.3V 0805
C389 100 UF 6.3V 0805
C575 100 UF 6.3V 0805
C523 100 UF 6.3V 0805
C513 100 UF 6.3V 0805
C487 100 UF 6.3V 0805
GND

5 EN_1 — 0603 10K R206 VCC_M3V3
6 EN_2 — 0603 10K R207 VCC_M3V3
3 PG_1 — 0603 10K R224 V_VCCINT_PG_A_1
4 PG_2 — 0603 10K R223 V_VCCINT_PG_A_2
10 SCL — V_VCCINT_A_SCL
11 SDA — V_VCCINT_A_SDA
12 SALERT — R208 10K 0603 GND; R205 10K 0603 GND
8 SHARE
7 SYNC — V_VCCINT_PWR_EN; R214 3.74K 0603 GND
9 ADDR — GND 0603 TBD R232
14 ASCRCFG — GND 0603 TBD R238
15 CFG — GND 0603 TBD R243

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

17 VS_1+ — R256 0 0603 V_VCCINT
18 VS_1- — R255 0 0603 GND
25 VOUT_2A
26 VOUT_2B

C402 330 UF 2.5V 3528
C422 330 UF 2.5V 3528
C566 330 UF 2.5V 3528
C545 330 UF 2.5V 3528
C432 100 UF 6.3V 0805
C412 100 UF 6.3V 0805
C535 100 UF 6.3V 0805
C556 100 UF 6.3V 0805
C390 100 UF 6.3V 0805
C576 100 UF 6.3V 0805
C524 100 UF 6.3V 0805
C514 100 UF 6.3V 0805
C488 100 UF 6.3V 0805
GND

21 VS_2+
20 VS_2-
13 SGND — GND
2 GND
24 GND
27 GND — GND
16 VTRIM_1 — R248 16.2K 0603 0.1% GND
19 VTRIM_2

RSET = 16.2K FOR 0.85V

U126
LGA80D

C467 120 UF 20V
C468 120 UF 20V
C457 10 UF 16V 0805
C477 10 UF 16V 0805
C458 10 UF 16V 0805
C478 10 UF 16V 0805
GND

1 VIN
28 VIN
B
22 VOUT_1A
23 VOUT_1B

C423 330 UF 2.5V 3528
C403 330 UF 2.5V 3528
C546 330 UF 2.5V 3528
C567 330 UF 2.5V 3528
C433 100 UF 6.3V 0805
C413 100 UF 6.3V 0805
C536 100 UF 6.3V 0805
C557 100 UF 6.3V 0805
C391 100 UF 6.3V 0805
C577 100 UF 6.3V 0805
C525 100 UF 6.3V 0805
C515 100 UF 6.3V 0805
C489 100 UF 6.3V 0805
GND

5 EN_1 — 0603 10K R210 VCC_M3V3
6 EN_2 — 0603 10K R211 VCC_M3V3
3 PG_1 — 0603 10K R226 V_VCCINT_PG_B_1
4 PG_2 — 0603 10K R225 V_VCCINT_PG_B_2
10 SCL — V_VCCINT_B_SCL
11 SDA — V_VCCINT_B_SDA
12 SALERT — R212 10K 0603 GND; R209 10K 0603 GND
8 SHARE
7 SYNC — GND 0603 TBD R234
9 ADDR — GND 0603 TBD R233
14 ASCRCFG — GND 0603 TBD R239
15 CFG — GND 0603 TBD R244

17 VS_1+
18 VS_1-
25 VOUT_2A
26 VOUT_2B

C424 330 UF 2.5V 3528
C404 330 UF 2.5V 3528
C568 330 UF 2.5V 3528
C547 330 UF 2.5V 3528
C434 100 UF 6.3V 0805
C414 100 UF 6.3V 0805
C537 100 UF 6.3V 0805
C558 100 UF 6.3V 0805
C392 100 UF 6.3V 0805
C578 100 UF 6.3V 0805
C490 100 UF 6.3V 0805
C516 100 UF 6.3V 0805
C526 100 UF 6.3V 0805
GND

21 VS_2+
20 VS_2-
13 SGND — GND
2 GND
24 GND
27 GND — GND
16 VTRIM_1 — R249 16.2K 0603 0.1% GND
19 VTRIM_2

RSET = 16.2K FOR 0.85V

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.05: POWER SOURCE VU7P INTERNAL

Size	Document Number	Rev
	6089-103	A

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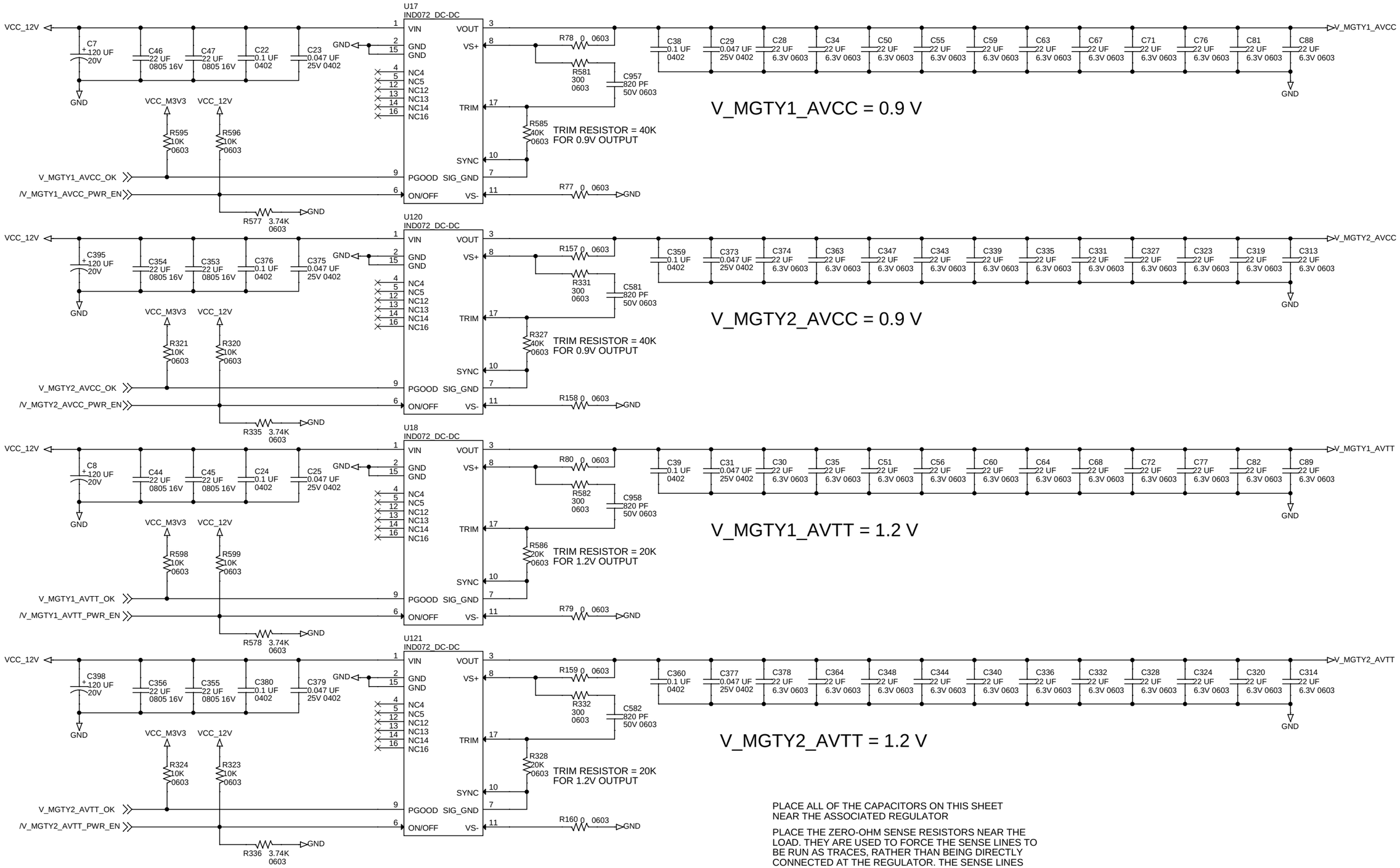

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 3.06: POWER SOURCE VU7P MGT XCVR		
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THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

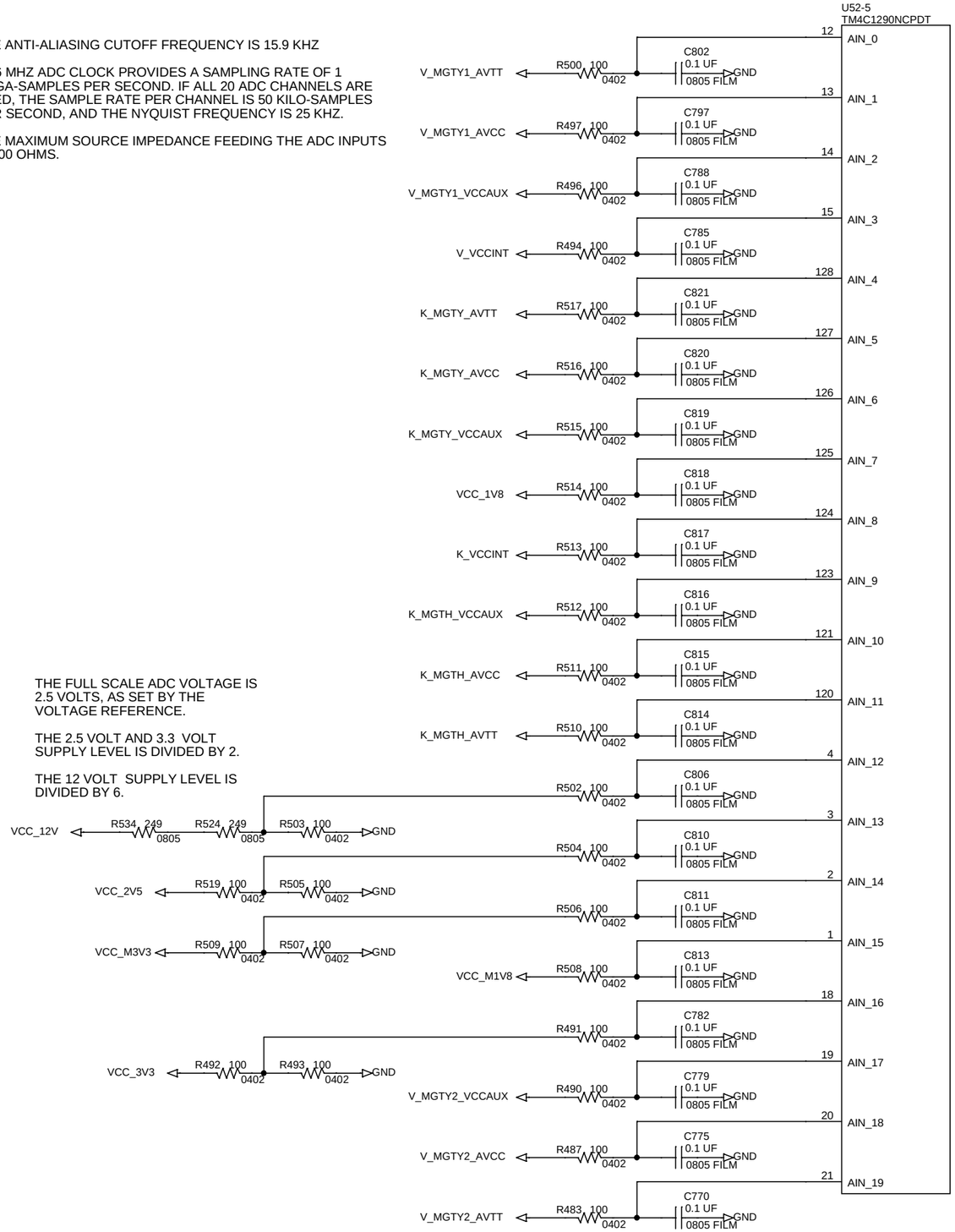
A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

THE FULL SCALE ADC VOLTAGE IS 2.5 VOLTS, AS SET BY THE VOLTAGE REFERENCE.

THE 2.5 VOLT AND 3.3 VOLT SUPPLY LEVEL IS DIVIDED BY 2.

THE 12 VOLT SUPPLY LEVEL IS DIVIDED BY 6.



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.07: POWER MEASUREMENT

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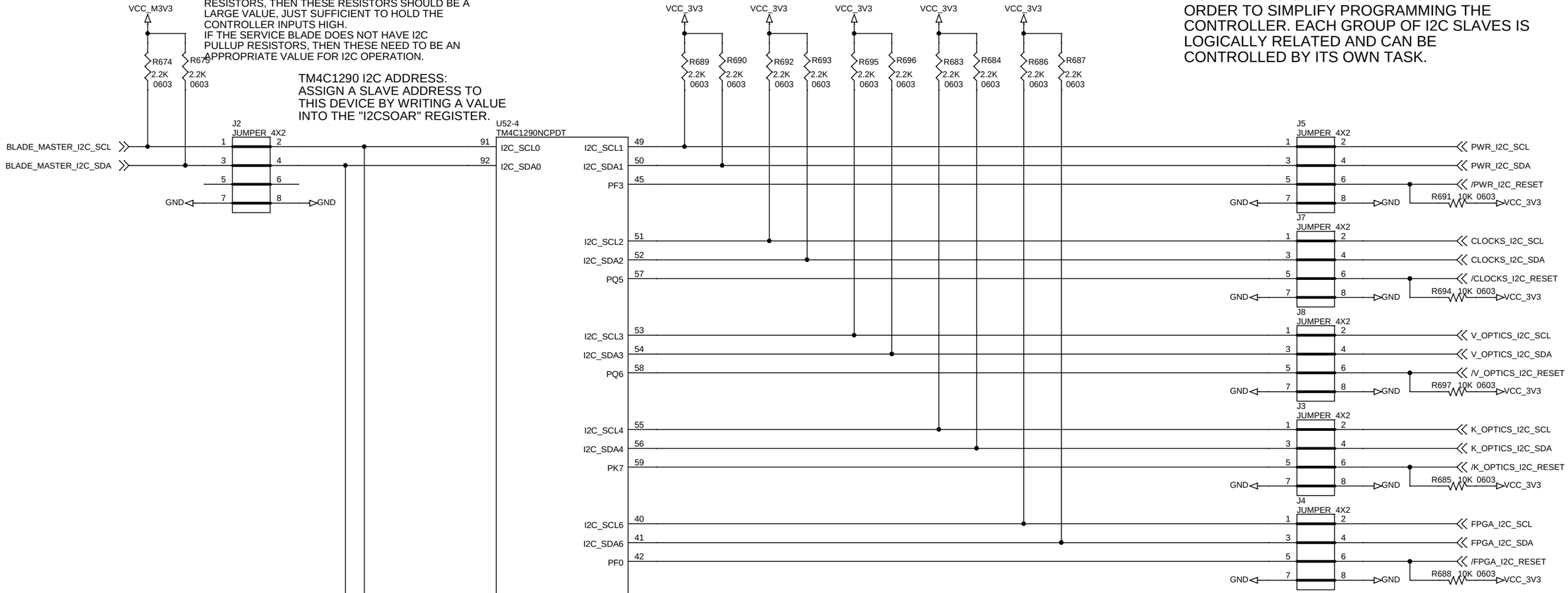
IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH.
IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

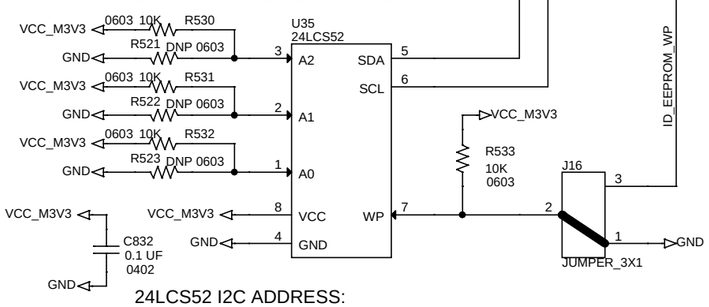
TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.



I2C MODULE 7 IN UNCOMMITTED. THE PINS CAN BE REPURPOSED IF NEEDED. I2C MODULE 8 ON PINS 35 AND 36 HAS BEEN REPURPOSED AS UART MODULE 4.

THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.



24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

THIS JUMPER CONFIGURES THE HARDWARE WRITE-PROTECT PIN.

IF NO JUMPER IS IN PLACE, THE HARDWARE WRITE PROTECTION IS ALWAYS ENABLED.

IF THE JUMPER CONNECTS PINS 1 AND 2, THE HARDWARE WRITE PROTECTION IS ALWAYS DISABLED.

IF THE JUMPER CONNECTS PINS 2 AND 3, THE HARDWARE PROTECTION IS CONTROLLED BY A GPIO PIN ON THE CONTROLLER.

REFER TO THE DATA SHEET FOR DETAILS ABOUT CONNECTING AN EXTERNAL HIGH VOLTAGE TO RESET THE SOFTWARE WRITE PROTECT FUSE.

HEADERS ARE PROVIDED TO SUPPORT DRIVING ANY I2C BUS WITH A STAND-ALONE USB-TO-I2C CONTROLLER.

NORMALLY, JUMPERS WILL CONNECT THE ON-BOARD "SCL", "SDA", AND "/RESET" SIGNALS STRAIGHT THROUGH THE HEADERS.

TO CONNECT THE STAND-ALONE CONTROLLER, PULL THE JUMPERS FROM THE HEADER AND CONNECT THE CONTROLLER'S SIGNALS TO PINS 2, 4, AND 6, AND CONNECT GND TO PIN 8.

CONFIGURE THE "SPI MISO" PIN ON THE AARDVARK CONTROLLER AS A "GPIO OUTPUT" TO CONTROL THE "RESET" SIGNAL.

THIS LAYOUT ASSUMES THAT THE STAND-ALONE CONTROLLER PROVIDES PULL-UP RESISTORS ON THE I2C SIGNALS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.01: I2C CONTROLLER

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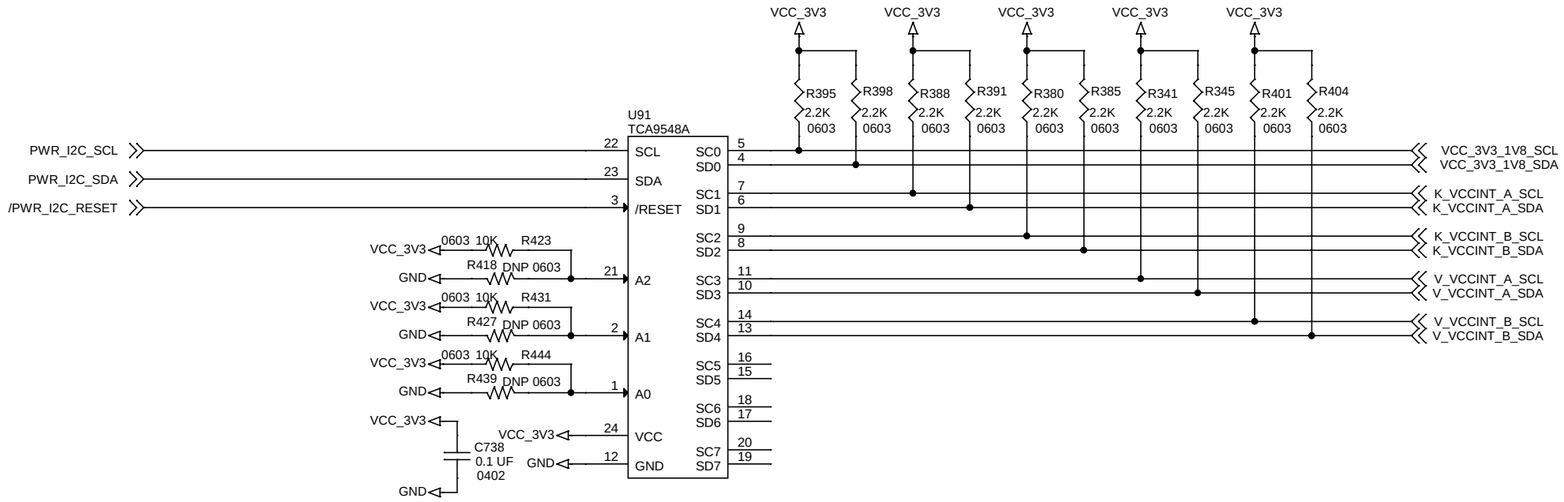


TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

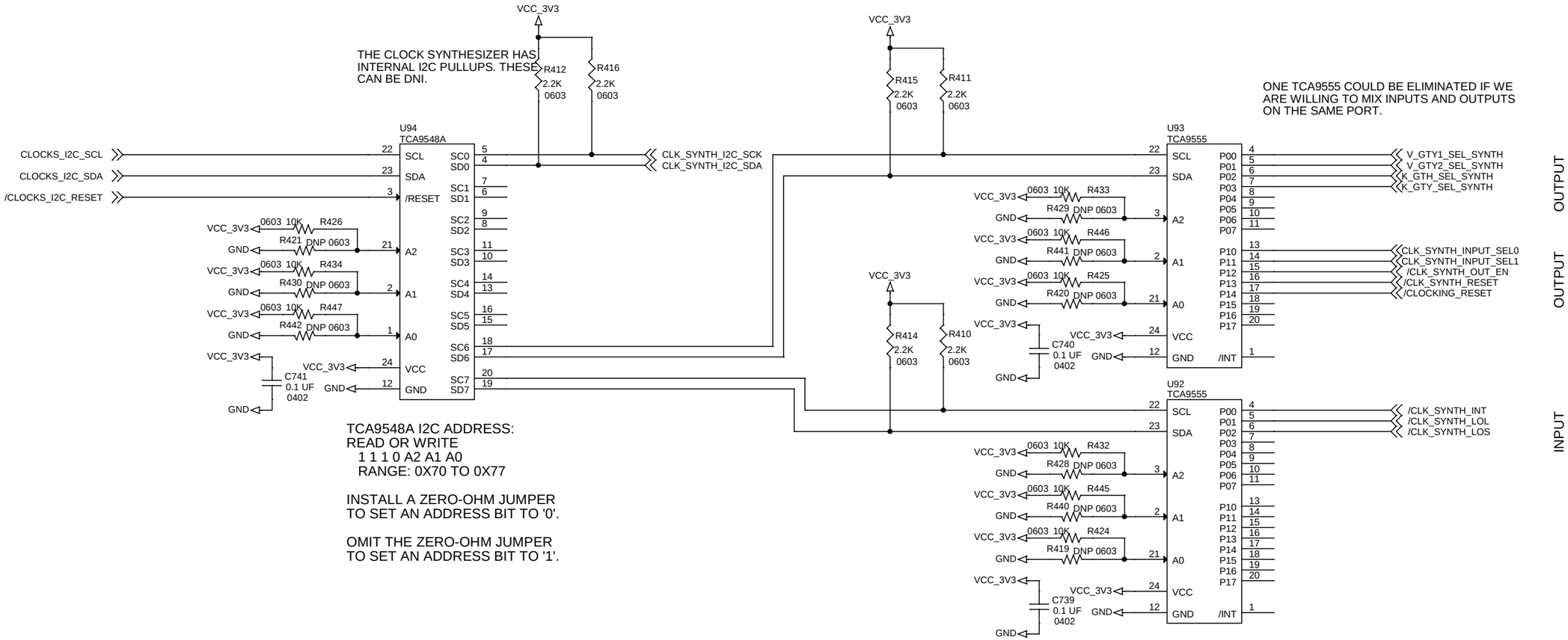
OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.02: I2C POWER CONTROL

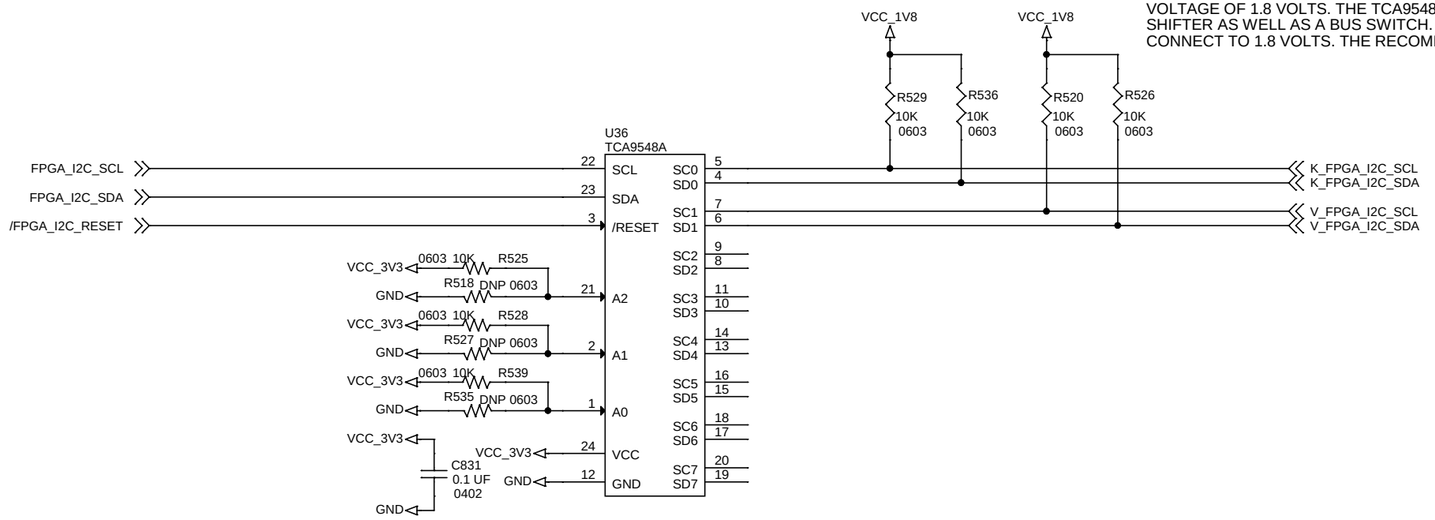
Size | Document Number: 6089-103 | Rev: A

Date: Sunday, February 17, 2019 Sheet 27 of 75



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.03: I2C CLOCK SOURCE CONTROL		
Size	Document Number: 6089-103	Rev: A
Date: Sunday, February 17, 2019	Sheet 28 of 75	

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.



TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

A2	A1	A0	I2C BUS SLAVE ADDRESS
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.04: I2C FPGA SYSMON

Size | Document Number: 6089-103 | Rev: A

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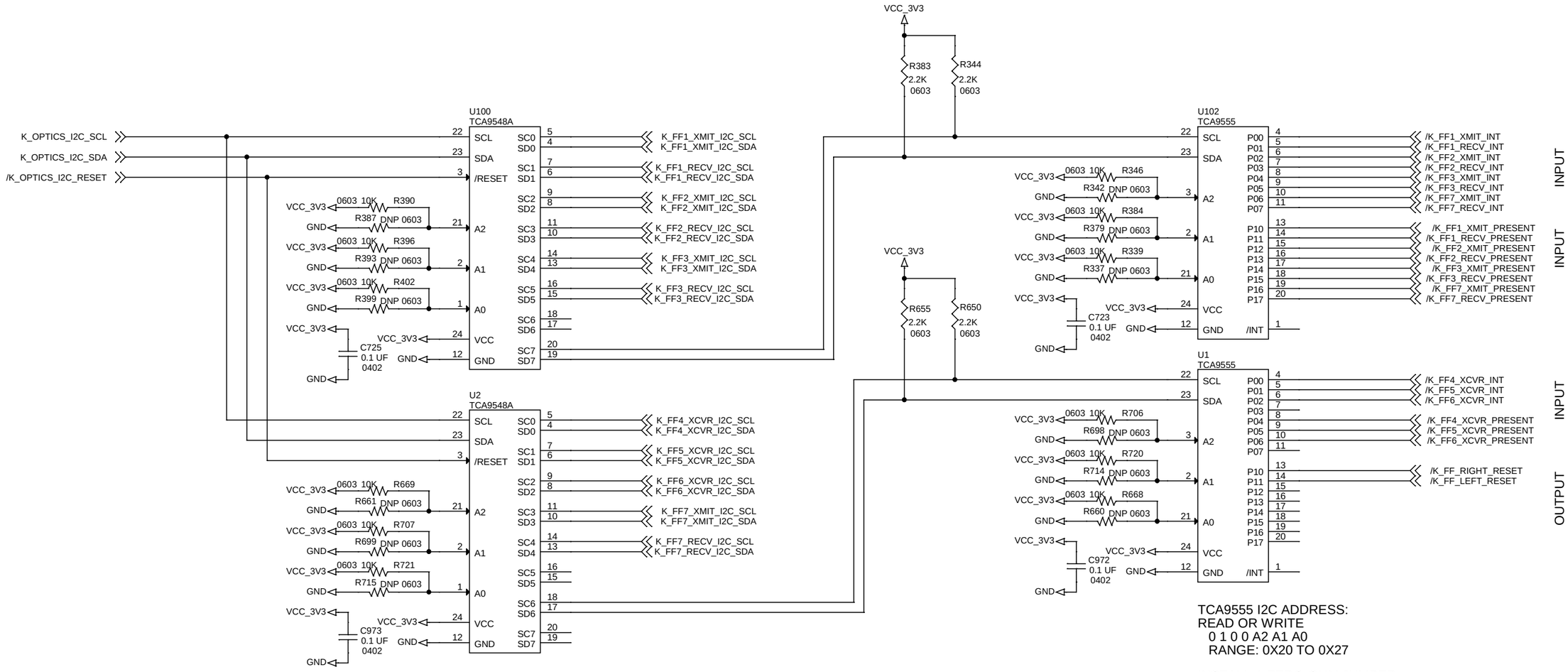


TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

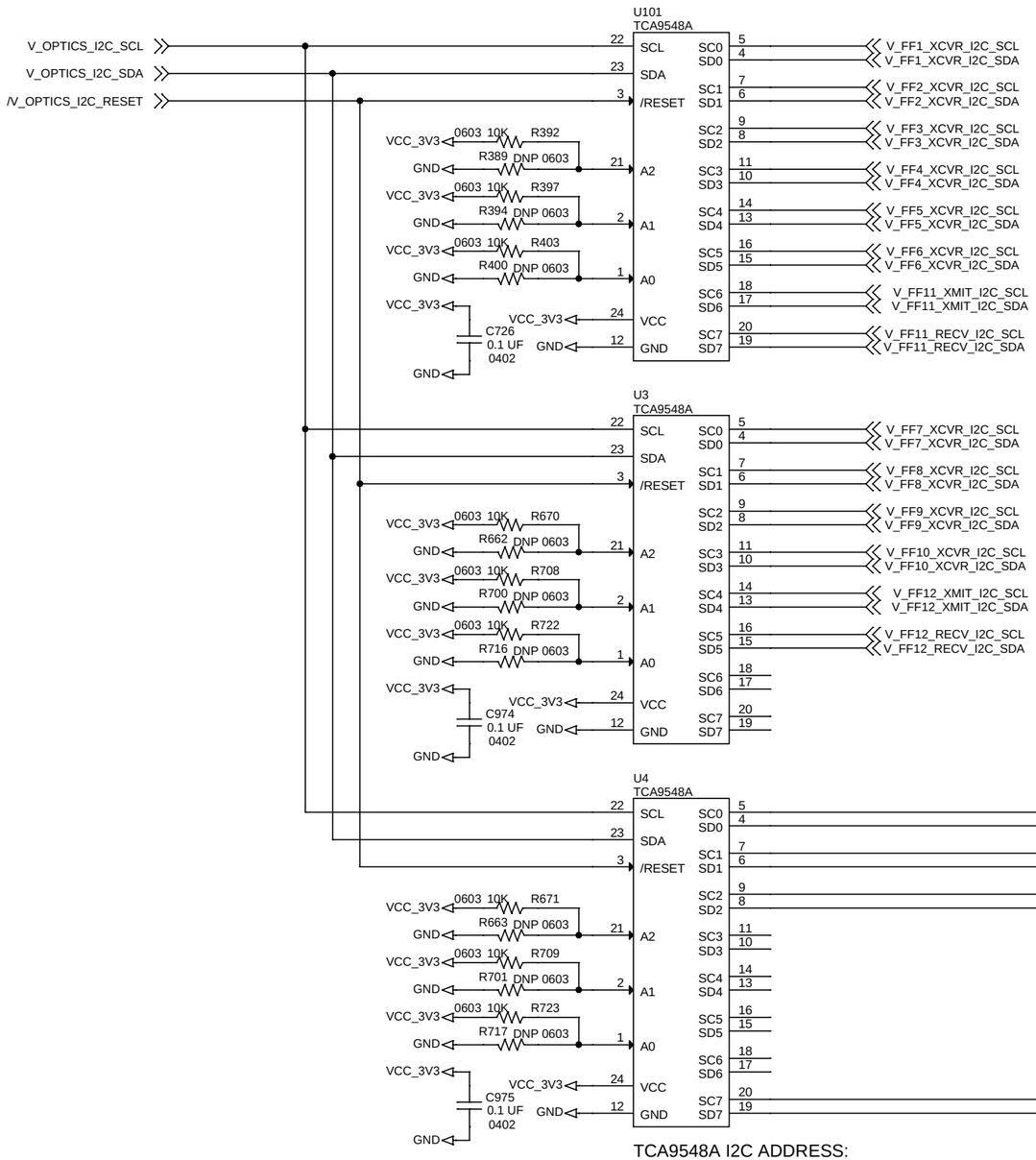
OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

TCA9555 I2C ADDRESS:
READ OR WRITE
0 1 0 0 A2 A1 A0
RANGE: 0X20 TO 0X27

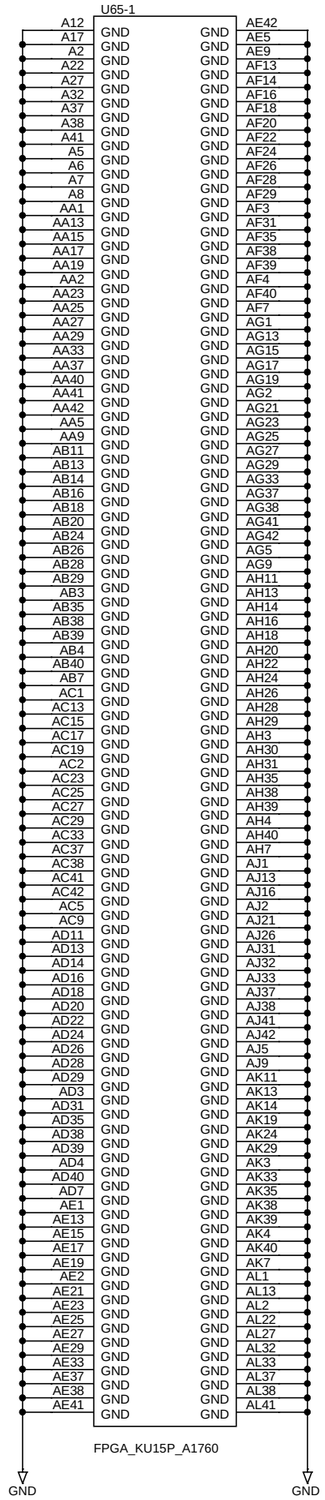
INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

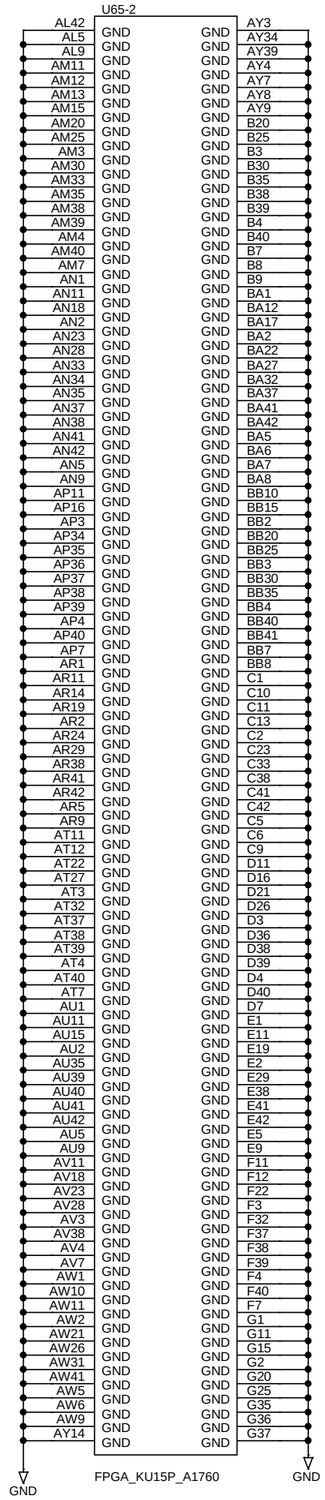
OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.
RANGE: 0X30 TO 0X37

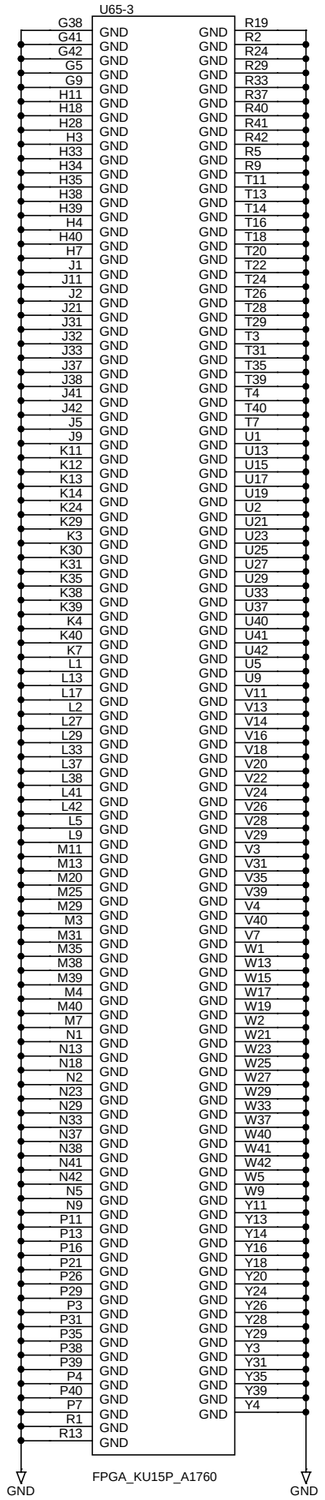
ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 4.05: I2C KU15P OPTICS		
Size	Document Number: 6089-103	Rev: A
Date: Sunday, February 17, 2019	Sheet 30 of 75	

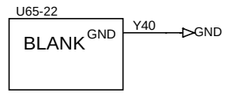


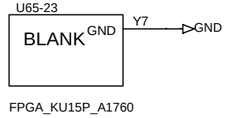
ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 4.06: I2C VU7P OPTICS			
Size	Document Number: 6089-103		Rev: A
Date: Sunday, February 17, 2019	Sheet 31 of 75		











ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 5.01: KU15P FPGA GND			
Size	Document Number: 6089-103		Rev: A
Date: Thursday, February 14, 2019	Sheet 32 of 75		

U65-4
FPGA_KU15P_A1760

K_VCCINT

VCCINT MUST BE 0.85V.

VCCINT: AA16, AA18, AA20, AA24, AA26, AB17, AB19, AB23, AB25, AC16, AC18, AC20, AC24, AC26, AD17, AD19, AD21, AD23, AD25, AE16, AE18, AE20, AE22, AE24, AE26, AF17, AF19, AF21, AF23, AF25, AG16, AG18, AG20, AG22, AG24, AG26, AH17, AH19, AH21, AH23, AH25, T17, T19, T21, T23, T25, U16, U18, U20, U22, U24, U26, V17, V19, V21, V23, V25, W16, W18, W20, W22, W24, W26, Y17, Y19, Y23, Y25

VCCAUX: AA28, AC28, AE28, AG28, U28, W28

VCC_1V8

VCCAUX_IO: AB27, AD27, AF27, AH27, T27, V27, Y27

VCC_1V8

VCCAUX_IO MUST BE CONNECTED TO VCCAUX (1.8V).

K_VCCINT

VCCINT_IO MUST BE CONNECTED TO VCC_INT (0.85V).

VCCINT_IO: AA14, AC14, AE14, AG14, U14, W14

K_VCCINT

VCCBRAM CAN BE CONNECTED TO VCC_INT (0.85V).

VCCBRAM: Y15, V15, AB15, AD15, AF15, AH15, T15

VCC_1V8

C263 47 UF 0805 6.3V
C131 47 UF 0805 6.3V
C262 47 UF 0805 6.3V
C130 47 UF 0805 6.3V
C315 47 UF 0805 6.3V

GND

VCC_1V8

C120 4.7 UF 0402
C279 4.7 UF 0402
C276 4.7 UF 0402
C117 4.7 UF 0402

GND

VCCAUX / VCCAUXIO / VCCO
ALL I/O BANKS ARE POWERED AT 1.8 VOLTS.

K_VCCINT

C163 470 UF 2V
C223 470 UF 2V
C164 470 UF 2V
C224 470 UF 2V

GND

K_VCCINT

C153 100 UF 0805 6.3V
C239 100 UF 0805 6.3V
C198 100 UF 0805 6.3V

GND

K_VCCINT

C179 4.7 UF 0402
C187 4.7 UF 0402
C208 4.7 UF 0402
C178 4.7 UF 0402
C186 4.7 UF 0402
C207 4.7 UF 0402

GND

K_VCCINT

C199 47 UF 0805 6.3V

GND

VCCINT / VCCINT_IO / VCCBRAM

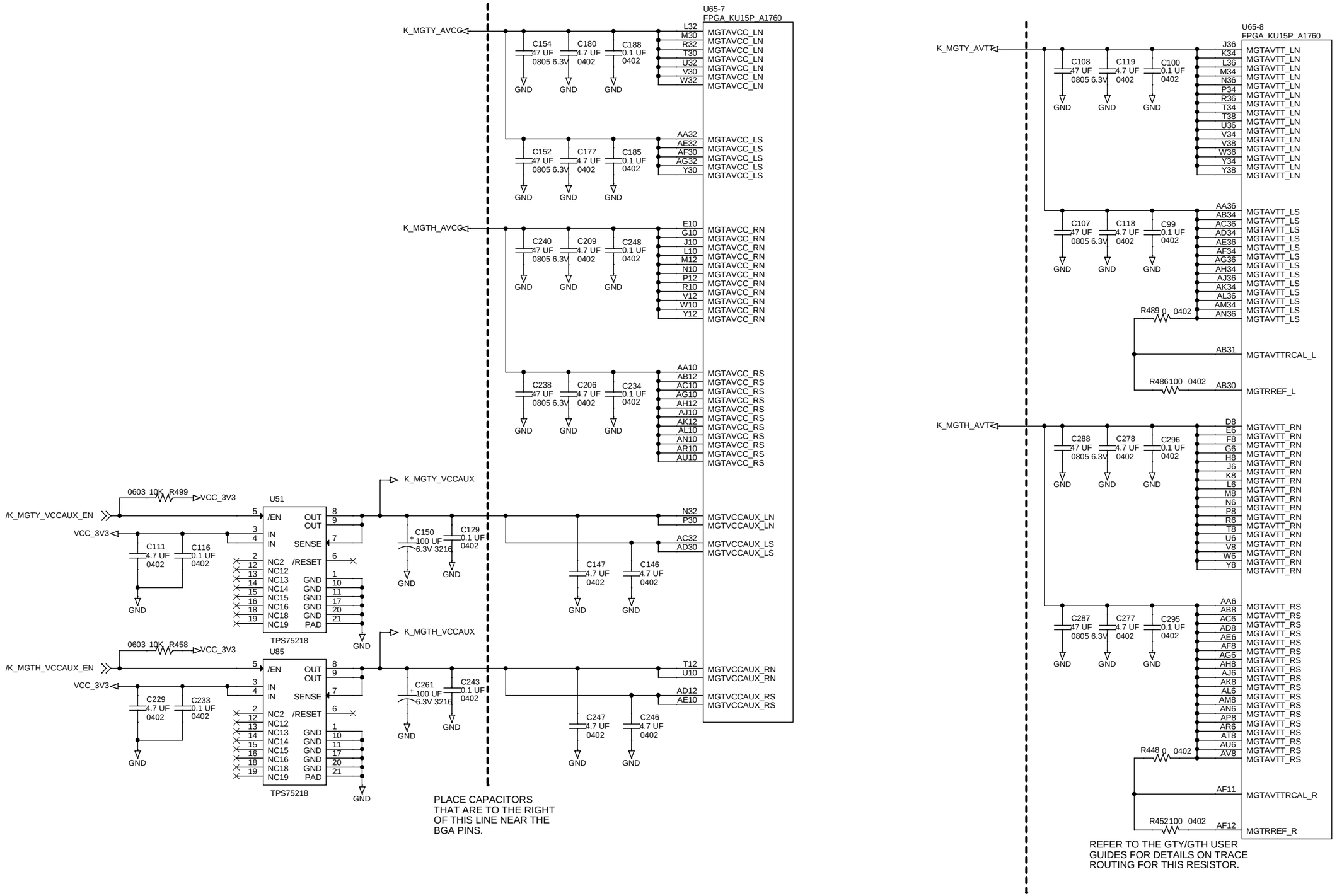
BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"xtp427-ultrascale-plus-schematic-review-checklist.xls"

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.02: KU15P FPGA INTERNAL POWER

Size | Document Number: 6089-103 | Rev: A

Date: Thursday, February 14, 2019 Sheet 33 of 75



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.03: KU15P GTH/GTY TRANSCEIVER POWER

Size	Document Number	Rev
	6089-103	A

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QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

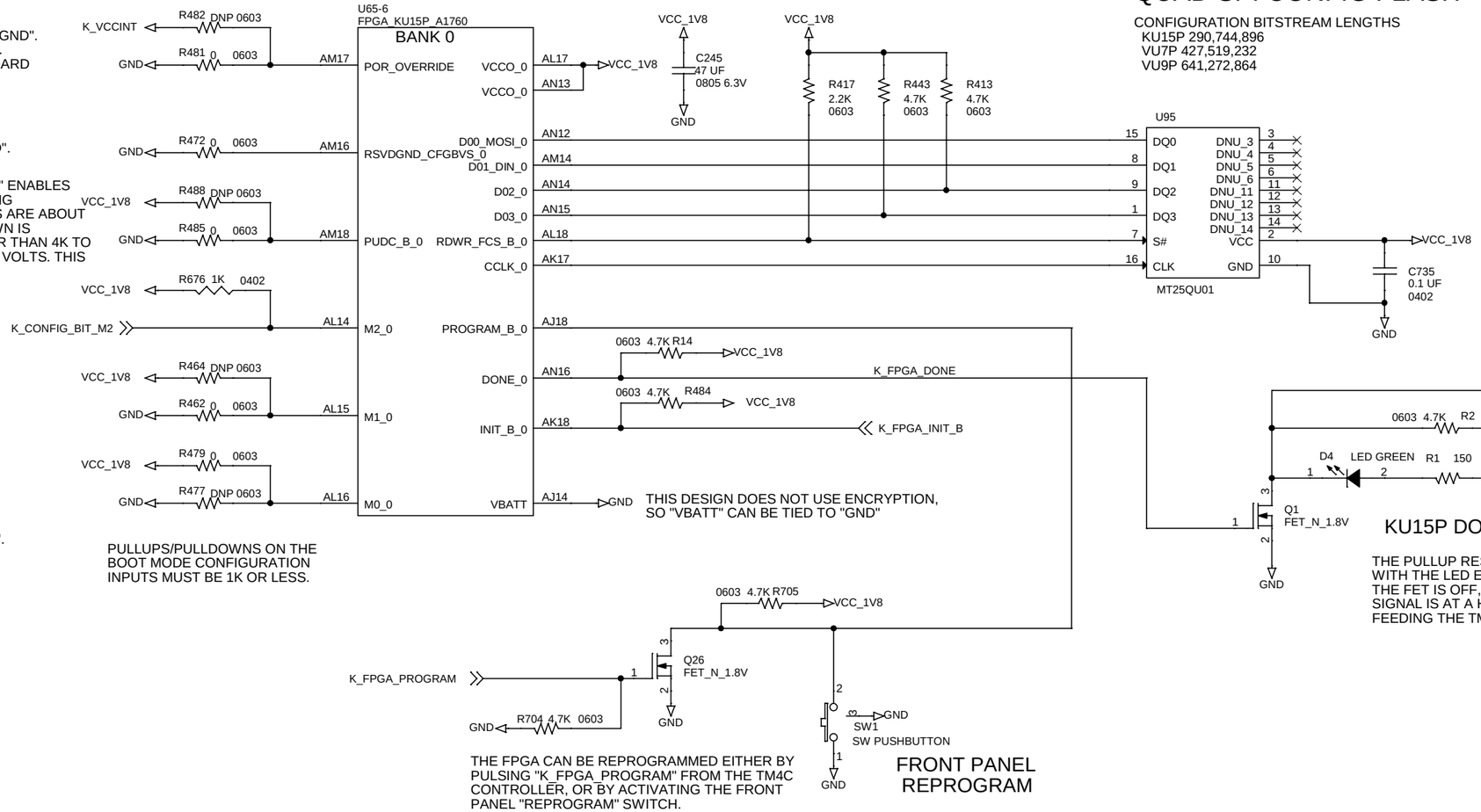
THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

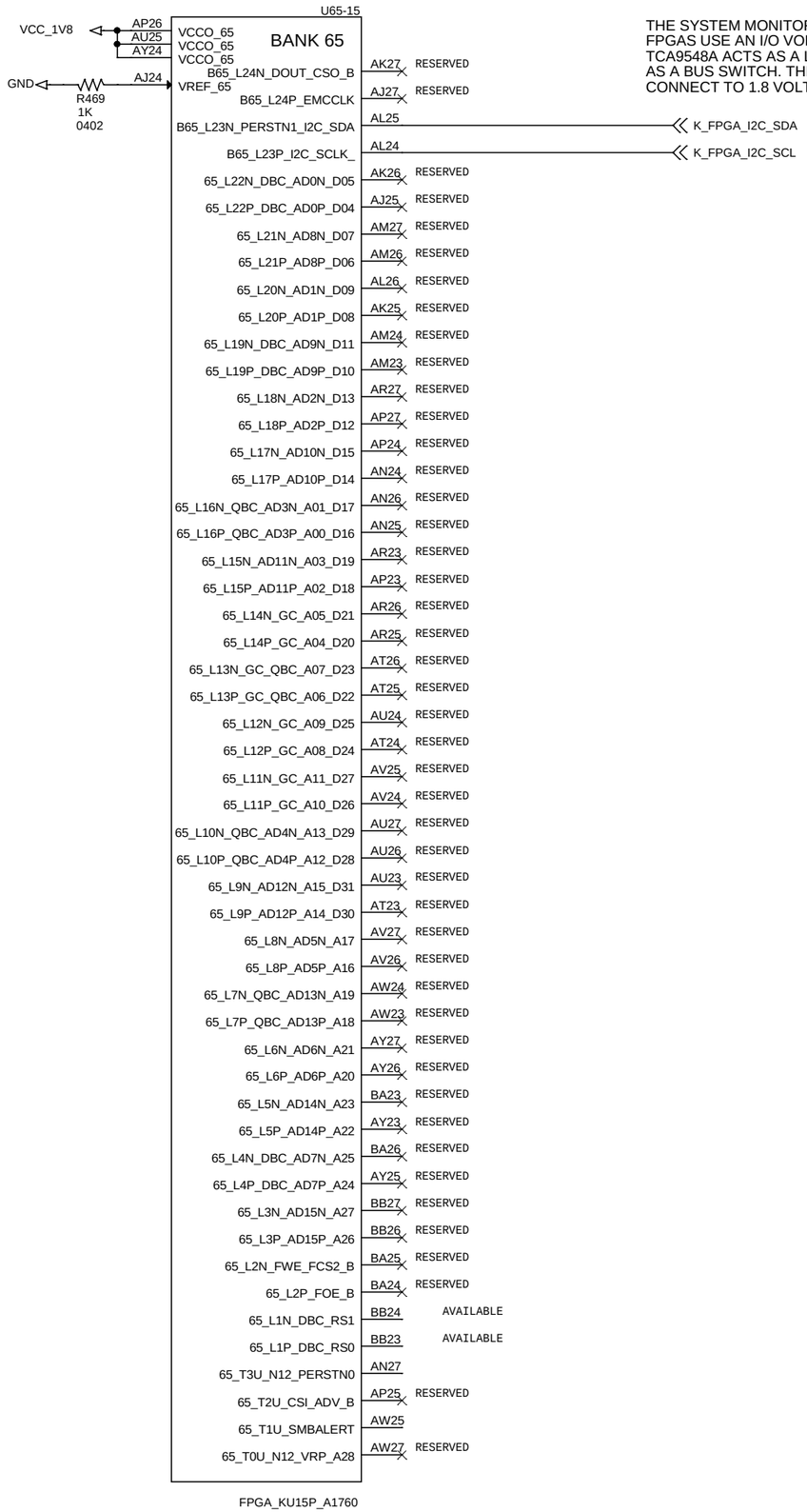
M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

PULLUPS/PULLDOWNS ON THE
BOOT MODE CONFIGURATION
INPUTS MUST BE 1K OR LESS.



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.04: KU15P FPGA CONFIGURATION		
Size	Document Number: 6089-103	Rev: A
Date: Sunday, February 17, 2019	Sheet 35 of 75	



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

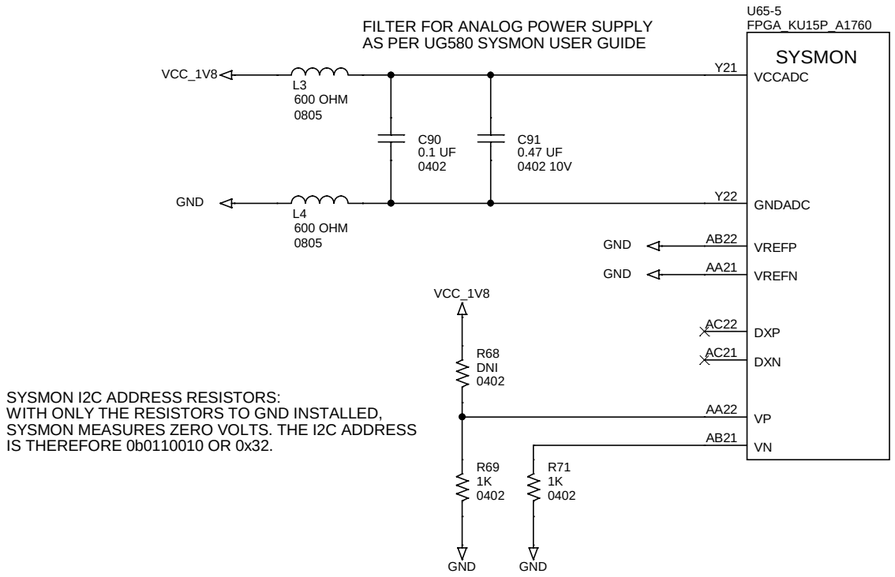
BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.05: KU15P BANK 65

Size	Document Number	Rev
	6089-103	A

Date: Sunday, February 17, 2019 Sheet 36 of 75

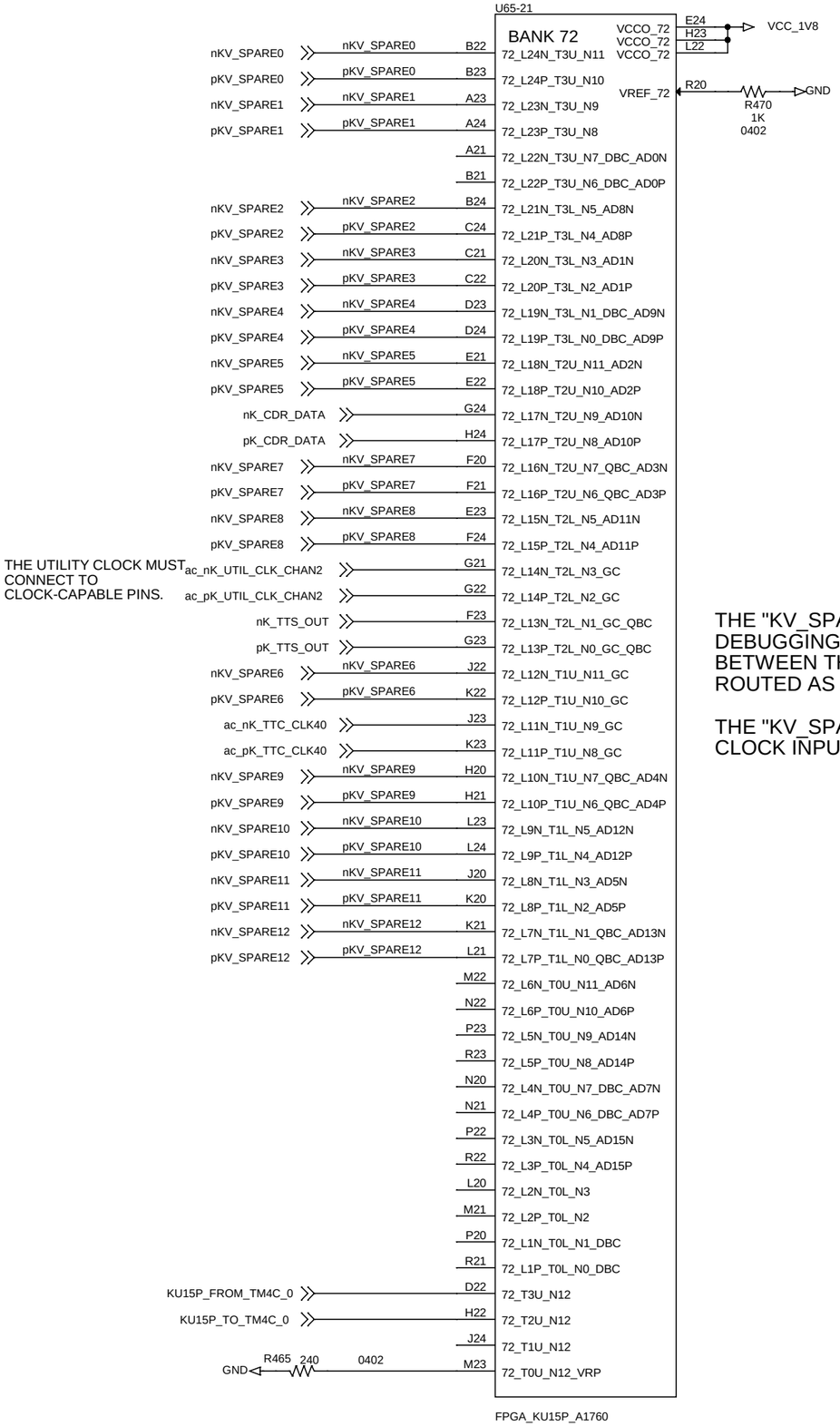


ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.06: KU15P SYSTEM MONITOR

Size	Document Number	Rev
	6089-103	A

Date: Thursday, February 14, 2019 Sheet 37 of 75

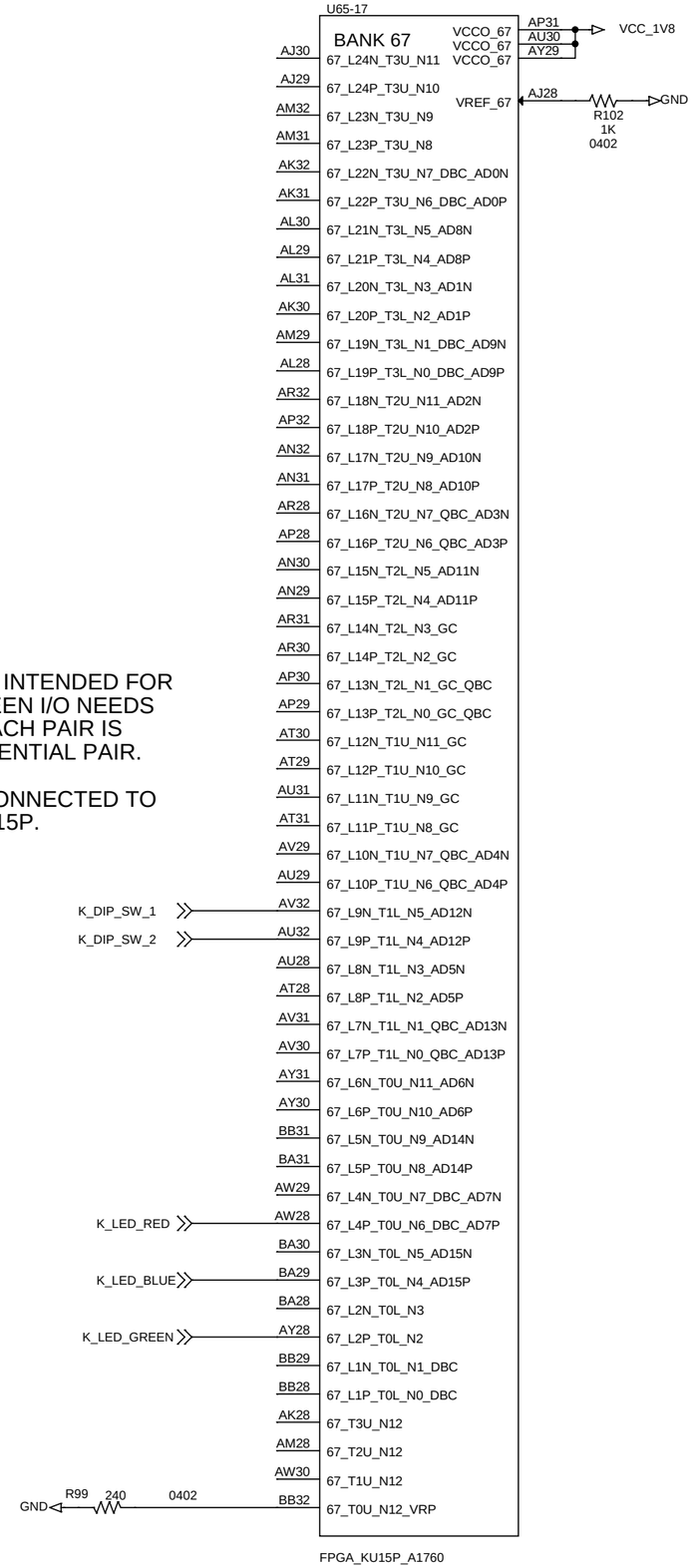


THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

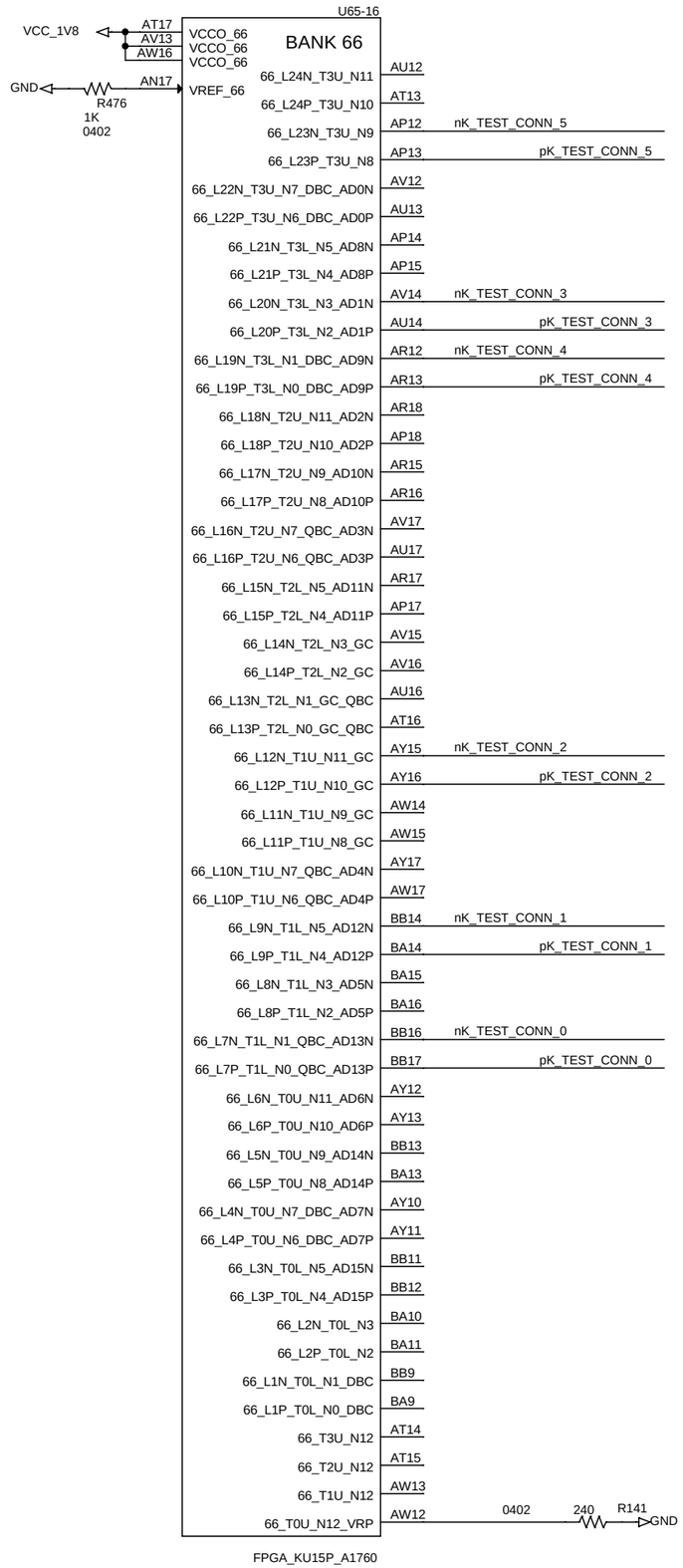
THE "KV_SPARE6" SIGNAL IS CONNECTED TO CLOCK INPUT PINS ON THE KU15P.

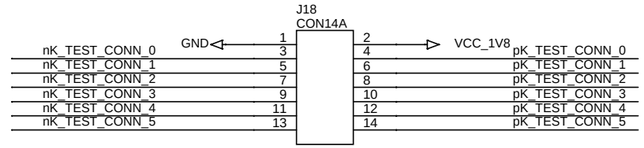
FPGA_KU15P_A1760



FPGA_KU15P_A1760

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 5.07: KU15P UTILITY BANKS		
Size	Document Number: 6089-103	Rev: A
Date: Sunday, February 17, 2019	Sheet 38 of 75	





THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "K_TEST_CONN_2" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.08 KU15P TEST CONNECTOR

Size	Document Number	Rev
	6089-103	A

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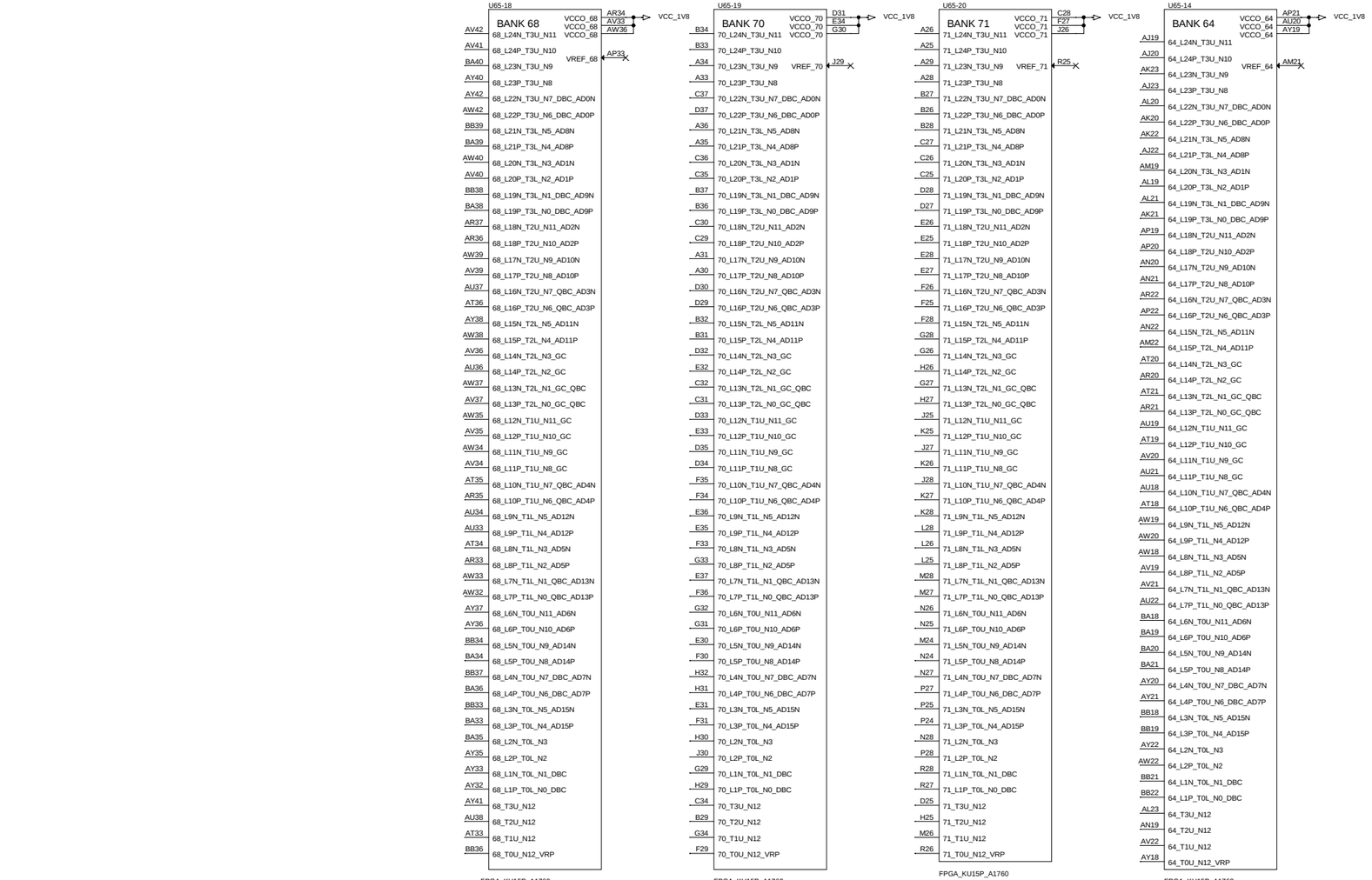

KU15P UNUSED BLOCKS

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.99: KU15P UNUSED BLOCKS

Size | Document Number: 6089-103 | Rev: A

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U66-1
FPGA_VU7P_B2104

A10	GND	GND	AF28
A12	GND	GND	AF3
A21	GND	GND	AF35
A3	GND	GND	AF36
A31	GND	GND	AF4
A41	GND	GND	AF40
A44	GND	GND	AF42
A6	GND	GND	AF45
AA1	GND	GND	AF46
AA10	GND	GND	AF5
AA13	GND	GND	AF8
AA15	GND	GND	AG1
AA17	GND	GND	AG11
AA19	GND	GND	AG17
AA2	GND	GND	AG2
AA21	GND	GND	AG21
AA23	GND	GND	AG23
AA25	GND	GND	AG25
AA27	GND	GND	AG27
AA29	GND	GND	AG33
AA31	GND	GND	AG35
AA35	GND	GND	AG39
AA38	GND	GND	AG42
AA42	GND	GND	AG43
AA43	GND	GND	AG44
AA44	GND	GND	AG5
AA5	GND	GND	AG7
AA6	GND	GND	AH14
AA7	GND	GND	AH16
AB12	GND	GND	AH20
AB14	GND	GND	AH22
AB16	GND	GND	AH24
AB18	GND	GND	AH26
AB20	GND	GND	AH3
AB22	GND	GND	AH30
AB24	GND	GND	AH35
AB26	GND	GND	AH37
AB28	GND	GND	AH4
AB3	GND	GND	AH41
AB30	GND	GND	AH42
AB35	GND	GND	AH45
AB37	GND	GND	AH46
AB4	GND	GND	AH5
AB40	GND	GND	AH9
AB42	GND	GND	AJ1
AB45	GND	GND	AJ10
AB46	GND	GND	AJ13
AB5	GND	GND	AJ15
AB8	GND	GND	AJ17
AC1	GND	GND	AJ2
AC10	GND	GND	AJ21
AC15	GND	GND	AJ23
AC17	GND	GND	AJ25
AC19	GND	GND	AJ35
AC2	GND	GND	AJ38
AC21	GND	GND	AJ42
AC23	GND	GND	AJ43
AC25	GND	GND	AJ44
AC27	GND	GND	AJ5
AC29	GND	GND	AJ6
AC35	GND	GND	AK14
AC39	GND	GND	AK16
AC42	GND	GND	AK18
AC43	GND	GND	AK20
AC44	GND	GND	AK22
AC5	GND	GND	AK24
AC7	GND	GND	AK3
AD14	GND	GND	AK34
AD16	GND	GND	AK35
AD18	GND	GND	AK37
AD20	GND	GND	AK4
AD22	GND	GND	AK40
AD24	GND	GND	AK42
AD26	GND	GND	AK45
AD28	GND	GND	AK46
AD3	GND	GND	AK5
AD32	GND	GND	AK8
AD35	GND	GND	AL1
AD37	GND	GND	AL11
AD4	GND	GND	AL2
AD41	GND	GND	AL31
AD42	GND	GND	AL35
AD45	GND	GND	AL39
AD46	GND	GND	AL42
AD5	GND	GND	AL43
AD9	GND	GND	AL44
AE1	GND	GND	AL5
AE10	GND	GND	AL7
AE17	GND	GND	AM18
AE19	GND	GND	AM28
AE2	GND	GND	AM3
AE21	GND	GND	AM35
AE23	GND	GND	AM37
AE25	GND	GND	AM4
AE27	GND	GND	AM41
AE29	GND	GND	AM42
AE35	GND	GND	AM45
AE38	GND	GND	AM46
AE42	GND	GND	AM5
AE43	GND	GND	AM9
AE44	GND	GND	AN1
AE5	GND	GND	AN10
AE6	GND	GND	AN12
AF12	GND	GND	AN15
AF14	GND	GND	AN2
AF16	GND	GND	AN25
AF20	GND	GND	AN35
AF22	GND	GND	AN38
AF24	GND	GND	AN42
AF26	GND	GND	AN43

GND GND

U66-2
FPGA_VU7P_B2104

AN44	GND	GND	B44
AN5	GND	GND	B45
AN6	GND	GND	B5
AP12	GND	GND	B6
AP22	GND	GND	B7
AP3	GND	GND	B8
AP32	GND	GND	BA11
AP35	GND	GND	BA21
AP36	GND	GND	BA3
AP4	GND	GND	BA31
AP40	GND	GND	BA37
AP42	GND	GND	BA38
AP45	GND	GND	BA39
AP46	GND	GND	BA44
AP5	GND	GND	BA6
AP8	GND	GND	BB1
AR1	GND	GND	BB18
AR11	GND	GND	BB2
AR12	GND	GND	BB28
AR19	GND	GND	BB3
AR2	GND	GND	BB39
AR29	GND	GND	BB40
AR35	GND	GND	BB41
AR39	GND	GND	BB44
AR42	GND	GND	BB45
AR43	GND	GND	BB46
AR44	GND	GND	BB6
AR5	GND	GND	BB8
AR7	GND	GND	BC15
AT12	GND	GND	BC25
AT16	GND	GND	BC3
AT26	GND	GND	BC35
AT3	GND	GND	BC4
AT35	GND	GND	BC41
AT37	GND	GND	BC42
AT4	GND	GND	BC44
AT41	GND	GND	BC6
AT42	GND	GND	BD1
AT45	GND	GND	BD12
AT46	GND	GND	BD22
AT5	GND	GND	BD3
AT9	GND	GND	BD32
AU1	GND	GND	BD41
AU10	GND	GND	BD44
AU12	GND	GND	BD46
AU2	GND	GND	BD6
AU23	GND	GND	BE19
AU33	GND	GND	BE2
AU35	GND	GND	BE29
AU38	GND	GND	BE3
AU42	GND	GND	BE39
AU43	GND	GND	BE41
AU44	GND	GND	BE45
AU5	GND	GND	BE5
AU6	GND	GND	BE6
AV12	GND	GND	BE9
AV20	GND	GND	BF16
AV3	GND	GND	BF26
AV30	GND	GND	BF3
AV35	GND	GND	BF36
AV36	GND	GND	BF41
AV37	GND	GND	BF44
AV4	GND	GND	BF6
AV40	GND	GND	C1
AV42	GND	GND	C11
AV45	GND	GND	C12
AV46	GND	GND	C15
AV5	GND	GND	C2
AV8	GND	GND	C25
AW1	GND	GND	C35
AW10	GND	GND	C41
AW11	GND	GND	C44
AW12	GND	GND	C46
AW17	GND	GND	C5
AW2	GND	GND	D12
AW27	GND	GND	D22
AW37	GND	GND	D3
AW39	GND	GND	D32
AW42	GND	GND	D4
AW43	GND	GND	D41
AW44	GND	GND	D42
AW5	GND	GND	D44
AW6	GND	GND	D5
AY1	GND	GND	D9
AY10	GND	GND	E1
AY14	GND	GND	E10
AY2	GND	GND	E12
AY24	GND	GND	E19
AY3	GND	GND	E2
AY34	GND	GND	E29
AY37	GND	GND	E41
AY4	GND	GND	E44
AY41	GND	GND	E45
AY42	GND	GND	E46
AY43	GND	GND	E5
AY44	GND	GND	E6
AY45	GND	GND	F12
AY46	GND	GND	F16
AY5	GND	GND	F26
AY6	GND	GND	F3
AY7	GND	GND	F36
AY8	GND	GND	F39
AY9	GND	GND	F4
B12	GND	GND	F40
B18	GND	GND	F41
B2	GND	GND	F44
B28	GND	GND	F5
B38	GND	GND	F8
B4	GND	GND	G1
B41	GND	GND	G11

GND GND

U66-3
FPGA_VU7P_B2104

G12	GND	GND	R35
G13	GND	GND	R39
G2	GND	GND	R42
G23	GND	GND	R43
G33	GND	GND	R44
G39	GND	GND	R5
G42	GND	GND	R7
G43	GND	GND	T12
G44	GND	GND	T14
G45	GND	GND	T16
G46	GND	GND	T18
G5	GND	GND	T20
G7	GND	GND	T22
H12	GND	GND	T24
H20	GND	GND	T3
H3	GND	GND	T35
H30	GND	GND	T37
H39	GND	GND	T4
H4	GND	GND	T41
H41	GND	GND	T42
H42	GND	GND	T45
H45	GND	GND	T46
H46	GND	GND	T5
H5	GND	GND	T9
H9	GND	GND	U1
J1	GND	GND	U10
J10	GND	GND	U13
J12	GND	GND	U15
J17	GND	GND	U17
J2	GND	GND	U19
J27	GND	GND	U2
J37	GND	GND	U21
J38	GND	GND	U23
J39	GND	GND	U25
J42	GND	GND	U27
J43	GND	GND	U33
J44	GND	GND	U35
J5	GND	GND	U38
J6	GND	GND	U42
K12	GND	GND	U43
K14	GND	GND	U44
K24	GND	GND	U5
K3	GND	GND	U6
K35	GND	GND	V14
K36	GND	GND	V16
K37	GND	GND	V18
K4	GND	GND	V20
K40	GND	GND	V22
K42	GND	GND	V24
K45	GND	GND	V26
K46	GND	GND	V28
K5	GND	GND	V3
K8	GND	GND	V30
L1	GND	GND	V35
L11	GND	GND	V36
L12	GND	GND	V4
L2	GND	GND	V40
L21	GND	GND	V42
L31	GND	GND	V45
L35	GND	GND	V46
L39	GND	GND	V5
L42	GND	GND	V8
L43	GND	GND	W1
L44	GND	GND	W11
L5	GND	GND	W13
L7	GND	GND	W15
M12	GND	GND	W17
M18	GND	GND	W19
M28	GND	GND	W2
M3	GND	GND	W21
M35	GND	GND	W23
M37	GND	GND	W25
M4	GND	GND	W27
M41	GND	GND	W29
M42	GND	GND	W35
M45	GND	GND	W39
M46	GND	GND	W42
M5	GND	GND	W43
M9	GND	GND	W44
N1	GND	GND	W5
N10	GND	GND	W7
N12	GND	GND	Y14
N15	GND	GND	Y16
N2	GND	GND	Y18
N25	GND	GND	Y20
N35	GND	GND	Y22
N38	GND	GND	Y24
N42	GND	GND	Y26
N43	GND	GND	Y28
N44	GND	GND	Y3
N5	GND	GND	Y34
N6	GND	GND	Y35
P12	GND	GND	Y37
P22	GND	GND	Y4
P3	GND	GND	Y41
P32	GND	GND	Y42
P35	GND	GND	Y45
P36	GND	GND	Y46
P4	GND	GND	Y5
P40	GND	GND	Y9
P42	GND		
P45	GND		
P46	GND		
P5	GND		
P8	GND		
R1	GND		
R10	GND		
R19	GND		
R2	GND		
R29	GND		

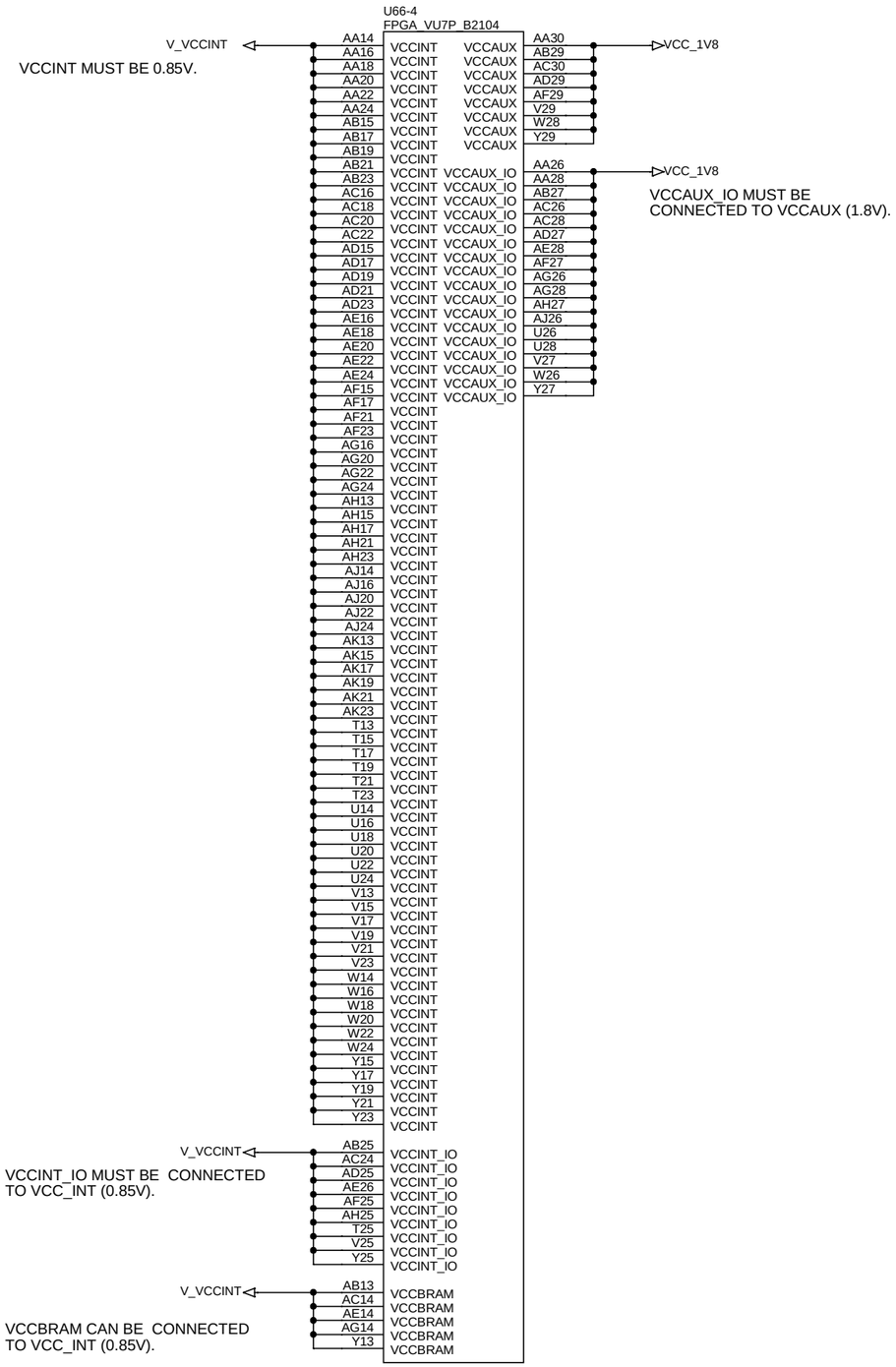
GND GND

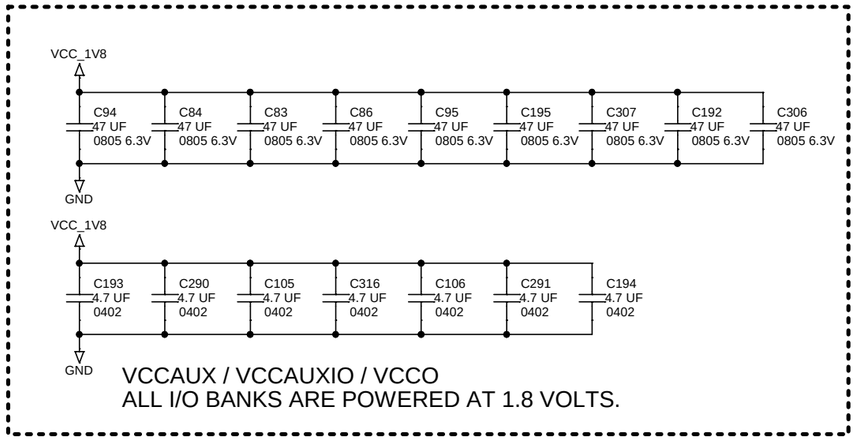
ATCA FPGA BOARD, KU15P AND VU7P, MK1

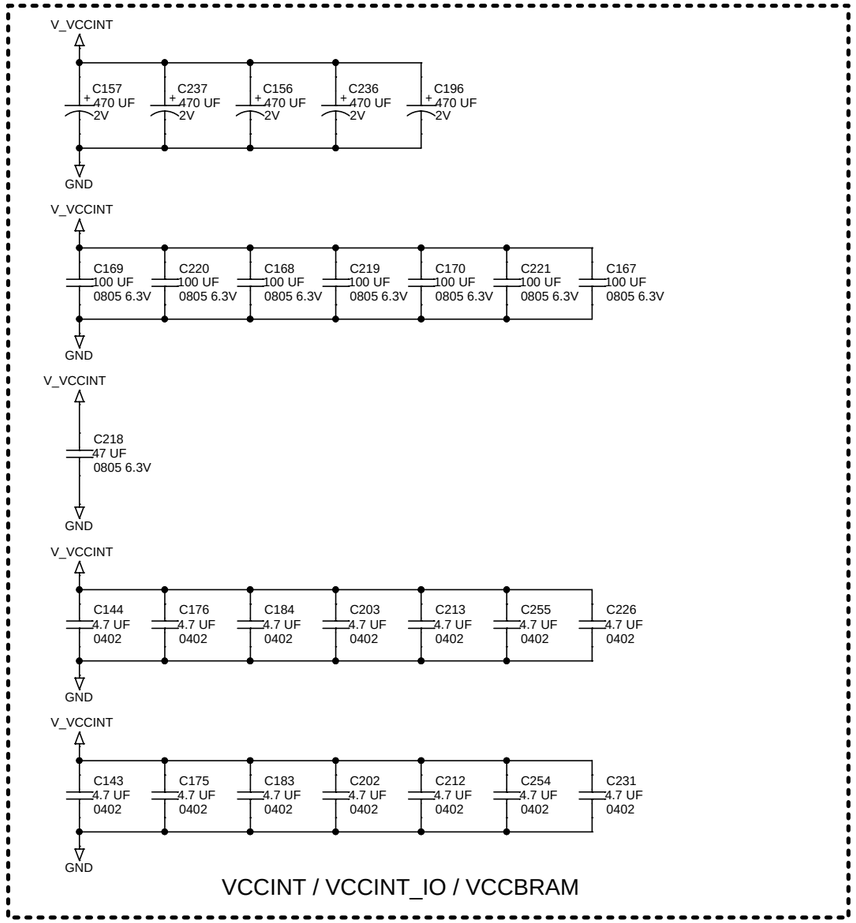
Title
6.01: VU7P FPGA GND

Size	Document Number	Rev
	6089-103	A

Date: Thursday, February 14, 2019 Sheet 41 of 75



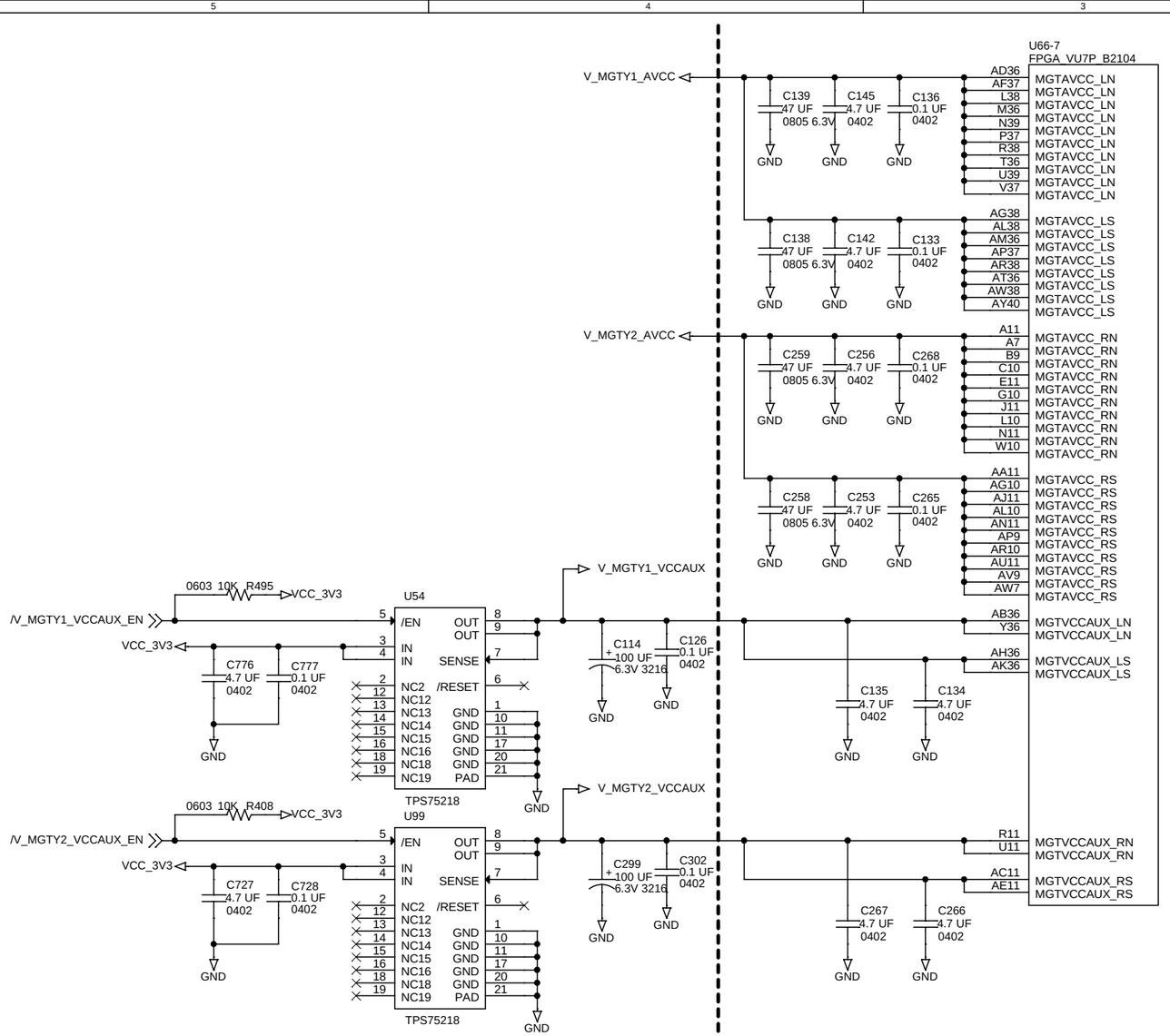


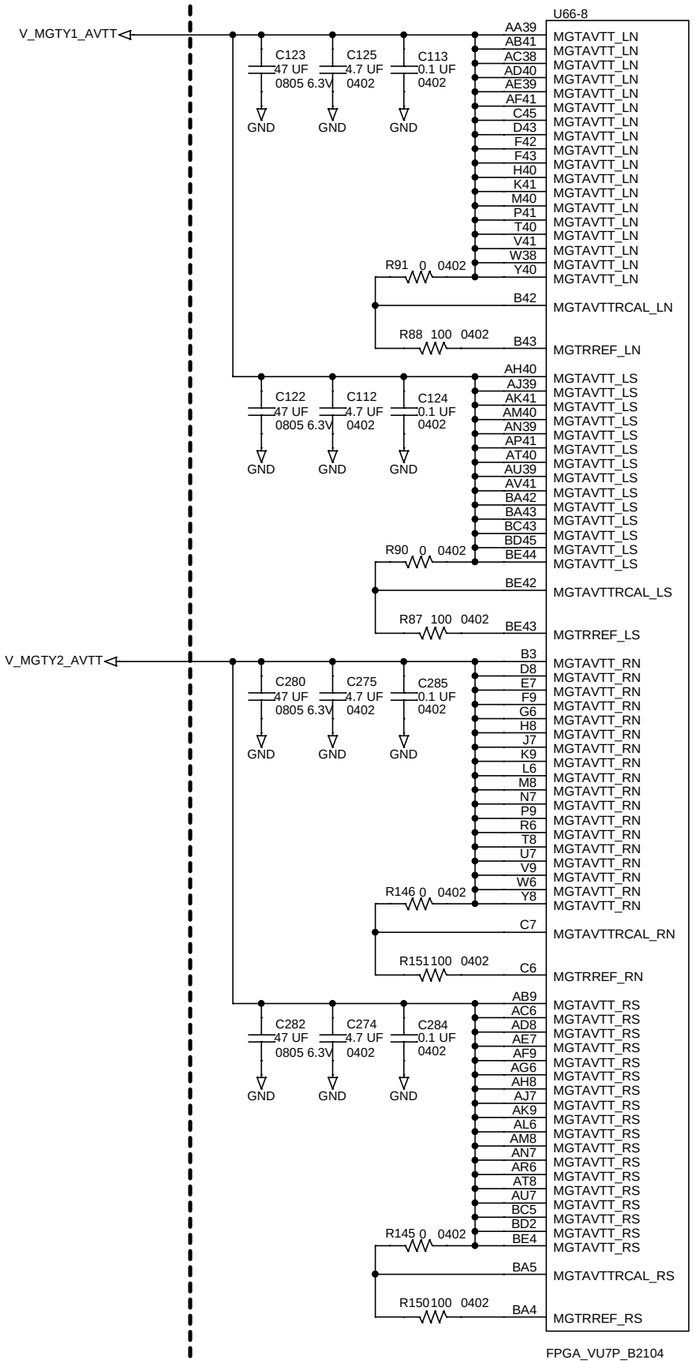


BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"xtp427-ultrascale-plus-schematic-review-checklist.xls"

QUANTITIES BASE ON POSSIBLE UPGRADE TO VU9P

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.02: VU7P FPGA INTERNAL POWER		
Size	Document Number: 6089-103	Rev: A
Date: Thursday, February 14, 2019	Sheet 42 of 75	





ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 6.03: VU7P GTY TRANSCEIVER POWER			
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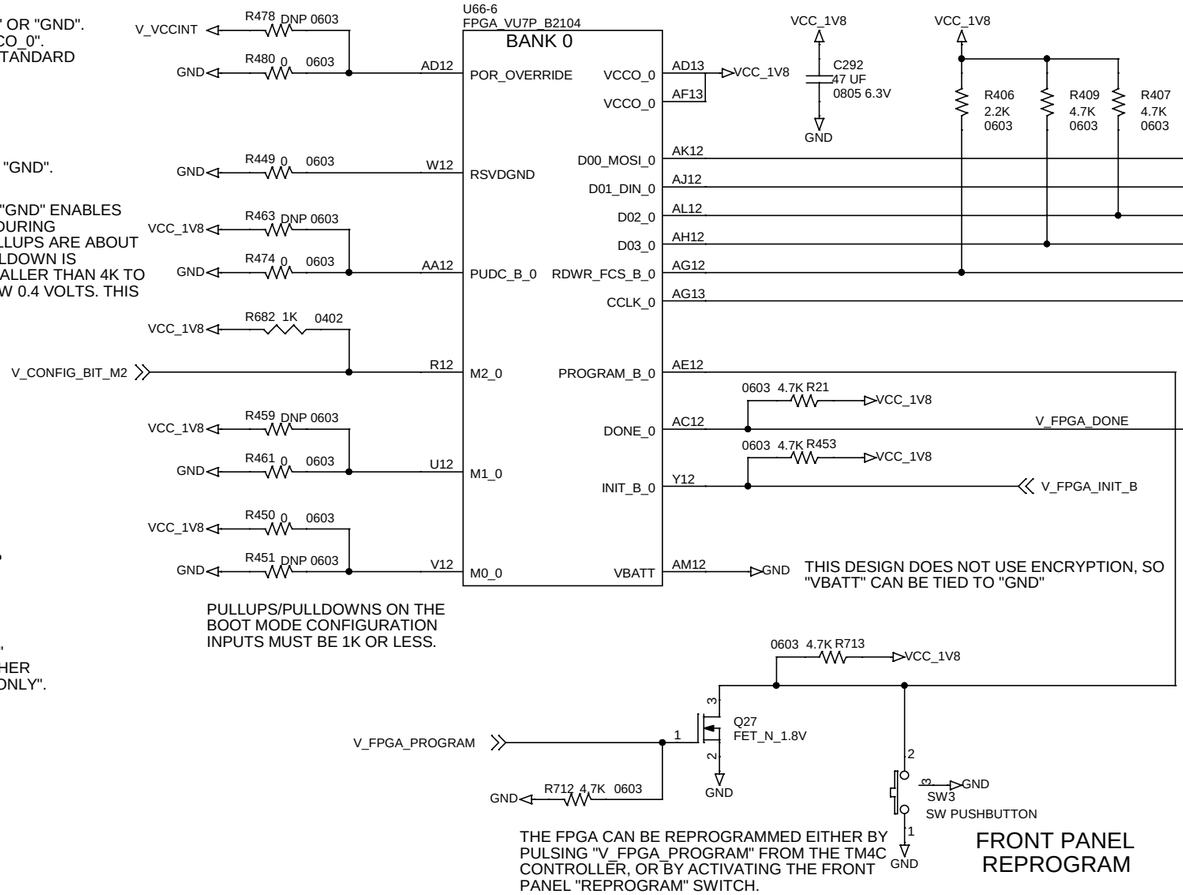
MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".



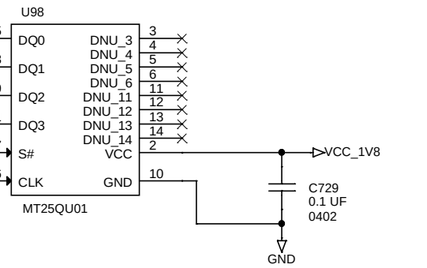
PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

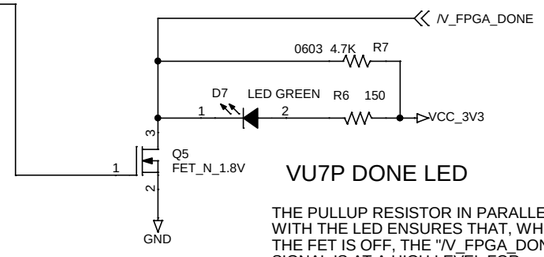
THE FPGA CAN BE REPROGRAMMED EITHER BY PULSING "V_FPGA_PROGRAM" FROM THE TM4C CONTROLLER, OR BY ACTIVATING THE FRONT PANEL "REPROGRAM" SWITCH.

FRONT PANEL REPROGRAM

QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864





VU7P DONE LED

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/V_FPGA_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE TM4C CONTROLLER.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 6.04: VU7P FPGA CONFIGURATION			
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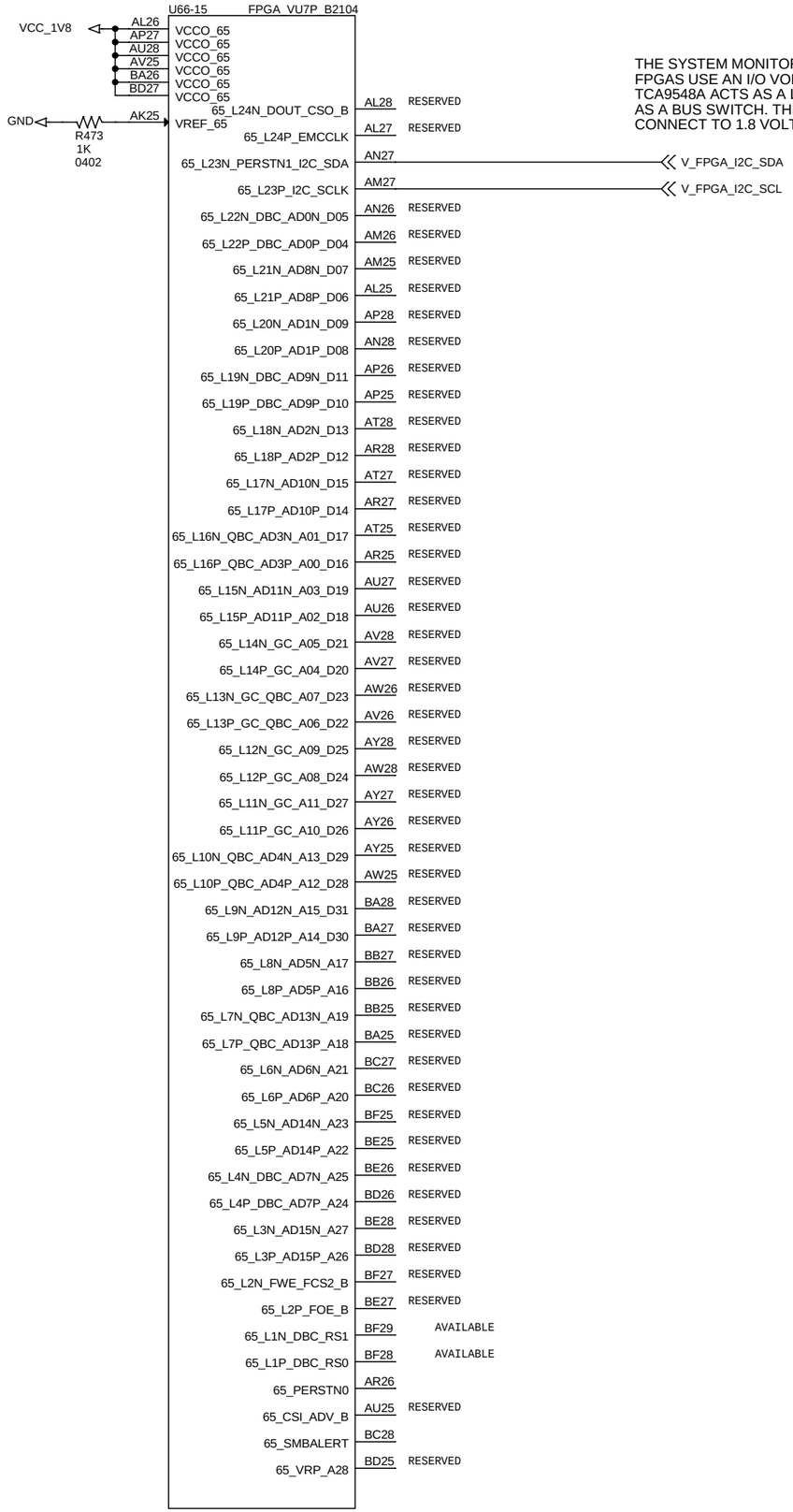

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.05: VU7P BANK 65

Size | Document Number: 6089-103 | Rev: A

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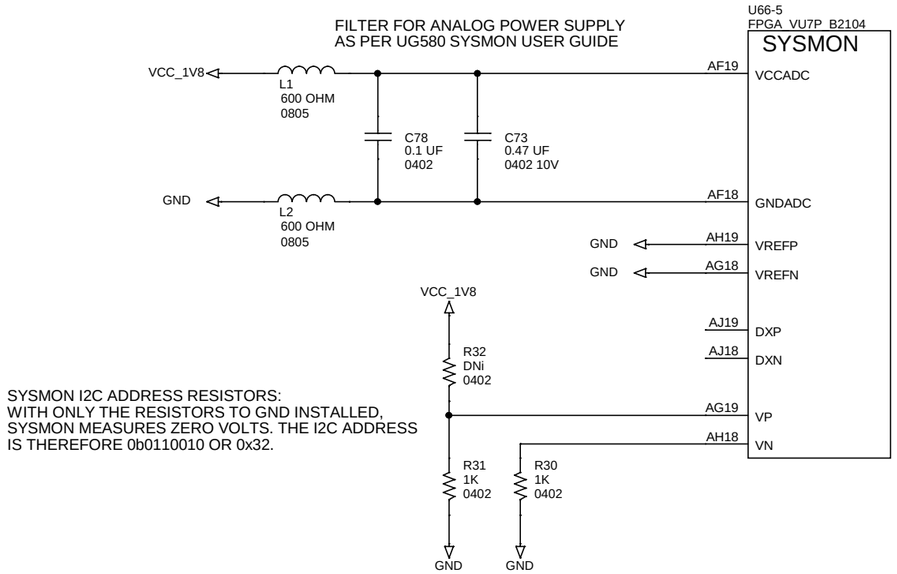

SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.06: VU7P SYSTEM MONITOR		
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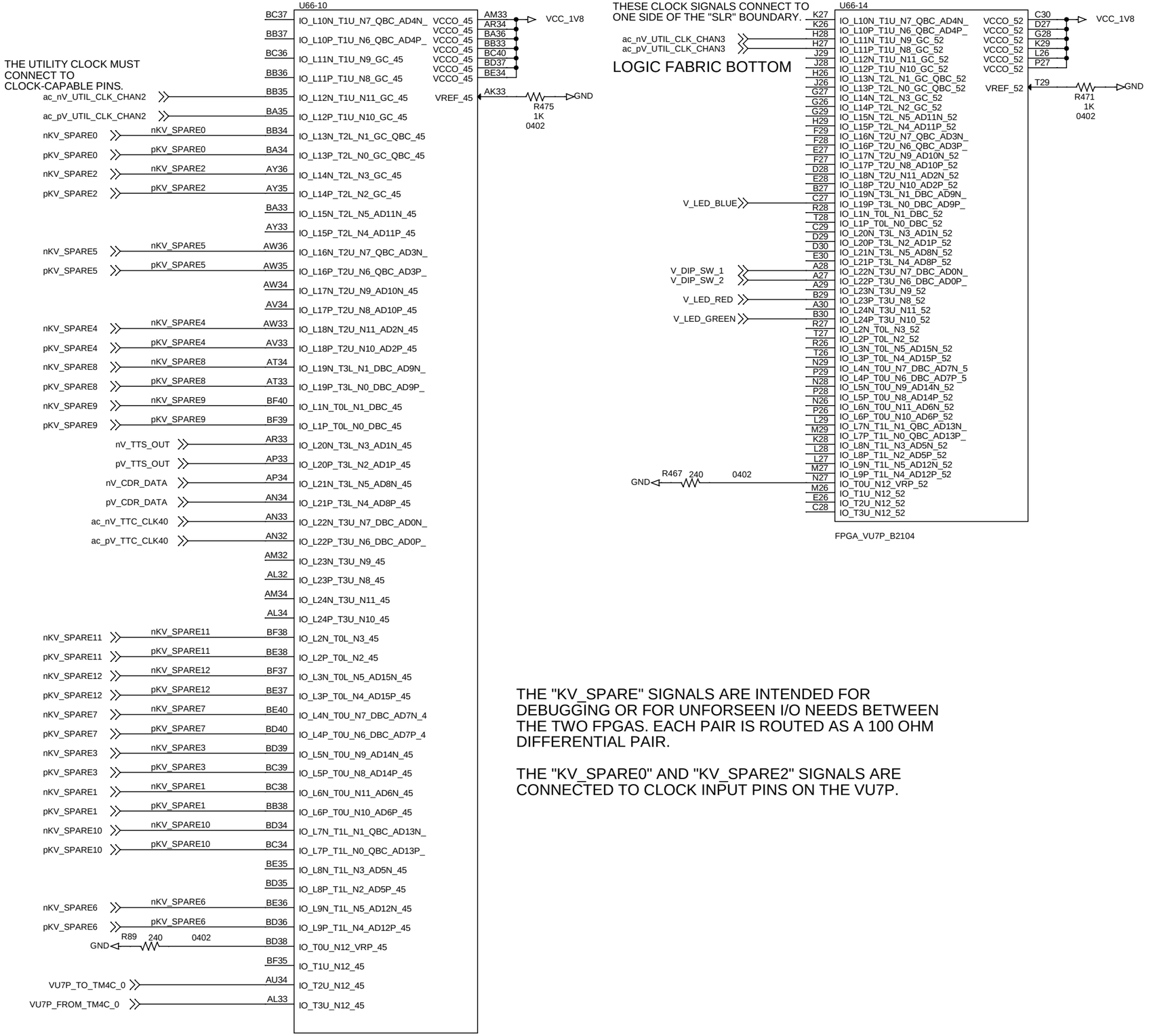
THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

THESE CLOCK SIGNALS CONNECT TO ONE SIDE OF THE "SLR" BOUNDARY.

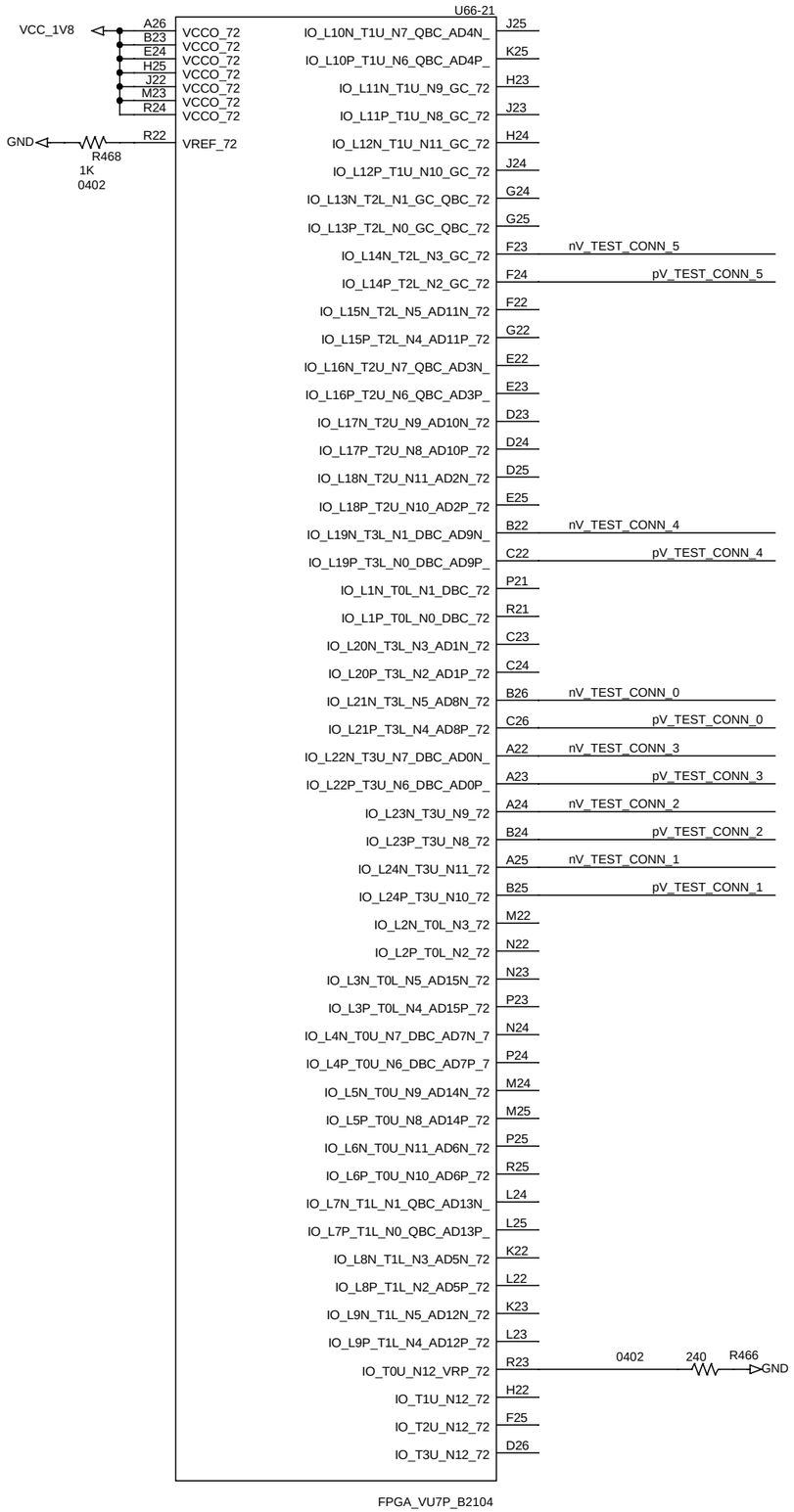
LOGIC FABRIC BOTTOM

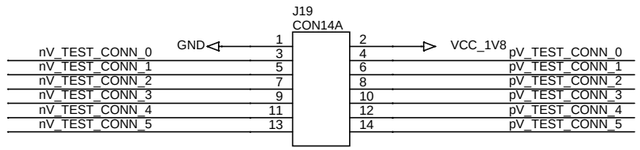
THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "KV_SPARE0" AND "KV_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE VU7P.



ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.07 VU7P UTILITY BANKS		
Size	Document Number: 6089-103	Rev: A
Date: Sunday, February 17, 2019	Sheet 47 of 75	





THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "V_TEST_CONN_5" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 6.08 VU7P TEST CONNECTOR		
Size	Document Number: 6089-103	Rev: A
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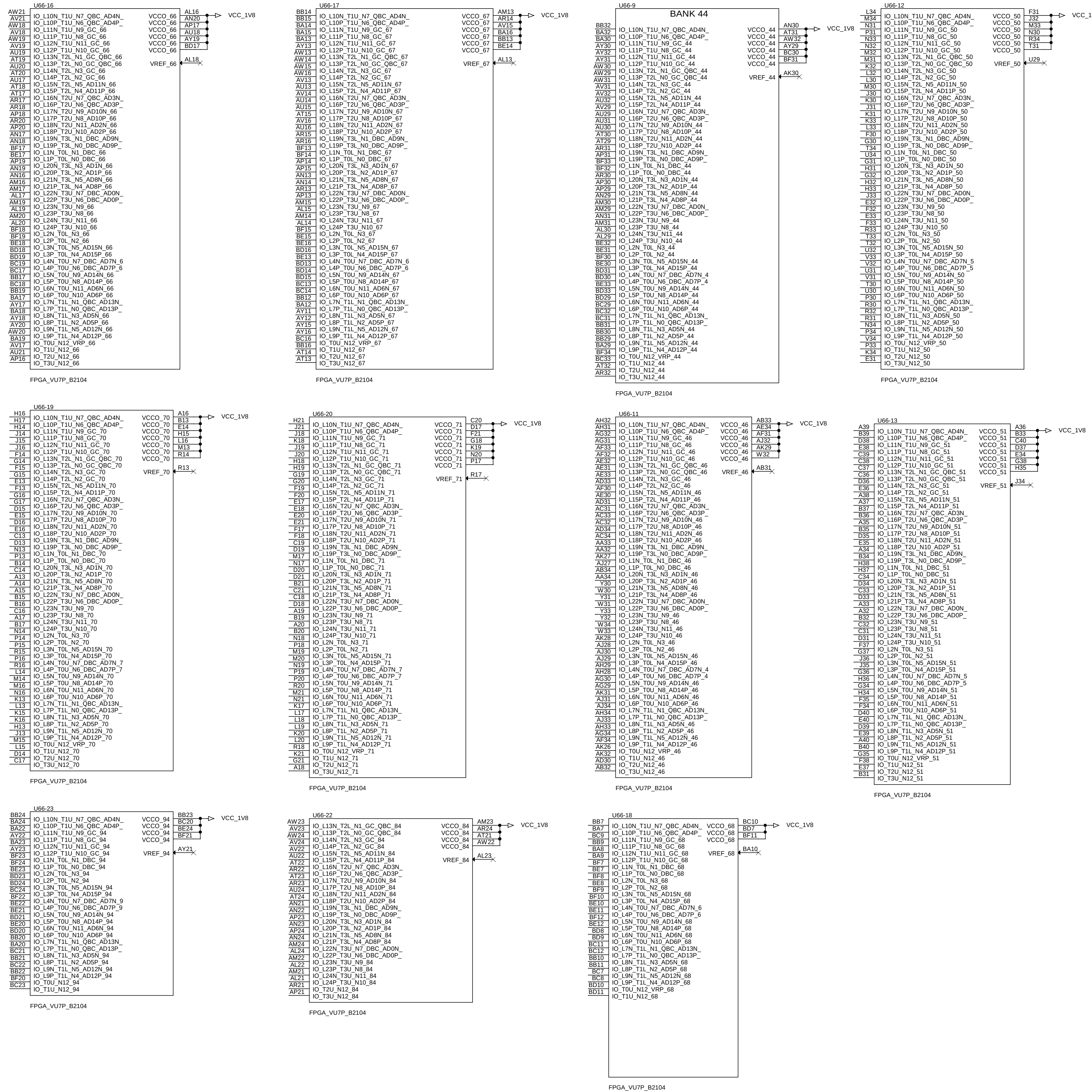

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.99: VU7P UNUSED BLOCKS

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	6089-103	A

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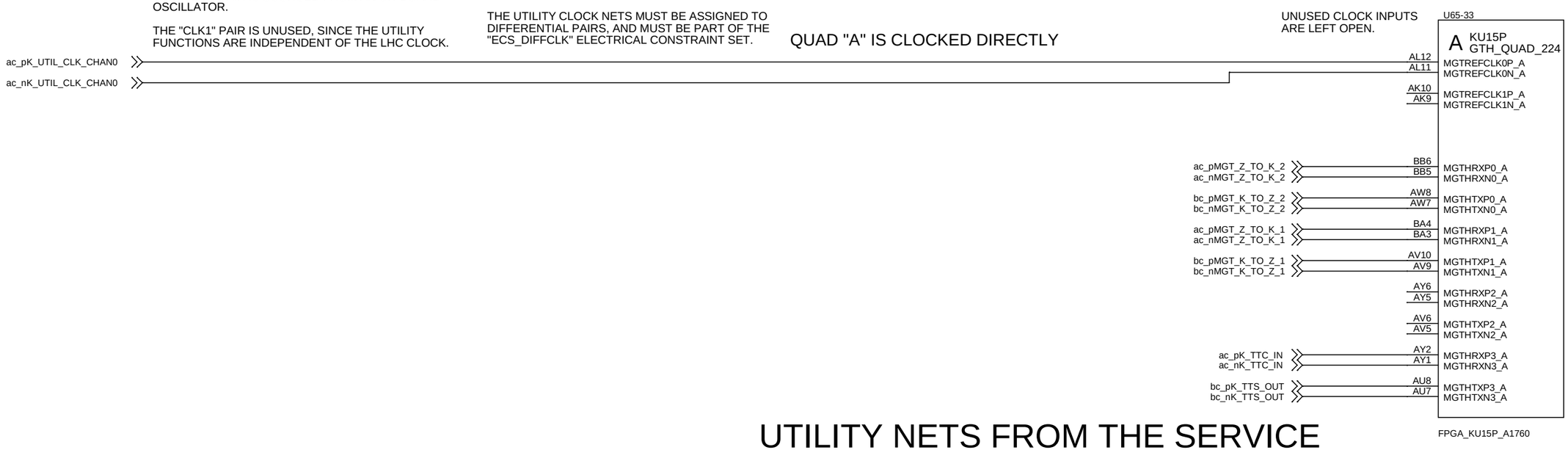
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.01: KU15P QUAD A UTILITY #1		
Size	Document Number: 6089-103	Rev: A
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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

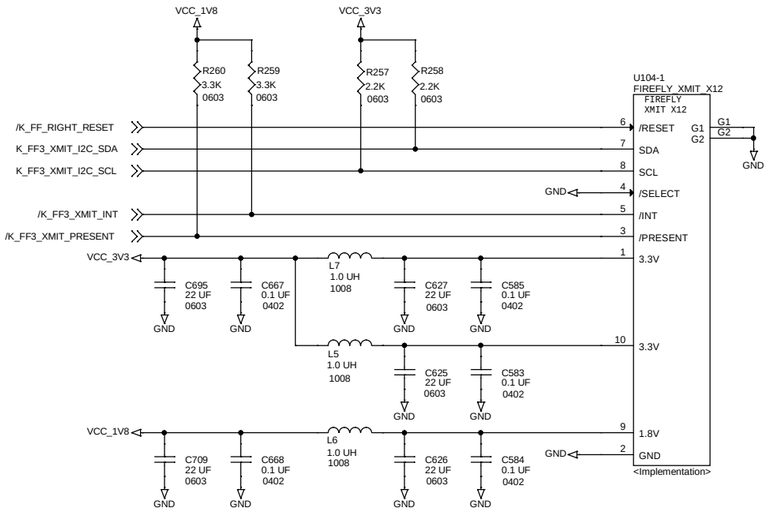
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

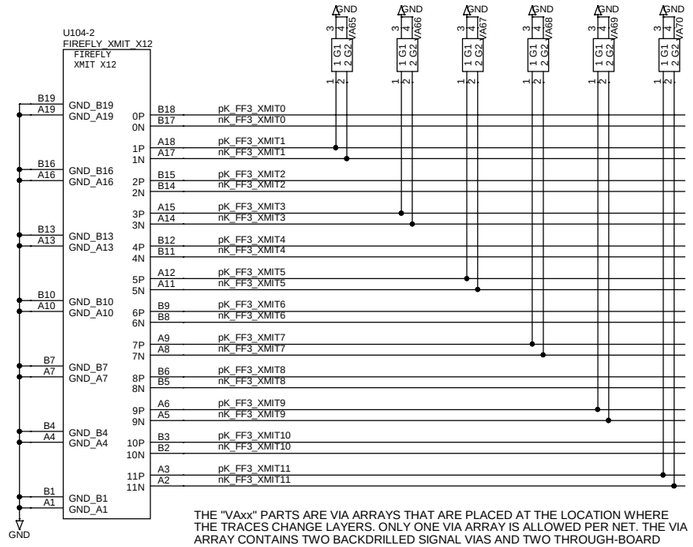
QUADS "B" AND "D" ARE CLOCKED FROM QUAD "C"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

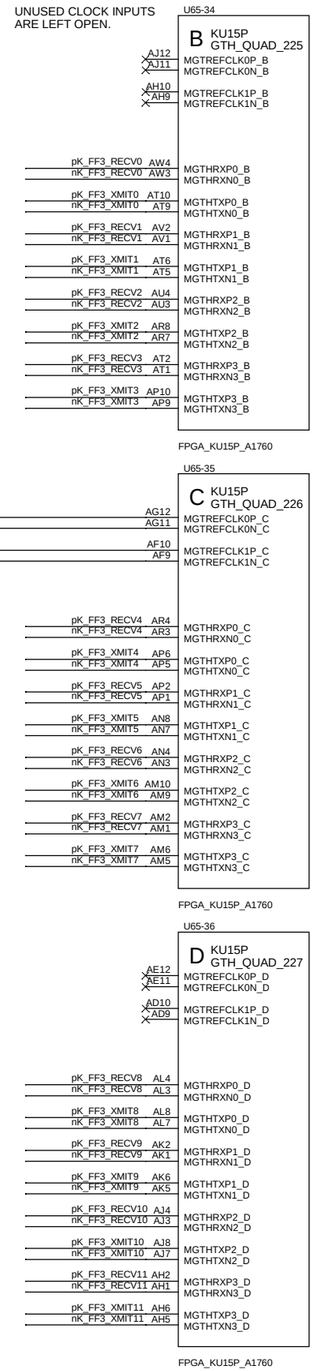
ac_pK_CLK0_CHAN
ac_nK_CLK0_CHAN
ac_pK_CLK1_CHAN
ac_nK_CLK1_CHAN

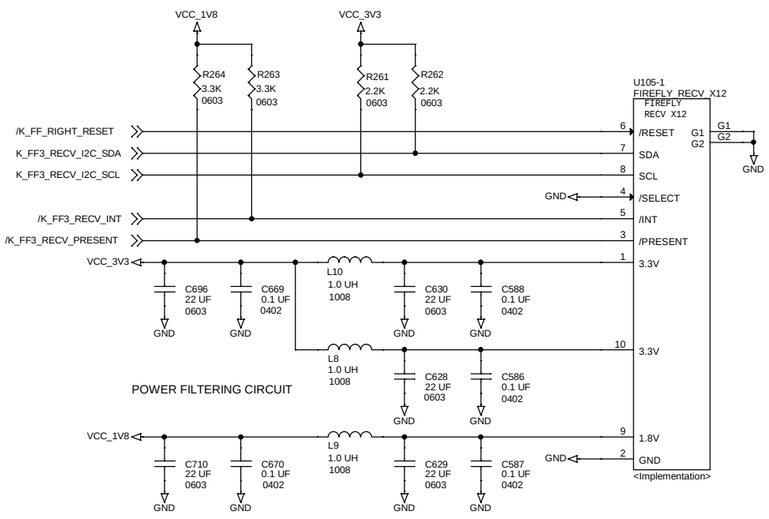


ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.





POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

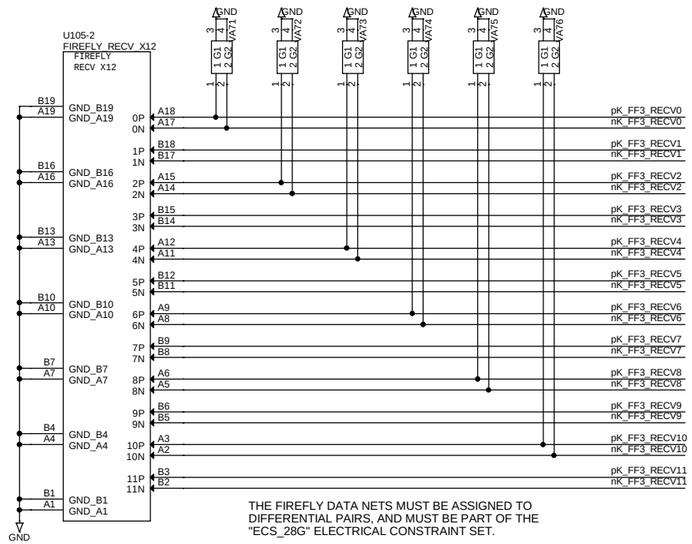
XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 7.02: KU15P QUADS BCD FIREFLY X12 #3			
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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

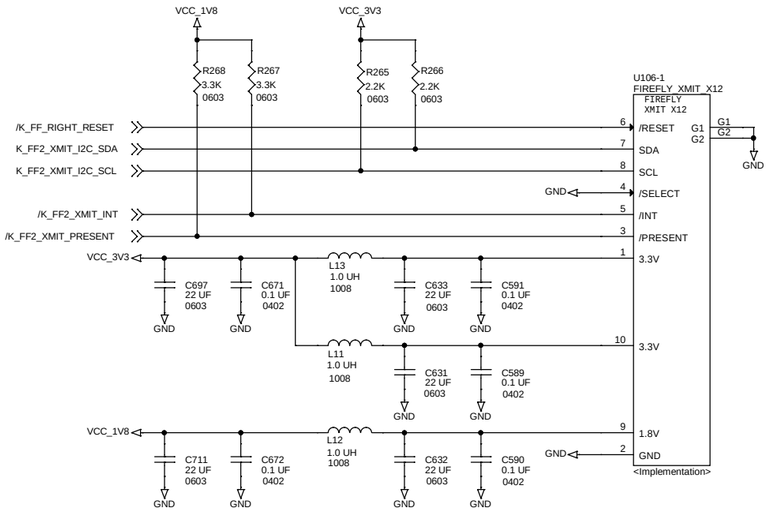
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

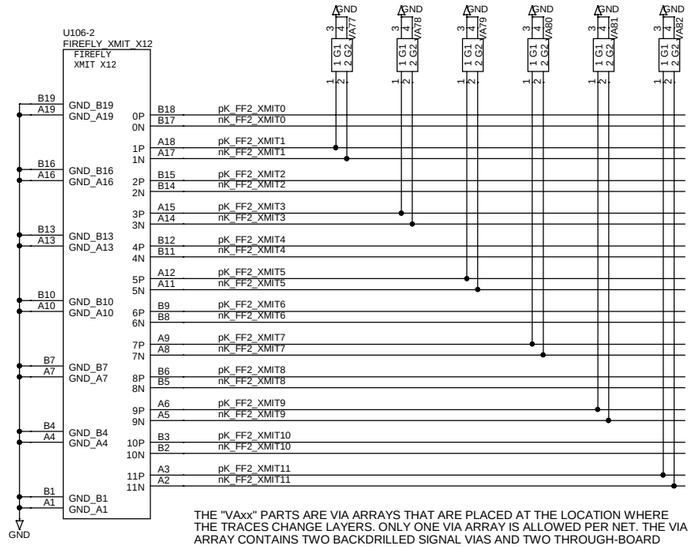
QUADS "E" AND "G" ARE CLOCKED FROM QUAD "F"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

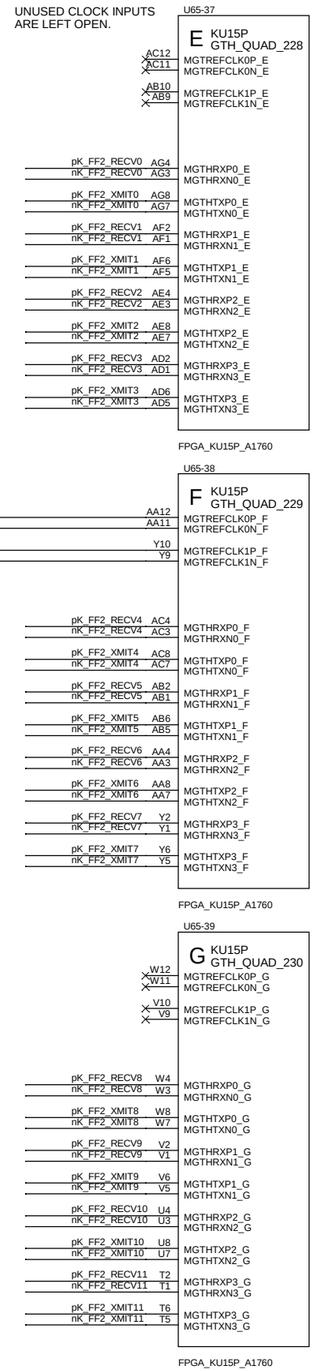
ac_pK_CLK0_CHAN
ac_nK_CLK0_CHAN
ac_pK_CLK1_CHAN
ac_nK_CLK1_CHAN

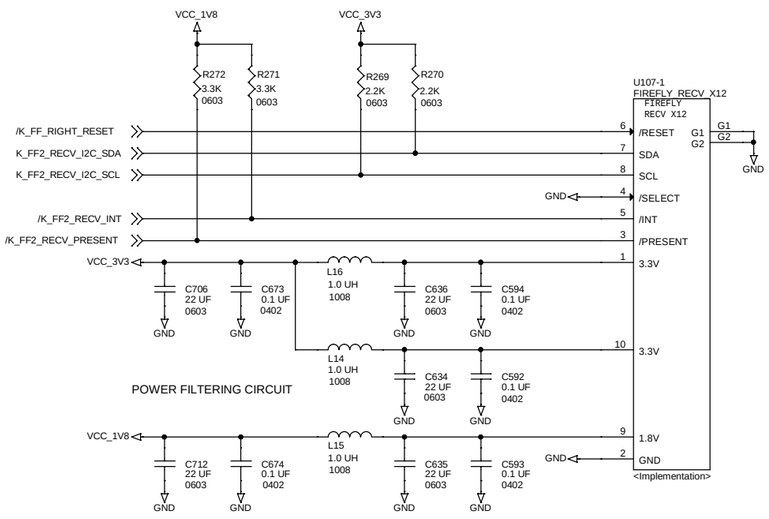


ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

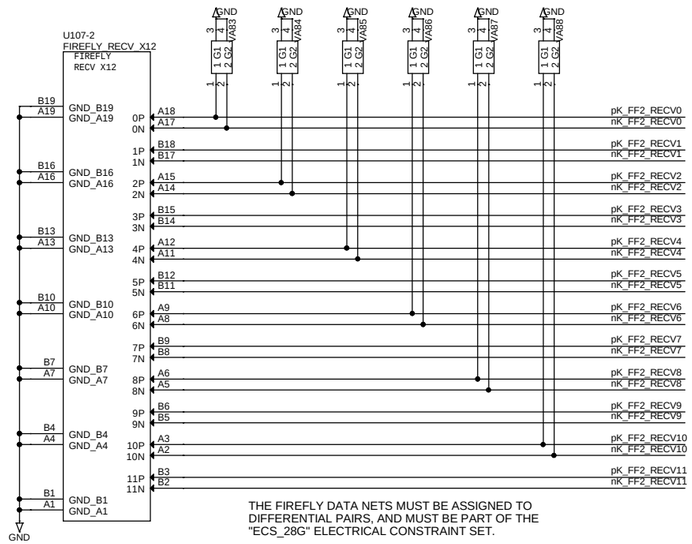


THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.





POWER FILTERING CIRCUIT



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.03: KU15P QUADS EFG FIREFLY X12 #2

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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN
ac_nK_CLK0_CHAN
ac_pK_CLK1_CHAN
ac_nK_CLK1_CHAN

U65-40
FPGA_KU15P_A1760
H KU15P GTH_QUAD_231
U12 MGTREFCLK0P_H
U11 MGTREFCLK0N_H
T10 MGTREFCLK1P_H
T9 MGTREFCLK1N_H

U65-41
FPGA_KU15P_A1760
I KU15P GTH_QUAD_232
R12 MGTREFCLK0P_I
R11 MGTREFCLK0N_I
P10 MGTREFCLK1P_I
P9 MGTREFCLK1N_I

U65-42
FPGA_KU15P_A1760
J KU15P GTH_QUAD_233
N12 MGTREFCLK0P_J
N11 MGTREFCLK0N_J
M10 MGTREFCLK1P_J
M9 MGTREFCLK1N_J

VCC_1V8, VCC_3V3
R276 3.3K 0603, R275 3.3K 0603, R273 2.2K 0603, R274 2.2K 0603

U108-1
FIREFLY_XMIT_X12
FIREFLY XMIT X12

/K_FF_RIGHT_RESET → /RESET (G1, G2 → GND)
K_FF1_XMIT_I2C_SDA → SDA
K_FF1_XMIT_I2C_SCL → SCL
GND → /SELECT
/K_FF1_XMIT_INT → /INT
/K_FF1_XMIT_PRESENT → /PRESENT
VCC_3V3 → 3.3V
VCC_3V3 → 3.3V
VCC_1V8 → 1.8V
GND → GND
<Implementation>

VCC_3V3: L19 1.0 UH 1008; C707 22 UF 0603; C675 0.1 UF 0402; C639 22 UF 0603; C597 0.1 UF 0402
L17 1.0 UH 1008; C637 22 UF 0603; C595 0.1 UF 0402
VCC_1V8: L18 1.0 UH 1008; C713 22 UF 0603; C676 0.1 UF 0402; C638 22 UF 0603; C596 0.1 UF 0402

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U108-2
FIREFLY_XMIT_X12
FIREFLY XMIT X12

B19 GND_B19 / A19 GND_A19	0P / 0N	B18 pK_FF1_XMIT0	B17 nK_FF1_XMIT0
	1P / 1N	A18 pK_FF1_XMIT1	A17 nK_FF1_XMIT1
B16 GND_B16 / A16 GND_A16	2P / 2N	B15 pK_FF1_XMIT2	B14 nK_FF1_XMIT2
	3P / 3N	A15 pK_FF1_XMIT3	A14 nK_FF1_XMIT3
B13 GND_B13 / A13 GND_A13	4P / 4N	B12 pK_FF1_XMIT4	B11 nK_FF1_XMIT4
	5P / 5N	A12 pK_FF1_XMIT5	A11 nK_FF1_XMIT5
B10 GND_B10 / A10 GND_A10	6P / 6N	B9 pK_FF1_XMIT6	B8 nK_FF1_XMIT6
	7P / 7N	A9 pK_FF1_XMIT7	A8 nK_FF1_XMIT7
B7 GND_B7 / A7 GND_A7	8P / 8N	B6 pK_FF1_XMIT8	B5 nK_FF1_XMIT8
	9P / 9N	A6 pK_FF1_XMIT9	A5 nK_FF1_XMIT9
B4 GND_B4 / A4 GND_A4	10P / 10N	B3 pK_FF1_XMIT10	B2 nK_FF1_XMIT10
	11P / 11N	A3 pK_FF1_XMIT11	A2 nK_FF1_XMIT11
B1 GND_B1 / A1 GND_A1			

GND → 1 G1 2 G2 /A95, /A96, /A91, /A92, /A93, /A94

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

VCC_1V8, VCC_3V3
R280 3.3K 0603, R279 3.3K 0603, R277 2.2K 0603, R278 2.2K 0603

U109-1
FIREFLY_RECV_X12
FIREFLY RECV X12

/K_FF_RIGHT_RESET → /RESET (G1, G2 → GND)
K_FF1_RECV_I2C_SDA → SDA
K_FF1_RECV_I2C_SCL → SCL
GND → /SELECT
/K_FF1_RECV_INT → /INT
/K_FF1_RECV_PRESENT → /PRESENT
VCC_3V3 → 3.3V
VCC_3V3 → 3.3V
VCC_1V8 → 1.8V
GND → GND
<Implementation>

POWER FILTERING CIRCUIT

VCC_3V3: L22 1.0 UH 1008; C708 22 UF 0603; C677 0.1 UF 0402; C642 22 UF 0603; C600 0.1 UF 0402
L20 1.0 UH 1008; C640 22 UF 0603; C598 0.1 UF 0402
VCC_1V8: L21 1.0 UH 1008; C714 22 UF 0603; C678 0.1 UF 0402; C641 22 UF 0603; C599 0.1 UF 0402

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

U109-2
FIREFLY_RECV_X12
FIREFLY RECV X12

B19 GND_B19 / A19 GND_A19	0P / 0N	A18 pK_FF1_RECV0	A17 nK_FF1_RECV0
	1P / 1N	B18 pK_FF1_RECV1	B17 nK_FF1_RECV1
B16 GND_B16 / A16 GND_A16	2P / 2N	A15 pK_FF1_RECV2	A14 nK_FF1_RECV2
	3P / 3N	B15 pK_FF1_RECV3	B14 nK_FF1_RECV3
B13 GND_B13 / A13 GND_A13	4P / 4N	A12 pK_FF1_RECV4	A11 nK_FF1_RECV4
	5P / 5N	B12 pK_FF1_RECV5	B11 nK_FF1_RECV5
B10 GND_B10 / A10 GND_A10	6P / 6N	A9 pK_FF1_RECV6	A8 nK_FF1_RECV6
	7P / 7N	B9 pK_FF1_RECV7	B8 nK_FF1_RECV7
B7 GND_B7 / A7 GND_A7	8P / 8N	A6 pK_FF1_RECV8	A5 nK_FF1_RECV8
	9P / 9N	B6 pK_FF1_RECV9	B5 nK_FF1_RECV9
B4 GND_B4 / A4 GND_A4	10P / 10N	A3 pK_FF1_RECV10	A2 nK_FF1_RECV10
	11P / 11N	B3 pK_FF1_RECV11	B2 nK_FF1_RECV11
B1 GND_B1 / A1 GND_A1			

GND → 1 G1 2 G2 /A95, /A96, /A97, /A98, /A99, /A100

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

pK_FF1_RECV0	R4	nK_FF1_RECV0	R3
pK_FF1_XMIT0	R8	nK_FF1_XMIT0	R7
pK_FF1_RECV1	P2	nK_FF1_RECV1	P1
pK_FF1_XMIT1	P6	nK_FF1_XMIT1	P5
pK_FF1_RECV2	N4	nK_FF1_RECV2	N3
pK_FF1_XMIT2	N8	nK_FF1_XMIT2	N7
pK_FF1_RECV3	M2	nK_FF1_RECV3	M1
pK_FF1_XMIT3	M6	nK_FF1_XMIT3	M5

MGTHRXP0_H MGTHRXN0_H
MGTHTXP0_H MGTHTXN0_H
MGTHRXP1_H MGTHRXN1_H
MGTHTXP1_H MGTHTXN1_H
MGTHRXP2_H MGTHRXN2_H
MGTHTXP2_H MGTHTXN2_H
MGTHRXP3_H MGTHRXN3_H
MGTHTXP3_H MGTHTXN3_H

pK_FF1_RECV4	L4	nK_FF1_RECV4	L3
pK_FF1_XMIT4	L8	nK_FF1_XMIT4	L7
pK_FF1_RECV5	K2	nK_FF1_RECV5	K1
pK_FF1_XMIT5	K6	nK_FF1_XMIT5	K5
pK_FF1_RECV6	J4	nK_FF1_RECV6	J3
pK_FF1_XMIT6	J8	nK_FF1_XMIT6	J7
pK_FF1_RECV7	H2	nK_FF1_RECV7	H1
pK_FF1_XMIT7	H6	nK_FF1_XMIT7	H5

MGTHRXP0_I MGTHRXN0_I
MGTHTXP0_I MGTHTXN0_I
MGTHRXP1_I MGTHRXN1_I
MGTHTXP1_I MGTHTXN1_I
MGTHRXP2_I MGTHRXN2_I
MGTHTXP2_I MGTHTXN2_I
MGTHRXP3_I MGTHRXN3_I
MGTHTXP3_I MGTHTXN3_I

pK_FF1_RECV8	G4	nK_FF1_RECV8	G3
pK_FF1_XMIT8	H10	nK_FF1_XMIT8	H9
pK_FF1_RECV9	F2	nK_FF1_RECV9	F1
pK_FF1_XMIT9	G8	nK_FF1_XMIT9	G7
pK_FF1_RECV10	E4	nK_FF1_RECV10	E3
pK_FF1_XMIT10	F6	nK_FF1_XMIT10	F5
pK_FF1_RECV11	D2	nK_FF1_RECV11	D1
pK_FF1_XMIT11	F10	nK_FF1_XMIT11	F9

MGTHRXP0_J MGTHRXN0_J
MGTHTXP0_J MGTHTXN0_J
MGTHRXP1_J MGTHRXN1_J
MGTHTXP1_J MGTHTXN1_J
MGTHRXP2_J MGTHRXN2_J
MGTHTXP2_J MGTHTXN2_J
MGTHRXP3_J MGTHRXN3_J
MGTHTXP3_J MGTHTXN3_J

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.04: KU15P QUADS HIJ FIREFLY X12 #1

Size: | Document Number: 6089-103 | Rev: A

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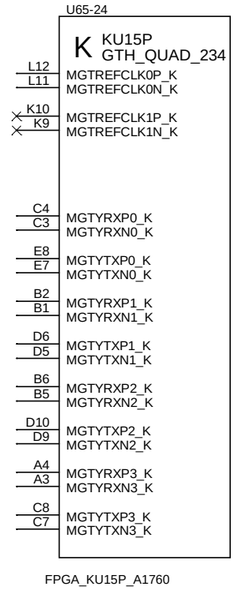
QUAD "K" IS UNUSED



FPGA_KU15P_A1760

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.05: KU15P QUAD K UNUSED

Size	Document Number	Rev
	6089-103	A

Date: Thursday, February 14, 2019 Sheet 54 of 75

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "L" AND "N" ARE CLOCKED FROM QUAD "M"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN4
ac_nK_CLK0_CHAN4
ac_pK_CLK1_CHAN4
ac_nK_CLK1_CHAN4

U65-25
L KU15P GTY_QUAD_127
AG30 MGTREFCLK0P_L
AG31 MGTREFCLK0N_L
AE30 MGTREFCLK1P_L
AE31 MGTREFCLK1N_L

pK_FF7_RECV11 AT41 MGTYRXP0_L
nK_FF7_RECV11 AT42 MGTYRXN0_L
pK_FF7_XMIT11 AM36 MGTYTXP0_L
nK_FF7_XMIT11 AM37 MGTYTXN0_L
pK_FF7_RECV10 AR39 MGTYRXP1_L
nK_FF7_RECV10 AR40 MGTYRXN1_L
pK_FF7_XMIT10 AL34 MGTYTXP1_L
nK_FF7_XMIT10 AL35 MGTYTXN1_L
pK_FF7_RECV9 AP41 MGTYRXP2_L
nK_FF7_RECV9 AP42 MGTYRXN2_L
pK_FF7_XMIT9 AK36 MGTYTXP2_L
nK_FF7_XMIT9 AK37 MGTYTXN2_L
pK_FF7_RECV8 AN39 MGTYRXP3_L
nK_FF7_RECV8 AN40 MGTYRXN3_L
pK_FF7_XMIT8 AJ34 MGTYTXP3_L
nK_FF7_XMIT8 AJ35 MGTYTXN3_L

FPGA_KU15P_A1760

U65-26
M KU15P GTY_QUAD_128
AD32 MGTREFCLK0P_M
AD33 MGTREFCLK0N_M
AC30 MGTREFCLK1P_M
AC31 MGTREFCLK1N_M

pK_FF7_RECV7 AM41 MGTYRXP0_M
nK_FF7_RECV7 AM42 MGTYRXN0_M
pK_FF7_XMIT7 AH32 MGTYTXP0_M
nK_FF7_XMIT7 AH33 MGTYTXN0_M
pK_FF7_RECV6 AL39 MGTYRXP1_M
nK_FF7_RECV6 AL40 MGTYRXN1_M
pK_FF7_XMIT6 AH36 MGTYTXP1_M
nK_FF7_XMIT6 AH37 MGTYTXN1_M
pK_FF7_RECV5 AK41 MGTYRXP2_M
nK_FF7_RECV5 AK42 MGTYRXN2_M
pK_FF7_XMIT5 AG34 MGTYTXP2_M
nK_FF7_XMIT5 AG35 MGTYTXN2_M
pK_FF7_RECV4 AJ39 MGTYRXP3_M
nK_FF7_RECV4 AJ40 MGTYRXN3_M
pK_FF7_XMIT4 AF32 MGTYTXP3_M
nK_FF7_XMIT4 AF33 MGTYTXN3_M

FPGA_KU15P_A1760

U65-27
N KU15P GTY_QUAD_129
AB32 MGTREFCLK0P_N
AB33 MGTREFCLK0N_N
AA30 MGTREFCLK1P_N
AA31 MGTREFCLK1N_N

pK_FF7_RECV3 AH41 MGTYRXP0_N
nK_FF7_RECV3 AH42 MGTYRXN0_N
pK_FF7_XMIT3 AF36 MGTYTXP0_N
nK_FF7_XMIT3 AF37 MGTYTXN0_N
pK_FF7_RECV2 AG39 MGTYRXP1_N
nK_FF7_RECV2 AG40 MGTYRXN1_N
pK_FF7_XMIT2 AE34 MGTYTXP1_N
nK_FF7_XMIT2 AE35 MGTYTXN1_N
pK_FF7_RECV1 AF41 MGTYRXP2_N
nK_FF7_RECV1 AF42 MGTYRXN2_N
pK_FF7_XMIT1 AD36 MGTYTXP2_N
nK_FF7_XMIT1 AD37 MGTYTXN2_N
pK_FF7_RECV0 AE39 MGTYRXP3_N
nK_FF7_RECV0 AE40 MGTYRXN3_N
pK_FF7_XMIT0 AC34 MGTYTXP3_N
nK_FF7_XMIT0 AC35 MGTYTXN3_N

FPGA_KU15P_A1760

VCC_1V8 VCC_3V3
R601 3.3K 0603
R602 3.3K 0603
R603 2.2K 0603
R604 2.2K 0603

U20-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

/K_FF_LEFT_RESET → 6 /RESET
K_FF7_XMIT_I2C_SDA → 7 SDA
K_FF7_XMIT_I2C_SCL → 8 SCL
GND → 4 /SELECT
/K_FF7_XMIT_INT → 5 /INT
/K_FF7_XMIT_PRESENT → 3 /PRESENT
G1 G2 → GND

VCC_3V3 → 1 3.3V
L47 1.0 UH 1008
C847 22 UF 0603
C860 0.1 UF 0402
C884 22 UF 0603
C920 0.1 UF 0402

10 3.3V
L49 1.0 UH 1008
C886 22 UF 0603
C922 0.1 UF 0402

VCC_1V8 → 9 1.8V
L48 1.0 UH 1008
C836 22 UF 0603
C859 0.1 UF 0402
C885 22 UF 0603
C921 0.1 UF 0402

GND → 2 GND

<Implementation>

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U20-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

B19 A19	GND_B19 GND_A19	0P 0N	B18 A18	pK_FF7_XMIT0 nK_FF7_XMIT0
		1P 1N	B17 A17	pK_FF7_XMIT1 nK_FF7_XMIT1
B16 A16	GND_B16 GND_A16	2P 2N	B15 A15	pK_FF7_XMIT2 nK_FF7_XMIT2
		3P 3N	B14 A14	pK_FF7_XMIT3 nK_FF7_XMIT3
B13 A13	GND_B13 GND_A13	4P 4N	B12 A12	pK_FF7_XMIT4 nK_FF7_XMIT4
		5P 5N	B11 A11	pK_FF7_XMIT5 nK_FF7_XMIT5
B10 A10	GND_B10 GND_A10	6P 6N	B9 A9	pK_FF7_XMIT6 nK_FF7_XMIT6
		7P 7N	B8 A8	pK_FF7_XMIT7 nK_FF7_XMIT7
B7 A7	GND_B7 GND_A7	8P 8N	B6 A6	pK_FF7_XMIT8 nK_FF7_XMIT8
		9P 9N	B5 A5	pK_FF7_XMIT9 nK_FF7_XMIT9
B4 A4	GND_B4 GND_A4	10P 10N	B3 A3	pK_FF7_XMIT10 nK_FF7_XMIT10
		11P 11N	B2 A2	pK_FF7_XMIT11 nK_FF7_XMIT11
B1 A1	GND_B1 GND_A1			

GND VA4 VA3 VA2 VA1 VA0

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

VCC_1V8 VCC_3V3
R605 3.3K 0603
R606 3.3K 0603
R607 2.2K 0603
R608 2.2K 0603

U21-1 FIREFLY_RECV_X12 FIREFLY RECV X12

/K_FF_LEFT_RESET → 6 /RESET
K_FF7_RECV_I2C_SDA → 7 SDA
K_FF7_RECV_I2C_SCL → 8 SCL
GND → 4 /SELECT
/K_FF7_RECV_INT → 5 /INT
/K_FF7_RECV_PRESENT → 3 /PRESENT
G1 G2 → GND

VCC_3V3 → 1 3.3V
L50 1.0 UH 1008
C848 22 UF 0603
C862 0.1 UF 0402
C887 22 UF 0603
C923 0.1 UF 0402

10 3.3V
L52 1.0 UH 1008
C889 22 UF 0603
C925 0.1 UF 0402

POWER FILTERING CIRCUIT

VCC_1V8 → 9 1.8V
L51 1.0 UH 1008
C837 22 UF 0603
C861 0.1 UF 0402
C888 22 UF 0603
C924 0.1 UF 0402

GND → 2 GND

<Implementation>

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
0x54 = 7 BIT ADDRESS
0xA8 = 8 BIT WRITE ADDRESS
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

U21-2 FIREFLY_RECV_X12 FIREFLY RECV X12

B19 A19	GND_B19 GND_A19	0P 0N	A18 A17	pK_FF7_RECV0 nK_FF7_RECV0
		1P 1N	B18 B17	pK_FF7_RECV1 nK_FF7_RECV1
B16 A16	GND_B16 GND_A16	2P 2N	A15 A14	pK_FF7_RECV2 nK_FF7_RECV2
		3P 3N	B15 B14	pK_FF7_RECV3 nK_FF7_RECV3
B13 A13	GND_B13 GND_A13	4P 4N	A12 A11	pK_FF7_RECV4 nK_FF7_RECV4
		5P 5N	B12 B11	pK_FF7_RECV5 nK_FF7_RECV5
B10 A10	GND_B10 GND_A10	6P 6N	A9 A8	pK_FF7_RECV6 nK_FF7_RECV6
		7P 7N	B9 B8	pK_FF7_RECV7 nK_FF7_RECV7
B7 A7	GND_B7 GND_A7	8P 8N	A6 A5	pK_FF7_RECV8 nK_FF7_RECV8
		9P 9N	B6 B5	pK_FF7_RECV9 nK_FF7_RECV9
B4 A4	GND_B4 GND_A4	10P 10N	A3 A2	pK_FF7_RECV10 nK_FF7_RECV10
		11P 11N	B3 B2	pK_FF7_RECV11 nK_FF7_RECV11
B1 A1	GND_B1 GND_A1			

GND VA11 VA10 VA9 VA8 VA7 VA6

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.06: KU15P QUADS LMN FIREFLY X12 #7

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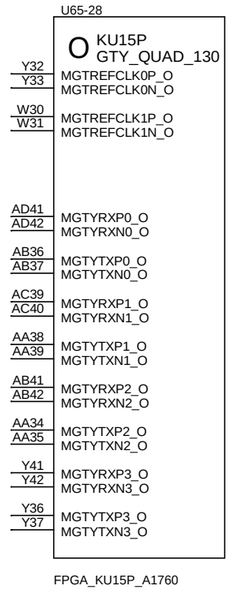
QUAD "O" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.07: KU15P QUAD O UNUSED

Size	Document Number	Rev
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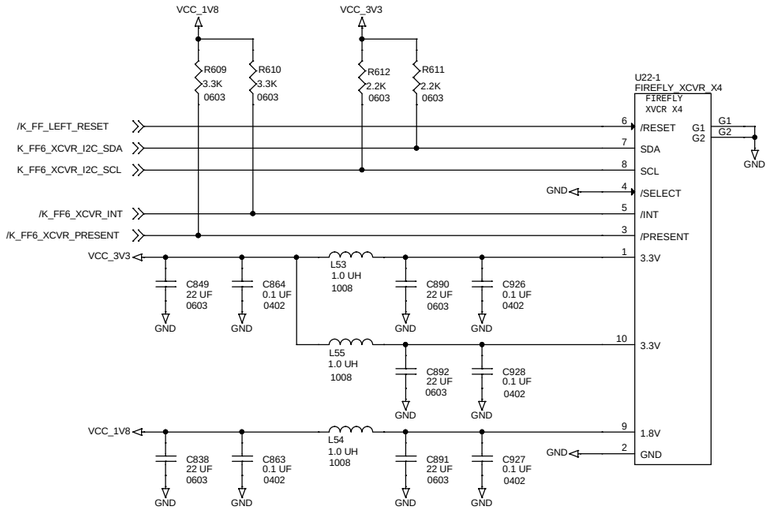
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

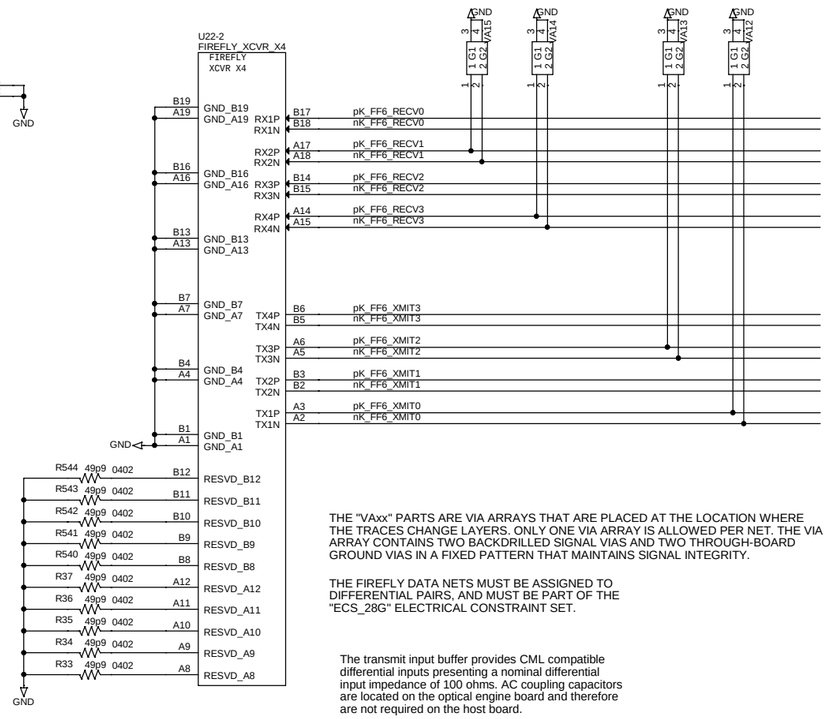
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.08: KU15P QUAD P FIREFLY X4 #6		
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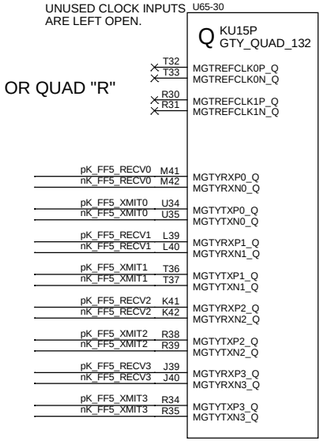
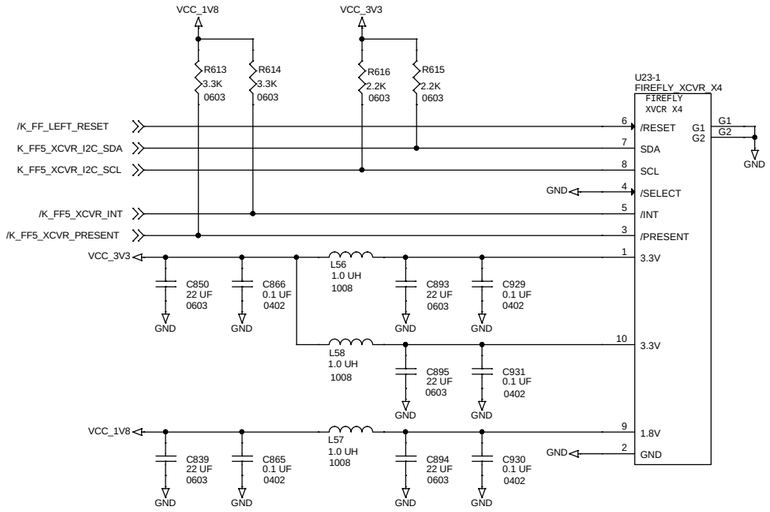
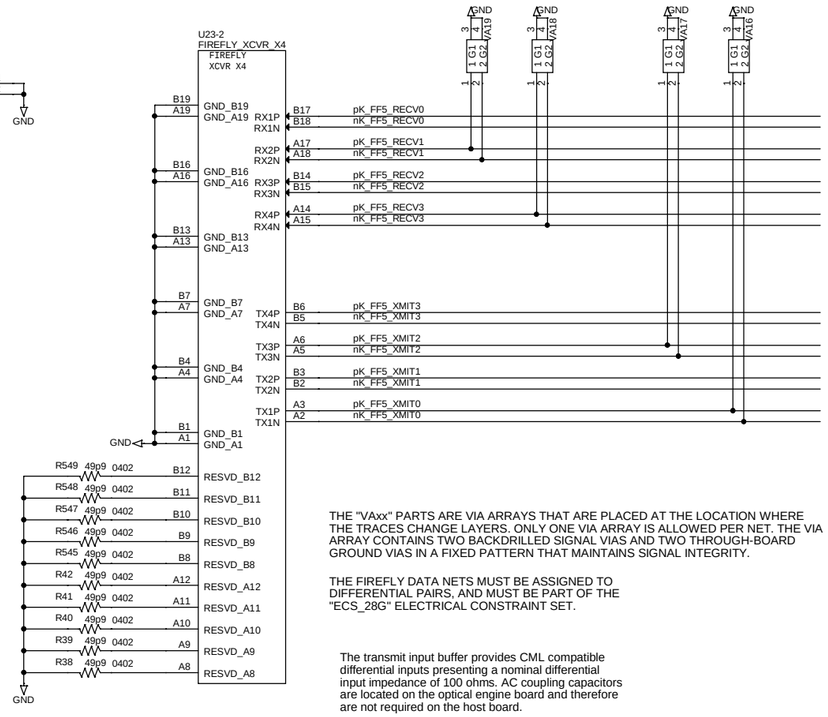
UNUSED CLOCK INPUTS ARE LEFT OPEN.

QUAD "Q" CAN BE CLOCKED FROM QUAD "P" OR QUAD "R"



FPGA_KU15P_A1760





THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.09: KU15P QUAD R FIREFLY X4 #5		
Size	Document Number: 6089-103	Rev: A
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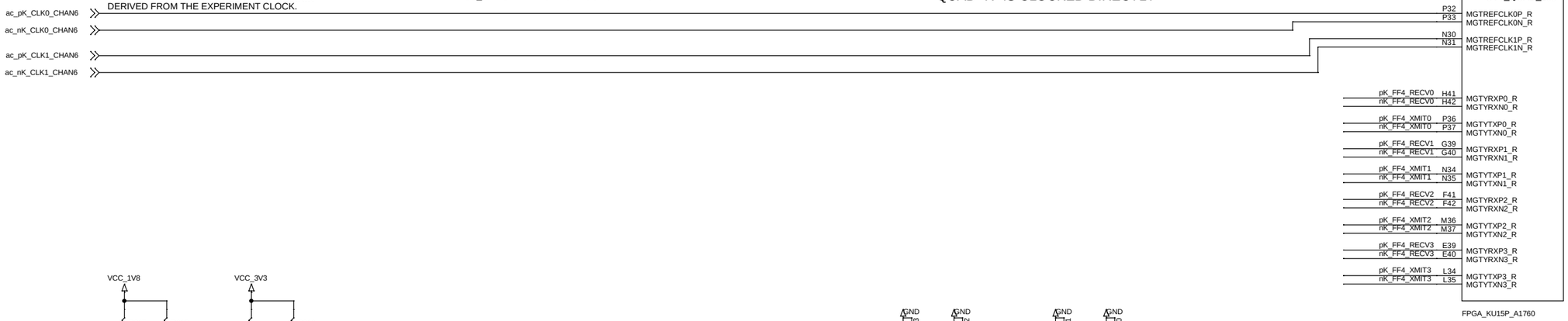
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

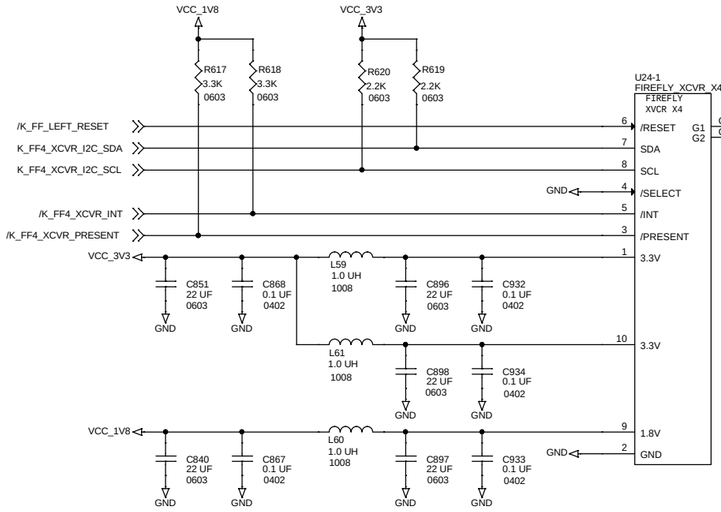
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

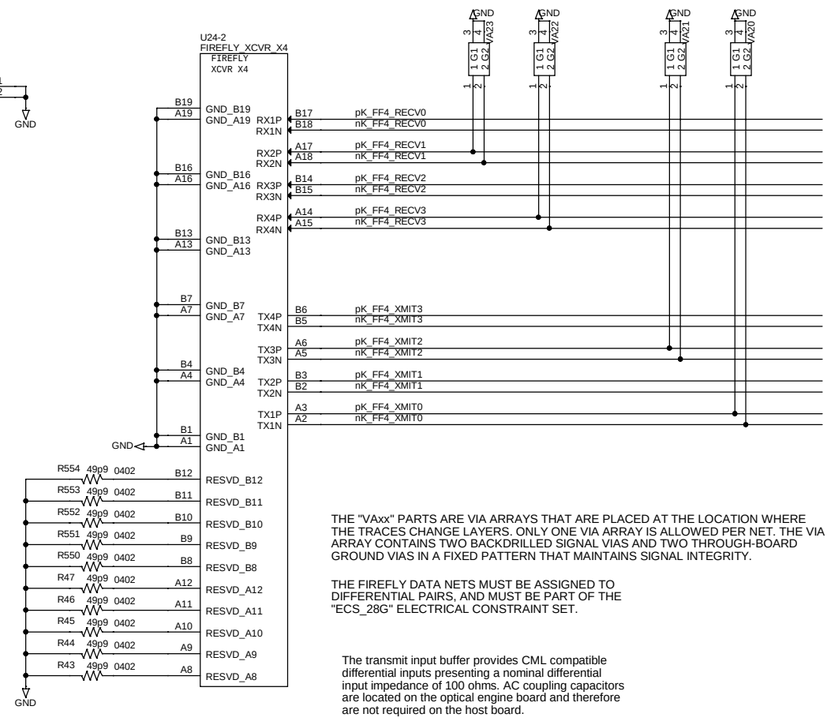
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "R" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1			
Title: 7.10: KU15P QUAD R FIREFLY X4 #4			
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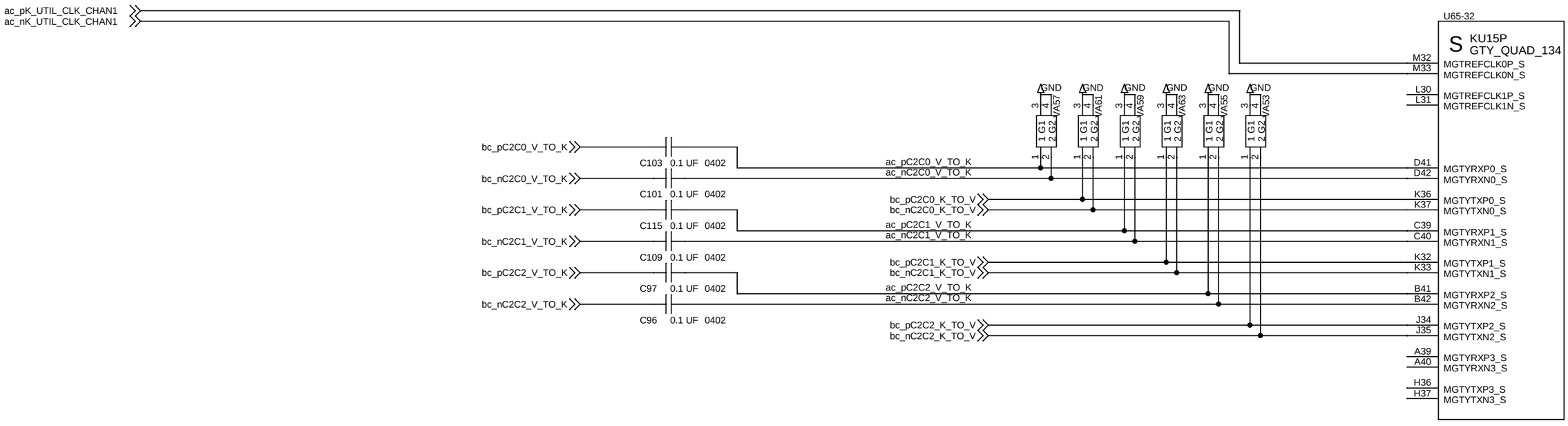
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "S" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

CONNECT UTILITY NETS HERE

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 7.11: KU15P QUAD S CHIP-TO-CHIP		
Size	Document Number: 6089-103	Rev: A
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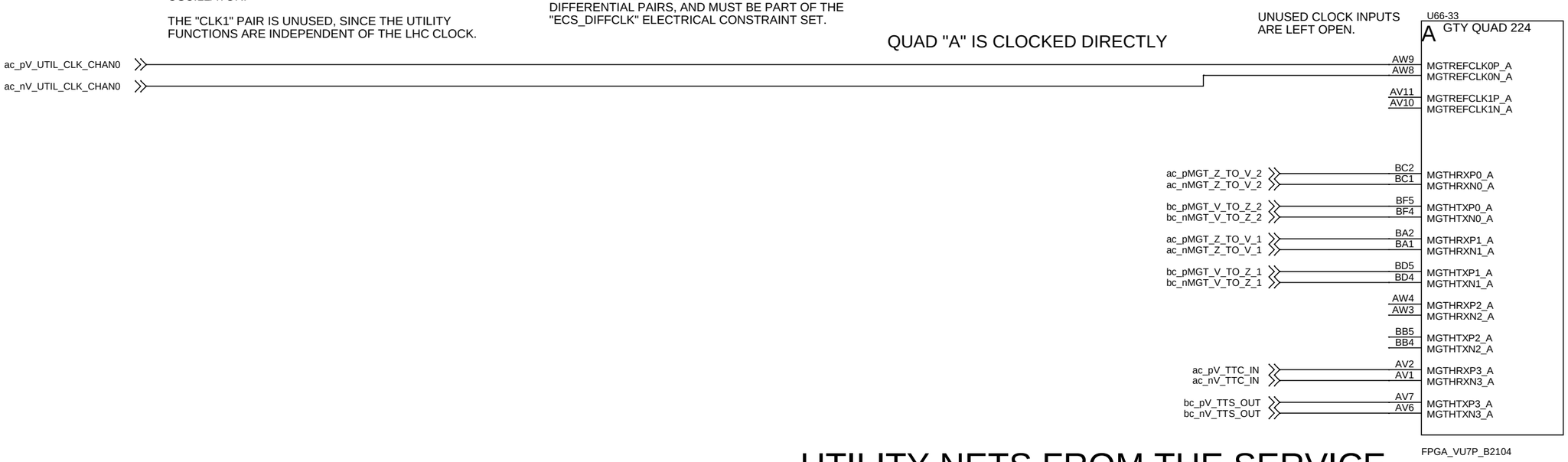
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.01: VU7P QUAD A UTILITY #1		
Size	Document Number: 6089-103	Rev: A
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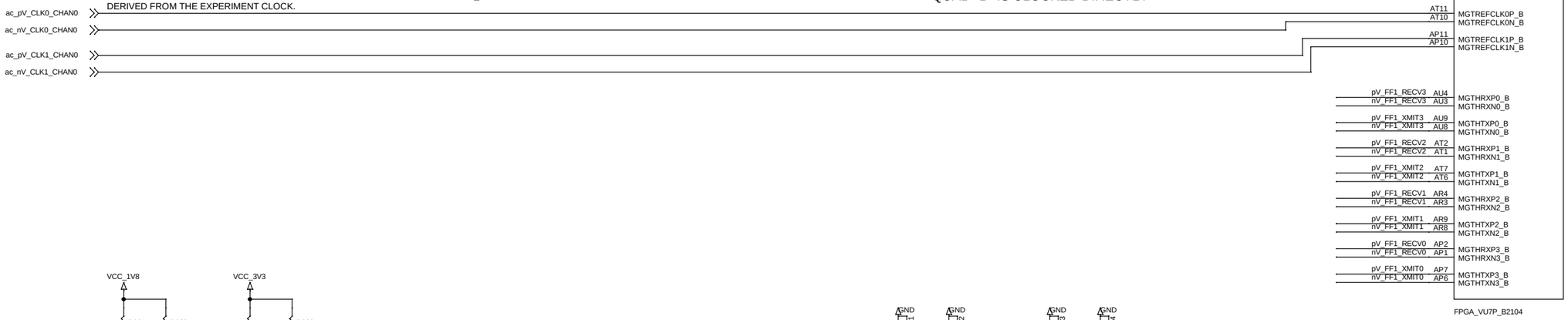
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

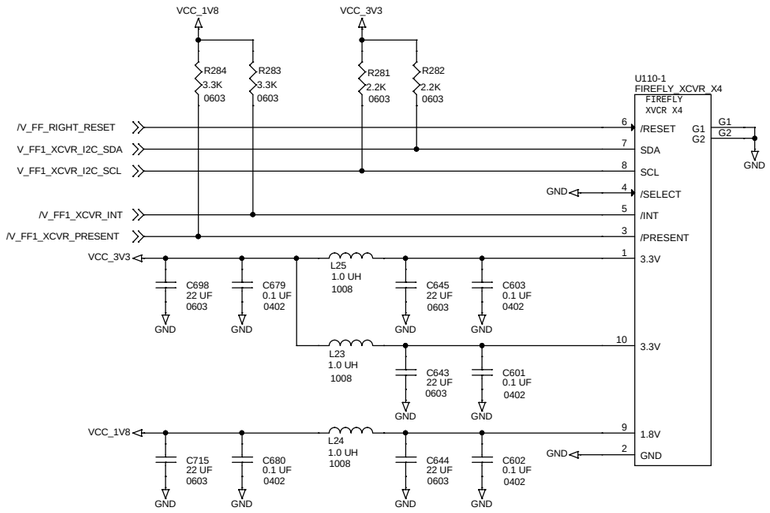
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

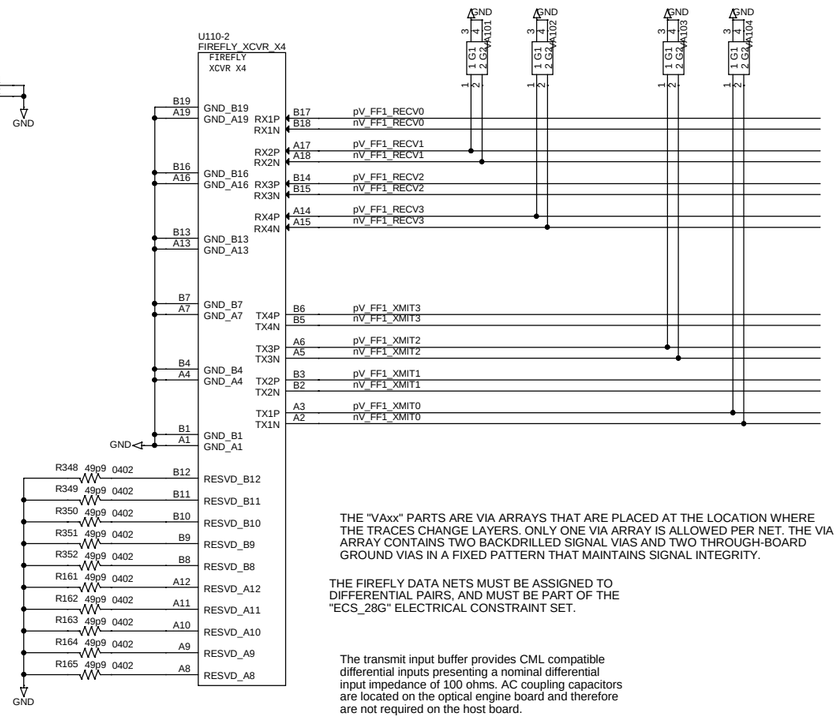
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "B" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.02: VU7P QUAD B FIREFLY X4 #1		
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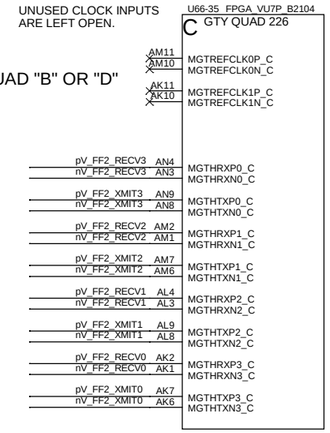
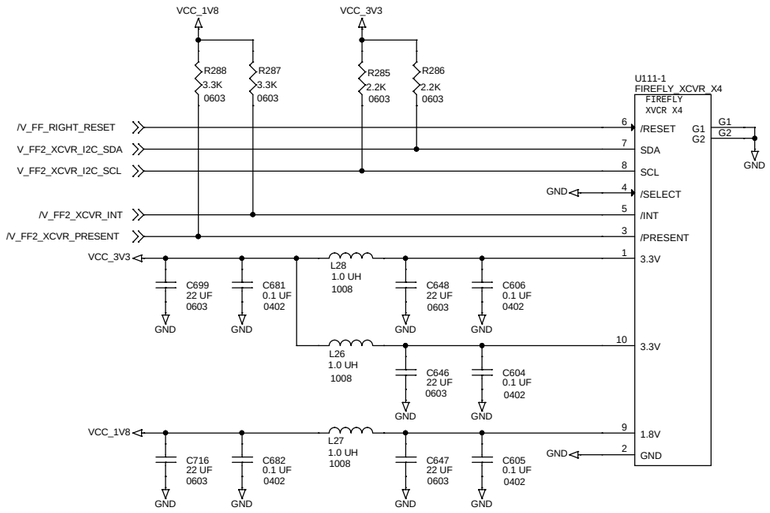
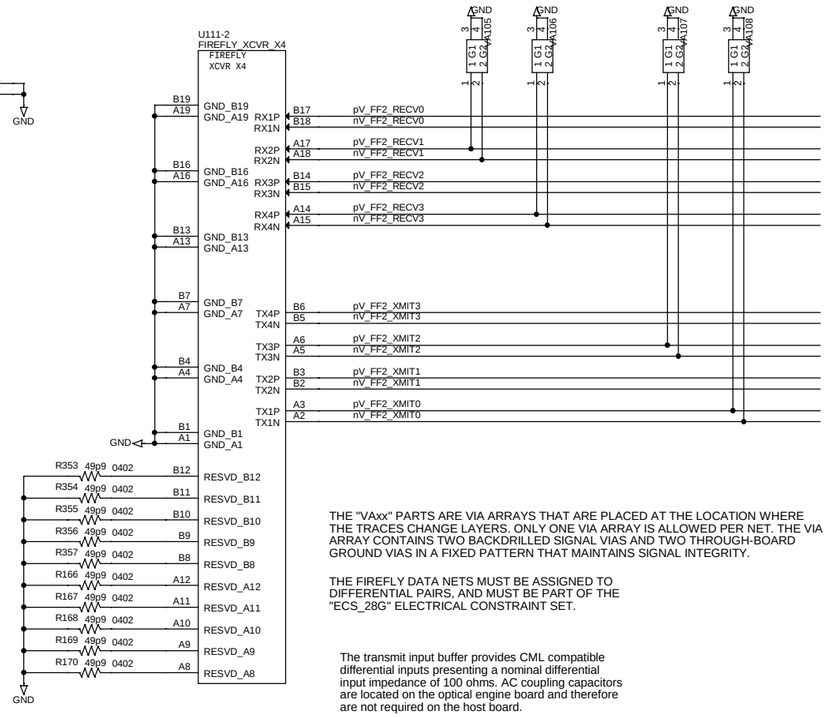
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "C" IS CLOCKED FROM EITHER QUAD "B" OR "D"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.03: VU7P QUAD C FIREFLY X4 #2		
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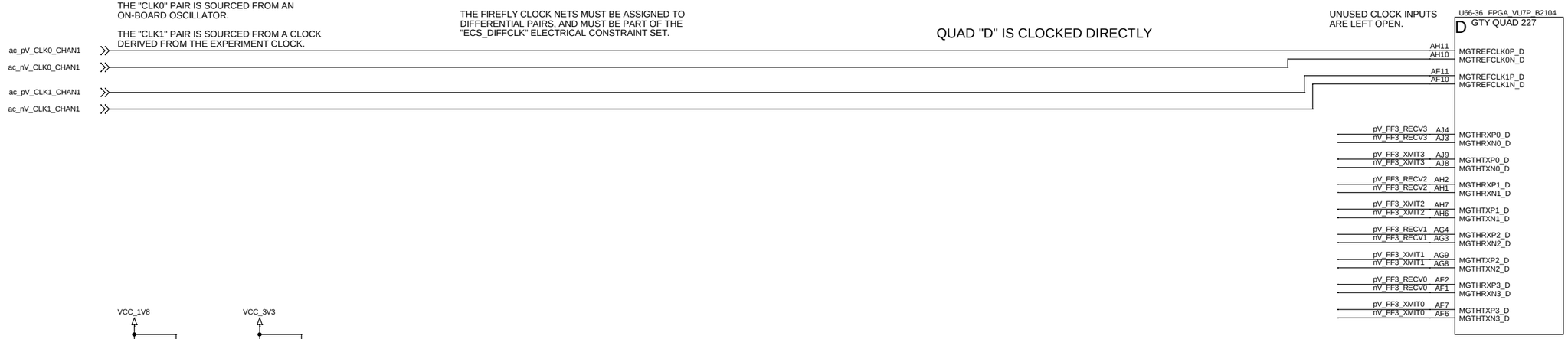
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

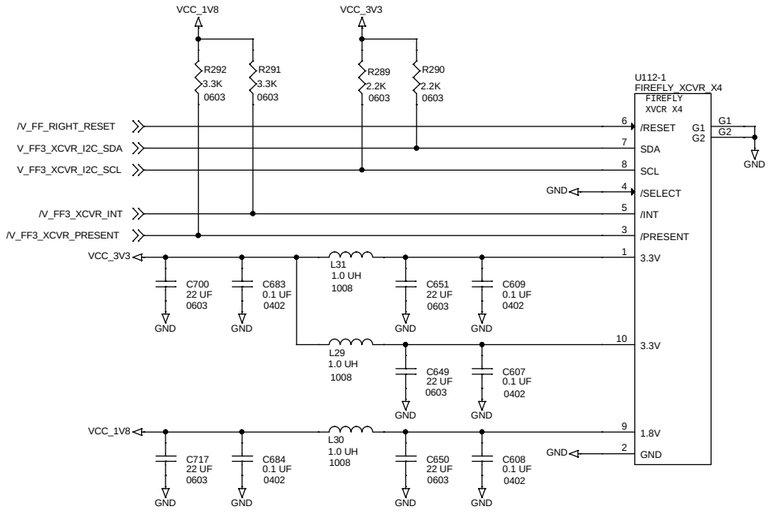
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

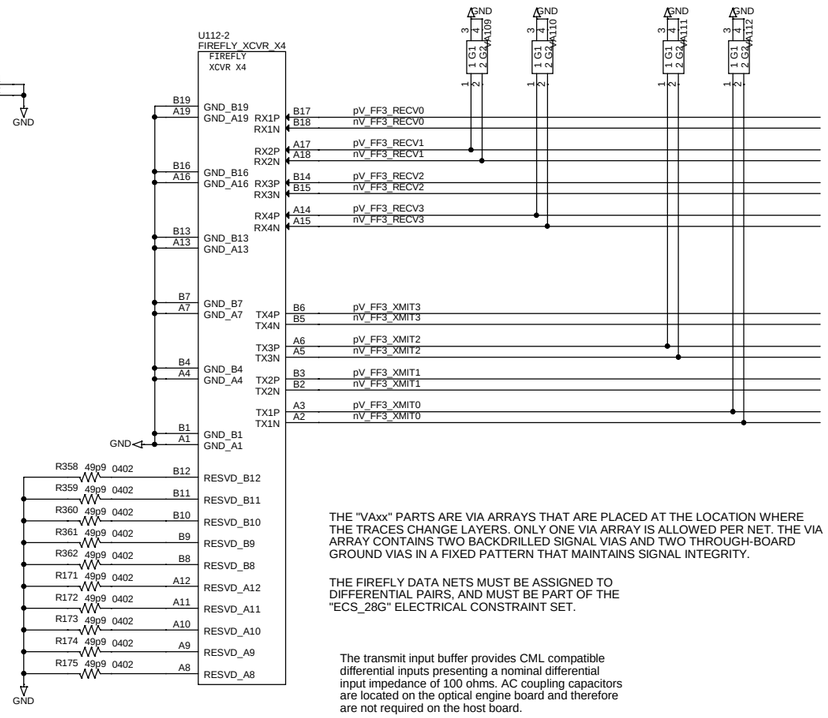
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "D" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.04: VU7P QUAD D FIREFLY X4 #3

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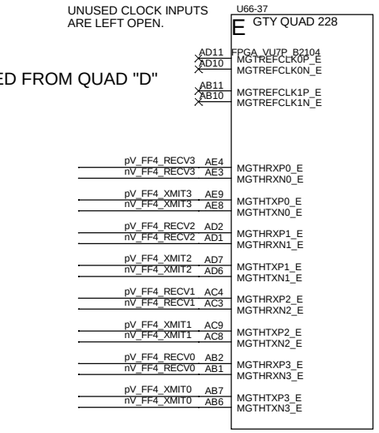
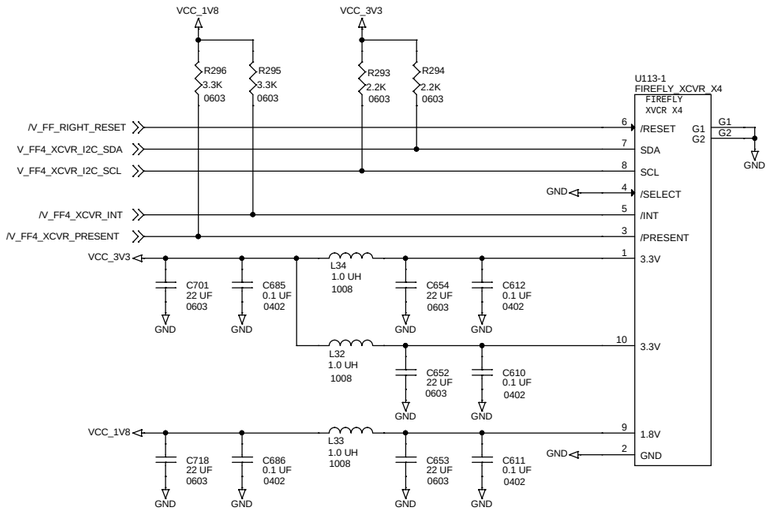
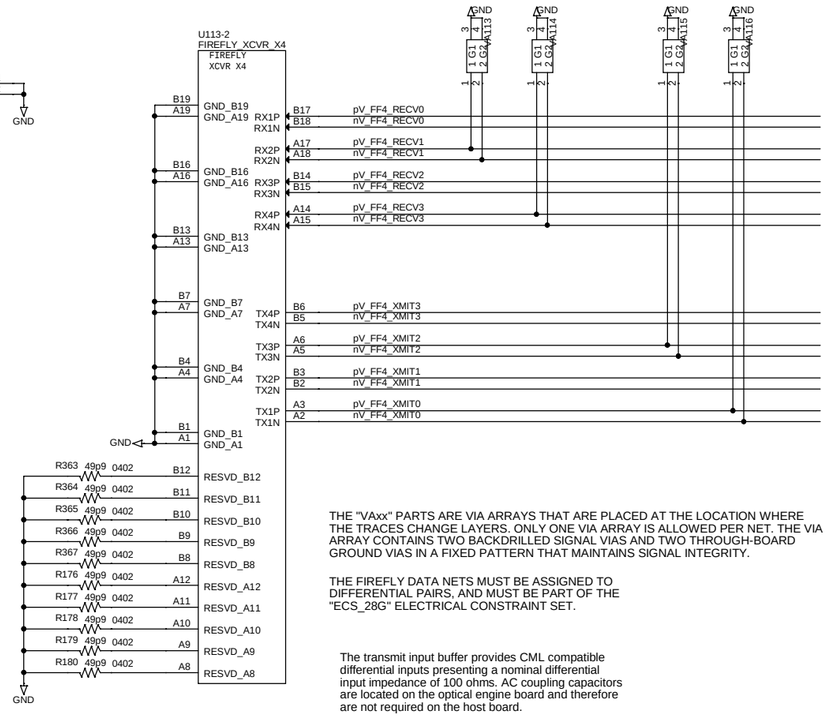
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "E" IS CLOCKED FROM QUAD "D"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.05: VU7P QUAD E FIREFLY X4 #4

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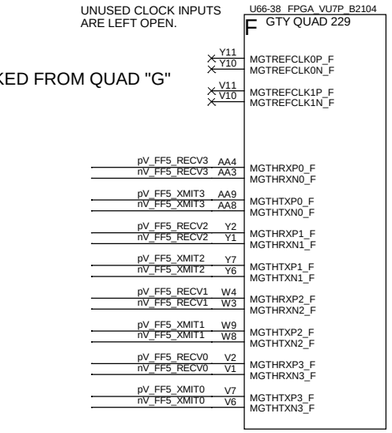
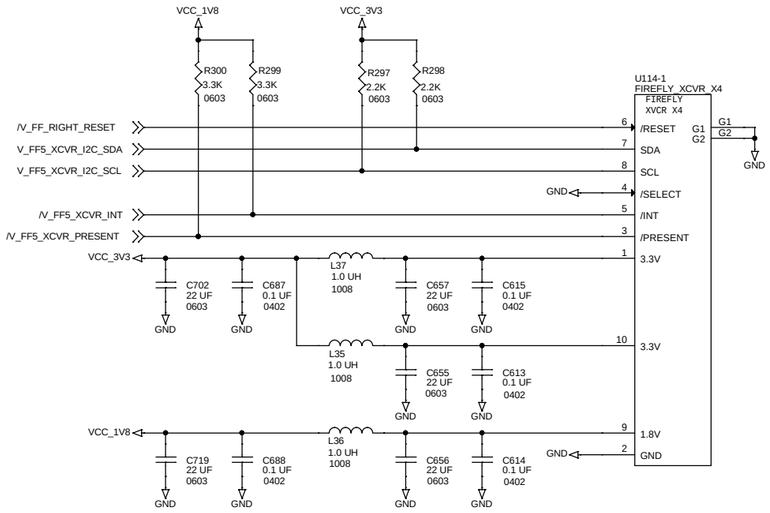
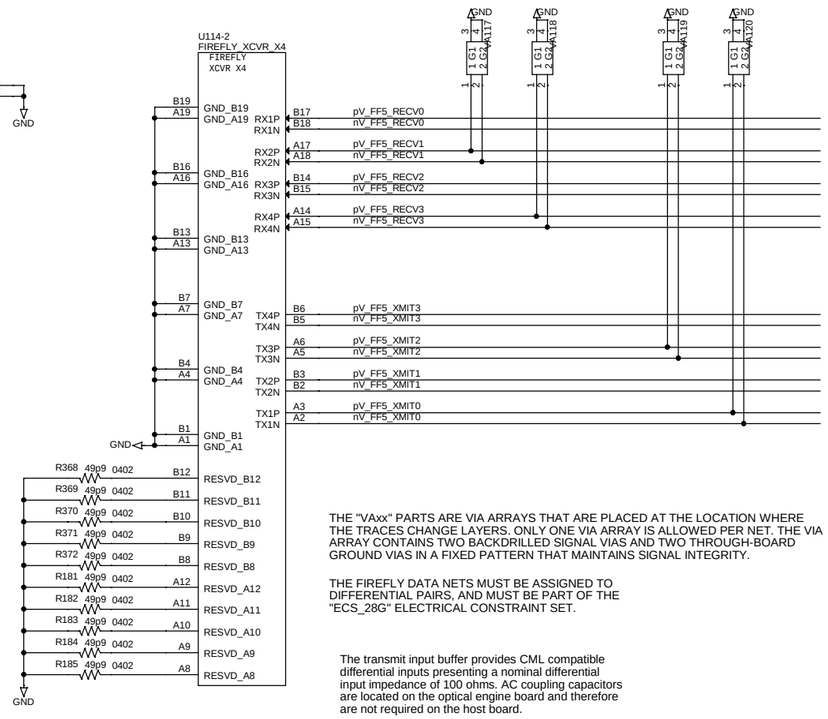
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "F" IS CLOCKED FROM QUAD "G"







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.06: VU7P QUAD F FIREFLY X4 #5

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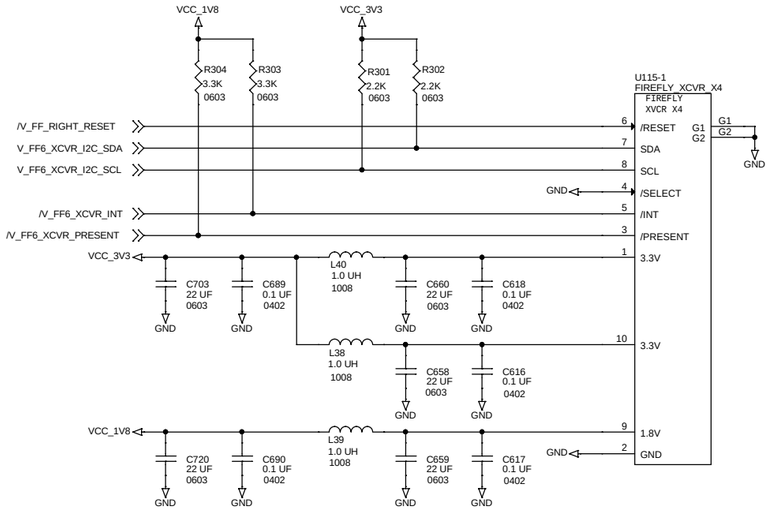
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

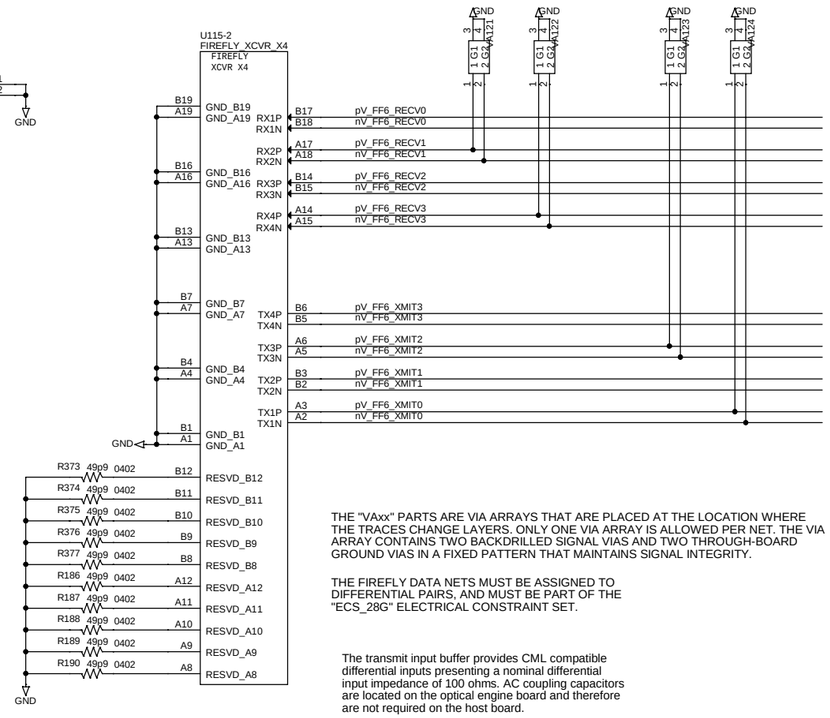
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "G" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.07: VU7P QUAD G FIREFLY X4 #6		
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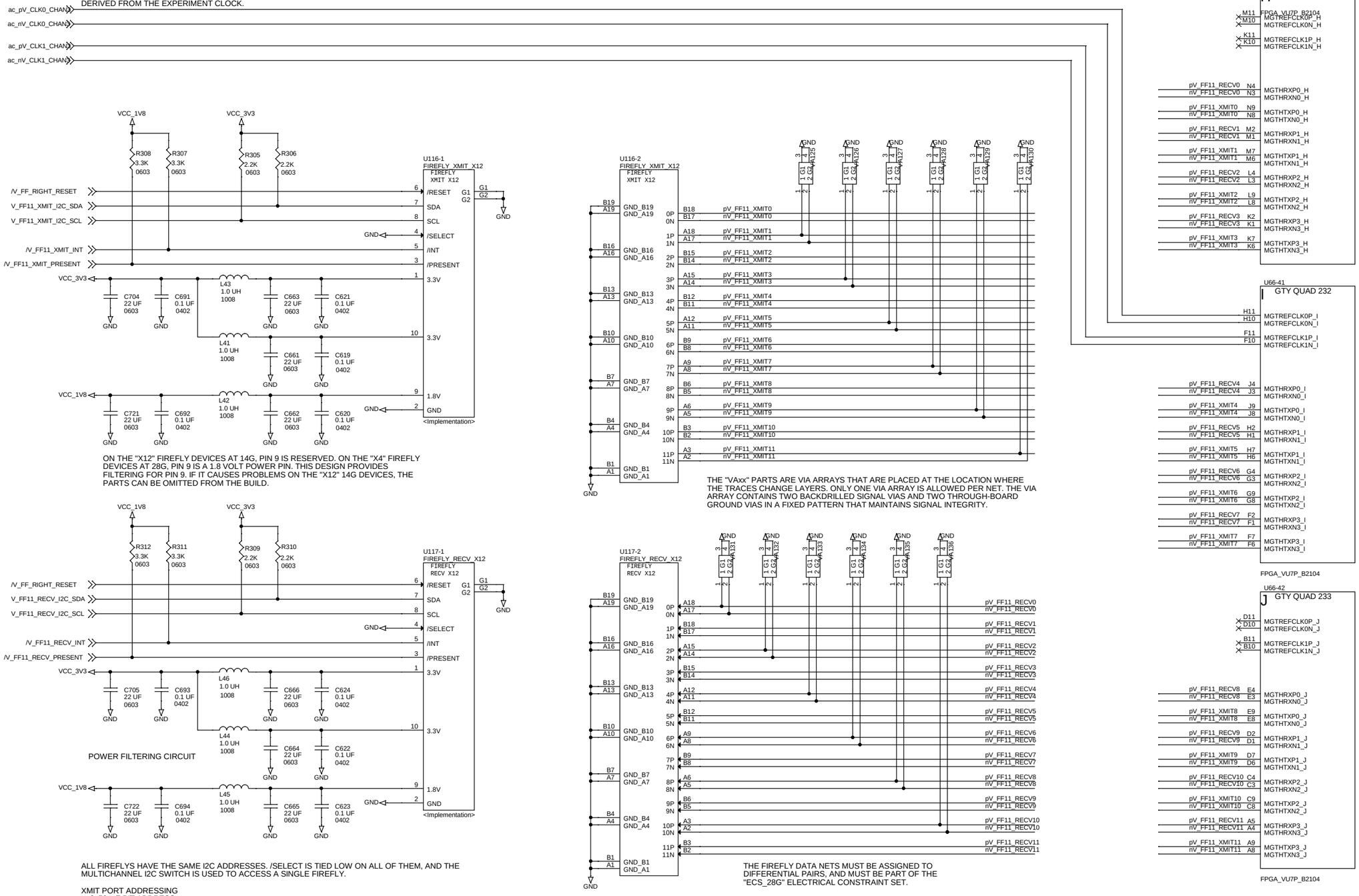
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

POWER FILTERING CIRCUIT

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.08: VU7P QUADS HIJ FIREFLY X12 #11

Size: | Document Number: 6089-103 | Rev: A

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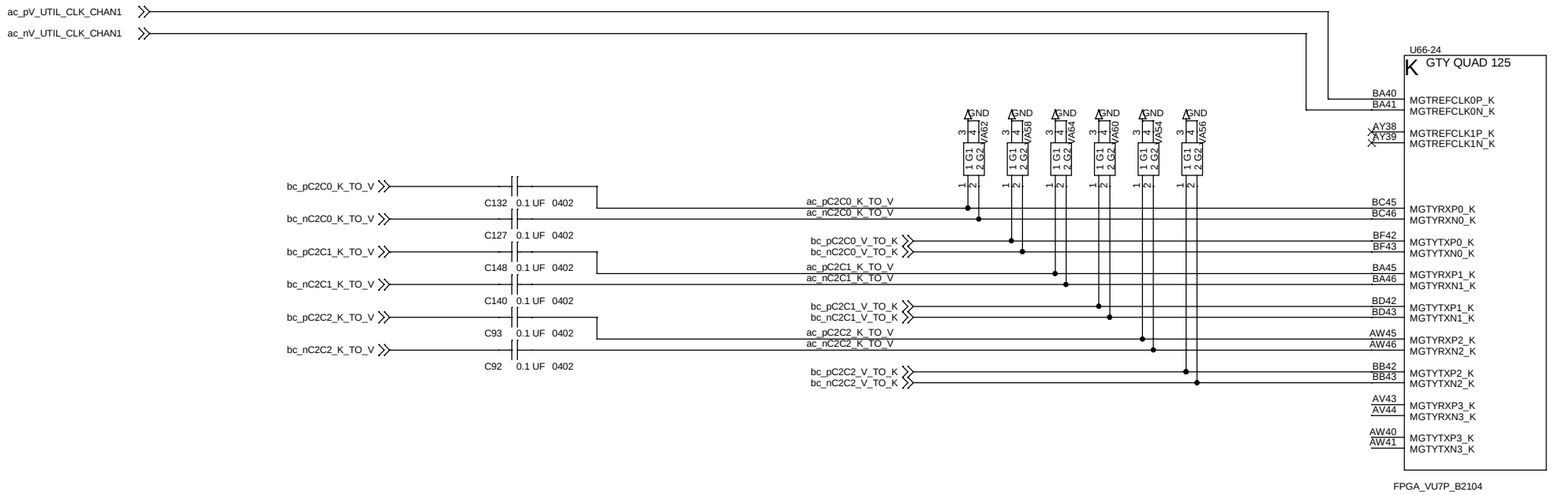
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

QUAD "K" IS CLOCKED DIRECTLY



THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.09: VU7P QUAD K CHIP TO CHIP

Size | Document Number: 6089-103 | Rev: A

Date: Thursday, February 14, 2019 Sheet 69 of 75

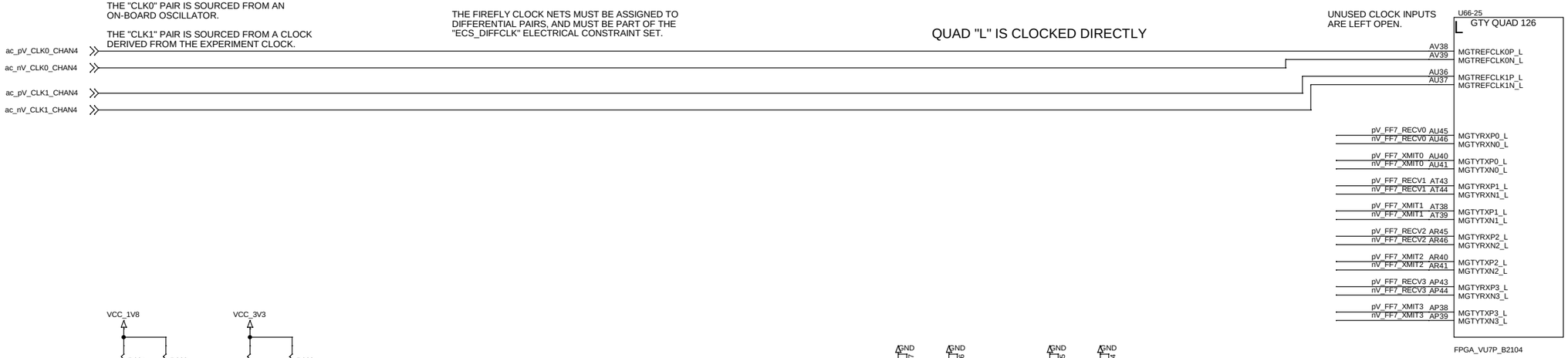
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

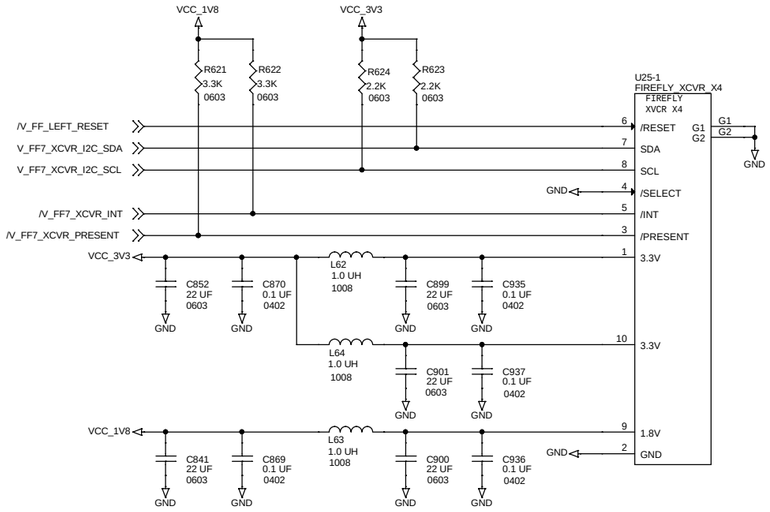
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

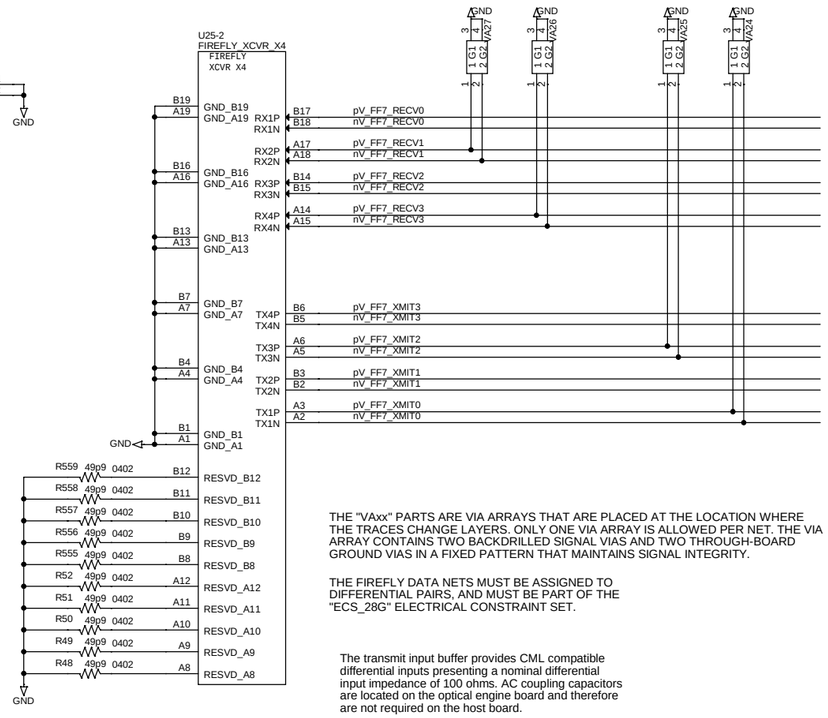
QUAD "L" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.



FPGA_VU7P_B2104





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.10: VU7P QUAD L FIREFLY X4 #7		
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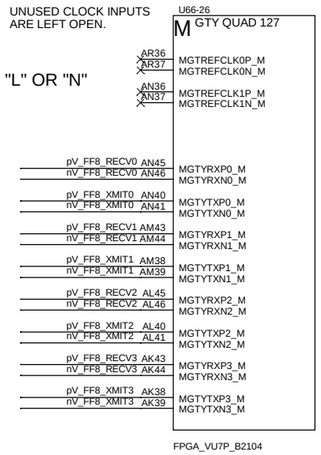
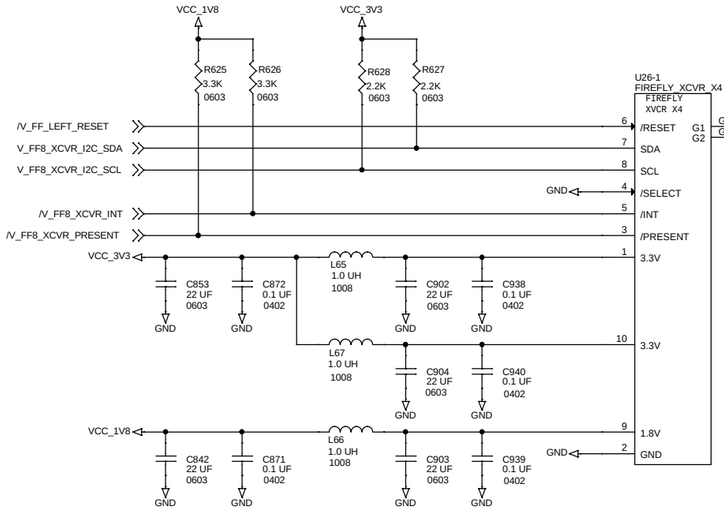
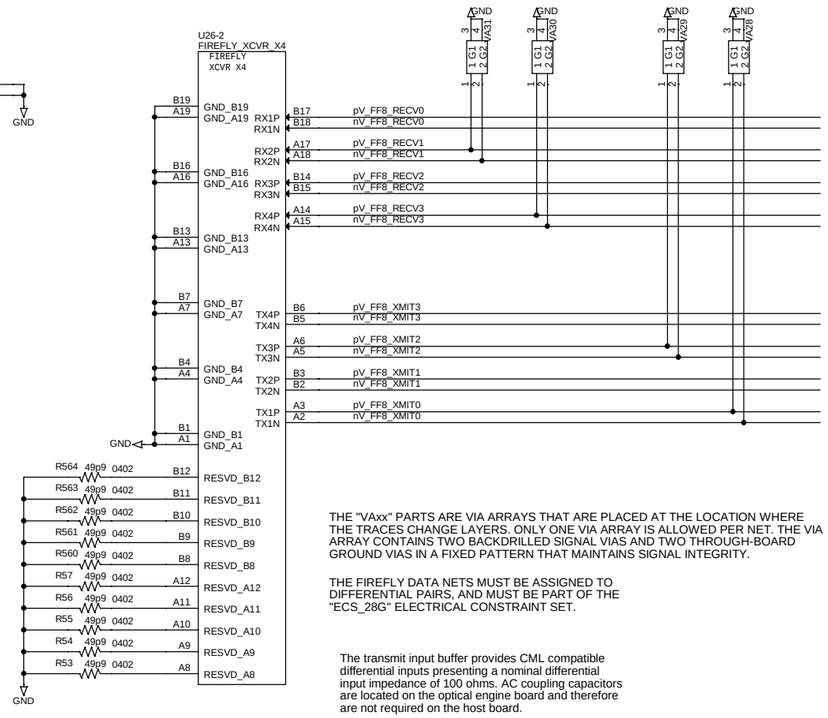
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "M" IS CLOCKED FROM EITHER QUAD "L" OR "N"



FPGA_VU7P_B2104





ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.11: VU7P QUAD M FIREFLY X4 #8

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	6089-103	A

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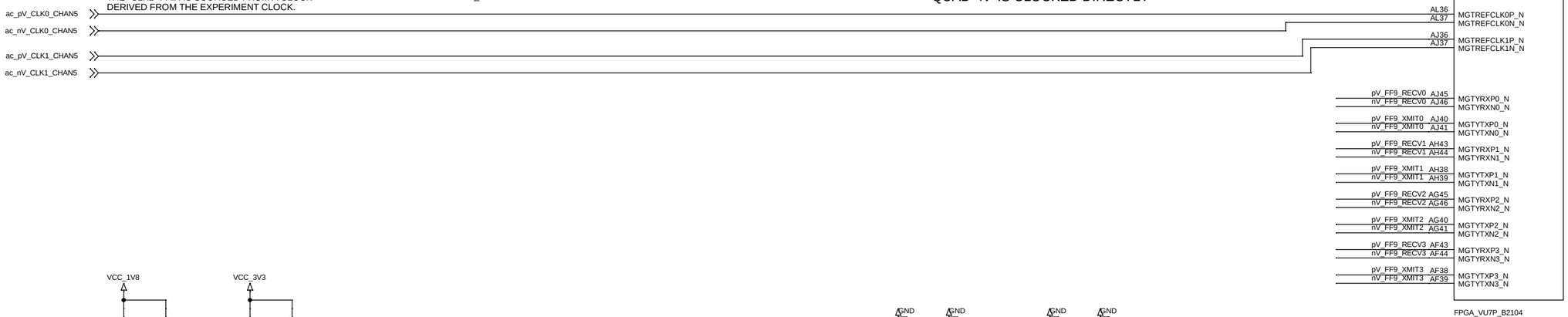
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

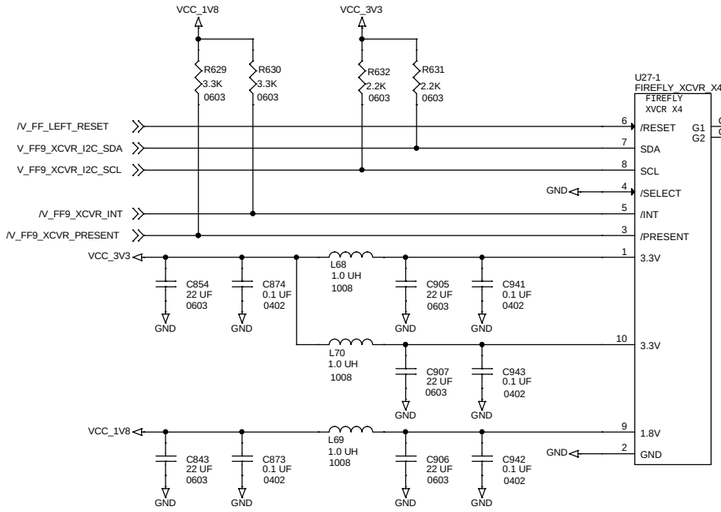
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

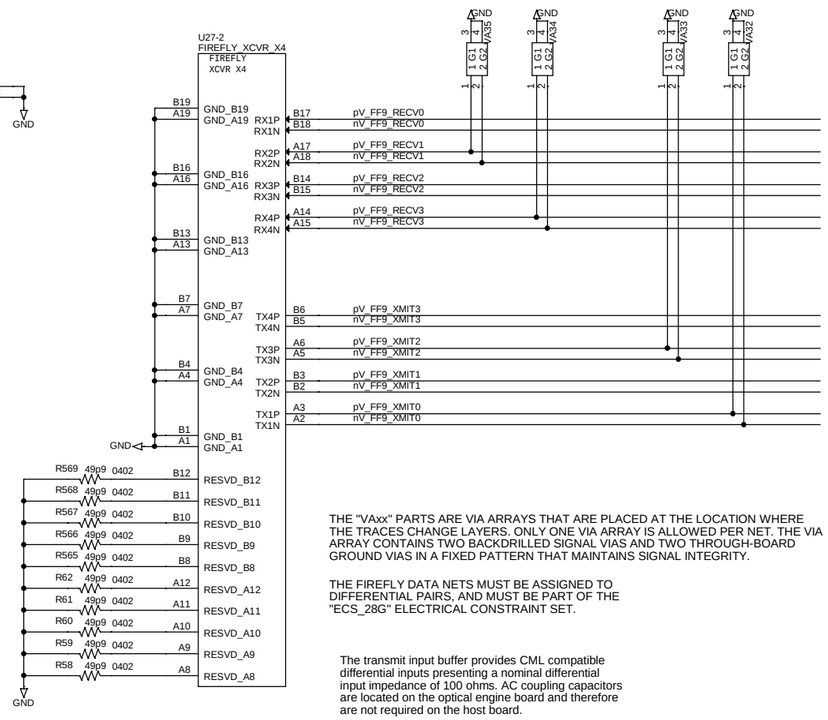
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "N" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.12: VU7P QUAD N FIREFLY X4 #9		
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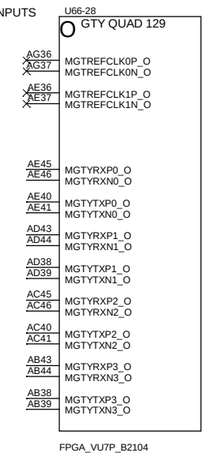
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "O" IS UNUSED



ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.13: VU7P QUAD O UNUSED

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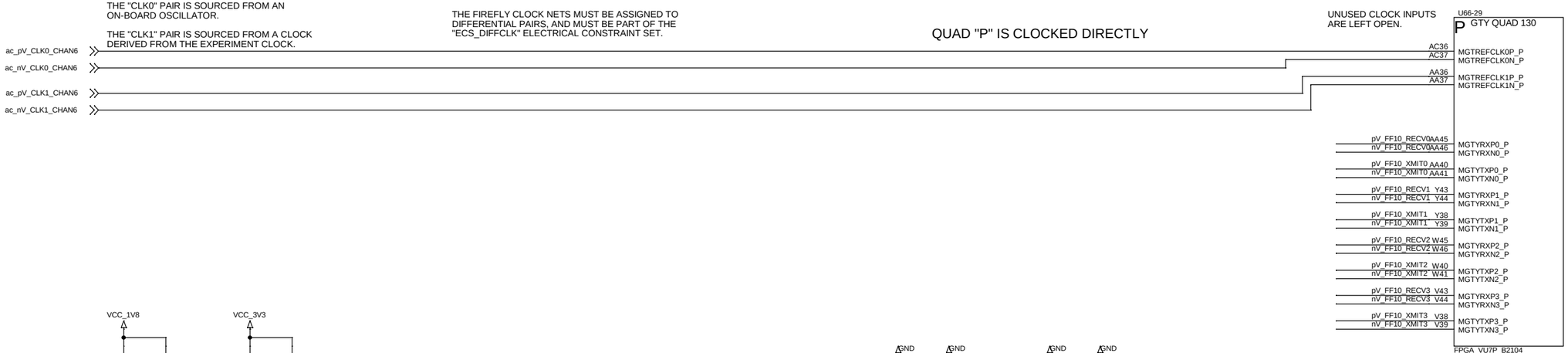
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

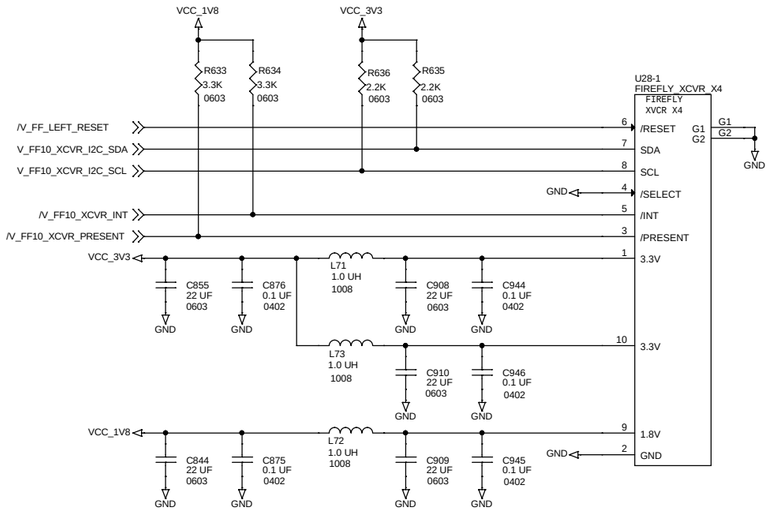
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

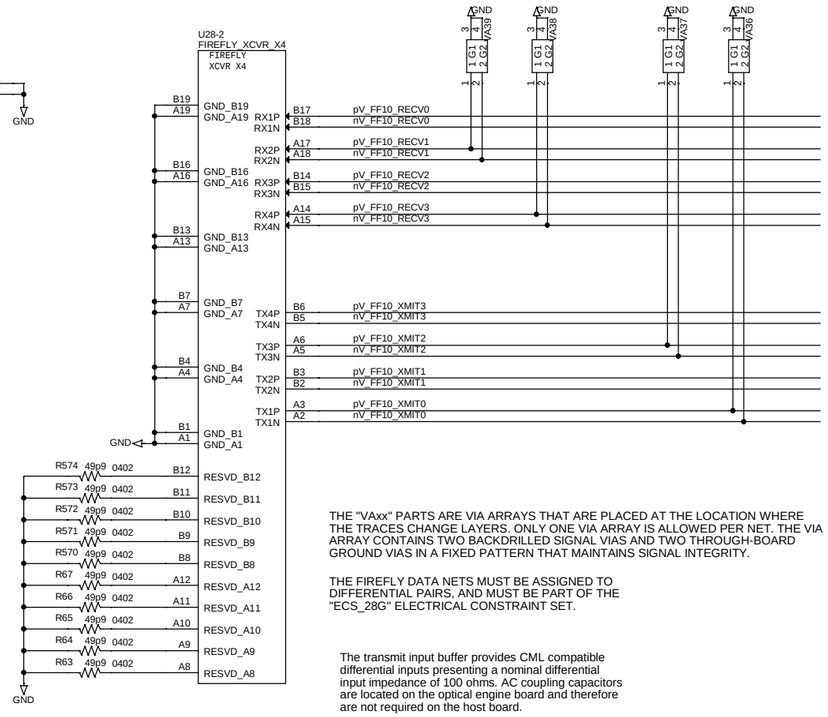
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1		
Title: 8.14: VU7P QUAD P FIREFLY X4 #10		
Size	Document Number: 6089-103	Rev: A
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THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

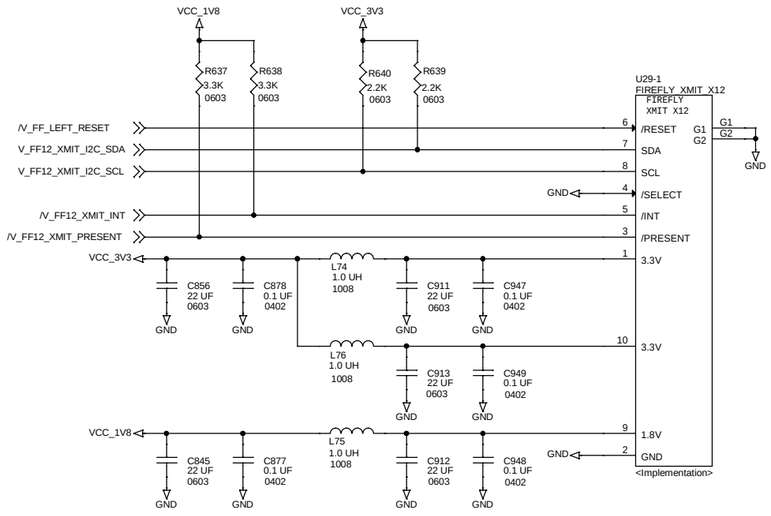
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

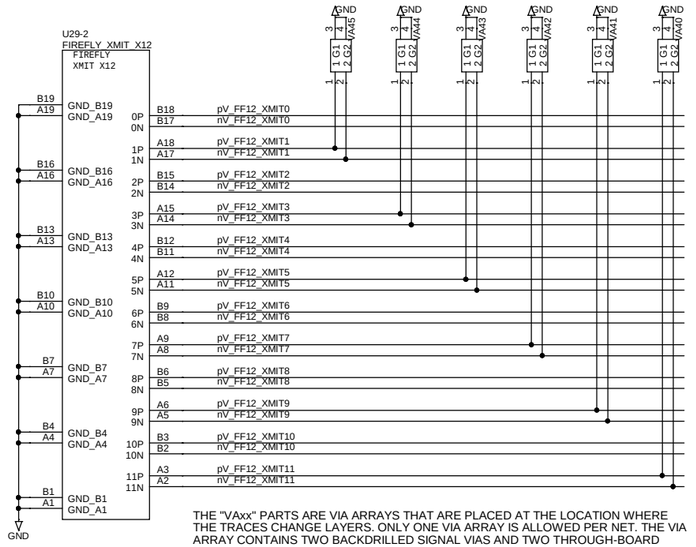
QUADS "Q" AND "S" ARE CLOCKED FROM QUAD "R"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

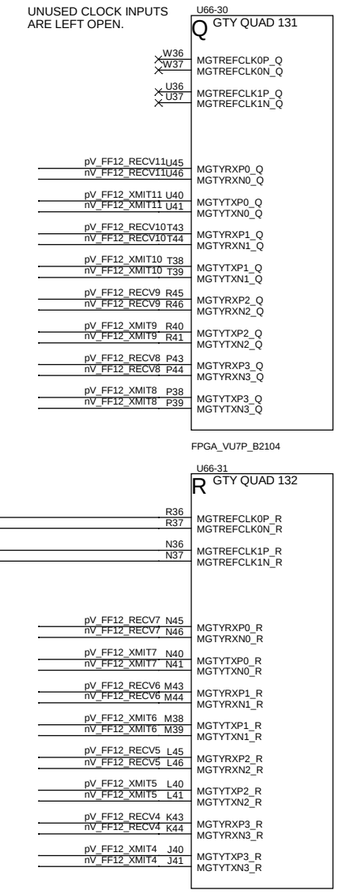
ac_pV_CLK0_CHAN7
ac_nV_CLK0_CHAN7
ac_pV_CLK1_CHAN7
ac_nV_CLK1_CHAN7

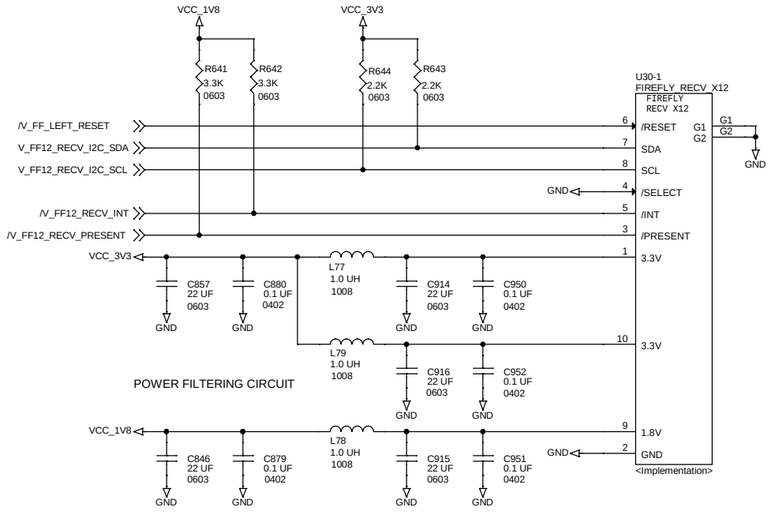


ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

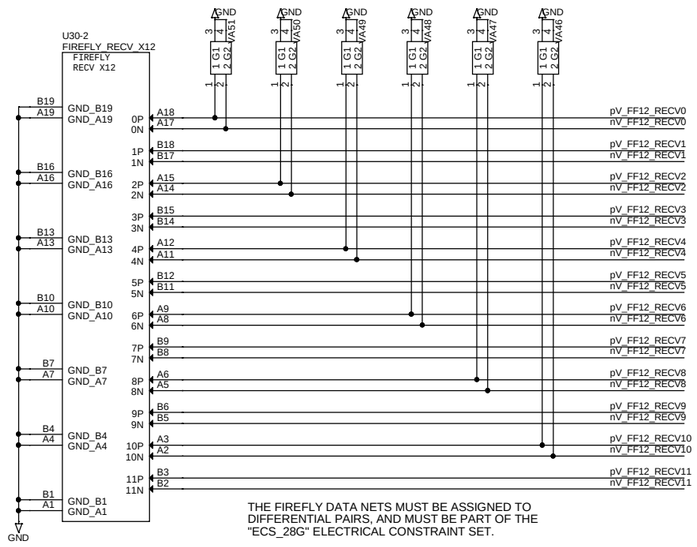


THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.





POWER FILTERING CIRCUIT



THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.15: VU7P QUADS QRS FIREFLY X12 #12

Size | Document Number: 6089-103 | Rev: A

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