THIS IS A FLAT SCHEMATIC, NOT A HIERARCHICAL ONE. NETS USE "OFFPAGE CONNECTOR" SYMBOLS TO GO FROM PAGE TO PAGE.

THE SCHEMATIC IS DIVIDED INTO SECTIONS OF RELATED FUNCTIONALITY.
THE SECTIONS ARE:
1: NOTES AND BLOCK DIAGRAMS
2: GLOBAL SIGNALS
3: POWER SOURCES AND CONTROLS
4: I2C CONTROLS
5: KU15P POWER AND SIGNAL (NON-MGT)
6: VU7P POWER AND SIGNAL (NON-MGT)
7: KU15P MGT TRANSCEIVERS
8: VU7P MGT TRANSCEIVERS

# TO DO:

CHECK "bc" AND "ac" PREFIXES ON AC-COUPLED SIGNALS

ON VU7P QUAD "S', CHANGE "...133" TO "...S" IN PIN NAMES

ON VU7P QUAD "A-J', CHANGE "...GTH" TO "...GTY" IN PIN NAMES

ASSIGN AND LABEL I2C ADDRESSES

SOLDERPASTE PATTERNS FOR UEC5_UCCE FOOTPRINT

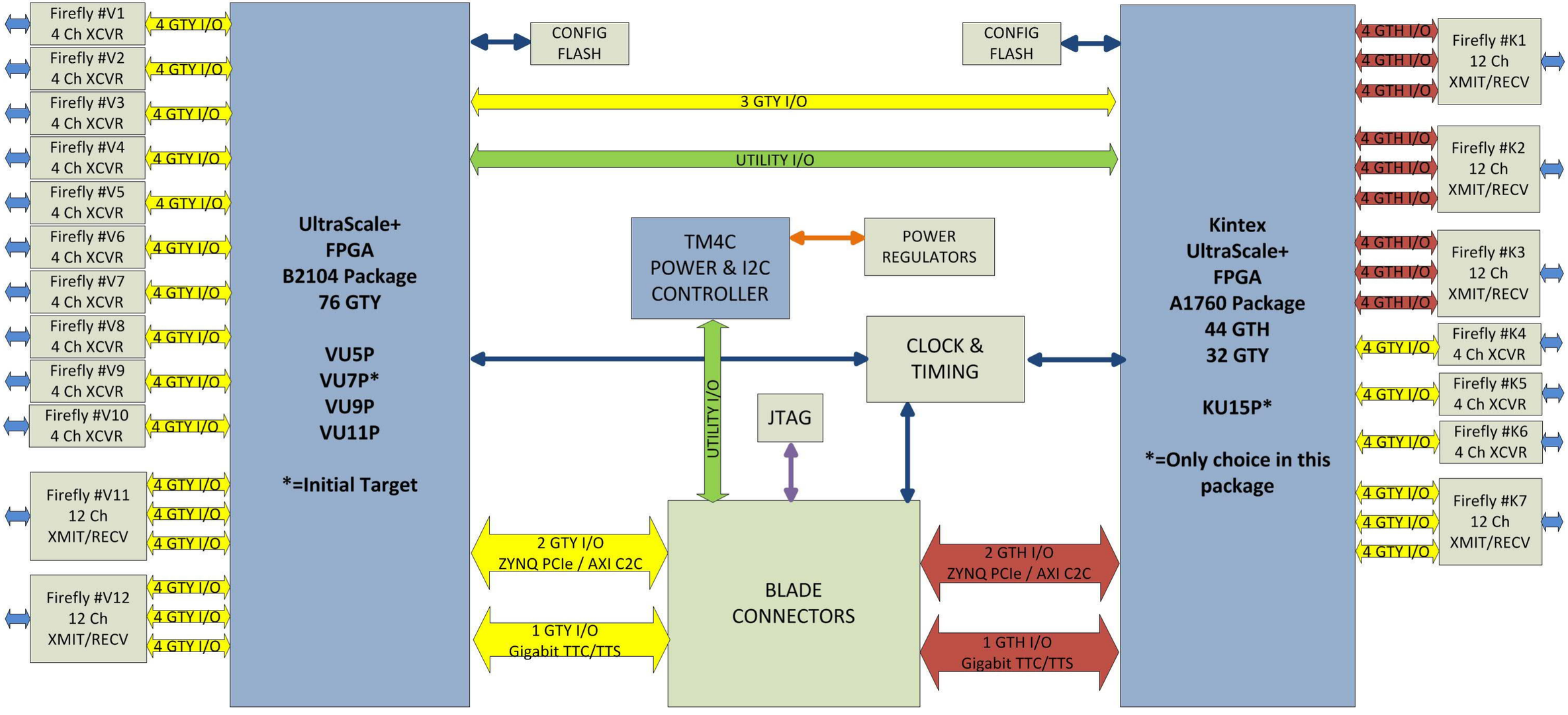
# NETS TO STUDY / DOCUMENT

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 1.01: NOTES

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 1 of 74




| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 1.02: BLOCK DIAGRAM | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Wednesday, March 06, 2019 | Sheet 2 of 74 | |

# KU15P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

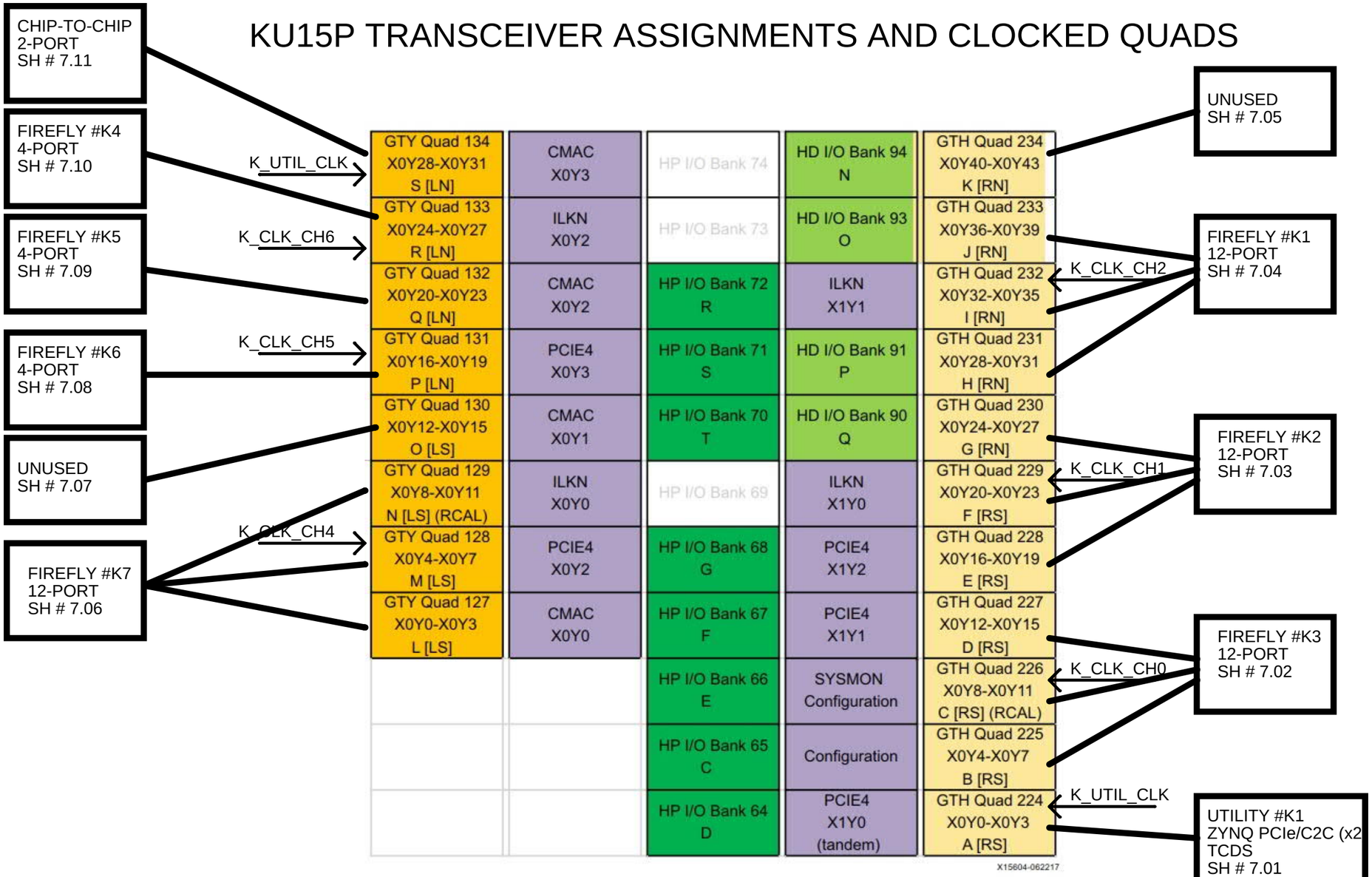



*Figure 1-86:* **XCKU15P Banks in FFVA1760 Package**

EACK "K_CLK_CHn" CONSISTS OF TWO CLOCKS.
ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 1.03: KU15P TRANSCEIVERS | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 3 of 74 | |

# VU7P TRANSCEIVER ASSIGNMENTS AND CLOCKED QUADS

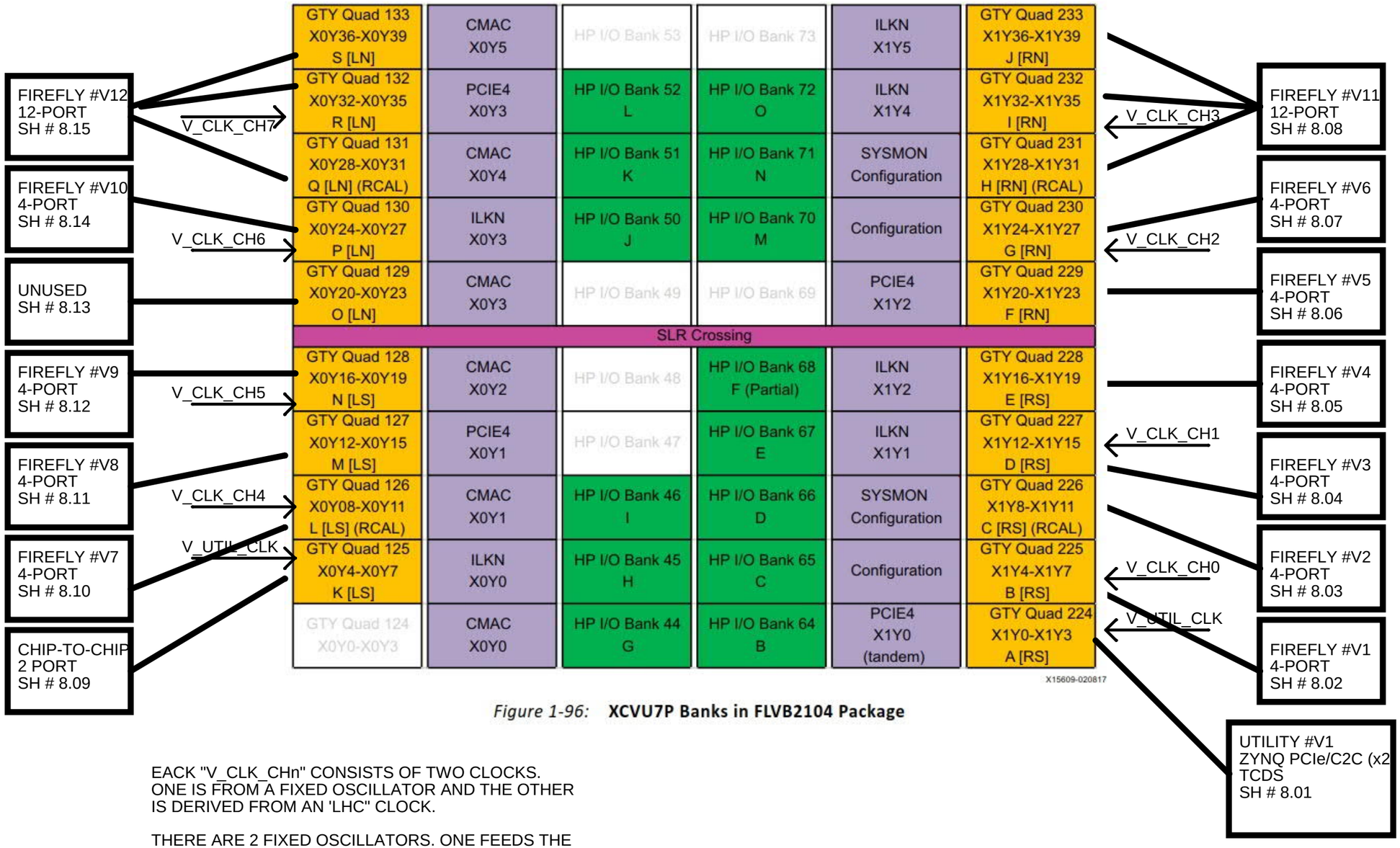



*Figure 1-96:* **XCVU7P Banks in FLVB2104 Package**

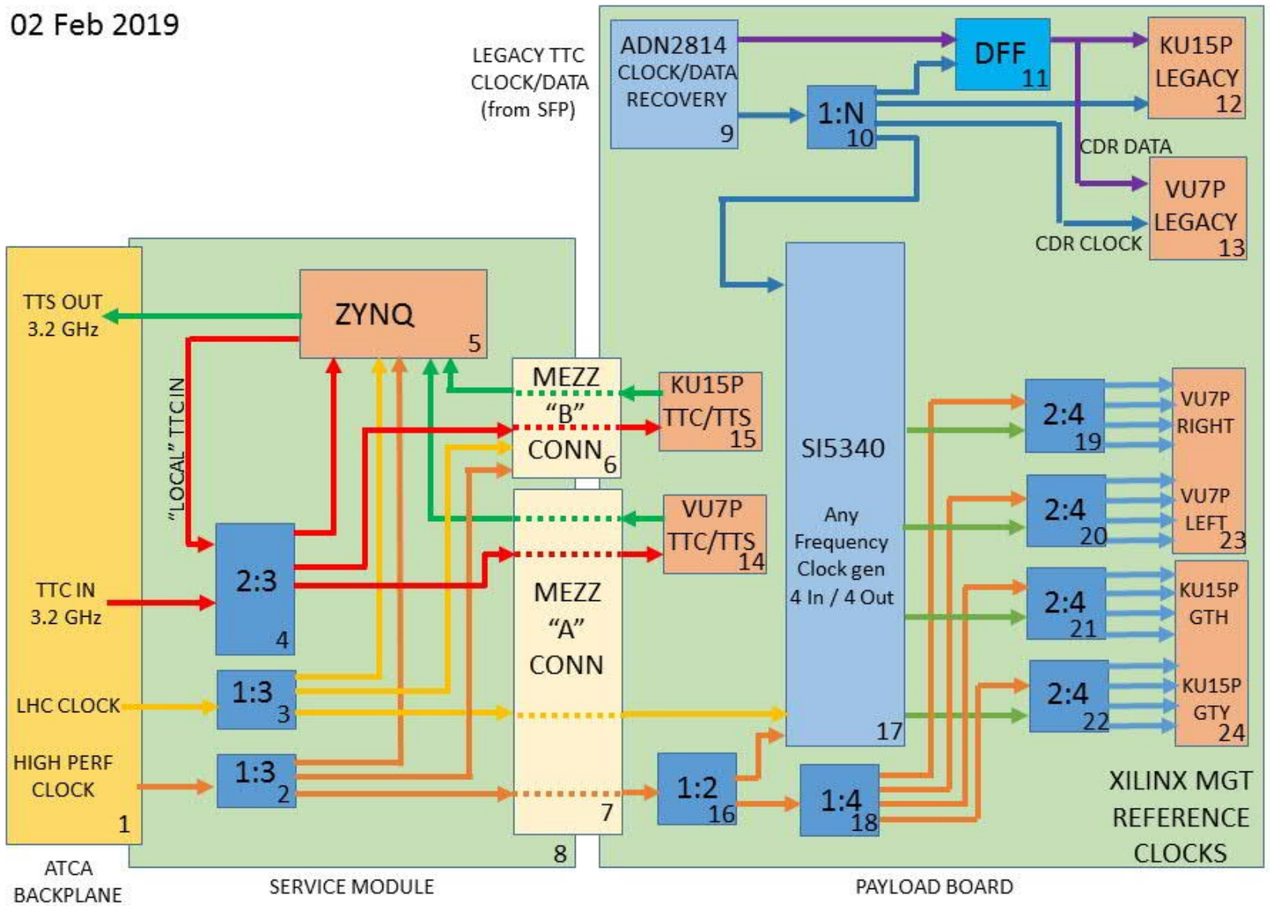
EACK "V_CLK_CHn" CONSISTS OF TWO CLOCKS. ONE IS FROM A FIXED OSCILLATOR AND THE OTHER IS DERIVED FROM AN 'LHC" CLOCK.

THERE ARE 2 FIXED OSCILLATORS. ONE FEEDS THE QUADS ON THE LEFT SIDE OF THE CHIP AND THE OTHER FEEDS THE QUADS ON THE RIGHT SIDE OF THE CHIP.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 1.04: VU7P TRANSCEIVERS | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 4 of 74 | |

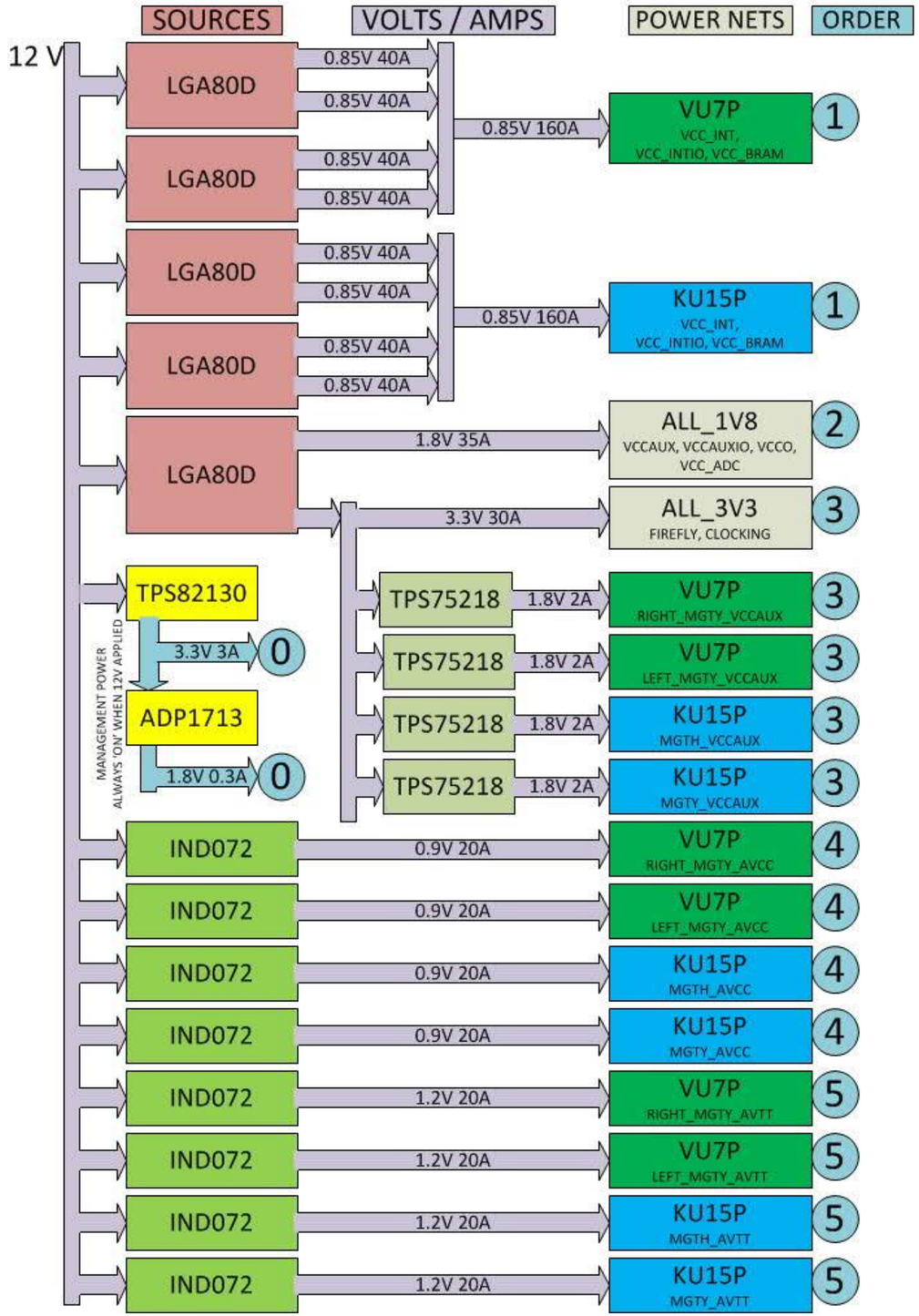
# BU/CU Apollo ATCA Backplane Signal Distribution

02 Feb 2019




Charlie Strohman crs5@cornell.edu

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 1.05: LHC SIGNAL DISTRIBUTION | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 5 of 74 | |

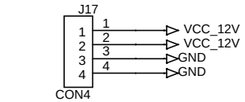



ATCA FPGA BOARD, KU15P AND VU7P, MK1

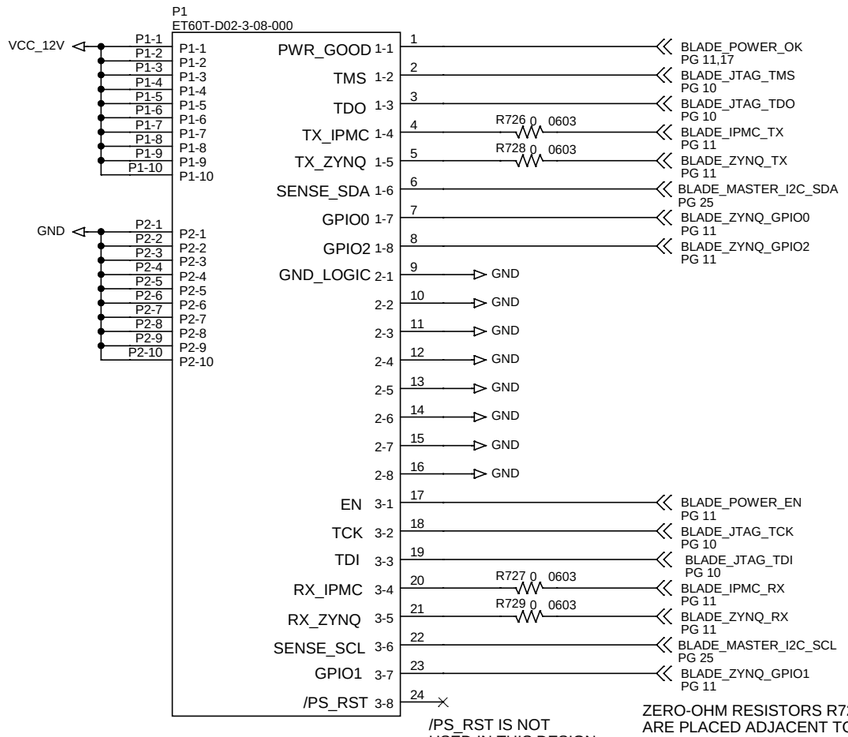
Title: 1.06: POWER DISTRIBUTION

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 6 of 74

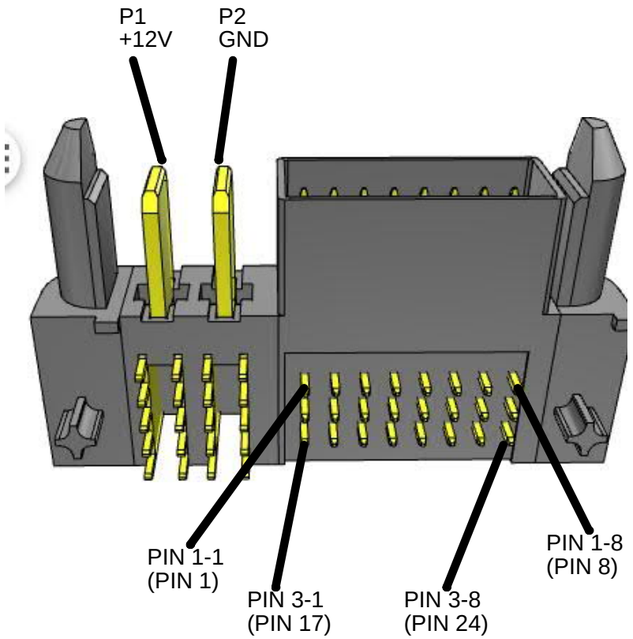



**Bench Top Power Inlet**




/PS_RST IS NOT USED IN THIS DESIGN

ZERO-OHM RESISTORS R726 AND R727 ARE PLACED ADJACENT TO EACH OTHER. IF "TX" AND "RX" NEED TO BE SWAPPED, REMOVE AND ROTATE THE JUMPERS BY 90 DEGREES. THE SAME IS TRUE FOR R728 AND R729.




ET60T-D02-3-08-000

THESE SHAPES DEFINE HOLES AND KEEPOUT AREAS FOR THE SPLICE PLATES.

SP2 DNI SP1 DNI

THESE HOLES ARE FOR MOUNTING THE FIREFLY HEATSINKS

H13 H12 H11 H8 H7 H6 — DNI

THESE HOLES ARE FOR MOUNTING THE TOP COVER

H5 H18 H4 H17 H3 H16 — DNI

THESE HOLES ARE FOR MOUNTING THE BOTTOM COVER

H1 H14 H9 H15 H10 H2 — DNI

THESE SHAPES DEFINE MECHANICAL OBJECTS THAT SHOULD BE IN THE BILL OF MATERIALS.

BR1 BR2 BR3 — BRACKET

BRACKETS FOR SUPPORTING A SUB-FRONT PANEL

M1 KU15P HEATSINK
M23 HEATSINK PLATE
M3 M3 STANDOFF
M4 M3 STANDOFF
M5 M3 STANDOFF
M6 M3 STANDOFF
M7 M3 STANDOFF
M8 M3 STANDOFF
M2 VU7P HEATSINK
M24 HEATSINK PLATE
M9 M3 STANDOFF
M10 M3 STANDOFF
M11 M3 STANDOFF
M12 M3 STANDOFF
M13 M3 STANDOFF
M14 M3 STANDOFF
M15 FIREFLY HEATSINK (LEFT SIDE)
M16 M2.5 STANDOFF
M17 M2.5 STANDOFF
M18 M2.5 STANDOFF
M19 FIREFLY HEATSINK (RIGHT SIDE)
M20 M2.5 STANDOFF
M21 M2.5 STANDOFF
M22 M2.5 STANDOFF

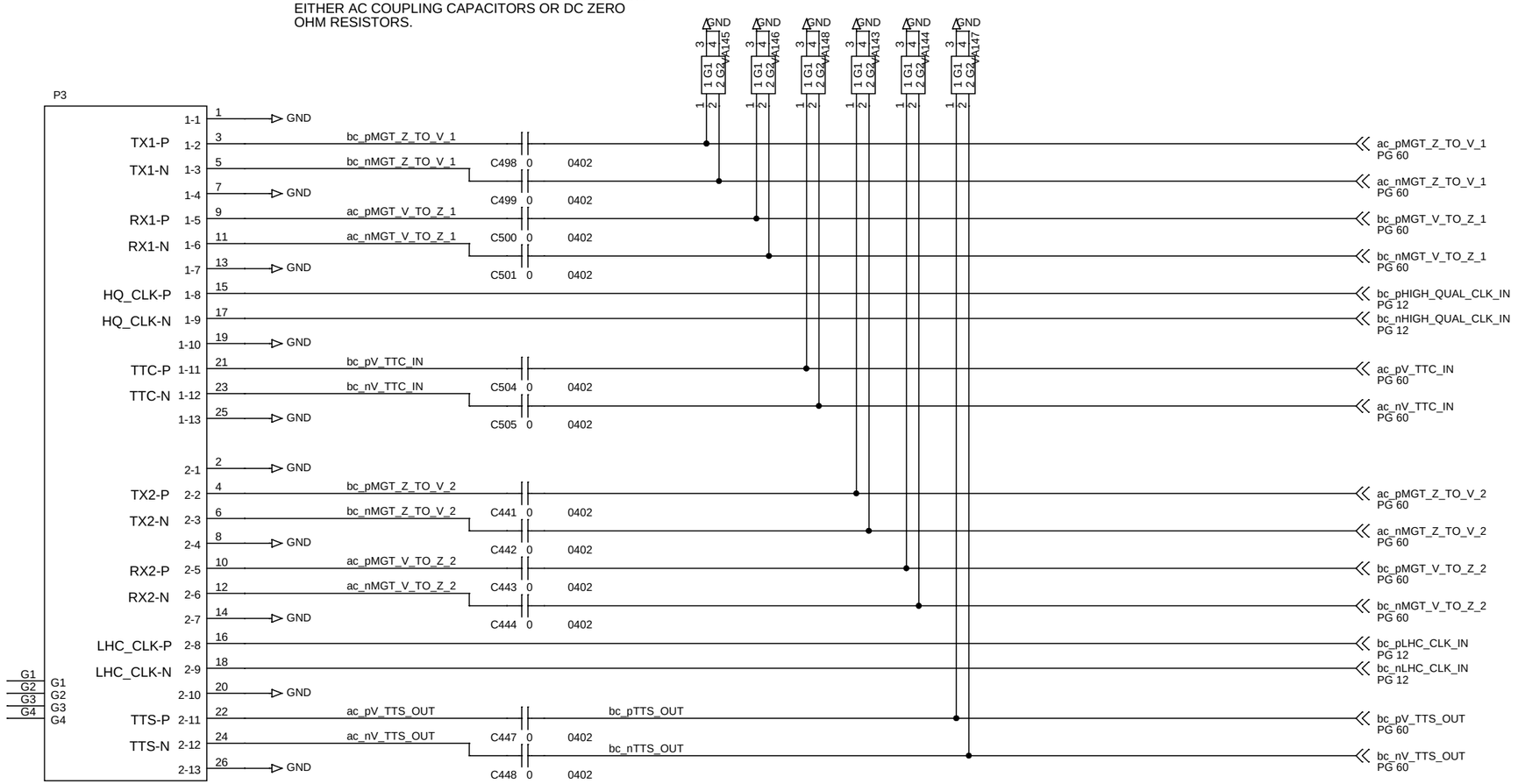
ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.01: BLADE POWER CONNECTOR

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Thursday, February 28, 2019 Sheet 7 of 74

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.



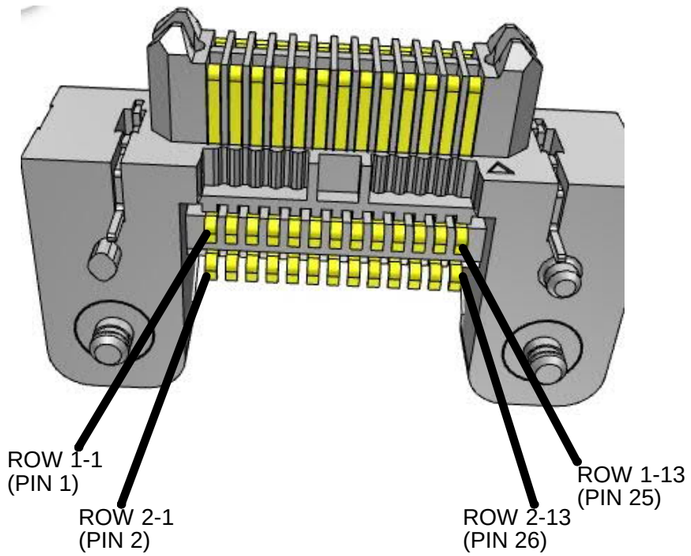

AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

REPLACED THE DC BLOCKING CAPACITORS WITH ZERO-OHM RESISTORS. THE SERVICE BLADE ALREADY PROVIDES CAPACITORS.

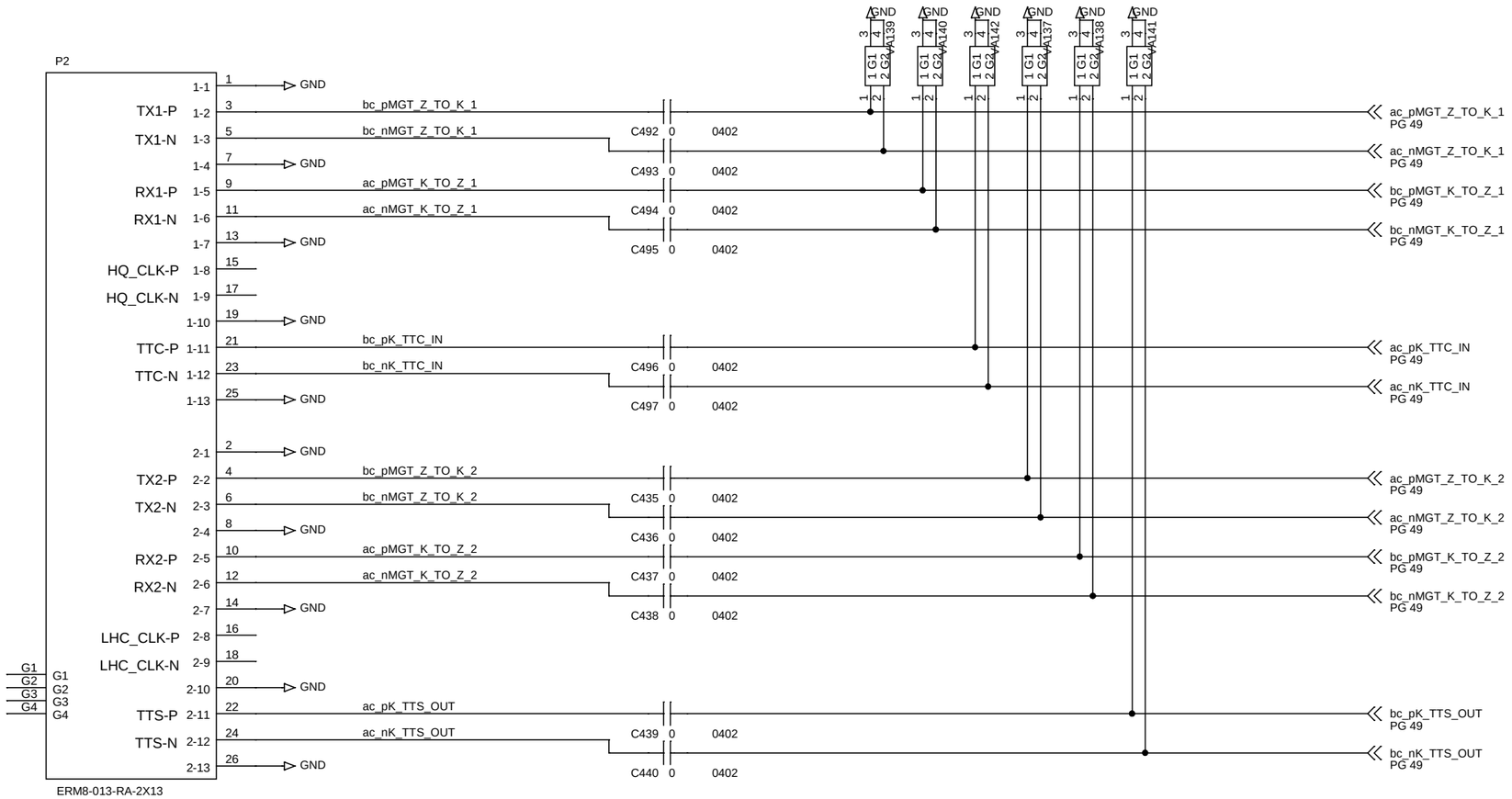
# VU7P AND BACKPLANE CLOCK SIGNALS ONLY




ERM8-013-01-L-D-RA-DS

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 2.02: BLADE HS CONNECTOR #1 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Friday, March 08, 2019 | Sheet 8 of 74 | |

THE SIGNALS THAT START WITH "MGT" ARE HIGH SPEED DIFFERENTIAL PAIRS CONNECTED TO GIGABIT TRANSCEIVERS. THEY ARE INTENDED FOR EITHER PCIe OR AXI-C2C. PADS ARE PROVIDED FOR EITHER AC COUPLING CAPACITORS OR DC ZERO OHM RESISTORS.



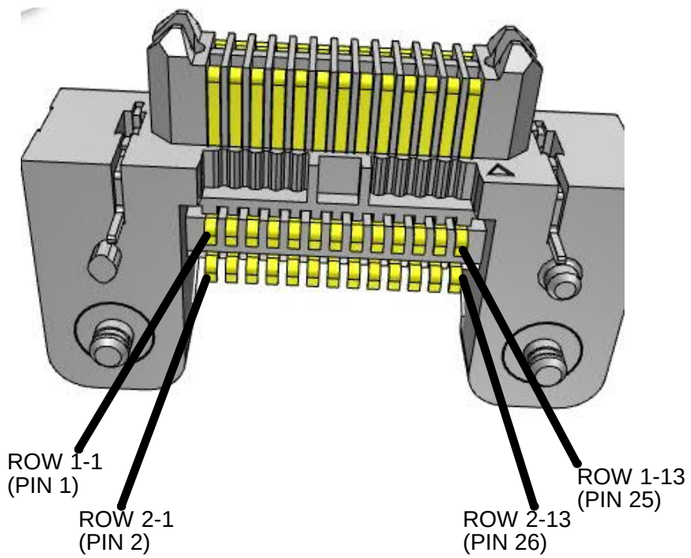

AC COUPLED SIGNALS

bc = BEFORE CAPACITOR

ac = AFTER CAPACITOR

REPLACED THE DC BLOCKING CAPACITORS WITH ZERO-OHM RESISTORS. THE SERVICE BLADE ALREADY PROVIDES CAPACITORS.

# KU15P SIGNALS ONLY




ERM8-013-01-L-D-RA-DS

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 2.03: BLADE HS CONNECTOR #2

Size | Document Number: 6089-103 | Rev: A

Date: Friday, March 08, 2019 | Sheet 9 of 74

TO BYPASS A DEVICE, CONNECT A JUMPER FROM 1 TO 3.
TO INCLUDE A DEVICE IN THE CHAIN, CONNECT A JUMPER FROM 1 TO 2 AND FROM 3 TO 4.
AS ILLUSTRATED, THE CONTROLLER AND THE VU7P ARE PART OF THE CHAIN, AND THE KU15P IS BYPASSED.

## BLADE JTAG

BLADE_JTAG_TMS PG 7

VCC_M3V3 — R108 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

U49 74LVC1G126 — R92 33 0603 — V_TMS_1V8
U53 74LVC1G126 — R98 33 0603 — K_TMS_1V8
U57 74LVC1G126 — R107 33 0603 — C_TMS_3V3
U50 74LVC1G125 — R95 33 0603
U55 74LVC1G125 — R101 33 0603
U60 74LVC1G125 — R109 33 0603
U62 74LVC1G126 — R113 33 0603 — V_TCK_1V8
U77 74LVC1G126 — R123 33 0603 — K_TCK_1V8
U84 74LVC1G126 — R133 33 0603 — C_TCK_3V3
U67 74LVC1G125 — R116 33 0603
U78 74LVC1G125 — R130 33 0603
U86 74LVC1G125 — R136 33 0603

VCC_M3V3 — R94 10K 0603

VCC_M1V8 GND VCC_M3V3

## BLADE JTAG

BLADE_JTAG_TCK PG 7

VCC_M3V3 — R134 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

VCC_M3V3 — R115 10K 0603

## FORCE JTAG CABLE

IF EITHER THE JUMPER IS IN PLACE, OR THE PROGRAMMING CABLE IS PLUGGED IN, THE OUTPUT OF THIS BUFFER WILL BE LOW. THIS WILL ENABLE ALL OF THE DRIVERS RELATED TO THE CABLE SIGNALS, AND DISABLE ALL OF THE DRIVERS RELATED TO THE MAIN BLADE.

VCC_M3V3 — R70 10K 0603 — U37 74LVC1G125 — VCC_M3V3

J12 JUMPER — GND

THE JTAG REFERENCE IS 3.3 VOLTS.

VCC_M3V3 — J1

CONN_JTAG_TMS
CONN_JTAG_TCK
CONN_JTAG_TDO
CONN_JTAG_TDI

GND — CON_2X7_RA

USE THE JUMPER IF PIN 13 IS NOT AUTOMATICALLY PULLED LOW WHEN THE CABLE IS PLUGGED IN.

PIN 13 SHOULD BE PULLED LOW WHEN THE CABLE IS PLUGGED IN.

## FRONT PANEL JTAG

## BLADE JTAG

BLADE_JTAG_TDI PG 7

VCC_M3V3 — R86 10K 0603

A VOLTAGE TRANSLATOR CAN BE INSERTED HERE IF THE MAIN BLADE HASOTHER THAN 3.3 VOLT LOGIC LEVELS ON THE JTAG SIGNALS. THE PULLUP RESISTOR CONNECTS TO THE LOGIC VOLTAGE.

VCC_M3V3 — R82 10K 0603

TDI_3V3

U42 74LVC1G126 — R85 33 0603 — VCC_M3V3 GND
U41 74LVC1G125 — R83 33 0603 — VCC_M3V3 GND

THESE VOLTAGE TRANSLATORS CONVERT THE 1.8 VOLT LOGIC LEVEL FROM THE LAST FPGA TO THE 3.3 VOLT LOGIC LEVEL USED ON THE MAIN BLADE OR THE EXTERNAL PROGRAMMER.

U38 74AUP1T34 — R72 33 0603 — VCC_M1V8 VCC_M3V3 GND
U40 74AUP1T34 — R81 33 0603 — BLADE_JTAG_TDO PG 7 — VCC_M1V8 VCC_M3V3 GND

## BLADE JTAG

JUMPER_2X2 J13 — BYPASS JUMPER

V_TDO AC13
V_TDI AE15
V_TMS_1V8 AG15
V_TCK_1V8 AE13

U66-43 FPGA_VU7P_B2104 — JTAG — TDO_0 TDI_0 TMS_0 TCK_0

# VU7P

U7 74LVC1G125 — R11 33 0603 — VCC_M1V8 GND

VCC_M3V3 — C771 C766 C752 C747 C825 0.1 UF 0402 — GND
VCC_M3V3 — C812 C809 C803 C826 0.1 UF 0402 — GND

JUMPER_2X2 J14 — BYPASS JUMPER

K_TDO AK16
K_TDI AJ15
K_TMS_1V8 AJ17
K_TCK_1V8 AK15

U65-11 FPGA_KU15P_A1760 — JTAG — TDO_0 TDI_0 TMS_0 TCK_0

# KU15P

VCC_M1V8 — C794 C786 C781 C778 C762 0.1 UF 0402 — GND
VCC_M1V8 — C761 C758 C755 C969 C971 0.1 UF 0402 — GND

TDI_1V8

U9 74LVC1G125 — R25 33 0603 — VCC_M1V8 GND

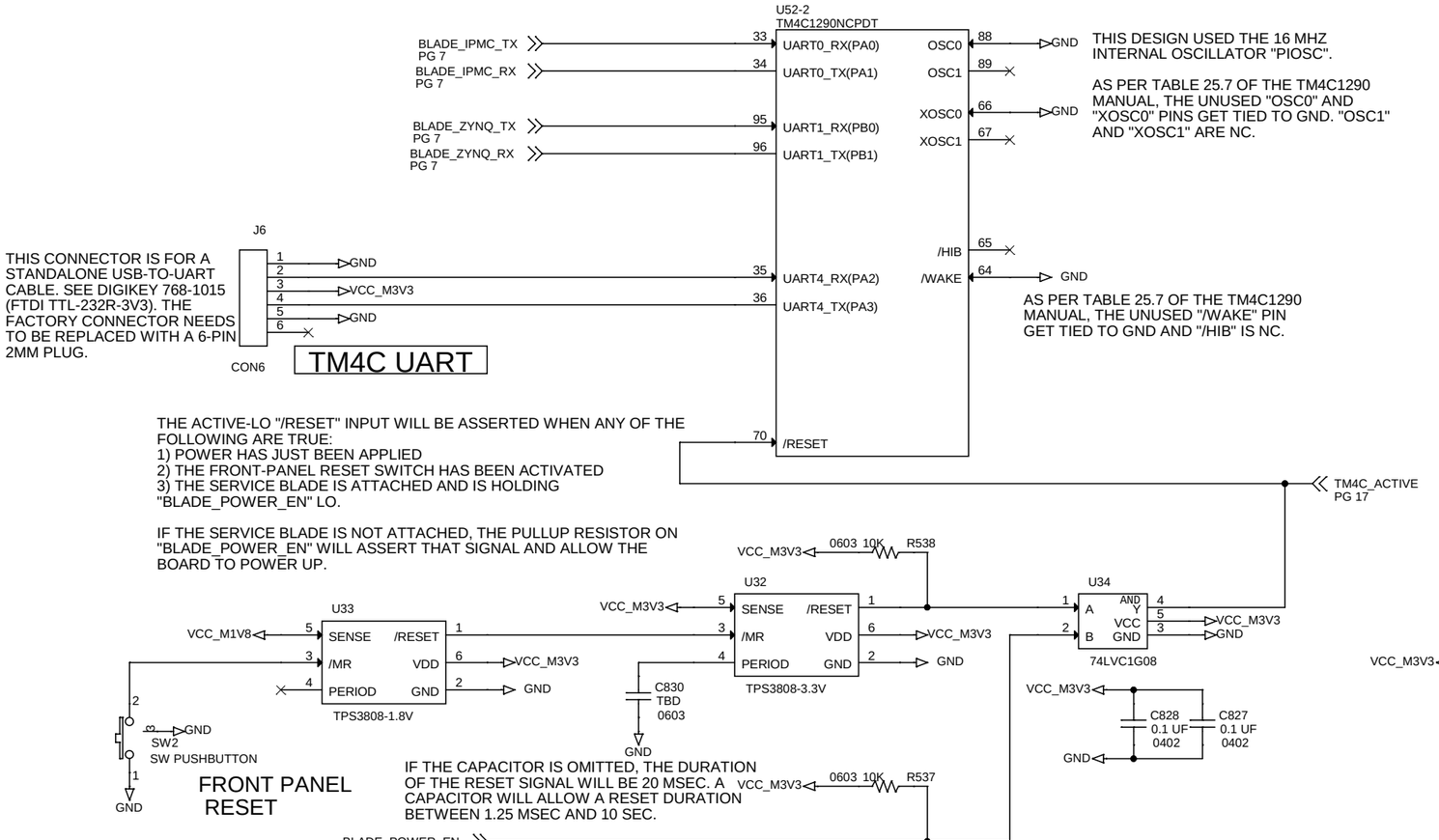
JUMPER_2X2 J15 — BYPASS JUMPER

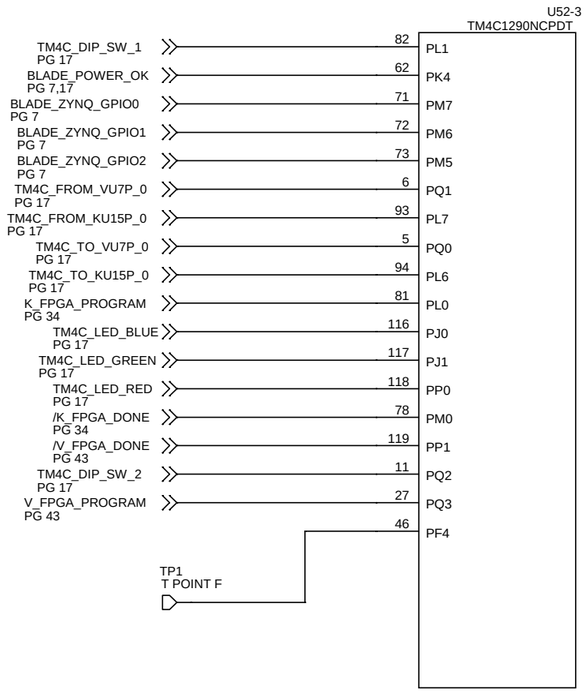
C_TDO 97
C_TDI 98
C_TMS_3V3 99
C_TCK_3V3 100

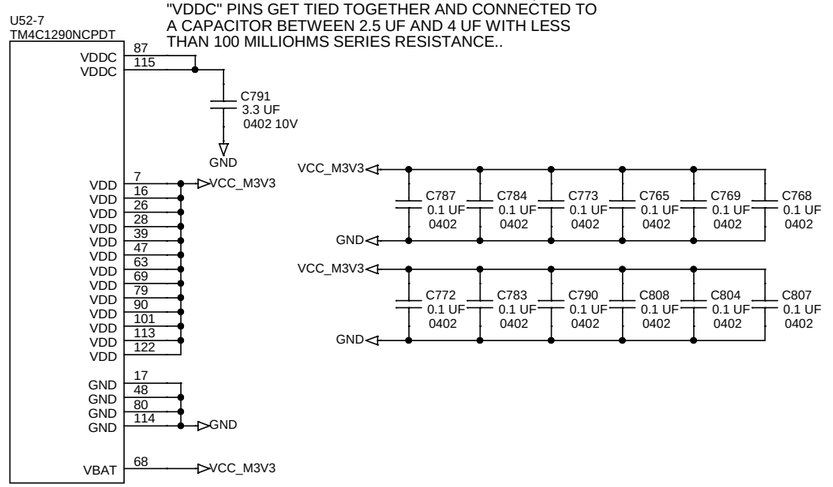
U52-1 TM4C1290NCPDT — JTAG_TDO JTAG_TDI JTAG_TMS JTAG_TCK

# CONTROLLER

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 2.04: JTAG CHAIN | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 10 of 74 | |




| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 2.05 CONTROLLER | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, April 16, 2019 | Sheet 11 of 74 | |

DO WE NEED TO ADD A BUFFER TO GET AN LHC-BASED CLOCK INTO THE FPGA LOGIC SECTION? WILL USING THE "TXOUTCLK" FROM A GTH/GTY BLOCK BE ADEQUATE?

bc_pLEGACY_CLK PG 14 — C1 0.1 UF 0402 — ac_pLEGACY_CLK
bc_nLEGACY_CLK PG 14 — C2 0.1 UF 0402 — ac_nLEGACY_CLK
R129 49.9 0402, R131 49.9 0402, C216 0.1 UF 0402 GND
bc_pLHC_CLK_IN PG 8 — C445 0.1 UF 0402 — ac_pLHC_CLK_IN
bc_nLHC_CLK_IN PG 8 — C446 0.1 UF 0402 — ac_nLHC_CLK_IN
R120 49.9 0402, R119 49.9 0402, C205 0.1 UF 0402 GND
bc_pHIGH_QUAL_CLK_IN PG 8 — C502 0.1 UF 0402 — ac_pHIGH_PERF_CLK_IN
bc_nHIGH_QUAL_CLK_IN PG 8 — C503 0.1 UF 0402 — ac_nHIGH_PERF_CLK_IN
R138 49.9 0402, R139 49.9 0402, C250 0.1 UF 0402 GND

U81-1 SI5340
pXTAL, X1, 48 MHz, nXTAL
XA, X1_SHIELD, X2_SHIELD, XB
FB_IN /FB_IN
OUT_0 /OUT_0 — pSYNTH_CLK0 / nSYNTH_CLK0
OUT_1 /OUT_1 — pSYNTH_CLK1 / nSYNTH_CLK1
OUT_2 /OUT_2 — pSYNTH_CLK2 / nSYNTH_CLK2
OUT_3 /OUT_3 — pSYNTH_CLK3 / nSYNTH_CLK3
IN_0 /IN_0, IN_1 /IN_1, IN_2 /IN_2

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

WE DO NOT HAVE AN UNUSED OUTPUT, SO WE CAN NOT USE FEEDBACK. ZERO-DELAY BUFFERING IS NOT A REQUIREMENT, NOR IS FIXED PHASE BETWEEN OUTPUTS.

U80 SI53340 1:2
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — pHIGH_PERF_CLK_BUF1 / nHIGH_PERF_CLK_BUF1
Q1 /Q1 — pHIGH_PERF_CLK_BUF0 / nHIGH_PERF_CLK_BUF0
Q2 /Q2, Q3 /QE, VDD, GND PAD
R126 4.7K 0603 GND
R121 100 0402, R110 100 0402
DC COUPLED LVDS
<Implementation>
C751 1 UF 0402 10v

THE SPLIT TERMINATOR WITH A CAPACITOR TO GND IS USED FOR CLOCKS COMING FROM OFF THE BOARD. CLOCKS THAT ARE STRICTLY WITHIN THE BOARD USE SIMPLE 100 OHM TERMINATORS.

U61 SI53340 1:4
CLK0 /CLK0, CLK1 /CLK1, NC8, CLK_SEL
Q0 /Q0 — pHIGH_PERF_CLK0 / nHIGH_PERF_CLK0
Q1 /Q1 — pHIGH_PERF_CLK1 / nHIGH_PERF_CLK1
Q2 /Q2 — pHIGH_PERF_CLK2 / nHIGH_PERF_CLK2
Q3 /QE — pHIGH_PERF_CLK3 / nHIGH_PERF_CLK3
R105 4.7K 0603 GND
<Implementation>
C767 1 UF 0402 10v

THESE CLOCKS DRIVE THE 4 BUFFERS AT THE BOTTOM OF THIS PAGE.

AC COUPLED LVDS

U83 SI53340 2:4
pHIGH_PERF_CLK0, nHIGH_PERF_CLK0 — R127 100 0402, R132 100 0402
pSYNTH_CLK0, nSYNTH_CLK0
DC COUPLED LVDS
R135 4.7K 0603 GND
V_GTY1_SEL_SYNTH PG 27
<Implementation>
C754 1 UF 0402 10v
Q0 /Q0 — bc_pV_CLK1_CHAN0 / bc_nV_CLK1_CHAN0 — C228 0.1 UF 0402 — ac_pV_CLK1_CHAN0 PG 61 / ac_nV_CLK1_CHAN0 PG 61 — QUAD B
Q1 /Q1 — bc_pV_CLK1_CHAN1 / bc_nV_CLK1_CHAN1 — C232 0.1 UF 0402, C241 0.1 UF 0402 — ac_pV_CLK1_CHAN1 PG 63 / ac_nV_CLK1_CHAN1 PG 63 — QUAD D
Q2 /Q2 — bc_pV_CLK1_CHAN2 / bc_nV_CLK1_CHAN2 — C244 0.1 UF 0402, C251 0.1 UF 0402 — ac_pV_CLK1_CHAN2 PG 66 / ac_nV_CLK1_CHAN2 PG 66 — QUAD G
Q3 /QE — bc_pV_CLK1_CHAN3 / bc_nV_CLK1_CHAN3 — C257 0.1 UF 0402, C269 0.1 UF 0402 — ac_pV_CLK1_CHAN3 PG 67 / ac_nV_CLK1_CHAN3 PG 67 — QUAD I

THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.

U56 SI53340 2:4
pHIGH_PERF_CLK1, nHIGH_PERF_CLK1 — R97 100 0402, R100 100 0402
pSYNTH_CLK1, nSYNTH_CLK1
DC COUPLED LVDS
R106 4.7K 0603 GND
V_GTY2_SEL_SYNTH PG 27
<Implementation>
C780 1 UF 0402 10v
Q0 /Q0 — bc_pV_CLK1_CHAN4 / bc_nV_CLK1_CHAN4 — C149 0.1 UF 0402 — ac_pV_CLK1_CHAN4 PG 69 / ac_nV_CLK1_CHAN4 PG 69 — QUAD L
Q1 /Q1 — bc_pV_CLK1_CHAN5 / bc_nV_CLK1_CHAN5 — C151 0.1 UF 0402, C158 0.1 UF 0402 — ac_pV_CLK1_CHAN5 PG 71 / ac_nV_CLK1_CHAN5 PG 71 — QUAD N
Q2 /Q2 — bc_pV_CLK1_CHAN6 / bc_nV_CLK1_CHAN6 — C160 0.1 UF 0402, C162 0.1 UF 0402 — ac_pV_CLK1_CHAN6 PG 73 / ac_nV_CLK1_CHAN6 PG 73 — QUAD P
Q3 /QE — bc_pV_CLK1_CHAN7 / bc_nV_CLK1_CHAN7 — C166 0.1 UF 0402, C172 0.1 UF 0402 — ac_pV_CLK1_CHAN7 PG 74 / ac_nV_CLK1_CHAN7 PG 74 — QUAD R

THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.

AC COUPLED LVDS

U87 SI53340 2:4
pHIGH_PERF_CLK2, nHIGH_PERF_CLK2 — R147 100 0402, R143 100 0402
pSYNTH_CLK2, nSYNTH_CLK2
DC COUPLED LVDS
R140 4.7K 0603 GND
K_GTH_SEL_SYNTH PG 27
SPARE
<Implementation>
C736 1 UF 0402 10v
Q0 /Q0 — bc_pK_CLK1_CHAN0 / bc_nK_CLK1_CHAN0 — C286 0.1 UF 0402 — ac_pK_CLK1_CHAN0 PG 50 / ac_nK_CLK1_CHAN0 PG 50 — QUAD C
Q1 /Q1 — bc_pK_CLK1_CHAN1 / bc_nK_CLK1_CHAN1 — C281 0.1 UF 0402, C270 0.1 UF 0402 — ac_pK_CLK1_CHAN1 PG 51 / ac_nK_CLK1_CHAN1 PG 51 — QUAD F
Q2 /Q2 — bc_pK_CLK1_CHAN2 / bc_nK_CLK1_CHAN2 — C264 0.1 UF 0402, C252 0.1 UF 0402 — ac_pK_CLK1_CHAN2 PG 52 / ac_nK_CLK1_CHAN2 PG 52 — QUAD I
Q3 /QE — C249 0.1 UF 0402

THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.

U68 SI53340 2:4
pHIGH_PERF_CLK3, nHIGH_PERF_CLK3 — R125 100 0402, R117 100 0402
pSYNTH_CLK3, nSYNTH_CLK3
DC COUPLED LVDS
R114 4.7K 0603 GND
K_GTY_SEL_SYNTH PG 27
<Implementation>
C759 1 UF 0402 10v
Q0 /Q0 — bc_pK_CLK1_CHAN4 / bc_nK_CLK1_CHAN4 — C211 0.1 UF 0402 — ac_pK_CLK1_CHAN4 PG 54 / ac_nK_CLK1_CHAN4 PG 54 — QUAD M
Q1 /Q1 — bc_pK_CLK1_CHAN5 / bc_nK_CLK1_CHAN5 — C204 0.1 UF 0402 — ac_pK_CLK1_CHAN5 PG 56 / ac_nK_CLK1_CHAN5 PG 56 — QUAD P
Q2 /Q2 — bc_pK_CLK1_CHAN6 / bc_nK_CLK1_CHAN6 — C200 0.1 UF 0402 — ac_pK_CLK1_CHAN6 PG 58 / ac_nK_CLK1_CHAN6 PG 58 — QUAD R
Q3 /QE — C191 0.1 UF 0402, C189 0.1 UF 0402, C181 0.1 UF 0402

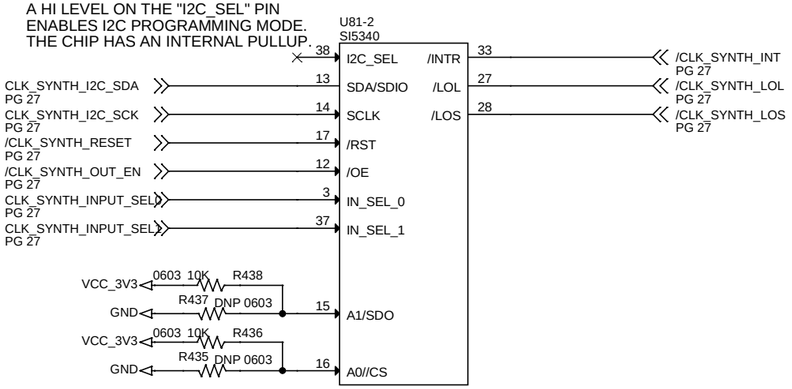
THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.

AC COUPLED LVDS
bc = BEFORE CAPACITOR
ac = AFTER CAPACITOR

THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title: 2.06: LHC CLOCKING
Size | Document Number: 6089-103 | Rev: A
Date: Tuesday, February 26, 2019 | Sheet 12 of 74

A HI LEVEL ON THE "I2C_SEL" PIN
ENABLES I2C PROGRAMMING MODE.
THE CHIP HAS AN INTERNAL PULLUP.

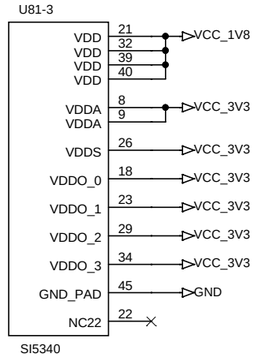


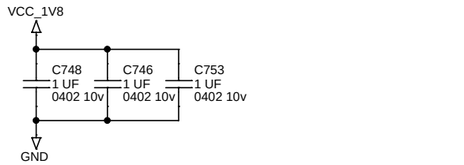

I2C ADDR = 0X77

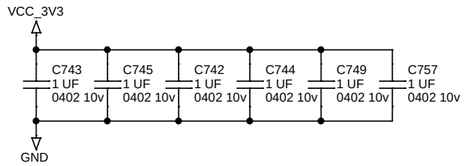
SI5340 I2C ADDRESS:
READ OR WRITE
1 1 1 0 1 A1 A0
RANGE: 0X74 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.




ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title
2.07: LHC CLOCKING SUPPORT

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Friday, March 08, 2019 Sheet 13 of 74

# THIS CIRCUIT ON THIS PAGE IS FOR USE IN THE PROTOTYPE ONLY. IT ALLOWS US TO FEED LEGACY TTC SIGNALS INTO THE SYSTEM.

U13-2
SFP_CONN_WITH_CAGE

U13-1
SFP_CONN_WITH_CAGE

THE SFP I2C SIGNALS AND CONTROL LINES ARE WIRED TO THE CHIPS THAT SUPPORT ACCESS TO THE KU15P OPTICS. THEY CAN BE CONNECTED ELSEWHERE IF DESIRED.

AMC13 CLK IN

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTS_OUT" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS WILL GENERATE THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

J11 JUMPER_DIFF

SFP+ CONNECTOR TO RECEIVE ENCODED TTC CLOCK/DATA STREAM.

THESE RESISTORS MUST BE NEAR THE 65LVDS100 INPUT PINS.

DC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

U12 NB7V52M

U8 65LVDS100

J10 JUMPER_DIFF

THIS BUFFER CONVERTS 2.5V CML SIGNALS TO LVDS LEVELS THAT ARE COMPATABLE WITH ULTRASCALE "HP" BANK INPUTS.

THIS JUMPER ALLOWS DIRECT CONNECTION OF "CDR_DATA" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS DATA, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

THE CLOCK POLARITY IS INVERTED.

U14 ADN2814

U11 SY89832U

THIS DIVIDER NETWORK PROVIDES A DIFFERENTIAL VOLTAGE OF 0.83 VOLTS. IT HOLDS THE RESET INPUT AT A "FALSE" VALUE.

U10 SY89872

AC COUPLED LVDS

THESE NETS NEED 100 OHM INTERNAL TERMINATION AT THE FPGA.

J9 JUMPER_DIFF

S1=0, S0=1 -> B=INPUT/4

THIS JUMPER ALLOWS DIRECT CONNECTION OF "TTC_CLK40" TO EITHER THE KU15P OR THE VU7P. IF BOTH FPGAS NEED THIS CLOCK, USE A UTILITY CONNECTION BETWEEN THEM TO ROUTE FROM ONE TO THE OTHER.

THE THRESHOLD ADJUST SET BY R27=33 IS NOT MUCH DIFFERENT THAN R27=10 OHMS. MAYBE CHECK WITH ERIC HAZEN TO VALIDATE THIS VALUE.

PLACE ONE OF EACH VALUE NEAR PINS 2, 12, 18, 24, AND 31.

THIS DESIGN ONLY USES 2,5 VOLTS FOR LEGACY TTC SUPPORT. IT DOES NOT NEED A DC-DC CONVERTER SUPPLY.

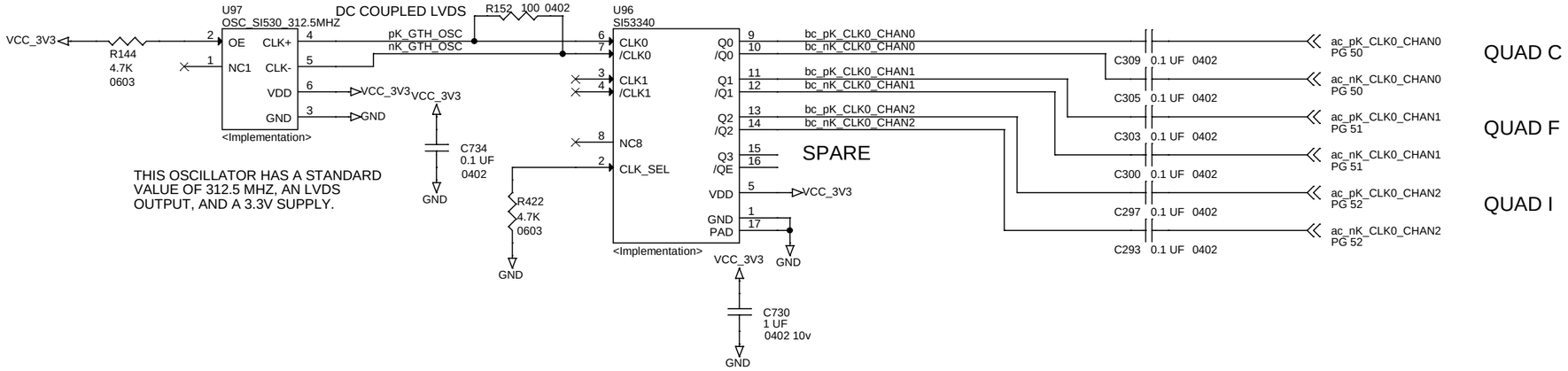
U19 LT1963A

| | | | |
|---|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | | |
| Title: 2.08: LEGACY TTC | | | |
| Size | Document Number: 6089-103 | | Rev: A |
| Date: Tuesday, April 16, 2019 | Sheet 14 of 74 | | |

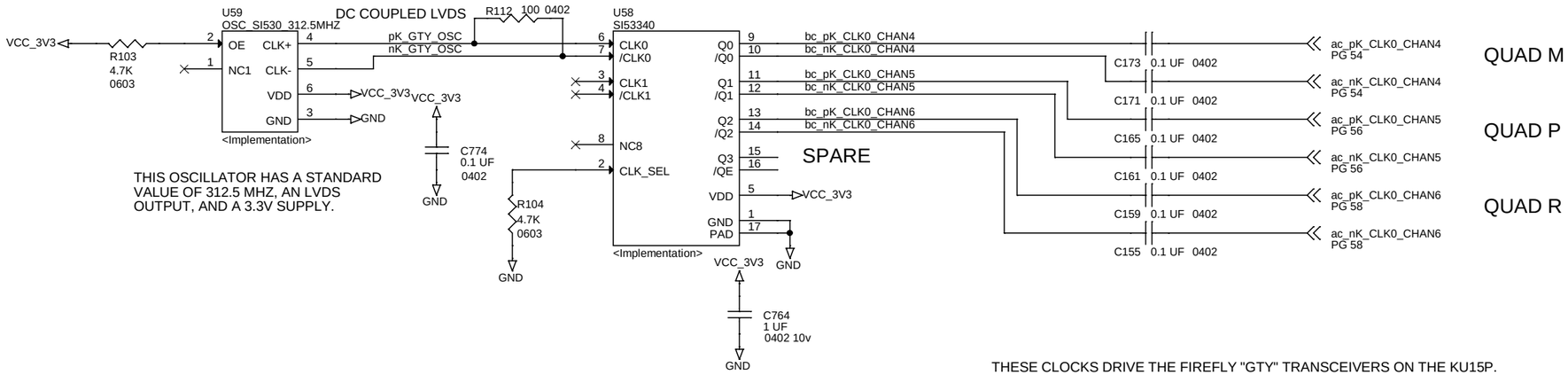
AC COUPLED LVDS

bc = BEFORE CAPACITOR

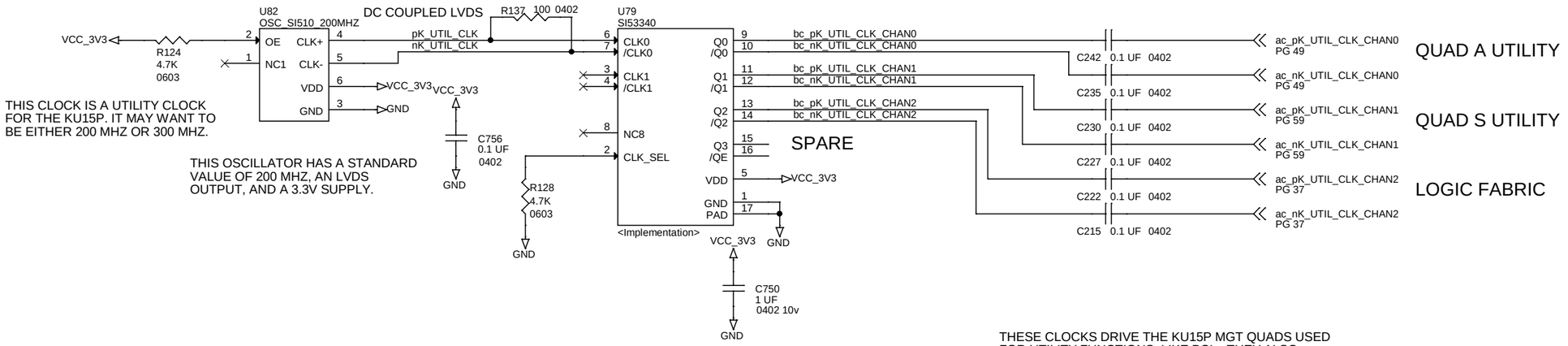
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.




THESE CLOCKS DRIVE THE FIREFLY "GTH" TRANSCEIVERS ON THE KU15P.




THESE CLOCKS DRIVE THE FIREFLY "GTY" TRANSCEIVERS ON THE KU15P.




THESE CLOCKS DRIVE THE KU15P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title

2.09: KU15P OSCILLATOR CLOCKING

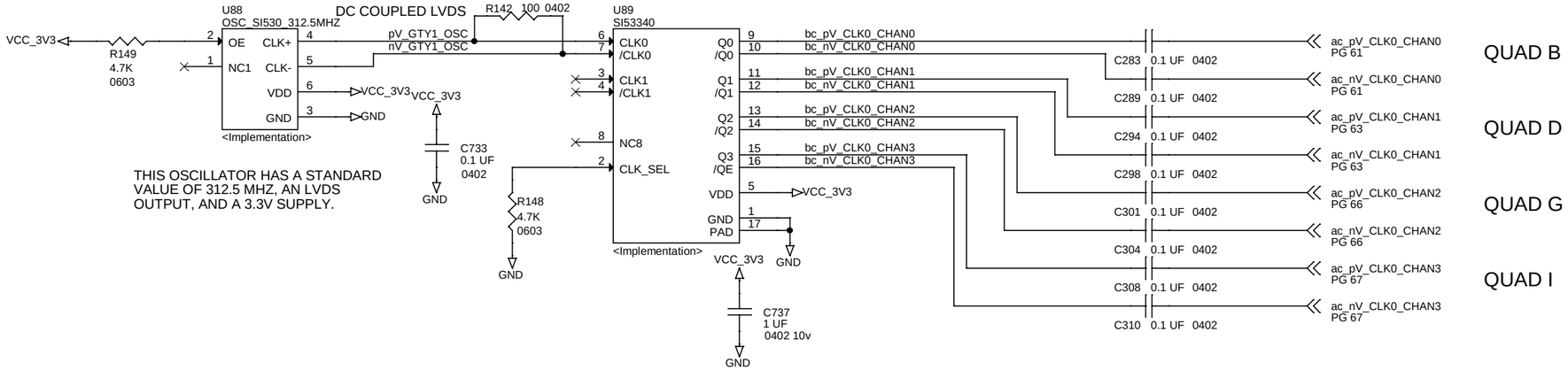
| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 15 of 74

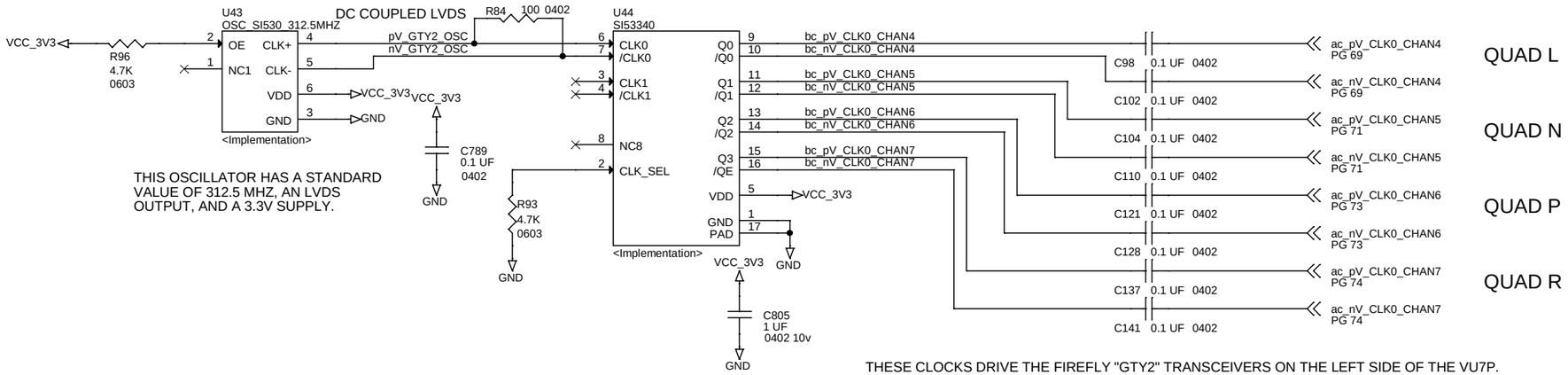
AC COUPLED LVDS

bc = BEFORE CAPACITOR

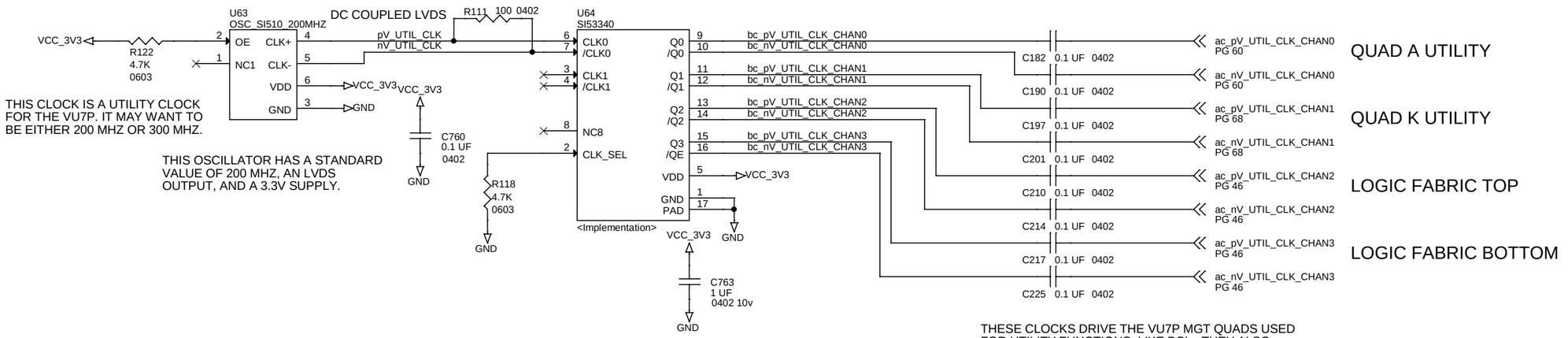
THE CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.




THESE CLOCKS DRIVE THE FIREFLY "GTY1" TRANSCEIVERS ON THE RIGHT SIDE OF THE VU7P.




THESE CLOCKS DRIVE THE FIREFLY "GTY2" TRANSCEIVERS ON THE LEFT SIDE OF THE VU7P.



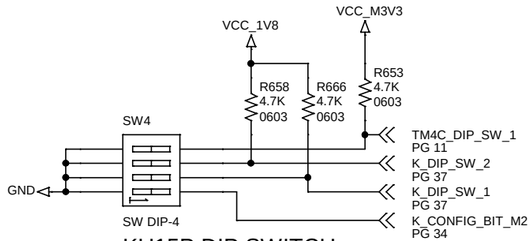

THESE CLOCKS DRIVE THE VU7P MGT QUADS USED FOR UTILITY FUNCTIONS, LIKE PCIe. THEY ALSO PROVIDE A CLOCK TO THE LOGIC FABRIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

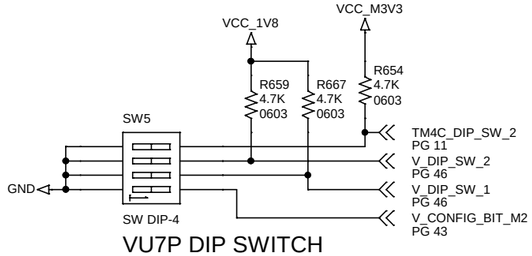
Title: 2.10: VU7P OSCILLATOR CLOCKING

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 16 of 74




KU15P DIP SWITCH

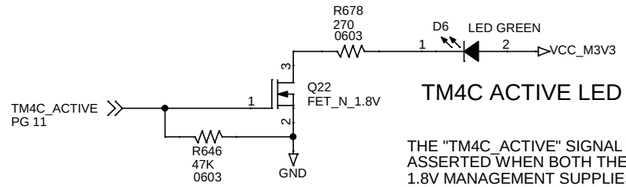



VU7P DIP SWITCH

SWITCH POSITION 4 IS USED TO TELL THE TM4C WHETHER OR NOT THE ASSOCIATED FPGA SHOULD BE POWERED. A HI LEVEL (SWITCH OPEN) MEANS "TURN ON FPGA POWER".

SWITCH POSITION 1 IS USED TO TELL THE FPGA WHETHER THE BOOT MODE IS "MASTER SPI (WITH JTAG OPTION)", OR "JTAG ONLY (MASTER SPI DISABLED)". A HI LEVEL (SWITCH OPEN) MEANS "JTAG ONLY (MASTER SPI DISABLED)"

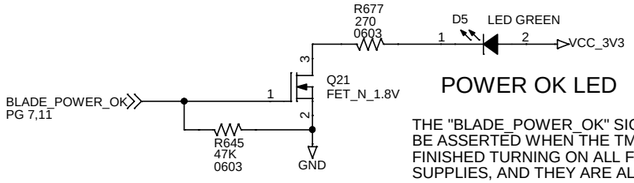
THE FUNCTION OF SWITCH POSITIONS 2 AND 3 ARE UNDEFINED AT THIS TIME.




TM4C ACTIVE LED

THE "TM4C_ACTIVE" SIGNAL WILL BE ASSERTED WHEN BOTH THE 3.3V AND 1.8V MANAGEMENT SUPPLIES ARE GOOD, THE "ENABLE" SIGNAL FROM THE SERVICE BLADE IS HIGH, AND THE "RESET" SWITCH IS NOT ACTIVATED.

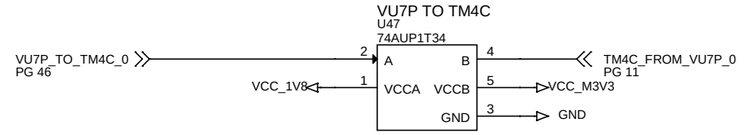
FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

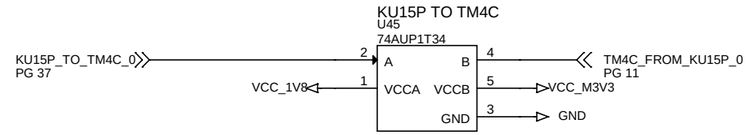


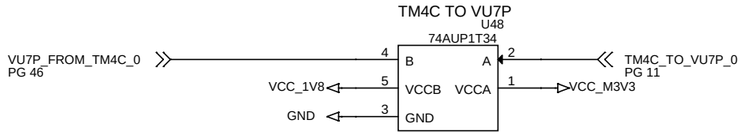

POWER OK LED

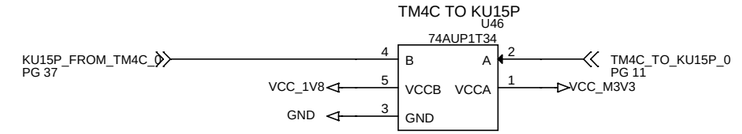
THE "BLADE_POWER_OK" SIGNAL WILL BE ASSERTED WHEN THE TM4C HAS FINISHED TURNING ON ALL FPGA POWER SUPPLIES, AND THEY ARE ALL GOOD.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

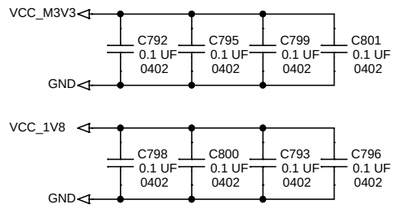


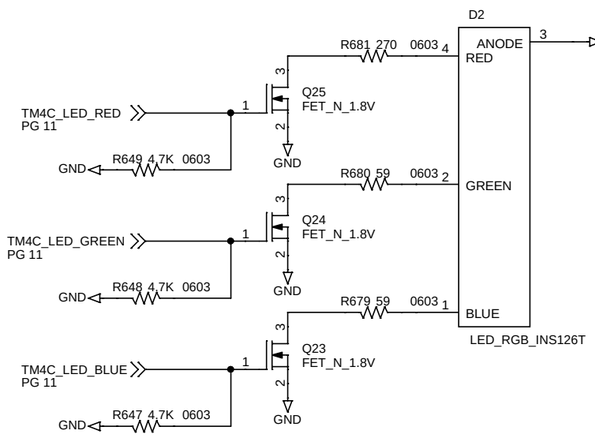




UTILITY CONNECTIONS BETWEEN THE TM4C CONTROLLER AND THE FPGAS. THE LEVEL TRANSLATORS ARE UNI-DIRECTIONAL.

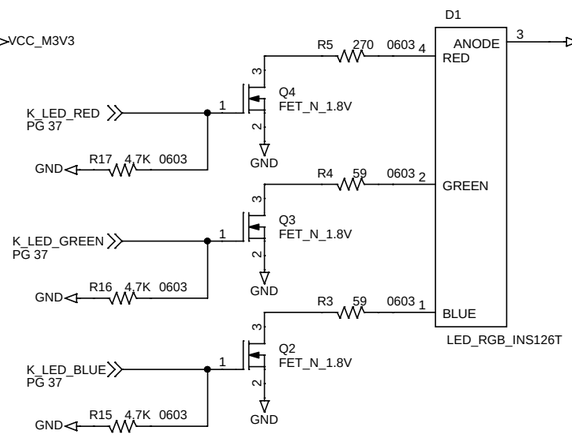



FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROPS ARE:
RED 2.0V. USE 270 OHM RESISTOR
BLUE 3.0V. USE 59 OHM RESISTOR
GREEN 3.0V. USE 59 OHM RESISTOR

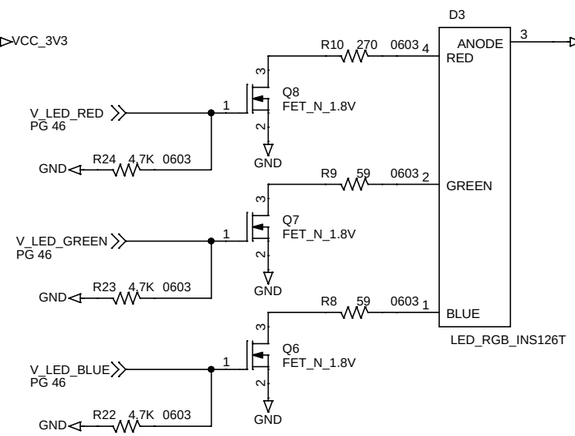
TM4C CONTROLLER LED




KU15P LED




VU7P LED




| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 2.11: LEDS, SWITCHES, LEVEL SHIFTERS | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Thursday, March 07, 2019 | Sheet 17 of 74 | |

U69
K_VCCINT_PG_A_1 PG 20
K_VCCINT_PG_A_2 PG 20
K_VCCINT_PG_A
VCC_M3V3
GND
74LVC1G08

U70
K_VCCINT_PG_B_1 PG 20
K_VCCINT_PG_B_2 PG 20
K_VCCINT_PG_B
VCC_M3V3
GND
74LVC1G08

U75
V_VCCINT_PG_A_1 PG 22
V_VCCINT_PG_A_2 PG 22
V_VCCINT_PG_A
VCC_M3V3
GND
74LVC1G08

U76
V_VCCINT_PG_B_1 PG 22
V_VCCINT_PG_B_2 PG 22
V_VCCINT_PG_B
VCC_M3V3
GND
74LVC1G08

USE 2-INPUT "AND" GATES TO COMBINE "PG" PINS FROM THE SAME MODULE AND SAVE CONTROLLER PINS

U52-6
TM4C1290NCPDT

| | | | | | |
|---|---|---|---|---|---|
| K_VCCINT_PG_A | 61 | PK5 | PF2 | 44 | CTRL_K_VCCINT_PWR_EN |
| K_VCCINT_PG_B | 60 | PK6 | | | |
| V_VCCINT_PG_A | 32 | PH3 | PA4 | 37 | CTRL_V_VCCINT_PWR_EN |
| V_VCCINT_PG_B | 31 | PH2 | PP4 | 105 | TP3 T POINT F |
| | | | PP3 | 104 | TP2 T POINT F |
| VCC_3V3_PG PG 19 | 30 | PH1 | PF1 | 43 | CTRL_VCC_3V3_PWR_EN |
| VCC_1V8_PG PG 19 | 29 | PH0 | PA5 | 38 | CTRL_VCC_1V8_PWR_EN |
| | | | PN5 | 112 | CTRL_V_MGTY1_VCCAUX_EN |
| | | | PN4 | 111 | CTRL_V_MGTY2_VCCAUX_EN |
| | | | PL2 | 83 | CTRL_K_MGTY_VCCAUX_EN |
| | | | PL3 | 84 | CTRL_K_MGTH_VCCAUX_EN |
| K_MGTY_AVCC_OK PG 21 | 76 | PM2 | PL4 | 85 | CTRL_K_MGTY_AVCC_PWR_EN |
| K_MGTH_AVCC_OK PG 21 | 75 | PM3 | PL5 | 86 | CTRL_K_MGTH_AVCC_PWR_EN |
| K_MGTY_AVTT_OK PG 21 | 77 | PM1 | PQ4 | 102 | CTRL_K_MGTY_AVTT_PWR_EN |
| K_MGTH_AVTT_OK PG 21 | 74 | PM4 | PP2 | 103 | CTRL_K_MGTH_AVTT_PWR_EN |
| V_MGTY2_AVTT_OK PG 23 | 25 | PC4 | PN0 | 107 | CTRL_V_MGTY2_AVTT_PWR_EN |
| V_MGTY1_AVTT_OK PG 23 | 22 | PC7 | PN1 | 108 | CTRL_V_MGTY1_AVTT_PWR_EN |
| V_MGTY2_AVCC_OK PG 23 | 24 | PC5 | PN2 | 109 | CTRL_V_MGTY2_AVCC_PWR_EN |
| V_MGTY1_AVCC_OK PG 23 | 23 | PC6 | PN3 | 110 | CTRL_V_MGTY1_AVCC_PWR_EN |

U71
CTRL_K_VCCINT_PWR_EN
R454 4.7K 0603
K_VCCINT_PWR_EN PG 20
VCC_M3V3
GND
74LVC1G08

U74
CTRL_V_VCCINT_PWR_EN
R457 4.7K 0603
V_VCCINT_PWR_EN PG 22
74LVC1G08

U72
CTRL_VCC_3V3_PWR_EN
R455 4.7K 0603
VCC_3V3_PWR_EN PG 19
74LVC1G08

U73
CTRL_VCC_1V8_PWR_EN
R456 4.7K 0603
VCC_1V8_PWR_EN PG 19
74LVC1G08

CTRL_V_MGTY1_VCCAUX_EN
R498 4.7K 0603
Q15 FET_N_1.8V
/V_MGTY1_VCCAUX_EN PG 42

CTRL_V_MGTY2_VCCAUX_EN
R405 4.7K 0603
Q13 FET_N_1.8V
/V_MGTY2_VCCAUX_EN PG 42

CTRL_K_MGTY_VCCAUX_EN
R501 4.7K 0603
Q16 FET_N_1.8V
/K_MGTY_VCCAUX_EN PG 33

CTRL_K_MGTH_VCCAUX_EN
R460 4.7K 0603
Q14 FET_N_1.8V
/K_MGTH_VCCAUX_EN PG 33

THE ACTIVE-HI "ENABLE" SIGNALS WILL ONLY BE ASSERTED WHEN VCC_M3V3 IS PRESENT AND THE CONTROLLER OUTPUT IS HIGH. OTHERWISE, PULLDOWN RESISTORS ON THE GATE INPUT AND THE POWER MODULE INPUT WILL KEEP THE ENABLE SIGNALS LOW.

CTRL_K_MGTY_AVCC_PWR_EN
R591 4.7K 0603
Q17 FET_N_1.8V
/K_MGTY_AVCC_PWR_EN PG 21

CTRL_K_MGTH_AVCC_PWR_EN
R313 4.7K 0603
Q9 FET_N_1.8V
/K_MGTH_AVCC_PWR_EN PG 21

CTRL_K_MGTY_AVTT_PWR_EN
R594 4.7K 0603
Q18 FET_N_1.8V
/K_MGTY_AVTT_PWR_EN PG 21

CTRL_K_MGTH_AVTT_PWR_EN
R316 4.7K 0603
Q10 FET_N_1.8V
/K_MGTH_AVTT_PWR_EN PG 21

CTRL_V_MGTY2_AVTT_PWR_EN
R322 4.7K 0603
Q12 FET_N_1.8V
/V_MGTY2_AVTT_PWR_EN PG 23

CTRL_V_MGTY1_AVTT_PWR_EN
R600 4.7K 0603
Q20 FET_N_1.8V
/V_MGTY1_AVTT_PWR_EN PG 23

CTRL_V_MGTY2_AVCC_PWR_EN
R319 4.7K 0603
Q11 FET_N_1.8V
/V_MGTY2_AVCC_PWR_EN PG 23

CTRL_V_MGTY1_AVCC_PWR_EN
R597 4.7K 0603
Q19 FET_N_1.8V
/V_MGTY1_AVCC_PWR_EN PG 23

THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. A VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

SPREAD THESE CAPACITORS AROUND THE BOARD

VCC_M3V3
C960 22 UF 6.3V 0603
C858 22 UF 6.3V 0603
C479 22 UF 6.3V 0603
C548 22 UF 6.3V 0603
GND

VCC_M1V8
C829 22 UF 6.3V 0603
C968 22 UF 6.3V 0603
GND

U31
TPS82130
VCC_12V
C15 10 UF 16V 0805
C834 3.3 NF 50V 0603
VIN
EN
SS/TR
VOUT
VOUT
FB
PG
GND
PAD
R28 110K 0603 0.1%
R29 34.8K 0603 0.1%
C52 22 UF 6.3V 0603
VCC_M3V3

THE VOLTAGE IS 3.33 VOLTS WITH RESISTORS OF 110K AND 34.8K.

U90
ADP1713_1V8
EN
IN
OUT
BYP
GND
C731 4.7 UF 0402
C732 0.1 UF 0402
C272 4.7 UF 0402
C260 0.1 UF 0402
C271 0.01 UF 0402
VCC_M1V8

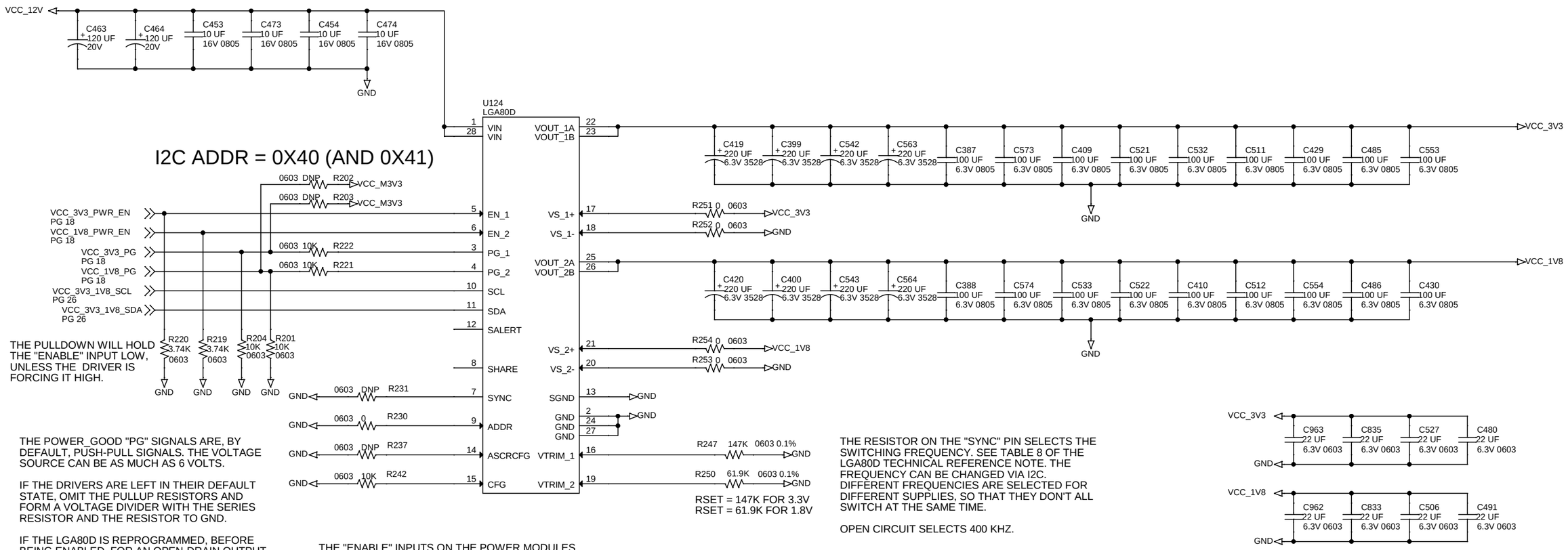
VCC_M3V3 AND VCC_M1V8 ARE THE "MANAGEMENT" POWER. THEY PROVIDE POWER TO THE POWER SEQUENCING CIRCUIT. THEY ARE ALWAYS ON WHEN +12V IS SUPPLIED TO THE BOARD.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.01: POWER CONTROL

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Monday, April 22, 2019 Sheet 18 of 74




# I2C ADDR = 0X40 (AND 0X41)

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=10K SELECTS 2-OUTPUT @ 25A EACH.

THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

RSET = 147K FOR 3.3V
RSET = 61.9K FOR 1.8V

THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

OPEN CIRCUIT SELECTS 400 KHZ.

THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. EVEN THOUGH EACH LGA80D IS ON A DIFFERENT I2C BUS, UNIQUE ADDRESS ARE ASSIGNE TO EACH. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

3.3/1.8V: R=0 -> ADDR = 0X40 (AND 0X41)
K_VCCINT MASTER: R=12.1K -> ADDR = 0X44
K_VCCINT SLAVE: R=11K -> ADDR = 0X43
V_VCCINT MASTER: R=14.7K -> ADDR = 0X46
V_VCCINT SLAVE: R=13.3K -> ADDR = 0X45




SPREAD THESE CAPACITORS AROUND THE BOARD

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 3.02: POWER GLOBAL 3.3V AND 1.8V | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, April 09, 2019 | Sheet 19 of 74 | |

KU15P VCCINT MUST BE 0.85V.

U122
LGA80D

VCC_12V

C459 120 UF 20V
C460 120 UF 20V
C449 10 UF 16V 0805
C469 10 UF 16V 0805
C450 10 UF 16V 0805
C470 10 UF 16V 0805

GND

I2C ADDR = 0X44

0603 DNP R194 VCC_M3V3
0603 DNP R195 VCC_M3V3
0603 10K R216
0603 10K R215

K_VCCINT_PG_A_1 PG 18
K_VCCINT_PG_A_2 PG 18
K_VCCINT_A_SCL PG 26
K_VCCINT_A_SDA PG 26

R196 10K 0603
R193 10K 0603

K_VCCINT_PWR_EN PG 18

R213 3.74K 0603

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

0603 12.1K R227
0603 DNP R235
0603 90.9K R240

| | | | |
|---|---|---|---|
| 1 | VIN | VOUT_1A | 22 |
| 28 | VIN | VOUT_1B | 23 |
| 5 | EN_1 | VS_1+ | 17 |
| 6 | EN_2 | VS_1- | 18 |
| 3 | PG_1 | | |
| 4 | PG_2 | VOUT_2A | 25 |
| | | VOUT_2B | 26 |
| 10 | SCL | | |
| 11 | SDA | | |
| 12 | SALERT | | |
| | | VS_2+ | 21 |
| 8 | SHARE | VS_2- | 20 |
| 7 | SYNC | SGND | 13 |
| 9 | ADDR | GND | 2 |
| | | GND | 24 |
| | | GND | 27 |
| 14 | ASCRCFG | VTRIM_1 | 16 |
| 15 | CFG | VTRIM_2 | 19 |

A

R191 0 0603
R192 0 0603

K_VCCINT

C415 330 UF 2.5V 3528
C393 330 UF 2.5V 3528
C538 330 UF 2.5V 3528
C559 330 UF 2.5V 3528
C425 100 UF 4V 0805
C405 100 UF 4V 0805
C528 100 UF 4V 0805
C550 100 UF 4V 0805
C383 100 UF 4V 0805
C569 100 UF 4V 0805
C481 100 UF 4V 0805
C507 100 UF 4V 0805
C517 100 UF 4V 0805

C416 330 UF 2.5V 3528
C394 330 UF 2.5V 3528
C539 330 UF 2.5V 3528
C560 330 UF 2.5V 3528
C426 100 UF 4V 0805
C406 100 UF 4V 0805
C529 100 UF 4V 0805
C551 100 UF 4V 0805
C384 100 UF 4V 0805
C570 100 UF 4V 0805
C482 100 UF 4V 0805
C508 100 UF 4V 0805
C518 100 UF 4V 0805

R245 16.2K 0603 0.1%

RSET = 16.2K FOR 0.85V

U123
LGA80D

C461 120 UF 20V
C462 120 UF 20V
C451 10 UF 16V 0805
C471 10 UF 16V 0805
C452 10 UF 16V 0805
C472 10 UF 16V 0805

GND

I2C ADDR = 0X43

0603 DNP R198 VCC_M3V3
0603 DNP R199 VCC_M3V3
0603 10K R218
0603 10K R217

K_VCCINT_PG_B_1 PG 18
K_VCCINT_PG_B_2 PG 18
K_VCCINT_B_SCL PG 26
K_VCCINT_B_SDA PG 26

R200 10K 0603
R197 10K 0603

0603 21.5K R229
0603 11.0K R228
0603 DNP R236
0603 100K R241

| | | | |
|---|---|---|---|
| 1 | VIN | VOUT_1A | 22 |
| 28 | VIN | VOUT_1B | 23 |
| 5 | EN_1 | VS_1+ | 17 |
| 6 | EN_2 | VS_1- | 18 |
| 3 | PG_1 | | |
| 4 | PG_2 | VOUT_2A | 25 |
| | | VOUT_2B | 26 |
| 10 | SCL | | |
| 11 | SDA | | |
| 12 | SALERT | | |
| | | VS_2+ | 21 |
| 8 | SHARE | VS_2- | 20 |
| 7 | SYNC | SGND | 13 |
| 9 | ADDR | GND | 2 |
| | | GND | 24 |
| | | GND | 27 |
| 14 | ASCRCFG | VTRIM_1 | 16 |
| 15 | CFG | VTRIM_2 | 19 |

B

C417 330 UF 2.5V 3528
C396 330 UF 2.5V 3528
C540 330 UF 2.5V 3528
C561 330 UF 2.5V 3528
C427 100 UF 4V 0805
C407 100 UF 4V 0805
C530 100 UF 4V 0805
C552 100 UF 4V 0805
C385 100 UF 4V 0805
C571 100 UF 4V 0805
C519 100 UF 4V 0805
C509 100 UF 4V 0805
C483 100 UF 4V 0805

C418 330 UF 2.5V 3528
C397 330 UF 2.5V 3528
C541 330 UF 2.5V 3528
C562 330 UF 2.5V 3528
C428 100 UF 4V 0805
C408 100 UF 4V 0805
C531 100 UF 4V 0805
C549 100 UF 4V 0805
C386 100 UF 4V 0805
C572 100 UF 4V 0805
C520 100 UF 4V 0805
C510 100 UF 4V 0805
C484 100 UF 4V 0805

R246 16.2K 0603 0.1%

RSET = 16.2K FOR 0.85V

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=90.9K SELECTS 4-PHASE MASTER @ 35A EACH
R=100K SELECTS 4-PHASE SLAVE @ 35A EACH

THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

21.5K SELECTS 432 KHZ.

THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. EVEN THOUGH EACH LGA80D IS ON A DIFFERENT I2C BUS, UNIQUE ADDRESS ARE ASSIGNE TO EACH. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

3.3/1.8V: R=0 -> ADDR = 0X40 (AND 0X41)
K_VCCINT MASTER: R=12.1K -> ADDR = 0X44
K_VCCINT SLAVE: R=11K -> ADDR = 0X43
V_VCCINT MASTER: R=14.7K -> ADDR = 0X46
V_VCCINT SLAVE: R=13.3K -> ADDR = 0X45

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

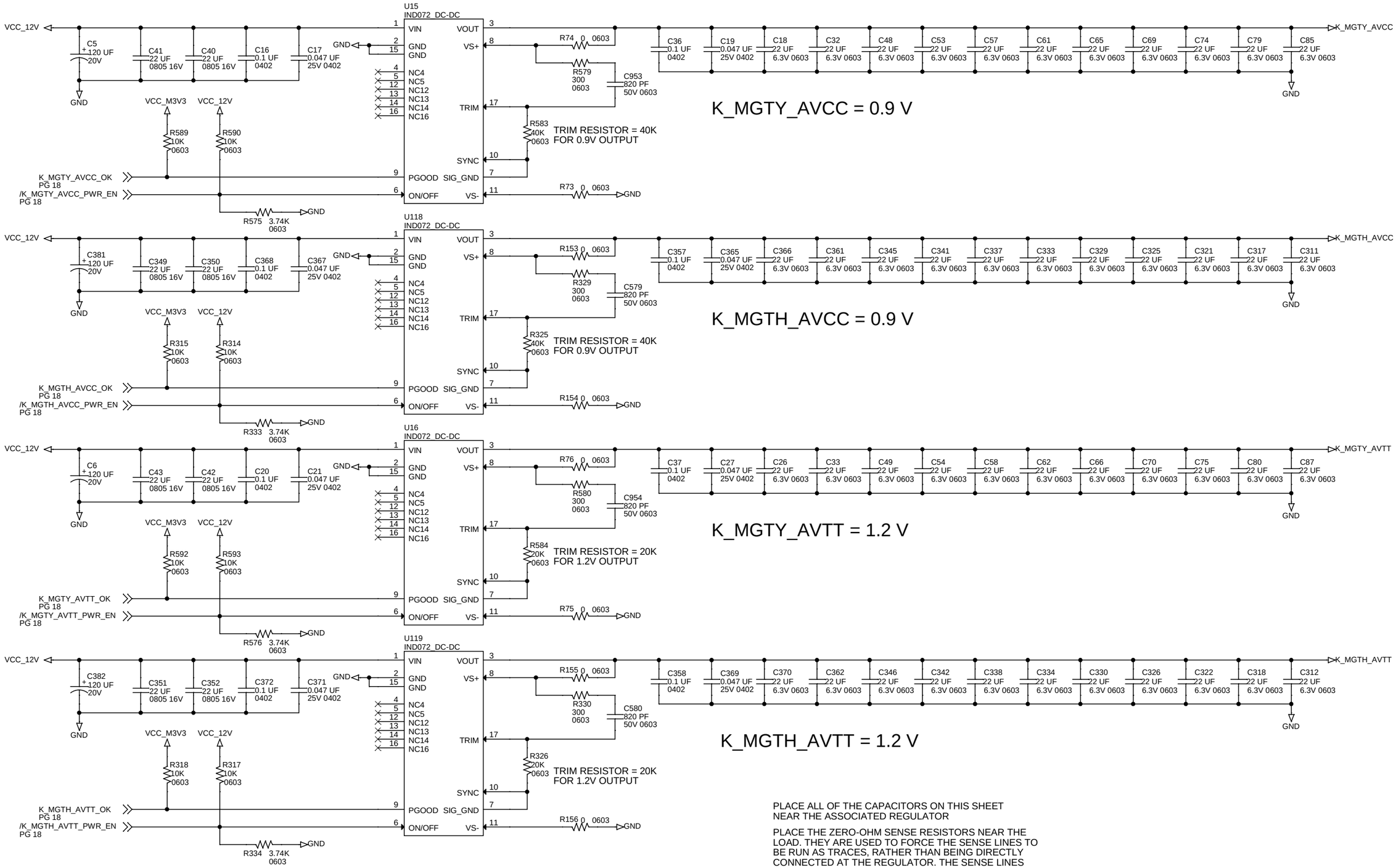
PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.03: POWER SOURCE KU15P INTERNAL

Size | Document Number: 6089-103 | Rev: A

Date: Thursday, March 07, 2019 Sheet 20 of 74




THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.04: POWER SOURCE KU15P MGT XCVR

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 21 of 74

VU7P VCCINT MUST BE 0.85V.

U125
LGA80D

VCC_12V

C465 120 UF 20V
C466 120 UF 20V
C455 10 UF 16V 0805
C475 10 UF 16V 0805
C456 10 UF 16V 0805
C476 10 UF 16V 0805

GND

I2C ADDR = 0X46

V_VCCINT_PG_A_1 PG 18
V_VCCINT_PG_A_2 PG 18
V_VCCINT_A_SCL PG 26
V_VCCINT_A_SDA PG 26

0603 DNP R206 VCC_M3V3
0603 DNP R207 VCC_M3V3
0603 10K R224
0603 10K R223

R208 10K 0603
R205 10K 0603

GND GND

V_VCCINT_PWR_EN PG 18

R214 3.74K 0603

THE PULLDOWN WILL HOLD THE "ENABLE" INPUT LOW, UNLESS THE DRIVER IS FORCING IT HIGH.

0603 14.7K R232
0603 DNP R238
0603 90.9K R243

| | | | |
|---|---|---|---|
| 1, 28 | VIN | VOUT_1A, VOUT_1B | 22, 23 |
| 5 | EN_1 | VS_1+ | 17 |
| 6 | EN_2 | VS_1- | 18 |
| 3 | PG_1 | | |
| 4 | PG_2 | VOUT_2A, VOUT_2B | 25, 26 |
| 10 | SCL | | |
| 11 | SDA | | |
| 12 | SALERT | | |
| | | VS_2+ | 21 |
| 8 | SHARE | VS_2- | 20 |
| 7 | SYNC | SGND | 13 GND |
| 9 | ADDR | GND, GND, GND | 2, 24, 27 GND |
| 14 | ASCRCFG | VTRIM_1 | 16 |
| 15 | CFG | VTRIM_2 | 19 |

A

R256 0 0603 V_VCCINT
R255 0 0603 GND

C421 330 UF 2.5V 3528
C401 330 UF 2.5V 3528
C544 330 UF 2.5V 3528
C565 330 UF 2.5V 3528
C431 100 UF 6.3V 0805
C411 100 UF 6.3V 0805
C534 100 UF 6.3V 0805
C555 100 UF 6.3V 0805
C389 100 UF 6.3V 0805
C575 100 UF 6.3V 0805
C523 100 UF 6.3V 0805
C513 100 UF 6.3V 0805
C487 100 UF 6.3V 0805

GND

C402 330 UF 2.5V 3528
C422 330 UF 2.5V 3528
C566 330 UF 2.5V 3528
C545 330 UF 2.5V 3528
C432 100 UF 6.3V 0805
C412 100 UF 6.3V 0805
C535 100 UF 6.3V 0805
C556 100 UF 6.3V 0805
C390 100 UF 6.3V 0805
C576 100 UF 6.3V 0805
C524 100 UF 6.3V 0805
C514 100 UF 6.3V 0805
C488 100 UF 6.3V 0805

GND

R248 16.2K 0603 0.1% GND

RSET = 16.2K FOR 0.85V

V_VCCINT

U126
LGA80D

C467 120 UF 20V
C468 120 UF 20V
C457 10 UF 16V 0805
C477 10 UF 16V 0805
C458 10 UF 16V 0805
C478 10 UF 16V 0805

GND

I2C ADDR = 0X45

V_VCCINT_PG_B_1 PG 18
V_VCCINT_PG_B_2 PG 18
V_VCCINT_B_SCL PG 26
V_VCCINT_B_SDA PG 26

0603 DNP R210 VCC_M3V3
0603 DNP R211 VCC_M3V3
0603 10K R226
0603 10K R225

R212 10K 0603
R209 10K 0603

GND GND

0603 23.7K R234
0603 13.3K R233
0603 DNP R239
0603 100K R244

| | | | |
|---|---|---|---|
| 1, 28 | VIN | VOUT_1A, VOUT_1B | 22, 23 |
| 5 | EN_1 | VS_1+ | 17 |
| 6 | EN_2 | VS_1- | 18 |
| 3 | PG_1 | | |
| 4 | PG_2 | VOUT_2A, VOUT_2B | 25, 26 |
| 10 | SCL | | |
| 11 | SDA | | |
| 12 | SALERT | | |
| | | VS_2+ | 21 |
| 8 | SHARE | VS_2- | 20 |
| 7 | SYNC | SGND | 13 GND |
| 9 | ADDR | GND, GND, GND | 2, 24, 27 GND |
| 14 | ASCRCFG | VTRIM_1 | 16 |
| 15 | CFG | VTRIM_2 | 19 |

B

C423 330 UF 2.5V 3528
C403 330 UF 2.5V 3528
C546 330 UF 2.5V 3528
C567 330 UF 2.5V 3528
C433 100 UF 6.3V 0805
C413 100 UF 6.3V 0805
C536 100 UF 6.3V 0805
C557 100 UF 6.3V 0805
C391 100 UF 6.3V 0805
C577 100 UF 6.3V 0805
C525 100 UF 6.3V 0805
C515 100 UF 6.3V 0805
C489 100 UF 6.3V 0805

GND

C424 330 UF 2.5V 3528
C404 330 UF 2.5V 3528
C568 330 UF 2.5V 3528
C547 330 UF 2.5V 3528
C434 100 UF 6.3V 0805
C414 100 UF 6.3V 0805
C537 100 UF 6.3V 0805
C558 100 UF 6.3V 0805
C392 100 UF 6.3V 0805
C578 100 UF 6.3V 0805
C490 100 UF 6.3V 0805
C516 100 UF 6.3V 0805
C526 100 UF 6.3V 0805

GND

R249 16.2K 0603 0.1% GND

RSET = 16.2K FOR 0.85V

V_VCCINT

THE POWER_GOOD "PG" SIGNALS ARE, BY DEFAULT, PUSH-PULL SIGNALS. THE VOLTAGE SOURCE CAN BE AS MUCH AS 6 VOLTS.

IF THE DRIVERS ARE LEFT IN THEIR DEFAULT STATE, OMIT THE PULLUP RESISTORS AND FORM A VOLTAGE DIVIDER WITH THE SERIES RESISTOR AND THE RESISTOR TO GND.

IF THE LGA80D IS REPROGRAMMED, BEFORE BEING ENABLED, FOR AN OPEN-DRAIN OUTPUT, THEN OMIT THE RESISTOR TO GND, INSERT THE PULLUP RESISTOR, AND MAKE THE SERIES RESISTOR BE A ZERO-OHM JUMPER.

THE "ENABLE" INPUTS ON THE POWER MODULES MUST BE HIGH FOR THE MODULES TO OPERATE.

THE RESISTOR ON THE "CFG" PIN SELECTS THE OPERATING MODE. SEE TABLE 9 OF THE LGA80D TECHNICAL REFERENCE NOTE.

R=90.9K SELECTS 4-PHASE MASTER @ 35A EACH
R=100K SELECTS 4-PHASE SLAVE @ 35A EACH

THE RESISTOR ON THE "ASCRCFG" PIN CONTROLS THE CHARGE MODE. SEE TABLE 10 OF THE LGA80D TECHNICAL REFERENCE NOTE.

WITHOUT PRIOR KNOWLEDGE OF THE PERFORMANCE, LEAVE THESE PINS "OPEN" FOR GAINS OF 500.

THE RESISTOR ON THE "SYNC" PIN SELECTS THE SWITCHING FREQUENCY. SEE TABLE 8 OF THE LGA80D TECHNICAL REFERENCE NOTE. THE FREQUENCY CAN BE CHANGED VIA I2C. DIFFERENT FREQUENCIES ARE SELECTED FOR DIFFERENT SUPPLIES, SO THAT THEY DON'T ALL SWITCH AT THE SAME TIME.

23.7K SELECTS 457 KHZ.

THE RESISTOR ON THE "ADDR" PIN SELECTS THE MODULE'S I2C (OR SMBUS) ADDRESS. SEE TABLE 7 OF THE LGA80D TECHNICAL REFERENCE NOTE. EVEN THOUGH EACH LGA80D IS ON A DIFFERENT I2C BUS, UNIQUE ADDRESS ARE ASSIGNE TO EACH. THERE ARE RULES ABOUT 2-OUTPUT MODULES, AND 4 -PHASE MASTER/SLAVE MODULES.

3.3/1.8V: R=0 -> ADDR = 0X40 (AND 0X41)
K_VCCINT MASTER: R=12.1K -> ADDR = 0X44
K_VCCINT SLAVE: R=11K -> ADDR = 0X43
V_VCCINT MASTER: R=14.7K -> ADDR = 0X46
V_VCCINT SLAVE: R=13.3K -> ADDR = 0X45

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

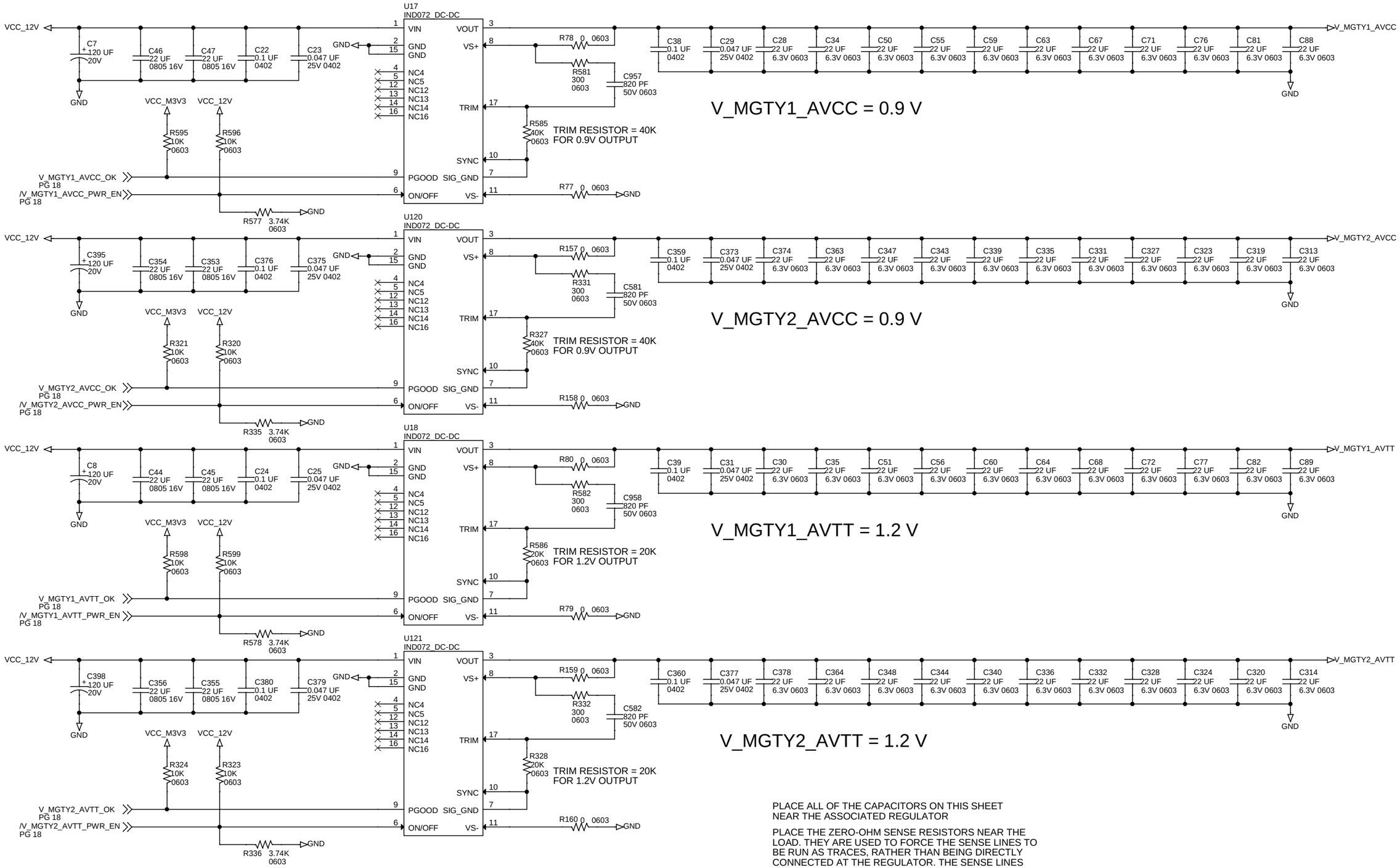
PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 3.05: POWER SOURCE VU7P INTERNAL

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Thursday, March 07, 2019 Sheet 22 of 74




THE "ON/OFF" INPUTS ON THE IND072 POWER MODULES MUST BE LOW FOR THE MODULES TO OPERATE. THE FET DRIVER WILL PULL THE "ON/OFF" INPUTS LOW WHENEVER THE INPUT TO THE DRIVER IS HIGH. THE VOLTAGE DIVIDER KEEPS THE "ON/OFF" INPUT HIGH UNLESS IT IS ACTIVELY PULLED LOW.

PLACE ALL OF THE CAPACITORS ON THIS SHEET NEAR THE ASSOCIATED REGULATOR

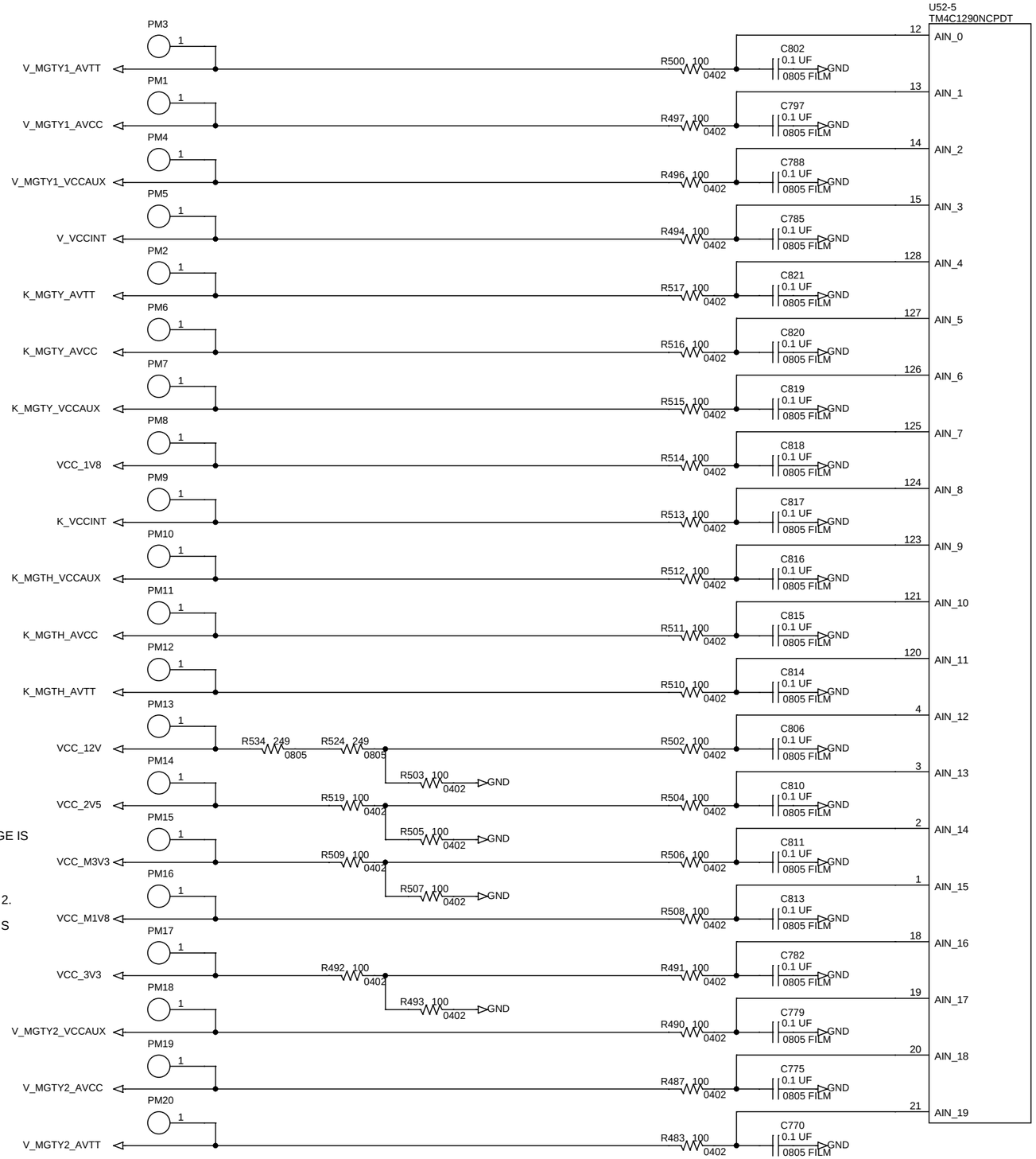
PLACE THE ZERO-OHM SENSE RESISTORS NEAR THE LOAD. THEY ARE USED TO FORCE THE SENSE LINES TO BE RUN AS TRACES, RATHER THAN BEING DIRECTLY CONNECTED AT THE REGULATOR. THE SENSE LINES SHOULD BE RUN AS A DIFFERENTIAL PAIR.

THE IND072 REGULATORS HAVE A TUNABLE LOOP THAT SHOULD BE ADJUSTED FOR THE AMOUNT OF CAPACITANCE THAT IS ON THE OUTPUT. REFER TO THE APP NOTE FOR SUGGESTED VALUES.

THE ON/OFF PIN NEEDS TO BE HELD AT A LOW LOGIC LEVEL TO TURN THE MODULE ON.

THE "PGOOD" SIGNAL WILL BE PULLED LOW IF THE OUTPUT VOLTAGE IS OUTSIDE OF 10% OF THE SETPOINT VALUE.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 3.06: POWER SOURCE VU7P MGT XCVR | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 23 of 74 | |




THE FULL SCALE ADC VOLTAGE IS 2.5 VOLTS, AS SET BY THE VOLTAGE REFERENCE.

THE 2.5 VOLT AND 3.3 VOLT SUPPLY LEVEL IS DIVIDED BY 2.

THE 12 VOLT SUPPLY LEVEL IS DIVIDED BY 6.

TEST POINTS TO MEASURE VOLTAGES

PM21 GND
PM22 GND
PM23 GND
PM24 GND
PM25 GND
PM26 GND

THE ANTI-ALIASING CUTOFF FREQUENCY IS 15.9 KHZ

A 16 MHZ ADC CLOCK PROVIDES A SAMPLING RATE OF 1 MEGA-SAMPLES PER SECOND. IF ALL 20 ADC CHANNELS ARE USED, THE SAMPLE RATE PER CHANNEL IS 50 KILO-SAMPLES PER SECOND, AND THE NYQUIST FREQUENCY IS 25 KHZ.

THE MAXIMUM SOURCE IMPEDANCE FEEDING THE ADC INPUTS IS 500 OHMS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

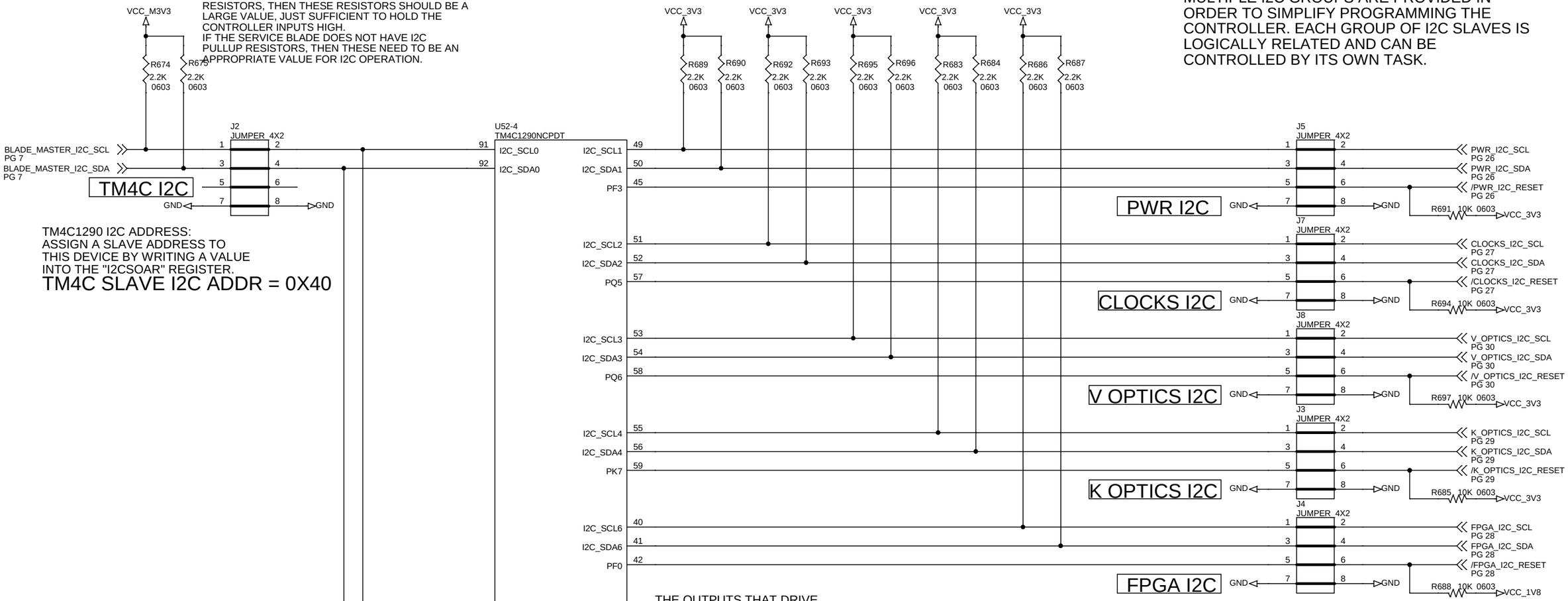
Title: 3.07: POWER MEASUREMENT

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 24 of 74

IF THE SERVICE BLADE HAS I2C PULLUP RESISTORS, THEN THESE RESISTORS SHOULD BE A LARGE VALUE, JUST SUFFICIENT TO HOLD THE CONTROLLER INPUTS HIGH.
IF THE SERVICE BLADE DOES NOT HAVE I2C PULLUP RESISTORS, THEN THESE NEED TO BE AN APPROPRIATE VALUE FOR I2C OPERATION.

MULTIPLE I2C GROUPS ARE PROVIDED IN ORDER TO SIMPLIFY PROGRAMMING THE CONTROLLER. EACH GROUP OF I2C SLAVES IS LOGICALLY RELATED AND CAN BE CONTROLLED BY ITS OWN TASK.

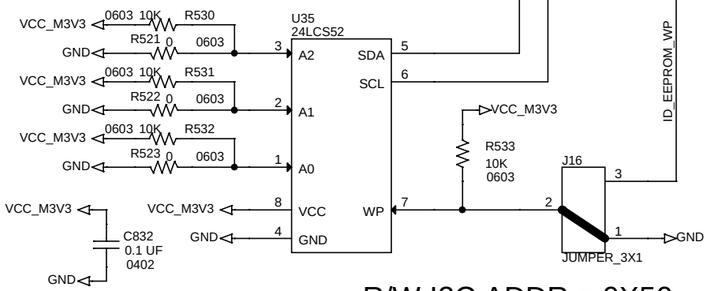



TM4C1290 I2C ADDRESS:
ASSIGN A SLAVE ADDRESS TO THIS DEVICE BY WRITING A VALUE INTO THE "I2CSOAR" REGISTER.

TM4C SLAVE I2C ADDR = 0X40

THE OUTPUTS THAT DRIVE THE "RESET" SIGNALS NEED TO BE OPEN-DRAIN.

THIS EEPROM IS FOR STORING UNCHANGING INFORMATION, LIKE SERIAL NUMBERS OR OTHER BOARD IDENTIFIERS.




24LCS52 I2C ADDRESS:
READ OR WRITE
1 0 1 0 A2 A1 A0
RANGE: 0X50 TO 0X57
WRITE-PROTECT REGISTER
0 1 1 0 A2 A1 A0

R/W I2C ADDR = 0X50

WP I2C ADDR = 0X30

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

THIS JUMPER CONFIGURES THE HARDWARE WRITE-PROTECT PIN.

IF NO JUMPER IS IN PLACE, THE HARDWARE WRITE PROTECTION IS ALWAYS ENABLED.

IF THE JUMPER CONNECTS PINS 1 AND 2, THE HARDWARE WRITE PROTECTION IS ALWAYS DISABLED.

IF THE JUMPER CONNECTS PINS 2 AND 3, THE HARDWARE PROTECTION IS CONTROLLED BY A GPIO PIN ON THE CONTROLLER.

REFER TO THE DATA SHEET FOR DETAILS ABOUT CONNECTING AN EXTERNAL HIGH VOLTAGE TO RESET THE SOFTWARE WRITE PROTECT FUSE.

HEADERS ARE PROVIDED TO SUPPORT DRIVING ANY I2C BUS WITH A STAND-ALONE USB-TO-I2C CONTROLLER.

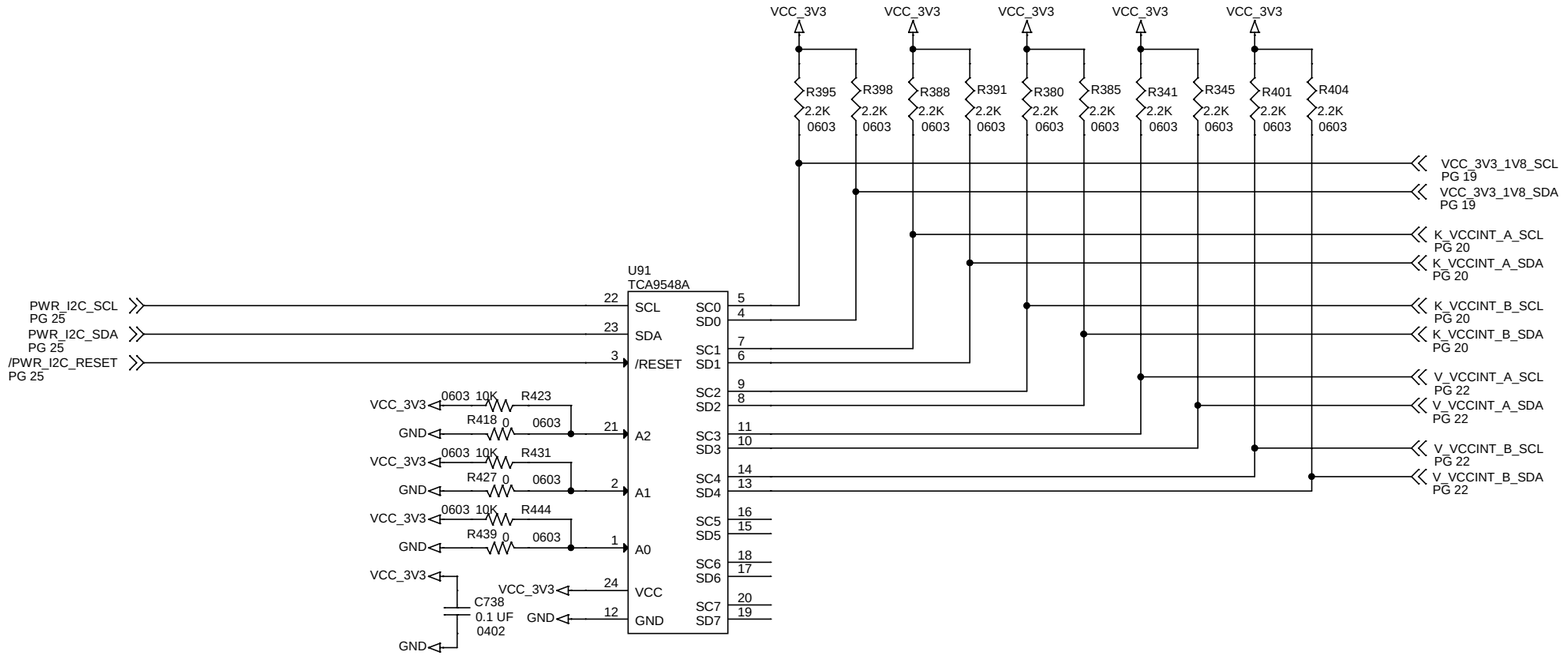
NORMALLY, JUMPERS WILL CONNECT THE ON-BOARD "SCL", "SDA", AND "/RESET" SIGNALS STRAIGHT THROUGH THE HEADERS.

TO CONNECT THE STAND-ALONE CONTROLLER, PULL THE JUMPERS FROM THE HEADER AND CONNECT THE CONTROLLER'S SIGNALS TO PINS 2, 4, AND 6, AND CONNECT GND TO PIN 8.

CONFIGURE THE "SPI MISO" PIN ON THE AARDVARK CONTROLLER AS A "GPIO OUTPUT" TO CONTROL THE "RESET" SIGNAL.

THIS LAYOUT ASSUMES THAT THE STAND-ALONE CONTROLLER PROVIDES PULL-UP RESISTORS ON THE I2C SIGNALS.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 4.01: I2C CONTROLLER | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, April 16, 2019 | Sheet 25 of 74 | |



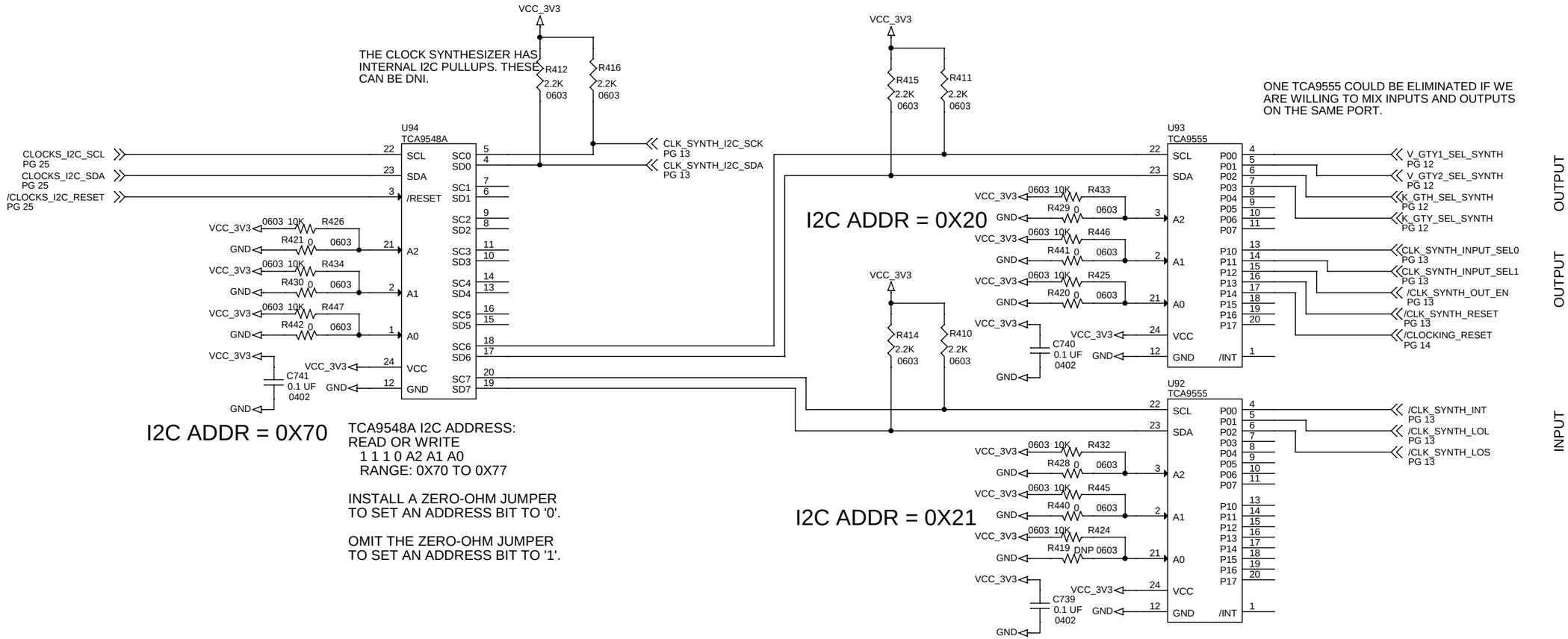

I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER
TO SET AN ADDRESS BIT TO '1'.

| | | | |
|---|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | | |
| Title: 4.02: I2C POWER CONTROL | | | |
| Size | Document Number: 6089-103 | | Rev: A |
| Date: Thursday, March 07, 2019 | | Sheet 26 of 74 | |



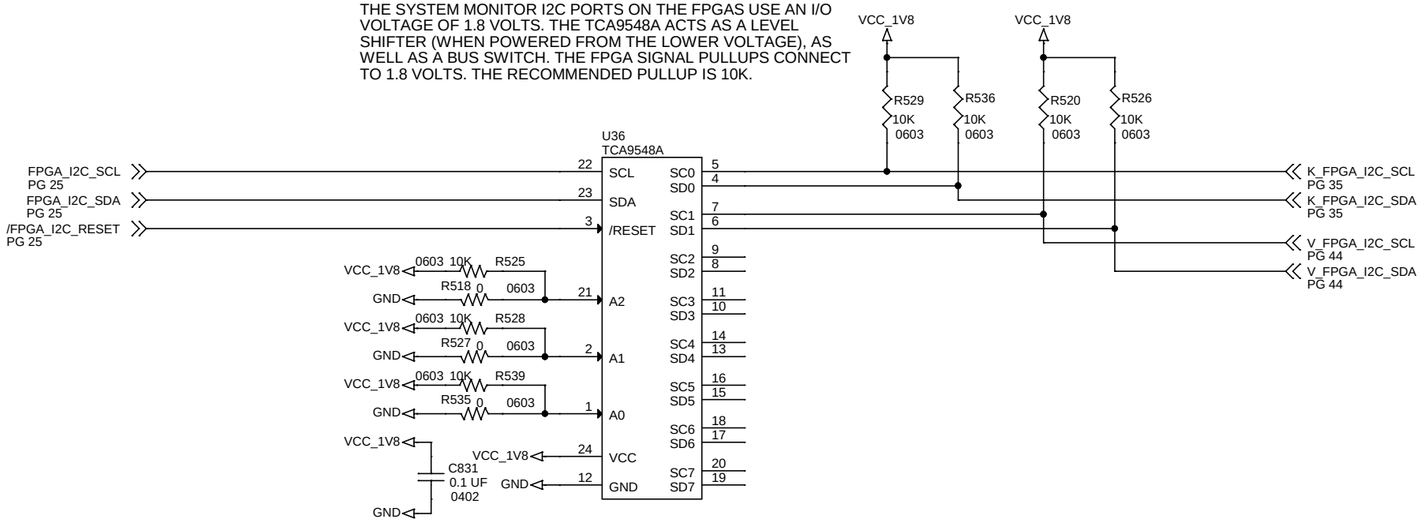

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 4.03: I2C CLOCK SOURCE CONTROL

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Thursday, March 07, 2019 Sheet 27 of 74

THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER (WHEN POWERED FROM THE LOWER VOLTAGE), AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS. THE RECOMMENDED PULLUP IS 10K.




I2C ADDR = 0X70

TCA9548A I2C ADDRESS:
READ OR WRITE
1 1 1 0 A2 A1 A0
RANGE: 0X70 TO 0X77

INSTALL A ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '0'.

OMIT THE ZERO-OHM JUMPER TO SET AN ADDRESS BIT TO '1'.

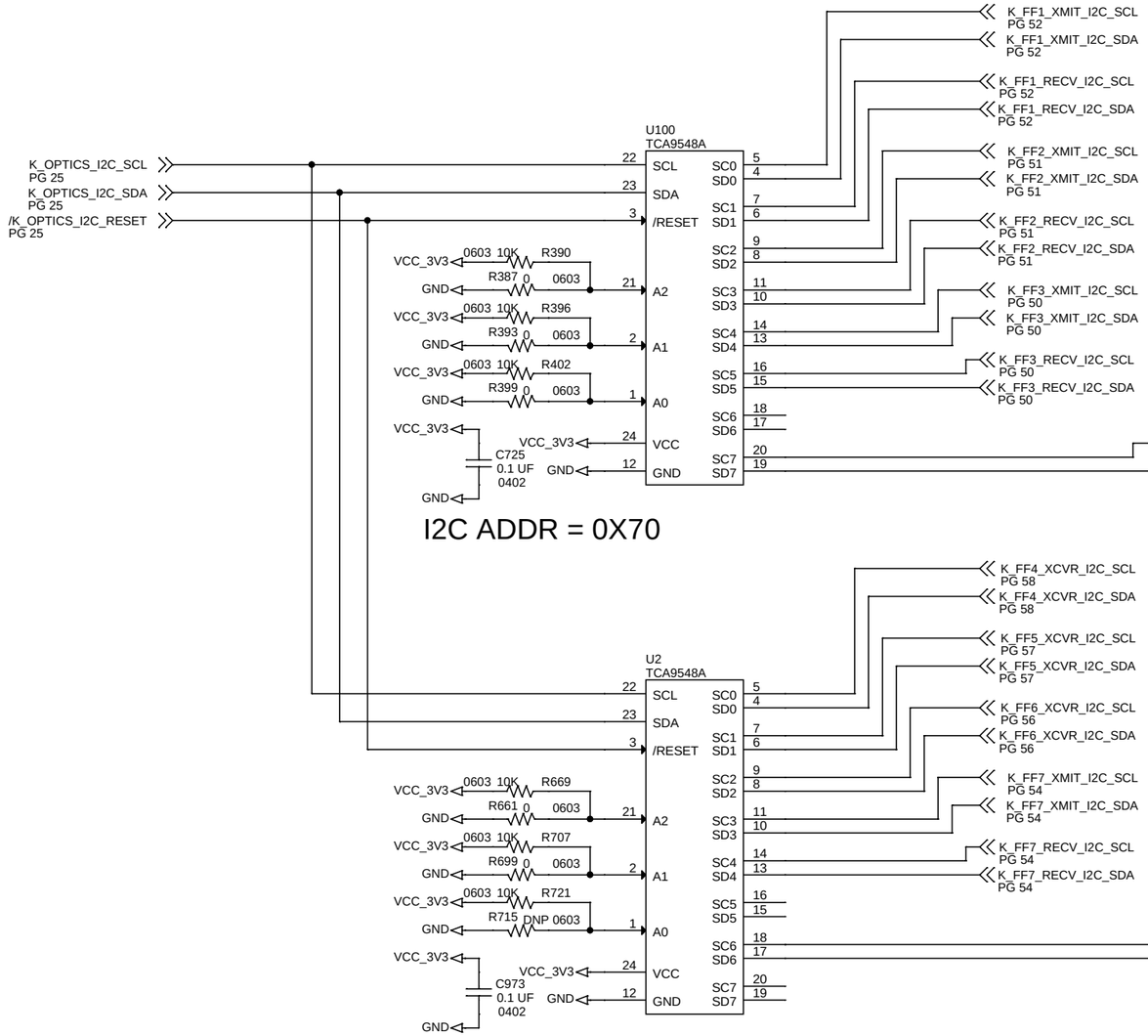
| A2 | A1 | A0 | I2C BUS SLAVE ADDRESS |
|---|---|---|---|
| L | L | L | 112 (decimal), 70 (hexadecimal) |
| L | L | H | 113 (decimal), 71 (hexadecimal) |
| L | H | L | 114 (decimal), 72 (hexadecimal) |
| L | H | H | 115 (decimal), 73 (hexadecimal) |
| H | L | L | 116 (decimal), 74 (hexadecimal) |
| H | L | H | 117 (decimal), 75 (hexadecimal) |
| H | H | L | 118 (decimal), 76 (hexadecimal) |
| H | H | H | 119 (decimal), 77 (hexadecimal) |

ATCA FPGA BOARD, KU15P AND VU7P, MK1

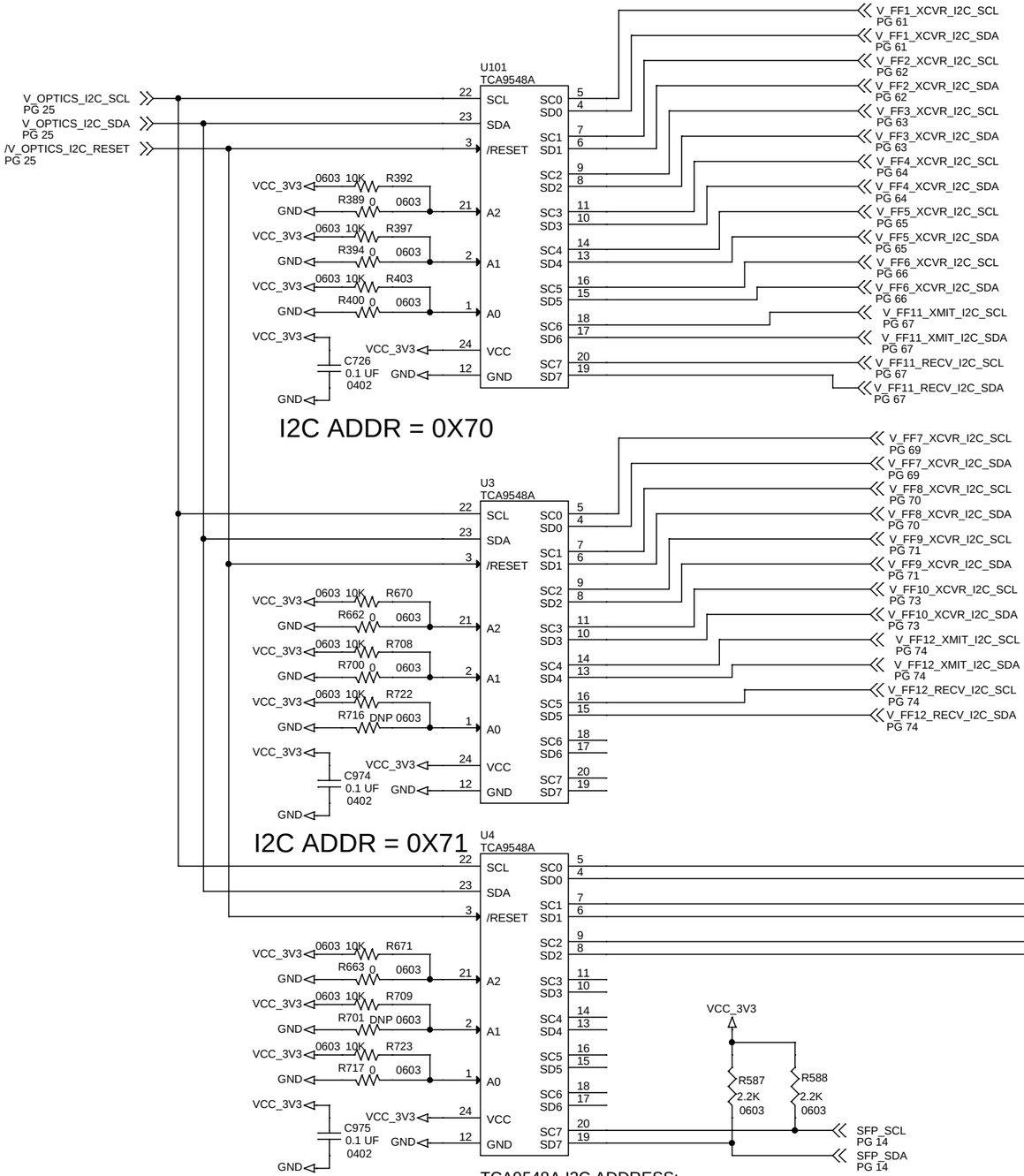
Title: 4.04: I2C FPGA SYSMON

Size | Document Number: 6089-103 | Rev: A

Date: Thursday, March 07, 2019 Sheet 28 of 74




| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 4.05: I2C KU15P OPTICS | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Thursday, March 07, 2019 | Sheet 29 of 74 | |

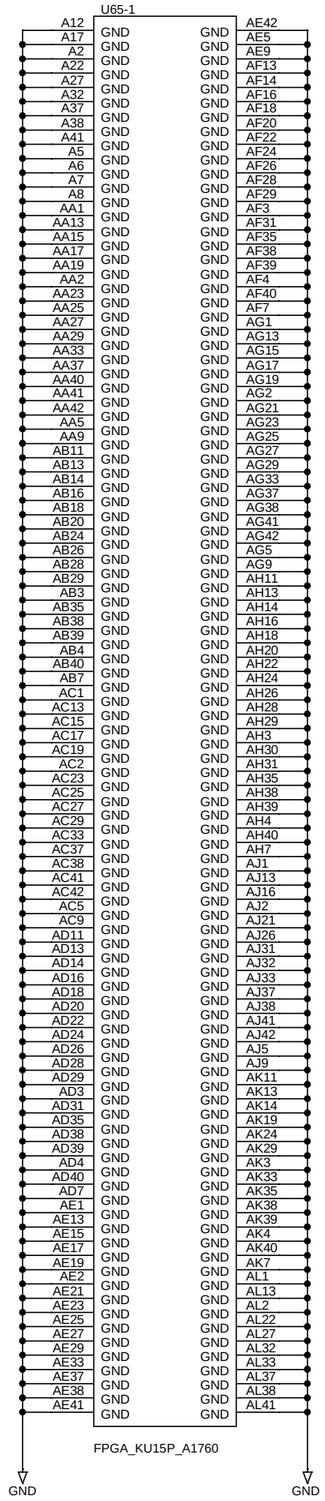


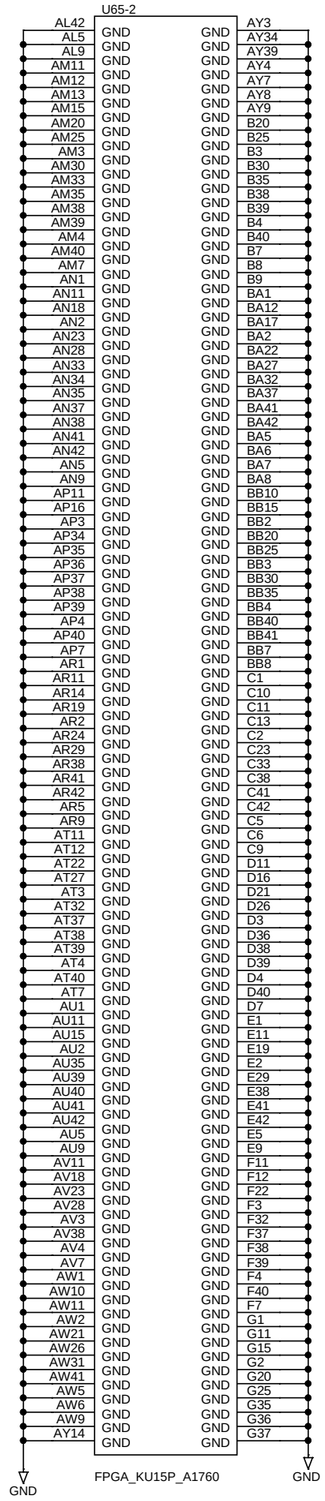

ATCA FPGA BOARD, KU15P AND VU7P, MK1

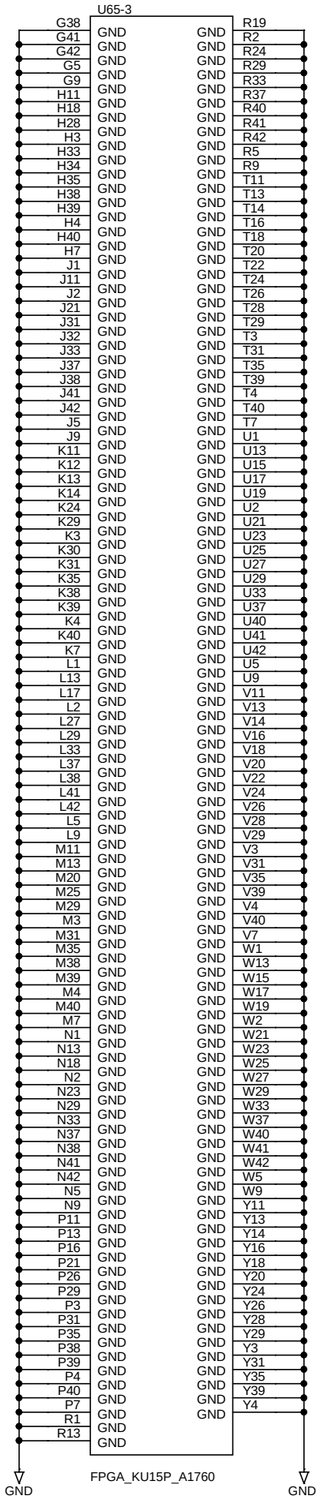
Title: 4.06: I2C VU7P OPTICS

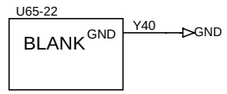
| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

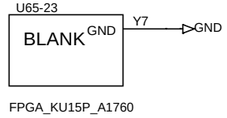
Date: Thursday, March 07, 2019 Sheet 30 of 74



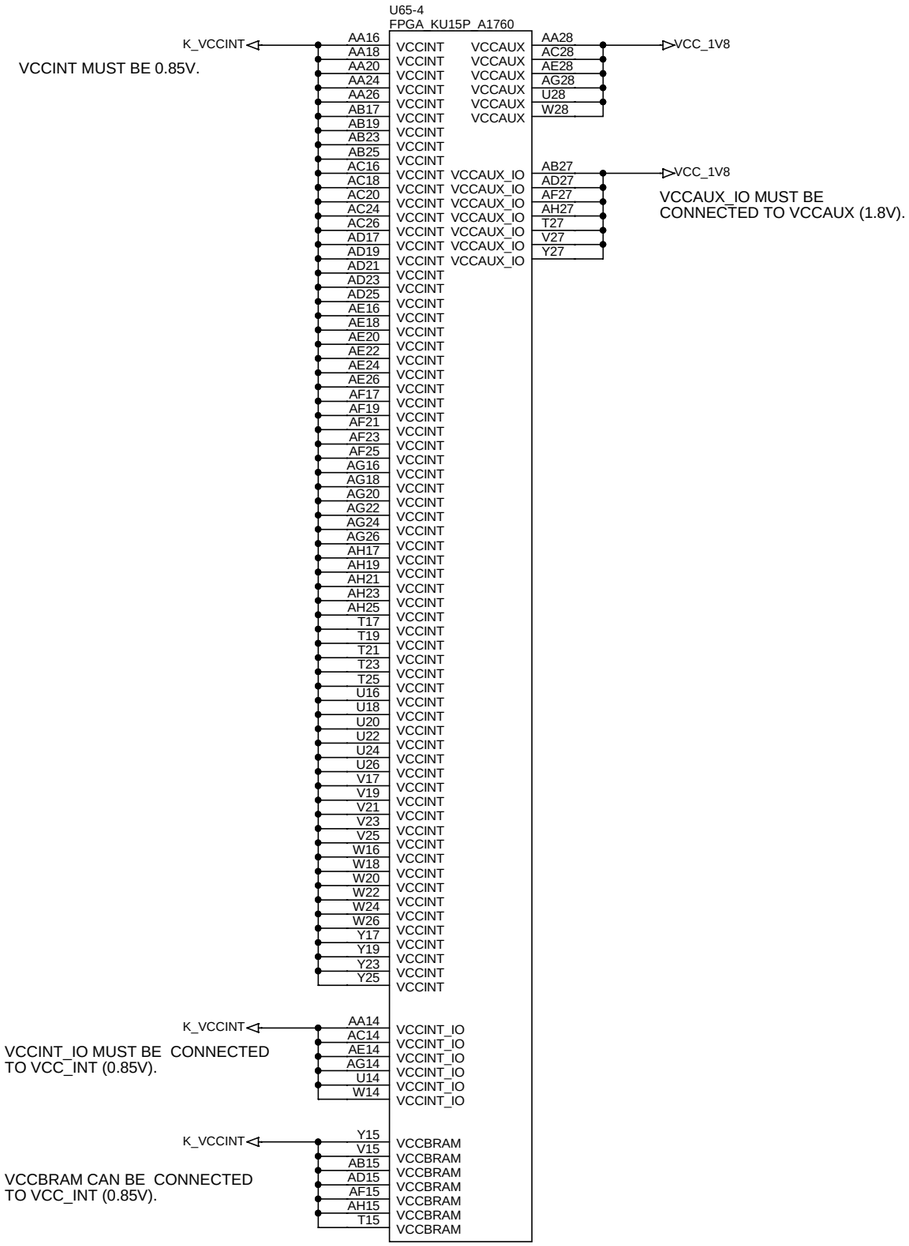



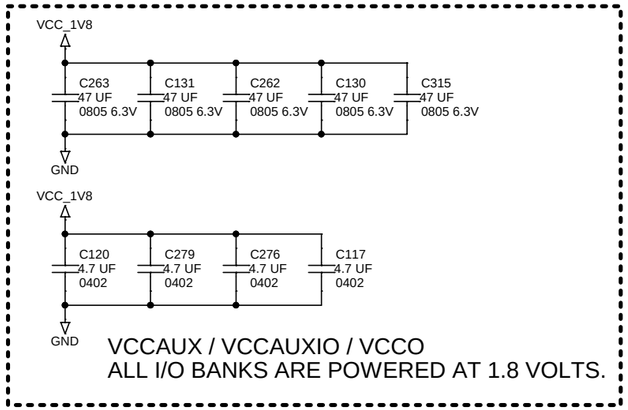



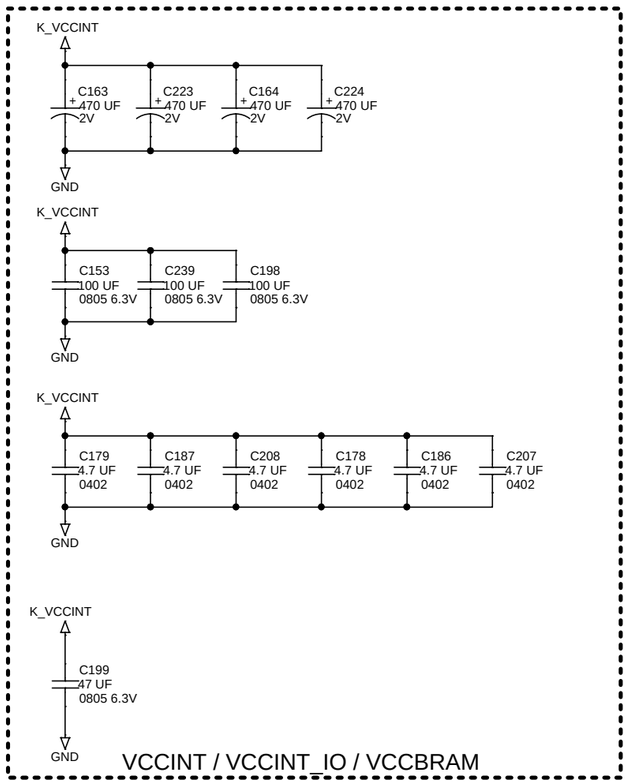




| | | | |
|---|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | | |
| Title: 5.01: KU15P FPGA GND | | | |
| Size | Document Number: 6089-103 | | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 31 of 74 | | |

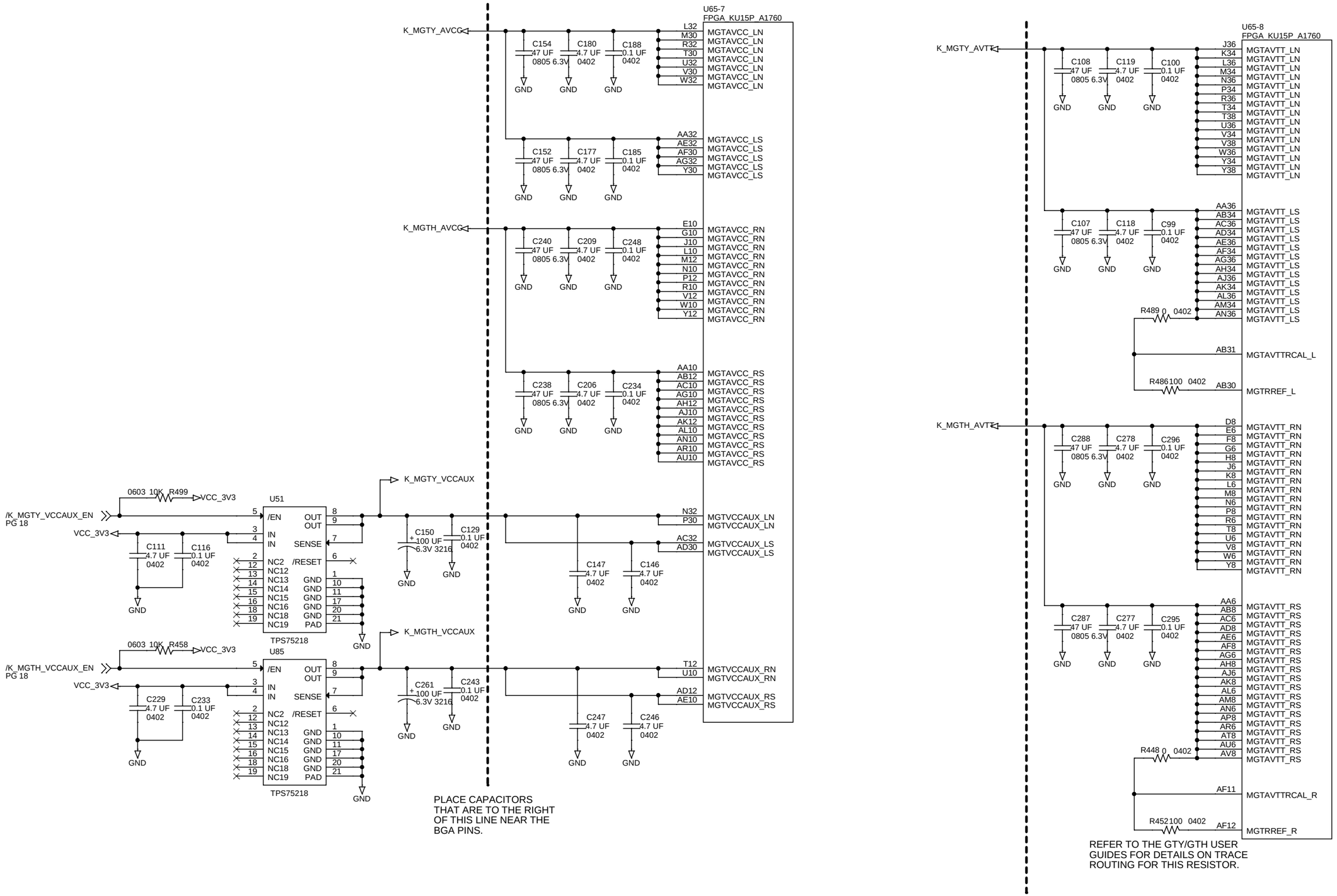



BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"xtp427-ultrascale-plus-schematic-review-checklist.xls"

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 5.02: KU15P FPGA INTERNAL POWER | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 32 of 74 | |




ON MIXED TRANSCEIVER DEVICES, REGIONS "LN" AND "LS" ARE GTY TRANSCEIVERS. REGIONS "RN" AND "RS" ARE GTH TRANSCEIVERS.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.03: KU15P GTH/GTY TRANSCEIVER POWER

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 33 of 74

# QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

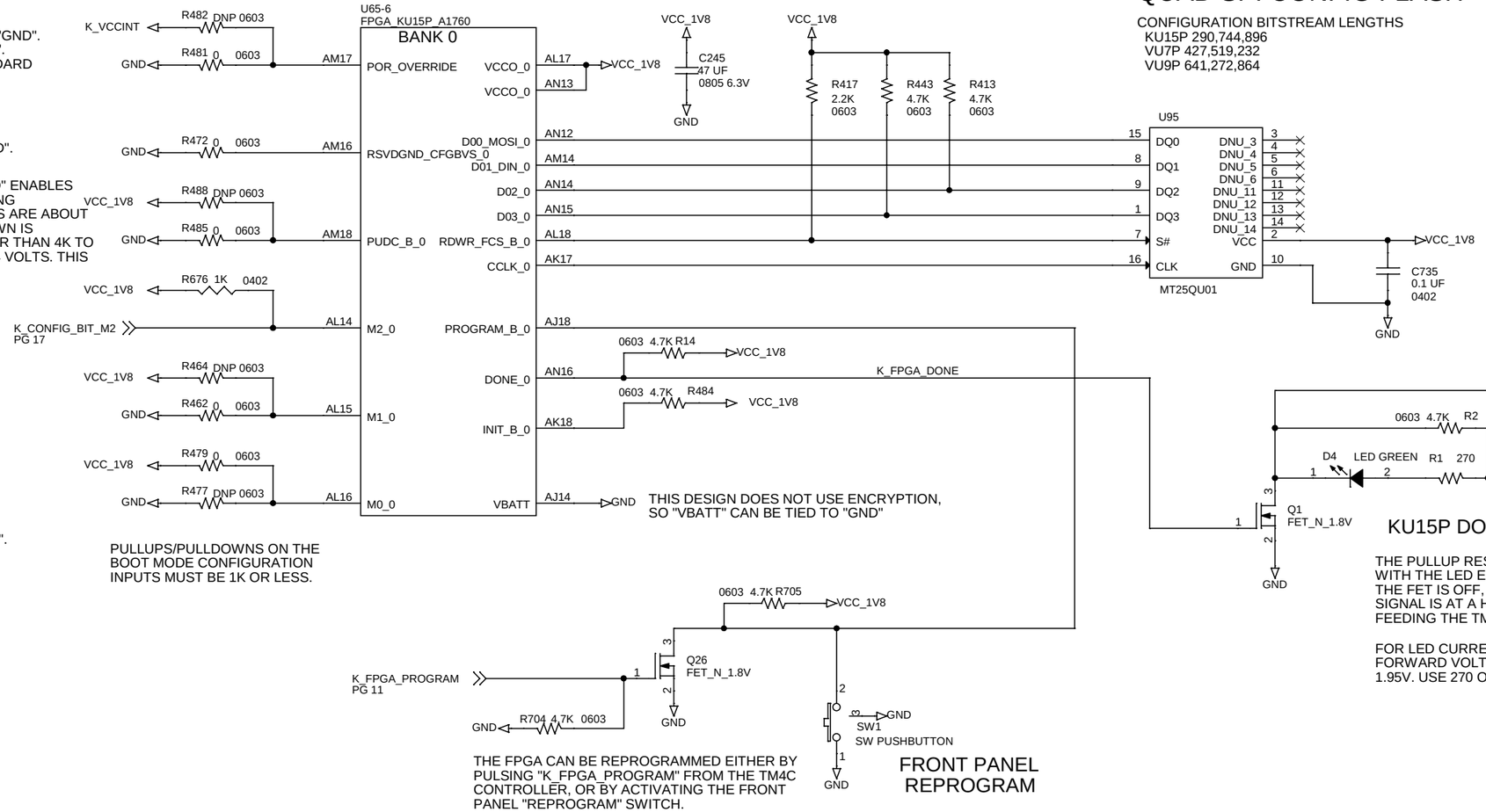
THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES
PULLUPS ON ALL I/O PINS DURING
CONFIGURATION. THE PULLUPS ARE ABOUT
15K AT 1.8 VOLTS. IF A PULLDOWN IS
REQUIRED, IT MUST BE SMALLER THAN 4K TO
DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS
PIN MUST NOT FLOAT.

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

PULLUPS/PULLDOWNS ON THE
BOOT MODE CONFIGURATION
INPUTS MUST BE 1K OR LESS.




## KU15P DONE LED

THE PULLUP RESISTOR IN PARALLEL
WITH THE LED ENSURES THAT, WHEN
THE FET IS OFF, THE "/K_FPGA_DONE"
SIGNAL IS AT A HIGH LEVEL FOR
FEEDING THE TM4C CONTROLLER.

FOR LED CURRENT OF 5 MA, THE
FORWARD VOLTAGE DROP IS
1.95V. USE 270 OHM RESISTOR.




THE FPGA CAN BE REPROGRAMMED EITHER BY
PULSING "K_FPGA_PROGRAM" FROM THE TM4C
CONTROLLER, OR BY ACTIVATING THE FRONT
PANEL "REPROGRAM" SWITCH.

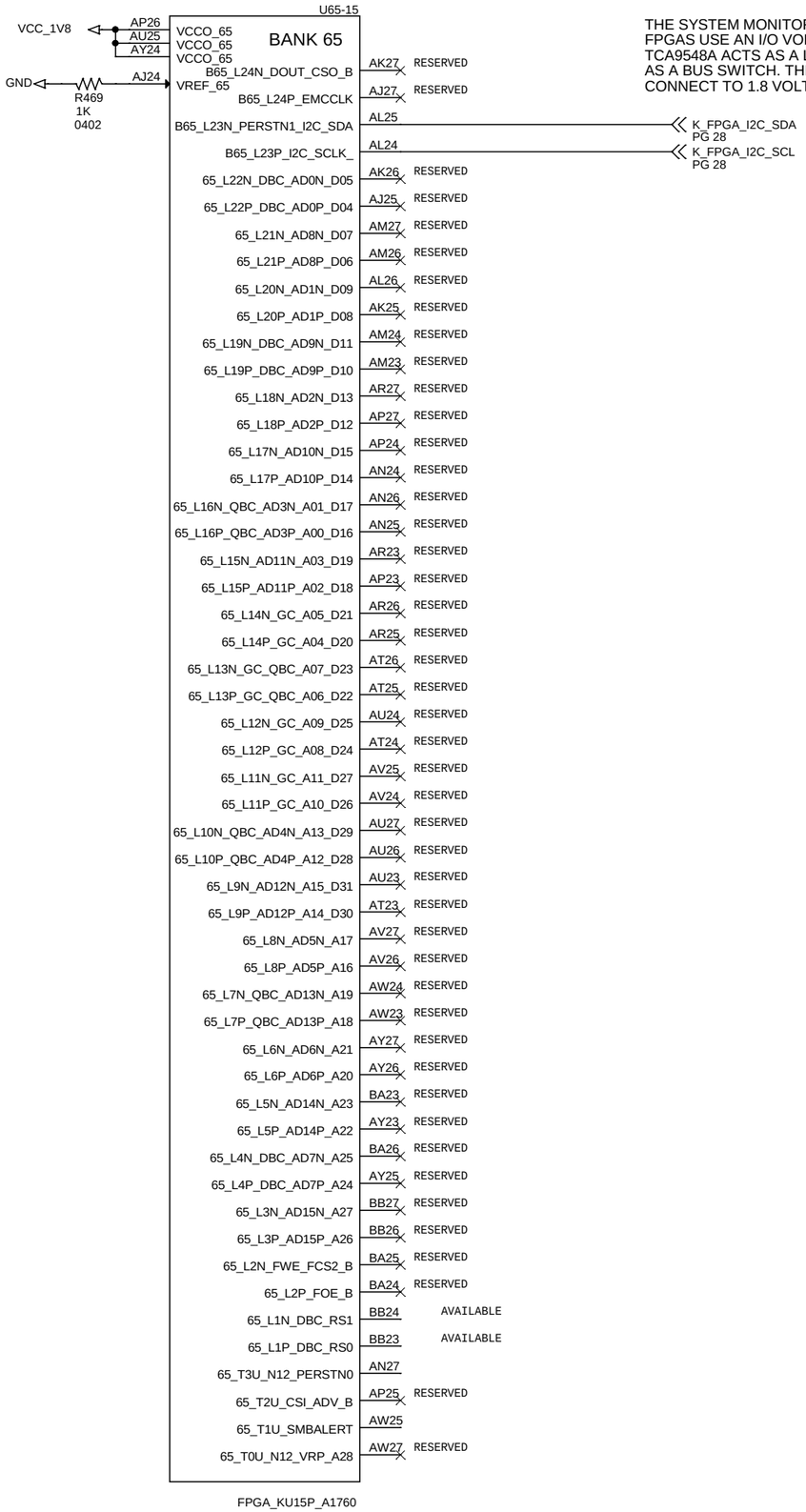
## FRONT PANEL REPROGRAM

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title
5.04: KU15P FPGA CONFIGURATION

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Wednesday, March 06, 2019 Sheet 34 of 74




THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

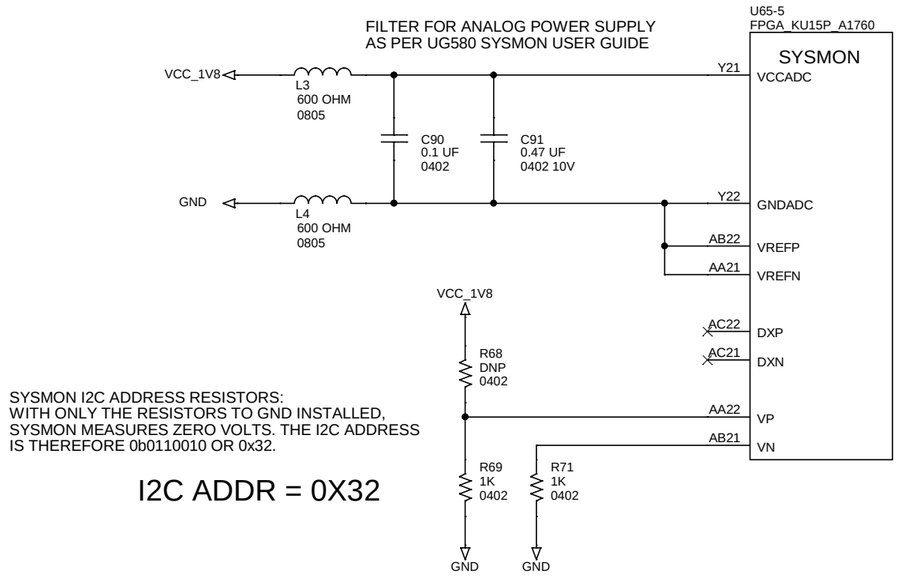
BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.05: KU15P BANK 65

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 35 of 74




SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

I2C ADDR = 0X32

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.06: KU15P SYSTEM MONITOR

Size | Document Number: 6089-103 | Rev: A

Date: Friday, March 08, 2019 | Sheet 36 of 74

THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "KV_SPARE6" SIGNAL IS CONNECTED TO CLOCK INPUT PINS ON THE KU15P.

U65-21

BANK 72

| | | | |
|---|---|---|---|
| nKV_SPARE0 PG 46 | nKV_SPARE0 | B22 | 72_L24N_T3U_N11 |
| pKV_SPARE0 PG 46 | pKV_SPARE0 | B23 | 72_L24P_T3U_N10 |
| nKV_SPARE1 PG 46 | nKV_SPARE1 | A23 | 72_L23N_T3U_N9 |
| pKV_SPARE1 PG 46 | pKV_SPARE1 | A24 | 72_L23P_T3U_N8 |
| | | A21 | 72_L22N_T3U_N7_DBC_AD0N |
| | | B21 | 72_L22P_T3U_N6_DBC_AD0P |
| nKV_SPARE2 PG 46 | nKV_SPARE2 | B24 | 72_L21N_T3L_N5_AD8N |
| pKV_SPARE2 PG 46 | pKV_SPARE2 | C24 | 72_L21P_T3L_N4_AD8P |
| nKV_SPARE3 PG 46 | nKV_SPARE3 | C21 | 72_L20N_T3L_N3_AD1N |
| pKV_SPARE3 PG 46 | pKV_SPARE3 | C22 | 72_L20P_T3L_N2_AD1P |
| nKV_SPARE4 PG 46 | nKV_SPARE4 | D23 | 72_L19N_T3L_N1_DBC_AD9N |
| pKV_SPARE4 PG 46 | pKV_SPARE4 | D24 | 72_L19P_T3L_N0_DBC_AD9P |
| nKV_SPARE5 PG 46 | nKV_SPARE5 | E21 | 72_L18N_T2U_N11_AD2N |
| pKV_SPARE5 PG 46 | pKV_SPARE5 | E22 | 72_L18P_T2U_N10_AD2P |
| nK_CDR_DATA PG 14 | | G24 | 72_L17N_T2U_N9_AD10N |
| pK_CDR_DATA PG 14 | | H24 | 72_L17P_T2U_N8_AD10P |
| nKV_SPARE7 PG 46 | nKV_SPARE7 | F20 | 72_L16N_T2U_N7_QBC_AD3N |
| pKV_SPARE7 PG 46 | pKV_SPARE7 | F21 | 72_L16P_T2U_N6_QBC_AD3P |
| nKV_SPARE8 PG 46 | nKV_SPARE8 | E23 | 72_L15N_T2L_N5_AD11N |
| pKV_SPARE8 PG 46 | pKV_SPARE8 | F24 | 72_L15P_T2L_N4_AD11P |
| ac_nK_UTIL_CLK_CHAN2 PG 15 | | G21 | 72_L14N_T2L_N3_GC |
| ac_pK_UTIL_CLK_CHAN2 PG 15 | | G22 | 72_L14P_T2L_N2_GC |
| nK_TTS_OUT PG 14 | | F23 | 72_L13N_T2L_N1_GC_QBC |
| pK_TTS_OUT PG 14 | | G23 | 72_L13P_T2L_N0_GC_QBC |
| nKV_SPARE6 PG 46 | nKV_SPARE6 | J22 | 72_L12N_T1U_N11_GC |
| pKV_SPARE6 PG 46 | pKV_SPARE6 | K22 | 72_L12P_T1U_N10_GC |
| ac_nK_TTC_CLK40 PG 14 | | J23 | 72_L11N_T1U_N9_GC |
| ac_pK_TTC_CLK40 PG 14 | | K23 | 72_L11P_T1U_N8_GC |
| nKV_SPARE9 PG 46 | nKV_SPARE9 | H20 | 72_L10N_T1U_N7_QBC_AD4N |
| pKV_SPARE9 PG 46 | pKV_SPARE9 | H21 | 72_L10P_T1U_N6_QBC_AD4P |
| nKV_SPARE10 PG 46 | nKV_SPARE10 | L23 | 72_L9N_T1L_N5_AD12N |
| pKV_SPARE10 PG 46 | pKV_SPARE10 | L24 | 72_L9P_T1L_N4_AD12P |
| nKV_SPARE11 PG 46 | nKV_SPARE11 | J20 | 72_L8N_T1L_N3_AD5N |
| pKV_SPARE11 PG 46 | pKV_SPARE11 | K20 | 72_L8P_T1L_N2_AD5P |
| nKV_SPARE12 PG 46 | nKV_SPARE12 | K21 | 72_L7N_T1L_N1_QBC_AD13N |
| pKV_SPARE12 PG 46 | pKV_SPARE12 | L21 | 72_L7P_T1L_N0_QBC_AD13P |
| | | M22 | 72_L6N_T0U_N11_AD6N |
| | | N22 | 72_L6P_T0U_N10_AD6P |
| | | P23 | 72_L5N_T0U_N9_AD14N |
| | | R23 | 72_L5P_T0U_N8_AD14P |
| | | N20 | 72_L4N_T0U_N7_DBC_AD7N |
| | | N21 | 72_L4P_T0U_N6_DBC_AD7P |
| | | P22 | 72_L3N_T0L_N5_AD15N |
| | | R22 | 72_L3P_T0L_N4_AD15P |
| | | L20 | 72_L2N_T0L_N3 |
| | | M21 | 72_L2P_T0L_N2 |
| | | P20 | 72_L1N_T0L_N1_DBC |
| | | R21 | 72_L1P_T0L_N0_DBC |
| KU15P_FROM_TM4C_0 PG 17 | | D22 | 72_T3U_N12 |
| KU15P_TO_TM4C_0 PG 17 | | H22 | 72_T2U_N12 |
| | | J24 | 72_T1U_N12 |
| | | M23 | 72_T0U_N12_VRP |

VCCO_72: E24, H23, L22 → VCC_1V8

VREF_72: R20 R470 1K 0402 → GND

GND: R465 240 0402

FPGA_KU15P_A1760

U65-17

BANK 67

| | | | |
|---|---|---|---|
| | | AJ30 | 67_L24N_T3U_N11 |
| | | AJ29 | 67_L24P_T3U_N10 |
| | | AM32 | 67_L23N_T3U_N9 |
| | | AM31 | 67_L23P_T3U_N8 |
| | | AK32 | 67_L22N_T3U_N7_DBC_AD0N |
| | | AK31 | 67_L22P_T3U_N6_DBC_AD0P |
| | | AL30 | 67_L21N_T3L_N5_AD8N |
| | | AL29 | 67_L21P_T3L_N4_AD8P |
| | | AL31 | 67_L20N_T3L_N3_AD1N |
| | | AK30 | 67_L20P_T3L_N2_AD1P |
| | | AM29 | 67_L19N_T3L_N1_DBC_AD9N |
| | | AL28 | 67_L19P_T3L_N0_DBC_AD9P |
| | | AR32 | 67_L18N_T2U_N11_AD2N |
| | | AP32 | 67_L18P_T2U_N10_AD2P |
| | | AN32 | 67_L17N_T2U_N9_AD10N |
| | | AN31 | 67_L17P_T2U_N8_AD10P |
| | | AR28 | 67_L16N_T2U_N7_QBC_AD3N |
| | | AP28 | 67_L16P_T2U_N6_QBC_AD3P |
| | | AN30 | 67_L15N_T2L_N5_AD11N |
| | | AN29 | 67_L15P_T2L_N4_AD11P |
| | | AR31 | 67_L14N_T2L_N3_GC |
| | | AR30 | 67_L14P_T2L_N2_GC |
| | | AP30 | 67_L13N_T2L_N1_GC_QBC |
| | | AP29 | 67_L13P_T2L_N0_GC_QBC |
| | | AT30 | 67_L12N_T1U_N11_GC |
| | | AT29 | 67_L12P_T1U_N10_GC |
| | | AU31 | 67_L11N_T1U_N9_GC |
| | | AT31 | 67_L11P_T1U_N8_GC |
| | | AV29 | 67_L10N_T1U_N7_QBC_AD4N |
| | | AU29 | 67_L10P_T1U_N6_QBC_AD4P |
| K_DIP_SW_1 PG 17 | | AV32 | 67_L9N_T1L_N5_AD12N |
| K_DIP_SW_2 PG 17 | | AU32 | 67_L9P_T1L_N4_AD12P |
| | | AU28 | 67_L8N_T1L_N3_AD5N |
| | | AT28 | 67_L8P_T1L_N2_AD5P |
| | | AV31 | 67_L7N_T1L_N1_QBC_AD13N |
| | | AV30 | 67_L7P_T1L_N0_QBC_AD13P |
| | | AY31 | 67_L6N_T0U_N11_AD6N |
| | | AY30 | 67_L6P_T0U_N10_AD6P |
| | | BB31 | 67_L5N_T0U_N9_AD14N |
| | | BA31 | 67_L5P_T0U_N8_AD14P |
| | | AW29 | 67_L4N_T0U_N7_DBC_AD7N |
| K_LED_RED PG 17 | | AW28 | 67_L4P_T0U_N6_DBC_AD7P |
| | | BA30 | 67_L3N_T0L_N5_AD15N |
| K_LED_BLUE PG 17 | | BA29 | 67_L3P_T0L_N4_AD15P |
| | | BA28 | 67_L2N_T0L_N3 |
| K_LED_GREEN PG 17 | | AY28 | 67_L2P_T0L_N2 |
| | | BB29 | 67_L1N_T0L_N1_DBC |
| | | BB28 | 67_L1P_T0L_N0_DBC |
| | | AK28 | 67_T3U_N12 |
| | | AM28 | 67_T2U_N12 |
| | | AW30 | 67_T1U_N12 |
| | | BB32 | 67_T0U_N12_VRP |

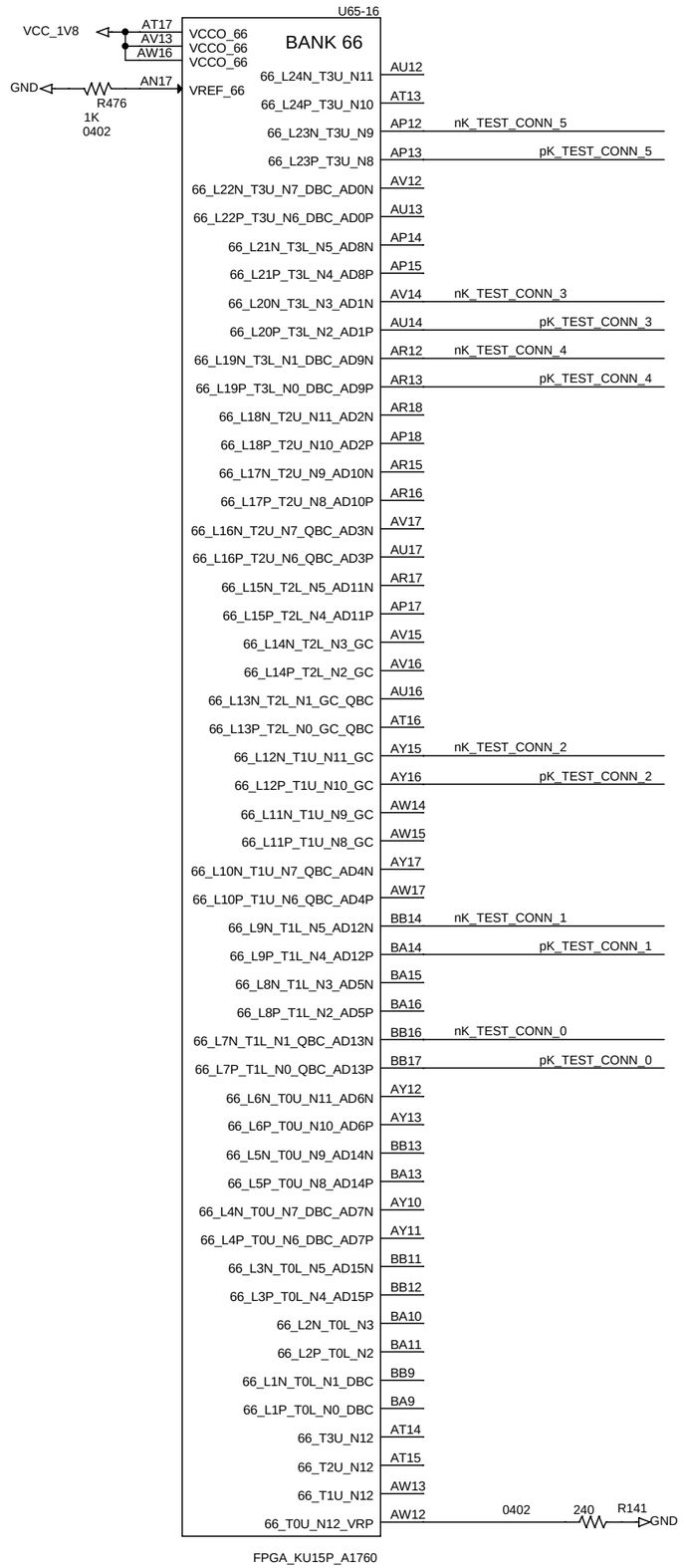
VCCO_67: AP31, AU30, AY29 → VCC_1V8

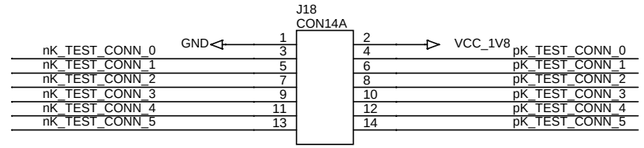
VREF_67: AJ28 R102 1K 0402 → GND

GND: R99 240 0402

FPGA_KU15P_A1760

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 5.07: KU15P UTILITY BANKS | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 37 of 74 | |




THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

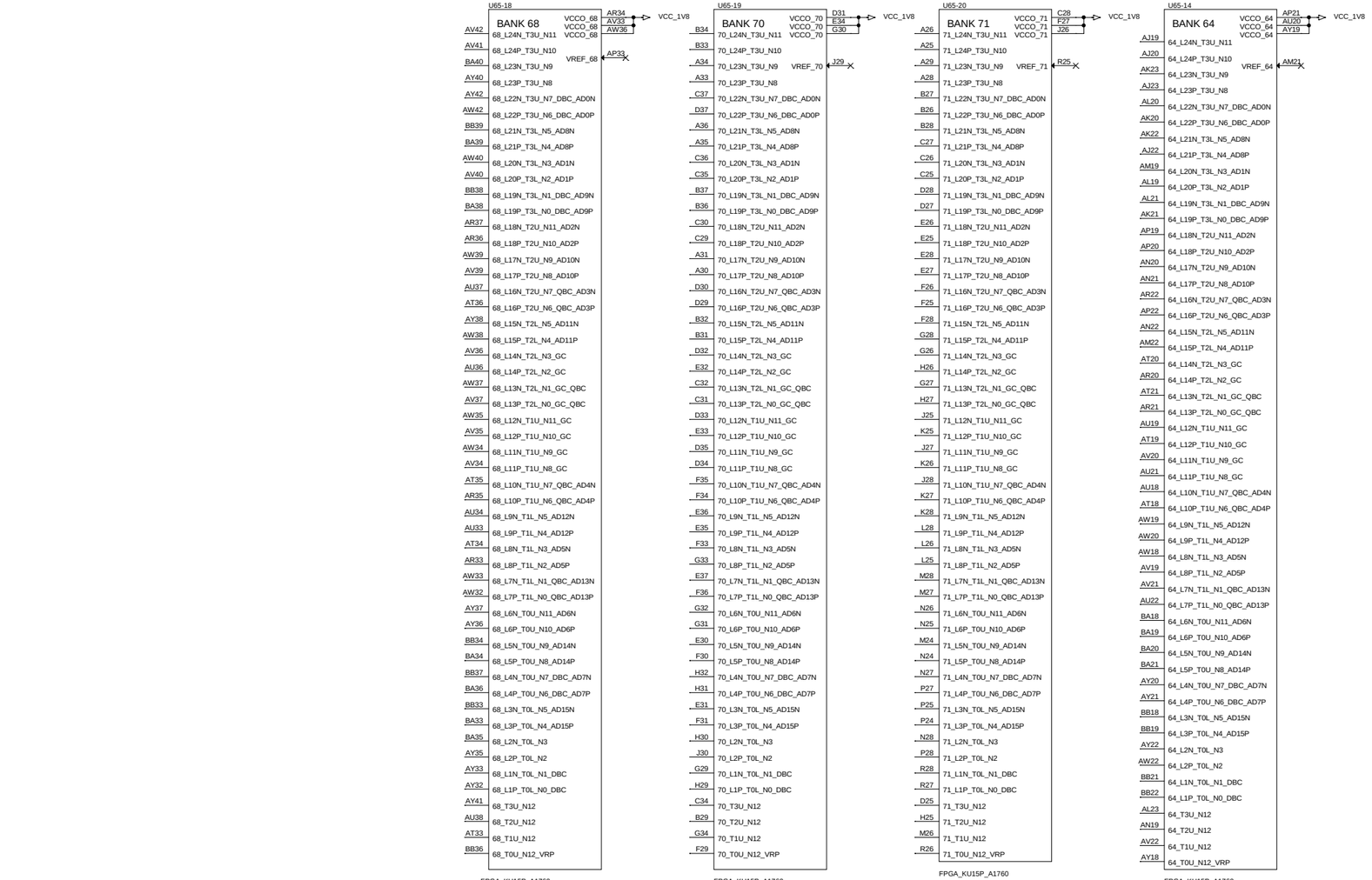
THE "K_TEST_CONN_2" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.08 KU15P TEST CONNECTOR

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 38 of 74




# KU15P UNUSED BLOCKS

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 5.99: KU15P UNUSED BLOCKS

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 39 of 74

U66-1
FPGA_VU7P_B2104

| | | | |
|---|---|---|---|
| A10 | GND | GND | AF28 |
| A12 | GND | GND | AF3 |
| A21 | GND | GND | AF35 |
| A3 | GND | GND | AF36 |
| A31 | GND | GND | AF4 |
| A41 | GND | GND | AF40 |
| A44 | GND | GND | AF42 |
| A6 | GND | GND | AF45 |
| AA1 | GND | GND | AF46 |
| AA10 | GND | GND | AF5 |
| AA13 | GND | GND | AF8 |
| AA15 | GND | GND | AG1 |
| AA17 | GND | GND | AG11 |
| AA19 | GND | GND | AG17 |
| AA2 | GND | GND | AG2 |
| AA21 | GND | GND | AG21 |
| AA23 | GND | GND | AG23 |
| AA25 | GND | GND | AG25 |
| AA27 | GND | GND | AG27 |
| AA29 | GND | GND | AG33 |
| AA31 | GND | GND | AG35 |
| AA35 | GND | GND | AG39 |
| AA38 | GND | GND | AG42 |
| AA42 | GND | GND | AG43 |
| AA43 | GND | GND | AG44 |
| AA44 | GND | GND | AG5 |
| AA5 | GND | GND | AG7 |
| AA6 | GND | GND | AH14 |
| AA7 | GND | GND | AH16 |
| AB12 | GND | GND | AH20 |
| AB14 | GND | GND | AH22 |
| AB16 | GND | GND | AH24 |
| AB18 | GND | GND | AH26 |
| AB20 | GND | GND | AH3 |
| AB22 | GND | GND | AH30 |
| AB24 | GND | GND | AH35 |
| AB26 | GND | GND | AH37 |
| AB28 | GND | GND | AH4 |
| AB3 | GND | GND | AH41 |
| AB30 | GND | GND | AH42 |
| AB35 | GND | GND | AH45 |
| AB37 | GND | GND | AH46 |
| AB4 | GND | GND | AH5 |
| AB40 | GND | GND | AH9 |
| AB42 | GND | GND | AJ1 |
| AB45 | GND | GND | AJ10 |
| AB46 | GND | GND | AJ13 |
| AB5 | GND | GND | AJ15 |
| AB8 | GND | GND | AJ17 |
| AC1 | GND | GND | AJ2 |
| AC10 | GND | GND | AJ21 |
| AC15 | GND | GND | AJ23 |
| AC17 | GND | GND | AJ25 |
| AC19 | GND | GND | AJ35 |
| AC2 | GND | GND | AJ38 |
| AC21 | GND | GND | AJ42 |
| AC23 | GND | GND | AJ43 |
| AC25 | GND | GND | AJ44 |
| AC27 | GND | GND | AJ5 |
| AC29 | GND | GND | AJ6 |
| AC35 | GND | GND | AK14 |
| AC39 | GND | GND | AK16 |
| AC42 | GND | GND | AK18 |
| AC43 | GND | GND | AK20 |
| AC44 | GND | GND | AK22 |
| AC5 | GND | GND | AK24 |
| AC7 | GND | GND | AK3 |
| AD14 | GND | GND | AK34 |
| AD16 | GND | GND | AK35 |
| AD18 | GND | GND | AK37 |
| AD20 | GND | GND | AK4 |
| AD22 | GND | GND | AK40 |
| AD24 | GND | GND | AK42 |
| AD26 | GND | GND | AK45 |
| AD28 | GND | GND | AK46 |
| AD3 | GND | GND | AK5 |
| AD32 | GND | GND | AK8 |
| AD35 | GND | GND | AL1 |
| AD37 | GND | GND | AL11 |
| AD4 | GND | GND | AL2 |
| AD41 | GND | GND | AL31 |
| AD42 | GND | GND | AL35 |
| AD45 | GND | GND | AL39 |
| AD46 | GND | GND | AL42 |
| AD5 | GND | GND | AL43 |
| AD9 | GND | GND | AL44 |
| AE1 | GND | GND | AL5 |
| AE10 | GND | GND | AL7 |
| AE17 | GND | GND | AM18 |
| AE19 | GND | GND | AM28 |
| AE2 | GND | GND | AM3 |
| AE21 | GND | GND | AM35 |
| AE23 | GND | GND | AM37 |
| AE25 | GND | GND | AM4 |
| AE27 | GND | GND | AM41 |
| AE29 | GND | GND | AM42 |
| AE35 | GND | GND | AM45 |
| AE38 | GND | GND | AM46 |
| AE42 | GND | GND | AM5 |
| AE43 | GND | GND | AM9 |
| AE44 | GND | GND | AN1 |
| AE5 | GND | GND | AN10 |
| AE6 | GND | GND | AN12 |
| AF12 | GND | GND | AN15 |
| AF14 | GND | GND | AN2 |
| AF16 | GND | GND | AN25 |
| AF20 | GND | GND | AN35 |
| AF22 | GND | GND | AN38 |
| AF24 | GND | GND | AN42 |
| AF26 | GND | GND | AN43 |

GND GND

U66-2
FPGA_VU7P_B2104

| | | | |
|---|---|---|---|
| AN44 | GND | GND | B44 |
| AN5 | GND | GND | B45 |
| AN6 | GND | GND | B5 |
| AP12 | GND | GND | B6 |
| AP22 | GND | GND | B7 |
| AP3 | GND | GND | B8 |
| AP32 | GND | GND | BA11 |
| AP35 | GND | GND | BA21 |
| AP36 | GND | GND | BA3 |
| AP4 | GND | GND | BA31 |
| AP40 | GND | GND | BA37 |
| AP42 | GND | GND | BA38 |
| AP45 | GND | GND | BA39 |
| AP46 | GND | GND | BA44 |
| AP5 | GND | GND | BA6 |
| AP8 | GND | GND | BB1 |
| AR1 | GND | GND | BB18 |
| AR11 | GND | GND | BB2 |
| AR12 | GND | GND | BB28 |
| AR19 | GND | GND | BB3 |
| AR2 | GND | GND | BB39 |
| AR29 | GND | GND | BB40 |
| AR35 | GND | GND | BB41 |
| AR39 | GND | GND | BB44 |
| AR42 | GND | GND | BB45 |
| AR43 | GND | GND | BB46 |
| AR44 | GND | GND | BB6 |
| AR5 | GND | GND | BB8 |
| AR7 | GND | GND | BC15 |
| AT12 | GND | GND | BC25 |
| AT16 | GND | GND | BC3 |
| AT26 | GND | GND | BC35 |
| AT3 | GND | GND | BC4 |
| AT35 | GND | GND | BC41 |
| AT37 | GND | GND | BC42 |
| AT4 | GND | GND | BC44 |
| AT41 | GND | GND | BC6 |
| AT42 | GND | GND | BD1 |
| AT45 | GND | GND | BD12 |
| AT46 | GND | GND | BD22 |
| AT5 | GND | GND | BD3 |
| AT9 | GND | GND | BD32 |
| AU1 | GND | GND | BD41 |
| AU10 | GND | GND | BD44 |
| AU12 | GND | GND | BD46 |
| AU2 | GND | GND | BD6 |
| AU23 | GND | GND | BE19 |
| AU33 | GND | GND | BE2 |
| AU35 | GND | GND | BE29 |
| AU38 | GND | GND | BE3 |
| AU42 | GND | GND | BE39 |
| AU43 | GND | GND | BE41 |
| AU44 | GND | GND | BE45 |
| AU5 | GND | GND | BE5 |
| AU6 | GND | GND | BE6 |
| AV12 | GND | GND | BE9 |
| AV20 | GND | GND | BF16 |
| AV3 | GND | GND | BF26 |
| AV30 | GND | GND | BF3 |
| AV35 | GND | GND | BF36 |
| AV36 | GND | GND | BF41 |
| AV37 | GND | GND | BF44 |
| AV4 | GND | GND | BF6 |
| AV40 | GND | GND | C1 |
| AV42 | GND | GND | C11 |
| AV45 | GND | GND | C12 |
| AV46 | GND | GND | C15 |
| AV5 | GND | GND | C2 |
| AV8 | GND | GND | C25 |
| AW1 | GND | GND | C35 |
| AW10 | GND | GND | C41 |
| AW11 | GND | GND | C44 |
| AW12 | GND | GND | C46 |
| AW17 | GND | GND | C5 |
| AW2 | GND | GND | D12 |
| AW27 | GND | GND | D22 |
| AW37 | GND | GND | D3 |
| AW39 | GND | GND | D32 |
| AW42 | GND | GND | D4 |
| AW43 | GND | GND | D41 |
| AW44 | GND | GND | D42 |
| AW5 | GND | GND | D44 |
| AW6 | GND | GND | D5 |
| AY1 | GND | GND | D9 |
| AY10 | GND | GND | E1 |
| AY14 | GND | GND | E10 |
| AY2 | GND | GND | E12 |
| AY24 | GND | GND | E19 |
| AY3 | GND | GND | E2 |
| AY34 | GND | GND | E29 |
| AY37 | GND | GND | E41 |
| AY4 | GND | GND | E44 |
| AY41 | GND | GND | E45 |
| AY42 | GND | GND | E46 |
| AY43 | GND | GND | E5 |
| AY44 | GND | GND | E6 |
| AY45 | GND | GND | F12 |
| AY46 | GND | GND | F16 |
| AY5 | GND | GND | F26 |
| AY6 | GND | GND | F3 |
| AY7 | GND | GND | F36 |
| AY8 | GND | GND | F39 |
| AY9 | GND | GND | F4 |
| B12 | GND | GND | F40 |
| B18 | GND | GND | F41 |
| B2 | GND | GND | F44 |
| B28 | GND | GND | F5 |
| B38 | GND | GND | F8 |
| B4 | GND | GND | G1 |
| B41 | GND | GND | G11 |

GND GND

U66-3
FPGA_VU7P_B2104

| | | | |
|---|---|---|---|
| G12 | GND | GND | R35 |
| G13 | GND | GND | R39 |
| G2 | GND | GND | R42 |
| G23 | GND | GND | R43 |
| G33 | GND | GND | R44 |
| G39 | GND | GND | R5 |
| G42 | GND | GND | R7 |
| G43 | GND | GND | T12 |
| G44 | GND | GND | T14 |
| G45 | GND | GND | T16 |
| G46 | GND | GND | T18 |
| G5 | GND | GND | T20 |
| G7 | GND | GND | T22 |
| H12 | GND | GND | T24 |
| H20 | GND | GND | T3 |
| H3 | GND | GND | T35 |
| H30 | GND | GND | T37 |
| H39 | GND | GND | T4 |
| H4 | GND | GND | T41 |
| H41 | GND | GND | T42 |
| H42 | GND | GND | T45 |
| H45 | GND | GND | T46 |
| H46 | GND | GND | T5 |
| H5 | GND | GND | T9 |
| H9 | GND | GND | U1 |
| J1 | GND | GND | U10 |
| J10 | GND | GND | U13 |
| J12 | GND | GND | U15 |
| J17 | GND | GND | U17 |
| J2 | GND | GND | U19 |
| J27 | GND | GND | U2 |
| J37 | GND | GND | U21 |
| J38 | GND | GND | U23 |
| J39 | GND | GND | U25 |
| J42 | GND | GND | U27 |
| J43 | GND | GND | U33 |
| J44 | GND | GND | U35 |
| J5 | GND | GND | U38 |
| J6 | GND | GND | U42 |
| K12 | GND | GND | U43 |
| K14 | GND | GND | U44 |
| K24 | GND | GND | U5 |
| K3 | GND | GND | U6 |
| K35 | GND | GND | V14 |
| K36 | GND | GND | V16 |
| K37 | GND | GND | V18 |
| K4 | GND | GND | V20 |
| K40 | GND | GND | V22 |
| K42 | GND | GND | V24 |
| K45 | GND | GND | V26 |
| K46 | GND | GND | V28 |
| K5 | GND | GND | V3 |
| K8 | GND | GND | V30 |
| L1 | GND | GND | V35 |
| L11 | GND | GND | V36 |
| L12 | GND | GND | V4 |
| L2 | GND | GND | V40 |
| L21 | GND | GND | V42 |
| L31 | GND | GND | V45 |
| L35 | GND | GND | V46 |
| L39 | GND | GND | V5 |
| L42 | GND | GND | V8 |
| L43 | GND | GND | W1 |
| L44 | GND | GND | W11 |
| L5 | GND | GND | W13 |
| L7 | GND | GND | W15 |
| M12 | GND | GND | W17 |
| M18 | GND | GND | W19 |
| M28 | GND | GND | W2 |
| M3 | GND | GND | W21 |
| M35 | GND | GND | W23 |
| M37 | GND | GND | W25 |
| M4 | GND | GND | W27 |
| M41 | GND | GND | W29 |
| M42 | GND | GND | W35 |
| M45 | GND | GND | W39 |
| M46 | GND | GND | W42 |
| M5 | GND | GND | W43 |
| M9 | GND | GND | W44 |
| N1 | GND | GND | W5 |
| N10 | GND | GND | W7 |
| N12 | GND | GND | Y14 |
| N15 | GND | GND | Y16 |
| N2 | GND | GND | Y18 |
| N25 | GND | GND | Y20 |
| N35 | GND | GND | Y22 |
| N38 | GND | GND | Y24 |
| N42 | GND | GND | Y26 |
| N43 | GND | GND | Y28 |
| N44 | GND | GND | Y3 |
| N5 | GND | GND | Y34 |
| N6 | GND | GND | Y35 |
| P12 | GND | GND | Y37 |
| P22 | GND | GND | Y4 |
| P3 | GND | GND | Y41 |
| P32 | GND | GND | Y42 |
| P35 | GND | GND | Y45 |
| P36 | GND | GND | Y46 |
| P4 | GND | GND | Y5 |
| P40 | GND | GND | Y9 |
| P42 | GND | | |
| P45 | GND | | |
| P46 | GND | | |
| P5 | GND | | |
| P8 | GND | | |
| R1 | GND | | |
| R10 | GND | | |
| R19 | GND | | |
| R2 | GND | | |
| R29 | GND | | |

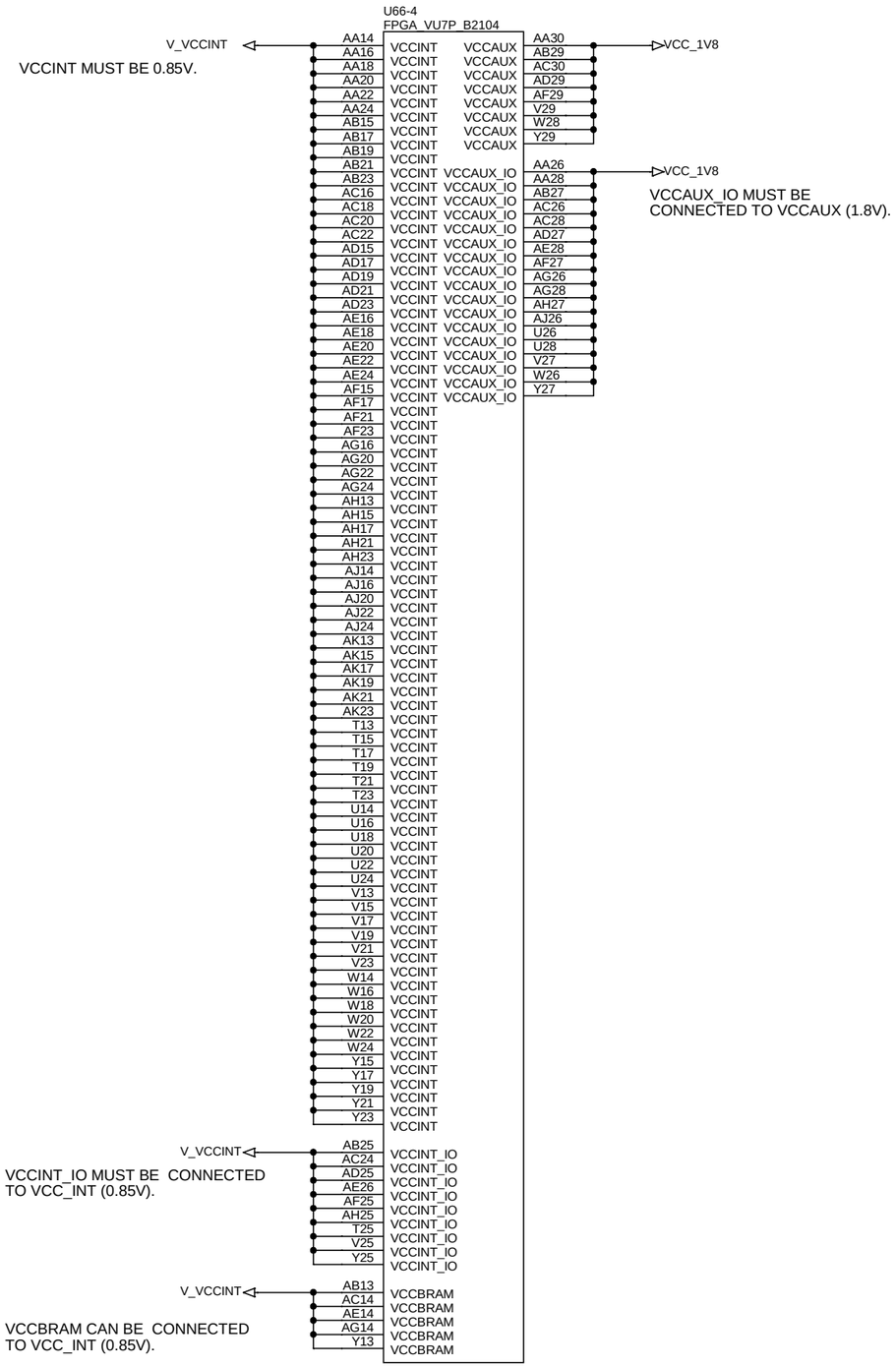
GND GND

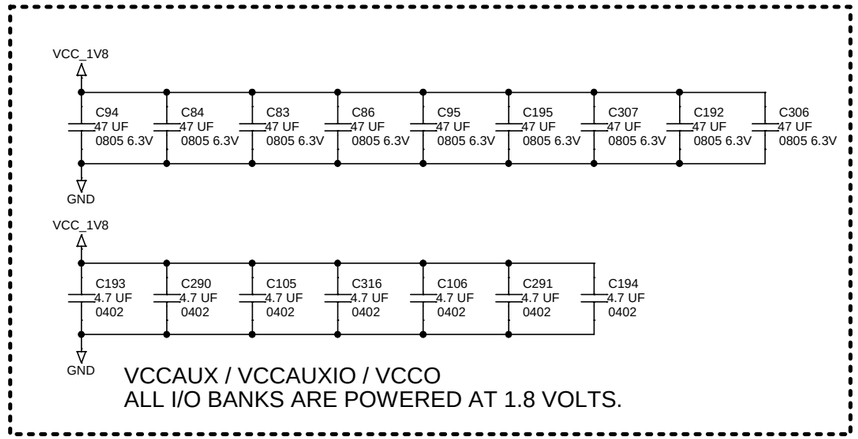
ATCA FPGA BOARD, KU15P AND VU7P, MK1

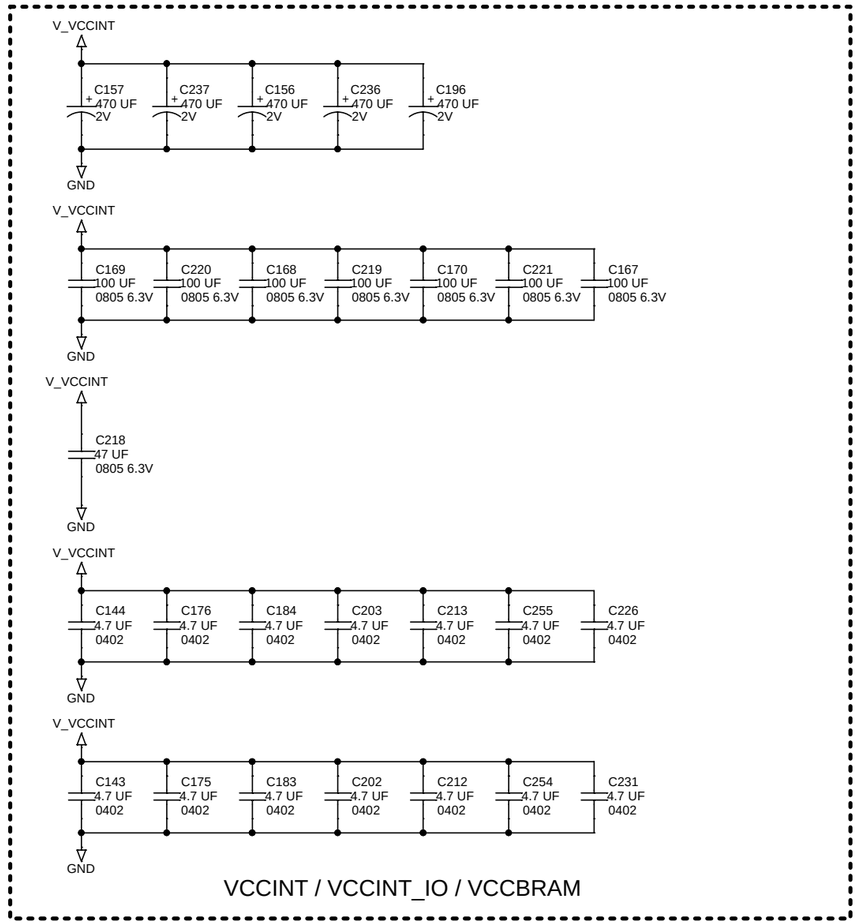
Title
6.01: VU7P FPGA GND

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 40 of 74




BYPASS CAPACITOR VALUES AND QUANTITIES FROM
"xtp427-ultrascale-plus-schematic-review-checklist.xls"

QUANTITIES BASE ON POSSIBLE UPGRADE TO VU9P

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 6.02: VU7P FPGA INTERNAL POWER | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 41 of 74 | |

U66-7
FPGA_VU7P_B2104

V_MGTY1_AVCC
C139 47 UF 0805 6.3V
C145 4.7 UF 0402
C136 0.1 UF 0402
AD36 MGTAVCC_LN
AF37 MGTAVCC_LN
L38 MGTAVCC_LN
M36 MGTAVCC_LN
N39 MGTAVCC_LN
P37 MGTAVCC_LN
R38 MGTAVCC_LN
T36 MGTAVCC_LN
U39 MGTAVCC_LN
V37 MGTAVCC_LN

C138 47 UF 0805 6.3V
C142 4.7 UF 0402
C133 0.1 UF 0402
AG38 MGTAVCC_LS
AL38 MGTAVCC_LS
AM36 MGTAVCC_LS
AP37 MGTAVCC_LS
AR38 MGTAVCC_LS
AT36 MGTAVCC_LS
AW38 MGTAVCC_LS
AY40 MGTAVCC_LS

V_MGTY2_AVCC
C259 47 UF 0805 6.3V
C256 4.7 UF 0402
C268 0.1 UF 0402
A11 MGTAVCC_RN
A7 MGTAVCC_RN
B9 MGTAVCC_RN
C10 MGTAVCC_RN
E11 MGTAVCC_RN
G10 MGTAVCC_RN
J11 MGTAVCC_RN
L10 MGTAVCC_RN
N11 MGTAVCC_RN
W10 MGTAVCC_RN

C258 47 UF 0805 6.3V
C253 4.7 UF 0402
C265 0.1 UF 0402
AA11 MGTAVCC_RS
AG10 MGTAVCC_RS
AJ11 MGTAVCC_RS
AL10 MGTAVCC_RS
AN11 MGTAVCC_RS
AP9 MGTAVCC_RS
AR10 MGTAVCC_RS
AU11 MGTAVCC_RS
AV9 MGTAVCC_RS
AW7 MGTAVCC_RS

0603 10K R495
VCC_3V3
/V_MGTY1_VCCAUX_EN
PG 18
U54
/EN
IN
IN
NC2
NC12
NC13
NC14
NC15
NC16
NC18
NC19
OUT
OUT
SENSE
/RESET
GND
PAD
TPS75218
V_MGTY1_VCCAUX
C776 4.7 UF 0402
C777 0.1 UF 0402
C114 100 UF 6.3V 3216
C126 0.1 UF 0402
AB36 MGTVCCAUX_LN
Y36 MGTVCCAUX_LN
AH36 MGTVCCAUX_LS
AK36 MGTVCCAUX_LS
C135 4.7 UF 0402
C134 4.7 UF 0402

0603 10K R408
VCC_3V3
/V_MGTY2_VCCAUX_EN
PG 18
U99
TPS75218
V_MGTY2_VCCAUX
C727 4.7 UF 0402
C728 0.1 UF 0402
C299 100 UF 6.3V 3216
C302 0.1 UF 0402
R11 MGTVCCAUX_RN
U11 MGTVCCAUX_RN
AC11 MGTVCCAUX_RS
AE11 MGTVCCAUX_RS
C267 4.7 UF 0402
C266 4.7 UF 0402

PLACE CAPACITORS
THAT ARE TO THE RIGHT
OF THIS LINE NEAR THE
BGA PINS.

U66-8
FPGA_VU7P_B2104

V_MGTY1_AVTT
C123 47 UF 0805 6.3V
C125 4.7 UF 0402
C113 0.1 UF 0402
AA39 MGTAVTT_LN
AB41 MGTAVTT_LN
AC38 MGTAVTT_LN
AD40 MGTAVTT_LN
AE39 MGTAVTT_LN
AF41 MGTAVTT_LN
C45 MGTAVTT_LN
D43 MGTAVTT_LN
F42 MGTAVTT_LN
F43 MGTAVTT_LN
H40 MGTAVTT_LN
K41 MGTAVTT_LN
M40 MGTAVTT_LN
P41 MGTAVTT_LN
T40 MGTAVTT_LN
V41 MGTAVTT_LN
W38 MGTAVTT_LN
Y40 MGTAVTT_LN
R91 0 0402
B42 MGTAVTTRCAL_LN
R88 100 0402
B43 MGTRREF_LN

C122 47 UF 0805 6.3V
C112 4.7 UF 0402
C124 0.1 UF 0402
AH40 MGTAVTT_LS
AJ39 MGTAVTT_LS
AK41 MGTAVTT_LS
AM40 MGTAVTT_LS
AN39 MGTAVTT_LS
AP41 MGTAVTT_LS
AT40 MGTAVTT_LS
AU39 MGTAVTT_LS
AV41 MGTAVTT_LS
BA42 MGTAVTT_LS
BA43 MGTAVTT_LS
BC43 MGTAVTT_LS
BD45 MGTAVTT_LS
BE44 MGTAVTT_LS
R90 0 0402
BE42 MGTAVTTRCAL_LS
R87 100 0402
BE43 MGTRREF_LS

V_MGTY2_AVTT
C280 47 UF 0805 6.3V
C275 4.7 UF 0402
C285 0.1 UF 0402
B3 MGTAVTT_RN
D8 MGTAVTT_RN
E7 MGTAVTT_RN
F9 MGTAVTT_RN
G6 MGTAVTT_RN
H8 MGTAVTT_RN
J7 MGTAVTT_RN
K9 MGTAVTT_RN
L6 MGTAVTT_RN
M8 MGTAVTT_RN
N7 MGTAVTT_RN
P9 MGTAVTT_RN
R6 MGTAVTT_RN
T8 MGTAVTT_RN
U7 MGTAVTT_RN
V9 MGTAVTT_RN
W6 MGTAVTT_RN
Y8 MGTAVTT_RN
R146 0 0402
C7 MGTAVTTRCAL_RN
R151 100 0402
C6 MGTRREF_RN

C282 47 UF 0805 6.3V
C274 4.7 UF 0402
C284 0.1 UF 0402
AB9 MGTAVTT_RS
AC6 MGTAVTT_RS
AD8 MGTAVTT_RS
AE7 MGTAVTT_RS
AF9 MGTAVTT_RS
AG6 MGTAVTT_RS
AH8 MGTAVTT_RS
AJ7 MGTAVTT_RS
AK9 MGTAVTT_RS
AL6 MGTAVTT_RS
AM8 MGTAVTT_RS
AN7 MGTAVTT_RS
AR6 MGTAVTT_RS
AT8 MGTAVTT_RS
AU7 MGTAVTT_RS
BC5 MGTAVTT_RS
BD2 MGTAVTT_RS
BE4 MGTAVTT_RS
R145 0 0402
BA5 MGTAVTTRCAL_RS
R150 100 0402
BA4 MGTRREF_RS

REFER TO THE GTY/GTH USER
GUIDES FOR DETAILS ON TRACE
ROUTING FOR THIS RESISTOR.

PLACE CAPACITORS AND RESISTORS
THAT ARE TO THE RIGHT OF THIS LINE
NEAR THE BGA PINS.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 6.03: VU7P GTY TRANSCEIVER POWER | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 42 of 74 | |

MUST BE TIED TO "VCCINT" OR "GND".
DO NOT CONNECT TO "VCCO_0".
CONNECT TO "GND" FOR STANDARD
POR DELAY.

THIS PIN MUST BE TIED TO "GND".

CONNECTING THIS PIN TO "GND" ENABLES PULLUPS ON ALL I/O PINS DURING CONFIGURATION. THE PULLUPS ARE ABOUT 15K AT 1.8 VOLTS. IF A PULLDOWN IS REQUIRED, IT MUST BE SMALLER THAN 4K TO DROP THE VOLTAGE BELOW 0.4 VOLTS. THIS PIN MUST NOT FLOAT.

V_CONFIG_BIT_M2
PG 17

M[2:0] MODE
000 Master serial
001 Master SPI
010 Master BPI
100 Master SelectMAP
101 JTAG only
110 Slave SelectMAP
111 Slave Serial

THIS SWITCH ON BIT "M2"
ALLOW A CHOICE OF EITHER
"MASTER SPI" OR "JTAG ONLY".

U66-6
FPGA_VU7P_B2104
BANK 0

V_VCCINT, GND, R478 DNP 0603, R480 0 0603 → AD12 POR_OVERRIDE
GND, R449 0 0603 → W12 RSVDGND
VCC_1V8, R463 DNP 0603; GND, R474 0 0603 → AA12 PUDC_B_0
VCC_1V8, R682 1K 0402 → R12 M2_0
VCC_1V8, R459 DNP 0603; GND, R461 0 0603 → U12 M1_0
VCC_1V8, R450 0 0603; GND, R451 DNP 0603 → V12 M0_0

VCCO_0: AD13, AF13 → VCC_1V8; C292 47 UF 0805 6.3V → GND
VCCO_0
D00_MOSI_0 AK12
D01_DIN_0 AJ12
D02_0 AL12
D03_0 AH12
RDWR_FCS_B_0 AG12
CCLK_0 AG13
PROGRAM_B_0 AE12
DONE_0 AC12 → 0603 4.7K R21 → VCC_1V8; V_FPGA_DONE
INIT_B_0 Y12 → 0603 4.7K R453 → VCC_1V8
VBATT AM12 → GND

THIS DESIGN DOES NOT USE ENCRYPTION, SO "VBATT" CAN BE TIED TO "GND"

PULLUPS/PULLDOWNS ON THE BOOT MODE CONFIGURATION INPUTS MUST BE 1K OR LESS.

VCC_1V8: R406 2.2K 0603, R409 4.7K 0603, R407 4.7K 0603

# QUAD SPI CONFIG FLASH

CONFIGURATION BITSTREAM LENGTHS
KU15P 290,744,896
VU7P 427,519,232
VU9P 641,272,864

U98 MT25QU01
15 DQ0, 8 DQ1, 9 DQ2, 1 DQ3, 7 S#, 16 CLK
DNU_3 3, DNU_4 4, DNU_5 5, DNU_6 6, DNU_11 11, DNU_12 12, DNU_13 13, DNU_14 14
VCC 2 → VCC_1V8; C729 0.1 UF 0402 → GND
GND 10 → GND

0603 4.7K R713 → VCC_1V8
V_FPGA_PROGRAM PG 11 → Q27 FET_N_1.8V (1, 2, 3); GND
R712 4.7K 0603: GND → V_FPGA_PROGRAM
SW3 SW PUSHBUTTON: 3 → GND; 1 → GND

THE FPGA CAN BE REPROGRAMMED EITHER BY PULSING "V_FPGA_PROGRAM" FROM THE TM4C CONTROLLER, OR BY ACTIVATING THE FRONT PANEL "REPROGRAM" SWITCH.

## FRONT PANEL REPROGRAM

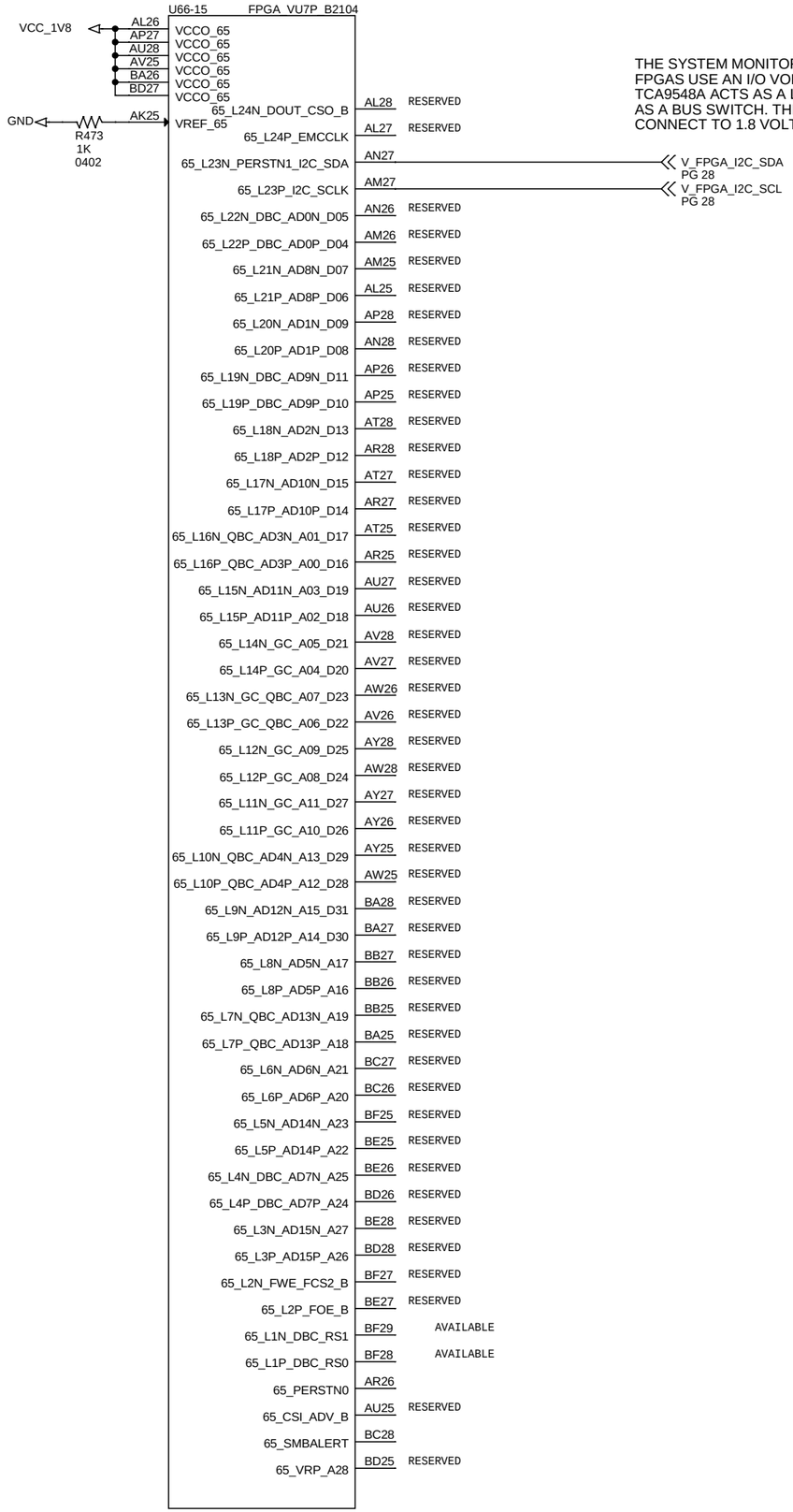
/V_FPGA_DONE
PG 11
0603 4.7K R7
D7 LED GREEN R6 270 → VCC_3V3
V_FPGA_DONE → Q5 FET_N_1.8V (1, 2, 3); GND

## VU7P DONE LED

THE PULLUP RESISTOR IN PARALLEL WITH THE LED ENSURES THAT, WHEN THE FET IS OFF, THE "/V_FPGA_DONE" SIGNAL IS AT A HIGH LEVEL FOR FEEDING THE TM4C CONTROLLER.

FOR LED CURRENT OF 5 MA, THE FORWARD VOLTAGE DROP IS 1.95V. USE 270 OHM RESISTOR.

ATCA FPGA BOARD, KU15P AND VU7P, MK1
Title: 6.04: VU7P FPGA CONFIGURATION
Size | Document Number: 6089-103 | Rev: A
Date: Wednesday, March 06, 2019 | Sheet 43 of 74

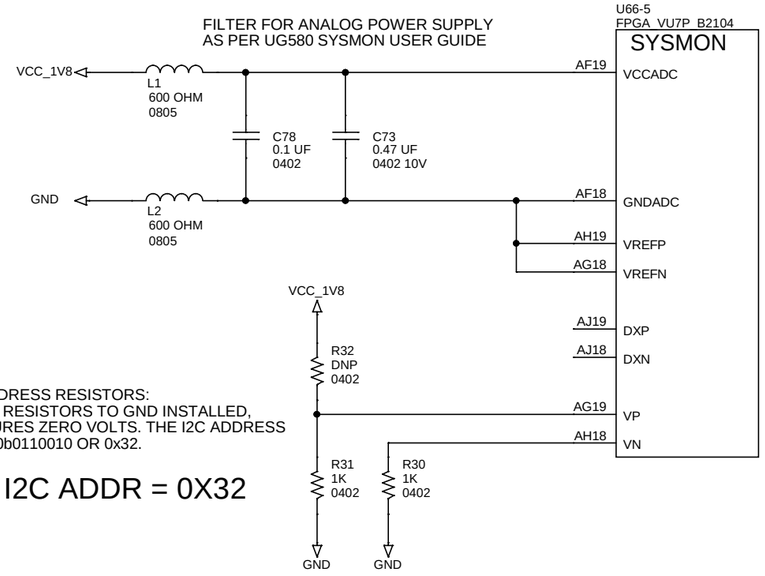



THE SYSTEM MONITOR I2C PORTS ON THE FPGAS USE AN I/O VOLTAGE OF 1.8 VOLTS. THE TCA9548A ACTS AS A LEVEL SHIFTER AS WELL AS A BUS SWITCH. THE FPGA SIGNAL PULLUPS CONNECT TO 1.8 VOLTS.

BANK 65 CONTAINS MANY DUAL-FUNCTION PINS THAT CAN BE USED DURING CONFIGURATION. THOSE PINS WILL BE MARKED AS "NO CONNECT" AND SHOULD NOT BE USED FOR NORMAL LOGIC.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 6.05: VU7P BANK 65 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 44 of 74 | |

FILTER FOR ANALOG POWER SUPPLY
AS PER UG580 SYSMON USER GUIDE




SYSMON I2C ADDRESS RESISTORS:
WITH ONLY THE RESISTORS TO GND INSTALLED, SYSMON MEASURES ZERO VOLTS. THE I2C ADDRESS IS THEREFORE 0b0110010 OR 0x32.

I2C ADDR = 0X32

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.06: VU7P SYSTEM MONITOR

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Friday, March 08, 2019 Sheet 45 of 74

THE UTILITY CLOCK MUST CONNECT TO CLOCK-CAPABLE PINS.

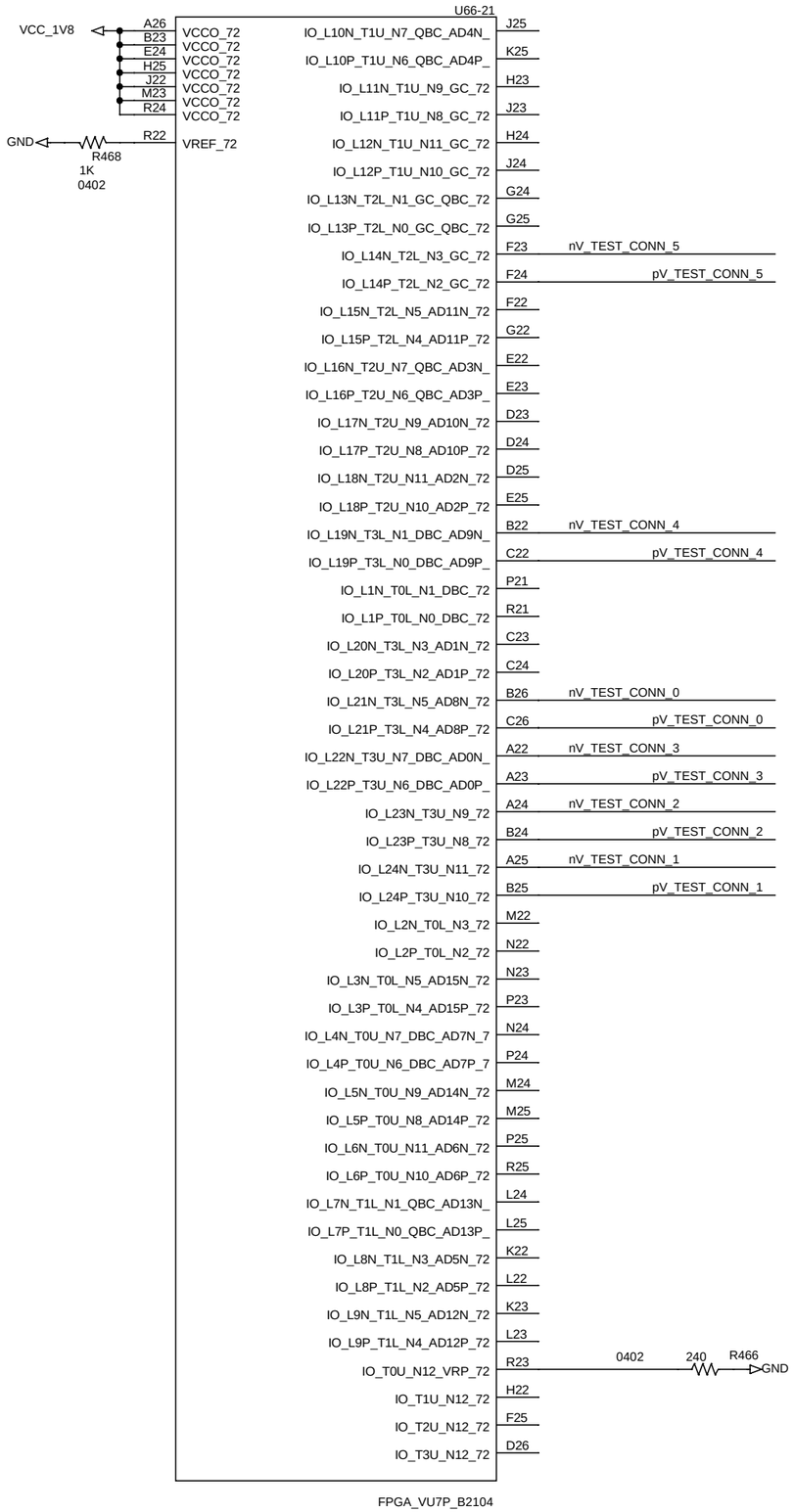
THESE CLOCK SIGNALS CONNECT TO ONE SIDE OF THE "SLR" BOUNDARY.

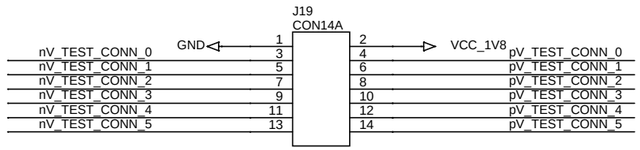
LOGIC FABRIC BOTTOM

THE "KV_SPARE" SIGNALS ARE INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS BETWEEN THE TWO FPGAS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "KV_SPARE0" AND "KV_SPARE2" SIGNALS ARE CONNECTED TO CLOCK INPUT PINS ON THE VU7P.

| | |
|---|---|
| Title | ATCA FPGA BOARD, KU15P AND VU7P, MK1 |
| | 6.07 VU7P UTILITY BANKS |
| Size | |
| Document Number | 6089-103 |
| Rev | A |
| Date: | Tuesday, February 26, 2019 |
| Sheet | 46 of 74 |



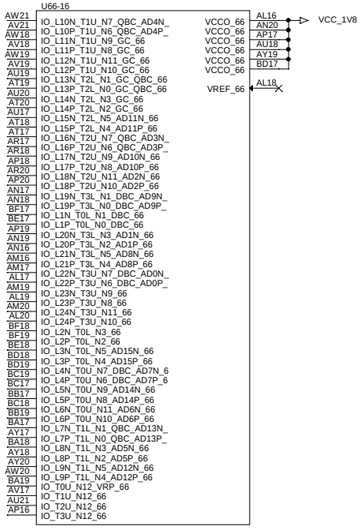




THIS CONNECTOR IS LOCATED ON THE BOTTOM OF THE BOARD. IF THE SITE IS POPULATED, THE CONNECTOR HEIGHT WILL EXCEED THE ATCA DIMENSIONS.

THE CONNECTOR SITE IS INTENDED FOR DEBUGGING OR FOR UNFORSEEN I/O NEEDS. EACH PAIR IS ROUTED AS A 100 OHM DIFFERENTIAL PAIR.

THE "V_TEST_CONN_5" SIGNAL IS CONNECTED TO GLOBAL CLOCK RESOURCES.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 6.08 VU7P TEST CONNECTOR | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 47 of 74 | |




ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 6.99: VU7P UNUSED BLOCKS

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 48 of 74

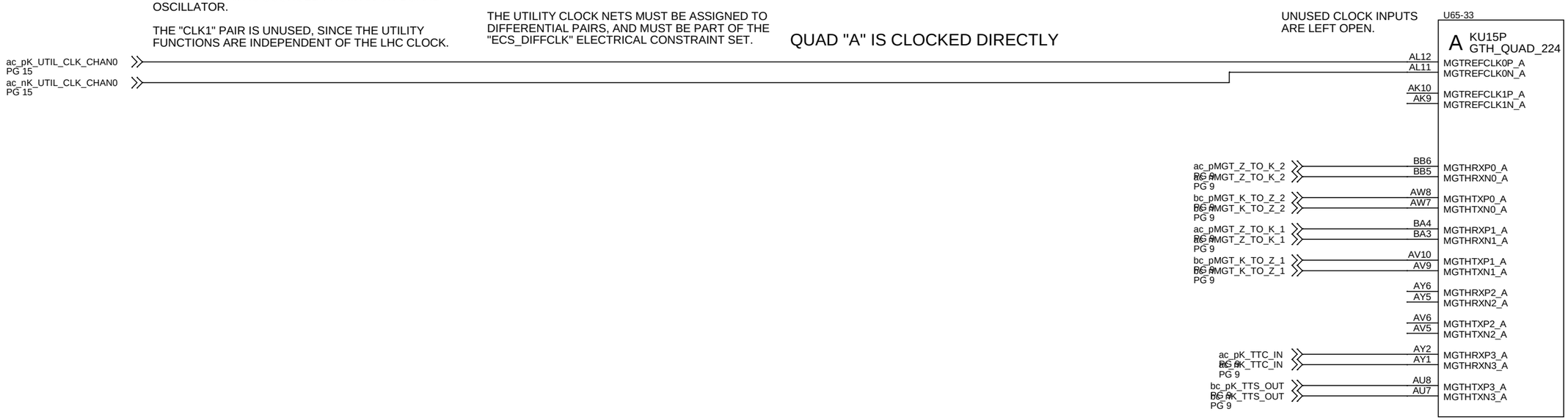
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.




# UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.01: KU15P QUAD A UTILITY #1

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 49 of 74

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

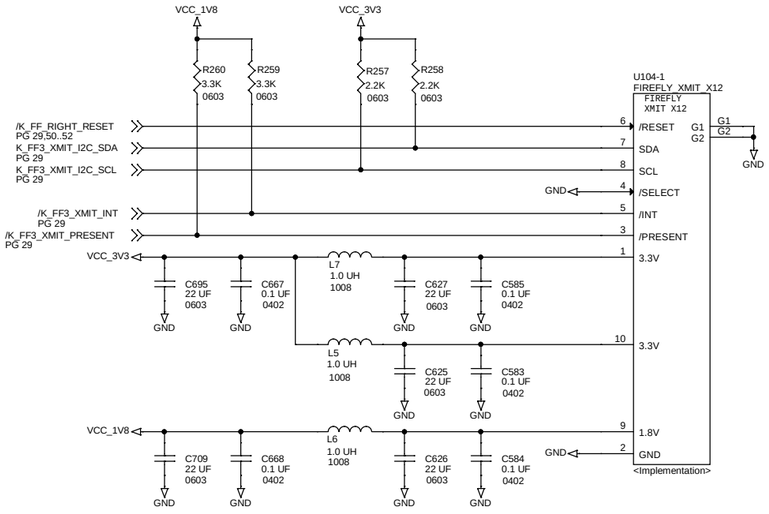
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

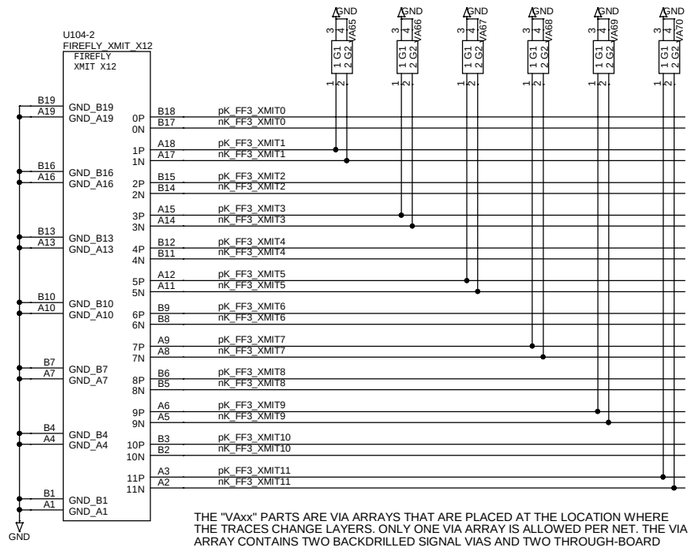
QUADS "B" AND "D" ARE CLOCKED FROM QUAD "C"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

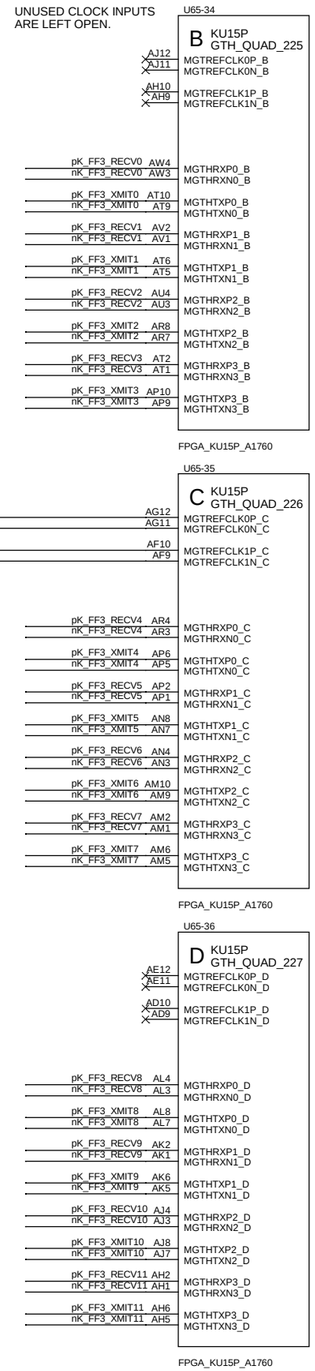
ac_pK_CLK0_CHAN PG 15
ac_nK_CLK0_CHAN PG 15
ac_pK_CLK1_CHAN PG 12
ac_nK_CLK1_CHAN PG 12

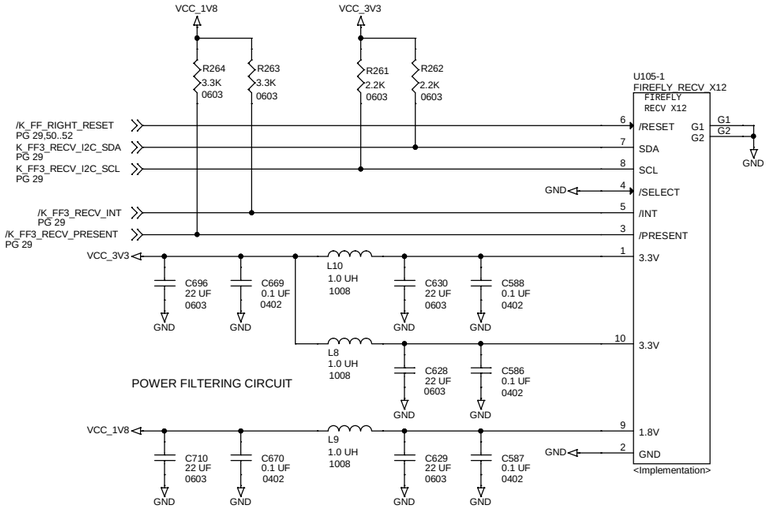



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.




THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.




POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

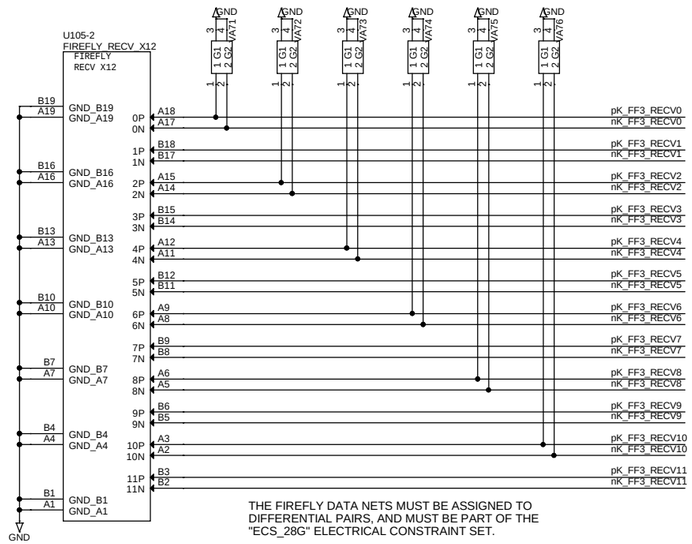
XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.




THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

| | | | |
|---|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | | |
| Title: 7.02: KU15P QUADS BCD FIREFLY X12 #3 | | | |
| Size | Document Number: 6089-103 | | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 50 of 74 | | |

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "E" AND "G" ARE CLOCKED FROM QUAD "F"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN PG 15
ac_nK_CLK0_CHAN PG 15
ac_pK_CLK1_CHAN PG 12
ac_nK_CLK1_CHAN PG 12

VCC_1V8 VCC_3V3

R268 3.3K 0603 R267 3.3K 0603 R265 2.2K 0603 R266 2.2K 0603

/K_FF_RIGHT_RESET PG 29,50..52
K_FF2_XMIT_I2C_SDA PG 29
K_FF2_XMIT_I2C_SCL PG 29
/K_FF2_XMIT_INT PG 29
/K_FF2_XMIT_PRESENT PG 29

U106-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12

6 /RESET G1 G2 → GND
7 SDA
8 SCL
4 /SELECT ← GND
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 1.8V
2 GND

VCC_3V3: L13 1.0 UH 1008; C697 22 UF 0603; C671 0.1 UF 0402; C633 22 UF 0603; C591 0.1 UF 0402
VCC_3V3: L11 1.0 UH 1008; C631 22 UF 0603; C589 0.1 UF 0402
VCC_1V8: L12 1.0 UH 1008; C711 22 UF 0603; C672 0.1 UF 0402; C632 22 UF 0603; C590 0.1 UF 0402

<Implementation>

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U106-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12

| | | | |
|---|---|---|---|
| B19 A19 | GND_B19 GND_A19 | 0P 0N | B18 A18 pK_FF2_XMIT0 nK_FF2_XMIT0 |
| | | 1P 1N | B17 A17 pK_FF2_XMIT1 nK_FF2_XMIT1 |
| B16 A16 | GND_B16 GND_A16 | 2P 2N | B15 B14 pK_FF2_XMIT2 nK_FF2_XMIT2 |
| | | 3P 3N | A15 A14 pK_FF2_XMIT3 nK_FF2_XMIT3 |
| B13 A13 | GND_B13 GND_A13 | 4P 4N | B12 B11 pK_FF2_XMIT4 nK_FF2_XMIT4 |
| | | 5P 5N | A12 A11 pK_FF2_XMIT5 nK_FF2_XMIT5 |
| B10 A10 | GND_B10 GND_A10 | 6P 6N | B9 B8 pK_FF2_XMIT6 nK_FF2_XMIT6 |
| | | 7P 7N | A9 A8 pK_FF2_XMIT7 nK_FF2_XMIT7 |
| B7 A7 | GND_B7 GND_A7 | 8P 8N | B6 B5 pK_FF2_XMIT8 nK_FF2_XMIT8 |
| | | 9P 9N | A6 A5 pK_FF2_XMIT9 nK_FF2_XMIT9 |
| B4 A4 | GND_B4 GND_A4 | 10P 10N | B3 B2 pK_FF2_XMIT10 nK_FF2_XMIT10 |
| | | 11P 11N | A3 A2 pK_FF2_XMIT11 nK_FF2_XMIT11 |
| B1 A1 | GND_B1 GND_A1 | | |

GND via 3 4 1 G1 2 G2 /A77 /A78 /A79 /A80 /A81 /A82

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

U65-37 E KU15P GTH_QUAD_228

| | |
|---|---|
| AC12 AC11 | MGTREFCLK0P_E MGTREFCLK0N_E |
| AB10 AB9 | MGTREFCLK1P_E MGTREFCLK1N_E |
| pK_FF2_RECV0 AG4 nK_FF2_RECV0 AG3 | MGTHRXP0_E MGTHRXN0_E |
| pK_FF2_XMIT0 AG8 nK_FF2_XMIT0 AG7 | MGTHTXP0_E MGTHTXN0_E |
| pK_FF2_RECV1 AF2 nK_FF2_RECV1 AF1 | MGTHRXP1_E MGTHRXN1_E |
| pK_FF2_XMIT1 AF6 nK_FF2_XMIT1 AF5 | MGTHTXP1_E MGTHTXN1_E |
| pK_FF2_RECV2 AE4 nK_FF2_RECV2 AE3 | MGTHRXP2_E MGTHRXN2_E |
| pK_FF2_XMIT2 AE8 nK_FF2_XMIT2 AE7 | MGTHTXP2_E MGTHTXN2_E |
| pK_FF2_RECV3 AD2 nK_FF2_RECV3 AD1 | MGTHRXP3_E MGTHRXN3_E |
| pK_FF2_XMIT3 AD6 nK_FF2_XMIT3 AD5 | MGTHTXP3_E MGTHTXN3_E |

FPGA_KU15P_A1760

U65-38 F KU15P GTH_QUAD_229

| | |
|---|---|
| AA12 AA11 | MGTREFCLK0P_F MGTREFCLK0N_F |
| Y10 Y9 | MGTREFCLK1P_F MGTREFCLK1N_F |
| pK_FF2_RECV4 AC4 nK_FF2_RECV4 AC3 | MGTHRXP0_F MGTHRXN0_F |
| pK_FF2_XMIT4 AC8 nK_FF2_XMIT4 AC7 | MGTHTXP0_F MGTHTXN0_F |
| pK_FF2_RECV5 AB2 nK_FF2_RECV5 AB1 | MGTHRXP1_F MGTHRXN1_F |
| pK_FF2_XMIT5 AB6 nK_FF2_XMIT5 AB5 | MGTHTXP1_F MGTHTXN1_F |
| pK_FF2_RECV6 AA4 nK_FF2_RECV6 AA3 | MGTHRXP2_F MGTHRXN2_F |
| pK_FF2_XMIT6 AA8 nK_FF2_XMIT6 AA7 | MGTHTXP2_F MGTHTXN2_F |
| pK_FF2_RECV7 Y2 nK_FF2_RECV7 Y1 | MGTHRXP3_F MGTHRXN3_F |
| pK_FF2_XMIT7 Y6 nK_FF2_XMIT7 Y5 | MGTHTXP3_F MGTHTXN3_F |

FPGA_KU15P_A1760

VCC_1V8 VCC_3V3

R272 3.3K 0603 R271 3.3K 0603 R269 2.2K 0603 R270 2.2K 0603

/K_FF_RIGHT_RESET PG 29,50..52
K_FF2_RECV_I2C_SDA PG 29
K_FF2_RECV_I2C_SCL PG 29
/K_FF2_RECV_INT PG 29
/K_FF2_RECV_PRESENT PG 29

U107-1 FIREFLY_RECV_X12 FIREFLY RECV X12

6 /RESET G1 G2 → GND
7 SDA
8 SCL
4 /SELECT ← GND
5 /INT
3 /PRESENT
1 3.3V
10 3.3V
9 1.8V
2 GND

VCC_3V3: L16 1.0 UH 1008; C706 22 UF 0603; C673 0.1 UF 0402; C636 22 UF 0603; C594 0.1 UF 0402
VCC_3V3: L14 1.0 UH 1008; C634 22 UF 0603; C592 0.1 UF 0402
VCC_1V8: L15 1.0 UH 1008; C712 22 UF 0603; C674 0.1 UF 0402; C635 22 UF 0603; C593 0.1 UF 0402

<Implementation>

POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
0x54 = 7 BIT ADDRESS
0xA8 = 8 BIT WRITE ADDRESS
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

U107-2 FIREFLY_RECV_X12 FIREFLY RECV X12

| | | | |
|---|---|---|---|
| B19 A19 | GND_B19 GND_A19 | 0P 0N | A18 A17 pK_FF2_RECV0 nK_FF2_RECV0 |
| | | 1P 1N | B18 B17 pK_FF2_RECV1 nK_FF2_RECV1 |
| B16 A16 | GND_B16 GND_A16 | 2P 2N | A15 A14 pK_FF2_RECV2 nK_FF2_RECV2 |
| | | 3P 3N | B15 B14 pK_FF2_RECV3 nK_FF2_RECV3 |
| B13 A13 | GND_B13 GND_A13 | 4P 4N | A12 A11 pK_FF2_RECV4 nK_FF2_RECV4 |
| | | 5P 5N | B12 B11 pK_FF2_RECV5 nK_FF2_RECV5 |
| B10 A10 | GND_B10 GND_A10 | 6P 6N | A9 A8 pK_FF2_RECV6 nK_FF2_RECV6 |
| | | 7P 7N | B9 B8 pK_FF2_RECV7 nK_FF2_RECV7 |
| B7 A7 | GND_B7 GND_A7 | 8P 8N | A6 A5 pK_FF2_RECV8 nK_FF2_RECV8 |
| | | 9P 9N | B6 B5 pK_FF2_RECV9 nK_FF2_RECV9 |
| B4 A4 | GND_B4 GND_A4 | 10P 10N | A3 A2 pK_FF2_RECV10 nK_FF2_RECV10 |
| | | 11P 11N | B3 B2 pK_FF2_RECV11 nK_FF2_RECV11 |
| B1 A1 | GND_B1 GND_A1 | | |

GND via 3 4 1 G1 2 G2 /A83 /A84 /A85 /A86 /A87 /A88

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

U65-39 G KU15P GTH_QUAD_230

| | |
|---|---|
| W12 W11 | MGTREFCLK0P_G MGTREFCLK0N_G |
| V10 V9 | MGTREFCLK1P_G MGTREFCLK1N_G |
| pK_FF2_RECV8 W4 nK_FF2_RECV8 W3 | MGTHRXP0_G MGTHRXN0_G |
| pK_FF2_XMIT8 W8 nK_FF2_XMIT8 W7 | MGTHTXP0_G MGTHTXN0_G |
| pK_FF2_RECV9 V2 nK_FF2_RECV9 V1 | MGTHRXP1_G MGTHRXN1_G |
| pK_FF2_XMIT9 V6 nK_FF2_XMIT9 V5 | MGTHTXP1_G MGTHTXN1_G |
| pK_FF2_RECV10 U4 nK_FF2_RECV10 U3 | MGTHRXP2_G MGTHRXN2_G |
| pK_FF2_XMIT10 U8 nK_FF2_XMIT10 U7 | MGTHTXP2_G MGTHTXN2_G |
| pK_FF2_RECV11 T2 nK_FF2_RECV11 T1 | MGTHRXP3_G MGTHRXN3_G |
| pK_FF2_XMIT11 T6 nK_FF2_XMIT11 T5 | MGTHTXP3_G MGTHTXN3_G |

FPGA_KU15P_A1760

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.03: KU15P QUADS EFG FIREFLY X12 #2

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 51 of 74

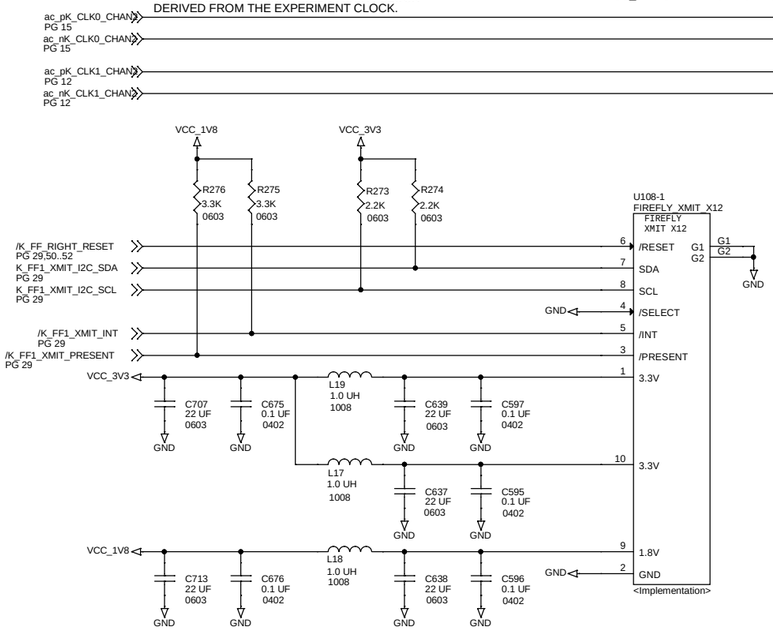
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

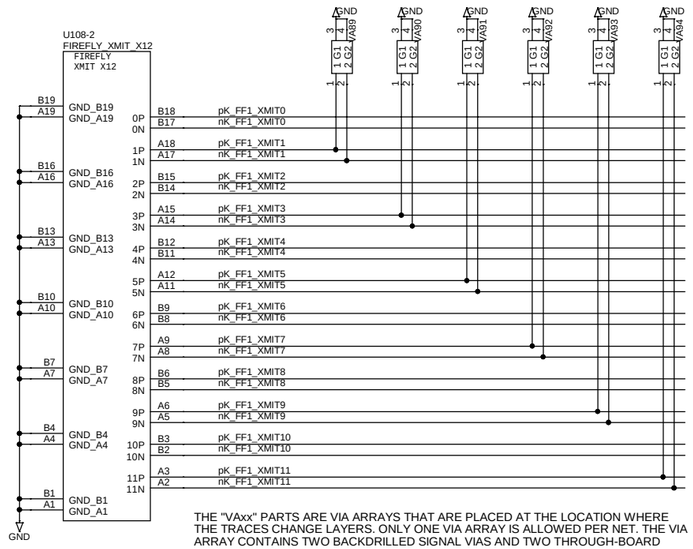
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

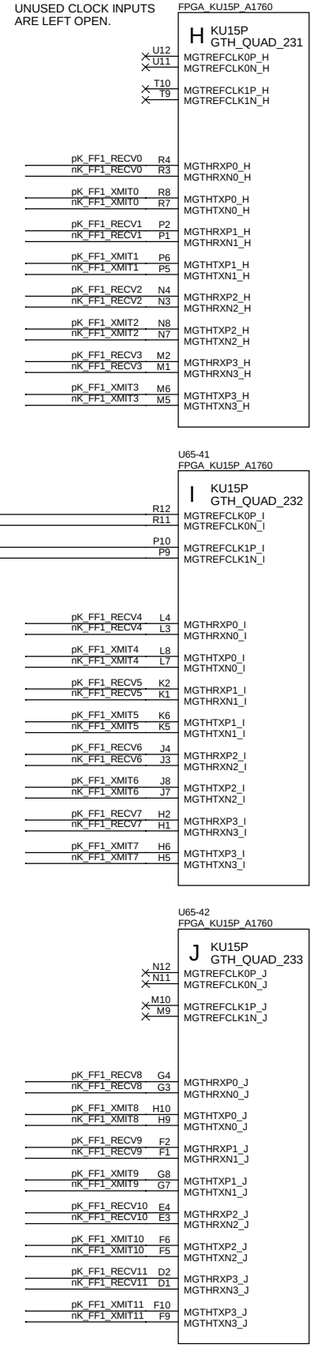
UNUSED CLOCK INPUTS ARE LEFT OPEN.

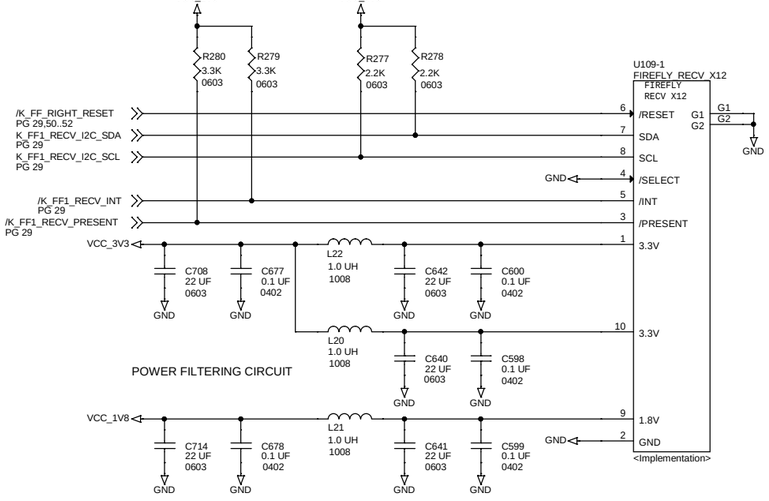



ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

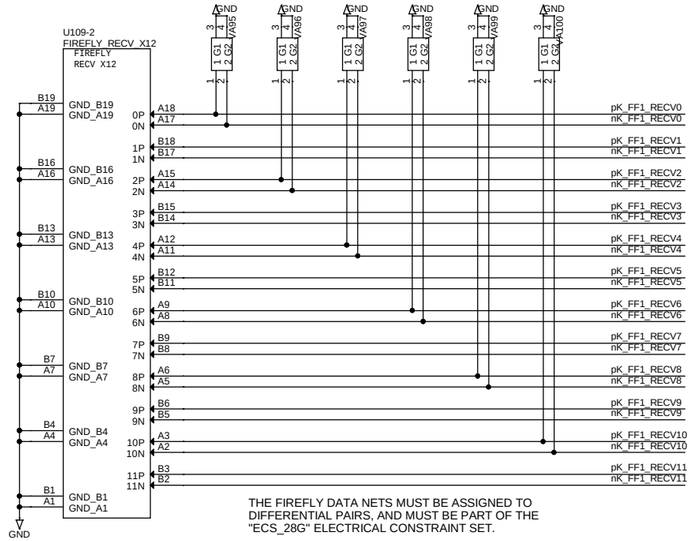



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.




POWER FILTERING CIRCUIT




THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.




The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

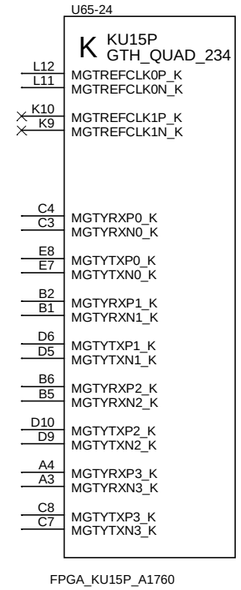
ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.04: KU15P QUADS HIJ FIREFLY X12 #1

Size: | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 52 of 74

QUAD "K" IS UNUSED




FPGA_KU15P_A1760

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.05: KU15P QUAD K UNUSED

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 53 of 74

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

# QUADS "L" AND "N" ARE CLOCKED FROM QUAD "M"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pK_CLK0_CHAN4 PG 15
ac_nK_CLK0_CHAN4 PG 15
ac_pK_CLK1_CHAN4 PG 12
ac_nK_CLK1_CHAN4 PG 12

U65-25
L KU15P GTY_QUAD_127
AG30 MGTREFCLK0P_L
AG31 MGTREFCLK0N_L
AE30 MGTREFCLK1P_L
AE31 MGTREFCLK1N_L
pK_FF7_RECV11 AT41 MGTYRXP0_L
nK_FF7_RECV11 AT42 MGTYRXN0_L
pK_FF7_XMIT11 AM36 MGTYTXP0_L
nK_FF7_XMIT11 AM37 MGTYTXN0_L
pK_FF7_RECV10 AR39 MGTYRXP1_L
nK_FF7_RECV10 AR40 MGTYRXN1_L
pK_FF7_XMIT10 AL34 MGTYTXP1_L
nK_FF7_XMIT10 AL35 MGTYTXN1_L
pK_FF7_RECV9 AP41 MGTYRXP2_L
nK_FF7_RECV9 AP42 MGTYRXN2_L
pK_FF7_XMIT9 AK36 MGTYTXP2_L
nK_FF7_XMIT9 AK37 MGTYTXN2_L
pK_FF7_RECV8 AN39 MGTYRXP3_L
nK_FF7_RECV8 AN40 MGTYRXN3_L
pK_FF7_XMIT8 AJ34 MGTYTXP3_L
nK_FF7_XMIT8 AJ35 MGTYTXN3_L
FPGA_KU15P_A1760

U65-26
M KU15P GTY_QUAD_128
AD32 MGTREFCLK0P_M
AD33 MGTREFCLK0N_M
AC30 MGTREFCLK1P_M
AC31 MGTREFCLK1N_M
pK_FF7_RECV7 AM41 MGTYRXP0_M
nK_FF7_RECV7 AM42 MGTYRXN0_M
pK_FF7_XMIT7 AH32 MGTYTXP0_M
nK_FF7_XMIT7 AH33 MGTYTXN0_M
pK_FF7_RECV6 AL39 MGTYRXP1_M
nK_FF7_RECV6 AL40 MGTYRXN1_M
pK_FF7_XMIT6 AH36 MGTYTXP1_M
nK_FF7_XMIT6 AH37 MGTYTXN1_M
pK_FF7_RECV5 AK41 MGTYRXP2_M
nK_FF7_RECV5 AK42 MGTYRXN2_M
pK_FF7_XMIT5 AG34 MGTYTXP2_M
nK_FF7_XMIT5 AG35 MGTYTXN2_M
pK_FF7_RECV4 AJ39 MGTYRXP3_M
nK_FF7_RECV4 AJ40 MGTYRXN3_M
pK_FF7_XMIT4 AF32 MGTYTXP3_M
nK_FF7_XMIT4 AF33 MGTYTXN3_M
FPGA_KU15P_A1760

U65-27
N KU15P GTY_QUAD_129
AB32 MGTREFCLK0P_N
AB33 MGTREFCLK0N_N
AA30 MGTREFCLK1P_N
AA31 MGTREFCLK1N_N
pK_FF7_RECV3 AH41 MGTYRXP0_N
nK_FF7_RECV3 AH42 MGTYRXN0_N
pK_FF7_XMIT3 AF36 MGTYTXP0_N
nK_FF7_XMIT3 AF37 MGTYTXN0_N
pK_FF7_RECV2 AG39 MGTYRXP1_N
nK_FF7_RECV2 AG40 MGTYRXN1_N
pK_FF7_XMIT2 AE34 MGTYTXP1_N
nK_FF7_XMIT2 AE35 MGTYTXN1_N
pK_FF7_RECV1 AF41 MGTYRXP2_N
nK_FF7_RECV1 AF42 MGTYRXN2_N
pK_FF7_XMIT1 AD36 MGTYTXP2_N
nK_FF7_XMIT1 AD37 MGTYTXN2_N
pK_FF7_RECV0 AE39 MGTYRXP3_N
nK_FF7_RECV0 AE40 MGTYRXN3_N
pK_FF7_XMIT0 AC34 MGTYTXP3_N
nK_FF7_XMIT0 AC35 MGTYTXN3_N
FPGA_KU15P_A1760

VCC_1V8 VCC_3V3
R601 3.3K 0603
R602 3.3K 0603
R604 2.2K 0603
R603 2.2K 0603

U20-1 FIREFLY_XMIT_X12 FIREFLY XMIT X12
/K_FF_LEFT_RESET PG 29,54,56..58 → /RESET
K_FF7_XMIT_I2C_SDA PG 29 → SDA
K_FF7_XMIT_I2C_SCL PG 29 → SCL
GND → /SELECT
/K_FF7_XMIT_INT PG 29 → /INT
/K_FF7_XMIT_PRESENT PG 29 → /PRESENT
3.3V
3.3V
1.8V
GND
G1 G2 GND
<Implementation>

L47 1.0 UH 1008
L49 1.0 UH 1008
L48 1.0 UH 1008
C847 22 UF 0603
C860 0.1 UF 0402
C884 22 UF 0603
C920 0.1 UF 0402
C886 22 UF 0603
C922 0.1 UF 0402
C836 22 UF 0603
C859 0.1 UF 0402
C885 22 UF 0603
C921 0.1 UF 0402

ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

U20-2 FIREFLY_XMIT_X12 FIREFLY XMIT X12
GND_B19 A19, GND_B16 A16, GND_B13 A13, GND_B10 A10, GND_B7 A7, GND_B4 A4, GND_B1 A1
0P 0N, 1P 1N, 2P 2N, 3P 3N, 4P 4N, 5P 5N, 6P 6N, 7P 7N, 8P 8N, 9P 9N, 10P 10N, 11P 11N
B18 A18 pK_FF7_XMIT0 / B17 A17 nK_FF7_XMIT0
B15 A15 pK_FF7_XMIT1 / B14 A14 nK_FF7_XMIT1
B12 A12 pK_FF7_XMIT2 / B11 A11 nK_FF7_XMIT2
B9 A9 pK_FF7_XMIT3 / B8 A8 nK_FF7_XMIT3
B6 A6 pK_FF7_XMIT4 / B5 A5 nK_FF7_XMIT4
B3 A3 pK_FF7_XMIT5 / B2 A2 nK_FF7_XMIT5
pK_FF7_XMIT6 / nK_FF7_XMIT6
pK_FF7_XMIT7 / nK_FF7_XMIT7
pK_FF7_XMIT8 / nK_FF7_XMIT8
pK_FF7_XMIT9 / nK_FF7_XMIT9
pK_FF7_XMIT10 / nK_FF7_XMIT10
pK_FF7_XMIT11 / nK_FF7_XMIT11
GND VA4 VA3 VA2 VA1

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

VCC_1V8 VCC_3V3
R605 3.3K 0603
R606 3.3K 0603
R608 2.2K 0603
R607 2.2K 0603

U21-1 FIREFLY_RECV_X12 FIREFLY RECV X12
/K_FF_LEFT_RESET PG 29,54,56..58 → /RESET
K_FF7_RECV_I2C_SDA PG 29 → SDA
K_FF7_RECV_I2C_SCL PG 29 → SCL
GND → /SELECT
/K_FF7_RECV_INT PG 29 → /INT
/K_FF7_RECV_PRESENT PG 29 → /PRESENT
3.3V
3.3V
1.8V
GND
G1 G2 GND
<Implementation>

L50 1.0 UH 1008
L52 1.0 UH 1008
L51 1.0 UH 1008
C848 22 UF 0603
C862 0.1 UF 0402
C887 22 UF 0603
C923 0.1 UF 0402
C889 22 UF 0603
C925 0.1 UF 0402
C837 22 UF 0603
C861 0.1 UF 0402
C888 22 UF 0603
C924 0.1 UF 0402

POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
0x54 = 7 BIT ADDRESS
0xA8 = 8 BIT WRITE ADDRESS
0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

U21-2 FIREFLY_RECV_X12 FIREFLY RECV X12
GND_B19 A19, GND_B16 A16, GND_B13 A13, GND_B10 A10, GND_B7 A7, GND_B4 A4, GND_B1 A1
0P 0N, 1P 1N, 2P 2N, 3P 3N, 4P 4N, 5P 5N, 6P 6N, 7P 7N, 8P 8N, 9P 9N, 10P 10N, 11P 11N
A18 A17 pK_FF7_RECV0 / nK_FF7_RECV0
B18 B17 pK_FF7_RECV1 / nK_FF7_RECV1
A15 A14 pK_FF7_RECV2 / nK_FF7_RECV2
B15 B14 pK_FF7_RECV3 / nK_FF7_RECV3
A12 A11 pK_FF7_RECV4 / nK_FF7_RECV4
B12 B11 pK_FF7_RECV5 / nK_FF7_RECV5
A9 A8 pK_FF7_RECV6 / nK_FF7_RECV6
B9 B8 pK_FF7_RECV7 / nK_FF7_RECV7
A6 A5 pK_FF7_RECV8 / nK_FF7_RECV8
B6 B5 pK_FF7_RECV9 / nK_FF7_RECV9
A3 A2 pK_FF7_RECV10 / nK_FF7_RECV10
B3 B2 pK_FF7_RECV11 / nK_FF7_RECV11
GND VA11 VA10 VA9 VA8 VA7

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

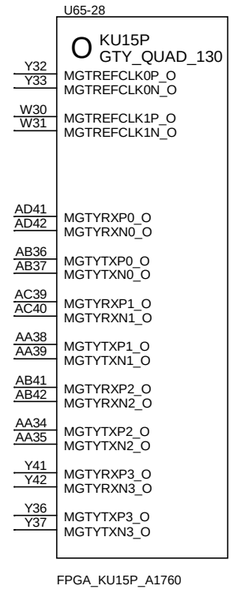
ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.06: KU15P QUADS LMN FIREFLY X12 #7

Size: | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 54 of 74

QUAD "O" IS UNUSED




ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.07: KU15P QUAD O UNUSED

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 55 of 74

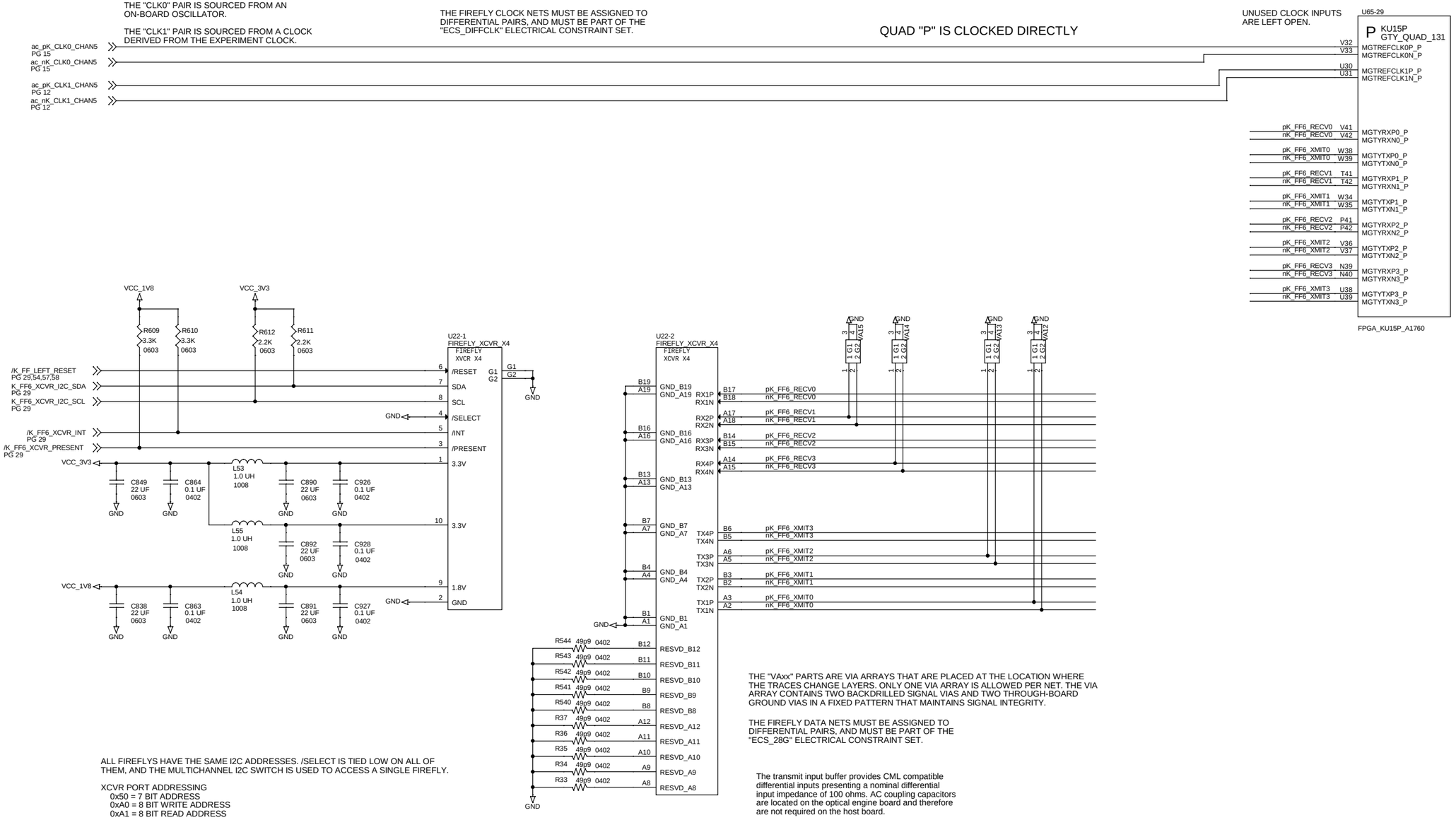
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.










THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

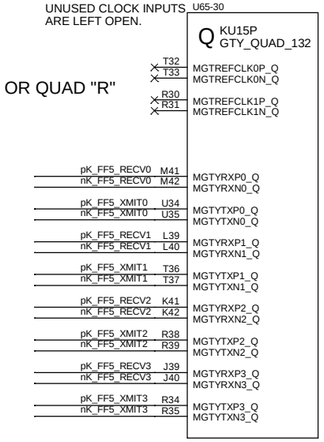
THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

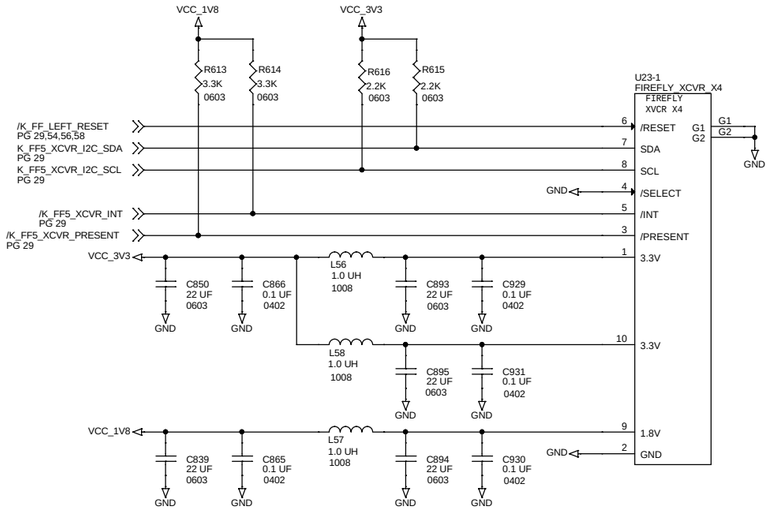
HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

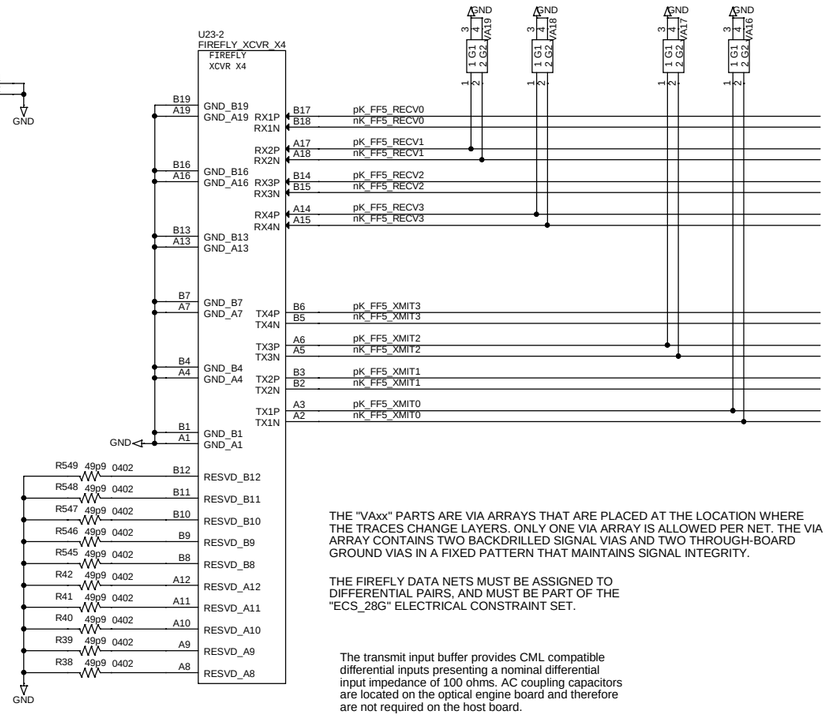
| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 7.08: KU15P QUAD P FIREFLY X4 #6 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 56 of 74 | |

UNUSED CLOCK INPUTS ARE LEFT OPEN.

QUAD "Q" CAN BE CLOCKED FROM QUAD "P" OR QUAD "R"




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.09: KU15P QUAD R FIREFLY X4 #5

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 57 of 74

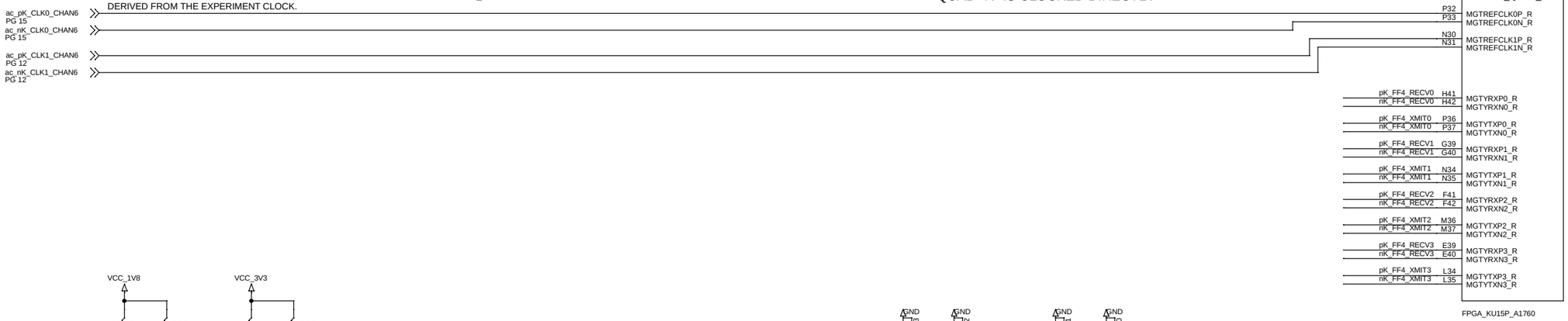
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

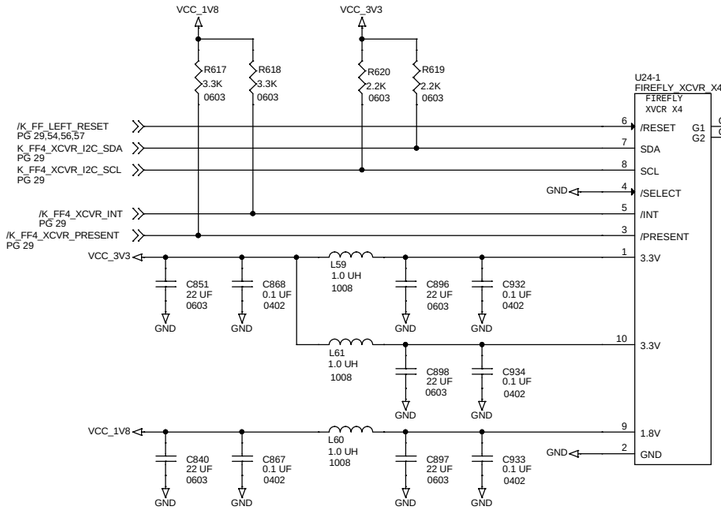
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

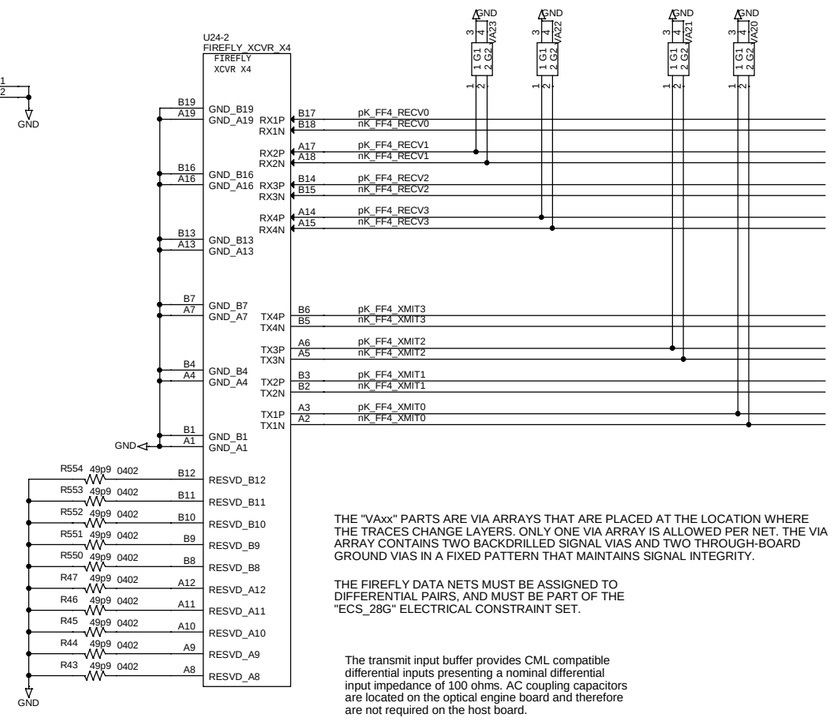
## QUAD "R" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.




FPGA_KU15P_A1760







ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.10: KU15P QUAD R FIREFLY X4 #4

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 58 of 74

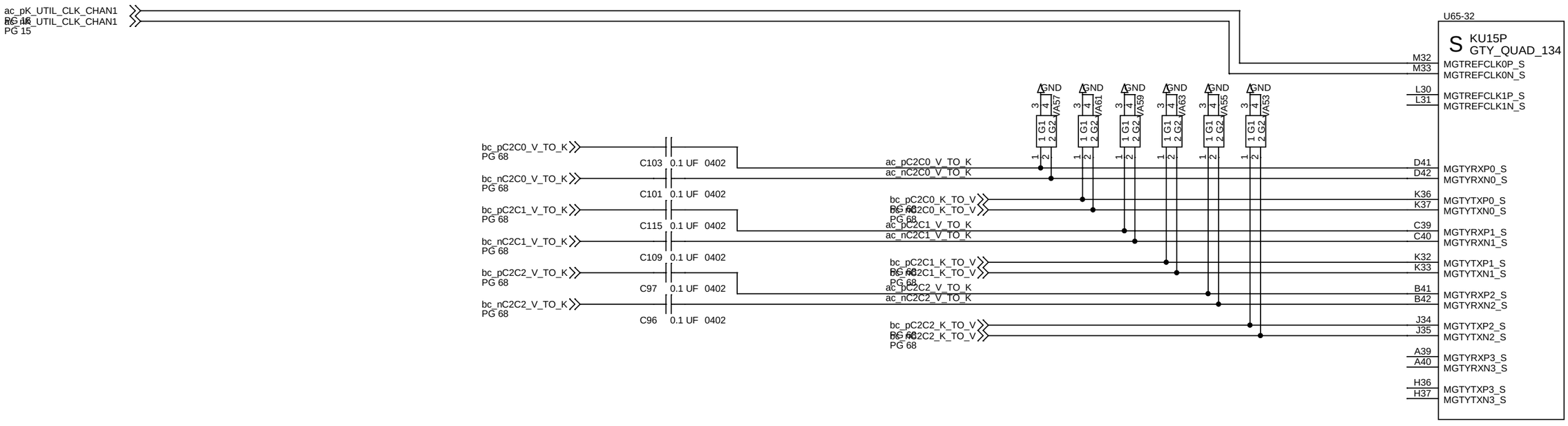
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

## QUAD "S" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.




THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

# CONNECT UTILITY NETS HERE

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 7.11: KU15P QUAD S CHIP-TO-CHIP

| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

Date: Tuesday, February 26, 2019 Sheet 59 of 74

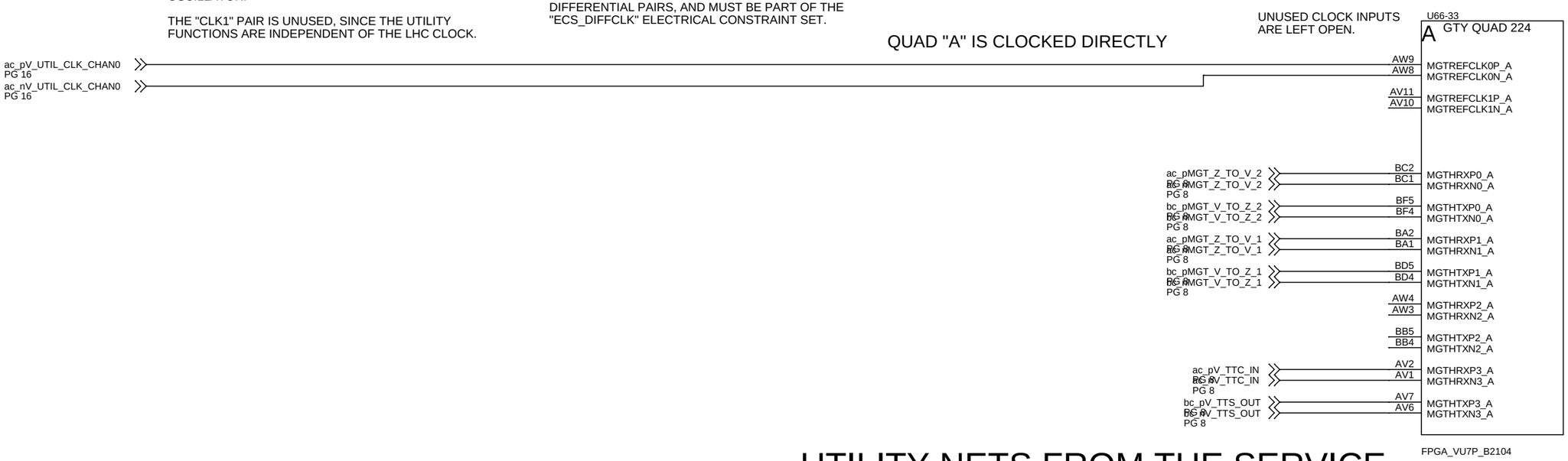
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "A" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.




# UTILITY NETS FROM THE SERVICE BOARD HIGH SPEED CONNECTOR

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.01: VU7P QUAD A UTILITY #1 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 60 of 74 | |

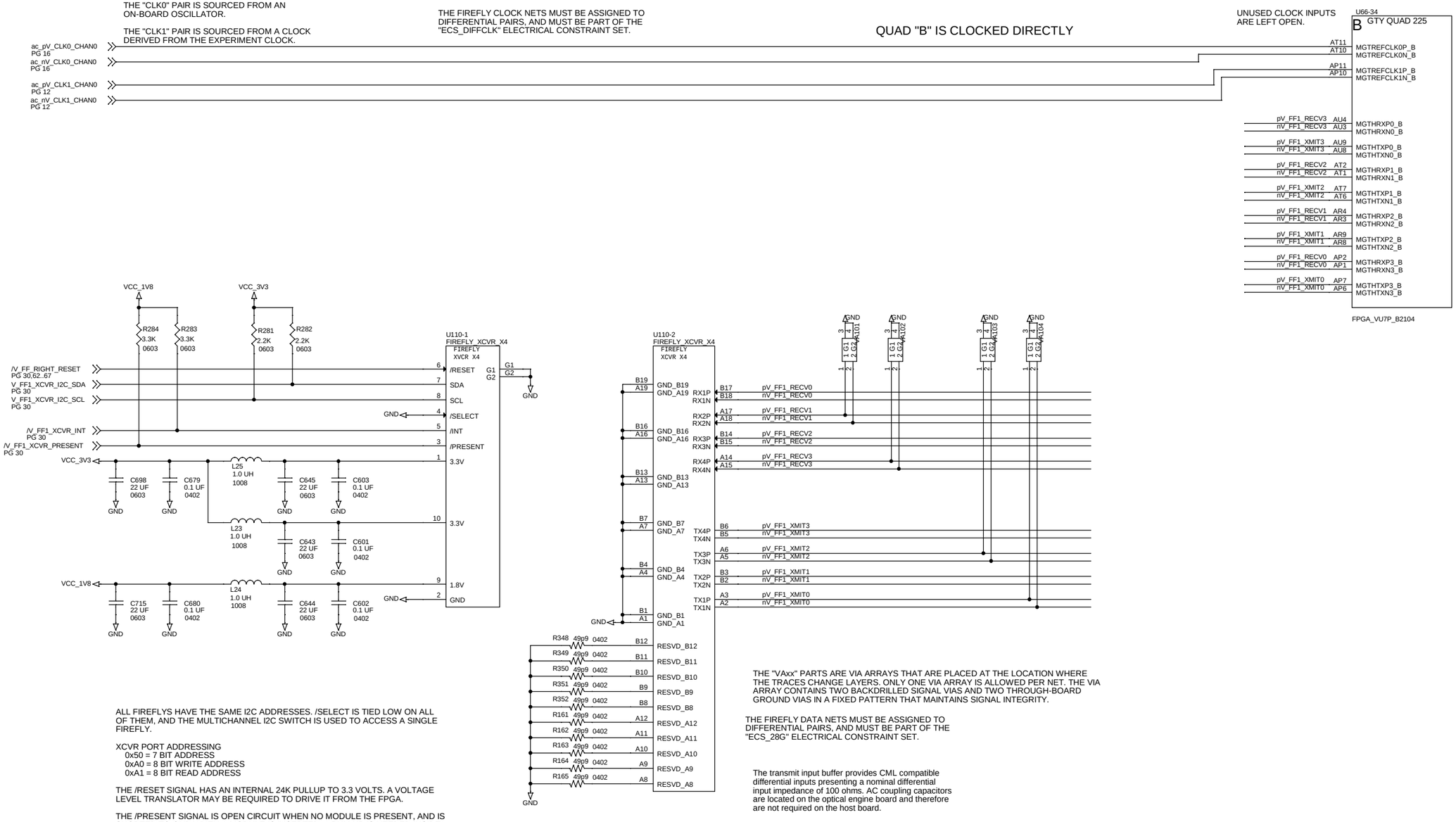
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "B" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.










ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

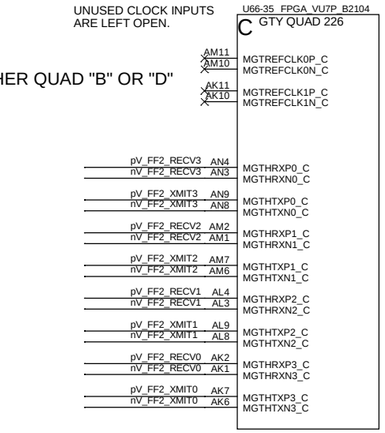
Title: 8.02: VU7P QUAD B FIREFLY X4 #1

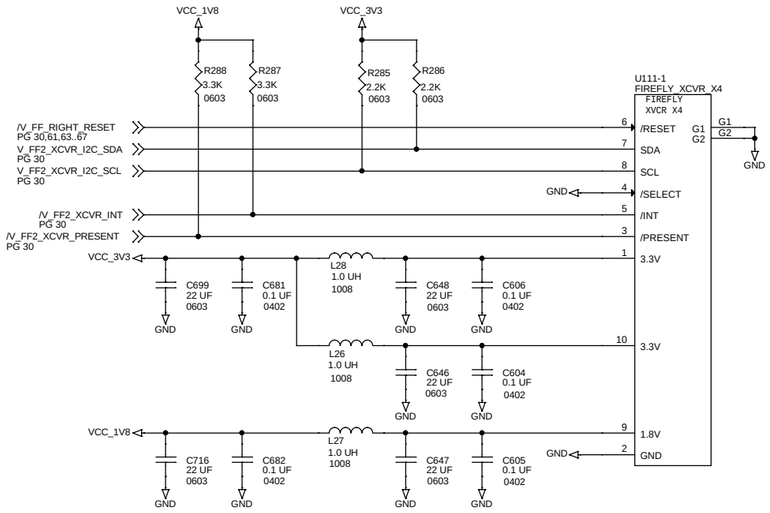
Size | Document Number: 6089-103 | Rev: A

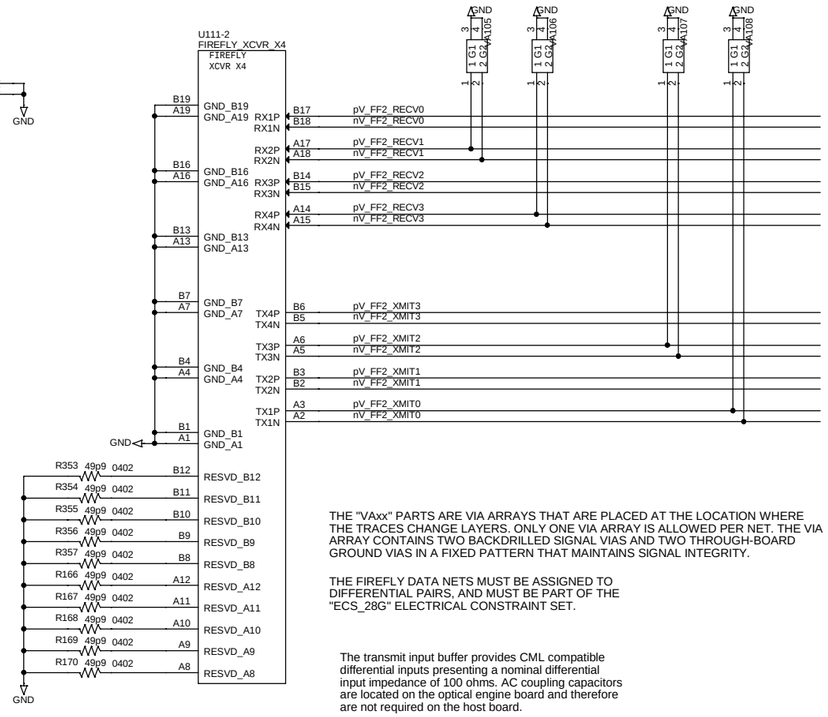
Date: Tuesday, February 26, 2019 | Sheet 61 of 74

UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "C" IS CLOCKED FROM EITHER QUAD "B" OR "D"




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.03: VU7P QUAD C FIREFLY X4 #2 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 62 of 74 | |

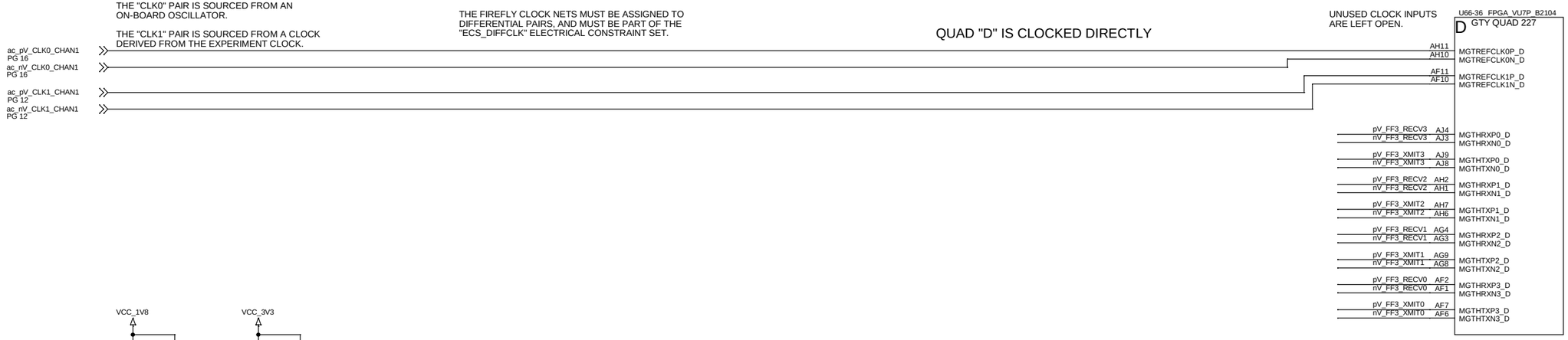
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

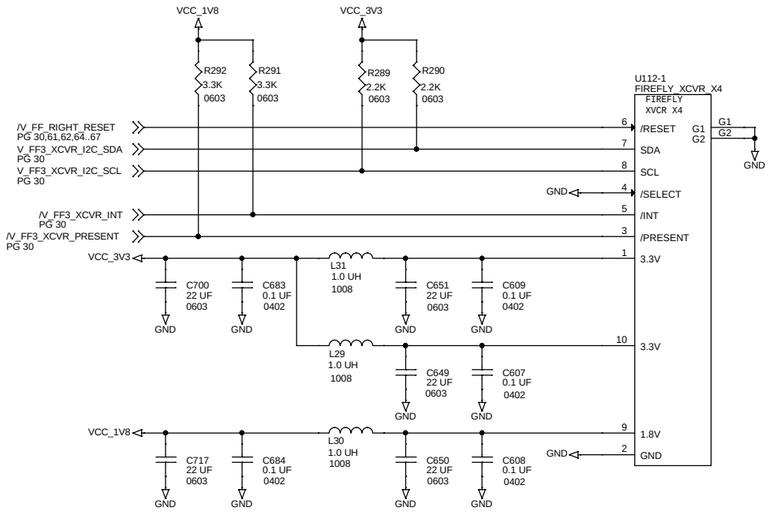
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

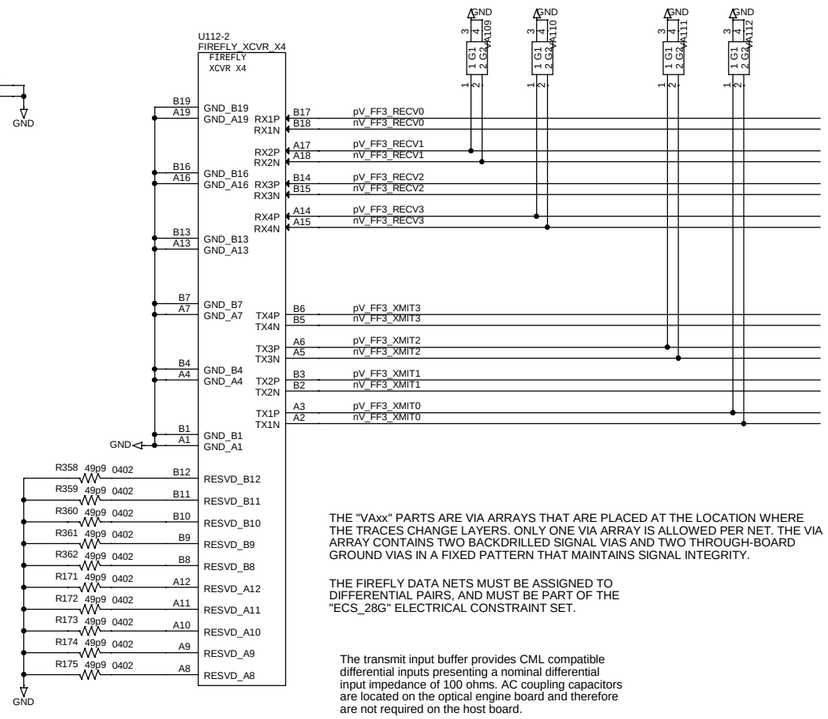
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

## QUAD "D" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

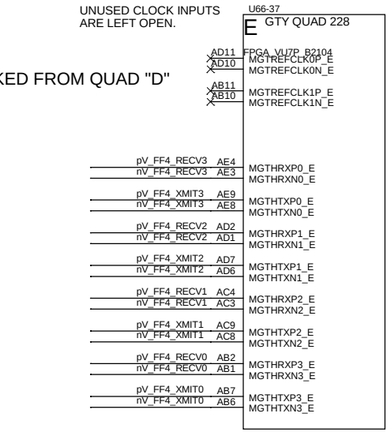
The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

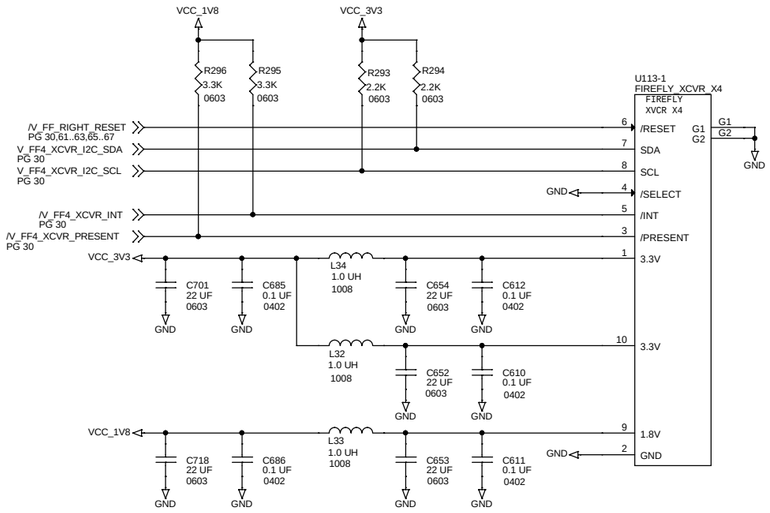
HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

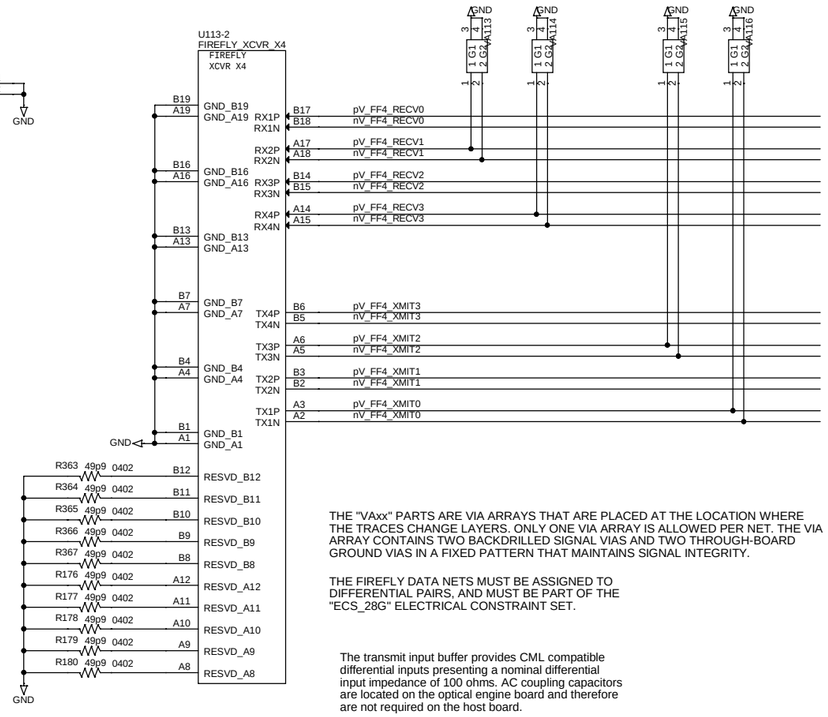
| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.04: VU7P QUAD D FIREFLY X4 #3 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 63 of 74 | |

UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "E" IS CLOCKED FROM QUAD "D"




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

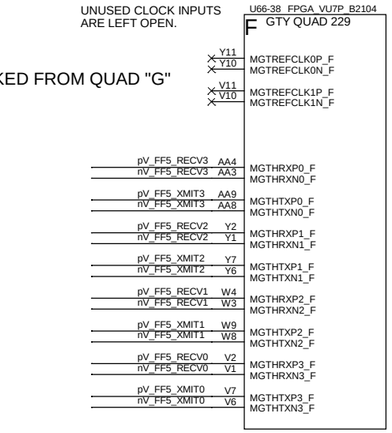
Title: 8.05: VU7P QUAD E FIREFLY X4 #4

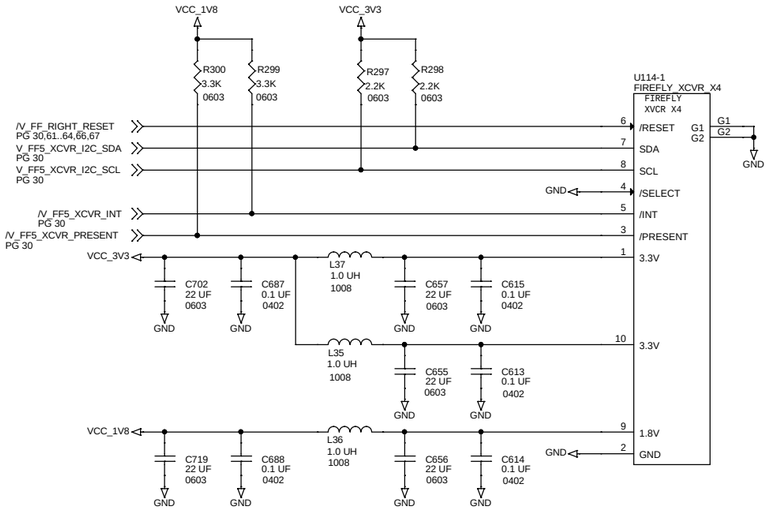
| Size | Document Number | Rev |
|---|---|---|
| | 6089-103 | A |

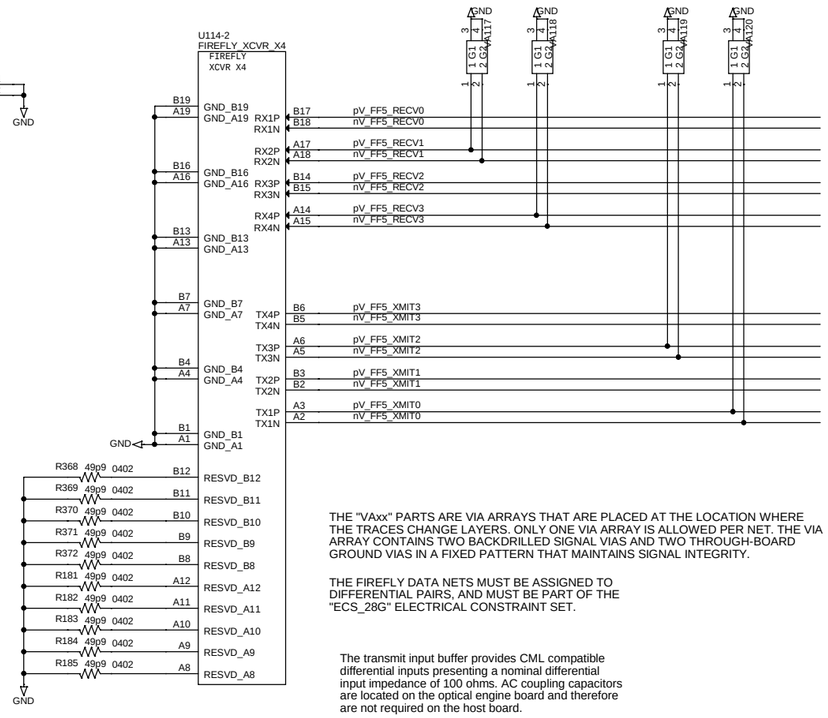
Date: Tuesday, February 26, 2019 Sheet 64 of 74

UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "F" IS CLOCKED FROM QUAD "G"




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.06: VU7P QUAD F FIREFLY X4 #5

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 65 of 74

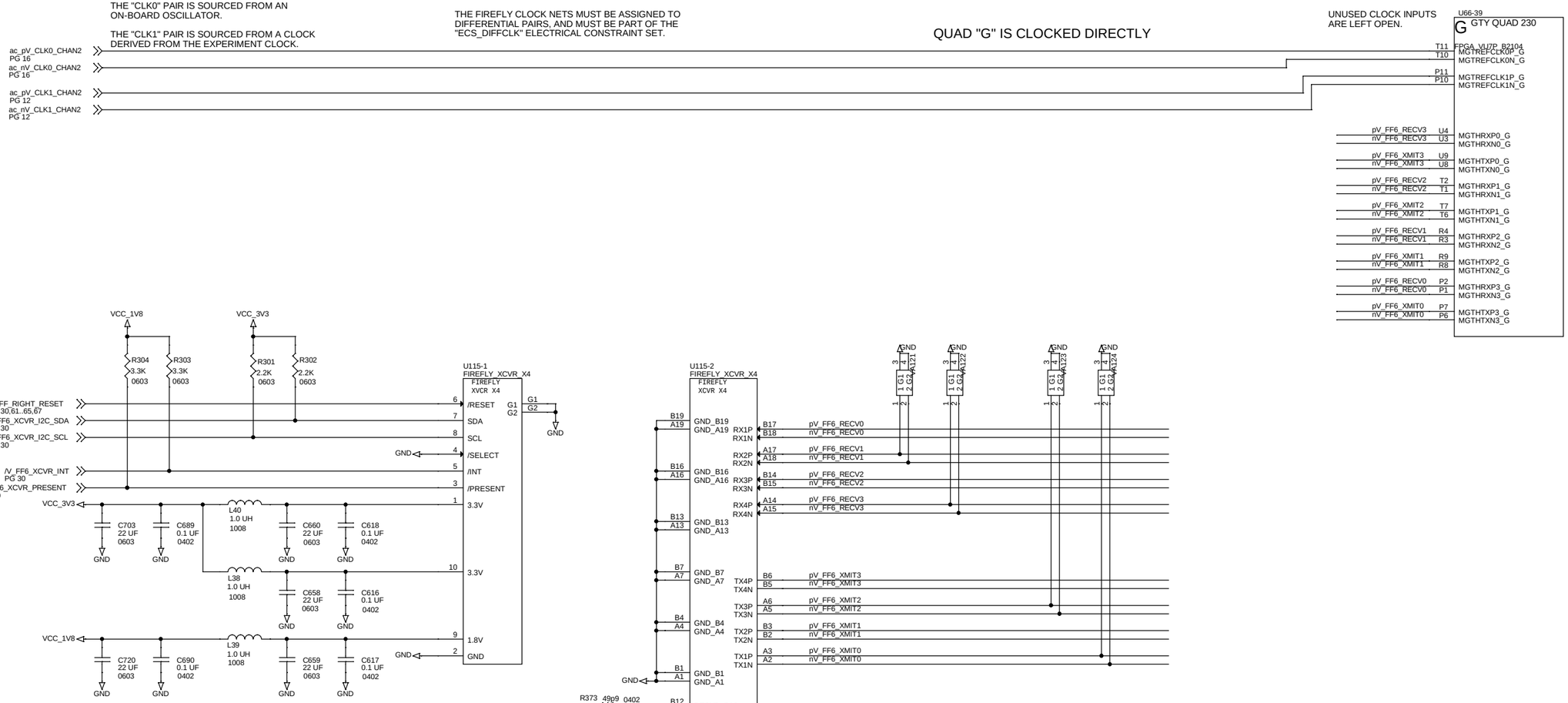
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

## QUAD "G" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.










ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.07: VU7P QUAD G FIREFLY X4 #6

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 66 of 74

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

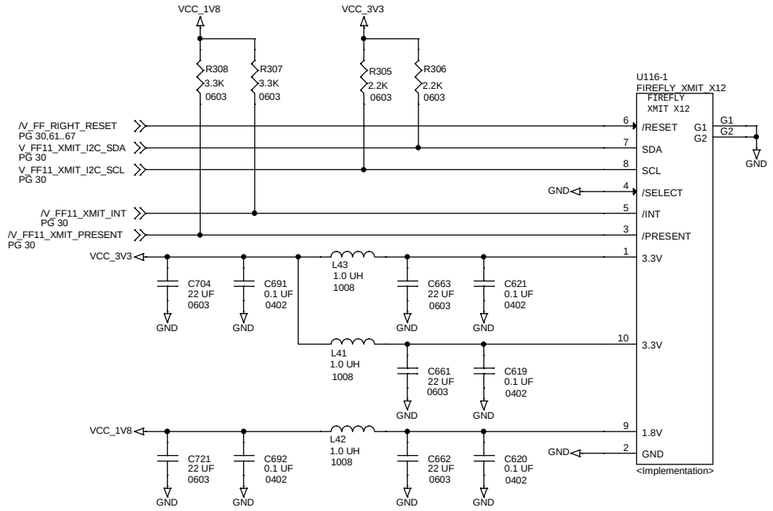
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

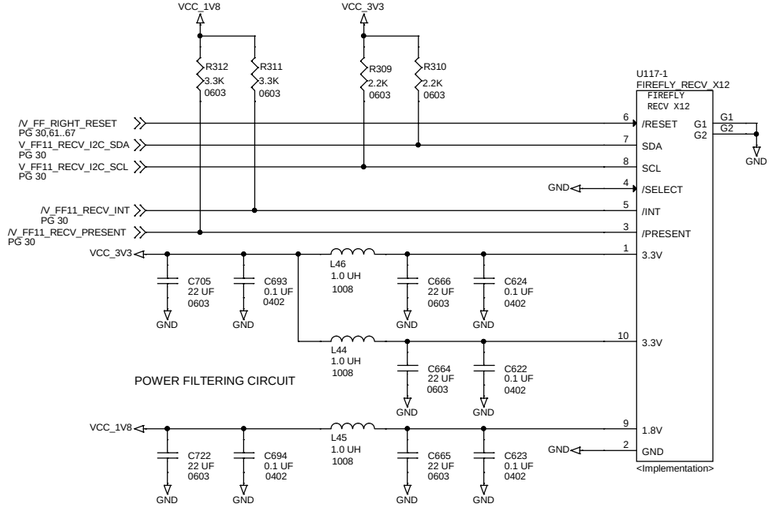
QUADS "H" AND "J" ARE CLOCKED FROM QUAD "I"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

ac_pV_CLK0_CHAN PG 16
ac_nV_CLK0_CHAN PG 16
ac_pV_CLK1_CHAN PG 12
ac_nV_CLK1_CHAN PG 12




ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.




POWER FILTERING CIRCUIT

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

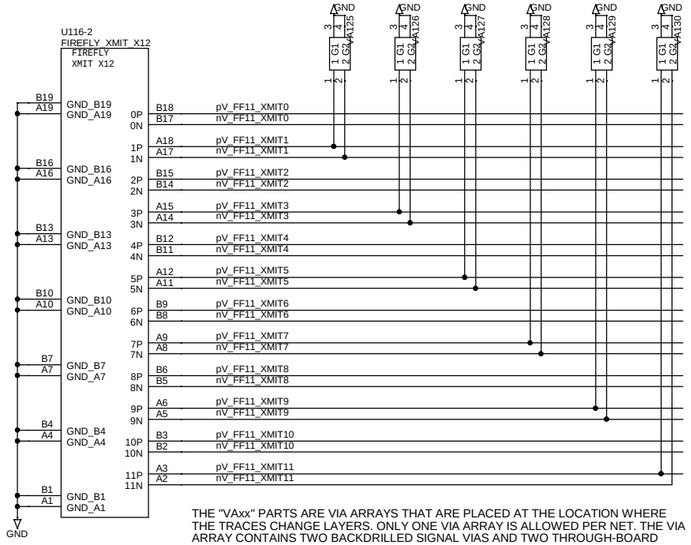
XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

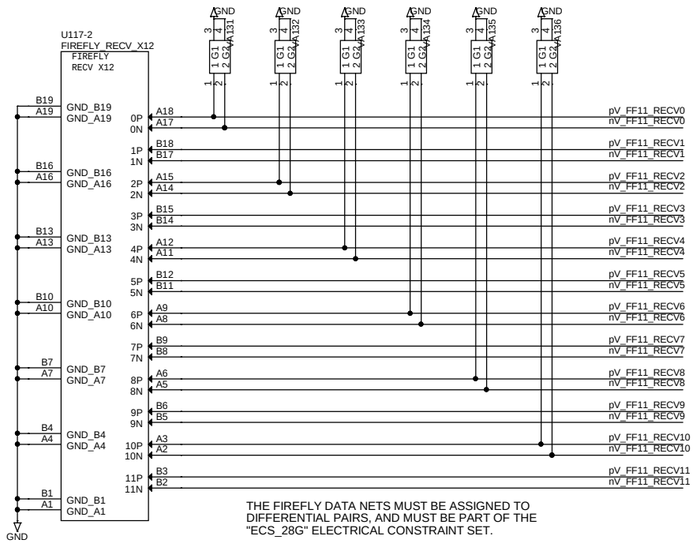
THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

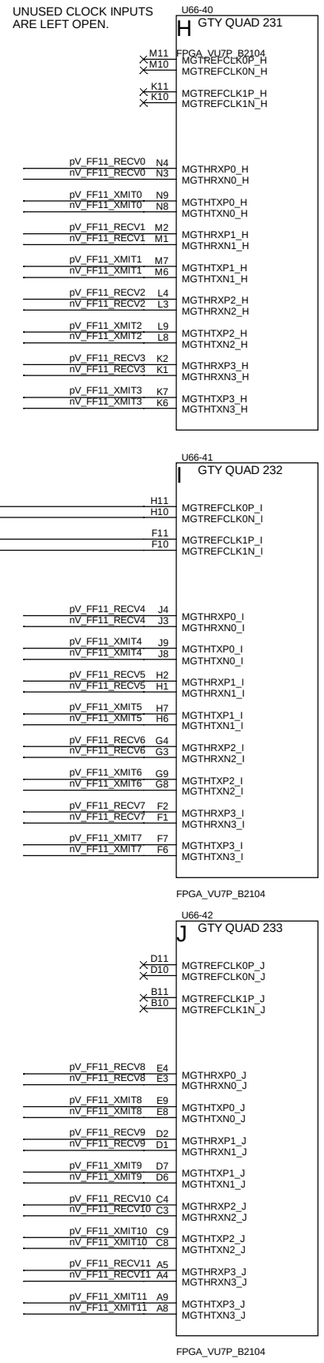



THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.




THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.




| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.08: VU7P QUADS HIJ FIREFLY X12 #11 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 67 of 74 | |

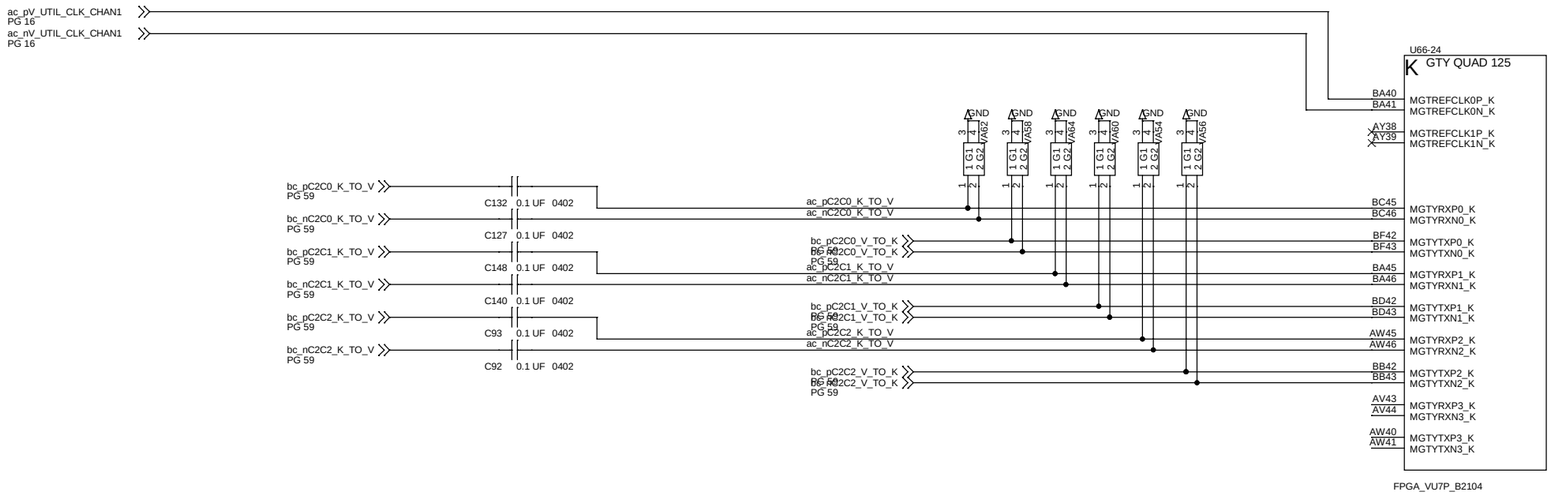
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS UNUSED, SINCE THE UTILITY FUNCTIONS ARE INDEPENDENT OF THE LHC CLOCK.

THE UTILITY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

UNUSED CLOCK INPUTS ARE LEFT OPEN.

## QUAD "K" IS CLOCKED DIRECTLY




THE "C2Cn_V_TO_K" AND "C2Cn_K_TO_V" SIGNALS ARE ROUTED DIRECTLY ON THE PCB. IF ADDITIONAL CHANNELS ARE NEEDED BETWEEN THE TWO FPGAS, USER A FIREFLY LINK.

THE DIRECT SIGNALS ARE AC-COUPLED. SUBSTITUTE A ZERO-OHM RESISTOR IN PLACE OF THE COUPLING CAPACITOR FOR DC-COUPLING.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.09: VU7P QUAD K CHIP TO CHIP

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 68 of 74

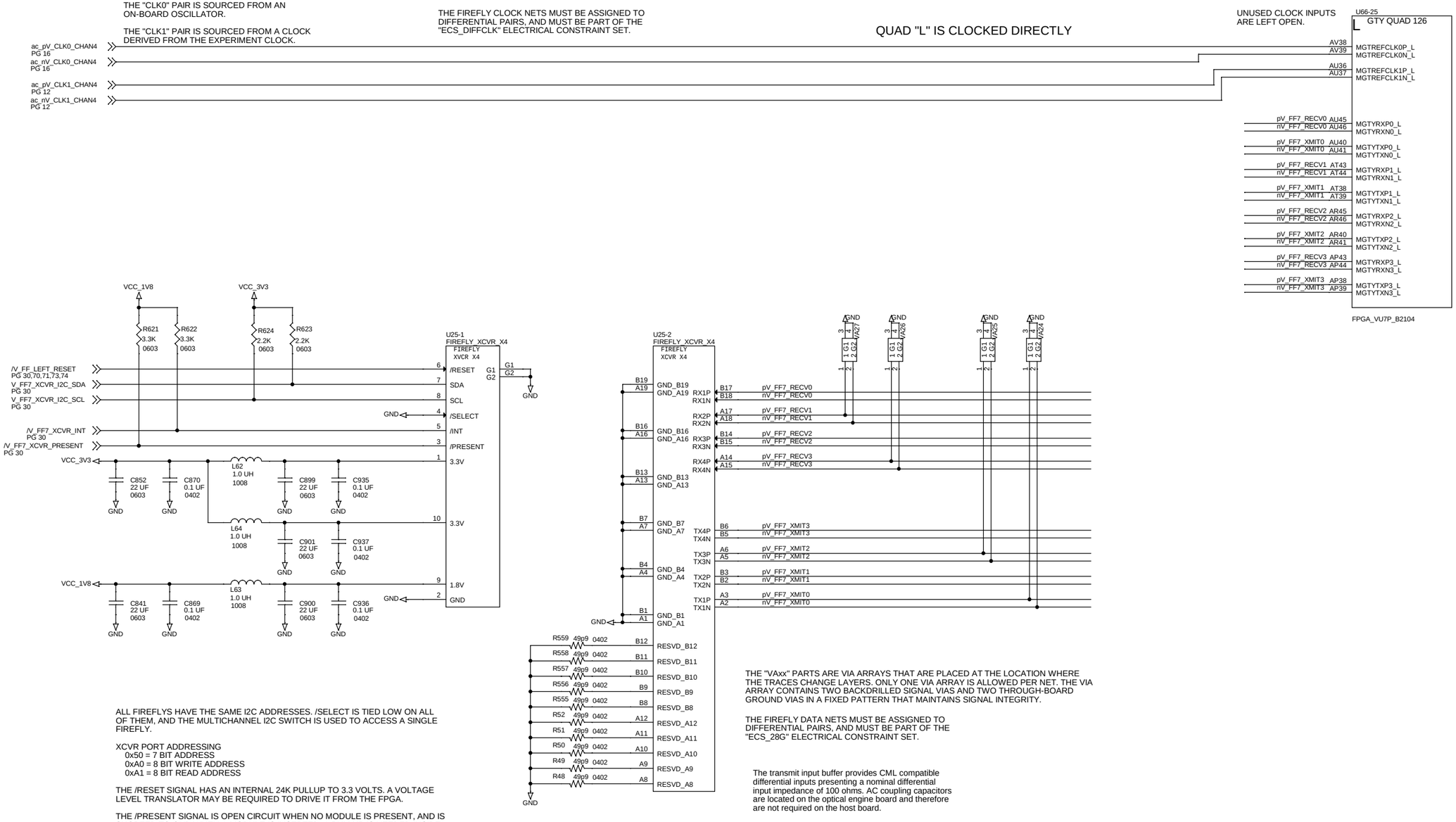
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "L" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.










ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

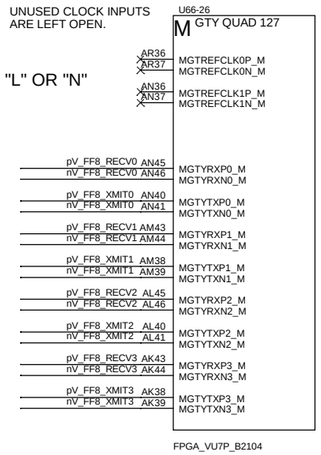
The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

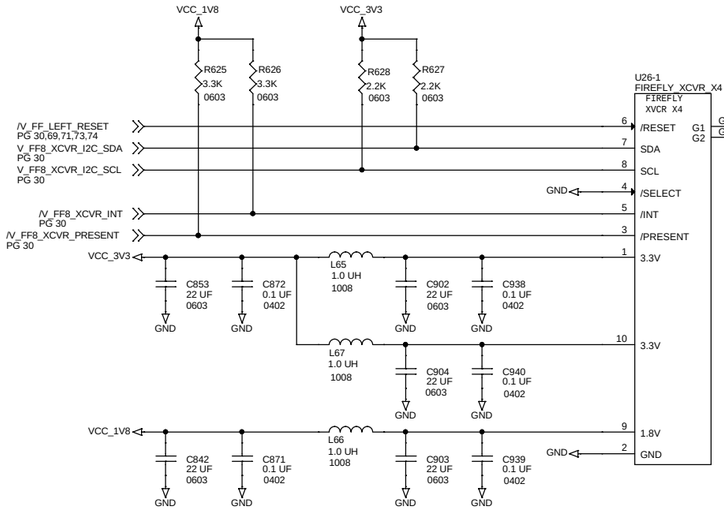
| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.10: VU7P QUAD L FIREFLY X4 #7 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 69 of 74 | |

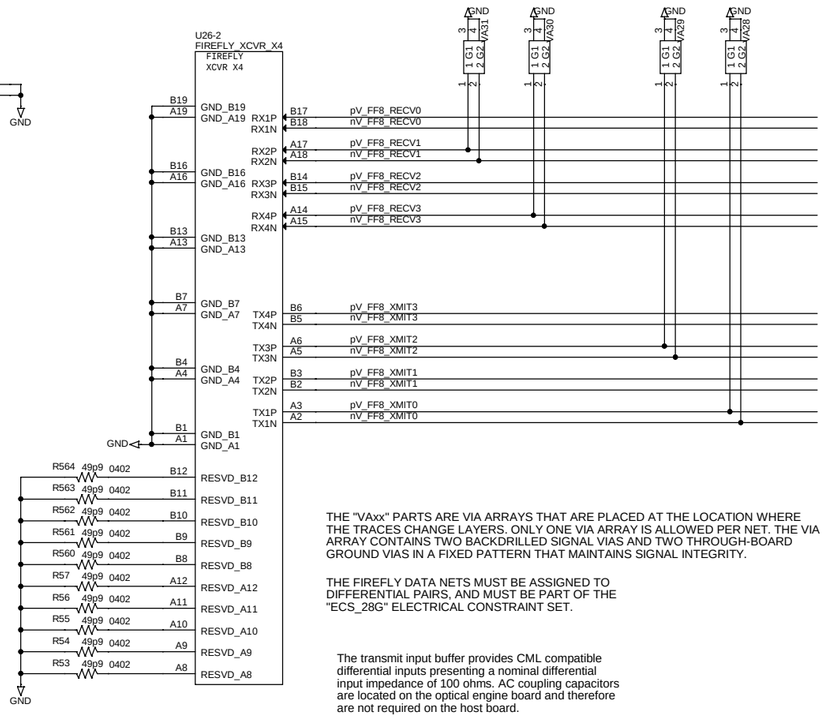
UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "M" IS CLOCKED FROM EITHER QUAD "L" OR "N"




FPGA_VU7P_B2104




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
0x50 = 7 BIT ADDRESS
0xA0 = 8 BIT WRITE ADDRESS
0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.11: VU7P QUAD M FIREFLY X4 #8 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 70 of 74 | |

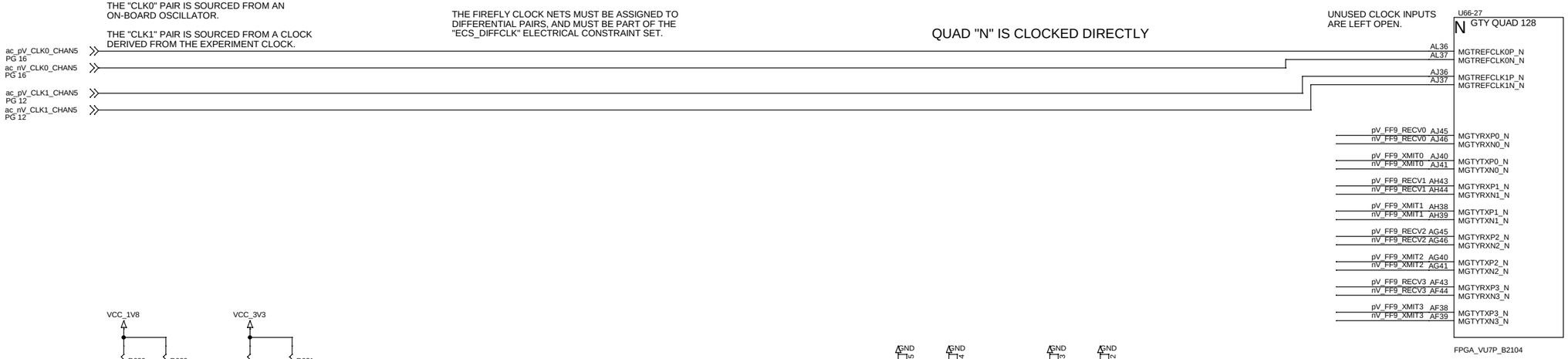
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

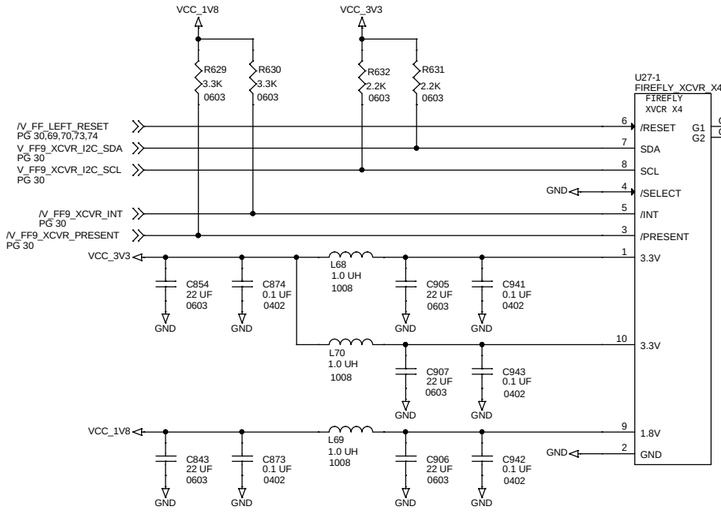
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

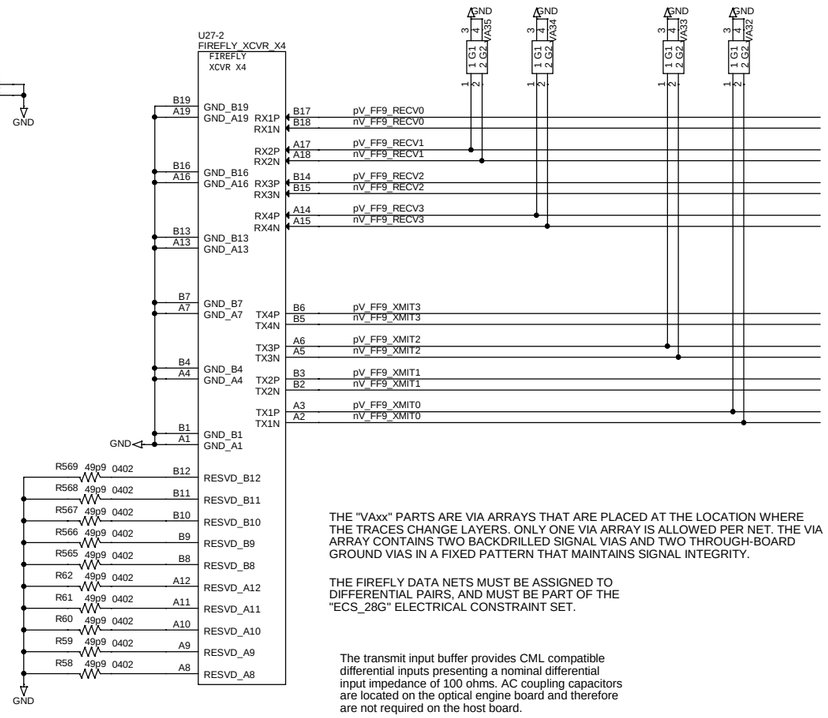
THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

## QUAD "N" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.




ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

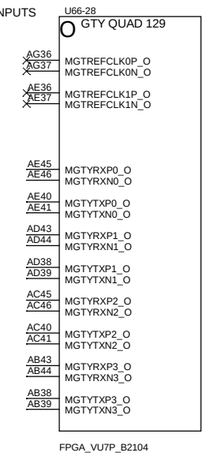
The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.12: VU7P QUAD N FIREFLY X4 #9 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 71 of 74 | |

UNUSED CLOCK INPUTS
ARE LEFT OPEN.

QUAD "O" IS UNUSED




ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.13: VU7P QUAD O UNUSED

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 72 of 74

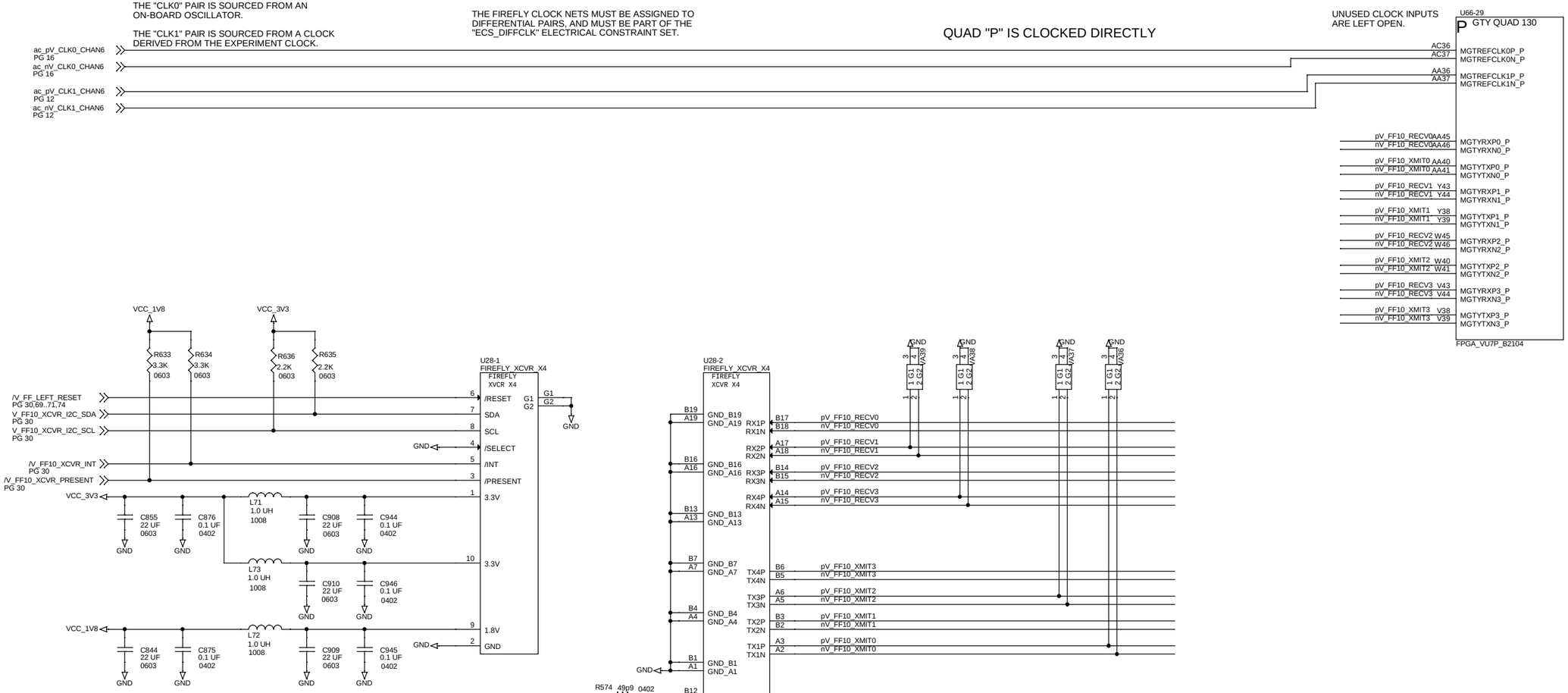
THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

QUAD "P" IS CLOCKED DIRECTLY

UNUSED CLOCK INPUTS ARE LEFT OPEN.










ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XCVR PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. A VOLTAGE LEVEL TRANSLATOR MAY BE REQUIRED TO DRIVE IT FROM THE FPGA.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED INSIDE THE FPGA.

THE /INT SIGNAL IS OPEN-COLLECTOR. THE PULLUP IS TIED TO THE SAME LEVEL AS THE FPGA BANK POWER.

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.

THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

HANDLING THE RESERVED PINS, ACCORDING TO SAMTEC:
If there is not space for 50 ohm resistors on every lane, it is better to leave those lanes open.
Tying all lanes together to a single resistor will create a current loop that can worsen crosstalk.

| | | |
|---|---|---|
| ATCA FPGA BOARD, KU15P AND VU7P, MK1 | | |
| Title: 8.14: VU7P QUAD P FIREFLY X4 #10 | | |
| Size | Document Number: 6089-103 | Rev: A |
| Date: Tuesday, February 26, 2019 | Sheet 73 of 74 | |

THE "CLK0" PAIR IS SOURCED FROM AN ON-BOARD OSCILLATOR.

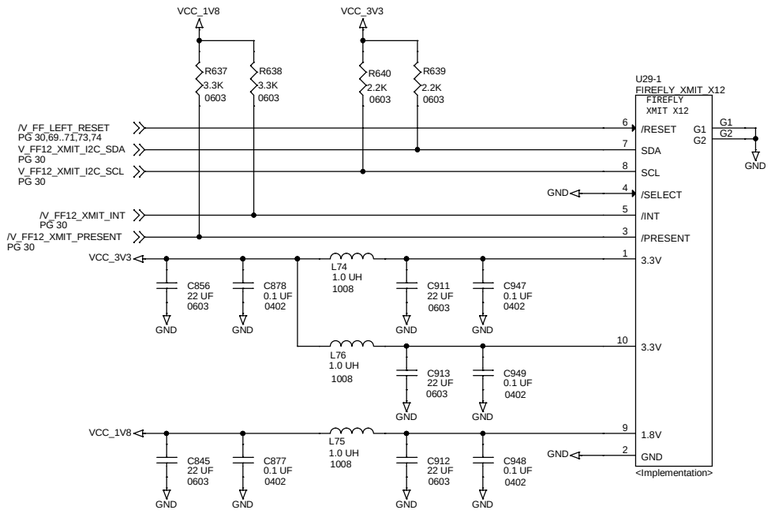
THE "CLK1" PAIR IS SOURCED FROM A CLOCK DERIVED FROM THE EXPERIMENT CLOCK.

THE FIREFLY CLOCK NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_DIFFCLK" ELECTRICAL CONSTRAINT SET.

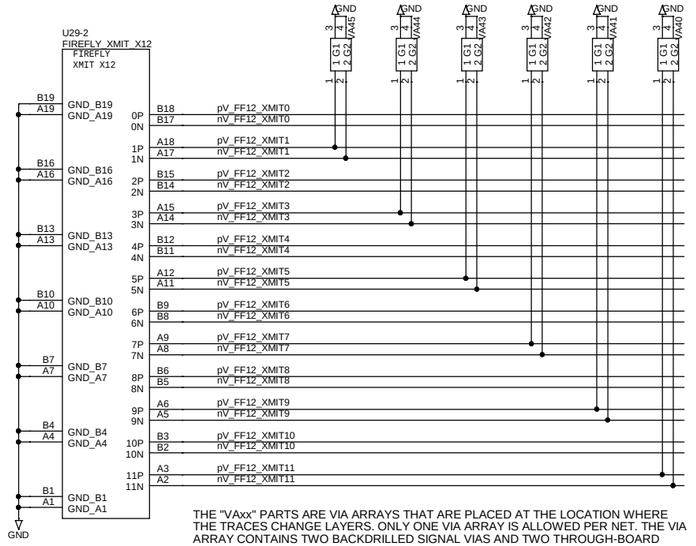
QUADS "Q" AND "S" ARE CLOCKED FROM QUAD "R"

UNUSED CLOCK INPUTS ARE LEFT OPEN.

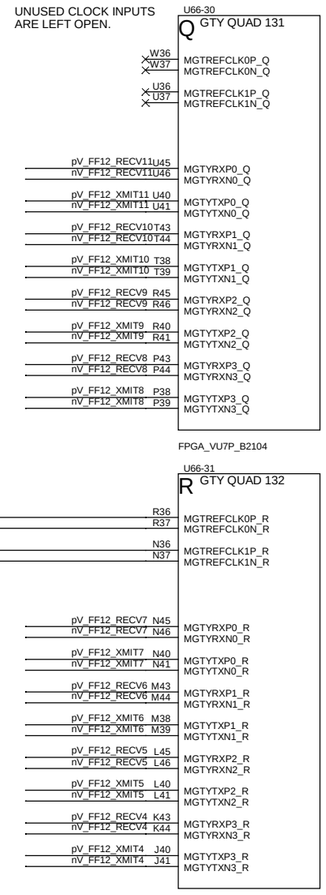
ac_pV_CLK0_CHAN7 PG 16
ac_nV_CLK0_CHAN7 PG 16
ac_pV_CLK1_CHAN7 PG 12
ac_nV_CLK1_CHAN7 PG 12




ON THE "X12" FIREFLY DEVICES AT 14G, PIN 9 IS RESERVED. ON THE "X4" FIREFLY DEVICES AT 28G, PIN 9 IS A 1.8 VOLT POWER PIN. THIS DESIGN PROVIDES FILTERING FOR PIN 9. IF IT CAUSES PROBLEMS ON THE "X12" 14G DEVICES, THE PARTS CAN BE OMITTED FROM THE BUILD.

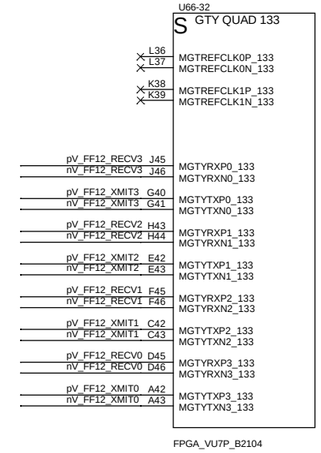


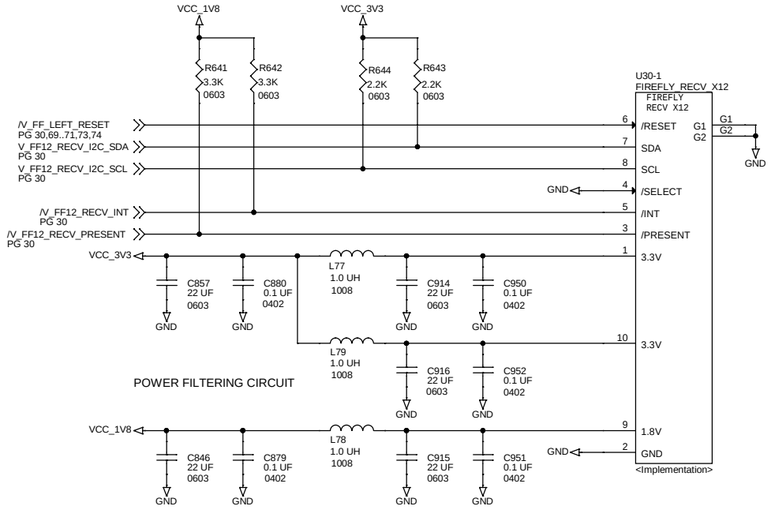

THE "VAxx" PARTS ARE VIA ARRAYS THAT ARE PLACED AT THE LOCATION WHERE THE TRACES CHANGE LAYERS. ONLY ONE VIA ARRAY IS ALLOWED PER NET. THE VIA ARRAY CONTAINS TWO BACKDRILLED SIGNAL VIAS AND TWO THROUGH-BOARD GROUND VIAS IN A FIXED PATTERN THAT MAINTAINS SIGNAL INTEGRITY.



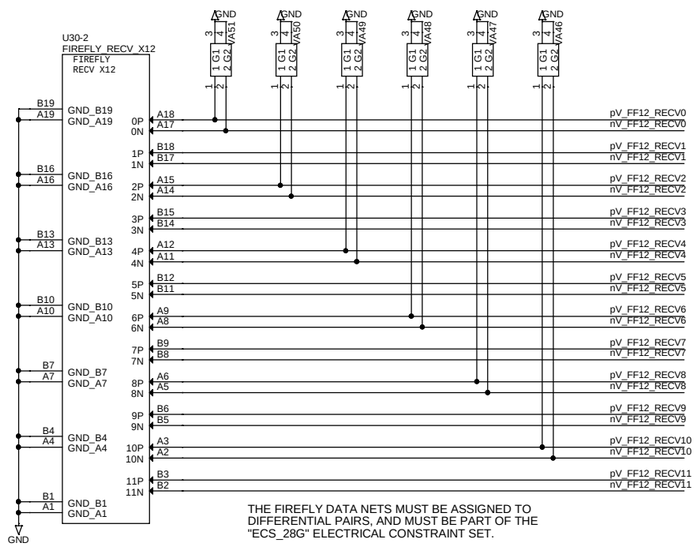







POWER FILTERING CIRCUIT




THE FIREFLY DATA NETS MUST BE ASSIGNED TO DIFFERENTIAL PAIRS, AND MUST BE PART OF THE "ECS_28G" ELECTRICAL CONSTRAINT SET.

The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

ALL FIREFLYS HAVE THE SAME I2C ADDRESSES. /SELECT IS TIED LOW ON ALL OF THEM, AND THE MULTICHANNEL I2C SWITCH IS USED TO ACCESS A SINGLE FIREFLY.

XMIT PORT ADDRESSING
- 0x50 = 7 BIT ADDRESS
- 0xA0 = 8 BIT WRITE ADDRESS
- 0xA1 = 8 BIT READ ADDRESS

RECV PORT ADDRESSING
- 0x54 = 7 BIT ADDRESS
- 0xA8 = 8 BIT WRITE ADDRESS
- 0xA9 = 8 BIT READ ADDRESS

THE /RESET SIGNAL HAS AN INTERNAL 24K PULLUP TO 3.3 VOLTS. ALL FIREFLY MODULES ON THE SAME SIDE OF THE SAME FPGA SHARE A COMMON RESET.

THE /PRESENT SIGNAL IS OPEN CIRCUIT WHEN NO MODULE IS PRESENT, AND IS SHORTED TO GND WHEN A MODULE IS INSERTED. A PULLUP IS NEEDED.

THE /INT SIGNAL IS OPEN-COLLECTOR. A PULLUP IS NEEDED.

ATCA FPGA BOARD, KU15P AND VU7P, MK1

Title: 8.15: VU7P QUADS QRS FIREFLY X12 #12

Size | Document Number: 6089-103 | Rev: A

Date: Tuesday, February 26, 2019 | Sheet 74 of 74