6089-103

CMS APOLLO COMMAND MODULE W/ VU7P AND KU15P

HARDWARE MANUAL

Contents

[Introduction 2](#_Toc6320028)

[To Do: 2](#_Toc6320029)

[Revision History: 3](#_Toc6320030)

[Version 1.1.1 3](#_Toc6320031)

[Front Panel LEDs 4](#_Toc6320032)

[Front Panel Switches 5](#_Toc6320033)

[Front Panel Connectors 6](#_Toc6320034)

[On-Board Jumpers 7](#_Toc6320035)

[On-Board Switches 7](#_Toc6320036)

[uTCA CONNECTIONS 8](#_Toc6320037)

[RTM CONNECTIONS 9](#_Toc6320038)

# Introduction

This manual can be found in the Windows directory:

[\\samba\accuser\cesrdaq\hardware\CMS\_Trigger\](file:///\\samba\accuser\cesrdaq\hardware\CMS_Trigger\)6089-103\_ATCA\_mezz\Docs

under the file name:

6089-103\_Hardware\_Manual\_1-1-1.docx

This manual will be updated routinely. Old versions will be saved in the same area.

# To Do:

1.

# Revision History:

## Version 1.1.1

1. Initial version

# Front Panel LEDs

There are 7 LEDs on the front panel. Starting at the top of the board near the JTAG connector, the LED functions are:

1) K DONE (GREEN) – The KU15P FPGA has successfully loaded a configuration file, either from the on-board EEPROM or by way of the JTAG chain. This LED is driven by the DONE\_0 pin on the KU15P. (SH 5.04)

2) K RGB (RGB) – This is an uncommitted LED that is driven by three signal lines from the KU15P. The firmware design determines the meaning of the display. (SH 2.11)

3) PWR OK (GREEN) – This LED is driven by the BLADE\_POWER\_OK signal from the TM4C controller. It will be activated when the TM4C has finished turning on all FPGA power supplies and they are all good. Since this is a GPIO pin on the TM4C, the programmer can use flashing to indicate a problem. (SH 2.11)

4) TM4C ACT (GREEN) – This LED is driven by the TM4C\_ACTIVE signal. It will be asserted when both the 3.3v and 1.8v management supplies are good, the BLADE\_POWER\_EN signal from the service blade is high, and the TM4C RESET switch is not activated. (SH 2.11)

5) TM4C RGB (RGB) – This is an uncommitted LED that is driven by three signal lines from the TM4C. The program determines the meaning of the display. (SH 2.11)

6) V DONE (GREEN) – The VU7P FPGA has successfully loaded a configuration file, either from the on-board EEPROM or by way of the JTAG chain. This LED is driven by the DONE\_0 pin on the VU7P. (SH 5.04)

7) V RGB (RGB) – This is an uncommitted LED that is driven by three signal lines from the VU7P. The firmware design determines the meaning of the display. (SH 2.11)

# Front Panel Switches

There are 3 switches on the front panel. Starting at the top of the board near the JTAG connector, the switch functions are:

1) K PROG – The KU15P FPGA will try to reload a configuration file from the on-board EEPROM. This switch is not needed when the reload is commanded by the TM4C, nor when the FPGA is being configured by way of the JTAG chain (SH 5.04)

2) TM4C RESET – The TM4C will go through a power-up reset sequence. All switched power supplies will first be disabled before being re-enabled in the proper sequence.

3) V PROG – The VU7P FPGA will try to reload a configuration file from the on-board EEPROM. This switch is not needed when the reload is commanded by the TM4C, nor when the FPGA is being configured by way of the JTAG chain (SH 6.04)

# Front Panel Connectors

There are 9 connectors on the front panel. Starting at the top of the board near the JTAG connector, the connector functions are:

1) JTAG (SH 2.04):

2) TM4C I2C (SH 4.01):

3) K OPTICS I2C (SH 4.01):

4) FPGA I2C (SH 4.01):

5) PWR I2C (SH 4.01):

6) AMC13 CLK IN (SH 2.08):

7) TM4C UART (SH 2.05):

8) CLOCK I2C (SH 4.01):

9) V OPTICS I2C (SH 4.01):

# KU15P Fiber Connectors



GTY Quad R (133)

FF x4 25 Gbps (U24)

GTY Quad P (131)

FF x4 25 Gbps (U22)

GTY Quad Q (132)

FF x4 25 Gbps (U23)

GTY Quads L/M/N (127/128/129)

FF X12 14 Gbps (U20/U21)

GTH Quads B/C/D (225/226/227)

FF X12 14 Gbps (U104/U105)

GTH Quads H/I/J (231/232/233)

FF X12 14 Gbps (U108/U109)

GTH Quads E/F/G (228/229/230)

FF X12 14 Gbps (U106/U107)

Unused

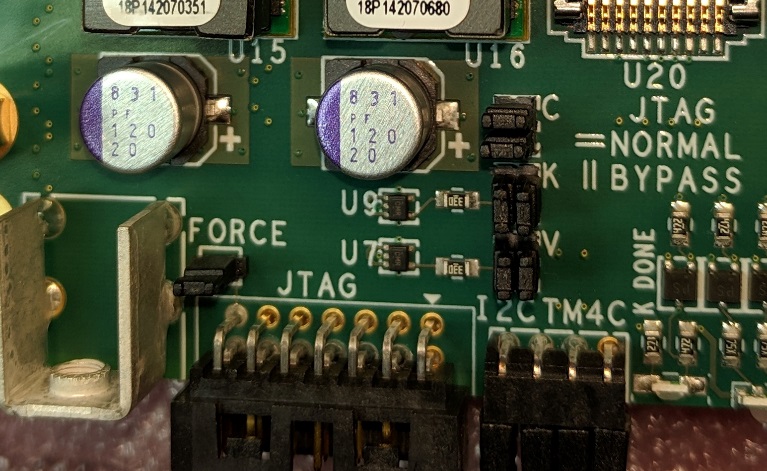
Unused

# On-Board JTAG Jumpers

There are 4 on-board jumper sites associated with the JTAG chain. They are all located near the front panel, adjacent to the JTAG connector.

1) JTAG NORMAL / BYPASS (SH 2.04): Three pairs of jumpers configure the JTAG chain. The paired jumpers cause the chain to either pass through the associated device (NORMAL) or to jump around the device (BYPASS). Set a pair of jumpers parallel to the front panel to include a device, and perpendicular to bypass a device. Marks on the silkscreen indicate the alignment for NORMAL or BYPASS. The jumpers are labeled V = VU7P, K = KU15P, C = TM4C controller. If a device is not installed, it must be bypassed. The illustration below shows the TM4C as the only device in the chain, with both FPGAs bypassed.

2) JTAG FORCE FRONT PANEL (SH 2.04): The JTAG chain can be driven either from the service module or from the front panel connector. Normally, if no cable is plugged into the front, the chain defaults to being driven by the service module. Plugging in a cable that has pin-13 connected to GND will switch the chain to use signals from the cable. However, if the particular cable does not automatically connect pin-13 to GND, a jumper can be used to force the use of the front panel connector.



J15 - TM4C Normal

J13 - VU7P Bypassed

J14 - KU15P Bypassed

Front panel JTAG forced

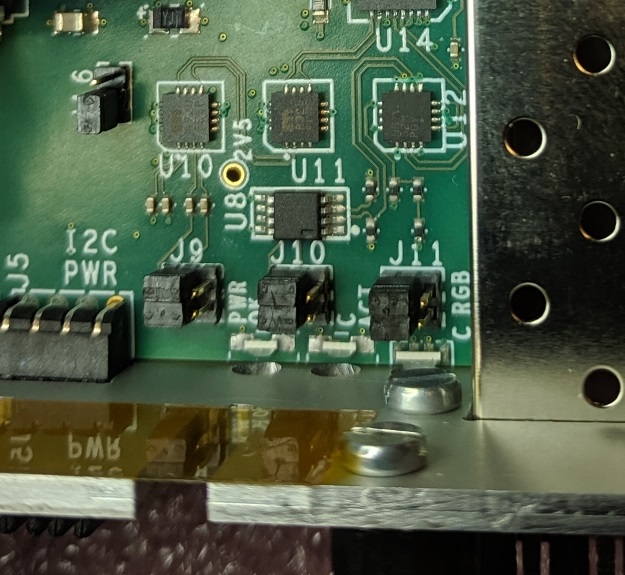
# 

# On-Board LEGACY TTC Jumpers

There are 3 on-board jumper sites associated with the legacy TTC signals. They are all located near the front panel, adjacent to the AMC13 CLK IN SFP connector.

1) CONNECT KU15P or VU7P (SH 2.08): Three pairs of jumpers configure the TTC signals to connect to either the KU15P or the VU7P. Each signal uses 3 pins. The center pin is the signal from or to the legacy TTC electronics. The pin closest to the KU15P connect to the KU15P. The pin closest to the VU7P connects to the VU7P.

Legacy TTC signals can only connect to one FPGA. If both FPGAs need the signals, the FPGA firmware needs to route the signals between the two FPGAs using some of the spare traces (SH 5.07 and 6.07).



J10 – TTC data to KU15P

J11 – TTS clk/data from KU15P

J9 – TTC clock to KU15P

# On-Board EEPROM WRITE-PROTECT Jumper

There is one on-board jumper that controls the WRITE-PROTECT input of the EEPROM. It is near the front panel, adjacent to the AMC13 CLK IN SFP connector.

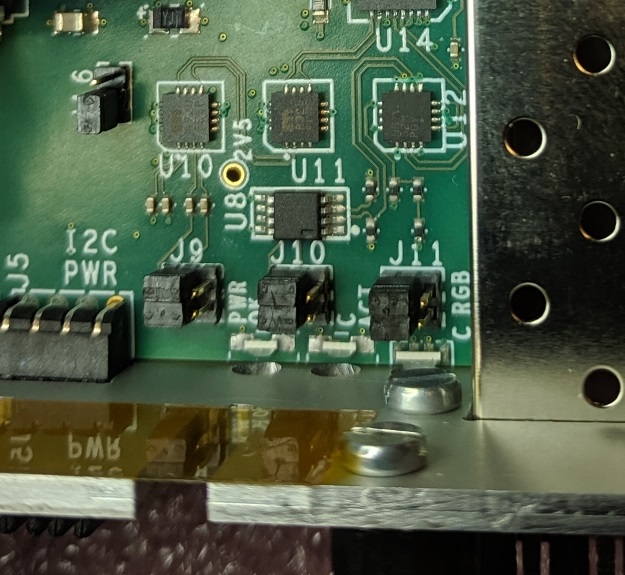
1) EEPROM WRITE PROTECT (SH 4.01): This jumper configures the hardware write-protect pin. Pin 1 is closest to the front panel.

a) If no jumper is in place, the hardware write protection is always enabled.

b) If the jumper connects pins 1 and 2, the hardware write protection is always disabled.

c) If the jumper connects pins 2 and 3, the hardware protection is controlled by a GPIO pin on the TM4C controller.

Refer to the data sheet for details about connecting an external high voltage to reset the software write protect fuse.



J16 – EEPROM always writable

# On-Board Switches

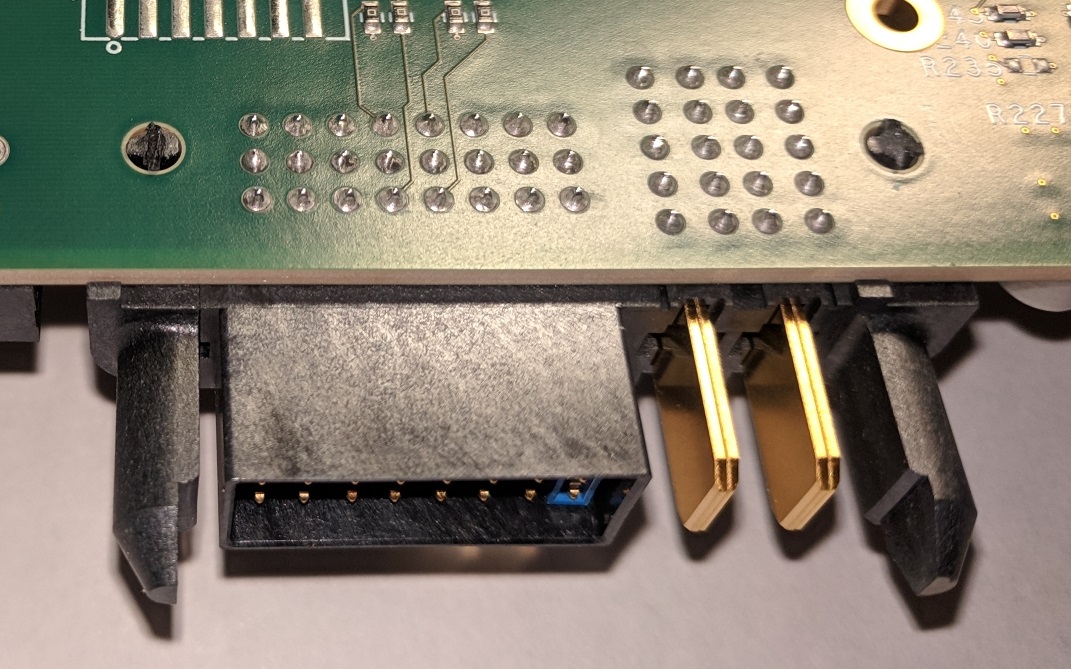
There are 2 on-board DIP switches.

1) JTAG (SH 2.04):

# New Board Setup

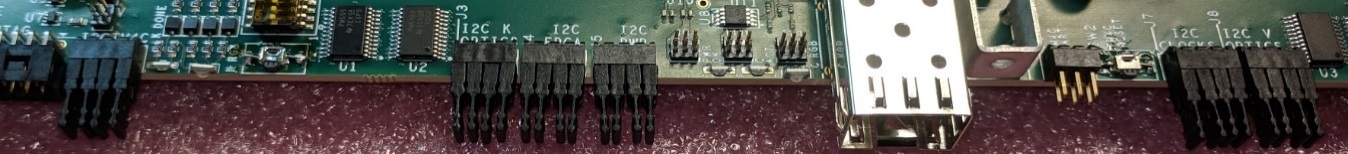
These steps need to be followed for all new boards.

1) Cut the protruding guideposts on side 2 from the P1 connector.



Cut guideposts

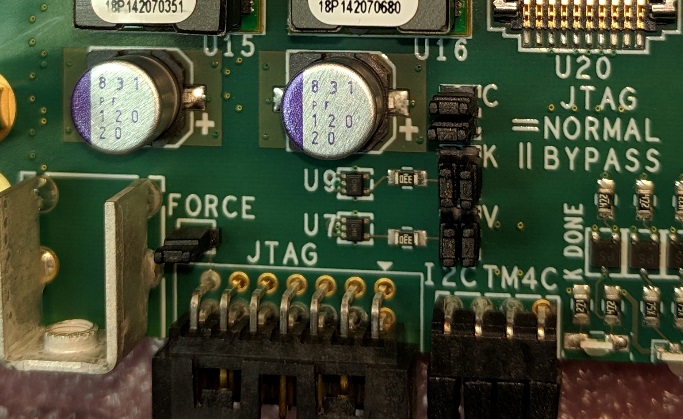
2) Install 4 2-mm jumpers on each of the 6 front panel I2C test connectors.



3) Install 3 sets of 2 50-mil jumpers to configure the JTAG chain. The TM4C should be set for NORMAL, and the KU15P and VU7P should be set for BYPASS. The silkscreen legend indicates how NORMAL has the jumpers parallel to the front panel, while BYPASS has them perpendicular to the front panel.

Set of 4 jumpers

Also install a 50-mil jumper on the pins labeled FORCE. This will force the JTAG chain to use only the front panel connector. Eventually, specially wired connectors will be used and the FORCE jumper will be removed. The special connector will connect pin #13 to GND.



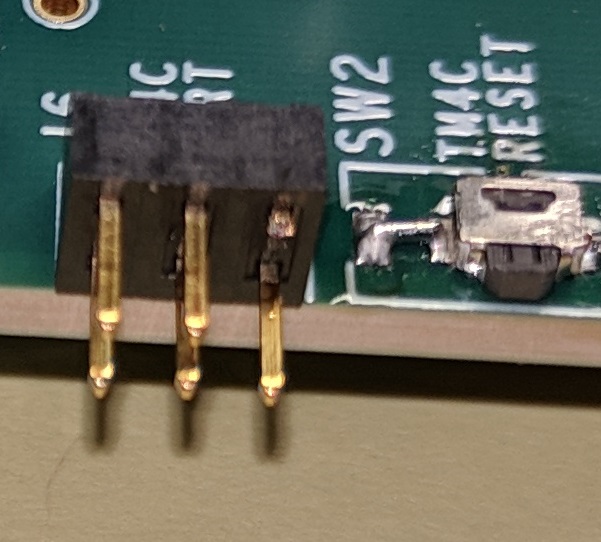
VU7P BYPASS

KU15P BYPASS

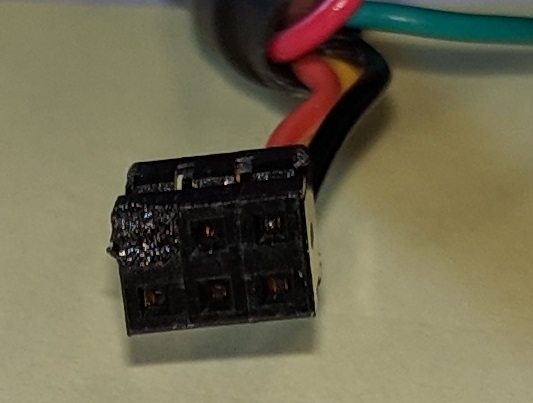
TM4C NORMAL

FORCE FRONT PANEL JTAG

4) Clip pin #6 from the TM4C UART connector on the front edge of the board. This will “key” the header so that the mating connector cannot be inserted in the wrong orientation.



Cut pin #6 (upper right)



Pin #6 is obstructed

# 

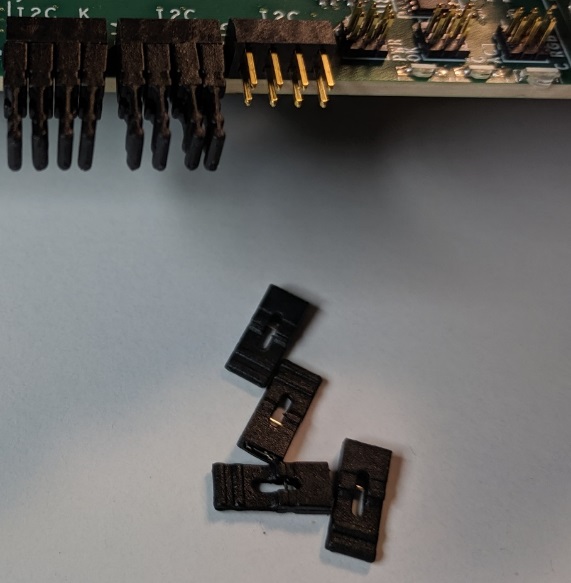
# DRIVING I2C SLAVES FROM THE AARDVARK HOST ADAPTER

Any of the six I2C chains can be driven from an external host adapter. The host adapter is connected by removing the 4 jumpers from the desired I2C chain and attaching the Aardvark I2C/SPI adapter by way of a custom cable, then running the TotalPhase SerialControl program.

The manual is at:

https://www.totalphase.com/support/articles/200468316-Aardvark-I2C-SPI-Host-Adapter-User-Manual

1) Remove the jumpers from the desired I2C slave bus. In this case, it is the I2C bus for the DC-DC converters.



2) Attach the adapter cable that is labeled “BOARD IS SLAVE”. The wires connect to the top row of pins, with the yellow wire to the left and the white wire to the right. The 8-pin front panel connector is not keyed. The 10-pin connector to the adapter is keyed.



3) The signals are:

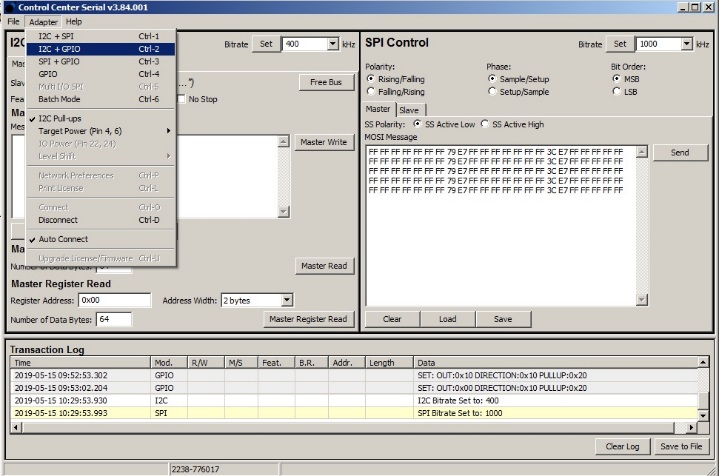
Yellow = SCL (I2C Clock)

Blue = SDA (I2C Data)

Red = RESET

White = GND

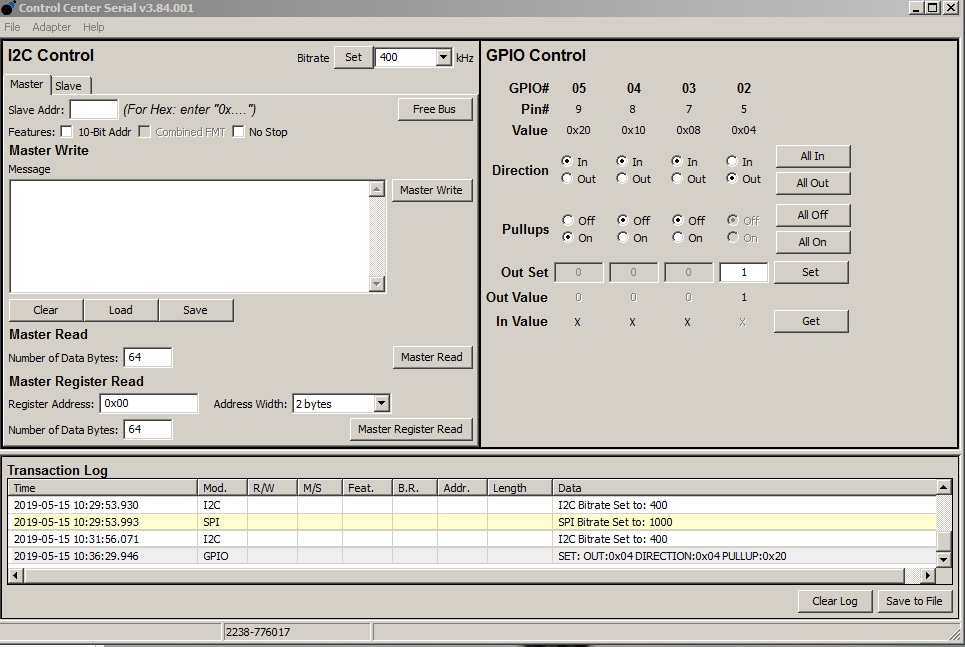
4) Start the TotalPhase “Control Center Serial” program. From the menu bar, select “Adapter” Then scroll down to “I2C + GPIO”.



5) The right side of the screen will change from “SPI Control” to “GPIO Control”. GPIO #2 drives the active-low “reset” signal. It needs to be high for normal operation. Select the direction for GPIO #2 to be “Out”, set the “Out Set” value to be “1’”, and press the “Set” button.

Anytime you want to perform a reset operation, set the “Out Set” value to “0” and press the “Set” button. Then set the “Out Set” value to be “1’”, and press the “Set” button again.

GPIO #2 to “Out”



Press to activate

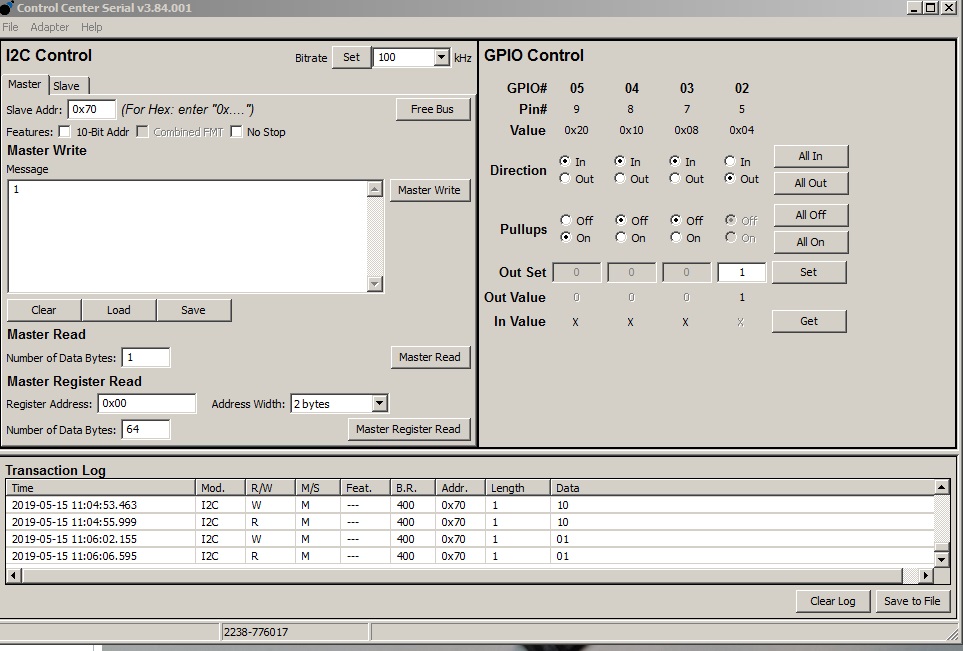
“Out” to 1

6) To configure a TCA9548A bus switch, set the “Bitrate” to “100 kHz”, set the “Slave Addr” to 0x70, and the “Master Write” message to the hex data representing the switch bits to set. Press the “Master Write” button. Read it back by setting the “Master Read” number of data bytes to 1 and pressing the “Master Read” button. The results show in the “Transaction Log” window.

Bitrate to 100 kHz

Write message to 1

Slave Addr to 0x70



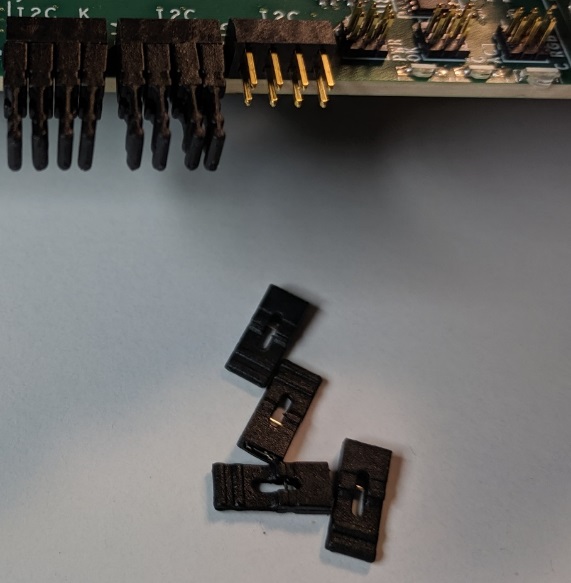
Result of read

Read bytes to 1

# OBSERVING I2C MASTERS WITH THE AARDVARK HOST ADAPTER

Any of the six I2C chains can be substituted with the external host adapter. The host adapter is connected by removing the 4 jumpers from the desired I2C chain and attaching the Aardvark I2C/SPI adapter by way of a custom cable, then running the TotalPhase SerialControl program.

1) Remove the jumpers from the desired I2C slave bus. In this case, it is the I2C bus for the DC-DC converters.



2) Attach the adapter cable that is labeled “BOARD IS MASTER”. The wires connect to the bottom row of pins, with the yellow wire to the left and the white wire to the right. The 8-pin front panel connector is not keyed. The 10-pin connector to the adapter is keyed.



3) The signals are:

Yellow = SCL (I2C Clock)

Blue = SDA (I2C Data)

Red = RESET (omitted initially until all TM4C I2C reset pins are open drain)

White = GND