RC Snubber & RCD Clamp Circuits Design

Contents

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1. Overview

In this work, it is aimed to design RC snubber and RCD clamp circuits. In many topologies like flyback, they require either a snubber or a clamp circuit to suppress ringing and spikes. Without any snubber/clamps, these spikes/rings could put excessive stress on the device. Otherwise, the device might be blown up. Therefore, some protections need to be implemented to protect the PCB/switching devices.

Spikes are usually generated because of leakages inductance

Ringing are usually ebcause of Ls & Cs resonating together.

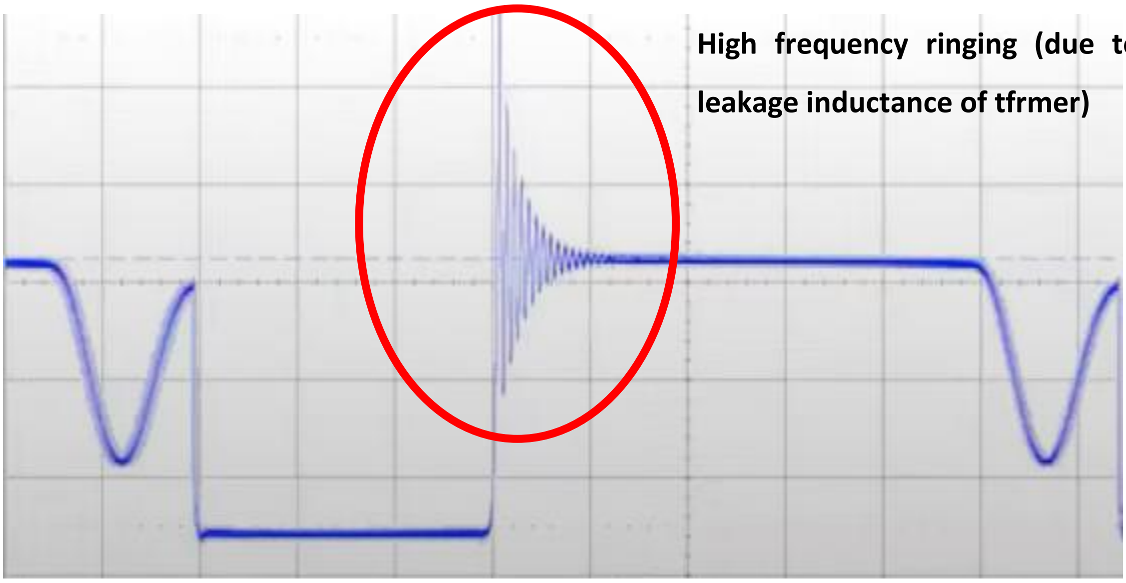


Figure 1. Example to spikes and ringing (without any snubbing or clamping circuit)

Flyback converters are notorious for having both ringing and a large leakage spikes.

2. Resonance in series and parallel circuits

2.1 Resonance in series RLC circuit

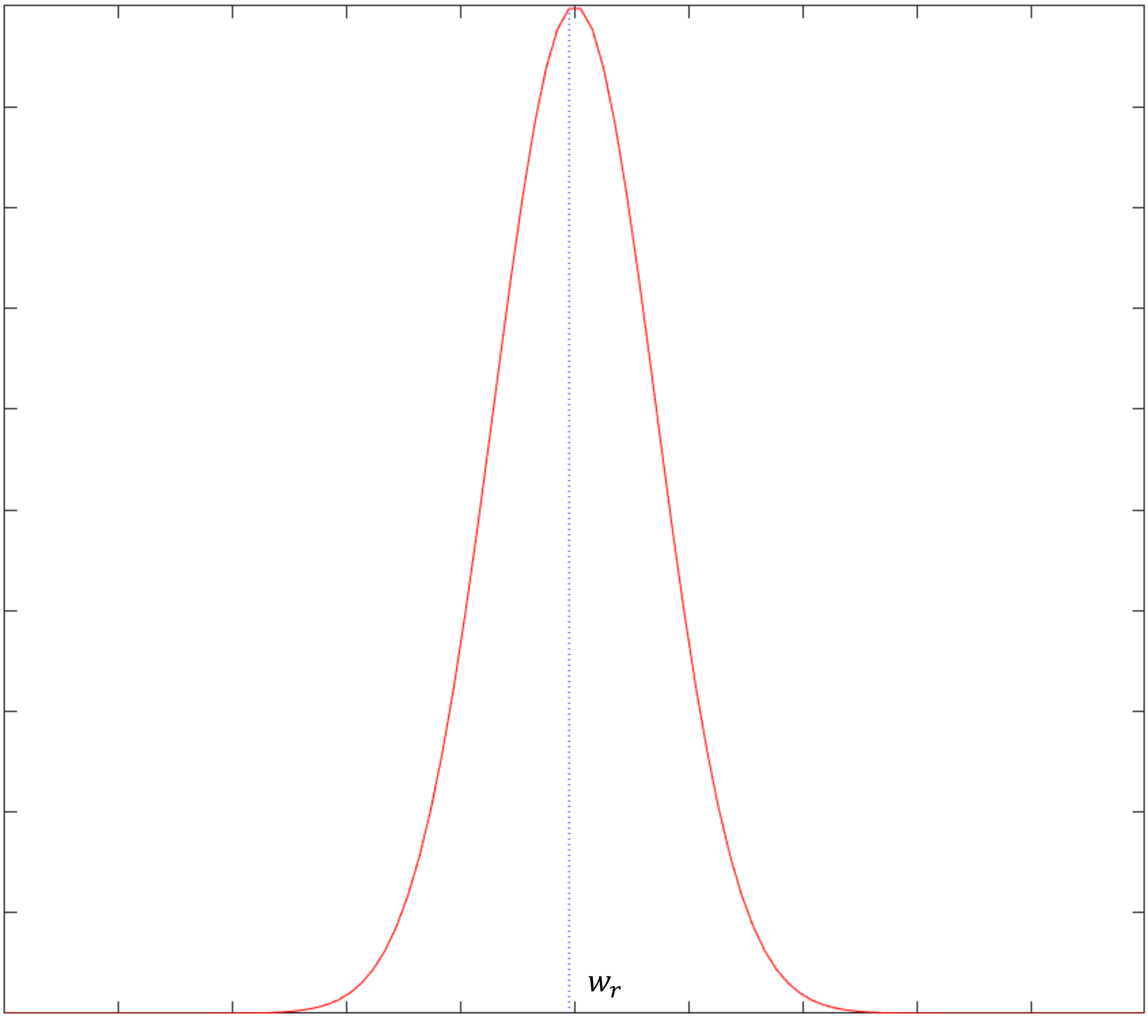


Figure 2. Resonance in circuit and resonant frequency Wr

If we analyze graphically this phenomena, it is shown as above. Neither lower nor higher frequency there is no current flowing through the circuit. As we move toward resonant frequency, there is increase in current and maximum current flows at resonant frequency. As we move away from resonant frequency, current will go down.

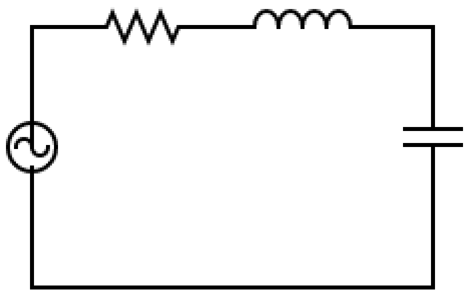


Figure 3. Series RLC circuit

Reactance of inductor is: $x_L = wL$

Reactance of capacitor is: $x_C = \frac{1}{wC}$

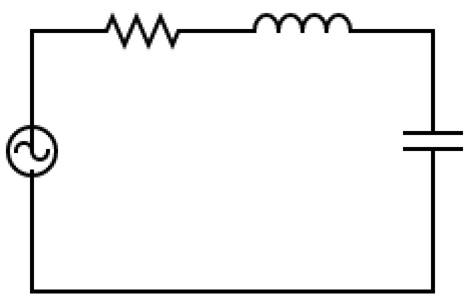
- At lower frequencies (w approaches zero) $w = 0 \rightarrow \; x_C = \infty, x_L = 0$

Capacitor acts as a open-circuit, so we will not find any current flowing

- At higher frequencies (w approaches infinity) $w = \infty \rightarrow \; x_C = 0, x_L = \infty$

Inductor acts as a open-circuit, so we will not find any current flowing

That is, at lower and higher frequencies, the current is flowing the circuit is minimum while at resonant frequency, the value of $x_L = x_C$. Hence, they will cancel each other, so impedance (Z) of the circuit is purely resistive.



$$I = \frac{V}{Z}$$

$$Z = R + x_C + x_L$$

$$Z = R + jwL + \frac{1}{jwC}$$

$$Z = R + jwL + \frac{-j}{wC}$$

$$Z = R + j\left[wL + \frac{-1}{wC}\right]$$

To get maximum amount of current, we need minimum impedance (Z)

$$I_{max} = \frac{V}{Z_{min}}$$

To get minimum impedance

$$Z = R + j\left[wL + \frac{-1}{wC}\right]$$

Imaginery part of impedance should be zero $\left[wL + \frac{-1}{wC}\right] = 0$

$$wL - \frac{1}{wC} = 0 \rightarrow wL = \frac{1}{wC}$$

$$Z_{min} = R$$

$$I_{max} = \frac{V}{Z_{min}} = \frac{V}{R}$$

$$wL = \frac{1}{wC} \rightarrow w^2 = \frac{1}{LC}$$

$$w = \sqrt{\frac{1}{LC}}$$

$$w_r = \sqrt{\frac{1}{LC}}$$

w_r is resonant frequency of the circuit.

$$w_r = 2\pi f_r$$

Or we can write in terms of frequency (f_r):

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

2.1.1 Quality Factor (Q)

Quality factor is defined as $2 \times \pi \times \frac{maximum\ energy\ stored\ in\ either\ cap.or\ ind.}{energy\ dissipated\ across\ the\ resistor}$

Quality factor defines the sharpness of the resonant curve.

$$Q = \frac{I^2 x_L}{I^2 R} = \frac{I^2 x_C}{I^2 R} = \frac{x_L}{R} = \frac{x_C}{R}$$

$$Q = \frac{wL}{R} = \frac{1}{wCR}$$

$$w_r = \sqrt{\frac{1}{LC}}$$

$$Q = \frac{1}{R} \cdot \sqrt{\frac{L}{C}}$$

Or we can write it in terms of bandwith ($B.W = \frac{R}{L}$)

$$Q = \frac{w_r L}{R} = \frac{w_r}{B.W}$$

2.2 Resonance in parallel RLC circuit

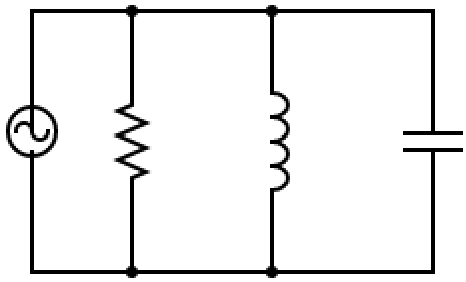


Figure 4. Parallel RLC circuit

As it is in series RLC cct;

Reactance of inductor is: $x_L = wL$

Reactance of capacitor is: $x_C = \frac{1}{wC}$

The point where $x_L = x_C$, the circuit will be in resonant condition. During the resonant, the impedance of the circuit will be purely resistive. That is, voltage & current will be in phase. Also at resonant condition in parallel RLC circuit, impedance is maximum and current is minimum unlike in series RLC circuit.

- At lower frequencies (w approaches zero) $w = 0 \rightarrow \ x_C = \infty, x_L = 0$
- At higher frequencies (w approaches infinity) $w = \infty \rightarrow \ x_C = 0, x_L = \infty$

$$I_{rms} = I_R + I_L + I_C$$

$$I_{rms} = \frac{V}{R} + \frac{V}{x_L} + \frac{V}{x_C}$$

$$I_{rms} = V\left[\frac{1}{R} + \frac{1}{x_L} + \frac{1}{x_C}\right]$$

$$I_{rms} = V\left[\frac{1}{R} + \frac{1}{jwL} + jwC\right]$$

$$I_{rms} = V\left[\frac{1}{R} + j\left[\frac{-1}{wL} + wC\right]\right]$$

$$Y\ (admittance) = \frac{1}{R} + j\left[\frac{-1}{wL} + wC\right]$$

$$I = V.Y$$

At resonant frequency in parallel RLC, the current that is flowing into the circuit is minimum. To get minimum current, Y should be minimum. To get minimum value of Y:

$$\frac{1}{wL} = wC$$

$$Y = \frac{1}{R}$$

$$Z = R$$

$$\frac{1}{wL} = wC$$

$$w^2 = \frac{1}{LC}$$

$$w_r = \frac{1}{\sqrt{LC}}$$

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

It is same with series RLC circuit.

At lower frequencies $x_L = 0$, the inductor become short circuit, the entire current flows through the inductor and the current lags the voltage.

At higher frequencies , $x_C = 0$, the capacitor become short circuit, the entire current flows through the capacitor and the current leads the voltage.

2.3 Quality Factor (Q)

$$Q = 2 \times \pi \times \frac{energy\ stored\ per\ cycle}{energy\ dissipated\ per\ cycle}$$

$$Q = w \times \frac{energy\ stored\ per\ cycle}{power\ dissipated} = \frac{1}{2}LI^2 = \frac{1}{2}CV^2$$

$$Q = w \times \frac{CV^2}{I^2R} = w \times \frac{CV^2}{\frac{V^2}{R}}$$

$$Q = \frac{R}{x_C} = \frac{R}{x_L}$$

$$Q = wCR = \frac{R}{wL}$$

3. RC Snubber Design

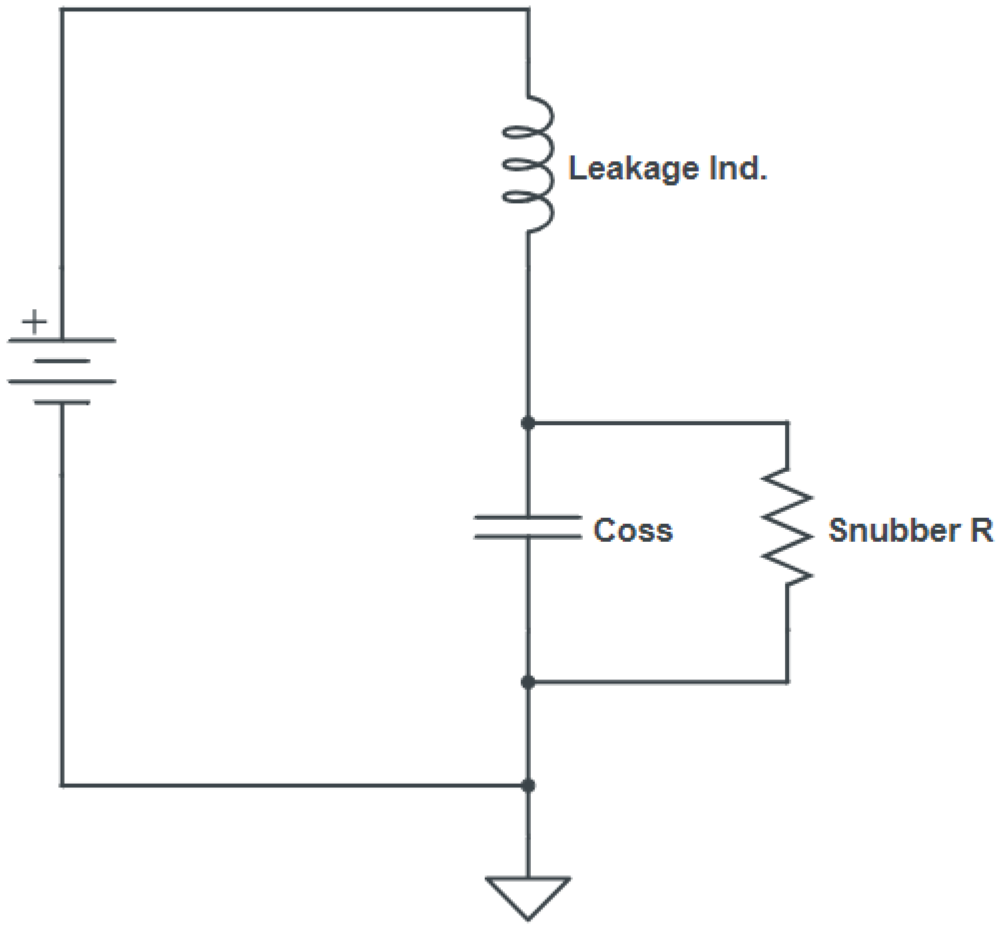


Figure 5. RC snubber design

Ignoring the snubber capacitor and the inductor resistance for the sake of analysis

$$H(s) = \frac{1}{LCs^2 + \frac{L}{R}s + 1}$$

Comparing this directly with the standard equation for a 2^{nd} order system

Where w_n = resonant frequency and Q is the quality factor (i.e. related to the our resonant bump & our spike

We have:

$$H(s) = \frac{1}{\frac{s^2}{{w_n}^2} + \frac{1}{Qw_n}s + 1}$$

$$w_n = \frac{1}{\sqrt{LC}}$$

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$Q = \frac{1}{2\zeta} = R\sqrt{\frac{C}{L}}$$

ζ = is the damping ratio (rarely used in PSU analysis and only included for completeness)

As we can see Q is related to damping, we would like to set Q to 1 to damp our system and reduce the spike. For Q = 1, we have

$$Q = R\sqrt{\frac{C}{L}}$$

$$1 = R\sqrt{\frac{C}{L}}$$

$$R = \sqrt{\frac{L}{C}}$$

We would like to calculate **R**

We know the leakage inductance L_{lkg} as we can measure it.

L_{lkg} is the total leakage inductance as seen on the primary side.

3.1 How to modeling transformer and finding leakage inductances

3.1.1 Finding magnetizing inductance

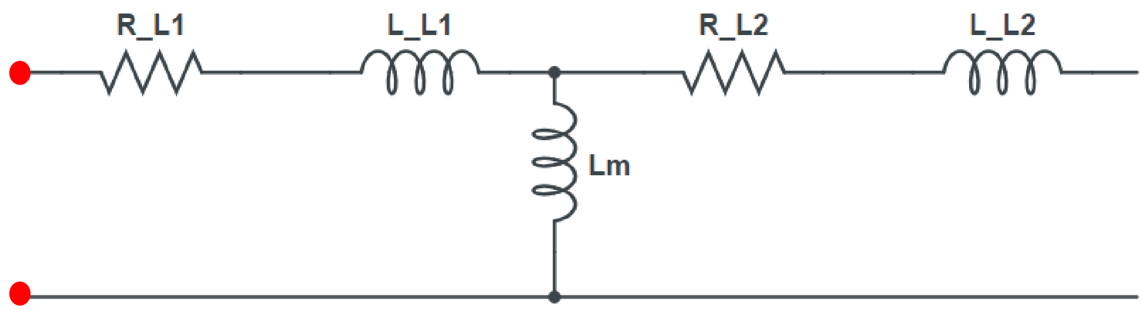


Figure 6. Transformer circuit modeling

$L_m = magnetizing\ inductance$

$L_{L1} = leakage\ inductance\ of\ primary\ side$

$L_{L2} = leakage\ inductance\ of\ primary\ side$

In the transformer, if we leave secondary side open circuit, no current will flow through that. Therefore, if we measure the total impedance from red dots as seen on the figure above because there is no current going through secondary side, therefore; simplified model will be like

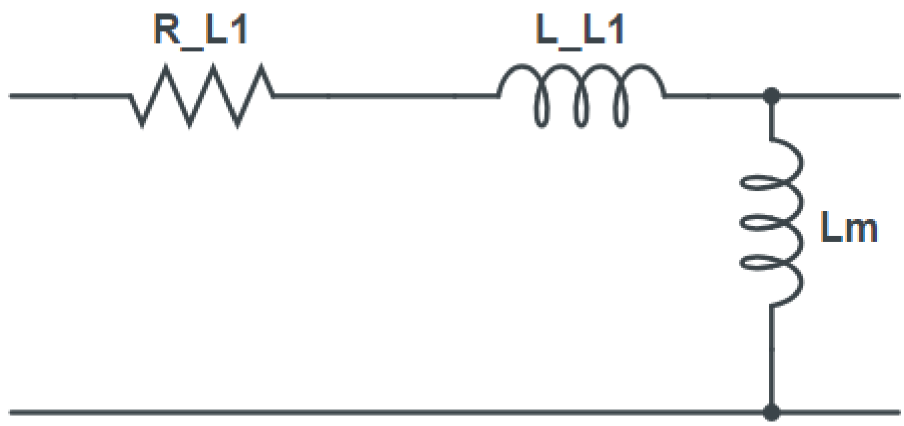


Figure 7. Transformer modeling with secondary side is open

We will notice that leakage and resistance of primary side is absolutely tiny as compared to impedance of magnetizing inductance. **L_m will be dominant part if we measure from primary while leaving the secondary side open.**

3.1.2 Finding turns ratio

If we want to work out the turn ratio measure from secondary side while leaving the primary side open and as we know from circuit theory

$$\frac{L_p}{L_s} = \frac{{N_p}^2}{{N_s}^2}$$

3.1.3 Finding leakage inductances (L_{L1} & L_{L2})

In order to find leakage inductances L_{L1} & L_{L2}, leave the secondary side shorted, as magnetizing inductance L_m is very large as compared to leakage inductances, therefore almost no current is going through that branch and majority of current flow through secondary side

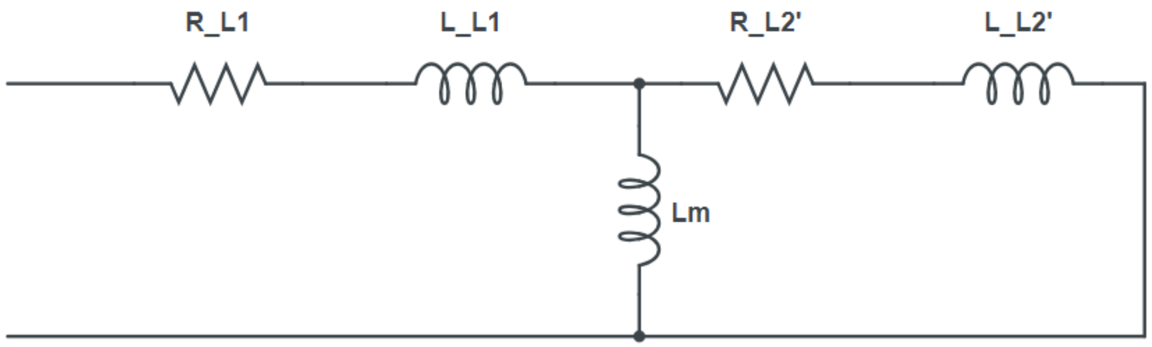


Figure 8. Transformer modeling with secondary side is shorted

$L_{L2}' = leakage\ of\ \boldsymbol{secondary\ referred\ to\ primary}\ side$

$R_{L2}' = resistance\ of\ secondary\ \boldsymbol{referred\ to\ primary\ side}$

As we know for a transformer referring secondary to primary

$V'_{sec} = V_{sec} \times N$

$I'_{sec} = \frac{I_{sec}}{N}$

$$Z'_{sec} = \frac{V'_{sec}}{I'_{sec}} = \frac{V_{sec} \times N}{\frac{I_{sec}}{N}} = \frac{V_{sec}}{I_{sec}} \times N^2$$

$$Z'_{sec} = Z_{sec} \times N^2$$

Where $N = \frac{N_1}{N_2}$

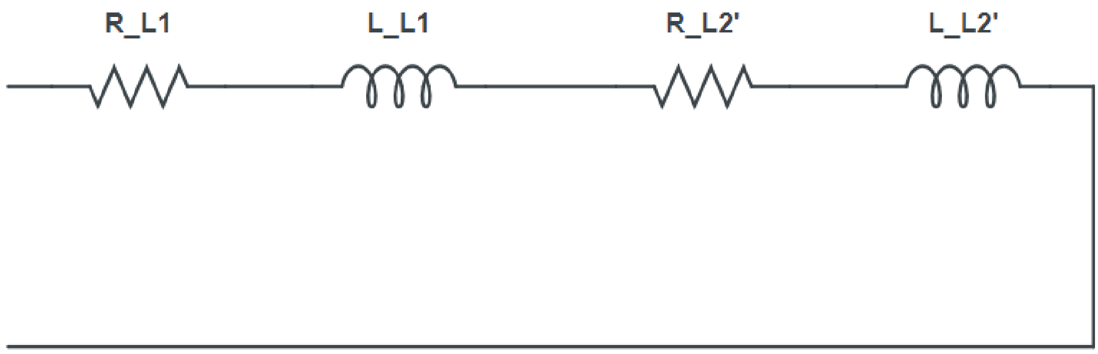


Figure 9. Simplified circuit when secondary side is shorted

That gives us total leakage as seen on the primary.

Now we continue to design RC snubber,

As we know

$f_r = resonant\ frequency\ or\ ringing\ frequency$

$C = parasitic\ capacitance\ of\ FET\ and\ generally\ is\ specified\ on\ datasheet$

C is not accurate because it depends on the voltage and in the datasheet it is measured on specific voltage. Therefore, it might not fit our design specifications. All we need to do it to calculate our parasitic capacitance in our circuit easily, because we know the equation for ringing frequency + we can measure f_r with oscilloscope

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$L\ is\ the\ leakage\ inductance\ as\ seen\ on\ primary$

We can found parasitic capacitance from this equation easily. After found parasitic capacitance, to find R

$$R = \sqrt{\frac{L}{C}} \quad for\ \ Q = 1$$

Or directly we can use the formula

$$R = 2\pi f_r L$$

Up until now, we had ignored the impact of the capacitor in our RC snubber because its inclusion would make our equations very complicated, so we will use an empirical method.

The snubber capacitor has the following impacts:

- The larger capacitor, the larger power loss but the better Q. i.e.:
    - If we use a large capacitor, we will get perfect correlation and a Q of 1, but have massive losses
    - If we use a very small capacitor, we will have low losses but larger Q and more oscillations
- A good compromise is to calculate capacitor value such that the losses are limited to around 25 to 60 mW → this avoid creation of hot spots on the PCB whilst maintaining a low Q

The equation for losses in our snubber is:

$$P_{loss\_snubber} = C_{snub} \times V^2{}_{c\_snub} \times f_s$$

$V_{c\_snub} = voltage\ on\ the\ drain\ at\ turnoff\ of\ FET$

$V_{c\_snub} = V_{in} + V_o \times N$ where N = turn ratio $(\frac{N_1}{N_2})$

That was for primary RC snubber design

3.1.4 Secondary RC Snubber Design

At the diode turn-off, the secondary diode parasitic capacitance will ring with leakage of flyback converter

The procedure and the design equations are exactly the same as primary RC snubber design we have seen on section 3.1 to 3.1.4

Step 1: Measure the leakage (L) as seen on the primary and referred to secondary

L which is seen on primary and refer to secondary

$$\frac{L}{N^2}$$

Where $N = \frac{N_1}{N_2}$

Step 2: Measure f_r from the ringing on the oscilloscope

For Q = 1, $R_{snub} = 2\pi f_r L$

Step 3: Calculate C_{snub} based on power dissipation of 25 mW to 60 mW

$$P_{loss\_snubber} = C_{snub} \times V^2{}_{c\_snub} \times f_s$$

$V_{c\_snub}\ for\ secondary\ is$

$$V_{c\_snub} = V_o + \frac{V_{in}}{N}$$

4. RCD Clamp Design

On some occasions (particularly in Flybacks) where the leakage spike is very high, an RC snubber is not enough

We would like clamp the peak of the spike to a voltage level that is not going to damage our FET

The most common is a RCD clamp

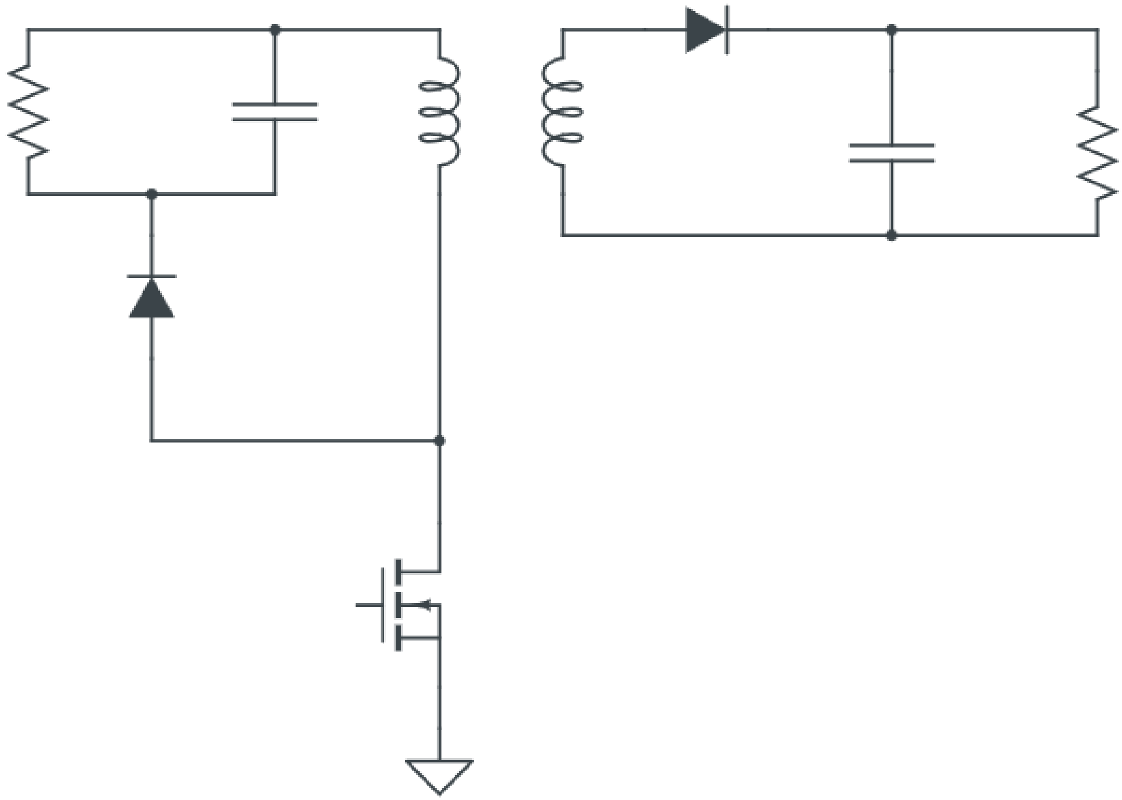


Figure 10. RCD clamp example

Voltage at turn-off on FET: $V_{in} + NV_o$

For example, $V_{in} = 12V$, $V_o = 7.5V$, and $N = 1$

Maximum turn-on voltage for example 29.8V

If the maximum desired voltage on FET = 30V

Then $V_{clamp} = 30 - 12 = 18\,V$

$$V_{clamp} = 18\,V$$

Step 1: Select maximum voltage, V_{max} that we are going to allow on our FET

The higher this voltage the lower losses in the snubber, we would like to maxium spike possible without damaging our FET

Typically 66% of FET's maximum allowable voltage or 85% of FET's maximum allowable voltage minus 20 V to overshoot is a good compromise

As an alternative, we can calculate how much power loss we want to tolerate in clamp and make sure about it and then reverse calculate the maximum clamp voltage

Step 2: Calculate V_{clamp}

$$V_{clamp} = V_{max} - V_{in}$$

Step 3: Calculate P_{clamp} from

$$R_{clamp} = \frac{2(V_{clamp} - NV_{out})}{f_s \times L_{leakage} \times I^2{}_{peak}}$$

Step 4: Calculate C_{clamp}

Unlike RC snubber, the value of RCD capacitor does not impact losses.

Its value, therefore; is not critical, it just needs to be large enough such that voltage remains constant during snubber operation.

It is essentially a RC circuit so a good compromise would be allow 2.5 to 5 time constant

$$C_{clamp} = \frac{5}{R_{clamp} \times f_s}$$

Step 5: Calculate the total power loss in the snubber

$$P_{loss\_clamp} = \frac{1}{2} L_{leakage} I^2{}_{peak} \times f_s \left[\frac{V_{clamp}}{V_{clamp} - NV_{out}}\right]$$