CSE331 Computer Organization
#HW2

First of all i design 3 different module.Those modules are

“MyXor,4x1Mux and Onebitalu”.

I design my own xor beacuse i wasn’t allowed use normal xor gate.

```
module myxor(x1,x2,f);
input x1,x2;
output f;
wire n1,n2;
and(n1,x1,~x2);
and(n2,x2,~x1);
or(f,n1,n2);


endmodule
```

We have 3 parameters.First two are inputs and the last one is output.We used 2 wires for the statements because I wasn’t allowed use “assign” keyword.

The second module is 4x1MUX.I used this module for the selection operation.

I designed this module according to Mux's general formula:

$$Z = \left(A.\bar{S}_0.\bar{S}_1\right) + \left(B.\bar{S}_0.S_1\right) + \left(C.S_0.\bar{S}_1\right) + \left(D.S_0.S_1\right)$$

The Mux selects according to inputs and also selecter bits.

```
module hw1(i0,i1,i2,i3,s0,s1,z);
input i0,i1,i2,i3,s0,s1;
output z;
wire n0,n1,n2,n3;
wire tem0,tem1,tem2,tem3;

and(tem0,~s0,~s1);
and(tem1,~s0,s1);
and(tem2,s0,~s1);
and(tem3,s0,s1);

and(n0,i0,tem0);
and(n1,i1,tem1);
and(n2,i2,tem2);
and(n3,i3,tem3);
or(z,n0,n1,n2,n3);



endmodule
```

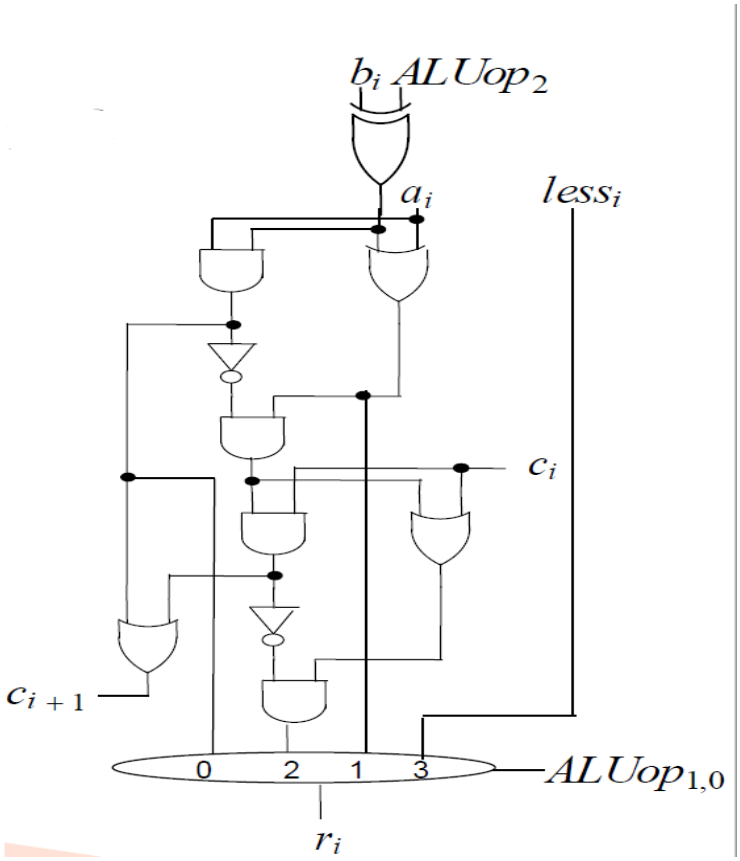
We have 7 parameters.

i0,i1,i2,i3 are the inputs.

S0,S1 are the selecter bits.

Z is the output of the 4x1 Mux.

The third module is onebitalu.I designed this module according to Lecture's pdf.



And this is my code design.

```
module onebitalu(ai,bi,lessi,ci,aluop0,aluop1,aluop2,cinext,ri);
input ai,bi,lessi,ci,aluop0,aluop1,aluop2;
output cinext,ri;
wire t1,t2temp0,temp1,temp2,temp3,temp4,temp5;
myxor(.x1(bi),.x2(aluop2),.f(t1));
and(temp0,t1,ai);
or(temp1,t1,ai);
and(t2,~temp0,temp1);
and(temp2,t2,ci);
or(temp3,t2,ci);
and(temp4,~temp2,temp3);
or(cinext,temp0,temp2);

wire n0,n1,n2,n3;
wire tem0,tem1,tem2,tem3;

and(tem0,~aluop0,~aluop1);
and(tem1,~aluop0,aluop1);
and(tem2,aluop0,~aluop1);
and(tem3,aluop0,aluop1);

and(n0,temp0,tem0);
and(n1,temp1,tem1);
and(n2,temp2,tem2);
and(n3,temp3,tem3);
or(ri,n0,n1,n2,n3);



endmodule
```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