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EEE 102-2

LAB-03: Combinational Logic Circuit

Purpose:

The goal of this assignment was to design and implement a logic circuit using integrated circuits which were chosen by the experimenter, jumper wires, a breadboard, a function generator, LEDs and 4-bit counter (the 74HC163). Additionally, no software implementation or FGPAs were involved in the experiment.

Design Specifications:

In this experiment, additional integrated circuits had to be chosen in order to set up the logic circuit. For this task, a quad 2-input NAND gate (74 LS/HC 00) and a quad 2-input AND gate (74 LS/HC 08) were used (Figure A, Figure B). Only three of the four possible outputs of the counter were used when building the design of the circuit. The first two inputs (Q0 and Q1) were fed to the AND gate. The output of the AND gate and the third output (Q2) were desired to be put through an XOR gate. However, since there were no dual-input XOR gate ICs in the given list, using the quad 2-input NAND gate, a single 2-input XOR gate was designed by wiring certain outputs of NAND gates to each other (Figure C). By using the effective XOR gate, the output of the AND gate and the third counter output were combined (Figure D) and the output was fed to an LED. By using an oscilloscope to monitor the voltage the LED, the design could be monitored to see if the real-world outputs matched ideal calculations.

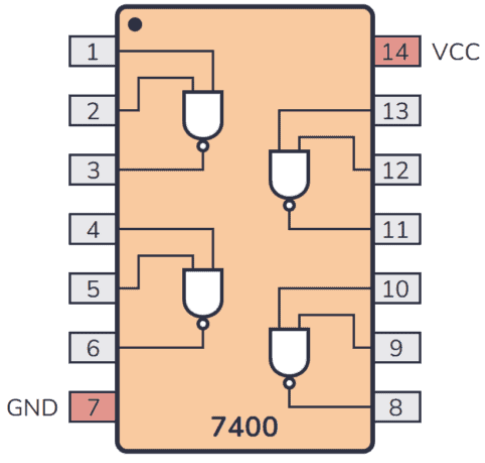

Figure A: Configuration for 74 LS/HC 00

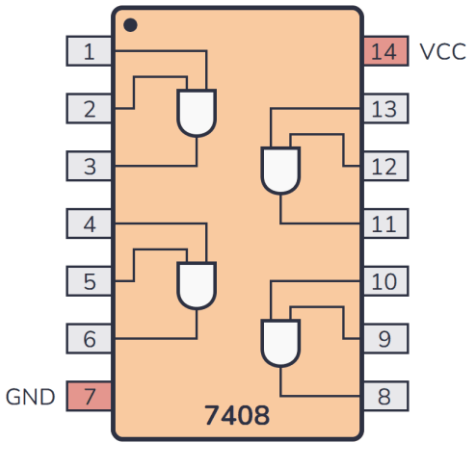

Figure B: Configuration for 74 LS/HC 08

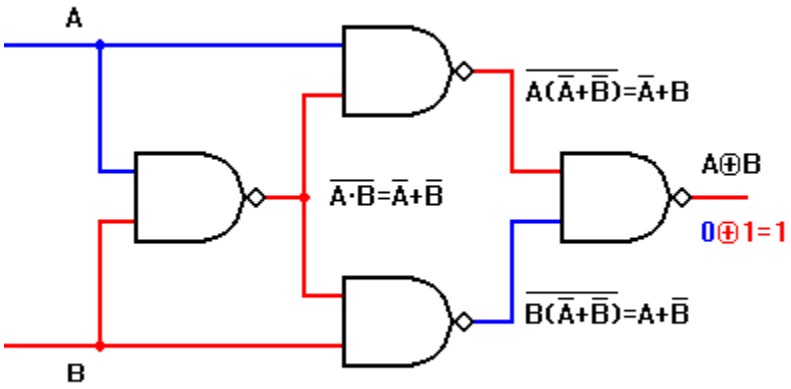

Figure C: Single 2-input XOR configuration using quad 2-input NANDs

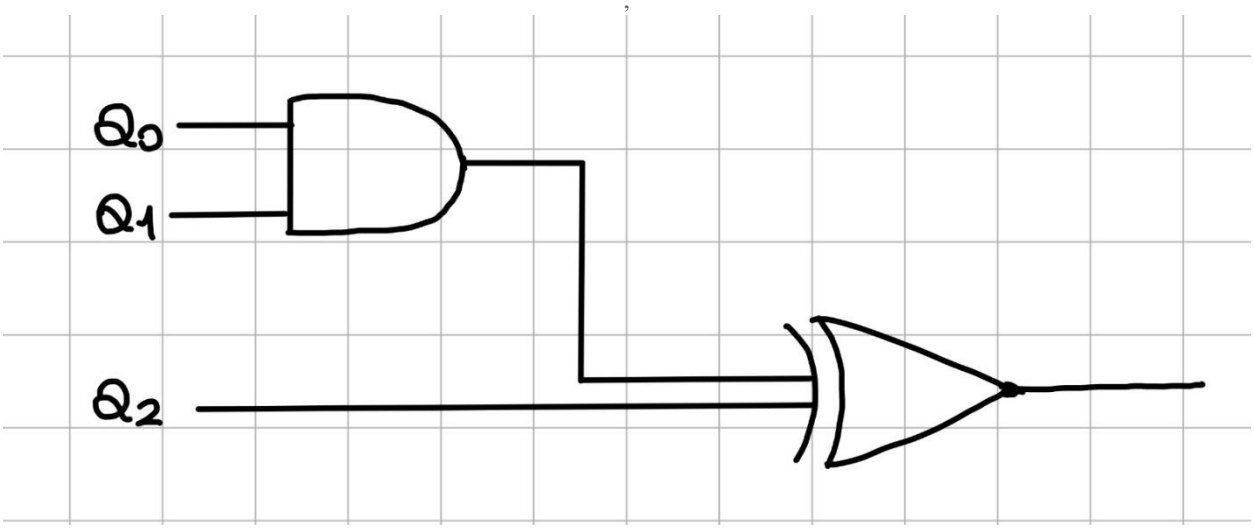

Figure D: Effective combined logic gates

After the required gates were wired with the required outputs, the clock output was formulated. After reading the pinouts of the IC (Figure E), the required implementation was formed. The oscillating waveform would be applied too the clock input whereas the continuous voltage waveform would be applied to the “positive supply voltage”, “parallel enable output” and “count enable input” to set the counter to “count” mode (Figure F). By applying these pins with a positive voltage, the outputs of the system would have equated a counter that would increment every low-to-high change in the square waveform.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

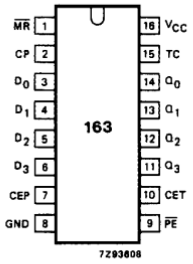

Fig.1 Pin configuration.

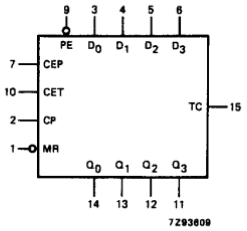

Fig.2 Logic symbol.

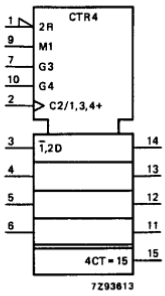

Fig.3 IEC logic symbol.

Figure E: Pinout configuration for the 74HC163

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(1)
count	h	↑	h	h	h	X	count	(1)
hold	h	X	l	X	h	X	q_n	(1)
(do nothing)	h	X	X	l	h	X	q_n	L

Notes

1. The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).
   H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   ↑ = LOW-to-HIGH CP transition

Figure F: Functions and the required pin voltage states required for the functions for the 74HC17-63

Methodology:

Task-1) Using the specified design, the combinational circuit was implemented onto the breadboard. A function generator was connected to the counter's clock input pin (pin 2) and the rest of the required voltages were provided by a power supply. Certain pins of the counter and the required power pins of the gates were powered by said power supply. By analyzing the counter's manual, it's mode was set to "count" by giving the required voltage to the pins (pin 7, 9, 16). To see the output gates at a specific time, LEDs and resistors were connected to the counter's output pins in series. Different outputs were compared to the theoretical cases by comparing them to the circuit's truth table (Table 1). Finally, the last LED was probed to analyze the waveform to observe it's relation to the truth table.

Q_2	Q_1	Q_0	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 1: Truth table for combinational logic circuit

Results:

Task-1) After checking the functionality of the 4-bit counter, the design was implemented to the breadboard (Figure 1.1). The function generator's output was connected to pin 2 and ground while applying a 5 Volt peak-to-peak square wave with a frequency of 1Hz. An adjustable power supply's positive and ground were connected to the positive and negative rails of the breadboard respectively which applied a potential of 5 Volts continuously to the rail. Pin 7, 9 and 16 were connected to the positive rail whereas pin 8 was connected to ground respectively. A count-up of one per second was observed on the output LEDs. Different states of the LEDs were observed and photographed (Figure 1.2-1.9). By observing these states and comparing them to the truth table, the given outputs equated to the ideal final output of the system. After comparing the Boolean states of the circuit, the oscilloscope probe was connected to the longer leg of the final output LED. The oscilloscope display was edited to see the full waveform of the signal (Figure 1.10). The waveform was observed to be equal to the truth table.

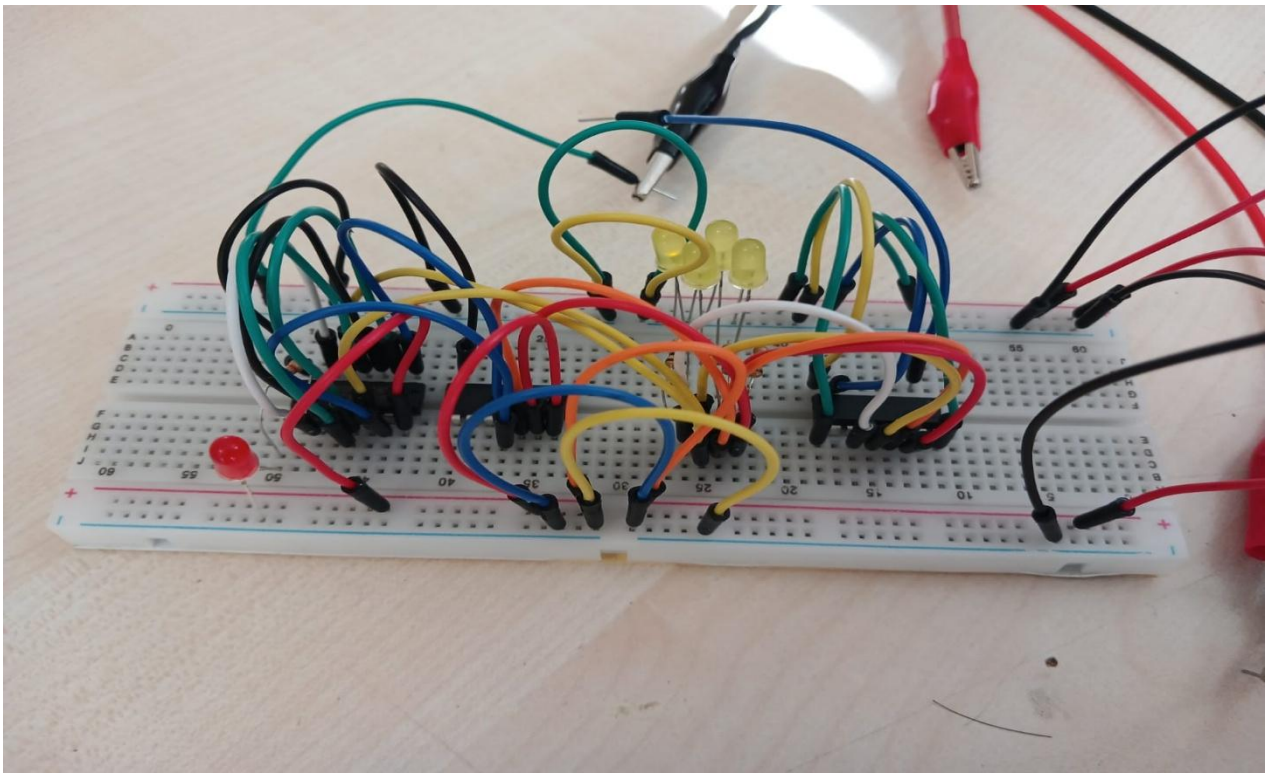

Figure 1.1: Default configuration of the circuit

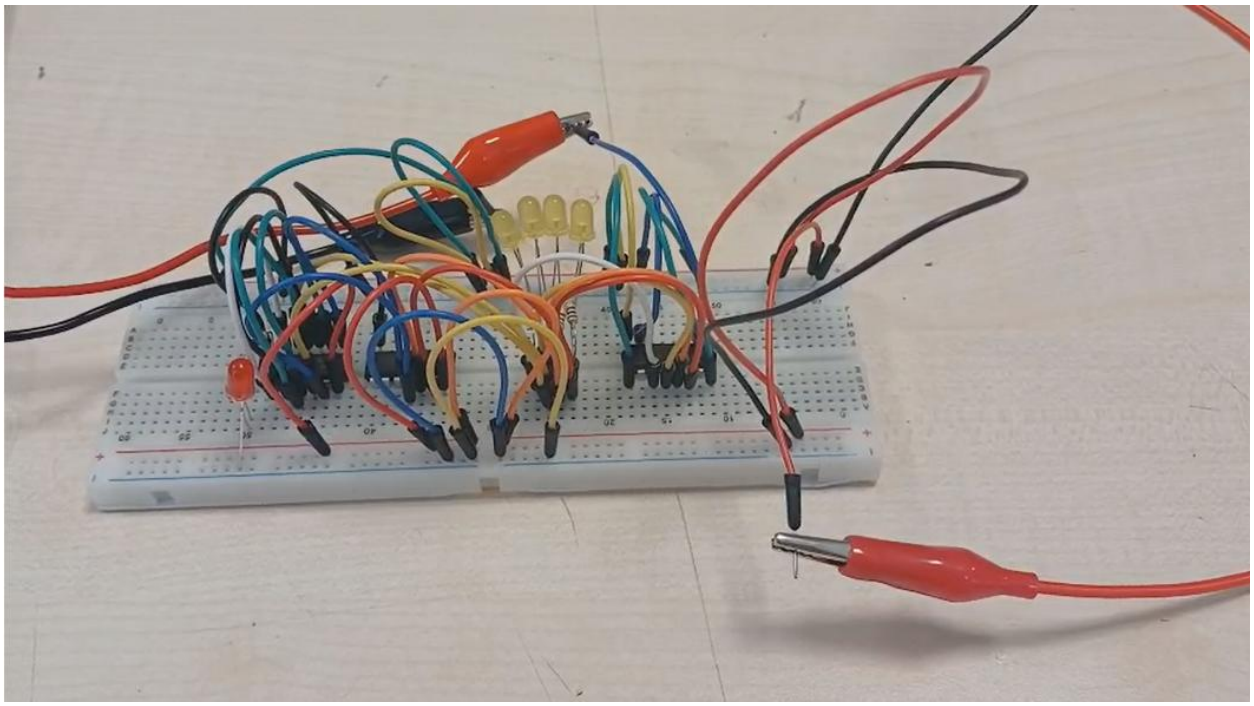

Figure 1.2: State of the circuit when Q0: 0, Q1:0, Q2:0

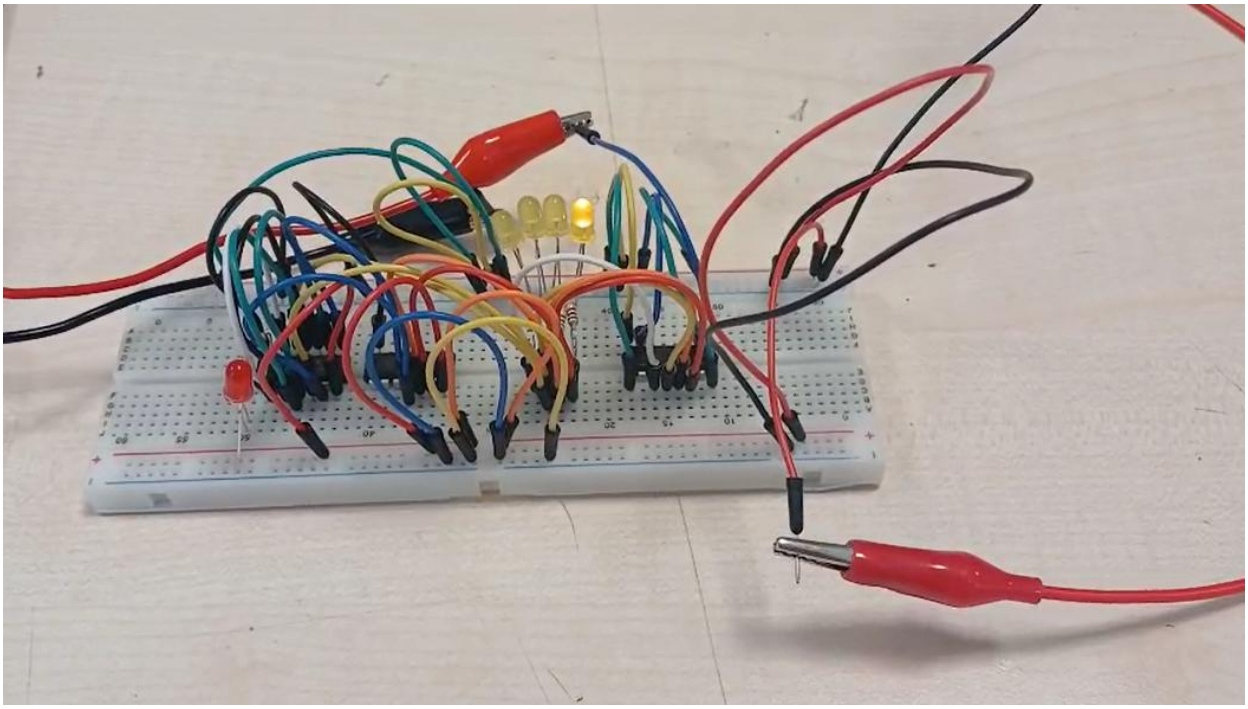

Figure 1.3: State of the circuit when Q0: 1, Q1:0, Q2:0

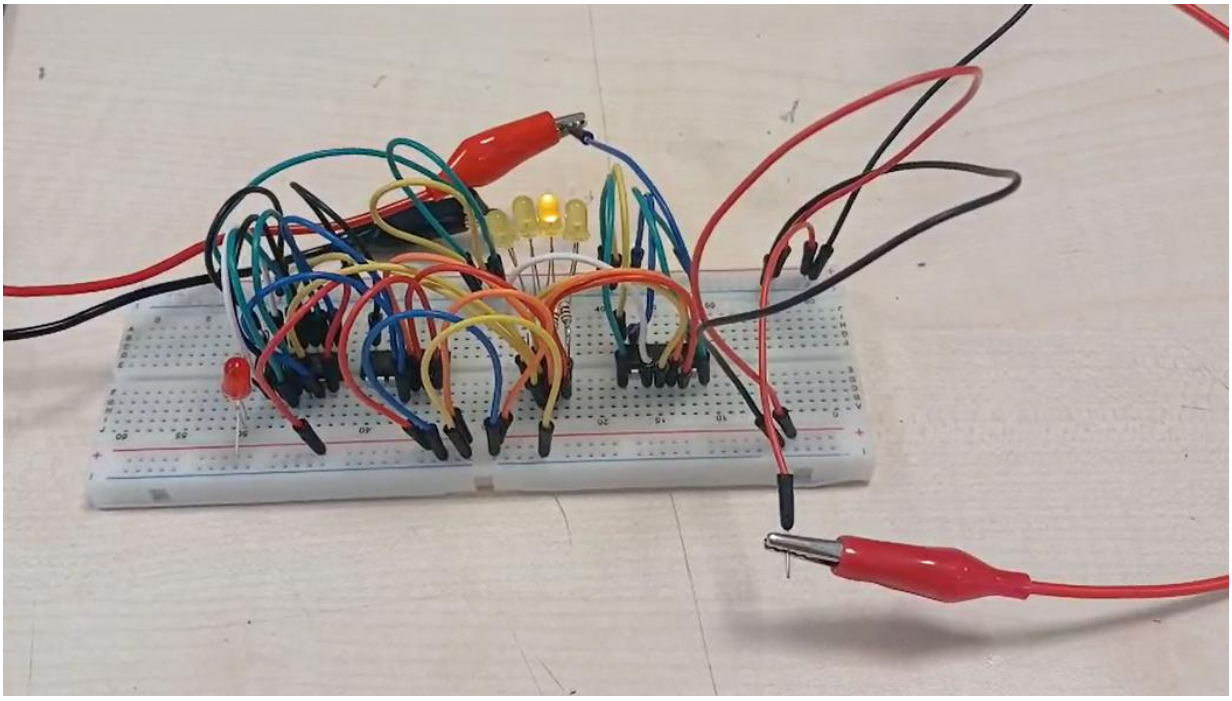

Figure 1.4: State of the circuit when Q0: 0, Q1: 1, Q2: 0

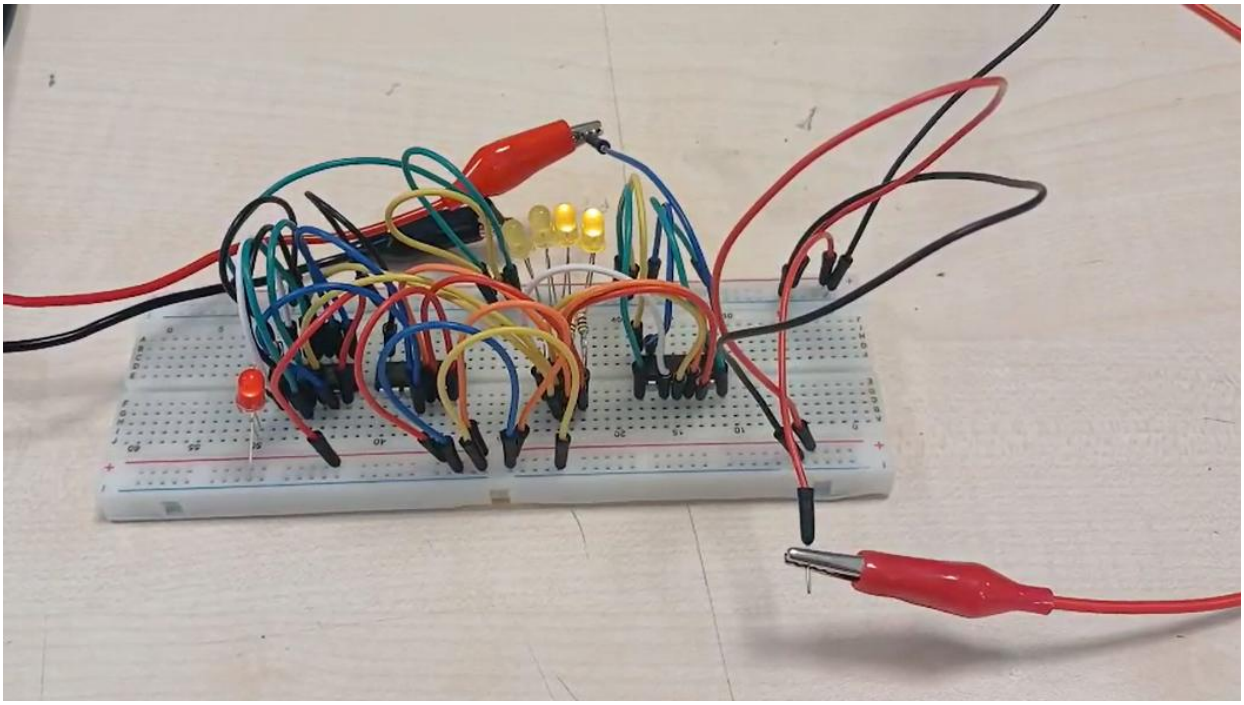

Figure 1.5: State of the circuit when Q0: 1, Q1: 1, Q2: 0

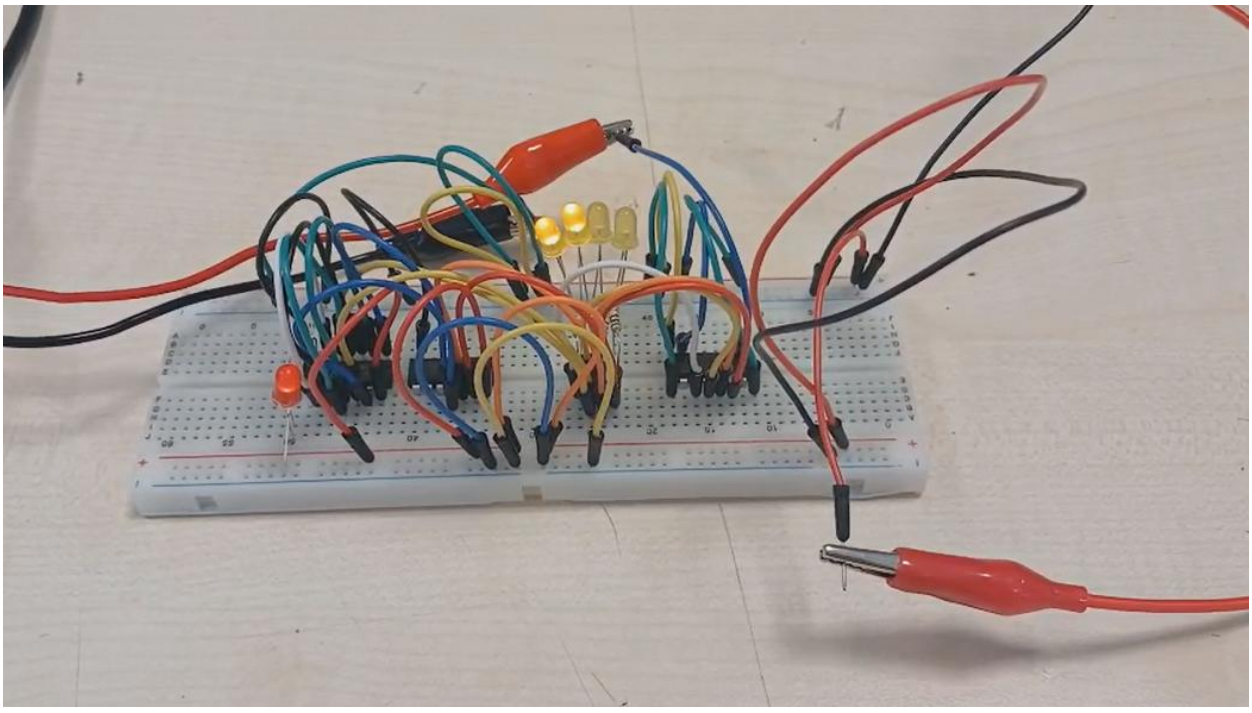

Figure 1.6: State of the circuit when Q0: 0, Q1: 0, Q2: 1

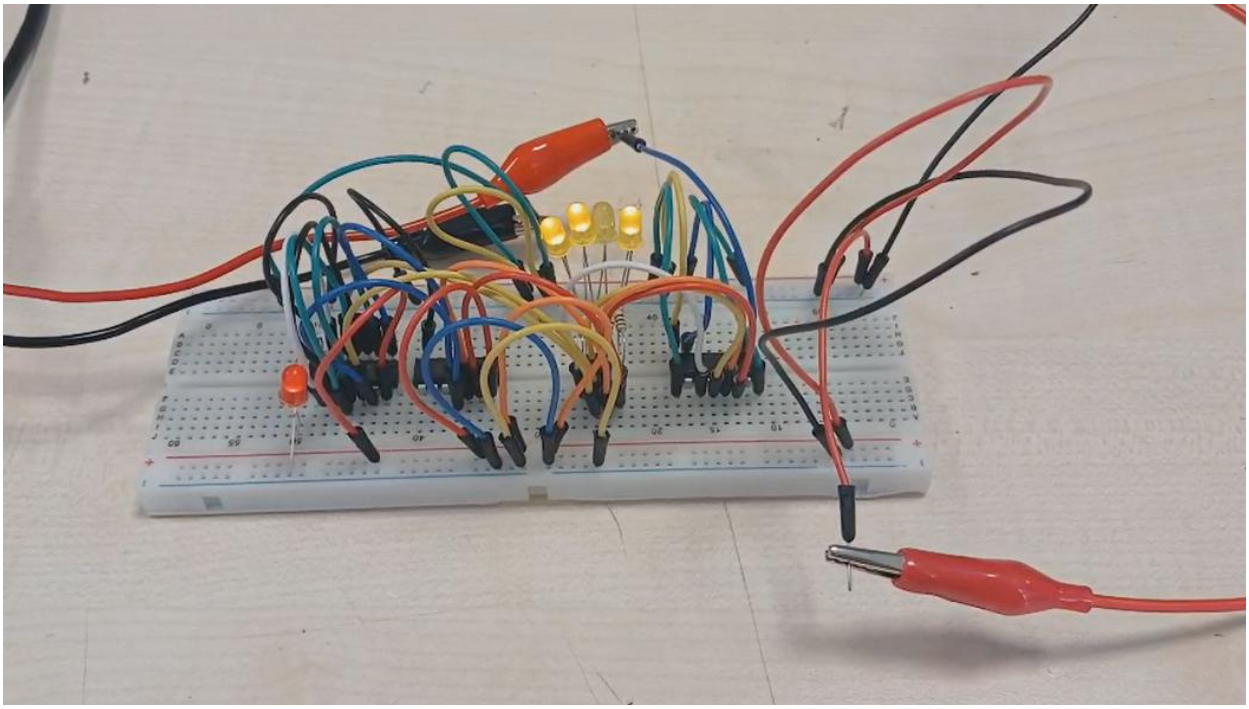

Figure 1.7: State of the circuit when Q0: 1, Q1: 0, Q2: 1

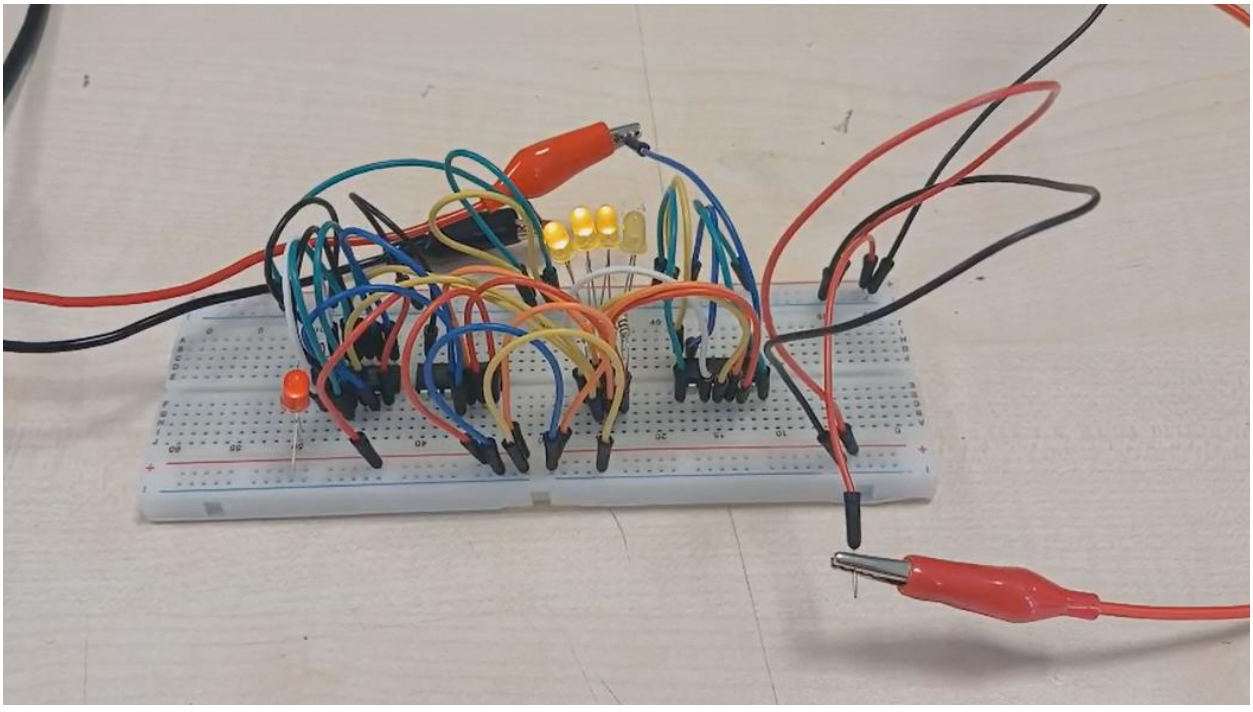

Figure 1.8: State of the circuit when Q0: 0, Q1: 1, Q2: 1

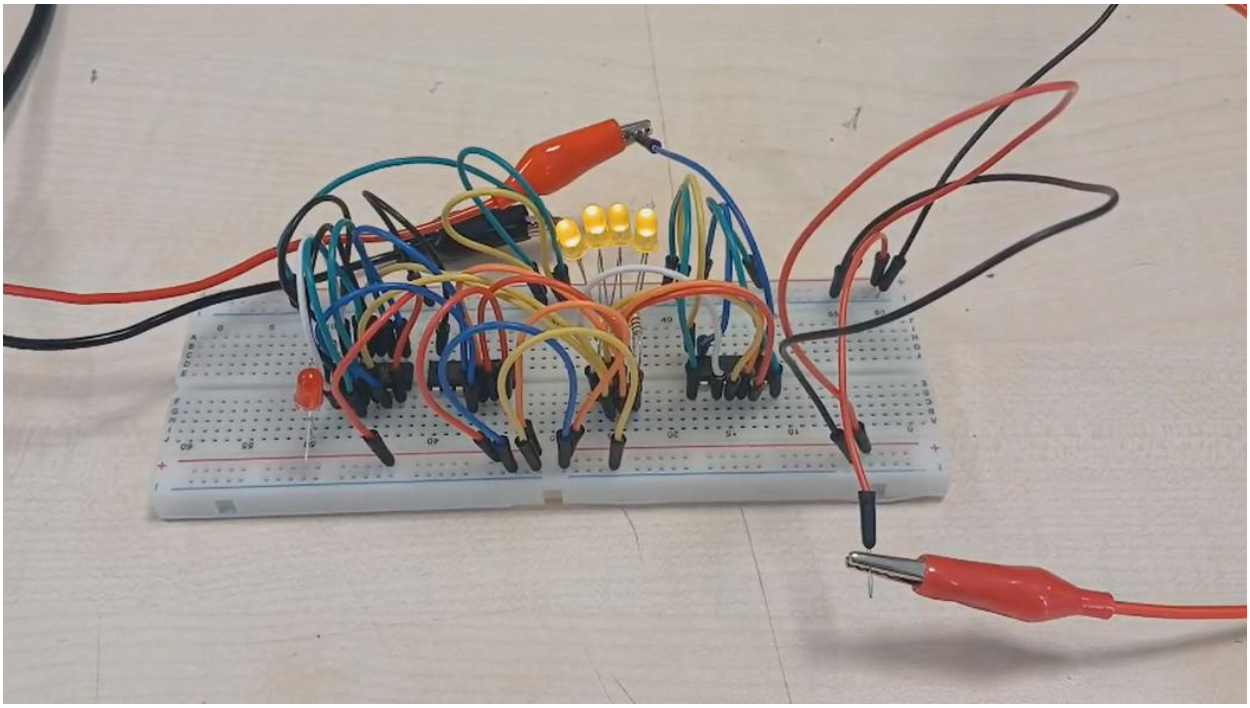

Figure 1.9: State of the circuit when Q0: 1, Q1: 1, Q2: 1

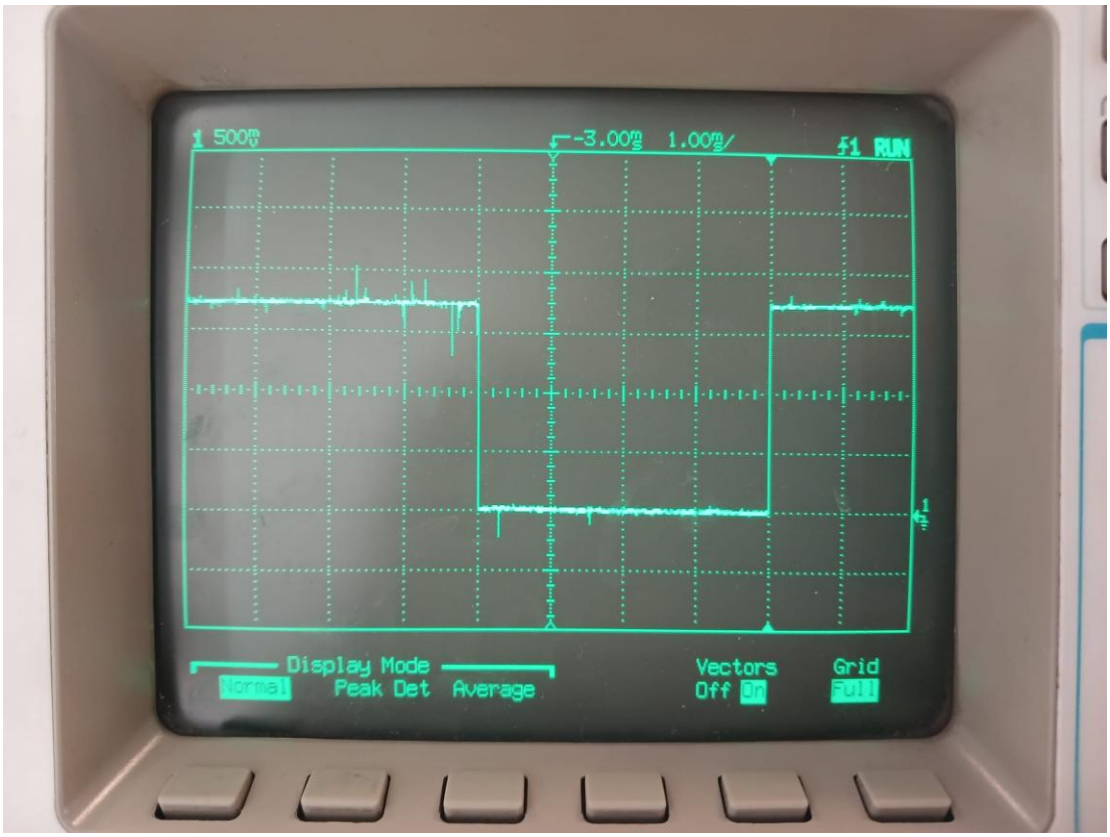

Figure 1.10: Waveform of the final output

Conclusion:

The purpose of this lab assignment was to design and create a combinational logic circuit without using FGPAs or software. A breadboard, a function generator, one 4-bit counter, a quad 2-input AND and NAND gate, five LEDs, five resistors and several jumper cables were used to build the designed circuit. After implementing the circuit, it's output was checked using an oscilloscope and was compared to the truth table of the same logic gate function. The observed results were the same as the ideal results. Through forming the experiment, basic logic implementation using breadboards and 4-bit counter operations were learnt effectively.

References:

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