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EEE 102-2

Project Proposal: Analog to Digital Converter

Purpose:

The purpose of this term project is to create an analog to digital converter using a BASYS 3, a power supply, a breadboard, a potentiometer and jumper cables. The converted signal will be displayed through the built-in LEDs and the 7-segment display using VHDL.

Design Specifications & Methodology:

A power source will be connected to the potentiometer which will be connected to the breadboard. The output of the potentiometer will be connected to one of the ports on the BASYS 3. This will be the main input of the circuit. The power source will supply an analog DC signal to the system which will be converted and turned into a digital signal with a non-continuous form using VHDL. The converted signal will be displayed through the seven-segment display, which will give a detailed reading, and the build in LEDs, which will give a rougher reading of the signal. These outputs will change in real time dependent on the output voltage of the potentiometer. A buzzer will be connected to the FPGA to audially denote the change of the output signal. As an example, if the number of lit-up LEDs decrease, which would mean a drop in the output signal's magnitude, a low frequency signal will be applied to the buzzer for a short time to create a low-pitch noise and a high frequency signal whenever the number of lit-up LEDs increase.

In summary, the device will take an analog DC signal and convert it to a digital DC signal. The strength of the signal will be displayed on the seven-segment display on the BASYS 3 and will also determine the number of LEDs that light up. For every noticeable change in the voltage, a buzzer will play a sound denoting an increase or a decrease of the output potential sequentially with the change in LEDs.

Project Phases:

Phase One: The modules required for translating the analog input into digital values that can be observed on the seven-segment display and the built-in LEDs will be created. Additionally, the module required for the buzzer to put out auditory sounds using signals that will be supplied by the FPGA will be written. A testbench that can simulate the written modules will be implemented and used to test the functionality of the other modules.

Phase Two: The modules will be initialized on the BASYS 3 and the required components will be connected accordingly to the specified design. Multiple states of the circuit will be tested to see if the theoretical states match the real-world outputs.