

MIMXRT1160-EVK Board User Manual



Contents

Chapter 1 Introduction.....	3
1.1 Board overview.....	3
1.2 IMXRT1160 EVK board revision history.....	4
1.3 IMXRT1160 EVK contents.....	4
1.4 Reference documentation.....	4
1.5 EVK design files.....	4
1.6 Acronyms and Abbreviations.....	4
1.7 PCB information.....	5
1.8 Contents of evaluation kit.....	6
Chapter 2 Specifications.....	7
2.1 Board pictures.....	8
2.2 i.MX RT1160 processor.....	9
2.3 Boot mode configurations.....	9
2.4 Power tree.....	10
2.5 SDRAM memory.....	13
2.6 SD card slot.....	13
2.7 Hyper Flash.....	13
2.8 QSPI Flash.....	13
2.9 ENET PHY connector.....	13
2.10 USB PHY connector.....	14
2.11 Audio input/output connector.....	14
2.12 OpenSDA circuit (DAP-Link).....	14
2.13 JTAG connector.....	14
2.14 Arduino expansion port.....	15
2.15 Camera module connector.....	16
2.16 User interface switch/button.....	16
2.17 Sensor (DNP).....	16
2.18 User interface LED indicator.....	16
2.19 LCD interface.....	16
Chapter 3 Revision history.....	18

Chapter 1

Introduction

This document is a Hardware User's Guide for the IMXRT1160 Evaluation Kit (EVK) based on NXP's i.MX RT1160 processor. NXP Semiconductors fully supports this board. The User's Guide includes system setup and debugging. It provides detailed information on the overall design and usage of the EVK board from a hardware systems perspective.

1.1 Board overview

This EVK board is platform designed to showcase the most commonly used features of the i.MX RT1160 Processor in a small, low-cost package. The IMXRT1160 EVK board is an entry level development board, which gives developers an option to be familiar with the processor before investing large amount or resources in more specific designs. For the Board Kit contents, refer to [Contents of evaluation kit](#).

Table 1 lists the features of the IMXRT1160 EVK board.

Table 1. Board features

Board Component	Specification	Details of provider (if any)
Processor	MIMXRT1166DVM6A	NXP Semiconductors
DRAM Memory	W9825G6KH-5I * 2, 512 MB SDRAM, 200 MHz	Winbond
DC-DC	MP2143DJ, MP1613GTL	MPS
LDO	UM1750S-00, UM1550S-28, AMS1117-1.8	UNION, AMS
Mass Storage	TF Card Slot	
	128 Mbit Quad SPI Flash	
	4 Mbit LPSPI Flash (DNP)	
	2 Gbit Parallel NAND Flash (DNP)	
Display Interface	MIPI DSI LCD Connector	
Ethernet	10/100 Mbit/s Ethernet Connector. PHY Chip: KSZ8081RNB	Microchip Technology
	10/100/1000 Mbit/s Ethernet Connector. PHY Chip: RTL8211FDT-CG	Realtek
USB	USB 2.0 OTG Connector * 2	
Audio Connector	3.5 mm Audio Stereo Headphone Jack	
	Board-Mounted Microphone	
	Left and Right Speaker Out Connectors	
	S/PDIF Interface (DNP)	

Table continues on the next page...

Table 1. Board features (continued)

Board Component	Specification	Details of provider (if any)
Power Connector	5 V DC-Jack	
Debug Connector	JTAG 20-pin Connector (SWD by default)	
	OpenSDA with DAP-Link	
Sensor (DNP)	FXOS8700CQ: 6-Axis Encompass (3-Axis Mag, 3-Axis Accel)	NXP Semiconductors
Camera	MIPI CSI Interface	
CAN	CAN Bus Connector	
User Interface Button	ON/OFF, POR Reset, Reset, USER Button	
LED Indicator	Power Status, Reset, OpenSDA, USER LED	
Expansion Port	Arduino Interface, M.2 interface	
PCB	5.1968 inch x 6.1024 inch (13.2 cm x 15.5 cm), 6-layer board	

1.2 IMXRT1160 EVK board revision history

- EVK REVA: Internal use, Alpha program, and product launch

1.3 IMXRT1160 EVK contents

The IMXRT1160 EVK contains the following items:

- IMXRT1160 EVK board
- 5 V power adapter
- USB cable (Micro B)

1.4 Reference documentation

Below are listed the additional documents and resources that you can refer to for more information on the IMXRT1160 EVK board. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local NXP field applications engineer (FAE) or sales representative.

- IMXRT1160 EVK Quick Start Guide

1.5 EVK design files

The schematics, layout files, and Gerber files (including Silkscreen) can be downloaded from MIMXRT1160-EVK Product Support Page on www.nxp.com.

1.6 Acronyms and Abbreviations

The following table lists the acronyms and abbreviations used in this document.

Table 2. Acronyms and abbreviations

Term	Description
ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
CAN	Controller Area Network
CSI	Camera Serial Interface
eMMC	Embedded Multimedia Card
GPIO	General Purpose In/Out
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LDO	Low Dropout Regulator
LED	Light Emitting Diode
MMC	MultiMedia Card
MSD	Mass Storage Device
PLL	Phase-Locked Loop
QSPI	Quad Serial Peripheral Interface
ROM	Read-Only Memory
RTC	Real-time Clock
SD	Secure Digital Card
SDHC	Secure Digital High Capacity
SRAM	Static Random Access Memory
SDRAM	Synchronous Dynamic Random-Access Memory
QSPI	Queued/Quad Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

1.7 PCB information

The IMXRT1160 EVK board uses the standard 6-layer technology. The material used is FR-4. The table below describes the PCB stack-up information.

Table 3. Board stack-up information

Layer	Description	Copper (Oz)	Dielectric thickness (mil)
1	Signal	1/2	—
	Dielectric	—	3.5
2	GND	1	
	Dielectric		5
3	Signal	1	—
	Dielectric	—	37
4	Power	1	—
	Dielectric		5
5	GND	1	—
	Dielectric	—	3.5
6	Signal	1/2	—

1.8 Contents of evaluation kit

Table 4. EVK contents

Item	Description
EVK board	EVK board with processor, memory, interfaces, and so on
Power adapter	5V/3A power adapter
USB cable	USB cable, Micro-B to Standard-A

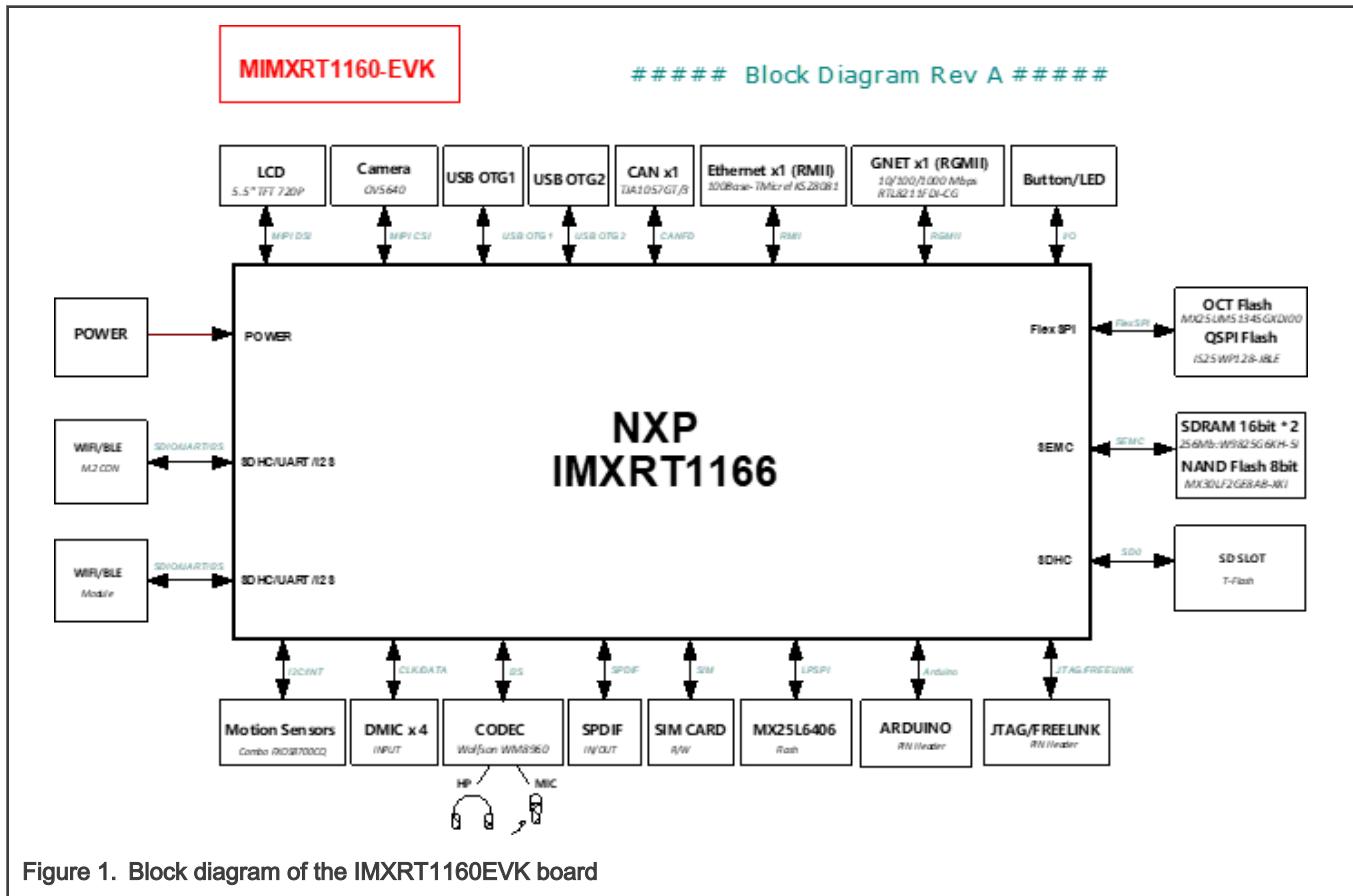
NOTE

Micro SD Card and LCD Module are not standard parts of the Evaluation Kit.

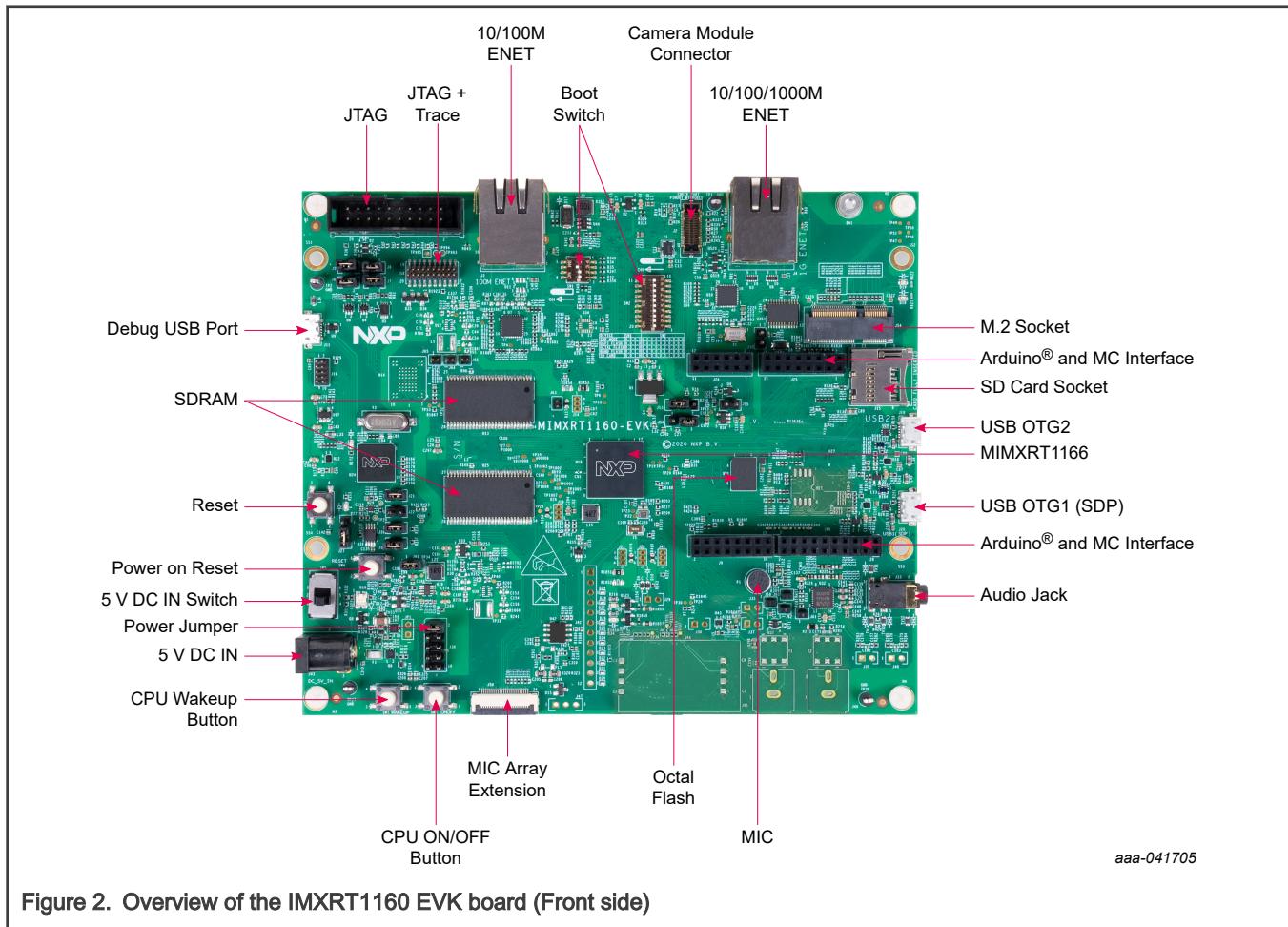
Chapter 2

Specifications

This chapter provides detailed information about the electrical design and practical considerations of the EVK board. [Figure 1](#) shows the block diagram of the IMXRT1160 EVK board. Board pictures are shown in the following section.



2.1 Board pictures



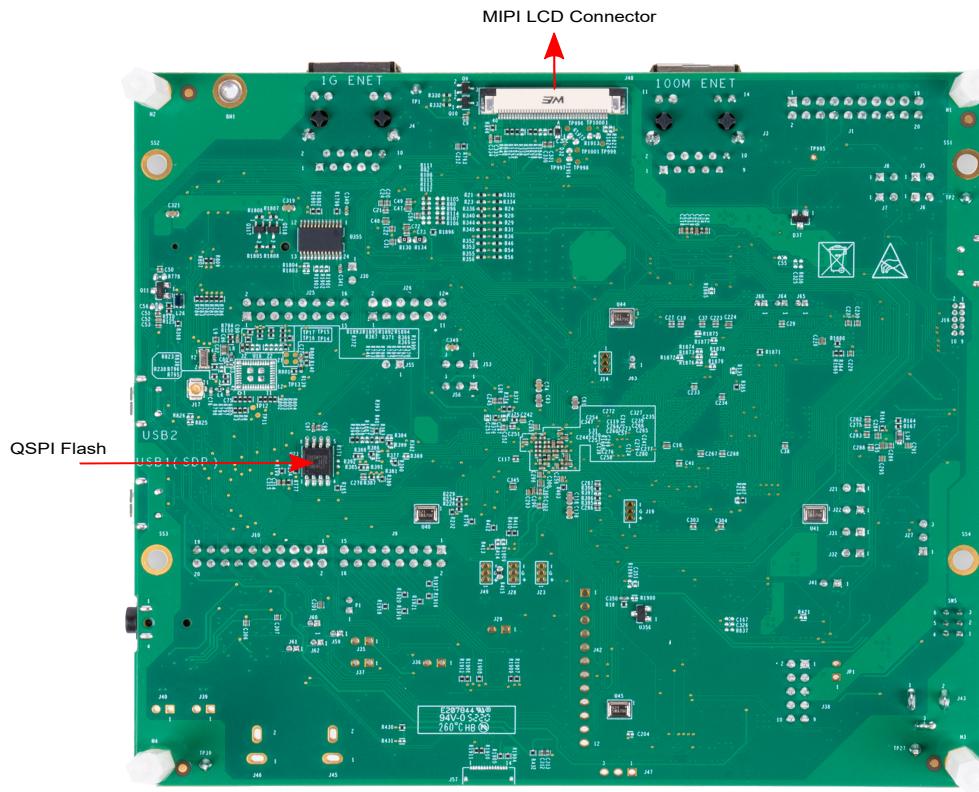


Figure 3. Overview of the IMXRT1160 EVK board (Back side)

2.2 i.MX RT1160 processor

The i.MX RT1160 is a new processor family featuring NXP's advanced implementation of the high performance Arm® Cortex®-R M7 Core and power efficient Arm CortexR-M4 Core. It provides high CPU performance and best real-time response.

The i.MX RT1160 has 2 MB on-chip RAM in total, including a 512 kB RAM which can be flexibly configured as TCM or general-purpose on-chip RAM. The i.MX RT1160 integrates advanced power management module with DC-DC and LDO that reduces complexity of external power supply and simplifies power sequencing.

It provides various memory interfaces, including SDRAM, Raw NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, Hyper RAM/Flash. It also provides a wide range of other interfaces for connecting peripherals, such as WLAN, BluetoothR, GPS, displays, and camera sensors. Like other i.MX processors, i.MX RT1160 also has rich audio and video features, including MIPI CSI/DSI, LCD display, graphics accelerator, camera interface, S/PDIF, and I2S audio interface.

The i.MX RT1160 applications processor can be used in areas such as industrial HMI, IoT, high-end audio appliance, low-end instrument cluster, motor control, and home appliances.

2.3 Boot mode configurations

The device has four boot modes, with one reserved for NXP use. The boot mode is selected based on the binary value stored in the internal BOOT_MODE register. Switches (SW1-3 and SW1-4) are used to select the boot mode on the IMXRT1160 EVK board.

Table 5. Boot mode pin settings

BOOT_MODE[1:0] (SW1-3 SW1-4)	BOOT type
00	Boot from fuses
01	Serial downloader
10	Internal boot
11	Reserved

Typically, the internal boot is selected for normal boot, which is configured by external `BOOT_CFG` GPIOs. The table below shows the typical boot mode and boot device settings.

Table 6. Typical boot modes and boot device settings

SW1-3	SW1-4	SW2-3	SW2-6	SW2-7	Boot device
0 ¹	1	0	0	0	SDP mode
1	0	0	0	0	QSPI Flash
1	0	1	0	0	OCT Flash
1	0	0	1	0	NAND Flash
1	0	0	0	1	SD card

1. Switch value is not described if the option remains 0 for different boot device.

NOTE

For more information about Boot mode configuration, refer to the "System Boot" Chapter in *MIMXRT1160 Reference Manual*.

For more information about IMXRT1160 EVK boot device selection and configuration, refer to the Board Schematic.

2.4 Power tree

Specifications

A DC 5 V external power supply is used to supply the IMXRT1160 EVK board at J43, and a slide switch SW5 is used to turn the power ON/OFF. J20 and J11 can also be used to supply the EVK Board. Different power supplies need to configure different Jumper setting of J38. The table below lists the details.

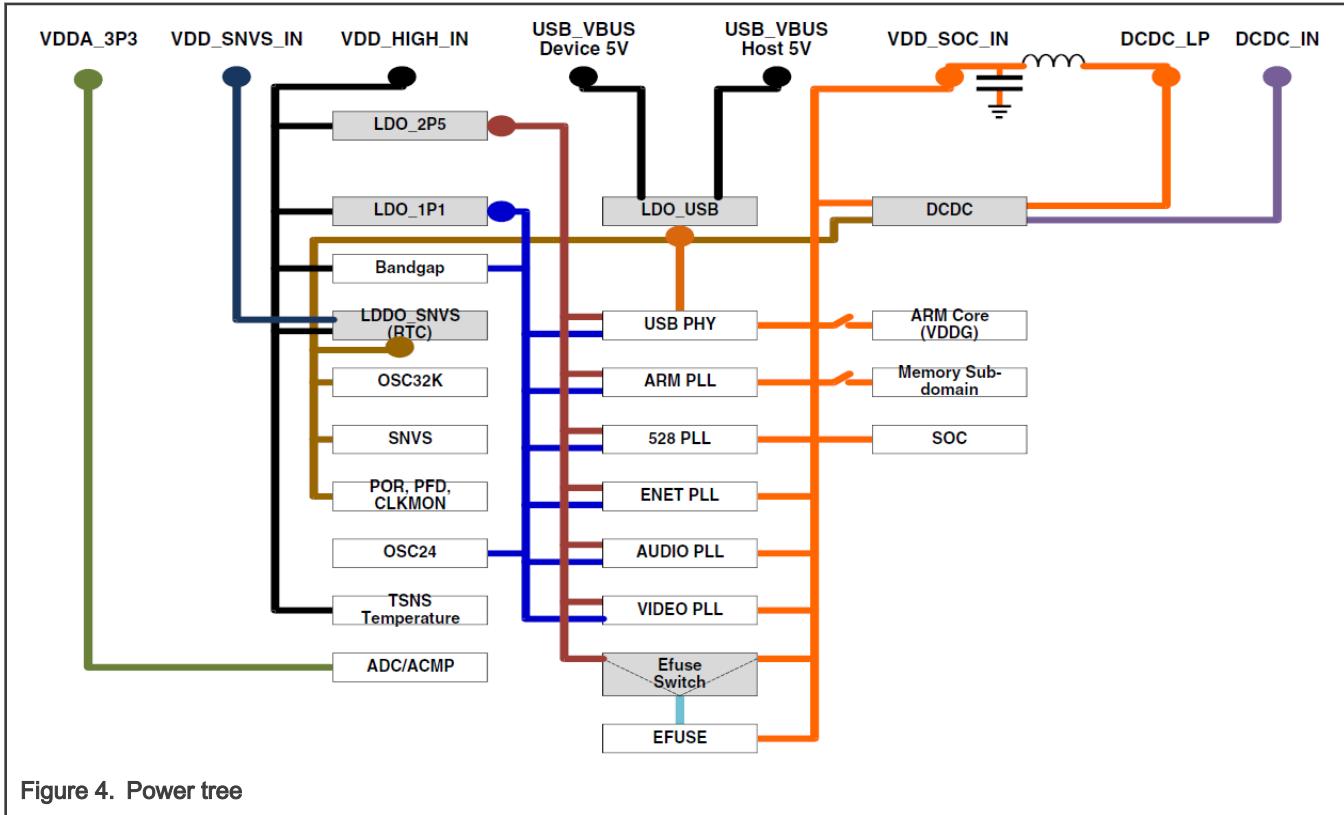
Table 7. Jumper settings of power supply

Power supply	J38 settings
J43	1-2
J20	3-4
J11	5-6

NOTE

For some use cases, the power consumption is larger than 500 mA@5V. For such cases, it is recommended to use a DC adapter that can support up to 3 A.

Figure 4 shows the power tree.

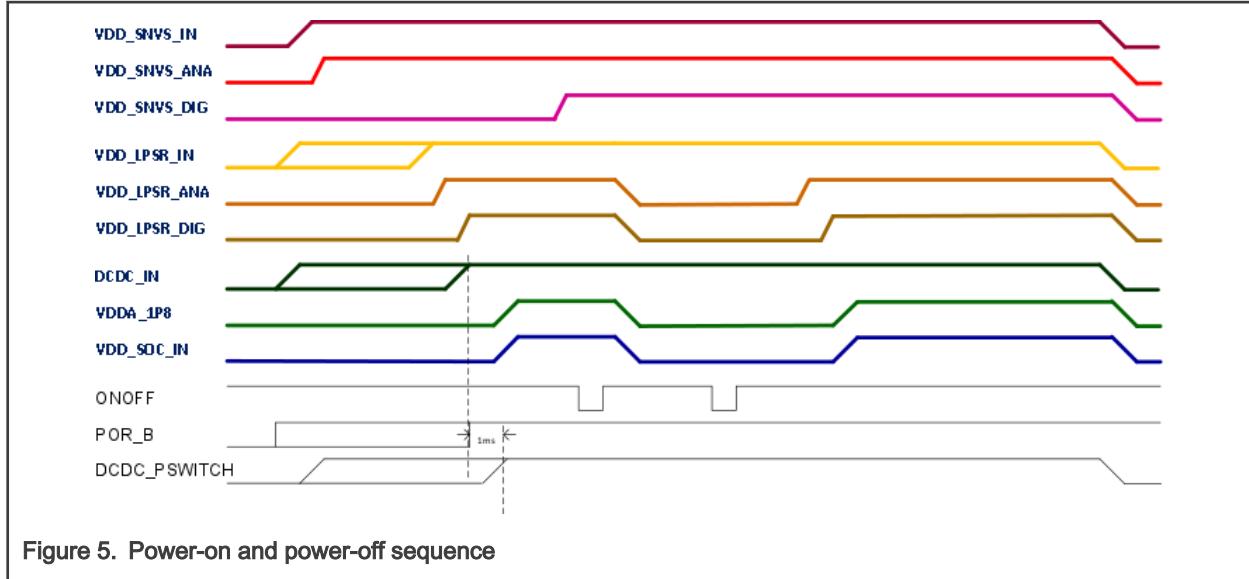


- **Power-on sequence requirements:**

- `VDD_SNVS_IN` supply must be turned on before any other power supply, or be connected (shorted) with `VDD_LPSR_IN` and `DCDC_IN` supply.
- If a coin cell is used to power `VDD_SNVS_IN`, ensure that it is connected before any other supply is switched on.
- When internal DC-DC is enabled, external delay circuit is required to delay the `DCDC_PSWITCH` signal 1 ms after `DCDC_IN` is stable.
- The `POR_B` input, if used, must be immediately asserted at power-on and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the `POR_B` input, the internal POR module takes control.

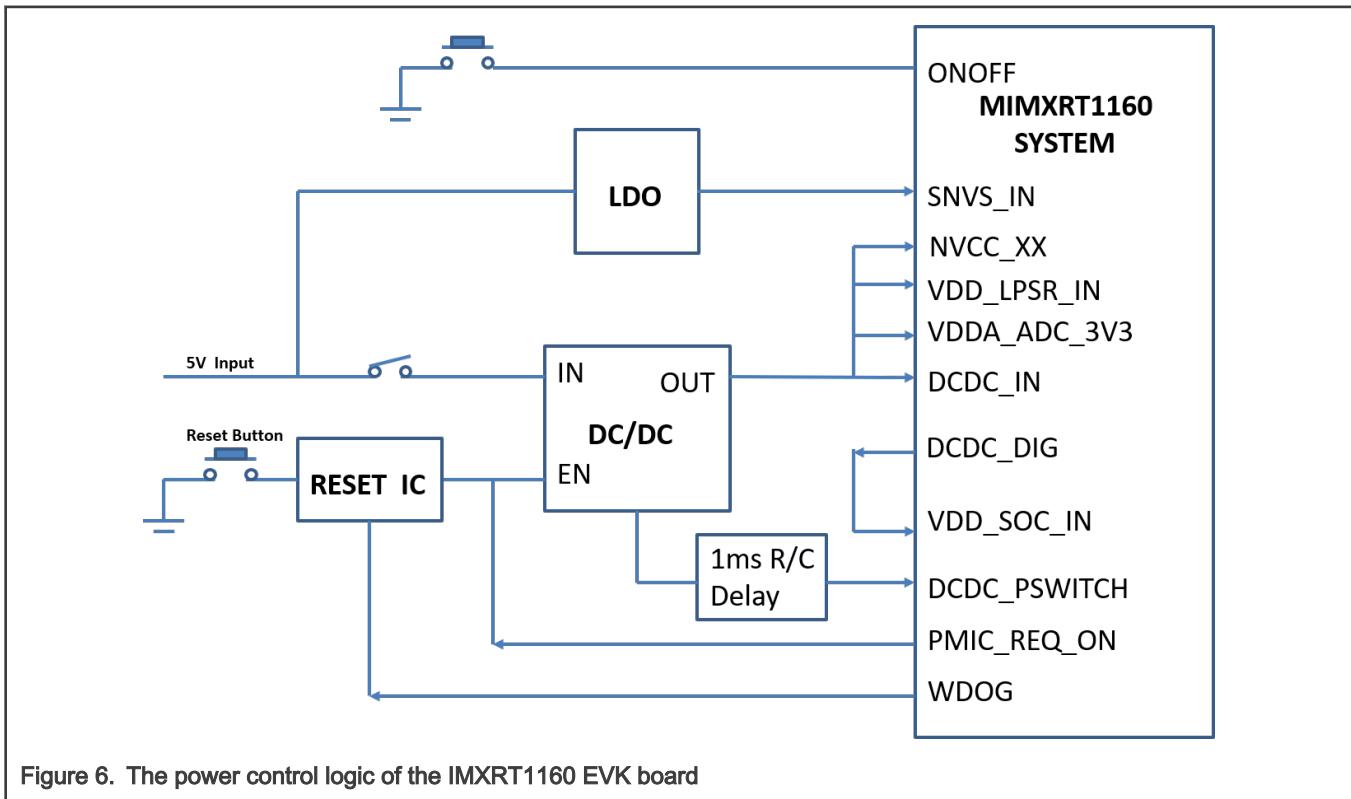
- **Power-off sequence requirements:**

- `VDD_SNVS_IN` supply must be turned off after any other power supply, or be connected (shorted) with `VDD_LPSR_IN` and `DCDC_IN` supply.
- If a coin cell is used to power `VDD_SNVS_IN`, ensure that it is removed after any other supply is switched off.



The figure below shows the power control logic of the IMXRT1160 EVK board.

- It powers up SNVS first, then PMIC_ON_REQ is switched on to enable external DC-DC to power up other power domains.
- ON/OFF button is used to switch ON/OFF PMIC_ON_REQ to control power modes.
- The RESET button and WDOG output are used to reset the system power.



The table below describes the power rails on the board.

Table 8. Power rails

Power rail	Min (V)	Typ (V)	Max (V)	Description
DCDC_IN	3	3.3	3.6	Power for DC-DC
VDDA_1P8_IN	1.71	1.8	1.89	Power for PLL, OSC, and LDOs
VDD_SOC_IN	0.7	1.0	1.155	Power for digital logics
VDD_LPSR_IN	3	3.3	3.6	Power for LPSR domain
VDD_SNVS_IN	2.4	3	3.6	Power for SNVS and RTC
VDD_USB_1P8	1.65	1.8	1.95	Power for USB OTG PHYs
VDD_USB_3P3	3	3.3	3.6	
VDD_ADC_1P8	1.65	1.8	1.95	Power for ADC, Power for DAC and ACMP, ADC_VREFH<VDDA_ADC_1P8>
VDD_ADC_3P3	3	3.3	3.6	
VDD_MIPI_1P8	1.65	1.8	1.95	Power for MIPI CSI/DSI PHY
VDD_MIPI_1P0	0.9	1.0	1.1	Power for MIPI CSI/DSI PHY

2.5 SDRAM memory

Two 256 MB, 200 MHz SDRAM (W9825G6KH-5I) is used on the EVK Board.

2.6 SD card slot

There is an SD card slot (J15) on the IMXRT1160 EVK board. J15 is the Micro SD slot for USDHC1 interface. If the developer wants to boot from the SD Card, the boot device switch settings should be set correctly as shown in [Table 6](#).

2.7 Hyper Flash

Specifications

On the IMXRT1160 EVK board, there is one 512 Mbit Hyper Flash device. If the developer wants to boot from the Hyper Flash, the boot device switch settings should be set correctly as shown in [Table 6](#).

By default, the Hyper Flash is not used. To enable the onboard OCT Flash, the settings must be changed.

1. Remove resistors: R380/R399/R386/R390/R392/R385.
2. Weld 0 Ω resistors: R381/R378/R382/R389/R402/R377/R388/R391.

2.8 QSPI Flash

A 128 Mbit QSPI Flash is used on the IMXRT1160 EVK board. If the developer wants to boot from the QSPI Flash, the boot device switch settings should be set correctly as shown in [Table 6](#).

By default, this QSPI Flash is enabled on the EVK.

2.9 ENET PHY connector

There are two Ethernet Mac controllers in the MIMXRT1160 processor.

The 10/100 M Ethernet subsystems of the IMXRT1160 EVK board are provided by the KSZ8081RNB 10/100 M Ethernet transceiver (U7) and an RJ45 (J3) with integrated magnetic.

The 10/100/1000 M Ethernet subsystems of the IMXRT1160 EVK board are provided by the RTL8211FDI-CG 10/100/1000 M Ethernet transceiver (U10) and an RJ45 (J4) with integrated magnetic.

2.10 USB PHY connector

The MIMXRT1160 contains two integrated USB 2.0 PHYs capable of connecting to USB host/device systems at the USB low-speed (LS) rate of 1.5 Mbits/s, full-speed (FS) rate of 12 Mbits/s or at the USB 2.0 high-speed (HS) rate of 480 Mbits/s.

2.11 Audio input/output connector

The audio CODEC used on the IMXRT1160 EVK board is Wolfson's low-power, high-quality Stereo Codec, WM8960. The IMXRT1160 EVK board includes:

1. One headphone interface (J33), which is a 3.5 mm audio stereo headphone jack that supports jack detection.
2. One on-board MIC (P1).
3. Two speaker interfaces (J39, J40).

The EVK also provides the SPDIF interface (J45 and J46, DNP) and DMIC interface input through U40/U41/U44/U45.

2.12 OpenSDA circuit (DAP-Link)

The OpenSDA circuit (CMSIS-DAP) is an open-standard serial and debug adapter. It bridges serial and debug communications between a USB host and an embedded target processor.

CMSIS-DAP features a Mass Storage Device (MSD) bootloader, which provides a quick and easy mechanism for loading different CMSIS-DAP Applications such as flash programmers, run-control debug interfaces, serial-to-USB converters, etc. Two or more CMSIS-DAP applications can run simultaneously. For example, run-control debug application and serial-to-USB converter run in parallel to provide a virtual COM communication interface while allowing code debugging via CMSIS-DAP with just a single USB connection.

For the IMXRT1160 EVK board, J11 is the connector between the USB host and the target processor. Jumper to serial downloader mode uses the stable DAP-Link debugger function. If developer wants to make OpenSDA going to the bootloader mode, jumper J27 to 1-2 and press SW3 when powering it on. Meanwhile, the OpenSDA supports drag/drop feature for U-Disk.

1. **Use the serial downloader mode to drag/drop the image file to U-Disk.**
2. **Select QSPI Flash as boot device.**
3. **Reset the board.**

Now the image runs.

2.13 JTAG connector

J1 is a standard 20-pin/2.54 mm box header connector for JTAG. [Figure 7](#) shows the pin definitions. SWD is supported by default.

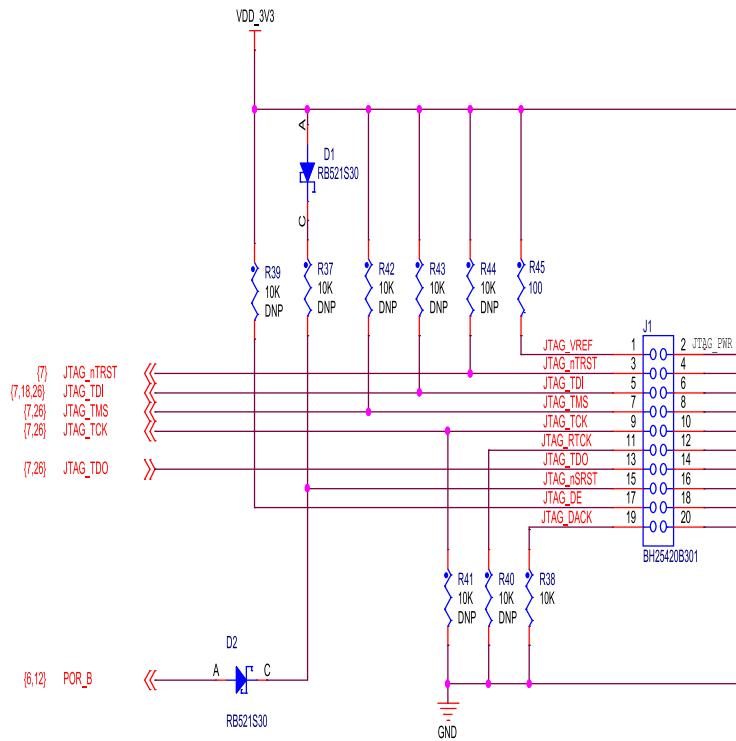


Figure 7. JTAG pin definitions

NOTE

By default, the RT1160 silicon can use both SWD and JTAG modes using the Arm stitching sequence. For the RT1160 EVK board, SWD debug is used by default without any board modification. To use JTAG debug, solder out R187, R208, R195, and R78, because some JTAG signals are multiplexed with other functions.

2.14 Arduino expansion port

J22 to J25 are defined as Arduino interfaces. The table below lists the pin definitions of Arduino interfaces.

Table 9. Arduino interface pin definitions

J9	J26	J10	J25
UART_RX/D0	A0/ADC0	D8/CLK0/ICP1	NC
UART_TX/D1	A1/ADC1	D9/OC1A/PWM	IOREF
D2/INT0	A2/ADC2	D10/SPI_CS	RESET
D3/INT1/PWM/OC2B	A3/ADC3	D11/OC2A/PWM/SPI_MOSI	3.3 V
D4/T0/XCK	A4/ADC4/SDA	D12/SPI_MISO	5 V
D5/TI/PWM	A5/ADC5/SCL	D13/SPI_CLK	GND
D6/AIN0/PWM/OC0A	—	GND	GND
D7/AIN1/PWM	—	AREF	VIN
—	—	D14/I2C_SDA	—
—	—	D15/I2C_SCL	—

2.15 Camera module connector

The i.MX RT1160 EVK board supports one MIPI CSI. There is a Camera Module Connector (J2) on the IMXRT1160 EVK board. The MT9M114 based on OV5640 can be used directly.

2.16 User interface switch/button

There are four user interface switches/buttons on the IMXRT1160 EVK board. Their functionalities are as below.

2.16.1 Power switch

SW5 is a slide switch to control the power of the IMXRT1160 EVK board when the power supply is from J43. The functions of this switch are listed as below:

- Sliding the switch to the ON position connects the 5 V power supply to the Evaluation board main power system.
- Sliding the switch to the OFF position immediately removes all power from the board.

2.16.2 ON/OFF button

SW6 is the ON/OFF button for IMXRT1160 EVK board. A short pressing in the OFF mode causes the internal power management state machine to change state to ON. In the ON mode, a short pressing generates an interrupt, intended to be a software-controllable (power-down). Pressing for approximate five seconds or longer causes a forced OFF. Both boot mode inputs can be disconnected.

2.16.3 Reset button

There are two reset buttons on the EVK board. SW4 is the power-on reset button. Pressing the SW4 in the ON state forces reset on the system power except for SNVS domain. The processor is immediately turned off and a boot cycle from the OFF state is reinitiated. SW3 is the POR pin reset button.

2.16.4 USER button

SW7 is the USER button connected to the WAKEUP pin for developer to use.

2.17 Sensor (DNP)

U34 on the EVK board is a 6-Axis Ecompass, 3-Axis Magnetometer, 3-Axis Accelerator, and sensor FXOS8700CQ. The Ecompass is connected to I2C5 port of i.MX RT1160.

2.18 User interface LED indicator

There are four LED status indicators on the EVK board. The functions of these LEDs include:

- Main power supply(D16)
 - Green: DC 5 V main supply is normal.
 - Red: J2 input voltage is over 5.6 V.
 - Off: the board is not powered.
- POR pin Reset RED LED (D7)
- USER LEDs (D6, D34)

2.19 LCD interface

The Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) controller is a flexible digital core, with high-performance and easy to use. It implements all protocol functions defined in the MIPI DSI specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals.

If developers want to use LCD, NXP provides an optional LCD module RK055HDMIPI4M equipped with a 5.5" 720*1280 TFT LCD display with touch sensitive overlay. This module contains one FPC cable that connects to RT1160 EVK. The LCD interface can be connected to J48. LCD modules can be purchased from the NXP website.

Chapter 3

Revision history

Table 10. Revision history

Revision number	Date	Substantive changes
1	07 September 2021	Deleted the MIPI CAMERA MODULE and DNP sensor
0	25 May 2021	Initial public release

How To Reach Us**Home Page:**nxp.com**Web Support:**nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 07 September 2021

Document identifier: UM11617

