a-Si TFT LCD Single Chip Driver 320RGBx480 Resolution and 16.7M color

Specification

Preliminary

Version: V1.00

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1 Introduction

GC9403 is a 16.7M-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 320RGB×480 dots, comprising a 960-channel source driver, a 480-channel gate driver, 345, 600 bytes GRAM for graphic display data of 320RGB×480 dots, and power supply circuit.

GC9403 supports parallel 8-/9-/16-/18-/24 bit data bus MCU interface, 16-/18-/24 bit data bus RGB interface, 3-/4-line serial peripheral interface (SPI) and MIPI interface. The GC9403 is also compliant with RGB (16-/18-/24-bit) data bus for video image display.

GC9403 can operate under 1.65V ~ 3.3V I/O interface voltage and support wide analog power supply range. GC9403 supports full color, 8-color display mode and sleep mode for precise power control by software, which make the GC9403 an ideal LCD driver for medium or small size portable products such as digital cellular phone, smart phone, MP3 and PMP where long battery life is a major concern.

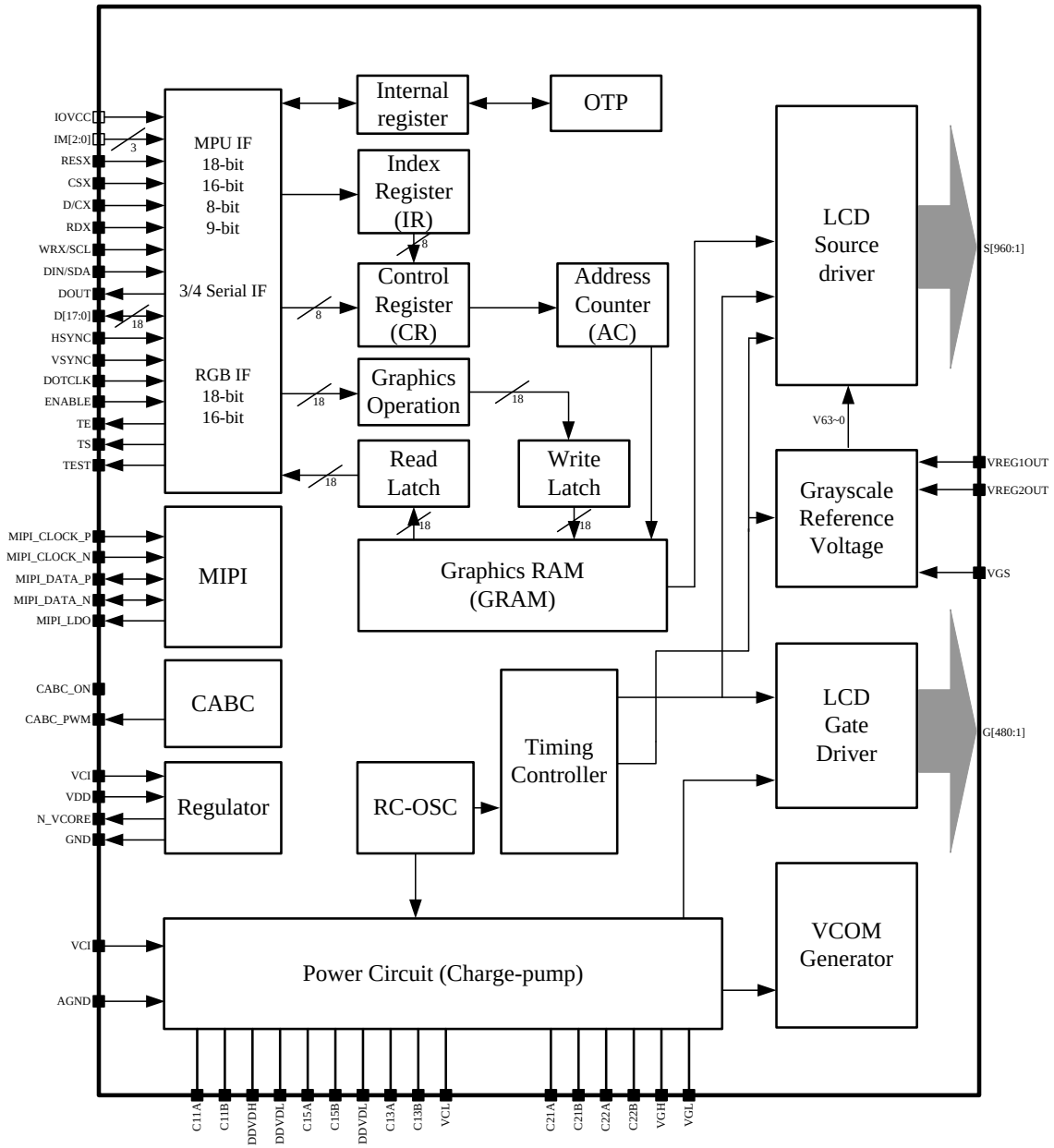
2 Features

- Display resolution: [320×RGB](H) × 480(V)
- Output:
  - 960 source outputs
  - 480 gate outputs
  - Common electrode output
- a-TFT LCD driver with on-chip full display RAM: 345,600 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits and 24-bits interface with 8080 series MCU
  - 3-line / 4-line serial interface
  - MIPI
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color, 65K-color,16.7M-color
  - Reduced color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - DC VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/Column/Z inversion
  - Separate RGB Gamma correction
  - CABC (Content Adaptive Brightness Control)
- OTP
  - 8 bits for ID1
  - 8 bits for ID2
  - 8 bits for ID3
  - 7 bits for VCOM adjustment
- Low -power consumption architecture
  - Low operating power supplies:
- IOVCC = 1.65V ~ 3.6V (logic)
- VCI = 2.5V ~ 3.6V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
- DDVDH − GND = 4.5V ~ 6.0V
- VCL − GND = −2.0V ~ −3.0V
- VCI − VCL ≦ 6.0V
  - Gate driver output voltage

- VGH − GND = 10.0V ~ 20.0V
- VGL− GND = −5.0V ~ −15.0V
- VGH − VGL ≦32V
  - VCOM driver output voltage
- VCOM = 0 ~ −2.0V
- Operate temperature range: −40℃ to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3 Block Diagram

3.1 Block diagram



3.2 Pin Descriptions

<table>
<tr><th colspan="4">Bus Interface Pins</th></tr>
<tr><td>Pin Name</td><td>I/O</td><td>Type</td><td>Descriptions</td></tr>
<tr><td>IM[2:0]</td><td>I</td><td>MPU
IOVCC/DGND</td><td>- Select the interface mode
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th><th>Data pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080 24-bit bus interface</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8080 9-bit bus interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8080 16-bit bus interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080 8-bit bus interface</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Prohibited</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-line SPI</td><td>SDA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI-DSI</td><td>MIPI_DATA_P
MIPI_DATA_N
MIPI_CLOCK_P
MIPI_CLOCK_N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-line SPI</td><td>SDA</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>MPU
Reset Circuit</td><td>- The external reset input.
- Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>MPU
IOVCC/DGND</td><td>- A chip select signal
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>D/CX</td><td>I</td><td>MPU
IOVCC/DGND</td><td>- Parallel interface (D/CX): the signal for command or parameter selection.
Low: command
High: parameter
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>MPU
IOVCC/DGND</td><td>- 8080 system (WRX): Serves as a write signal and writes data at the rising edge.
- 3-/4-line serial interface (SCL): Serves as serial clock pin.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>MPU
IOVCC/DGND</td><td>- 8080 system (RDX): Serves as a read signal and read data at the rising edge.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>DIN/SDA</td><td>I/O</td><td>MPU
IOVCC/DGND</td><td>- Serial data input / output.
Fix to IOVCC or DGND level when not in use.</td></tr>
</table>

<table>
<tr><td>DOUT</td><td>O</td><td>MCU</td><td>- Serial data output.
Leave the pin open when not in use.</td></tr>
<tr><td>TE</td><td>O</td><td>MPU</td><td>- Tearing effect output.
Leave the pin open when not in use.</td></tr>
<tr><td>CABC_PWM</td><td>O</td><td>VCI</td><td>- Backlight control pin.
Leave the pin open when not in use.</td></tr>
<tr><td>CABC_ON</td><td>O</td><td>VCI</td><td>- Backlight control pin.
Leave the pin open when not in use.</td></tr>
<tr><td>MIPI_CLOCK_P</td><td>I</td><td>MIPI</td><td>- Positive polarity of low voltage differential clock signal</td></tr>
<tr><td>MIPI_CLOCK_N</td><td>I</td><td>MIPI</td><td>- Negative polarity of low voltage differential clock signal</td></tr>
<tr><td>MIPI_DATA_P</td><td>I/O</td><td>MIPI</td><td>- Positive polarity of low voltage differential data signal</td></tr>
<tr><td>MIPI_DATA_N</td><td>I/O</td><td>MIPI</td><td>- Negative polarity of low voltage differential data signal</td></tr>
<tr><td>DB[23:0]</td><td>I/O</td><td>MPU</td><td>- A 18-bit parallel bi-directional data bus for MCU system
<table>
<tr><th>Interface mode</th><th>Data pin in use</th></tr>
<tr><td>8-bit MCU system interface mode</td><td>DB[7:0]</td></tr>
<tr><td>9-bit MCU system interface mode</td><td>DB[8:0]</td></tr>
<tr><td>16-bit MCU system interface mode</td><td>DB[15:0]</td></tr>
<tr><td>24-bit MCU system interface mode</td><td>DB[23:0]</td></tr>
<tr><td>16-bit RGB interface mode</td><td>DB[15:0]</td></tr>
<tr><td>18-bit RGB interface mode</td><td>DB[17:0]</td></tr>
<tr><td>24-bit RGB interface mode</td><td>DB[23:0]</td></tr>
</table>
Fix to DGND level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>- Frame synchronizing signal for RGB interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>- Line synchronizing signal for RGB interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>Enable</td><td>I</td><td>MPU</td><td>- Data enable signal for RGB interface operation.
Low: access enabled
High: access inhibited
Fix to DGND level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU</td><td>- Dot clock signal for RGB interface operation.
Fix to IOVCC level when not in use.</td></tr>
</table>

Charge-pump and regulator circuit			
Pin Name	I/O	Type	Descriptions
VCI	P	Power supply	- A supply voltage to the analog circuit. Connect to an external power supply of 2.5V ~ 3.6V.
DDVDH	O	Stabilizing capacitor	- Power supply for the source driver and VCOM driver. - Place a stabilizing capacitor between DDVDH and GND.
DDVDL	O	Stabilizing capacitor	- Power supply for the source driver and VCOM driver. - Place a stabilizing capacitor between DDVDL and GND.
VGH	O	Stabilizing capacitor	- Power supply for the gate driver. - Place a stabilizing capacitor between VGH and GND.
VGL	O	Stabilizing capacitor	- Power supply for the gate driver. - Place a stabilizing capacitor between VGL and GND.
VCL	O	Stabilizing capacitor	- Power supply for the VCOM driver. - VCL = 0.5V ~ −VCI, place a stabilizing capacitor between VCL and GND.
C11A, C11B C15A, C15B	O	Step-up capacitor	- Capacitor connection pins for the step-up circuit 1.
C13A, C13B C21A, C21B C22A, C22B	O	Step-up capacitor	- Capacitor connection pins for the step-up circuit 2.

Power pads			
Pin Name	I/O	Type	Descriptions
IOVCC	P	Power supply	- A supply voltage to the digital circuit. Connect to an external power supply of 1.65V ~ 3.6V.
VDD	O	Power	- Digital circuit power pad. - Connect to a 1μF capacitor.
N_VCORE	O	Power	- Digital circuit negative power pad. - Connect to a 1μF capacitor.
DGND	P	Power supply	- DGND for the digital side: DGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	P	Power supply	- AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
MIPI_LDO	P	Stabilizing capacitor	***Leave the pin open.***

Test Pins			
Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation ,leave these pads open.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		960 pins (320 × RGB)
2	TFT Gate Driver		480 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S960	V0~V63 grayscales
		G1~G480	VGH / VGL
		VCOM	0 ~ −2.0V
5	Input Voltage	IOVCC	1.65V ~ 3.30V
		VCI	2.50V ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.5V
		DDVDL	−6.5 V ~ −4.5V
		VGH	10.0V ~ 20.0V
		VGL	−5.0V ~ −15.0V
		VCL	−1.9V ~ −3.0V
		VGH − VGL	Max. 32.0V
7	Internal Step-up Circuits	DDVDH	VCI × 2
		DDVDL	−(VCI − VCL)
		VGH	VCI × 4, × 5, × 6
		VGL	VCI × −3, × −4, × −5
		VCL	VCI × −1

3.3 PAD coordinates

	Pad name	X	Y
1	TESTP	-11165	-272.75
2	TESTP	-11095	-272.75
3	VSSAM	-11025	-272.75
4	VSSAM	-10955	-272.75
5	VPG	-10885	-272.75
6	DUMMY_DMP0	-10815	-272.75
7	DUMMY_DMP1	-10745	-272.75
8	DUMMY_DMP2	-10675	-272.75
9	DUMMY_DMP3	-10605	-272.75
10	DUMMY_DMP4	-10535	-272.75
11	DUMMY_DMP5	-10465	-272.75
12	DUMMY_DMP6	-10395	-272.75
13	MVDDA	-10325	-272.75
14	MVDDA	-10255	-272.75
15	DUMMY_DMP7	-10185	-272.75
16	MIPI_DATA_N	-10115	-272.75
17	MIPI_DATA_N	-10045	-272.75
18	MIPI_DATA_P	-9975	-272.75
19	MIPI_DATA_P	-9905	-272.75
20	MIPI_CLOCK_N	-9835	-272.75
21	MIPI_CLOCK_N	-9765	-272.75
22	MIPI_CLOCK_P	-9695	-272.75
23	MIPI_CLOCK_P	-9625	-272.75
24	TS0	-9555	-272.75
25	TS1	-9485	-272.75
26	TS2	-9415	-272.75
27	TEST_VREF	-9345	-272.75
28	DB23	-9275	-272.75
29	DB22	-9205	-272.75
30	DB21	-9135	-272.75
31	DB20	-9065	-272.75
32	DB19	-8995	-272.75
33	DB18	-8925	-272.75
34	CABC_PWM	-8855	-272.75
35	IM0	-8785	-272.75
36	IM1	-8715	-272.75
37	IM2	-8645	-272.75
38	RESX	-8575	-272.75
39	VSYNC	-8505	-272.75
40	HSYNC	-8435	-272.75
41	DOTCLK	-8365	-272.75
42	ENABLE	-8295	-272.75
43	DB17	-8225	-272.75
44	DB16	-8155	-272.75
45	DB15	-8085	-272.75
46	DB14	-8015	-272.75
47	DB13	-7945	-272.75
48	DB12	-7875	-272.75
49	DB11	-7805	-272.75
50	DB10	-7735	-272.75

No.	Pad name	X	Y
51	DB9	-7665	-272.75
52	DB8	-7595	-272.75
53	DB7	-7525	-272.75
54	DB6	-7455	-272.75
55	DB5	-7385	-272.75
56	DB4	-7315	-272.75
57	DB3	-7245	-272.75
58	DB2	-7175	-272.75
59	DB1	-7105	-272.75
60	DB0	-7035	-272.75
61	DOUT	-6965	-272.75
62	DIN_SDA	-6895	-272.75
63	RDX	-6825	-272.75
64	WRX_SCL	-6755	-272.75
65	D_CX	-6685	-272.75
66	CSX	-6615	-272.75
67	TE	-6545	-272.75
68	IOVCC	-6475	-272.75
69	IOVCC	-6405	-272.75
70	IOVCC	-6335	-272.75
71	IOVCC	-6265	-272.75
72	IOVCC	-6195	-272.75
73	IOVCC	-6125	-272.75
74	IOVCC	-6055	-272.75
75	VDD	-5985	-272.75
76	VDD	-5915	-272.75
77	VDD	-5845	-272.75
78	VDD	-5775	-272.75
79	VDD	-5705	-272.75
80	VDD	-5635	-272.75
81	VDD	-5565	-272.75
82	VDD	-5495	-272.75
83	VDD	-5425	-272.75
84	VDD	-5355	-272.75
85	VDD	-5285	-272.75
86	GND	-5215	-272.75
87	GND	-5145	-272.75
88	GND	-5075	-272.75
89	GND	-5005	-272.75
90	GND	-4935	-272.75
91	GND	-4865	-272.75
92	GND	-4795	-272.75
93	GND	-4725	-272.75
94	VGS	-4655	-272.75
95	VGS	-4585	-272.75
96	vreg1out	-4515	-272.75
97	AGND	-4445	-272.75
98	AGND	-4375	-272.75
99	AGND	-4305	-272.75
100	AGND	-4235	-272.75

No.	Pad name	X	Y
101	AGND	-4165	-272.75
102	AGND	-4095	-272.75
103	AGND	-4025	-272.75
104	AGND	-3955	-272.75
105	AGND	-3885	-272.75
106	AGND	-3815	-272.75
107	VCOM	-3745	-272.75
108	VCOM	-3675	-272.75
109	VCOM	-3605	-272.75
110	VCOM	-3535	-272.75
111	VCOM	-3465	-272.75
112	VCOM	-3395	-272.75
113	VCOM	-3325	-272.75
114	VCOM	-3255	-272.75
115	VCOM	-3185	-272.75
116	VCOM	-3115	-272.75
117	VCOM	-3045	-272.75
118	VCOM	-2975	-272.75
119	VCOM	-2905	-272.75
120	VCOM	-2835	-272.75
121	VCOM	-2765	-272.75
122	VCOM	-2695	-272.75
123	C41A	-2625	-272.75
124	C41A	-2555	-272.75
125	C41A	-2485	-272.75
126	C41A	-2415	-272.75
127	C41A	-2345	-272.75
128	C41A	-2275	-272.75
129	C41A	-2205	-272.75
130	C41A	-2135	-272.75
131	C41A	-2065	-272.75
132	C41A	-1995	-272.75
133	C41B	-1925	-272.75
134	C41B	-1855	-272.75
135	C41B	-1785	-272.75
136	C41B	-1715	-272.75
137	C41B	-1645	-272.75
138	C41B	-1575	-272.75
139	C41B	-1505	-272.75
140	N_VCORE	-1435	-272.75
141	N_VCORE	-1365	-272.75
142	N_VCORE	-1295	-272.75
143	N_VCORE	-1225	-272.75
144	DUMMY	-1155	-272.75
145	VCL	-1085	-272.75
146	VCL	-1015	-272.75
147	VCL	-945	-272.75
148	VCL	-875	-272.75
149	VCL	-805	-272.75
150	VCL	-735	-272.75

No.	Pad name	X	Y
151	VCL	-665	-272.75
152	VCL	-595	-272.75
153	VCL	-525	-272.75
137.25	DDVDH	-455	-272.75
155	DDVDH	-385	-272.75
156	DDVDH	-315	-272.75
157	DDVDH	-245	-272.75
158	DDVDH	-175	-272.75
159	DDVDH	-105	-272.75
160	DDVDH	-35	-272.75
161	DDVDH	35	-272.75
162	DDVDH	105	-272.75
163	DDVDL	175	-272.75
164	DDVDL	245	-272.75
165	DDVDL	315	-272.75
166	DDVDL	385	-272.75
167	DDVDL	455	-272.75
168	DDVDL	525	-272.75
169	DDVDL	595	-272.75
170	DDVDL	665	-272.75
171	DDVDL	735	-272.75
172	DDVDL	805	-272.75
173	DDVDL	875	-272.75
174	VCI	945	-272.75
175	VCI	1015	-272.75
176	VCI	1085	-272.75
177	VCI	1155	-272.75
178	VCI	1225	-272.75
179	VCI	1295	-272.75
180	VCI	1365	-272.75
181	VCI	1435	-272.75
182	VCI	1505	-272.75
183	VCI	1575	-272.75
184	VCI	1645	-272.75
185	VCI	1715	-272.75
186	VCI	1785	-272.75
187	VCI	1855	-272.75
188	VCI	1925	-272.75
189	VCI	1995	-272.75
190	VCI	2065	-272.75
191	VCI	2135	-272.75
192	VCI	2205	-272.75
193	vreg2out	2275	-272.75
194	C11B	2345	-272.75
195	C11B	2415	-272.75
196	C11B	2485	-272.75
197	C11B	2555	-272.75
198	C11B	2625	-272.75
199	C11B	2695	-272.75
200	C11B	2765	-272.75

No.	Pad name	X	Y
201	C11B	2835	-272.75
202	C11B	2905	-272.75
203	C11B	2975	-272.75
204	C11B	3045	-272.75
205	C11A	3115	-272.75
206	C11A	3185	-272.75
207	C11A	3255	-272.75
208	C11A	3325	-272.75
209	C11A	3395	-272.75
210	C11A	3465	-272.75
211	C11A	3535	-272.75
212	C11A	3605	-272.75
213	C11A	3675	-272.75
214	C11A	3745	-272.75
215	C11A	3815	-272.75
216	C12B	3885	-272.75
217	C12B	3955	-272.75
218	C12B	4025	-272.75
219	C12B	4095	-272.75
220	C12B	4165	-272.75
221	C12B	4235	-272.75
222	C12B	4305	-272.75
223	C12B	4375	-272.75
224	C12B	4445	-272.75
225	C12B	4515	-272.75
226	C12A	4585	-272.75
227	C12A	4655	-272.75
228	C12A	4725	-272.75
229	C12A	4795	-272.75
230	C12A	4865	-272.75
231	C12A	4935	-272.75
232	C12A	5005	-272.75
233	C12A	5075	-272.75
234	C12A	5145	-272.75
235	C12A	5215	-272.75
236	VGL	5285	-272.75
237	VGL	5355	-272.75
238	VGL	5425	-272.75
239	VGL	5495	-272.75
240	VGL	5565	-272.75
241	VGL	5635	-272.75
242	VGL	5705	-272.75
243	VGL	5775	-272.75
244	VGL	5845	-272.75
245	VGL	5915	-272.75
246	AGND	5985	-272.75
247	AGND	6055	-272.75
248	AGND	6125	-272.75
249	VGH	6195	-272.75
250	VGH	6265	-272.75

No.	Pad name	X	Y
251	VGH	6335	-272.75
252	VGH	6405	-272.75
253	VGH	6475	-272.75
254	VGH	6545	-272.75
255	VGH	6615	-272.75
256	VGH	6685	-272.75
257	C51B	6755	-272.75
258	C51B	6825	-272.75
259	C51B	6895	-272.75
260	C51B	6965	-272.75
261	C51B	7035	-272.75
262	C51B	7105	-272.75
263	C51A	7175	-272.75
264	C51A	7245	-272.75
265	C51A	7315	-272.75
266	C51A	7385	-272.75
267	C51A	7455	-272.75
268	C51A	7525	-272.75
269	C52B	7595	-272.75
270	C52B	7665	-272.75
271	C52B	7735	-272.75
272	C52B	7805	-272.75
273	C52B	7875	-272.75
274	C52B	7945	-272.75
275	C52B	8015	-272.75
276	C52B	8085	-272.75
277	C52B	8155	-272.75
278	C52B	8225	-272.75
264.7	C52B	8295	-272.75
280	C52B	8365	-272.75
281	C52B	8435	-272.75
282	C52B	8505	-272.75
283	C52A	8575	-272.75
284	C52A	8645	-272.75
285	C52A	8715	-272.75
286	C52A	8785	-272.75
287	C52A	8855	-272.75
288	C52A	8925	-272.75
272.7	C52A	8995	-272.75
290	C52A	9065	-272.75
291	C52A	9135	-272.75
292	C52A	9205	-272.75
293	C52A	9275	-272.75
294	C52A	9345	-272.75
295	C52A	9415	-272.75
296	C21B	9485	-272.75
297	C21B	9555	-272.75
298	C21B	9625	-272.75
299	C21B	9695	-272.75
300	C21B	9765	-272.75

No.	Pad name	X	Y
301	C21B	9835	-272.75
302	C21B	9905	-272.75
303	C21B	9975	-272.75
304	C21B	10045	-272.75
305	C21B	10115	-272.75
306	C21B	10185	-272.75
307	C21B	10255	-272.75
308	C21A	10325	-272.75
309	C21A	10395	-272.75
310	C21A	10465	-272.75
311	C21A	10535	-272.75
312	C21A	10605	-272.75
313	C21A	10675	-272.75
314	C21A	10745	-272.75
315	C21A	10815	-272.75
316	C21A	10885	-272.75
317	C21A	10955	-272.75
318	C21A	11025	-272.75
319	C21A	11095	-272.75
320	C21A	11165	-272.75
321	DUMMY	11205	137.25
322	DUMMY	11190	264.75
323	G1	11175	137.25
324	G3	11160	264.75
325	G5	11145	137.25
326	G7	11130	264.75
327	G9	11115	137.25
328	G11	11100	264.75
329	G13	11085	137.25
330	G15	11070	264.75
331	G17	11055	137.25
332	G19	11040	264.75
333	G21	11025	137.25
334	G23	11010	264.75
335	G25	10995	137.25
336	G27	10980	264.75
337	G29	10965	137.25
338	G31	10950	264.75
339	G33	10935	137.25
340	G35	10920	264.75
341	G37	10905	137.25
342	G39	10890	264.75
343	G41	10875	137.25
344	G43	10860	264.75
345	G45	10845	137.25
346	G47	10830	264.75
347	G49	10815	137.25
348	G51	10800	264.75
349	G53	10785	137.25
350	G55	10770	264.75

No.	Pad name	X	Y
351	G57	10755	137.2
352	G59	10740	264.7
353	G61	10725	137.2
354	G63	10710	264.7
355	G65	10695	137.2
356	G67	10680	264.7
357	G69	10665	137.2
358	G71	10650	264.7
359	G73	10635	137.2
360	G75	10620	264.7
361	G77	10605	137.2
362	G79	10590	264.7
363	G81	10575	137.2
364	G83	10560	264.7
365	G85	10545	137.2
366	G87	10530	264.7
367	G89	10515	137.2
368	G91	10500	264.7
369	G93	10485	137.2
370	G95	10470	264.7
371	G97	10455	137.2
372	G99	10440	264.7
373	G101	10425	137.2
374	G103	10410	264.7
375	G105	10395	137.2
376	G107	10380	264.7
377	G109	10365	137.2
378	G111	10350	264.7
379	G113	10335	137.2
380	G115	10320	264.7
381	G117	10305	137.2
382	G119	10290	264.7
383	G121	10275	137.2
384	G123	10260	264.7
385	G125	10245	137.2
386	G127	10230	264.7
387	G129	10215	137.2
388	G131	10200	264.7
389	G133	10185	137.2
390	G135	10170	264.7
391	G137	10155	137.2
392	G139	10140	264.7
393	G141	10125	137.2
394	G143	10110	264.7
395	G145	10095	137.2
396	G147	10080	264.7
397	G149	10065	137.2
398	G151	10050	264.7
399	G153	10035	137.2
400	G155	10020	264.7

No.	Pad name	X	Y
401	G157	10005	137.2
402	G159	9990	264.7
403	G161	9975	137.2
404	G163	9960	264.7
405	G165	9945	137.2
406	G167	9930	264.7
407	G169	9915	137.2
408	G171	9900	264.7
409	G173	9885	137.2
410	G175	9870	264.7
411	G177	9855	137.2
412	G179	9840	264.7
413	G181	9825	137.2
414	G183	9810	264.7
415	G185	9795	137.2
416	G187	9780	264.7
417	G189	9765	137.2
418	G191	9750	264.7
419	G193	9735	137.2
420	G195	9720	264.7
421	G197	9705	137.2
422	G199	9690	264.7
423	G201	9675	137.2
424	G203	9660	264.7
425	G205	9645	137.2
426	G207	9630	264.7
427	G209	9615	137.2
428	G211	9600	264.7
429	G213	9585	137.2
430	G215	9570	264.7
431	G217	9555	137.2
432	G219	9540	264.7
433	G221	9525	137.2
434	G223	9510	264.7
435	G225	9495	137.2
436	G227	9480	264.7
437	G229	9465	137.2
438	G231	9450	264.7
439	G233	9435	137.2
440	G235	9420	264.7
441	G237	9405	137.2
442	G239	9390	264.7
443	G241	9375	137.2
444	G243	9360	264.7
445	G245	9345	137.2
446	G247	9330	264.7
447	G249	9315	137.2
448	G251	9300	264.7
449	G253	9285	137.2
450	G255	9270	264.7

No.	Pad	X	Y
451	G257	9255	137.2
452	G259	9240	264.7
453	G261	9225	137.2
454	G263	9210	264.7
455	G265	9195	137.2
456	G267	9180	264.7
457	G269	9165	137.2
458	G271	9150	264.7
459	G273	9135	137.2
460	G275	9120	264.7
461	G277	9105	137.2
462	G264.7	9090	264.7
463	G281	9075	137.2
464	G283	9060	264.7
465	G285	9045	137.2
466	G287	9030	264.7
467	G272.7	9015	137.2
468	G291	9000	264.7
469	G293	8985	137.2
470	G295	8970	264.7
471	G297	8955	137.2
472	G299	8940	264.7
473	G301	8925	137.2
474	G303	8910	264.7
475	G305	8895	137.2
476	G307	8880	264.7
477	G309	8865	137.2
478	G311	8850	264.7
479	G313	8835	137.2
480	G315	8820	264.7
481	G317	8805	137.2
482	G319	8790	264.7
483	G321	8775	137.2
484	G323	8760	264.7
485	G325	8745	137.2
486	G327	8730	264.7
487	G329	8715	137.2
488	G331	8700	264.7
489	G333	8685	137.2
490	G335	8670	264.7
491	G337	8655	137.2
492	G339	8640	264.7
493	G341	8625	137.2
494	G343	8610	264.7
495	G345	8595	137.2
496	G347	8580	264.7
497	G349	8565	137.2
498	G351	8550	264.7
499	G353	8535	137.2
500	G355	8520	264.7

No.	Pad name	X	Y
501	G357	8505	137.2
502	G359	8490	264.7
503	G361	8475	137.2
504	G363	8460	264.7
505	G365	8445	137.2
506	G367	8430	264.7
507	G369	8415	137.2
508	G371	8400	264.7
509	G373	8385	137.2
510	G375	8370	264.7
511	G377	8355	137.2
512	G379	8340	264.7
513	G381	8325	137.2
514	G383	8310	264.7
515	G385	8295	137.2
516	G387	8280	264.7
517	G389	8265	137.2
518	G391	8250	264.7
519	G393	8235	137.2
520	G395	8220	264.7
521	G397	8205	137.2
522	G399	8190	264.7
523	G401	8175	137.2
524	G403	8160	264.7
525	G405	8145	137.2
526	G407	8130	264.7
527	G409	8115	137.2
528	G411	8100	264.7
529	G413	8085	137.2
530	G415	8070	264.7
531	G417	8055	137.2
532	G419	8040	264.7
533	G421	8025	137.2
534	G423	8010	264.7
535	G425	7995	137.2
536	G427	7980	264.7
537	G429	7965	137.2
538	G431	7950	264.7
539	G433	7935	137.2
540	G435	7920	264.7
541	G437	7905	137.2
542	G439	7890	264.7
543	G441	7875	137.2
544	G443	7860	264.7
545	G445	7845	137.2
546	G447	7830	264.7
547	G449	7815	137.2
548	G451	7800	264.7
549	G453	7785	137.2
550	G455	7770	264.7

No.	Pad name	X	Y
551	G457	7755	137.2
552	G459	7740	264.7
553	G461	7725	137.2
554	G463	7710	264.7
555	G465	7695	137.2
556	G467	7680	264.7
557	G469	7665	137.2
558	G471	7650	264.7
559	G473	7635	137.2
560	G475	7620	264.7
561	G477	7605	137.2
562	G479	7590	264.7
563	DUMMY	7575	137.2
564	DUMMY	7560	264.7
565	DUMMY	7395	137.2
566	S961	7380	264.7
567	S960	7365	137.2
568	S959	7350	264.7
569	S958	7335	137.2
570	S957	7320	264.7
571	S956	7305	137.2
572	S955	7290	264.7
573	S954	7275	137.2
574	S953	7260	264.7
575	S952	7245	137.2
576	S951	7230	264.7
577	S950	7215	137.2
578	S949	7200	264.7
579	S948	7185	137.2
580	S947	7170	264.7
581	S946	7155	137.2
582	S945	7140	264.7
583	S944	7125	137.2
584	S943	7110	264.7
585	S942	7095	137.2
586	S941	7080	264.7
587	S940	7065	137.2
588	S939	7050	264.7
589	S938	7035	137.2
590	S937	7020	264.7
591	S936	7005	137.2
592	S935	6990	264.7
593	S934	6975	137.2
594	S933	6960	264.7
595	S932	6945	137.2
596	S931	6930	264.7
597	S930	6915	137.2
598	S929	6900	264.7
599	S928	6885	137.2
600	S927	6870	264.7

No.	Pad name	X	Y
601	S926	6855	137.2
602	S925	6840	264.7
603	S924	6825	137.2
604	S923	6810	264.7
605	S922	6795	137.2
606	S921	6780	264.7
607	S920	6765	137.2
608	S919	6750	264.7
609	S918	6735	137.2
610	S917	6720	264.7
611	S916	6705	137.2
612	S915	6690	264.7
613	S914	6675	137.2
614	S913	6660	264.7
615	S912	6645	137.2
616	S911	6630	264.7
617	S910	6615	137.2
618	S909	6600	264.7
619	S908	6585	137.2
620	S907	6570	264.7
621	S906	6555	137.2
622	S905	6540	264.7
623	S904	6525	137.2
624	S903	6510	264.7
625	S902	6495	137.2
626	S901	6480	264.7
627	S900	6465	137.2
628	S899	6450	264.7
629	S898	6435	137.2
630	S897	6420	264.7
631	S896	6405	137.2
632	S895	6390	264.7
633	S894	6375	137.2
634	S893	6360	264.7
635	S892	6345	137.2
636	S891	6330	264.7
637	S890	6315	137.2
638	S889	6300	264.7
639	S888	6285	137.2
640	S887	6270	264.7
641	S886	6255	137.2
642	S885	6240	264.7
643	S884	6225	137.2
644	S883	6210	264.7
645	S882	6195	137.2
646	S881	6180	264.7
647	S880	6165	137.2
648	S879	6150	264.7
649	S878	6135	137.2
650	S877	6120	264.7

No.	Pad	X	Y
651	S876	6105	137.2
652	S875	6090	264.7
653	S874	6075	137.2
654	S873	6060	264.7
655	S872	6045	137.2
656	S871	6030	264.7
657	S870	6015	137.2
658	S869	6000	264.7
659	S868	5985	137.2
660	S867	5970	264.7
661	S866	5955	137.2
662	S865	5940	264.7
663	S864	5925	137.2
664	S863	5910	264.7
665	S862	5895	137.2
666	S861	5880	264.7
667	S860	5865	137.2
668	S859	5850	264.7
669	S858	5835	137.2
670	S857	5820	264.7
671	S856	5805	137.2
672	S855	5790	264.7
673	S854	5775	137.2
674	S853	5760	264.7
675	S852	5745	137.2
676	S851	5730	264.7
677	S850	5715	137.2
678	S849	5700	264.7
679	S848	5685	137.2
680	S847	5670	264.7
681	S846	5655	137.2
682	S845	5640	264.7
683	S844	5625	137.2
684	S843	5610	264.7
685	S842	5595	137.2
686	S841	5580	264.7
687	S840	5565	137.2
688	S839	5550	264.7
689	S838	5535	137.2
690	S837	5520	264.7
691	S836	5505	137.2
692	S835	5490	264.7
693	S834	5475	137.2
694	S833	5460	264.7
695	S832	5445	137.2
696	S831	5430	264.7
697	S830	5415	137.2
698	S829	5400	264.7
699	S828	5385	137.2
700	S827	5370	264.7

No.	Pad name	X	Y
701	S826	5355	137.2
702	S825	5340	264.7
703	S824	5325	137.2
704	S823	5310	264.7
705	S822	5295	137.2
706	S821	5280	264.7
707	S820	5265	137.2
708	S819	5250	264.7
709	S818	5235	137.2
710	S817	5220	264.7
711	S816	5205	137.2
712	S815	5190	264.7
713	S814	5175	137.2
714	S813	5160	264.7
715	S812	5145	137.2
716	S811	5130	264.7
717	S810	5115	137.2
718	S809	5100	264.7
719	S808	5085	137.2
720	S807	5070	264.7
721	S806	5055	137.2
722	S805	5040	264.7
723	S804	5025	137.2
724	S803	5010	264.7
725	S802	4995	137.2
726	S801	4980	264.7
727	S800	4965	137.2
728	S799	4950	264.7
729	S798	4935	137.2
730	S797	4920	264.7
731	S796	4905	137.2
732	S795	4890	264.7
733	S794	4875	137.2
734	S793	4860	264.7
735	S792	4845	137.2
736	S791	4830	264.7
737	S790	4815	137.2
738	S789	4800	264.7
739	S788	4785	137.2
740	S787	4770	264.7
741	S786	4755	137.2
742	S785	4740	264.7
743	S784	4725	137.2
744	S783	4710	264.7
745	S782	4695	137.2
746	S781	4680	264.7
747	S780	4665	137.2
748	S779	4650	264.7
749	S778	4635	137.2
750	S777	4620	264.7

No.	Pad name	X	Y
751	S776	4605	137.2
752	S775	4590	264.7
753	S774	4575	137.2
754	S773	4560	264.7
755	S772	4545	137.2
756	S771	4530	264.7
757	S770	4515	137.2
758	S769	4500	264.7
759	S768	4485	137.2
760	S767	4470	264.7
761	S766	4455	137.2
762	S765	4440	264.7
763	S764	4425	137.2
764	S763	4410	264.7
765	S762	4395	137.2
766	S761	4380	264.7
767	S760	4365	137.2
768	S759	4350	264.7
769	S758	4335	137.2
770	S757	4320	264.7
771	S756	4305	137.2
772	S755	4290	264.7
773	S754	4275	137.2
774	S753	4260	264.7
775	S752	4245	137.2
776	S751	4230	264.7
777	S750	4215	137.2
778	S749	4200	264.7
779	S748	4185	137.2
780	S747	4170	264.7
781	S746	4155	137.2
782	S745	4140	264.7
783	S744	4125	137.2
784	S743	4110	264.7
785	S742	4095	137.2
786	S741	4080	264.7
787	S740	4065	137.2
788	S739	4050	264.7
789	S738	4035	137.2
790	S737	4020	264.7
791	S736	4005	137.2
792	S735	3990	264.7
793	S734	3975	137.2
794	S733	3960	264.7
795	S732	3945	137.2
796	S731	3930	264.7
797	S730	3915	137.2
798	S729	3900	264.7
799	S728	3885	137.2
800	S727	3870	264.7

No.	Pad name	X	Y
801	S726	3855	137.2
802	S725	3840	264.7
803	S724	3825	137.2
804	S723	3810	264.7
805	S722	3795	137.2
806	S721	3780	264.7
807	S720	3765	137.2
808	S719	3750	264.7
809	S718	3735	137.2
810	S717	3720	264.7
811	S716	3705	137.2
812	S715	3690	264.7
813	S714	3675	137.2
814	S713	3660	264.7
815	S712	3645	137.2
816	S711	3630	264.7
817	S710	3615	137.2
818	S709	3600	264.7
819	S708	3585	137.2
820	S707	3570	264.7
821	S706	3555	137.2
822	S705	3540	264.7
823	S704	3525	137.2
824	S703	3510	264.7
825	S702	3495	137.2
826	S701	3480	264.7
827	S700	3465	137.2
828	S699	3450	264.7
829	S698	3435	137.2
830	S697	3420	264.7
831	S696	3405	137.2
832	S695	3390	264.7
833	S694	3375	137.2
834	S693	3360	264.7
835	S692	3345	137.2
836	S691	3330	264.7
837	S690	3315	137.2
838	S689	3300	264.7
839	S688	3285	137.2
840	S687	3270	264.7
841	S686	3255	137.2
842	S685	3240	264.7
843	S684	3225	137.2
844	S683	3210	264.7
845	S682	3195	137.2
846	S681	3180	264.7
847	S680	3165	137.2
848	S679	3150	264.7
849	S678	3135	137.2
850	S677	3120	264.7

No.	Pad	X	Y
851	S676	3105	137.2
852	S675	3090	264.7
853	S674	3075	137.2
854	S673	3060	264.7
855	S672	3045	137.2
856	S671	3030	264.7
857	S670	3015	137.2
858	S669	3000	264.7
859	S668	2985	137.2
860	S667	2970	264.7
861	S666	2955	137.2
862	S665	2940	264.7
863	S664	2925	137.2
864	S663	2910	264.7
865	S662	272.755	137.2
866	S661	2880	264.7
867	S660	2865	137.2
868	S659	2850	264.7
869	S658	2835	137.2
870	S657	2820	264.7
871	S656	2805	137.2
872	S655	264.750	264.7
873	S654	2775	137.2
874	S653	2760	264.7
875	S652	2745	137.2
876	S651	2730	264.7
877	S650	2715	137.2
878	S649	2700	264.7
879	S648	2685	137.2
880	S647	2670	264.7
881	S646	2655	137.2
882	S645	2640	264.7
883	S644	2625	137.2
884	S643	2610	264.7
885	S642	2595	137.2
886	S641	2580	264.7
887	S640	2565	137.2
888	S639	2550	264.7
889	S638	2535	137.2
890	S637	2520	264.7
891	S636	2505	137.2
892	S635	2490	264.7
893	S634	2475	137.2
894	S633	2460	264.7
895	S632	2445	137.2
896	S631	2430	264.7
897	S630	2415	137.2
898	S629	2400	264.7
899	S628	2385	137.2
900	S627	2370	264.7

No.	Pad name	X	Y
901	S626	2355	137.2
902	S625	2340	264.7
903	S624	2325	137.2
904	S623	2310	264.7
905	S622	2295	137.2
906	S621	2280	264.7
907	S620	2265	137.2
908	S619	2250	264.7
909	S618	2235	137.2
910	S617	2220	264.7
911	S616	2205	137.2
912	S615	2190	264.7
913	S614	2175	137.2
914	S613	2160	264.7
915	S612	2145	137.2
916	S611	2130	264.7
917	S610	2115	137.2
918	S609	2100	264.7
919	S608	2085	137.2
920	S607	2070	264.7
921	S606	2055	137.2
922	S605	2040	264.7
923	S604	2025	137.2
924	S603	2010	264.7
925	S602	1995	137.2
926	S601	1980	264.7
927	S600	1965	137.2
928	S599	1950	264.7
929	S598	1935	137.2
930	S597	1920	264.7
931	S596	1905	137.2
932	S595	1890	264.7
933	S594	1875	137.2
934	S593	1860	264.7
935	S592	1845	137.2
936	S591	1830	264.7
937	S590	1815	137.2
938	S589	1800	264.7
939	S588	1785	137.2
940	S587	1770	264.7
941	S586	1755	137.2
942	S585	1740	264.7
943	S584	1725	137.2
944	S583	1710	264.7
945	S582	1695	137.2
946	S581	1680	264.7
947	S580	1665	137.2
948	S579	1650	264.7
949	S578	1635	137.2
950	S577	1620	264.7

No.	Pad name	X	Y
951	S576	1605	137.2
952	S575	1590	264.7
953	S574	1575	137.2
954	S573	1560	264.7
955	S572	137.2	137.2
956	S571	1530	264.7
957	S570	1515	137.2
958	S569	1500	264.7
959	S568	1485	137.2
960	S567	1470	264.7
961	S566	1455	137.2
962	S565	1440	264.7
963	S564	1425	137.2
964	S563	1410	264.7
965	S562	1395	137.2
966	S561	1380	264.7
967	S560	1365	137.2
968	S559	1350	264.7
969	S558	1335	137.2
970	S557	1320	264.7
971	S556	1305	137.2
972	S555	1290	264.7
973	S554	1275	137.2
974	S553	1260	264.7
975	S552	1245	137.2
976	S551	1230	264.7
977	S550	1215	137.2
978	S549	1200	264.7
979	S548	1185	137.2
980	S547	1170	264.7
981	S546	1155	137.2
982	S545	1140	264.7
983	S544	1125	137.2
984	S543	1110	264.7
985	S542	1095	137.2
986	S541	1080	264.7
987	S540	1065	137.2
988	S539	1050	264.7
989	S538	1035	137.2
990	S537	1020	264.7
991	S536	1005	137.2
992	S535	990	264.7
993	S534	975	137.2
994	S533	960	264.7
995	S532	945	137.2
996	S531	930	264.7
997	S530	915	137.2
998	S529	900	264.7
999	S528	885	137.2
1000	S527	870	264.7

No.	Pad name	X	Y
1001	S526	855	137.2
1002	S525	840	264.7
1003	S524	825	137.2
1004	S523	810	264.7
1005	S522	795	137.2
1006	S521	780	264.7
1007	S520	765	137.2
1008	S519	750	264.7
1009	S518	735	137.2
1010	S517	720	264.7
1011	S516	705	137.2
1012	S515	690	264.7
1013	S514	675	137.2
1014	S513	660	264.7
1015	S512	645	137.2
1016	S511	630	264.7
1017	S510	615	137.2
1018	S509	600	264.7
1019	S508	585	137.2
1020	S507	570	264.7
1021	S506	555	137.2
1022	S505	540	264.7
1023	S504	525	137.2
1024	S503	510	264.7
1025	S502	495	137.2
1026	S501	480	264.7
1027	S500	465	137.2
1028	S499	450	264.7
1029	S498	435	137.2
1030	S497	420	264.7
1031	S496	405	137.2
1032	S495	390	264.7
1033	S494	375	137.2
1034	S493	360	264.7
1035	S492	345	137.2
1036	S491	330	264.7
1037	S490	315	137.2
1038	S489	300	264.7
1039	S488	285	137.2
1040	S487	270	264.7
1041	S486	255	137.2
1042	S485	240	264.7
1043	S484	225	137.2
1044	S483	210	264.7
1045	S482	195	137.2
1046	S481	180	264.7
1047	DUMMY	165	137.2
1048	DUMMY	150	264.7
1049	DUMMY	-150	264.7
1050	DUMMY	-165	137.2

No.	Pad	X	Y
1051	S480	-180	264.7
1052	S479	-195	137.2
1053	S478	-210	264.7
1054	S477	-225	137.2
1055	S476	-240	264.7
1056	S475	-255	137.2
1057	S474	-270	264.7
1058	S473	-285	137.2
1059	S472	-300	264.7
1060	S471	-315	137.2
1061	S470	-330	264.7
1062	S469	-345	137.2
1063	S468	-360	264.7
1064	S467	-375	137.2
1065	S466	-390	264.7
1066	S465	-405	137.2
1067	S464	-420	264.7
1068	S463	-435	137.2
1069	S462	-450	264.7
1070	S461	-465	137.2
1071	S460	-480	264.7
1072	S459	-495	137.2
1073	S458	-510	264.7
1074	S457	-525	137.2
1075	S456	-540	264.7
1076	S455	-555	137.2
1077	S454	-570	264.7
1078	S453	-585	137.2
1079	S452	-600	264.7
1080	S451	-615	137.2
1081	S450	-630	264.7
1082	S449	-645	137.2
1083	S448	-660	264.7
1084	S447	-675	137.2
1085	S446	-690	264.7
1086	S445	-705	137.2
1087	S444	-720	264.7
1088	S443	-735	137.2
1089	S442	-750	264.7
1090	S441	-765	137.2
1091	S440	-780	264.7
1092	S439	-795	137.2
1093	S438	-810	264.7
1094	S437	-825	137.2
1095	S436	-840	264.7
1096	S435	-855	137.2
1097	S434	-870	264.7
1098	S433	-885	137.2
1099	S432	-900	264.7
1100	S431	-915	137.2

No.	Pad name	X	Y
1101	S430	-930	264.7
1102	S429	-945	137.2
1103	S428	-960	264.7
1104	S427	-975	137.2
1105	S426	-990	264.7
1106	S425	-1005	137.2
1107	S424	-1020	264.7
1108	S423	-1035	137.2
1109	S422	-1050	264.7
1110	S421	-1065	137.2
1111	S420	-1080	264.7
1112	S419	-1095	137.2
1113	S418	-1110	264.7
1114	S417	-1125	137.2
1115	S416	-1140	264.7
1116	S415	-1155	137.2
1117	S414	-1170	264.7
1118	S413	-1185	137.2
1119	S412	-1200	264.7
1120	S411	-1215	137.2
1121	S410	-1230	264.7
1122	S409	-1245	137.2
1123	S408	-1260	264.7
1124	S407	-1275	137.2
1125	S406	-1290	264.7
1126	S405	-1305	137.2
1127	S404	-1320	264.7
1128	S403	-1335	137.2
1129	S402	-1350	264.7
1130	S401	-1365	137.2
1131	S400	-1380	264.7
1132	S399	-1395	137.2
1133	S398	-1410	264.7
1134	S397	-1425	137.2
1135	S396	-1440	264.7
1136	S395	-1455	137.2
1137	S394	-1470	264.7
1138	S393	-1485	137.2
1139	S392	-1500	264.7
1140	S391	-1515	137.2
1141	S390	-1530	264.7
1142	S389	-137.255	137.2
1143	S388	-1560	264.7
1144	S387	-1575	137.2
1145	S386	-1590	264.7
1146	S385	-1605	137.2
1147	S384	-1620	264.7
1148	S383	-1635	137.2
1149	S382	-1650	264.7
1150	S381	-1665	137.2

No.	Pad name	X	Y
1151	S380	-1680	264.7
1152	S379	-1695	137.2
1153	S378	-1710	264.7
1137.	S377	-1725	137.2
1155	S376	-1740	264.7
1156	S375	-1755	137.2
1157	S374	-1770	264.7
1158	S373	-1785	137.2
1159	S372	-1800	264.7
1160	S371	-1815	137.2
1161	S370	-1830	264.7
1162	S369	-1845	137.2
1163	S368	-1860	264.7
1164	S367	-1875	137.2
1165	S366	-1890	264.7
1166	S365	-1905	137.2
1167	S364	-1920	264.7
1168	S363	-1935	137.2
1169	S362	-1950	264.7
1170	S361	-1965	137.2
1171	S360	-1980	264.7
1172	S359	-1995	137.2
1173	S358	-2010	264.7
1174	S357	-2025	137.2
1175	S356	-2040	264.7
1176	S355	-2055	137.2
1177	S354	-2070	264.7
1178	S353	-2085	137.2
1179	S352	-2100	264.7
1180	S351	-2115	137.2
1181	S350	-2130	264.7
1182	S349	-2145	137.2
1183	S348	-2160	264.7
1184	S347	-2175	137.2
1185	S346	-2190	264.7
1186	S345	-2205	137.2
1187	S344	-2220	264.7
1188	S343	-2235	137.2
1189	S342	-2250	264.7
1190	S341	-2265	137.2
1191	S340	-2280	264.7
1192	S339	-2295	137.2
1193	S338	-2310	264.7
1194	S337	-2325	137.2
1195	S336	-2340	264.7
1196	S335	-2355	137.2
1197	S334	-2370	264.7
1198	S333	-2385	137.2
1199	S332	-2400	264.7
1200	S331	-2415	137.2

No.	Pad name	X	Y
1201	S330	-2430	264.7
1202	S329	-2445	137.2
1203	S328	-2460	264.7
1204	S327	-2475	137.2
1205	S326	-2490	264.7
1206	S325	-2505	137.2
1207	S324	-2520	264.7
1208	S323	-2535	137.2
1209	S322	-2550	264.7
1210	S321	-2565	137.2
1211	S320	-2580	264.7
1212	S319	-2595	137.2
1213	S318	-2610	264.7
1214	S317	-2625	137.2
1215	S316	-2640	264.7
1216	S315	-2655	137.2
1217	S314	-2670	264.7
1218	S313	-2685	137.2
1219	S312	-2700	264.7
1220	S311	-2715	137.2
1221	S310	-2730	264.7
1222	S309	-2745	137.2
1223	S308	-2760	264.7
1224	S307	-2775	137.2
1225	S306	-264.7	264.7
1226	S305	-2805	137.2
1227	S304	-2820	264.7
1228	S303	-2835	137.2
1229	S302	-2850	264.7
1230	S301	-2865	137.2
1231	S300	-2880	264.7
1232	S299	-272.7	137.2
1233	S298	-2910	264.7
1234	S297	-2925	137.2
1235	S296	-2940	264.7
1236	S295	-2955	137.2
1237	S294	-2970	264.7
1238	S293	-2985	137.2
1239	S292	-3000	264.7
1240	S291	-3015	137.2
1241	S290	-3030	264.7
1242	S272.75	-3045	137.2
1243	S288	-3060	264.7
1244	S287	-3075	137.2
1245	S286	-3090	264.7
1246	S285	-3105	137.2
1247	S284	-3120	264.7
1248	S283	-3135	137.2
1249	S282	-3150	264.7
1250	S281	-3165	137.2

No.	Pad name	X	Y
1251	S280	-318	264.7
1252	S264.75	-319	137.2
1253	S278	-321	264.7
1254	S277	-322	137.2
1255	S276	-324	264.7
1256	S275	-325	137.2
1257	S274	-327	264.7
1258	S273	-328	137.2
1259	S272	-330	264.7
1260	S271	-331	137.2
1261	S270	-333	264.7
1262	S269	-334	137.2
1263	S268	-336	264.7
1264	S267	-337	137.2
1265	S266	-339	264.7
1266	S265	-340	137.2
1267	S264	-342	264.7
1268	S263	-343	137.2
1269	S262	-345	264.7
1270	S261	-346	137.2
1271	S260	-348	264.7
1272	S259	-349	137.2
1273	S258	-351	264.7
1274	S257	-352	137.2
1275	S256	-354	264.7
1276	S255	-355	137.2
1277	S254	-357	264.7
1278	S253	-358	137.2
1264	S252	-360	264.7
1280	S251	-361	137.2
1281	S250	-363	264.7
1282	S249	-364	137.2
1283	S248	-366	264.7
1284	S247	-367	137.2
1285	S246	-369	264.7
1286	S245	-370	137.2
1287	S244	-372	264.7
1288	S243	-373	137.2
1272	S242	-375	264.7
1290	S241	-376	137.2
1291	S240	-378	264.7
1292	S239	-379	137.2
1293	S238	-381	264.7
1294	S237	-382	137.2
1295	S236	-384	264.7
1296	S235	-385	137.2
1297	S234	-387	264.7
1298	S233	-388	137.2
1299	S232	-390	264.7
1300	S231	-391	137.2

No.	Pad name	X	Y
1301	S230	-3930	264.7
1302	S229	-3945	137.2
1303	S228	-3960	264.7
1304	S227	-3975	137.2
1305	S226	-3990	264.7
1306	S225	-4005	137.2
1307	S224	-4020	264.7
1308	S223	-4035	137.2
1309	S222	-4050	264.7
1310	S221	-4065	137.2
1311	S220	-4080	264.7
1312	S219	-4095	137.2
1313	S218	-4110	264.7
1314	S217	-4125	137.2
1315	S216	-4140	264.7
1316	S215	-4155	137.2
1317	S214	-4170	264.7
1318	S213	-4185	137.2
1319	S212	-4200	264.7
1320	S211	-4215	137.2
1321	S210	-4230	264.7
1322	S209	-4245	137.2
1323	S208	-4260	264.7
1324	S207	-4275	137.2
1325	S206	-4290	264.7
1326	S205	-4305	137.2
1327	S204	-4320	264.7
1328	S203	-4335	137.2
1329	S202	-4350	264.7
1330	S201	-4365	137.2
1331	S200	-4380	264.7
1332	S199	-4395	137.2
1333	S198	-4410	264.7
1334	S197	-4425	137.2
1335	S196	-4440	264.7
1336	S195	-4455	137.2
1337	S194	-4470	264.7
1338	S193	-4485	137.2
1339	S192	-4500	264.7
1340	S191	-4515	137.2
1341	S190	-4530	264.7
1342	S189	-4545	137.2
1343	S188	-4560	264.7
1344	S187	-4575	137.2
1345	S186	-4590	264.7
1346	S185	-4605	137.2
1347	S184	-4620	264.7
1348	S183	-4635	137.2
1349	S182	-4650	264.7
1350	S181	-4665	137.2

No.	Pad name	X	Y
1351	S180	-4680	264.7
1352	S179	-4695	137.2
1353	S178	-4710	264.7
1354	S177	-4725	137.2
1355	S176	-4740	264.7
1356	S175	-4755	137.2
1357	S174	-4770	264.7
1358	S173	-4785	137.2
1359	S172	-4800	264.7
1360	S171	-4815	137.2
1361	S170	-4830	264.7
1362	S169	-4845	137.2
1363	S168	-4860	264.7
1364	S167	-4875	137.2
1365	S166	-4890	264.7
1366	S165	-4905	137.2
1367	S164	-4920	264.7
1368	S163	-4935	137.2
1369	S162	-4950	264.7
1370	S161	-4965	137.2
1371	S160	-4980	264.7
1372	S159	-4995	137.2
1373	S158	-5010	264.7
1374	S157	-5025	137.2
1375	S156	-5040	264.7
1376	S155	-5055	137.2
1377	S137.25	-5070	264.7
1378	S153	-5085	137.2
1379	S152	-5100	264.7
1380	S151	-5115	137.2
1381	S150	-5130	264.7
1382	S149	-5145	137.2
1383	S148	-5160	264.7
1384	S147	-5175	137.2
1385	S146	-5190	264.7
1386	S145	-5205	137.2
1387	S144	-5220	264.7
1388	S143	-5235	137.2
1389	S142	-5250	264.7
1390	S141	-5265	137.2
1391	S140	-5280	264.7
1392	S139	-5295	137.2
1393	S138	-5310	264.7
1394	S137	-5325	137.2
1395	S136	-5340	264.7
1396	S135	-5355	137.2
1397	S134	-5370	264.7
1398	S133	-5385	137.2
1399	S132	-5400	264.7
1400	S131	-5415	137.2

No.	Pad name	X	Y
1401	S130	-5430	264.7
1402	S129	-5445	137.2
1403	S128	-5460	264.7
1404	S127	-5475	137.2
1405	S126	-5490	264.7
1406	S125	-5505	137.2
1407	S124	-5520	264.7
1408	S123	-5535	137.2
1409	S122	-5550	264.7
1410	S121	-5565	137.2
1411	S120	-5580	264.7
1412	S119	-5595	137.2
1413	S118	-5610	264.7
1414	S117	-5625	137.2
1415	S116	-5640	264.7
1416	S115	-5655	137.2
1417	S114	-5670	264.7
1418	S113	-5685	137.2
1419	S112	-5700	264.7
1420	S111	-5715	137.2
1421	S110	-5730	264.7
1422	S109	-5745	137.2
1423	S108	-5760	264.7
1424	S107	-5775	137.2
1425	S106	-5790	264.7
1426	S105	-5805	137.2
1427	S104	-5820	264.7
1428	S103	-5835	137.2
1429	S102	-5850	264.7
1430	S101	-5865	137.2
1431	S100	-5880	264.7
1432	S99	-5895	137.2
1433	S98	-5910	264.7
1434	S97	-5925	137.2
1435	S96	-5940	264.7
1436	S95	-5955	137.2
1437	S94	-5970	264.7
1438	S93	-5985	137.2
1439	S92	-6000	264.7
1440	S91	-6015	137.2
1441	S90	-6030	264.7
1442	S89	-6045	137.2
1443	S88	-6060	264.7
1444	S87	-6075	137.2
1445	S86	-6090	264.7
1446	S85	-6105	137.2
1447	S84	-6120	264.7
1448	S83	-6135	137.2
1449	S82	-6150	264.7
1450	S81	-6165	137.2

No.	Pad name	X	Y
1451	S80	-618	264.7
1452	S79	-619	137.2
1453	S78	-621	264.7
1454	S77	-622	137.2
1455	S76	-624	264.7
1456	S75	-625	137.2
1457	S74	-627	264.7
1458	S73	-628	137.2
1459	S72	-630	264.7
1460	S71	-631	137.2
1461	S70	-633	264.7
1462	S69	-634	137.2
1463	S68	-636	264.7
1464	S67	-637	137.2
1465	S66	-639	264.7
1466	S65	-640	137.2
1467	S64	-642	264.7
1468	S63	-643	137.2
1469	S62	-645	264.7
1470	S61	-646	137.2
1471	S60	-648	264.7
1472	S59	-649	137.2
1473	S58	-651	264.7
1474	S57	-652	137.2
1475	S56	-654	264.7
1476	S55	-655	137.2
1477	S54	-657	264.7
1478	S53	-658	137.2
1479	S52	-660	264.7
1480	S51	-661	137.2
1481	S50	-663	264.7
1482	S49	-664	137.2
1483	S48	-666	264.7
1484	S47	-667	137.2
1485	S46	-669	264.7
1486	S45	-670	137.2
1487	S44	-672	264.7
1488	S43	-673	137.2
1489	S42	-675	264.7
1490	S41	-676	137.2
1491	S40	-678	264.7
1492	S39	-679	137.2
1493	S38	-681	264.7
1494	S37	-682	137.2
1495	S36	-684	264.7
1496	S35	-685	137.2
1497	S34	-687	264.7
1498	S33	-688	137.2
1499	S32	-690	264.7
1500	S31	-691	137.2

No.	Pad name	X	Y
1501	S30	-6930	264.7
1502	S29	-6945	137.2
1503	S28	-6960	264.7
1504	S27	-6975	137.2
1505	S26	-6990	264.7
1506	S25	-7005	137.2
1507	S24	-7020	264.7
1508	S23	-7035	137.2
1509	S22	-7050	264.7
1510	S21	-7065	137.2
1511	S20	-7080	264.7
1512	S19	-7095	137.2
1513	S18	-7110	264.7
1514	S17	-7125	137.2
1515	S16	-7140	264.7
1516	S15	-7155	137.2
1517	S14	-7170	264.7
1518	S13	-7185	137.2
1519	S12	-7200	264.7
1520	S11	-7215	137.2
1521	S10	-7230	264.7
1522	S9	-7245	137.2
1523	S8	-7260	264.7
1524	S7	-7275	137.2
1525	S6	-7290	264.7
1526	S5	-7305	137.2
1527	S4	-7320	264.7
1528	S3	-7335	137.2
1529	S2	-7350	264.7
1530	S1	-7365	137.2
1531	DUMMY	-7380	264.7
1532	DUMMY	-7395	137.2
1533	DUMMY	-7560	264.7
1534	DUMMY	-7575	137.2
1535	G480	-7590	264.7
1536	G478	-7605	137.2
1537	G476	-7620	264.7
1538	G474	-7635	137.2
1539	G472	-7650	264.7
137.25	G470	-7665	137.2
137.25	G468	-7680	264.7
137.25	G466	-7695	137.2
137.25	G464	-7710	264.7
137.25	G462	-7725	137.2
137.25	G460	-7740	264.7
137.25	G458	-7755	137.2
137.25	G456	-7770	264.7
137.25	G454	-7785	137.2
137.25	G452	-7800	264.7
1550	G450	-7815	137.2

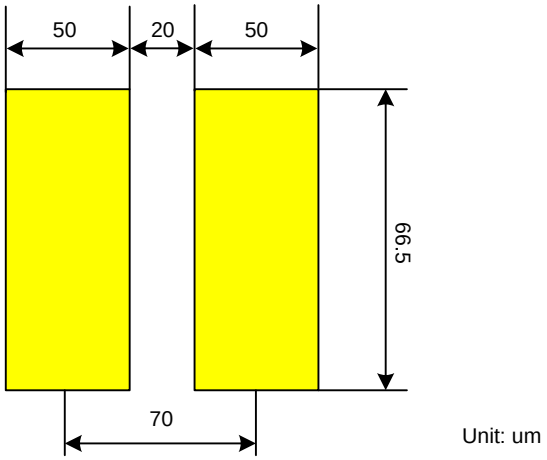
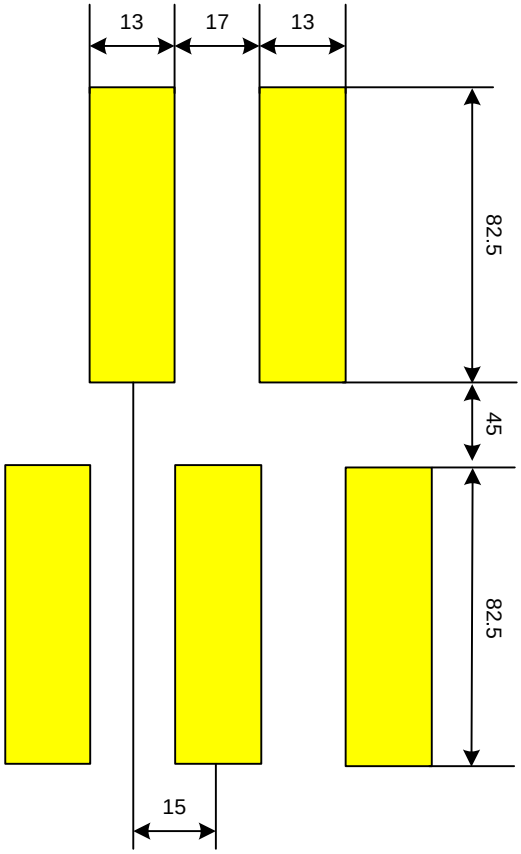
No.	Pad name	X	Y
1551	G448	-7830	264.7
1552	G446	-7845	137.2
1553	G444	-7860	264.7
1554	G442	-7875	137.2
1555	G440	-7890	264.7
1556	G438	-7905	137.2
1557	G436	-7920	264.7
1558	G434	-7935	137.2
1559	G432	-7950	264.7
1560	G430	-7965	137.2
1561	G428	-7980	264.7
1562	G426	-7995	137.2
1563	G424	-8010	264.7
1564	G422	-8025	137.2
1565	G420	-8040	264.7
1566	G418	-8055	137.2
1567	G416	-8070	264.7
1568	G414	-8085	137.2
1569	G412	-8100	264.7
1570	G410	-8115	137.2
1571	G408	-8130	264.7
1572	G406	-8145	137.2
1573	G404	-8160	264.7
1574	G402	-8175	137.2
1575	G400	-8190	264.7
1576	G398	-8205	137.2
1577	G396	-8220	264.7
1578	G394	-8235	137.2
1579	G392	-8250	264.7
1580	G390	-8265	137.2
1581	G388	-8280	264.7
1582	G386	-8295	137.2
1583	G384	-8310	264.7
1584	G382	-8325	137.2
1585	G380	-8340	264.7
1586	G378	-8355	137.2
1587	G376	-8370	264.7
1588	G374	-8385	137.2
1589	G372	-8400	264.7
1590	G370	-8415	137.2
1591	G368	-8430	264.7
1592	G366	-8445	137.2
1593	G364	-8460	264.7
1594	G362	-8475	137.2
1595	G360	-8490	264.7
1596	G358	-8505	137.2
1597	G356	-8520	264.7
1598	G354	-8535	137.2
1599	G352	-8550	264.7
1600	G350	-8565	137.2

No.	Pad name	X	Y
1601	G348	-8580	264.7
1602	G346	-8595	137.2
1603	G344	-8610	264.7
1604	G342	-8625	137.2
1605	G340	-8640	264.7
1606	G338	-8655	137.2
1607	G336	-8670	264.7
1608	G334	-8685	137.2
1609	G332	-8700	264.7
1610	G330	-8715	137.2
1611	G328	-8730	264.7
1612	G326	-8745	137.2
1613	G324	-8760	264.7
1614	G322	-8775	137.2
1615	G320	-8790	264.7
1616	G318	-8805	137.2
1617	G316	-8820	264.7
1618	G314	-8835	137.2
1619	G312	-8850	264.7
1620	G310	-8865	137.2
1621	G308	-8880	264.7
1622	G306	-8895	137.2
1623	G304	-8910	264.7
1624	G302	-8925	137.2
1625	G300	-8940	264.7
1626	G298	-8955	137.2
1627	G296	-8970	264.7
1628	G294	-8985	137.2
1629	G292	-9000	264.7
1630	G290	-9015	137.2
1631	G288	-9030	264.7
1632	G286	-9045	137.2
1633	G284	-9060	264.7
1634	G282	-9075	137.2
1635	G280	-9090	264.7
1636	G278	-9105	137.2
1637	G276	-9120	264.7
1638	G274	-9135	137.2
1639	G272	-9150	264.7
1640	G270	-9165	137.2
1641	G268	-9180	264.7
1642	G266	-9195	137.2
1643	G264	-9210	264.7
1644	G262	-9225	137.2
1645	G260	-9240	264.7
1646	G258	-9255	137.2
1647	G256	-9270	264.7
1648	G254	-9285	137.2
1649	G252	-9300	264.7
1650	G250	-9315	137.2

No.	Pad name	X	Y
1651	G248	-9330	264.7
1652	G246	-9345	137.2
1653	G244	-9360	264.7
1654	G242	-9375	137.2
1655	G240	-9390	264.7
1656	G238	-9405	137.2
1657	G236	-9420	264.7
1658	G234	-9435	137.2
1659	G232	-9450	264.7
1660	G230	-9465	137.2
1661	G228	-9480	264.7
1662	G226	-9495	137.2
1663	G224	-9510	264.7
1664	G222	-9525	137.2
1665	G220	-9540	264.7
1666	G218	-9555	137.2
1667	G216	-9570	264.7
1668	G214	-9585	137.2
1669	G212	-9600	264.7
1670	G210	-9615	137.2
1671	G208	-9630	264.7
1672	G206	-9645	137.2
1673	G204	-9660	264.7
1674	G202	-9675	137.2
1675	G200	-9690	264.7
1676	G198	-9705	137.2
1677	G196	-9720	264.7
1678	G194	-9735	137.2
1679	G192	-9750	264.7
1680	G190	-9765	137.2
1681	G188	-9780	264.7
1682	G186	-9795	137.2
1683	G184	-9810	264.7
1684	G182	-9825	137.2
1685	G180	-9840	264.7
1686	G178	-9855	137.2
1687	G176	-9870	264.7
1688	G174	-9885	137.2
1689	G172	-9900	264.7
1690	G170	-9915	137.2
1691	G168	-9930	264.7
1692	G166	-9945	137.2
1693	G164	-9960	264.7
1694	G162	-9975	137.2
1695	G160	-9990	264.7
1696	G158	-10005	137.2
1697	G156	-10020	264.7
1698	G137.25	-10035	137.2
1699	G152	-10050	264.7
1700	G150	-10065	137.2

No.	Pad name	X	Y
1701	G148	-10080	264.7
1702	G146	-10095	137.2
1703	G144	-10110	264.7
1704	G142	-10125	137.2
1705	G140	-10140	264.7
1706	G138	-10155	137.2
1707	G136	-10170	264.7
1708	G134	-10185	137.2
1709	G132	-10200	264.7
1710	G130	-10215	137.2
1711	G128	-10230	264.7
1712	G126	-10245	137.2
1713	G124	-10260	264.7
1714	G122	-10275	137.2
1715	G120	-10290	264.7
1716	G118	-10305	137.2
1717	G116	-10320	264.7
1718	G114	-10335	137.2
1719	G112	-10350	264.7
1720	G110	-10365	137.2
1721	G108	-10380	264.7
1722	G106	-10395	137.2
1723	G104	-10410	264.7
1724	G102	-10425	137.2
1725	G100	-10440	264.7
1726	G98	-10455	137.2
1727	G96	-10470	264.7
1728	G94	-10485	137.2
1729	G92	-10500	264.7
1730	G90	-10515	137.2
1731	G88	-10530	264.7
1732	G86	-10545	137.2
1733	G84	-10560	264.7
1734	G82	-10575	137.2
1735	G80	-10590	264.7
1736	G78	-10605	137.2
1737	G76	-10620	264.7
1738	G74	-10635	137.2
1739	G72	-10650	264.7
1740	G70	-10665	137.2
1741	G68	-10680	264.7
1742	G66	-10695	137.2
1743	G64	-10710	264.7
1744	G62	-10725	137.2
1745	G60	-10740	264.7
1746	G58	-10755	137.2
1747	G56	-10770	264.7
1748	G54	-10785	137.2
1749	G52	-10800	264.7
1750	G50	-10815	137.2

No.	Pad name	X	Y
1751	G48	-10830	264.7
1752	G46	-10845	137.2
1753	G44	-10860	264.7
1754	G42	-10875	137.2
1755	G40	-10890	264.7
1756	G38	-10905	137.2
1757	G36	-10920	264.7
1758	G34	-10935	137.2
1759	G32	-10950	264.7
1760	G30	-10965	137.2
1761	G28	-10980	264.7
1762	G26	-10995	137.2
1763	G24	-11010	264.7
1764	G22	-11025	137.2
1765	G20	-11040	264.7
1766	G18	-11055	137.2
1767	G16	-11070	264.7
1768	G14	-11085	137.2
1769	G12	-11100	264.7
1770	G10	-11115	137.2
1771	G8	-11130	264.7
1772	G6	-11145	137.2
1773	G4	-11160	264.7
1774	G2	-11175	137.2
1775	DUMMY	-11190	264.7
1776	DUMMY	-11205	137.2
	alignment	-11300	-272.5
	alignment	11300	-272.5

BUMP Size	
Input Pads (1 ~ 320)	
Output Pads (321 ~ 1776)	

Chip Size: 22828μm x 690μm

Chip thickness: 300μm(typ.)

Pad Location: Pad Center.

Coordinate Origin: Chip center

Au bump height: 9μm(typ.)

Au bump size:

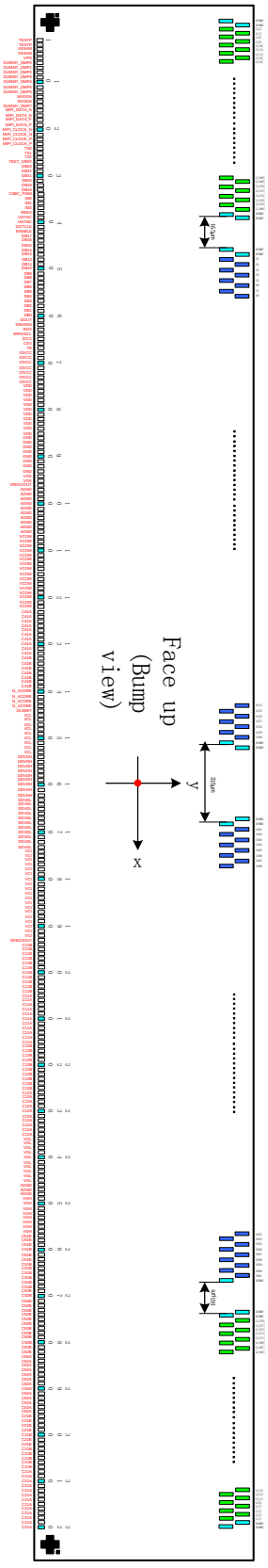
1. 13μm × 82.5μm

   Gate: G1 ~ G480

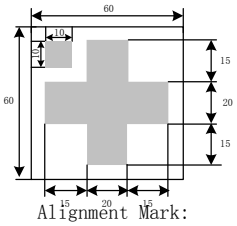
   Source: S1 ~ S961

2. 50μm × 66.5μm

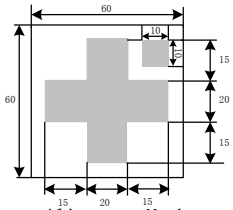
   Input pads 1 ~ 320



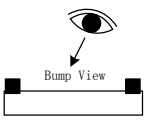
Alignment Marks



Alignment Mark:
Left



Alignment Mark:
Right



4 Interface setting

4.1 MCU interfaces

GC9403 provides the 8-/9-/16-/18-/24 bit parallel system interface for 8080 series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [2:0] and the data format for each pixel color is selected by DBI [2:0] bits.

4.1.1 MCU interface selection

The selection of system interface by IM[2:0] is shown as follows.

IM2	IM1	IM0	MCU-Interface Mode	Data pin in use
0	0	0	8080 24-bit bus interface	DB[23:0]
0	0	1	8080 9-bit bus interface	DB[8:0]
0	1	0	8080 16-bit bus interface	DB[15:0]
0	1	1	8080 8-bit bus interface	DB[7:0]
1	0	0	prohibited	-
1	0	1	3-line SPI	SDA
1	1	0	MIPI_DSI	MIPI_DATA_P MIPI_DATA_N MIPI_CLOCK_P MIPI_CLOCK_N
1	1	1	4-line SPI	SDA

4.1.2 8080 Series Parallel Interface

GC9403 can be accessed via 8-/9-/16-/24-bit MCU 8080 series parallel interface. The chip-select CSX (active low) is used to enable or disable GC9403. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[23:0] is the parallel data bus.

GC9403 latches the input data at the rising edge of WRX. D/CX is the signal of data/command selection. When D/CX='1', D[23:0] bits are display RAM data or command's parameters. When D/CX='0', D[7:0] bits are commands.

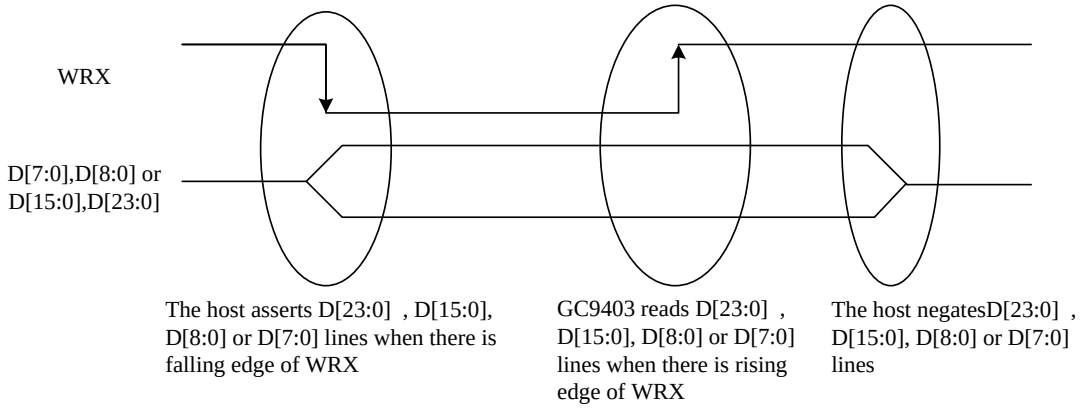
The 8080 series bi-directional interface can be used for communication between MCU controller and LCD driver chip. The selection of 8080 series parallel interface is shown in the following table.

IM2	IM1	IM0	MPU-interface	WRX	RDX	D/CX	Function
0	0	0	24-bit parallel	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Read parameter or display data.
0	0	1	9-bit parallel	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Read parameter or display data.
0	1	0	16-bit parallel	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Read parameter or display data.
0	1	1	8-bit parallel	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Read parameter or display data.

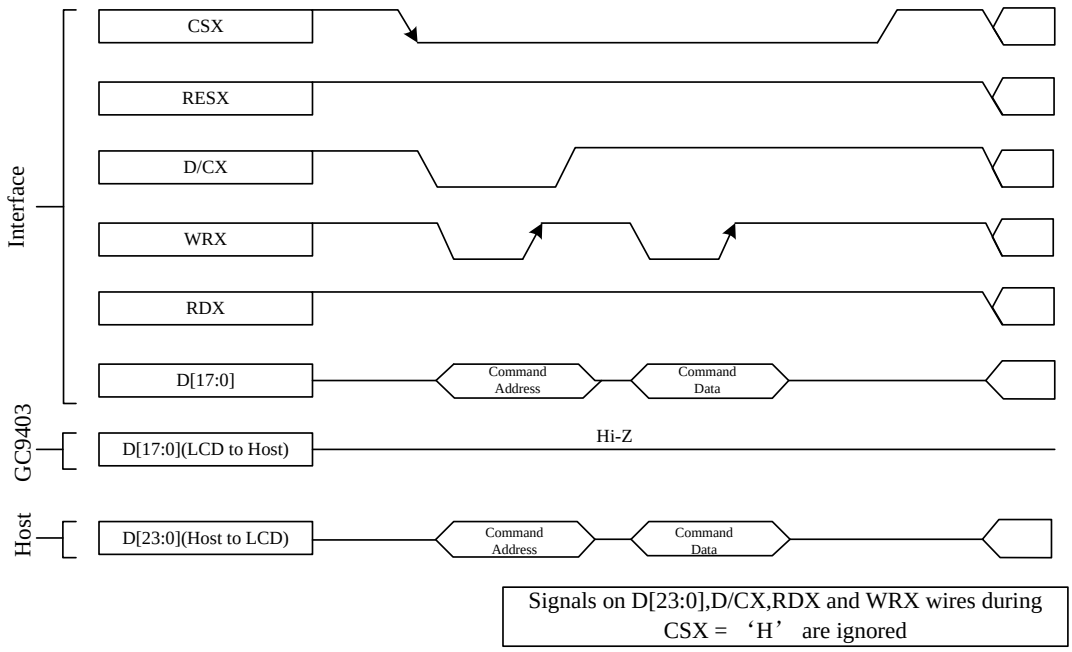
4.1.3 Write Cycle Sequence

The WRX signal is driven from high to low and then pulled back to high during the write cycle. The host processor provides information during the write cycle which is captured by the display module on the rising edge of WRX. Input data on the interface is interpreted as command information if D/CX is driven low; otherwise it represents GRAM data or a command's parameter.

The following figure shows a write cycle for the 8080 MCU interface.



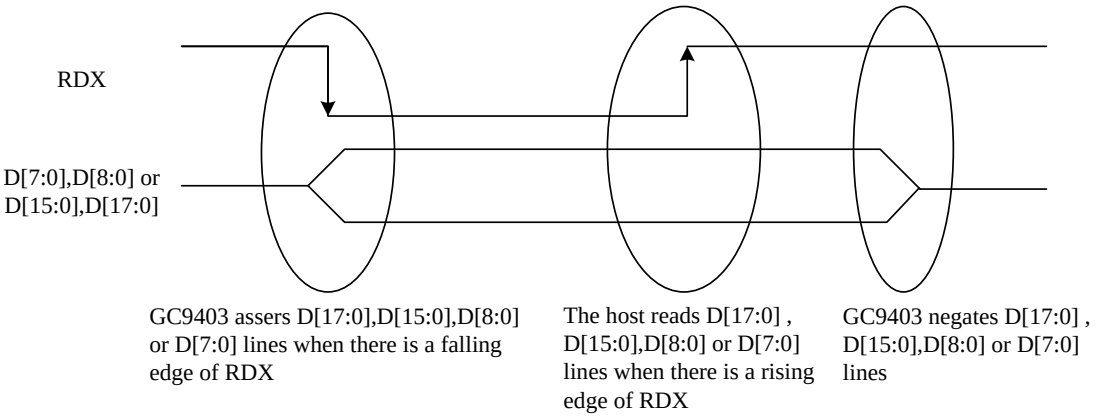
Note: WRX is an unsynchronized signal (It can be stopped)



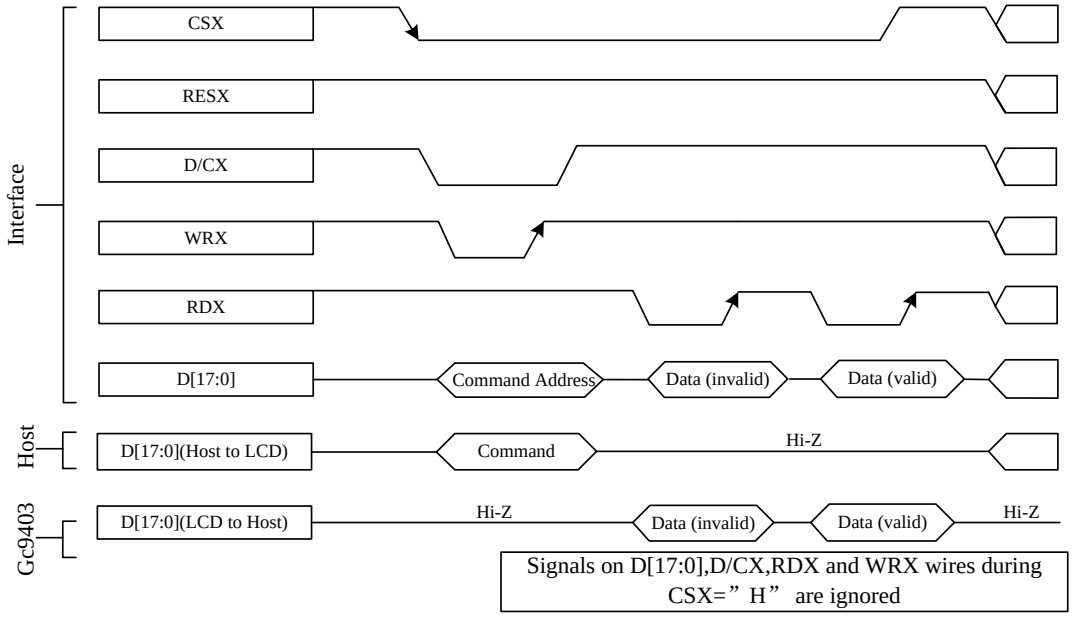
4.1.4 Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, which is captured on the rising edge of RDX signal. Input data on the interface is interpreted as command if D/CX is driven low; otherwise it represents GRAM data or a command's parameter.

The following figure shows the read cycle for the 8080 MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5 Serial Interface

The selection of interface is done by IM[2:0] bit. Please refer to the Table in the following.

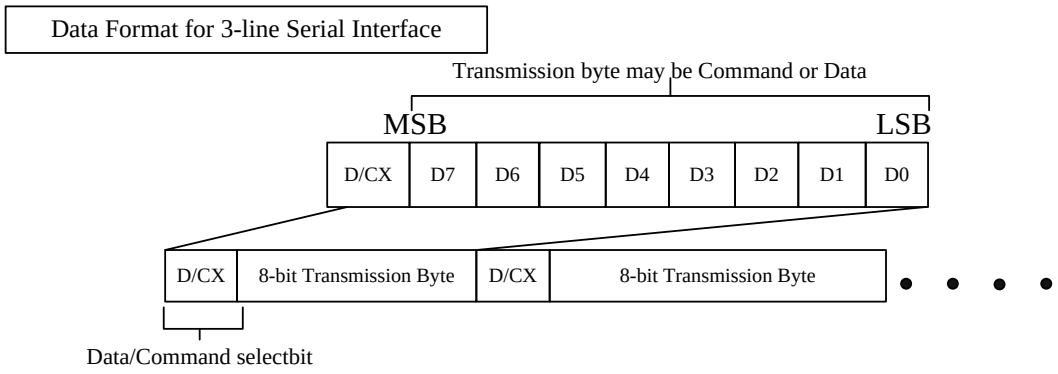
IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	0	1	3-line serial interface	“L”	-	⌐¬	Read / Write command, parameter or display data.
1	1	1	4-line serial interface	“L”	"H" / "L"	⌐¬	Read / Write command, parameter or display data.

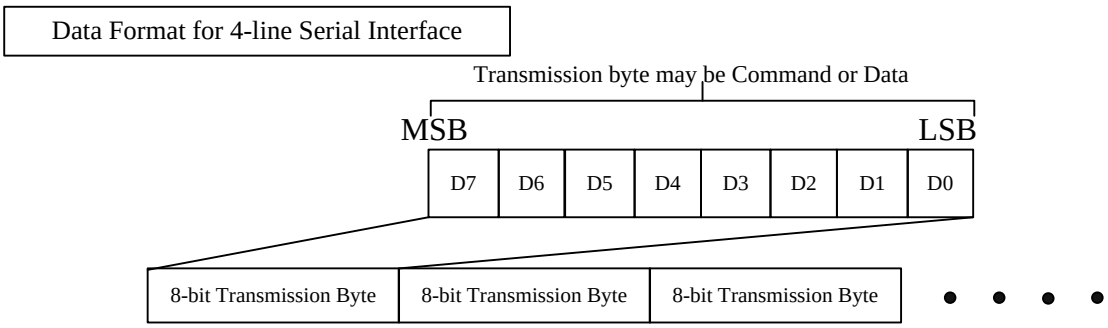
GC9403 provides 3-line / 9-bit and 4-line / 8-bit bi-directional serial interfaces for communication between host and GC9403. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data input / output (SDA). The 4-line serial mode consists of the data / command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data input / output (SDA) for data transmission. Unused data pins should be connected to ground. Serial clock (SCL) is only used for the interface between GC9403 with MCU, therefore can be halted when communication is not required.

4.1.6 Write Cycle Sequence

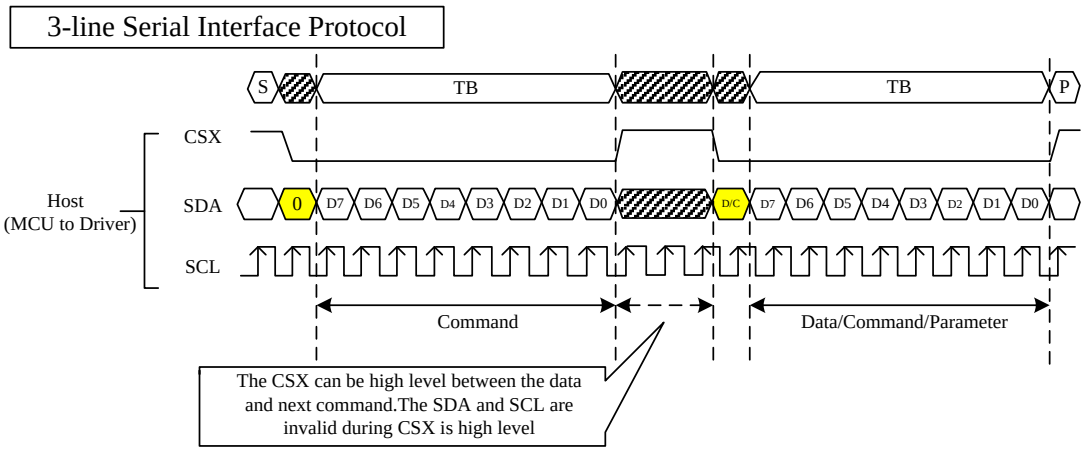
The write mode of the interface means that host writes commands or data to GC9403. The 3-line serial data packet contains a data / command selection bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM (Memory write command), or the command register as parameter.

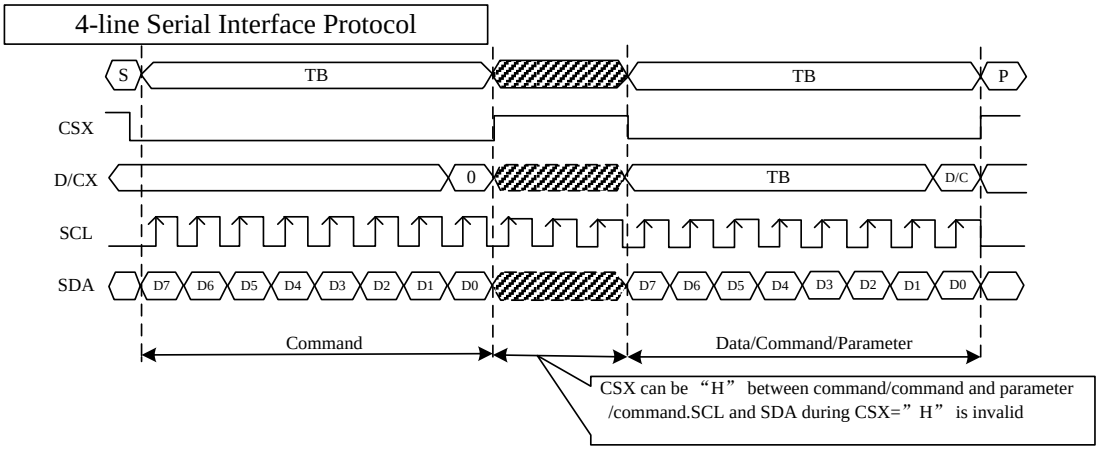
Instructions can be sent in any order to GC9403 with MSB transmitted first. When the CSX signal is driven high, the serial interface enters its initial state, in which SCL and SDA signals have no effect. A falling edge of CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3- / 4-line serial interface.





Host processor pulls the CSX pin low by setting the D/CX bit on SDA. The bit is read by GC9403 on the first rising edge of SCL. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host, followed by the next bits (D6 ~ D0) set at each falling edge one after another. Eight write cycles are required to complete one transmission byte. The above write sequence is shown in the following figure.



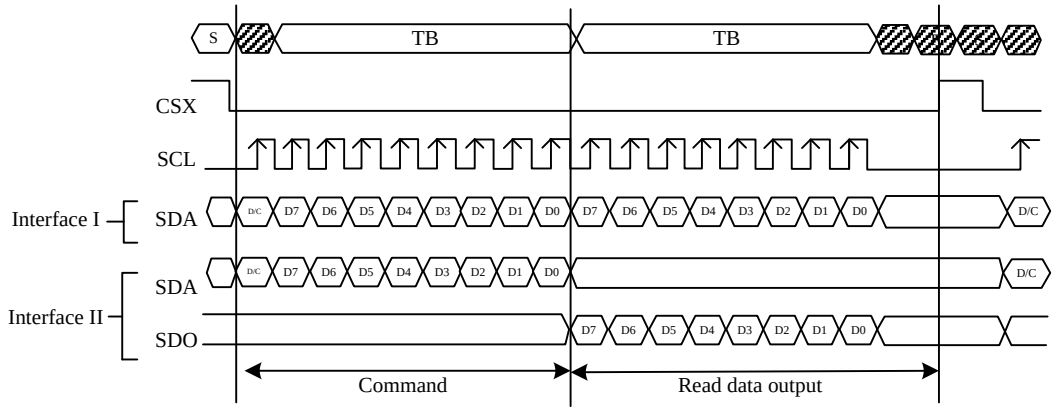


4.1.7 Read Cycle Sequence

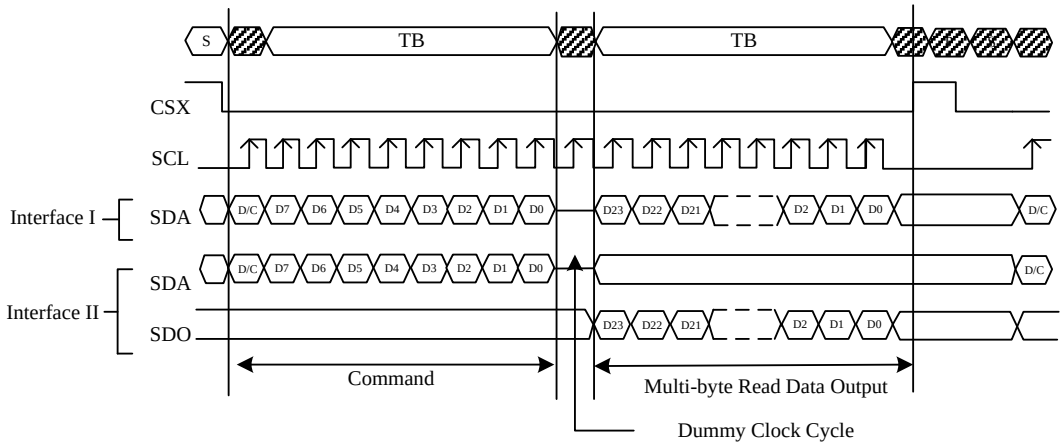
The read mode of interface means that the host reads register vale from GC9403. The host has to send out a command (Read ID or register command) first to start the transmission. GC9403 latches the SDA (input data) at each rising edge of SCL (serial clock), and then shifts SDA (output data) at the next falling edge of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state no later than the falling edge of SCL of the last bit. The read mode has three types of command data (8- / 24- / 32-bit) according to command code.

3-wire Serial Interface Protocol

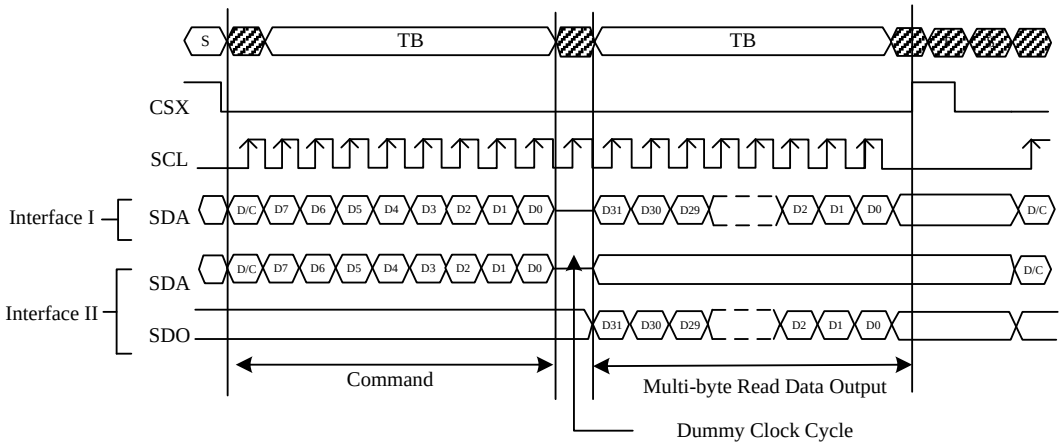
3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



3-wire Serial Protocol (for RDDID command:24-bit read)

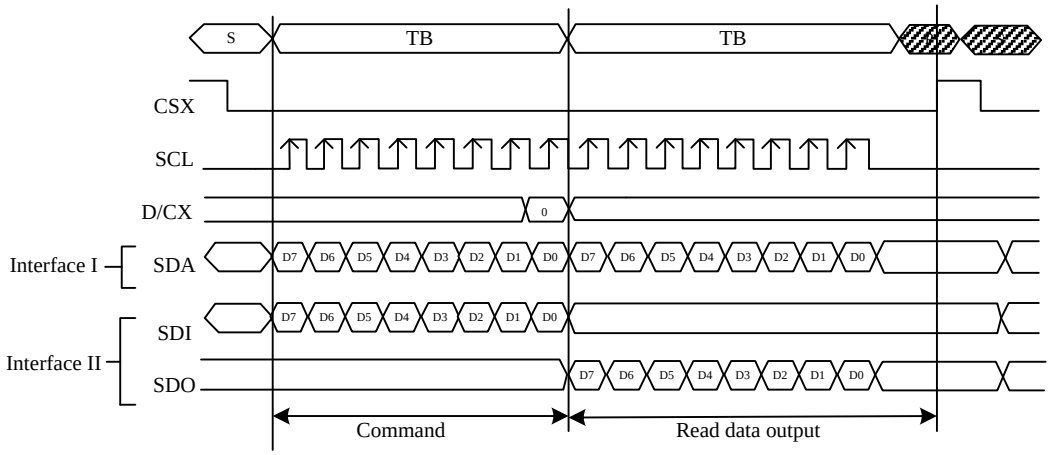


3-wire Serial Protocol (for RDDST command:32-bit read)

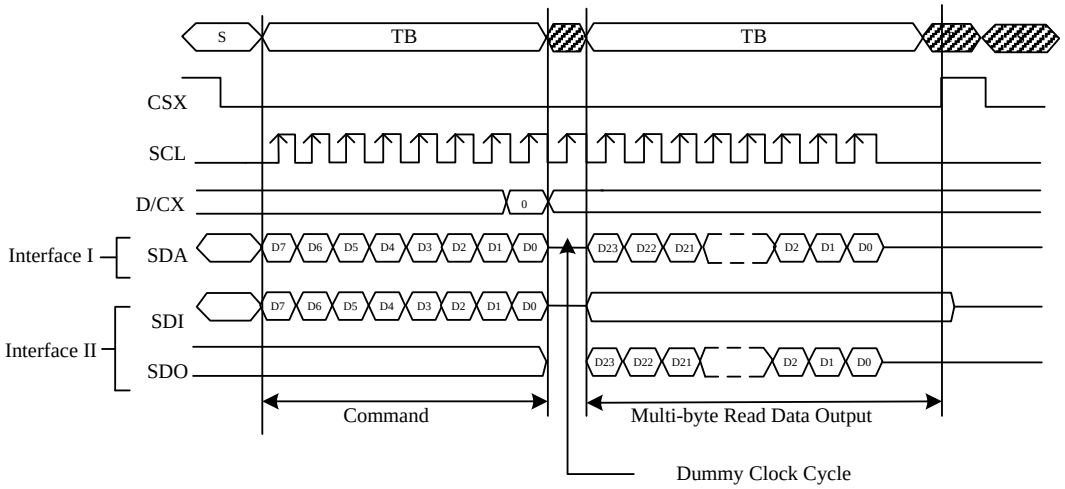


4-wire Serial Interface Protocol

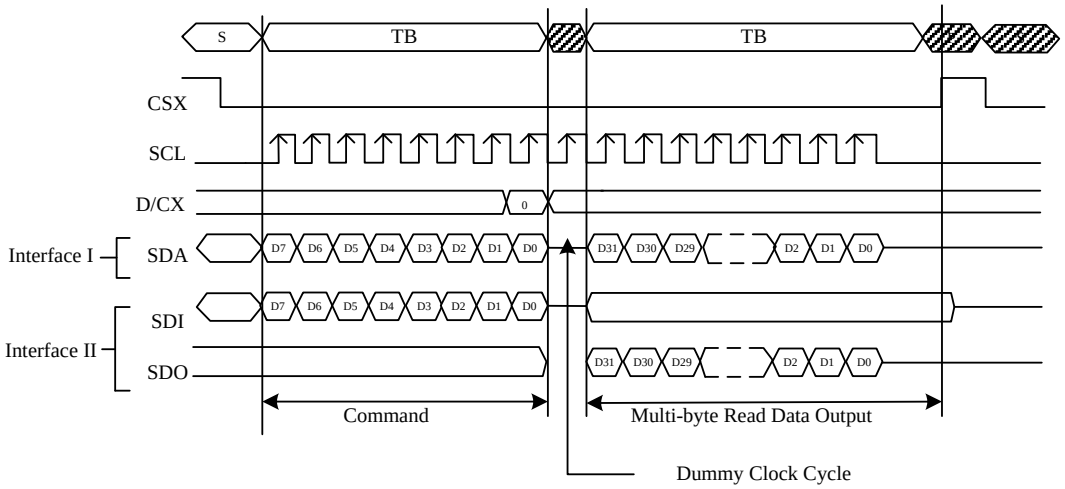
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



4-wire Serial Protocol (for RDDID command:24-bit read)

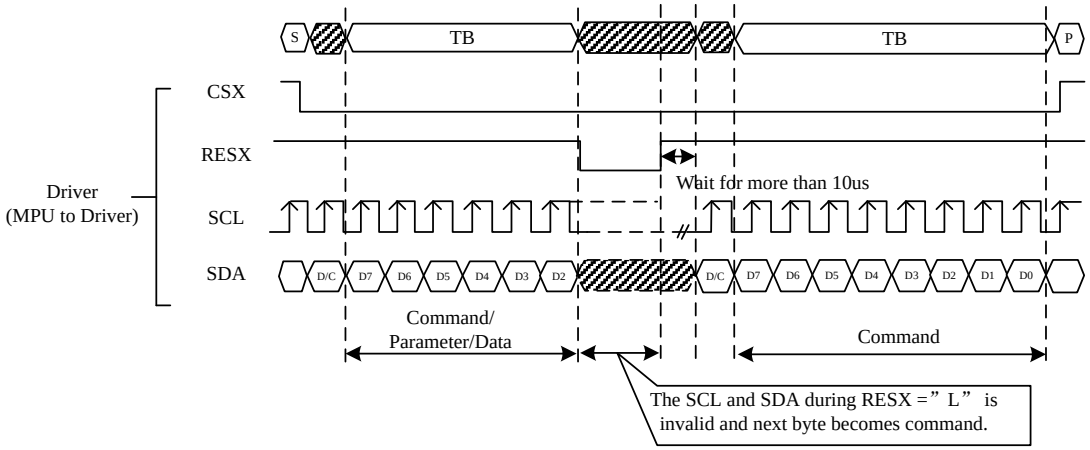


4-wire Serial Protocol (for RDDST command:32-bit read)

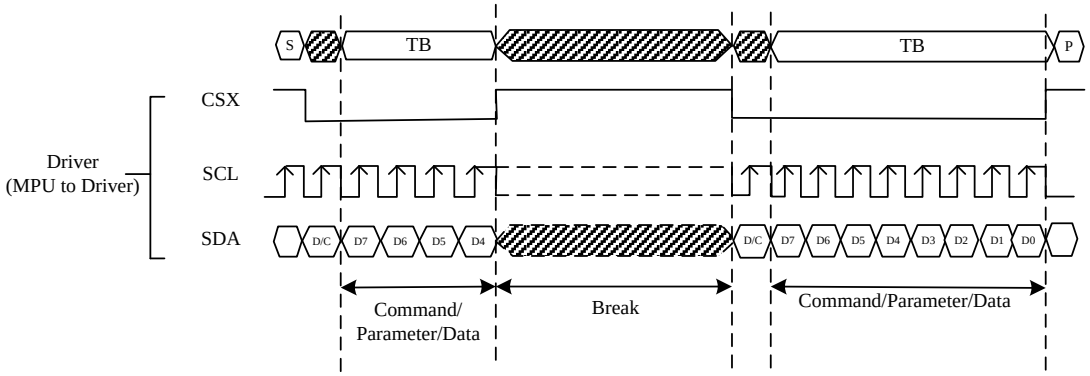


4.1.8 Data Transfer Break and Recovery

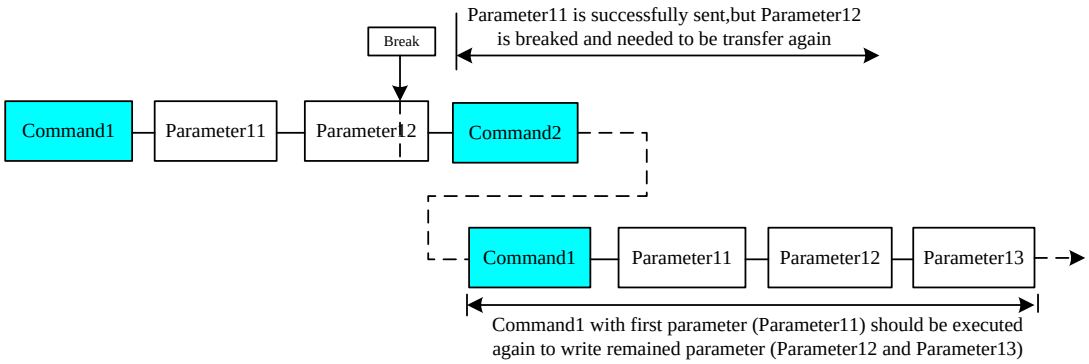
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface so that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX returns to high.



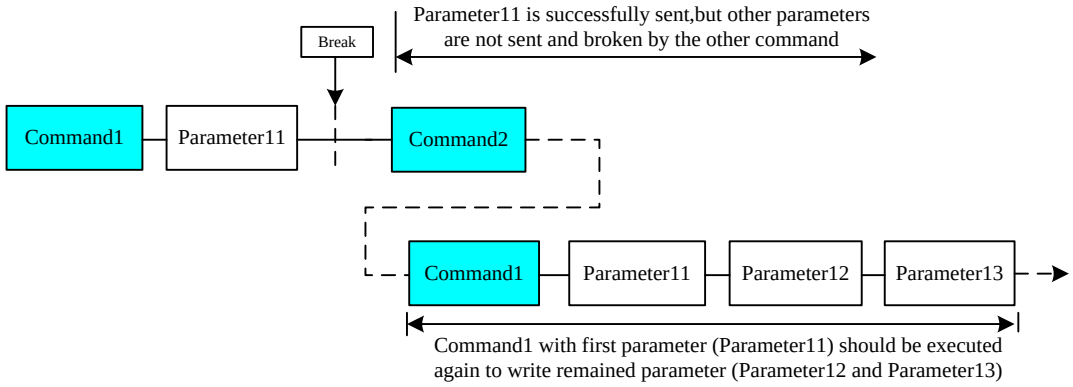
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before finishing bit D0 of the byte, GC9403 rejects all previous bits and resets the interface for the re-transmission of the same byte after the CSX is active again.



While commands with more than a parameter, if a break occurs before the last one and then the host begins sending out a new command rather than the remained bits of the interrupted command, GC9403 stores the successfully received parameters and discards the incomplete one. The interface is ready to receive next byte. The above sequence is shown as follows.



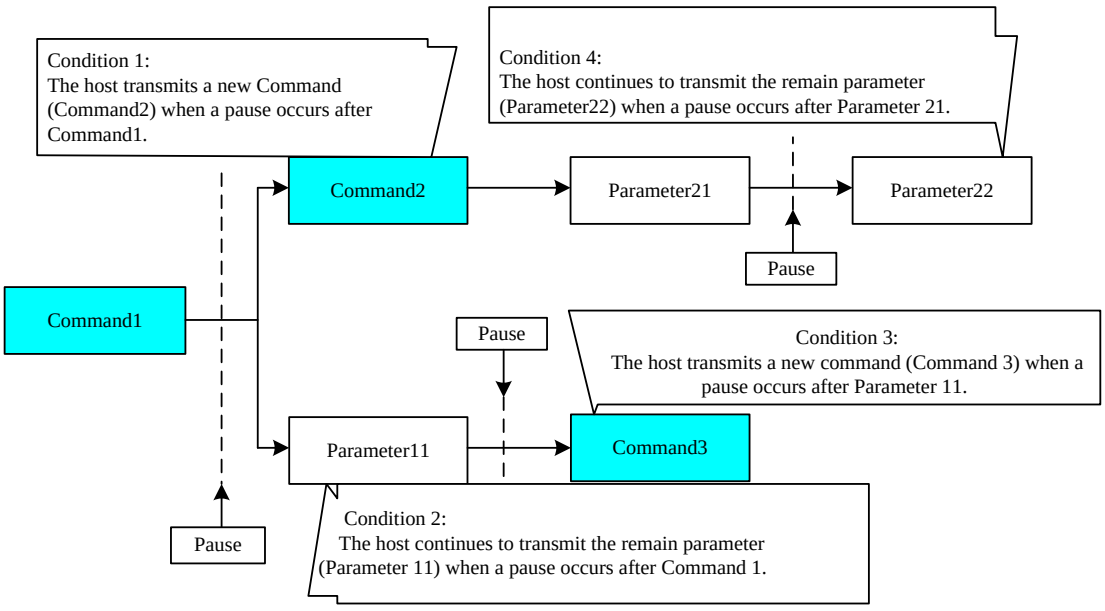
If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



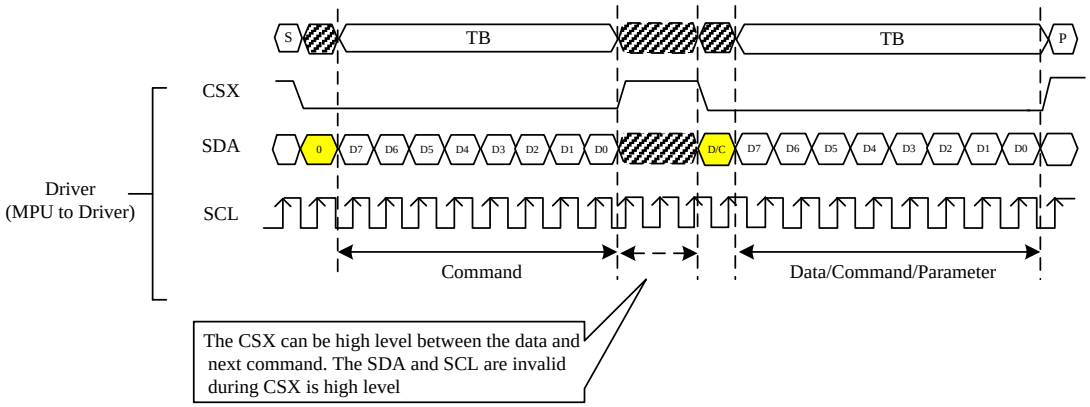
4.1.9 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9403 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

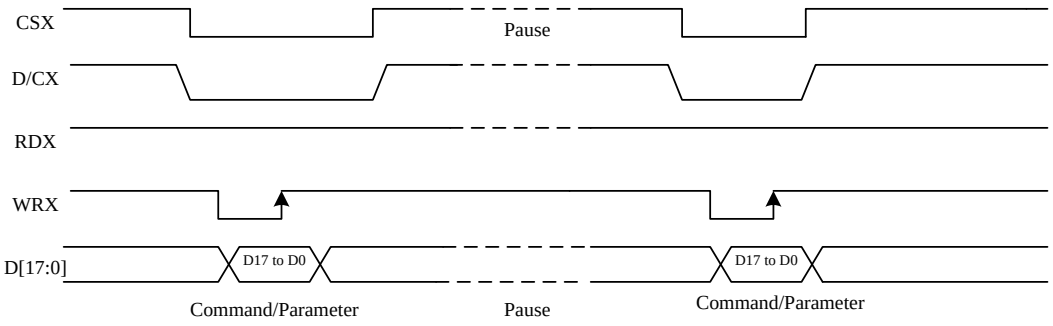
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter



4.1.10 Serial Interface Pause (3_wire)



4.1.11 Parallel Interface Pause

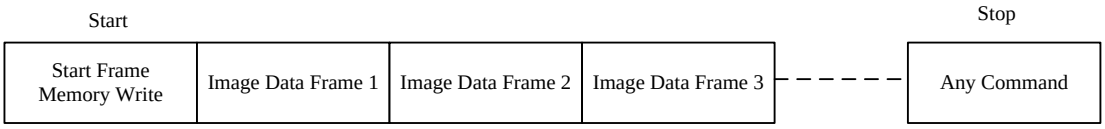


4.1.12 Data Transfer Mode

GC9403 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

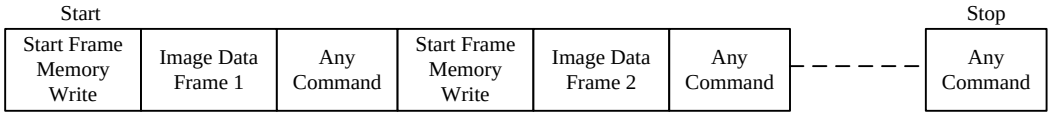
4.1.13 Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



4.1.14 Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2 RGB Interface

4.2.1 RGB Interface Selection

GC9403 has two types of RGB interfaces which can be selected by RCM bit. When RCM is set to “0”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, and D[17:0] pins; when RCM is set to “1”, the SYNC mode is selected which utilizes VSYNC, HSYNC,DOTCLK, and D[17:0] pins. GC9403 supports several pixel formats that can be selected by DPI[3:0] bits of “Pixel Format Set (3Ah)” command. The selection of the given interfaces is shown in the following table.

RCM	DPI[3:0]				RGB interface Mode	RGB Mode	Used Pins
0	0	1	1	1	24-bit RGB interface (16.7M colors)	**DE Mode** Valid data is determined by the DE signal.	VSYNC,HSYNC,DE,DOTCLK,D[23:0]
0	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK,D[17:0]
0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK,D[15:0]
1	0	1	1	1	24-bit RGB interface (16.7M colors)	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC,HSYNC,DOTCLK,D[23:0]
1	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK,D[17:0]
1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK,D[15:0]

24-bit data bus interface (D[23:0] is used), DPI[2:0] = “111”.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24bpp Frame Memory Write	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

18-bit data bus interface (D[17:0] is used), DPI[2:0] = “110”.

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

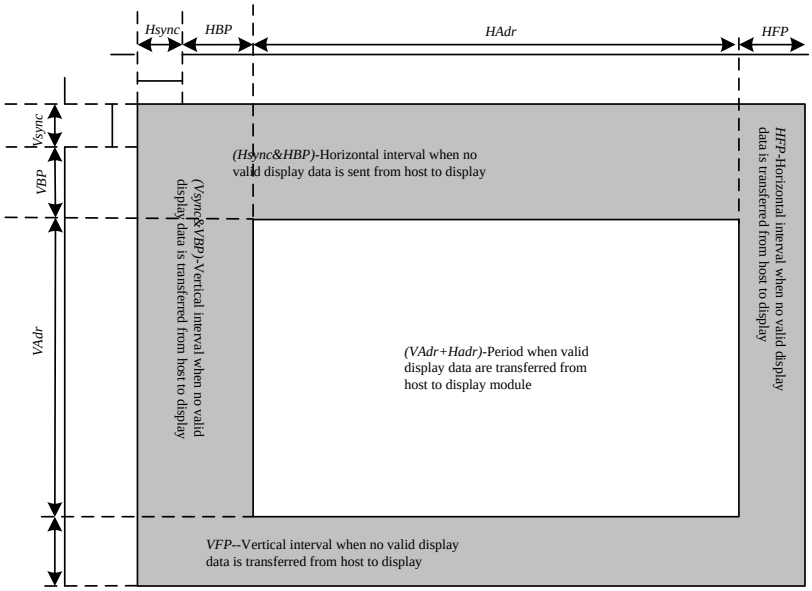
16-bit data bus interface (D[15:0] is used) , DPI[2:0] = “101”.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color are same as MSB data.

Pixel clock (DOTCLK) is running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLE and DB[17:0] states when there is a rising edge of the DOTCLK.

Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.
Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.
In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal.
D [23:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [23:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Notes:

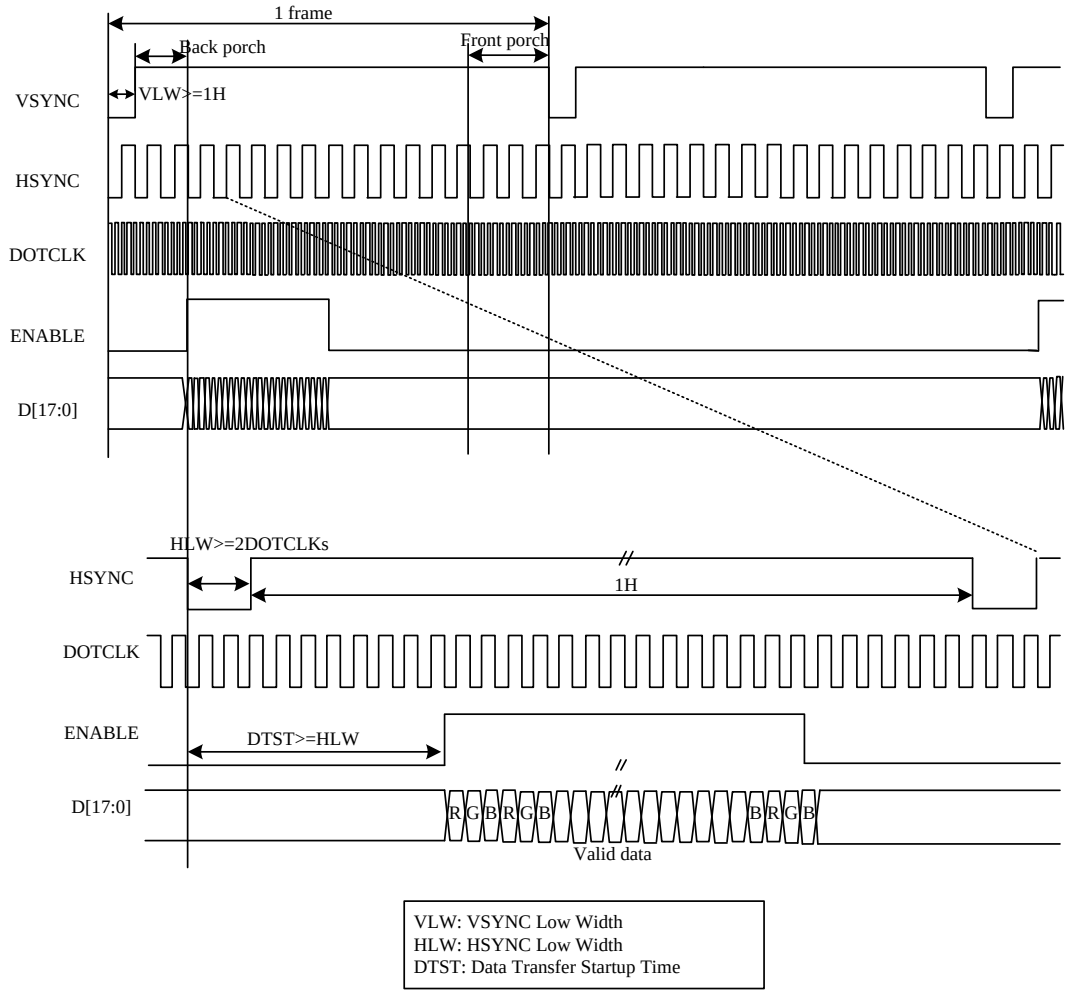
1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

4.2.2 RGB Interface Timing

The timing chart of 24-/18-/16-bit RGB interface mode is shown as below.



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

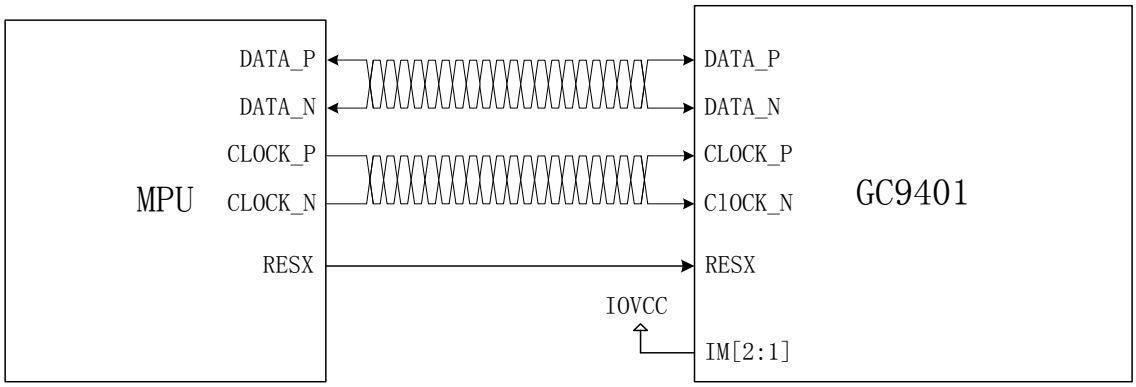
Note 2: VSPL=’0’, HSPL=’0’, DPL=’0’ and EPL=’0’ of “Interface Mode Control (B0h)” command.

4.3 MIPI (Mobile Industry Processor Interface – Display Serial Interface)

GC9403supports MIPI DSI which can be enabled or disabled by external IM [2:0] pin. GC9403can be accessed through one PHY lane module which communicates via two lines to a complementary part at the other side of the lane interconnects. The communication can be separated two different levels between the MCU and GC9403:

- Low level communication what is done on the interface level.
- High level communication what is done on the packet level.

GC9403 uses data and clock lane differential pairs for DSI, The data lane (DATAP and DATAN) is used for data communication and clock lane (CLKP and CLKN) is used to transmit the clock signal. The Mobile Industry Processor Interface (MIPI) can be used for communication between the processor and DSI-compliant LCD driver chip. The selection of this interface is done when IM [2:0] pins are high state (IOVCC level).



Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to GC9403 and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane pair state code	Line DC Voltage Levels		High Speed	Low Power	
	DATA_P	DATA_N	Burst mode	CLOKC_P	CLOCK_N
HS-0	Low(HS)	High(HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low(LP)	Low(LP)	Not define	Bridge	Space
LP-01	Low(LP)	High(LP)	Not define	HS-Request	Mark-0
LP-10	High(LP)	Low(LP)	Not define	LP-Request	Mark-1
LP-11	High(LP)	High(LP)	Not define	Stop	Note 2

Notes: (1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

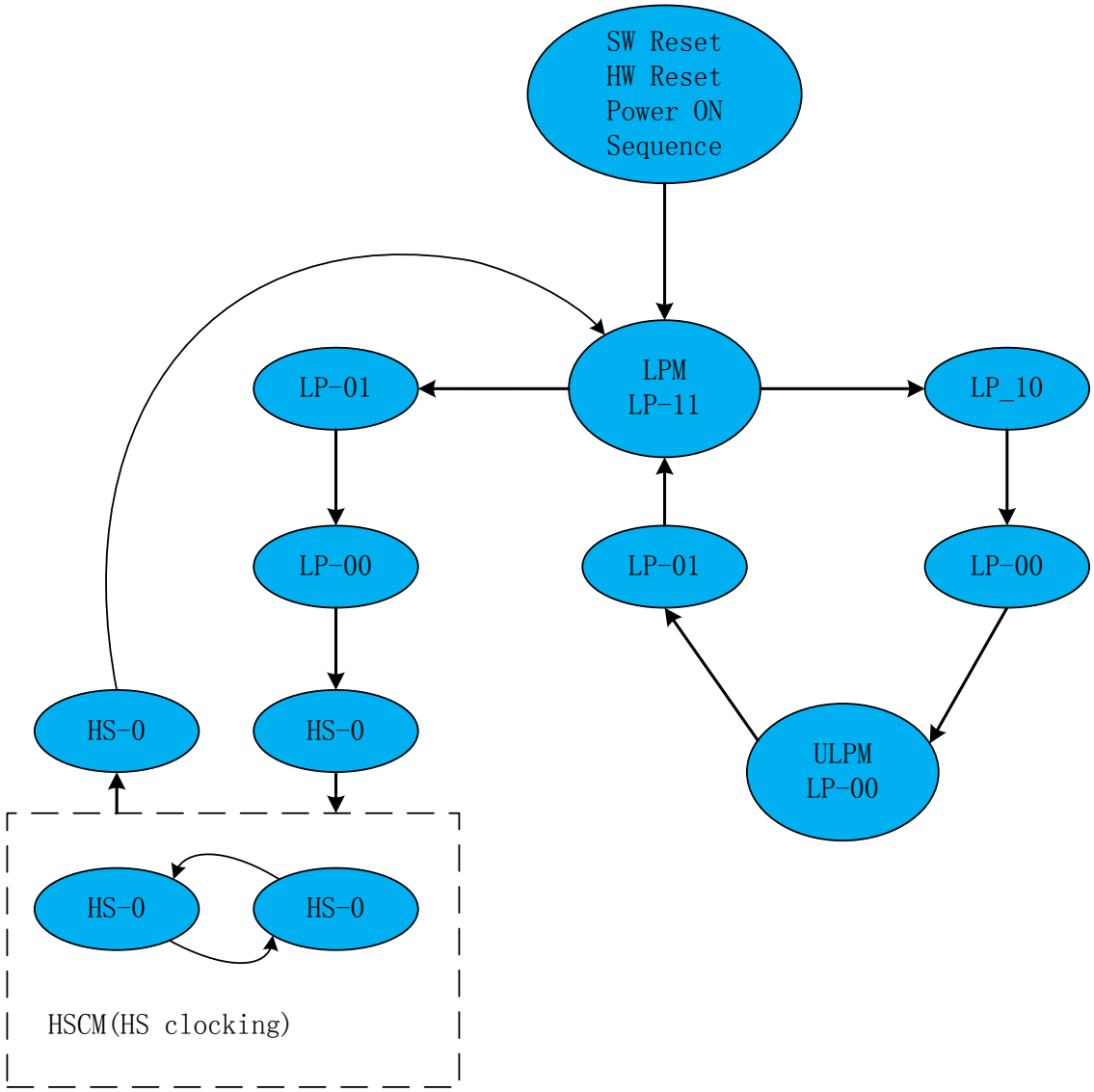
(2) If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

4.3.1 Interface Level Communication – Clock Lanes

DSI-CLOCK_P/N lanes can be driven into three different power modes:

- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

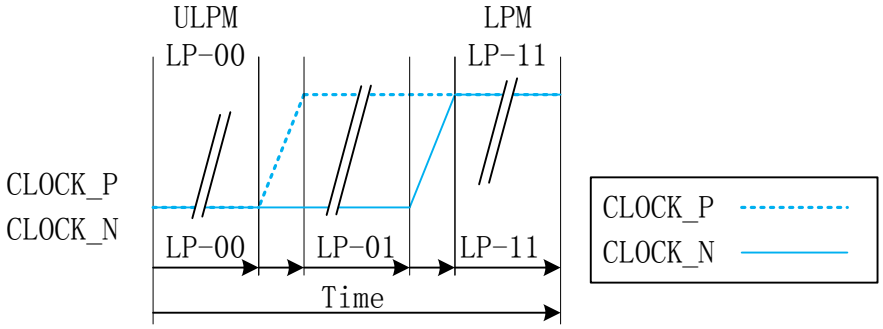
Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).
Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).
These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.
The principal flow chart of the different clock lanes power modes is illustrated below.



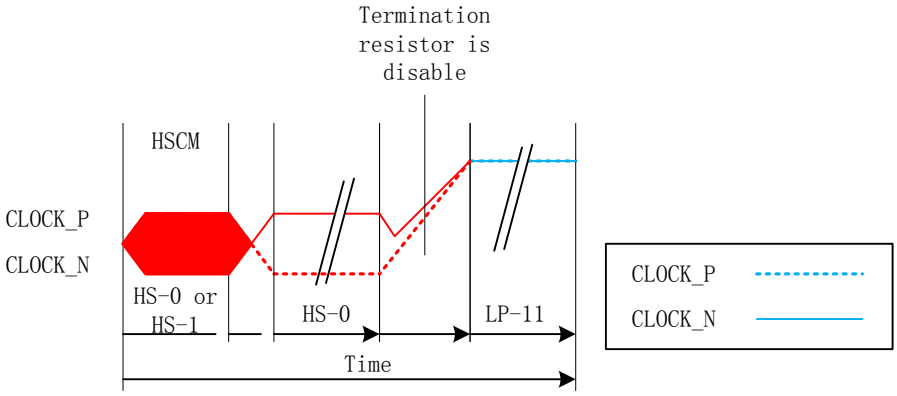
4.3.1.1 Low Power Mode (LPM)

DSI-CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when DSI-CLOCK lanes are entering LP-11 State Code, in three different ways:

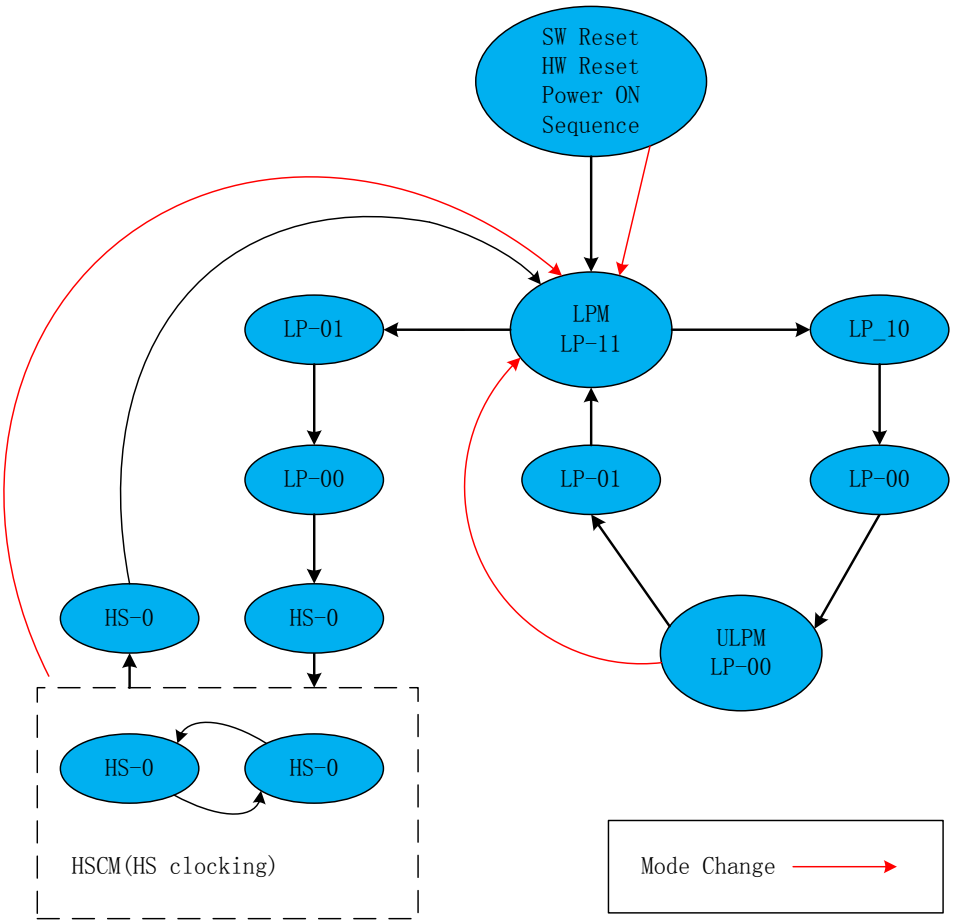
1) After SW Reset, HW Reset or Power On Sequence =>LP-11
2) After DSI-CLOCK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

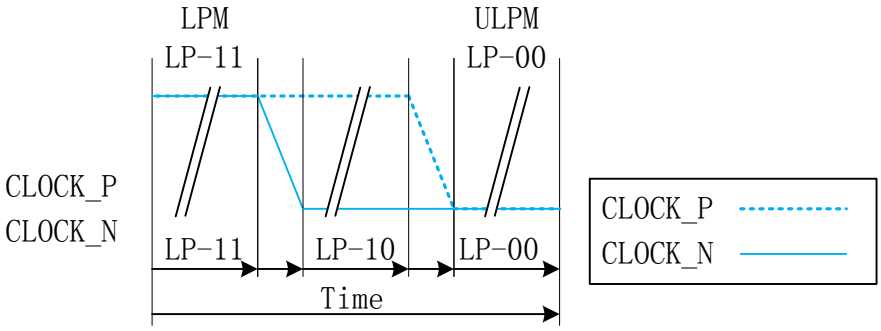


All three mode changes are illustrated a flow chart below.

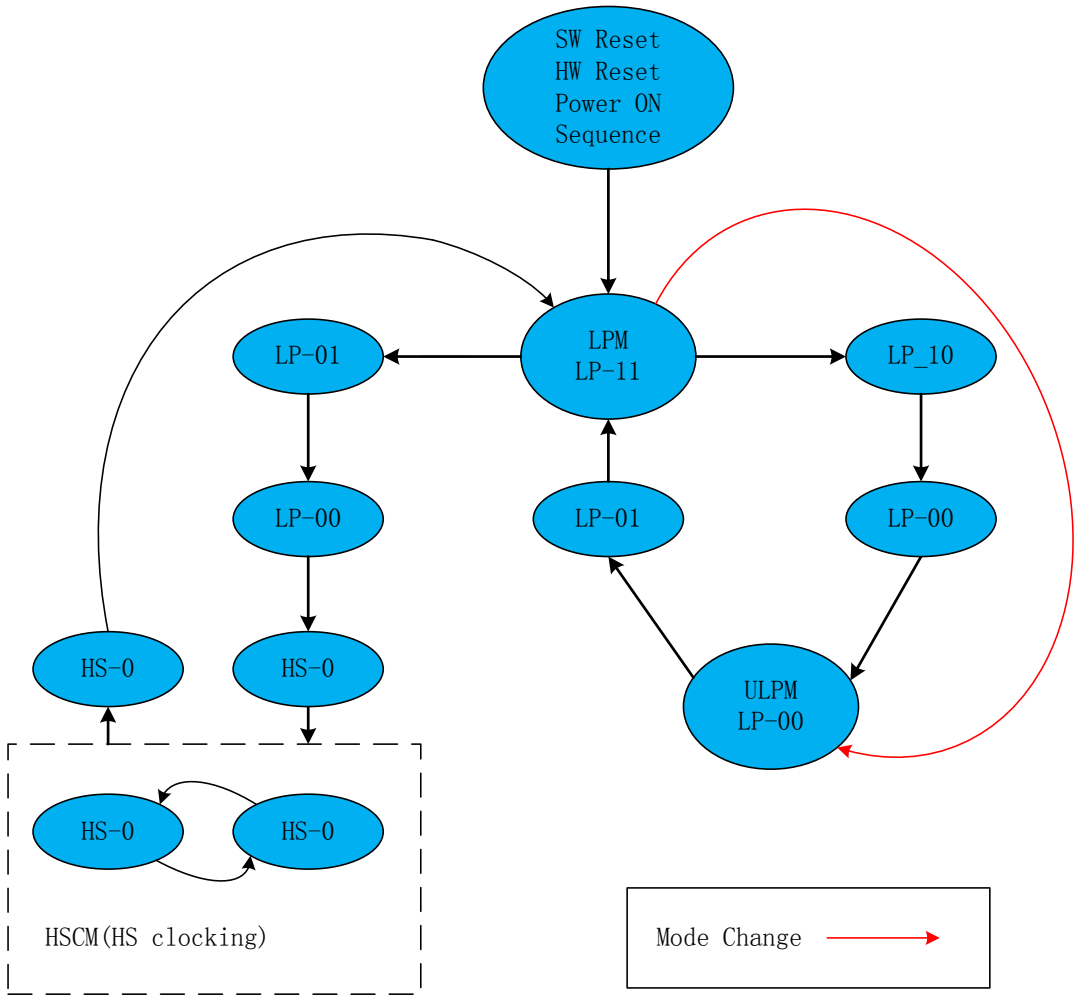

SW Reset
HW Reset
Power ON
Sequence
LPM
LP-11
LP-01
LP_10
LP-00
LP-01
LP-00
HS-0
HS-0
ULPM
LP-00
HS-0
HS-0
HSCM(HS clocking)
Mode Change

4.3.1.2 Ultra Low Power Mode (ULPM)

DSI-CLOCK_P/N lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLOCK lanes are entering LP-00 State Code.
The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below

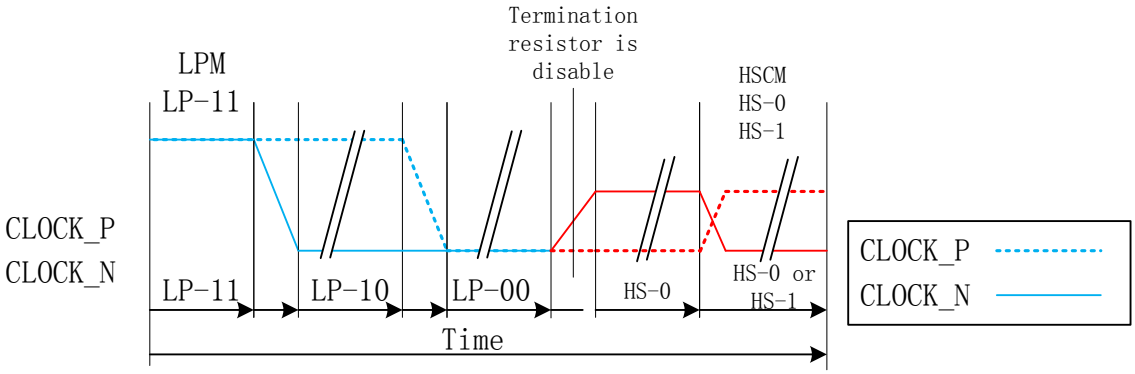


The mode change is also illustrated below.

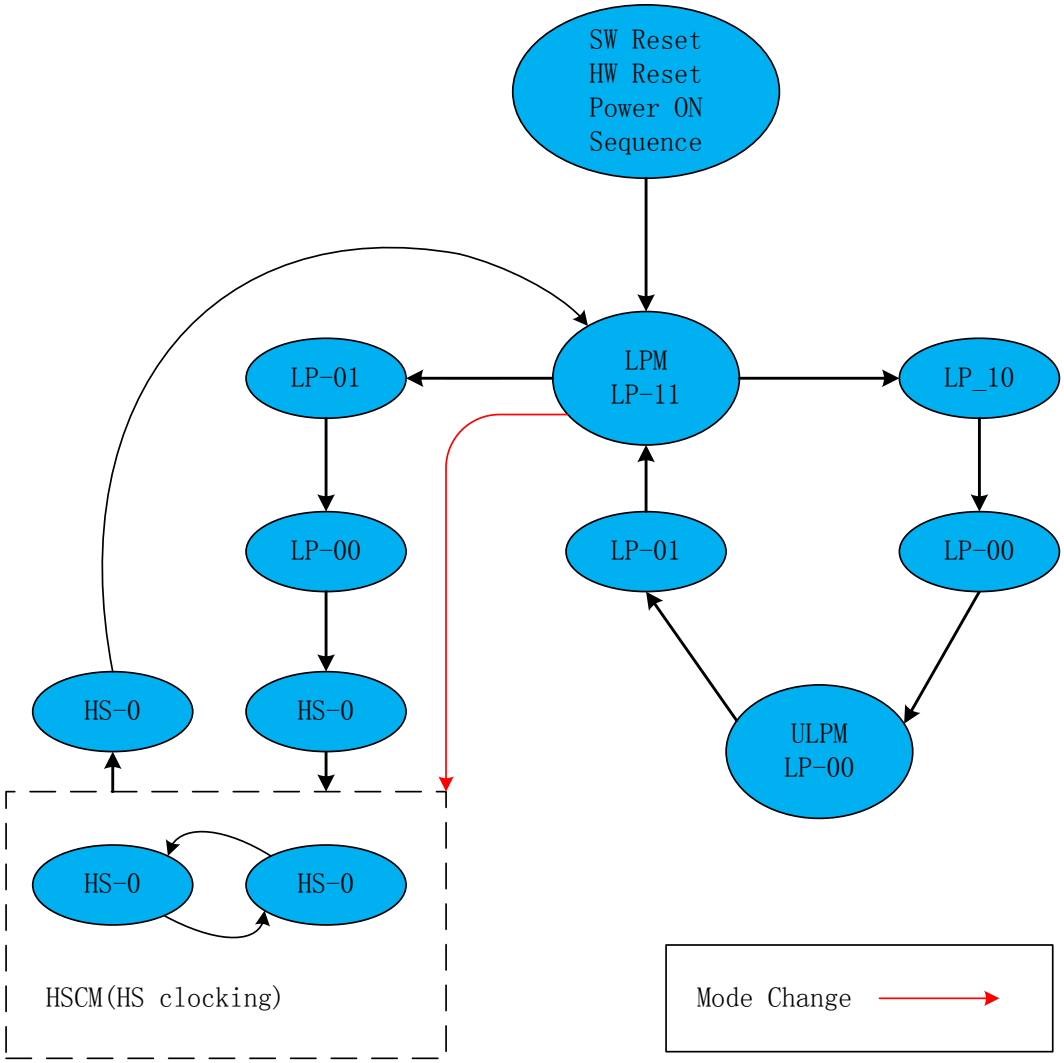


4.3.1.3 High-Speed Clocked Mode (HSCM)

DSI-CLOCK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLOCK lanes are starting to work between HS-0 and HS-1 State Codes.
The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

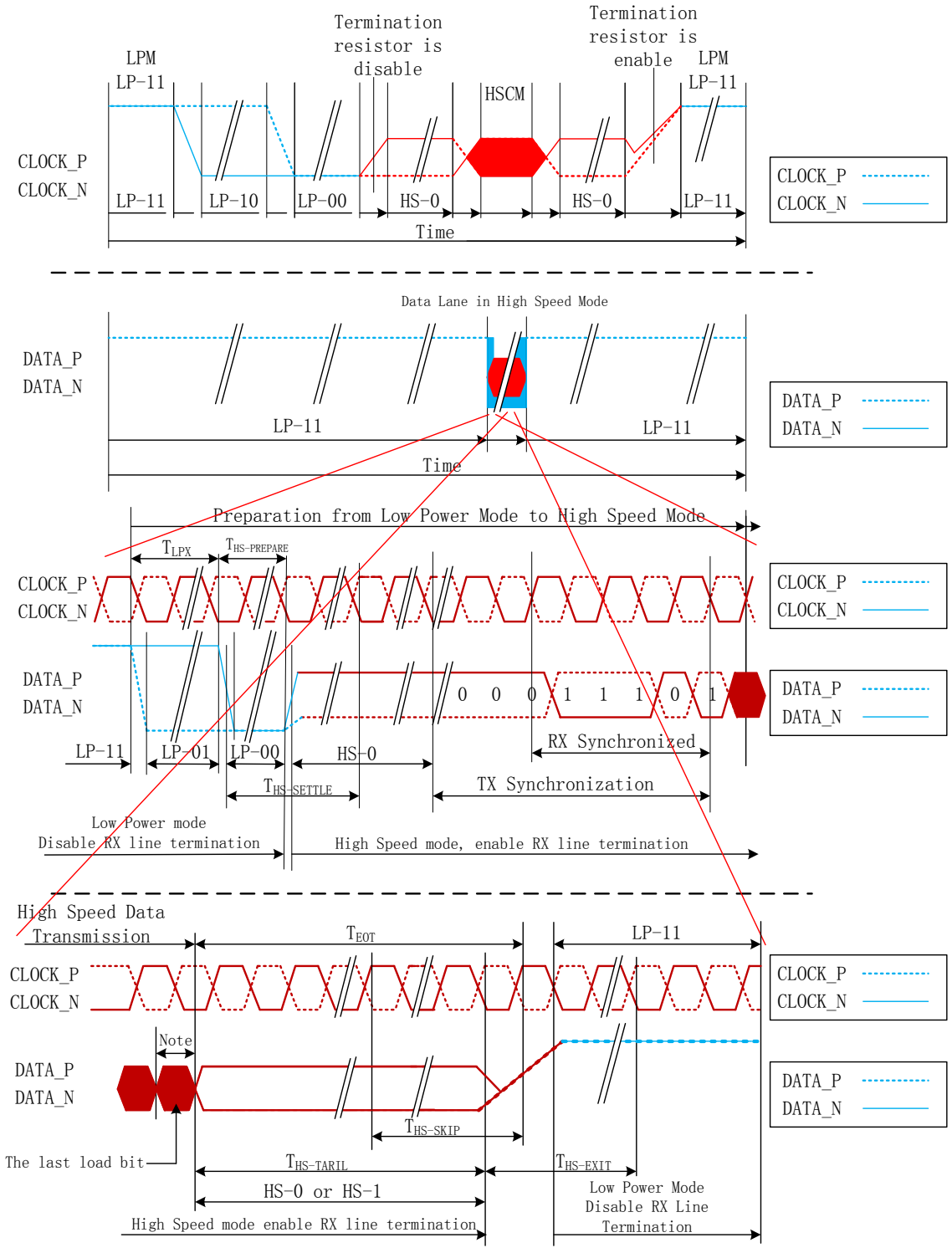


The mode change is also illustrated below.



The high speed clock (DSI-CLOCK_P/N) is started before high speed data is sent via DSI-DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped. The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Notes: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.3.2 Interface Level Communication – Data Lanes

DSI-DATA_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 →LP-01 →LP-00	LP-00 →LP-10 →LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 →LP-01 →LP-00 →HS-0	(HS-0 or HS-1) →LP-11
Bus Turnaround Request	LP-11 →LP-10 →LP-00 →LP-10 →LP-00	Hi-Z

4.3.2.1 Escape Modes

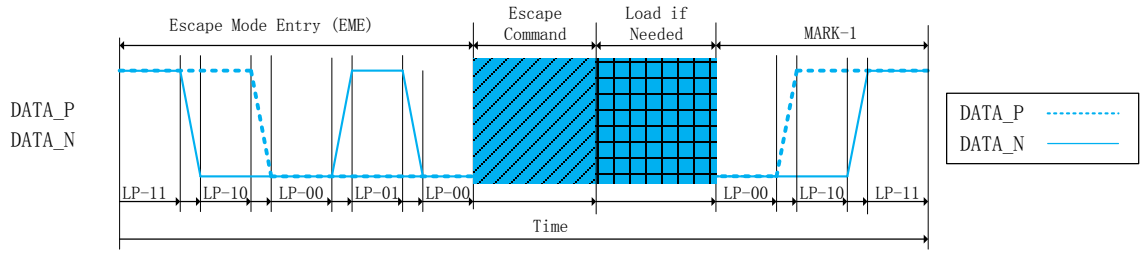
Data lanes (DSI-DATA_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to GC9403,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting GC9403,
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from GC9403 to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from GC9403 to the MCU

The basic sequence of the Escape Mode is as follow:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-DATA_P = 1, DSI-DATA_N- = 0) e.g. When DSI-DATA_N is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



There are a total of eight Escape Command(EC) divided into two types, Modes and Triggers(see below table).
An example of a Mode type Escape Command is “Ultra-Low Power Mode” where the MCU instructs the display module to enter it’s Ultra-Low Power Mode.
An example of Trigger type Escape Command is ‘Tearing Effect’. In this case the MCU has already instructed .The display module to provide this trigger and is waiting for the response. The display module then sends a TE Trigger(TEE) on the next V-sync event.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First to Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001
Ultra-Low Power Mode	Mode	0001 1110
Undefined-1, Note	Mode	1001 1111
Undefined-2, Note	Mode	1101 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001
Uknown-5, Note	Trigger	1010 0000

Note: This Escape command support has not been implemented on GC9403.

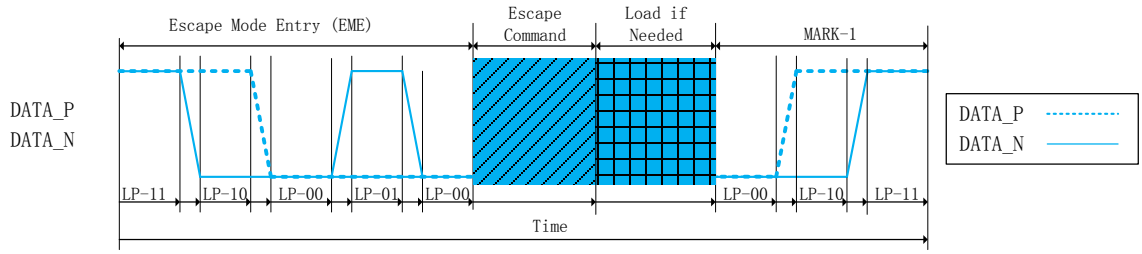
4.3.2.1.1 Low-Power Data Transmission (LPDT)

The MCU can send data to GC9403 in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to GC9403. GC9403 is also using the same sequence when it is sending data to the MCU.

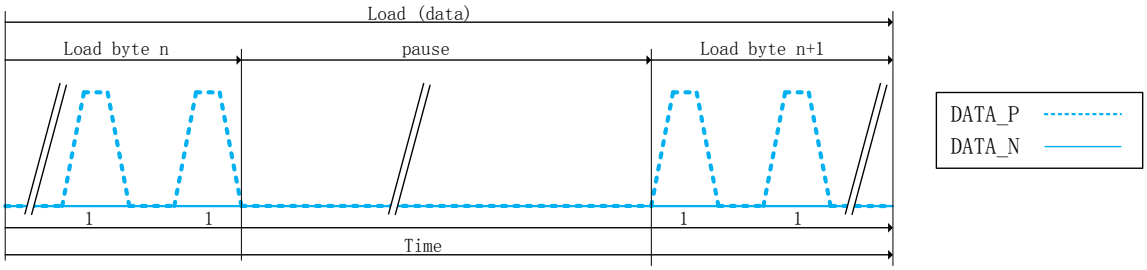
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical ‘1’ in this example.



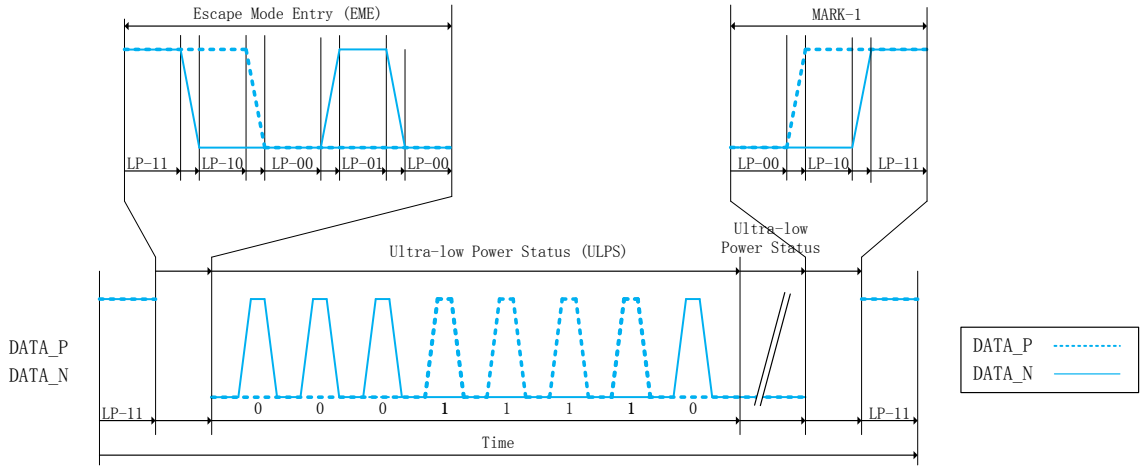
4.3.2.1.2 Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



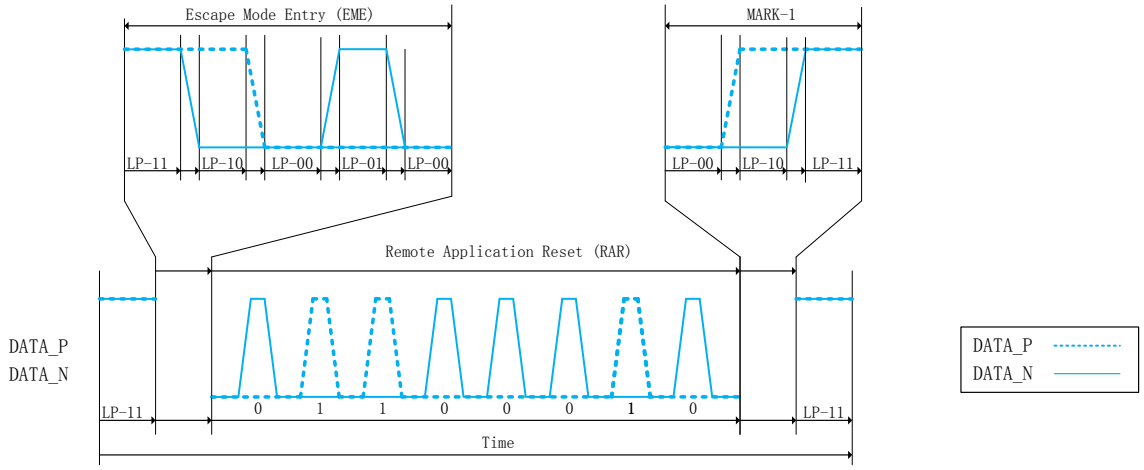
4.3.2.1.3 Remote Application Reset (RAR)

The MCU can inform to GC9403 that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



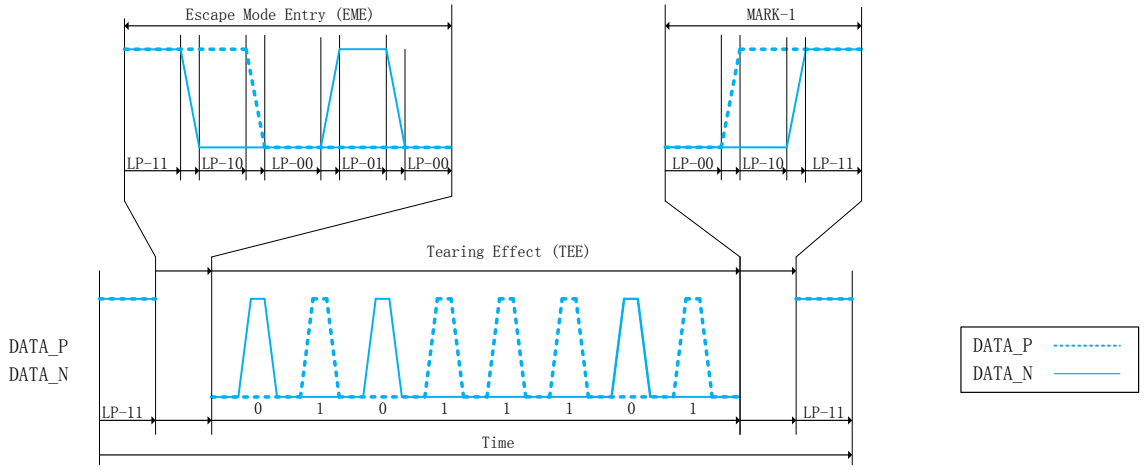
4.3.2.1.4 Tearing Effect (TEE)

GC9403 can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



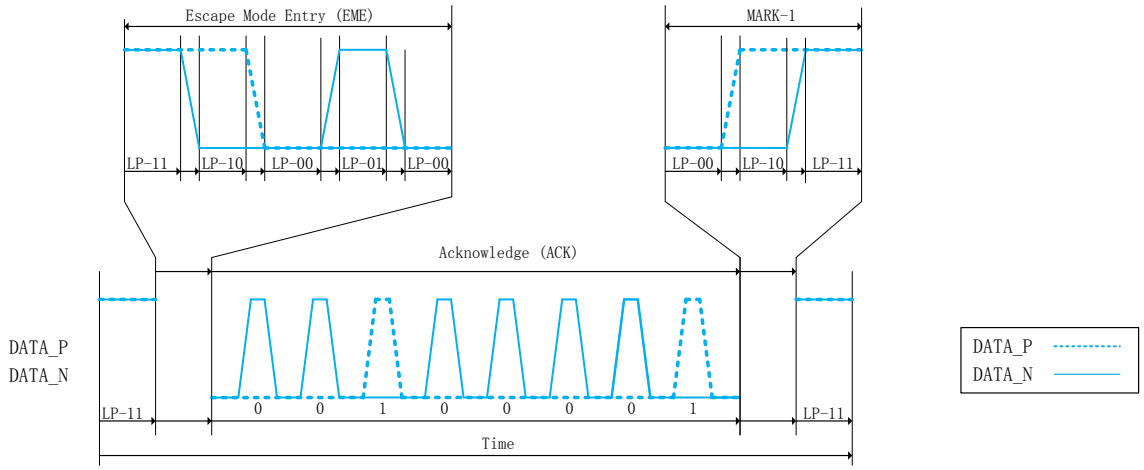
4.3.2.1.5 Acknowledge (ACK)

GC9403 can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



4.3.2.2 High-Speed Data Transmission (HSDT)

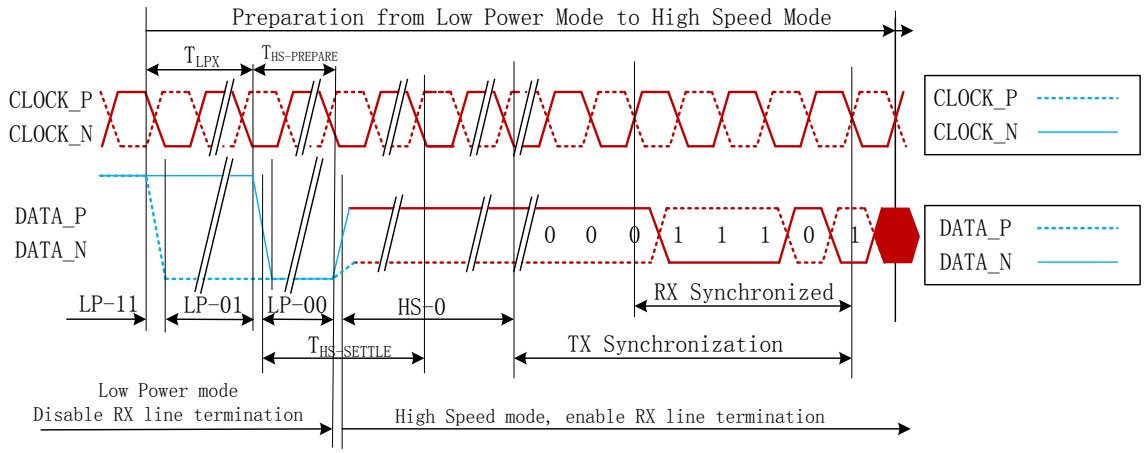
4.3.2.2.1 Entering High-Speed Data Transmission (TSOT of HSDT)

GC9403 is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLOCK_P/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes DSI-DATA_P/N of GC9403 are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below:



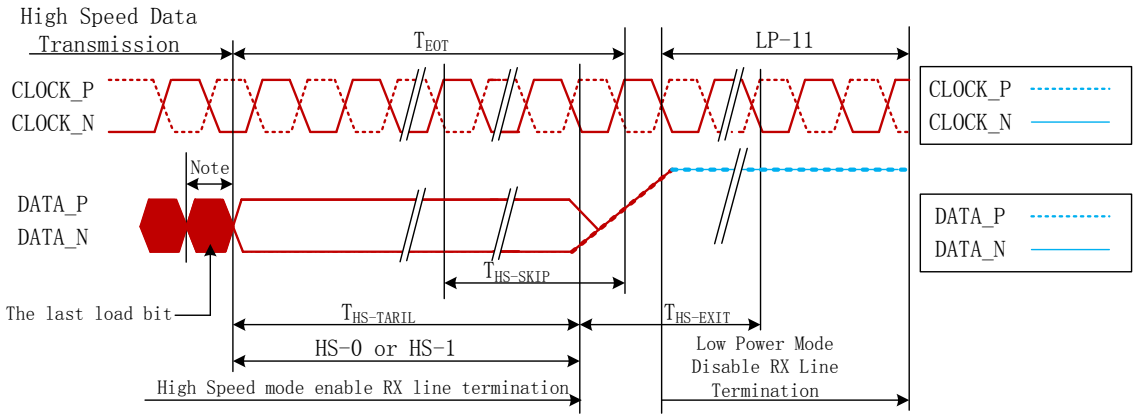
4.3.2.2.2 Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

GC9403 is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLOCK_P/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-DATA_P/N are in LP-11 mode.

Data lanes DSI-DATA_P/N of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

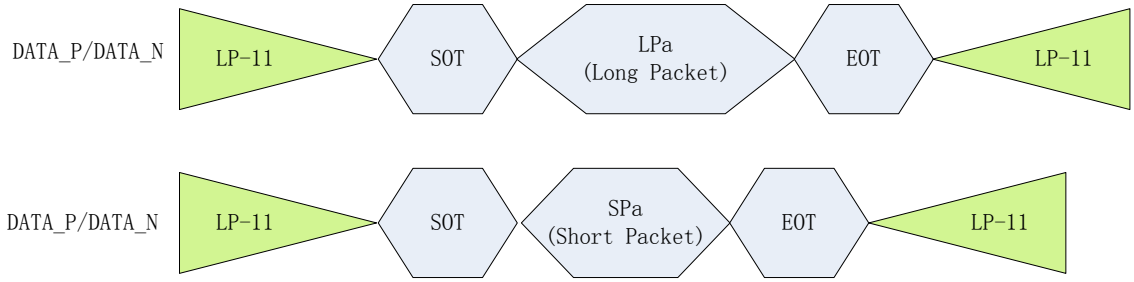
This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



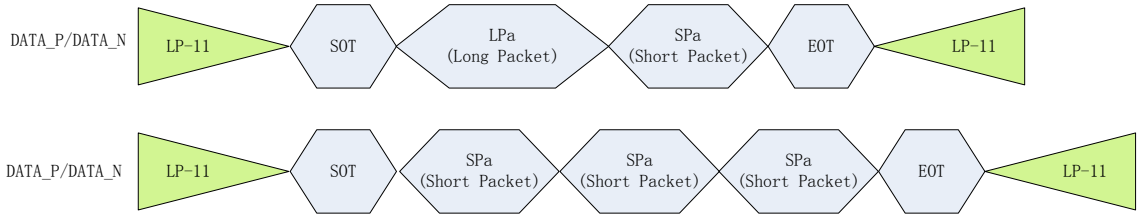
Note: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.3.2.2.3 Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “4.3.3.1 Short Packet (SPa) and Long Packet (LPa) Structures“.
The single packet in High-Speed Data Transmission is illustrated for reference purposes below:



The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:



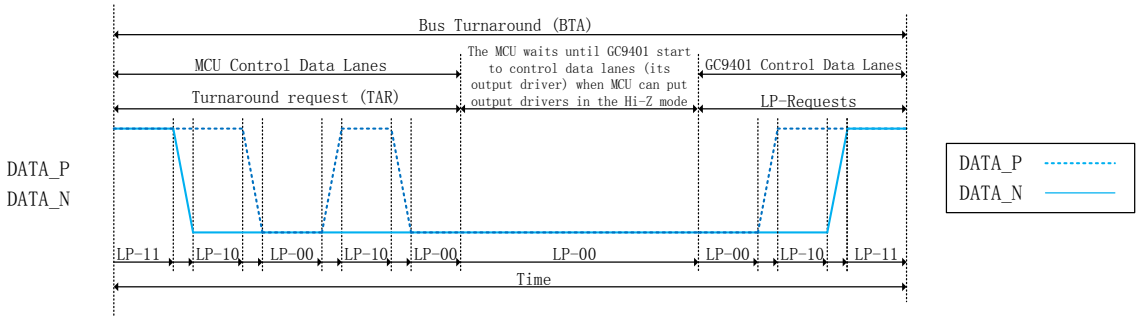
Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

4.3.2.3 Bus Turnaround (BTA)

The MCU or GC9403, which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or GC9403. The MCU and GC9403 are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to GC9403, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00=>LP-10=>LP-00
- The MCU waits until GC9403 is starting to control DSI-DATA_P/N data lanes and the MCU stops to control DSI-DATA_P/N data lanes (= High-Z)
- GC9403 changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to GC9403) is illustrated below:



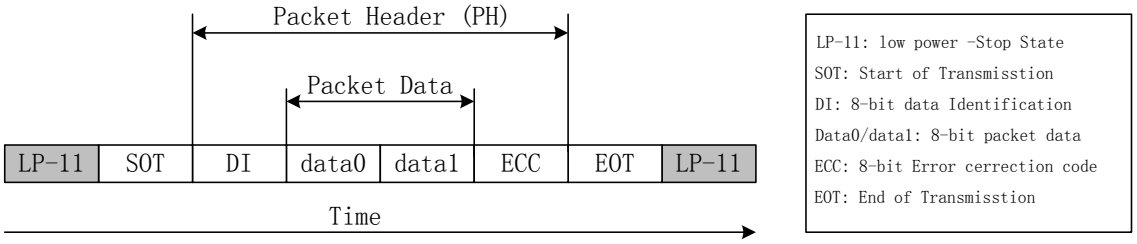
4.3.3 Packet Level Communication

4.3.3.1 Short Packet and Long Packet Structures

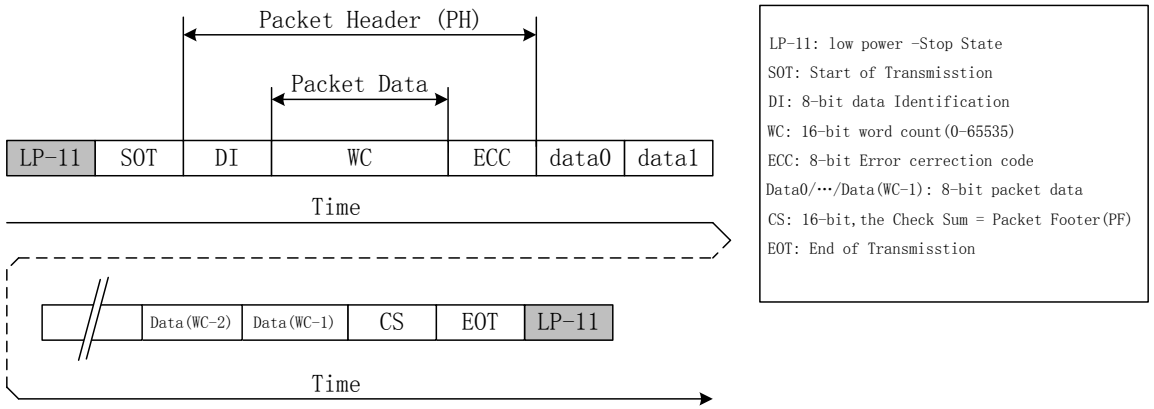
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.
The lengths of the packets are：

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).
The Short Packet structure is illustrated as below:



The Long Packet structure is illustrated as below:

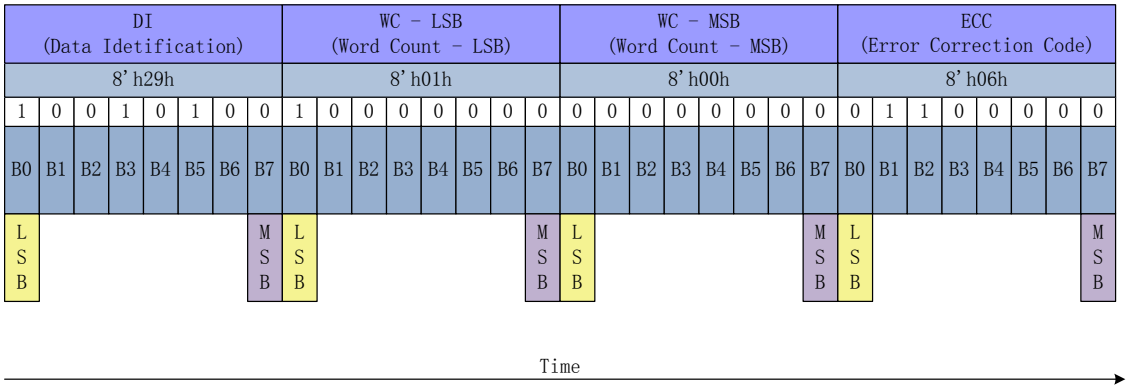


The other possibility is that there is not needed SOT, EOT and LP-11 between packets if packets have sent in multiple packet format e.g.

- LP-11 =>SOT =>SPa =>LPa =>SPa =>SPa =>EOT =>LP-11
- LP-11 =>SOT =>SPa =>SPa =>SPa =>EOT =>LP-11
- LP-11 =>SOT =>LPa =>LPa =>LPa =>EOT =>LP-11

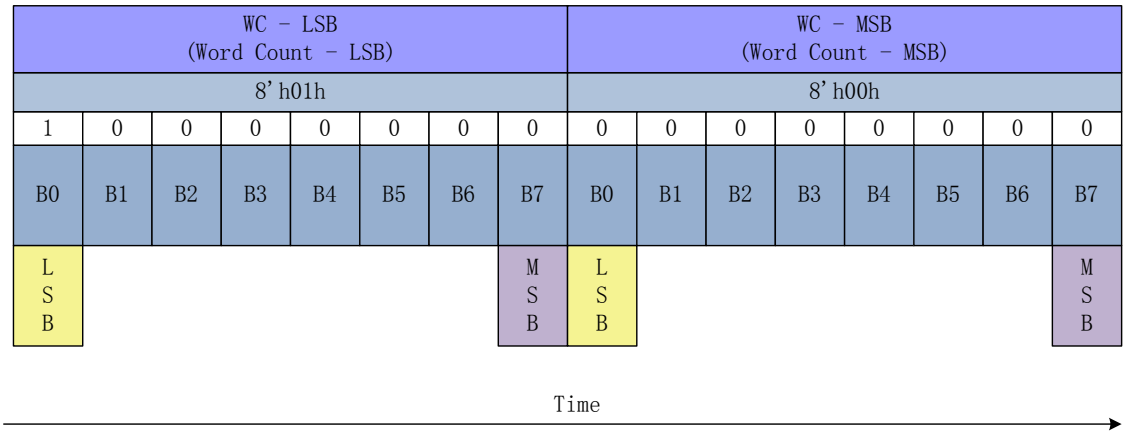
4.3.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.
This same order is illustrated for reference purposes below.



4.3.3.1.2 Byte Order of the Multiple Byte Information on Packets

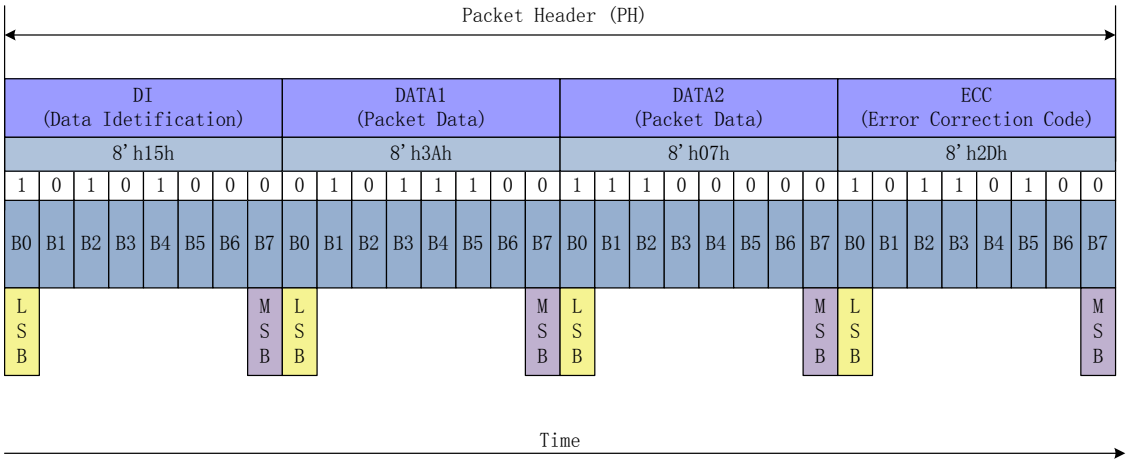
Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.
This same order is illustrated for reference purposes below.



4.3.3.1.3 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).
Short Packet (SPa):

- 1_{st} byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2_{nd} and 3_{rd} bytes: Packet Data (PD), Data 0 and 1
- 4_{th} byte: Error Correction Code (ECC)

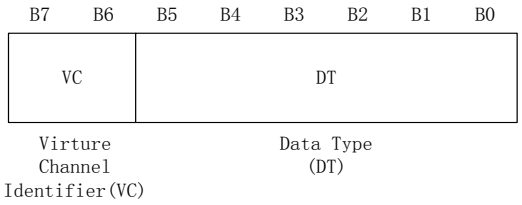


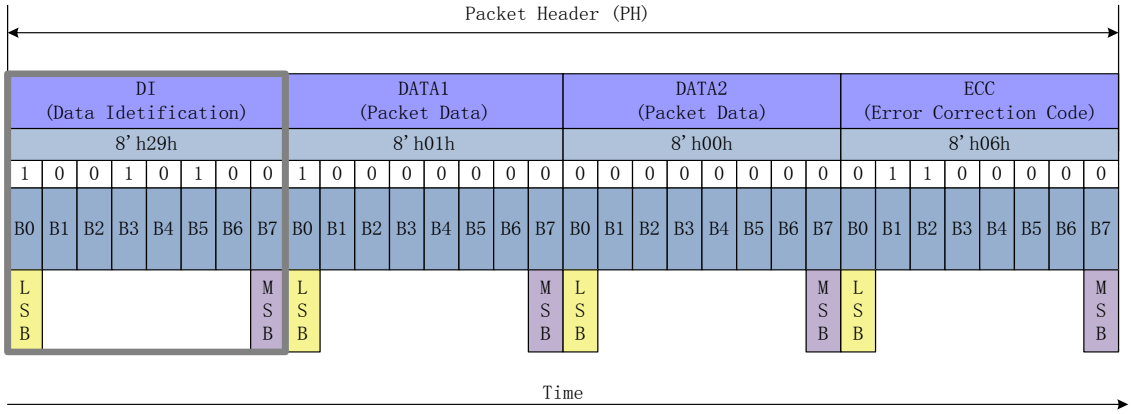
4.3.3.1.3.1 Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated on a diagram below.

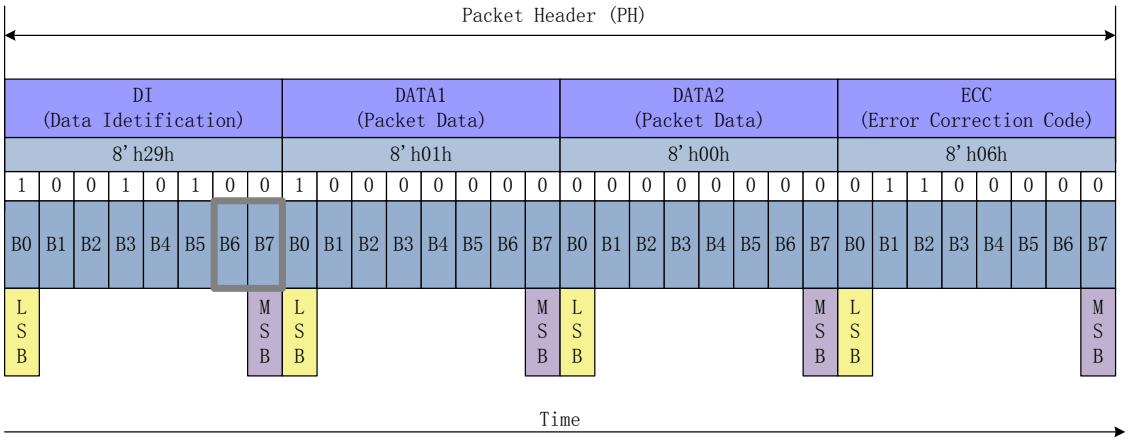




4.3.3.1.3.1.1 Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals.

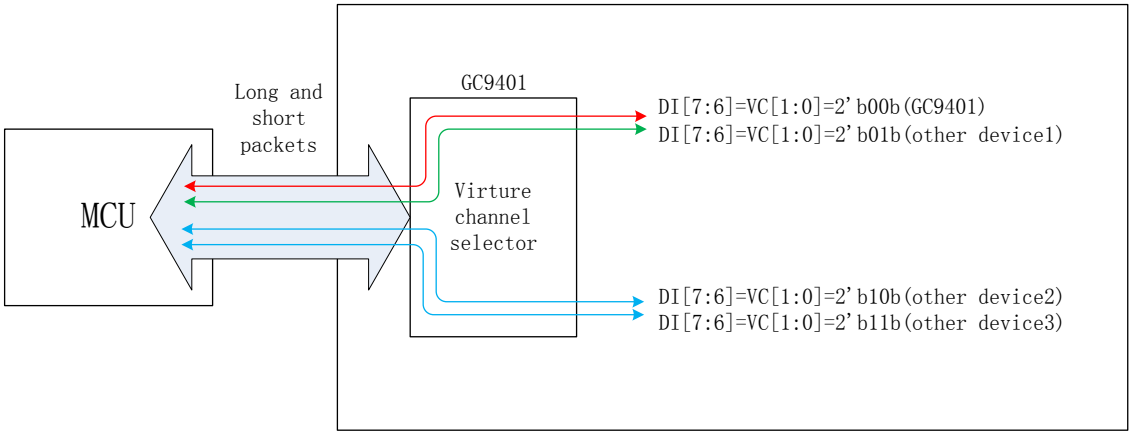
Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.



Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



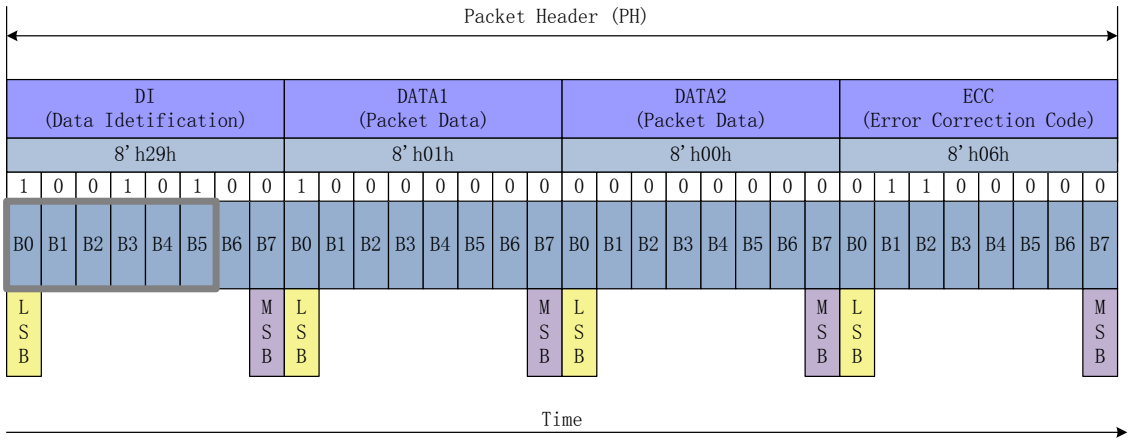
Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00b) when the MCU is sending "End of Transmission Packet" to the display module.

4.3.3.1.3.1.2 Data Type (DT)

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count Field for Long Packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start/end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet.

When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

Data Type (DT) is a part of Data Identification (DI [5…0]) structure and it is used to define a type of the used data on a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.



This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below

From the MCU to GC9403									
B5	B4	B3	B2	B1	B0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note1	Spa (Short Packet)	EOTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Notes: 1. This can be used when the MCU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

2. This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

3. The receiver is ignored other Data Type (DT) if they are not defined on tables.

From the GC9403 to MCU									
B5	B4	B3	B2	B1	B0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	Spa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

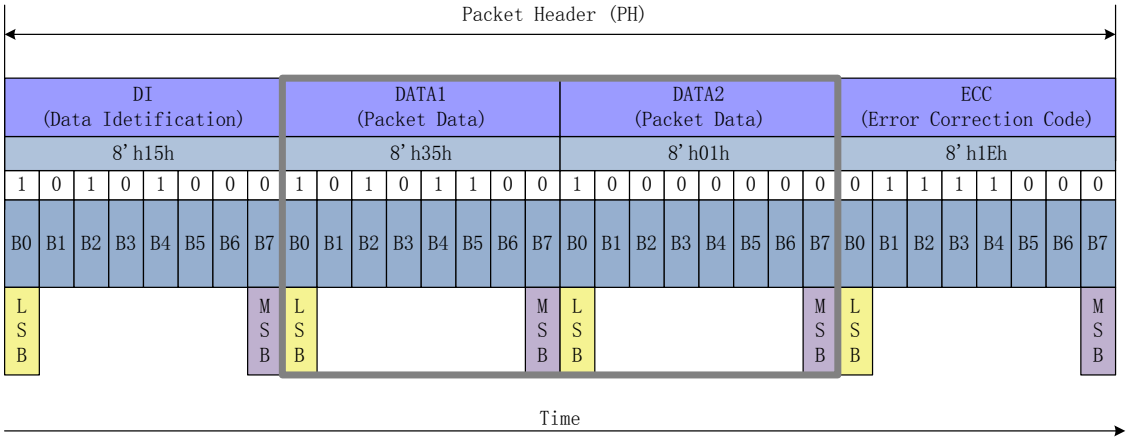
Notes: 1. The receiver is ignored other Data Type (DT) if they are not defined on tables.

4.3.3.1.3.2 Packet Data on the Short Packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.
Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

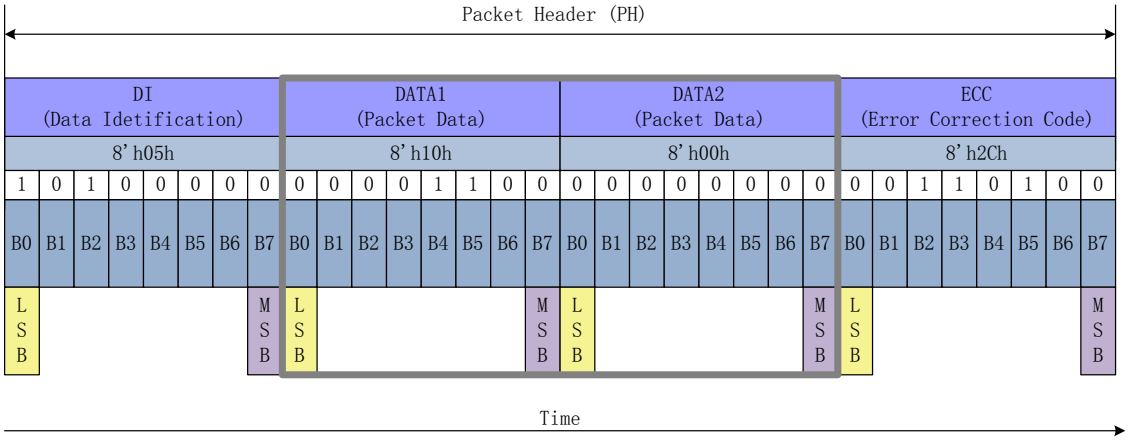
Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)



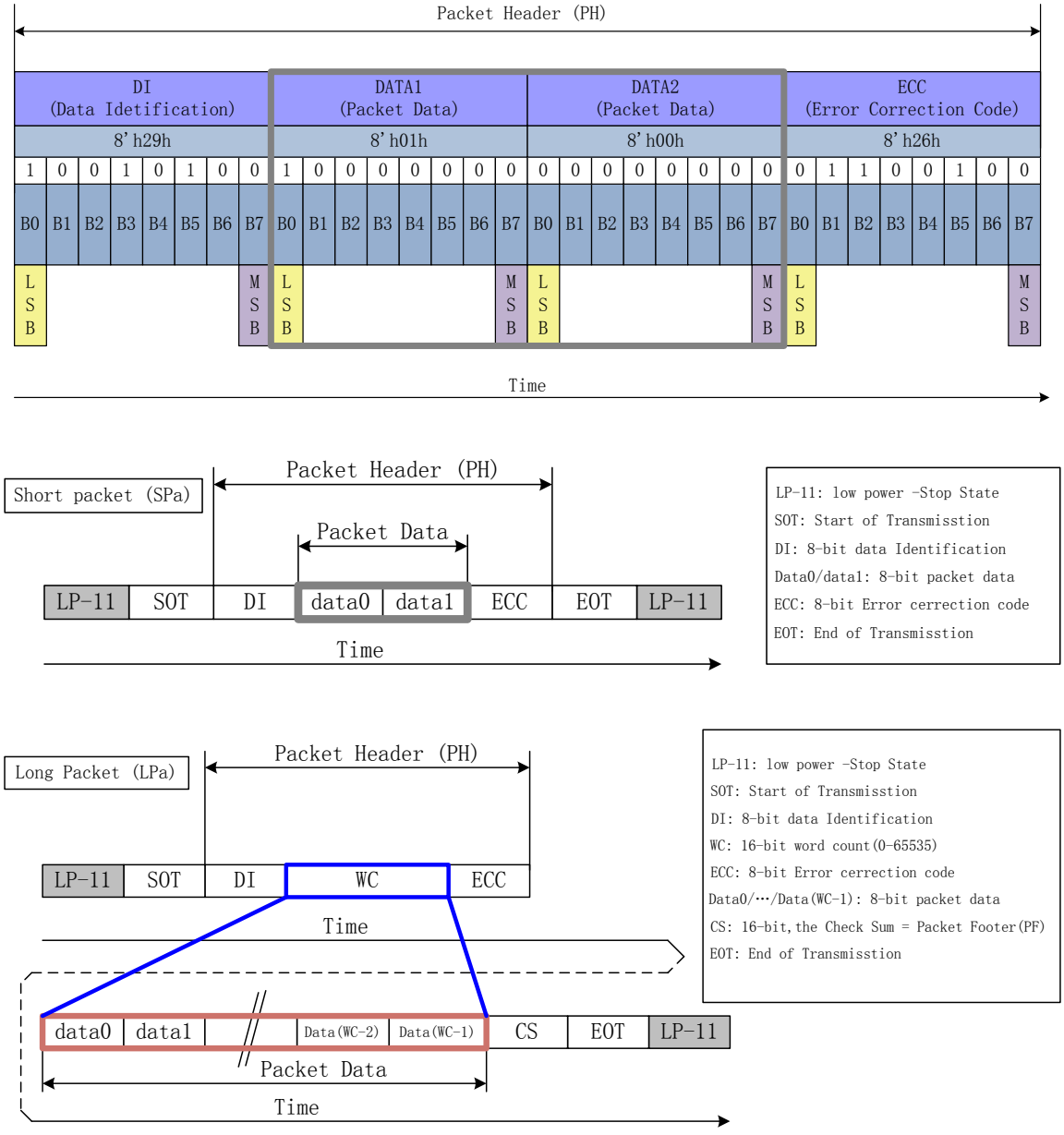
Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)



4.3.3.1.3.3 Word Count on the Long Packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) are placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.
These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.
Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.



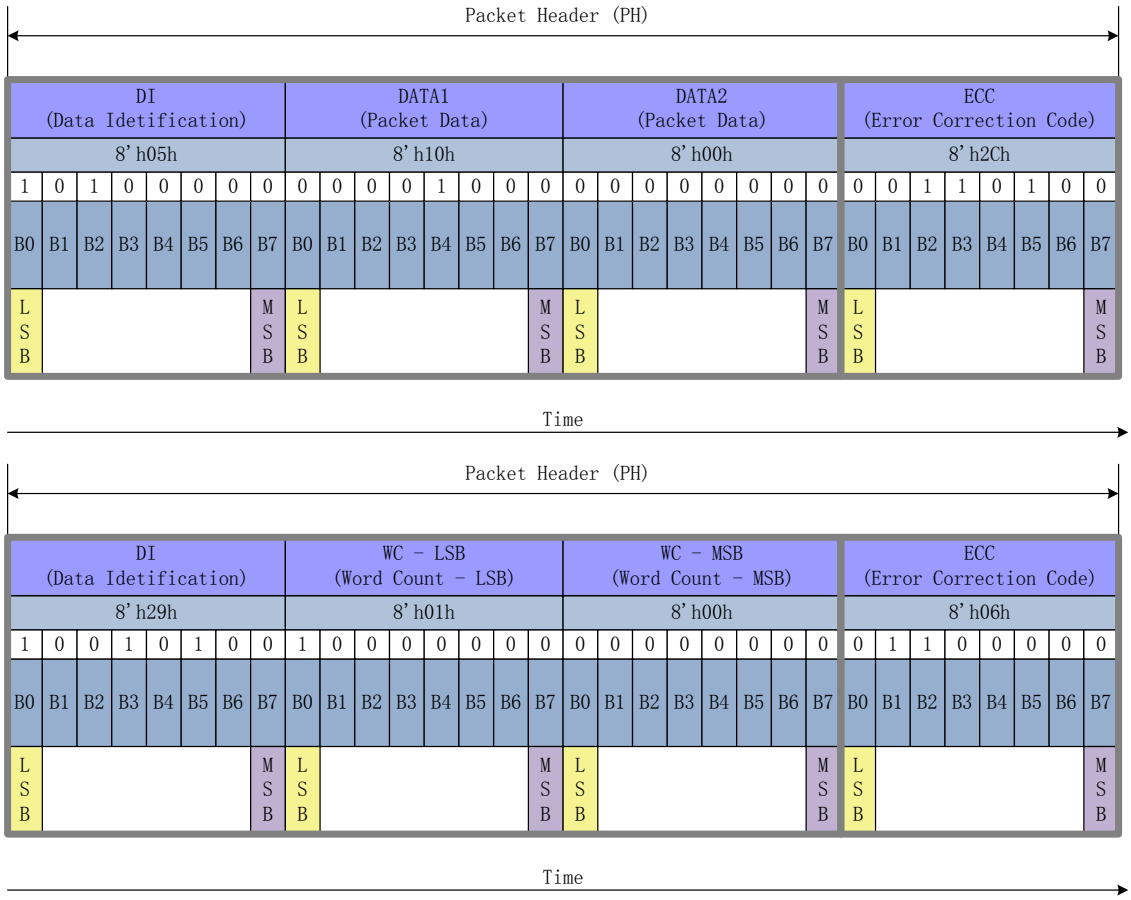
4.3.3.1.3.4 Error Correction Code (ECC)

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte and GC9403 supports ECC in both forward- and reverse-direction communications.

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D [23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D [23…0])

D [23…0] is illustrated for reference purposes below.

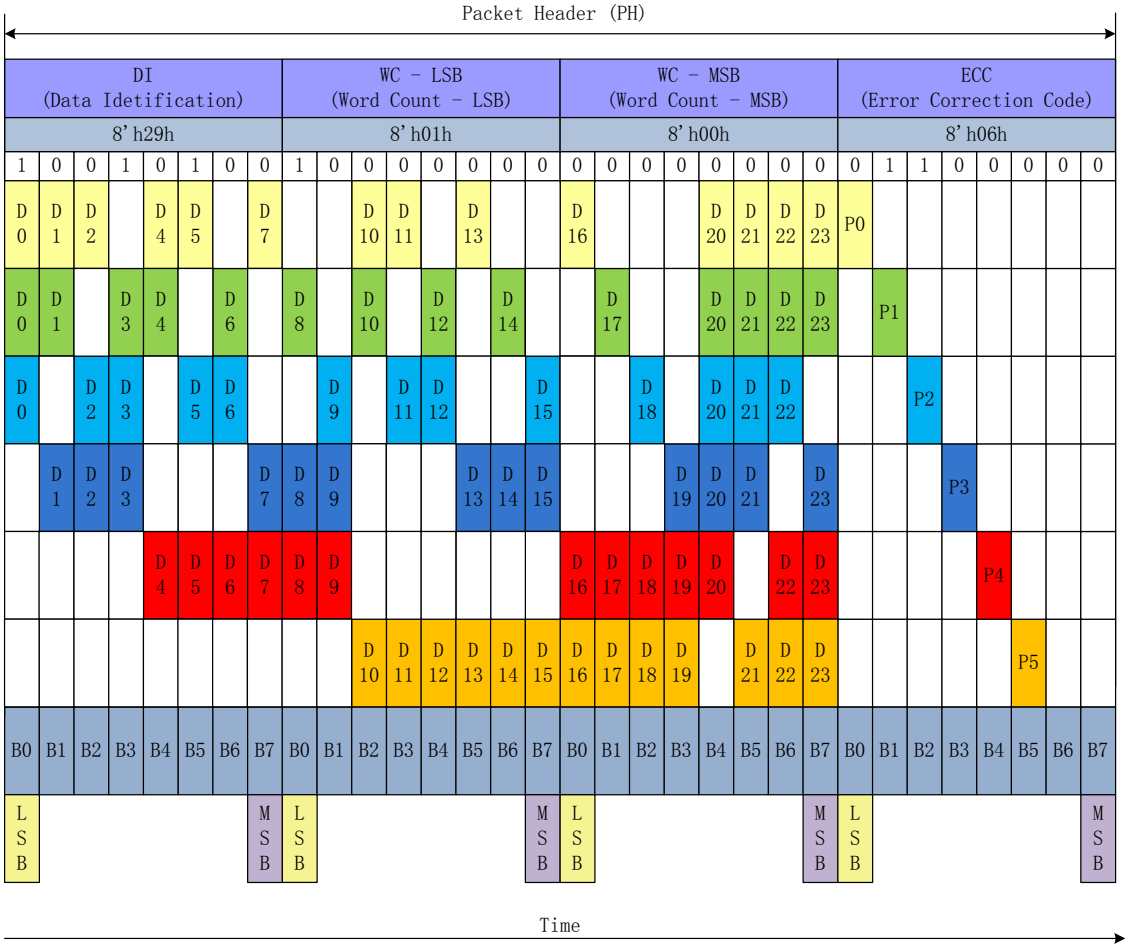


Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

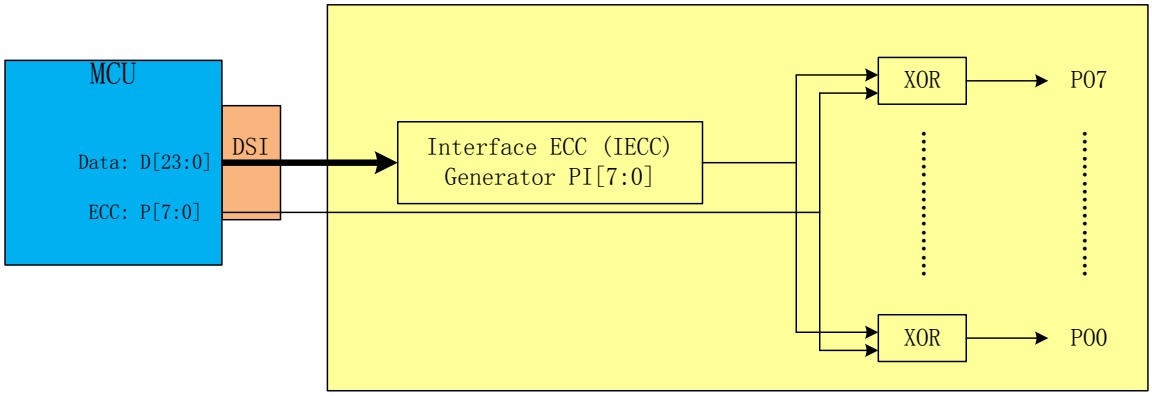
- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



The transmitter (The MCU or GC9403) is sending data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (GC9403 or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this

function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is GC9403, is illustrated for reference purposes below.



The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
(ECC) ⊕ (IECC)→PO[7:0]	0	0	0	0	0	0	0	0	=00h → No Error
	LSB							MSB	

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
(ECC) ⊕ (IECC)→PO[7:0]	0	0	1	1	0	0	0	0	=0Ch → Error
	LSB							MSB	

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

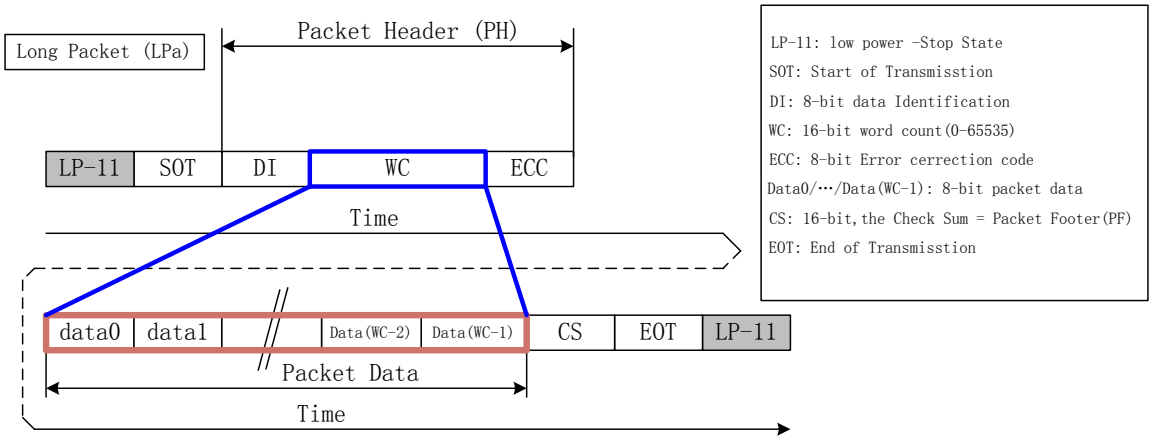
One error is detected if the value of the PO [7…0] is on the above table : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

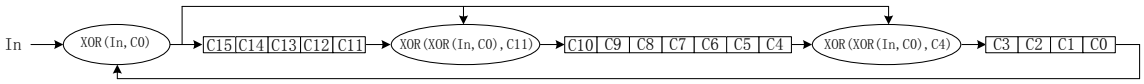
4.3.3.1.4 Packet Data on the Long Packet

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is illustrated as below:

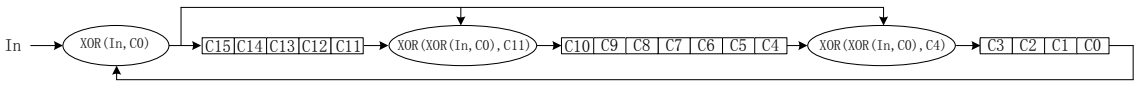


4.3.3.1.5 Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16}+X_{12}+X_5+X_0$ as it is illustrated below.

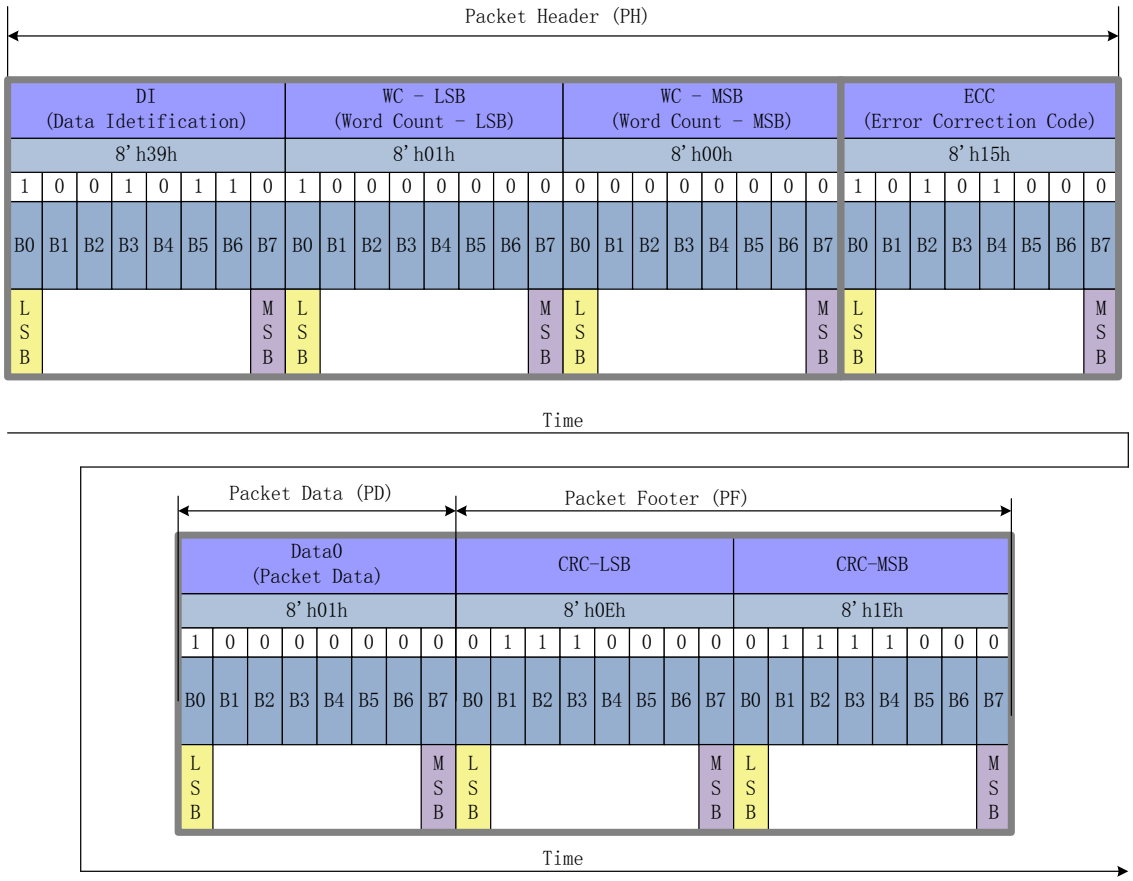


The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.
The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

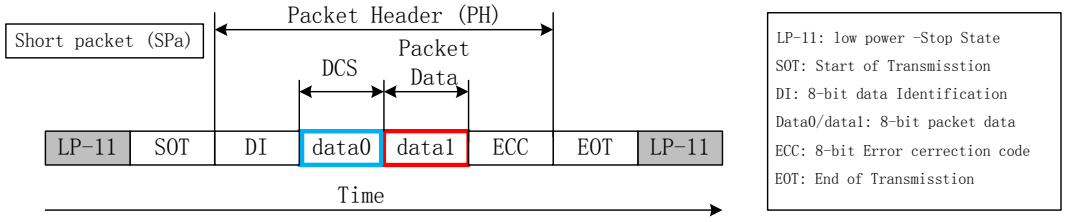
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

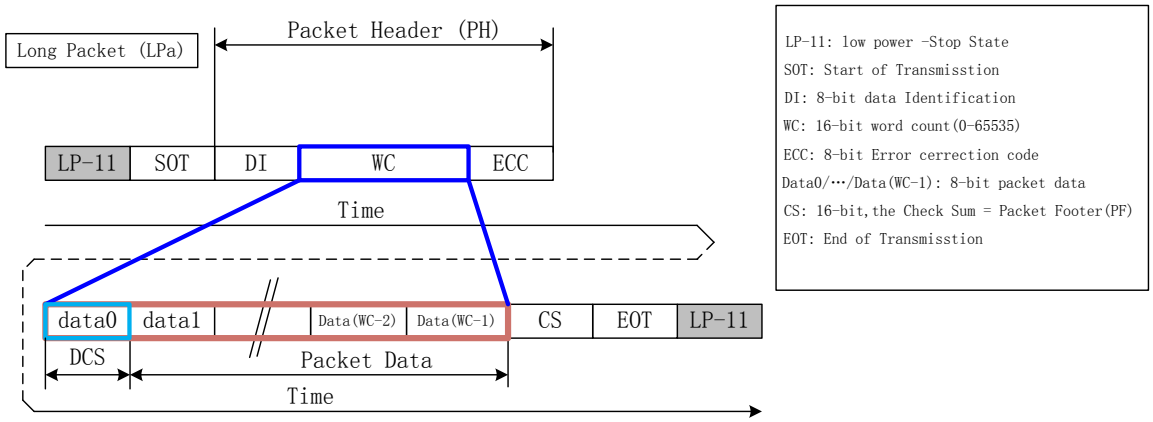
4.3.3.2 Packet Transmissions

4.3.3.2.1 Packet form the MCU to GC9403

4.3.3.2.1.1 Display Command Set (DCS)

Display Command Set (DCS), which is defined on next chapter, is used from the MCU to GC9403. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated as below.





4.3.3.2.1.2 Display Command Set Write, no Parameter (DCSWN-S)

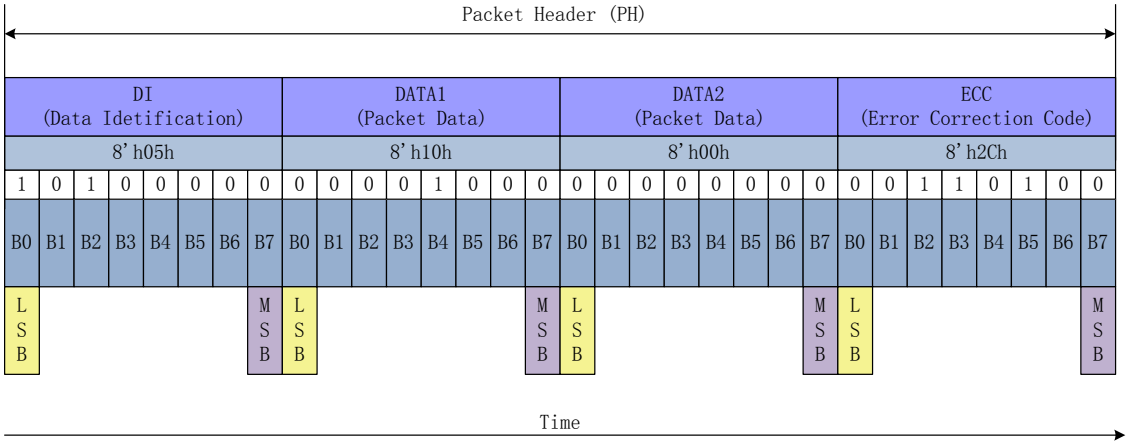
"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to GC9403. These commands are defined on a table below.

Command
NOP (00h)
Software Reset (01h)
Sleep IN (10h)
Sleep Out (11h)
Partial Mode ON (12h)
Normal Display Mode ON (13h)
Display OFF (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode OFF (38h)
Idle Mode ON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.


Packet Header (PH)
DI
(Data Idetification)
DATA1
(Packet Data)
DATA2
(Packet Data)
ECC
(Error Correction Code)
8'h05h
8'h10h
8'h00h
8'h2Ch
1 0 1 0 0 0 0 0
0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0
0 0 1 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7
LSB
MSB
Time

4.3.3.2.1.3 Display Command Set Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to GC9403. These commands are defined on a table below.

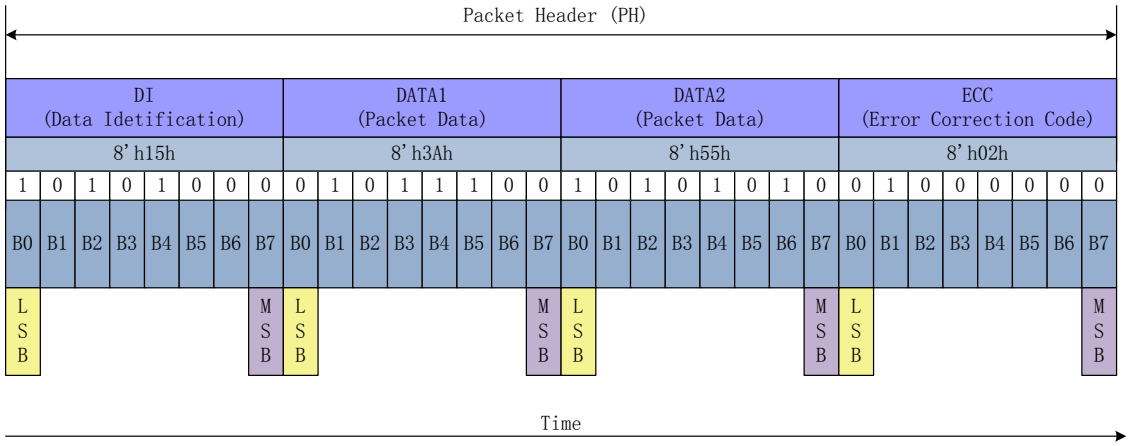
Command
Memory Write (2Ch), Note
Tearing Effect Line ON (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Partial Mode ON (12h)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Tearing Effect Line OFF (34h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note: One Subpixel has been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: "Interface Pixel Format (3Ah)", Display Command Set (DCS)
  - Data 1: 55hex, Parameter of the DCS.
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



4.3.3.2.1.4 Display Command Set Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to GC9403. Command (No Parameters) and Write (1 or more parameters) are defined on a table below.

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep IN (10h) , Note 1
Sleep Out (11h) , Note 1
Partial Mode ON (12h) , Note 1
Normal Display Mode ON (13h) , Note 1
Display OFF (28h) , Note 1
Display ON (29h) , Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), Note 2
Partial Area (30h)
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode OFF (38h) , Note 1
Idle Mode ON (39h) , Note 1
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note 2
Write Display Brightness (51h), Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

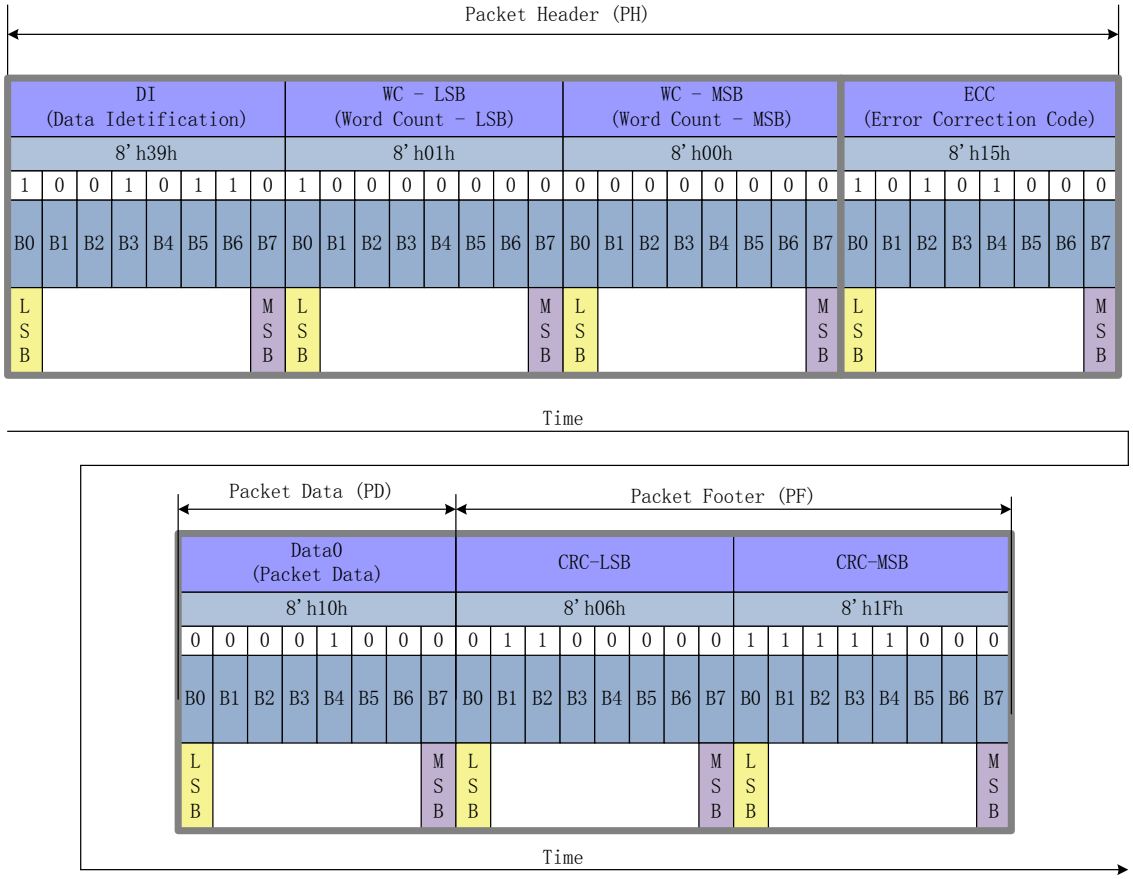
Notes: (1) Also Short Packet (SPa) can be used; See chapter "4.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter"

(2) Also Short Packet (SPa) can be used; See chapter "4.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter"

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

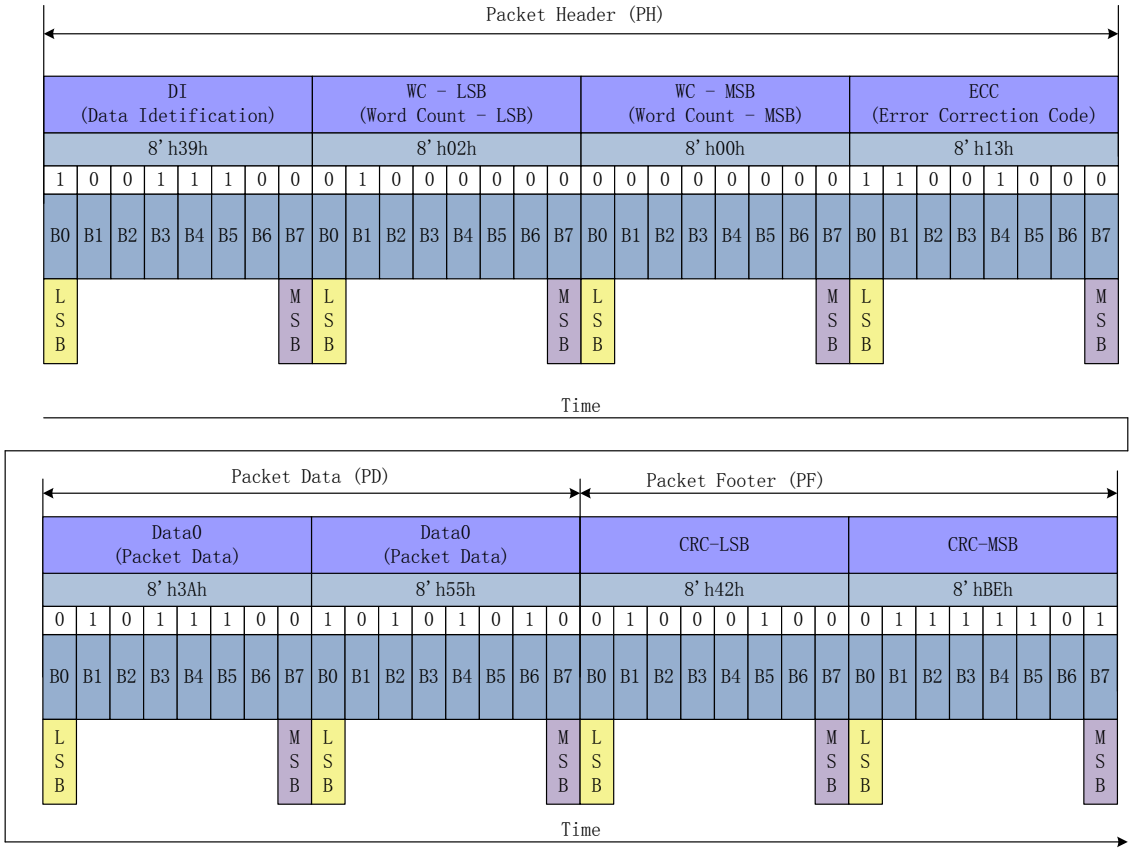
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a command (1 Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Interface Pixel Format (3Ah)”, Display Command Set (DCS)
  - Data 1: 55hex, Parameter of the DCS
- Packet Footer (PF)

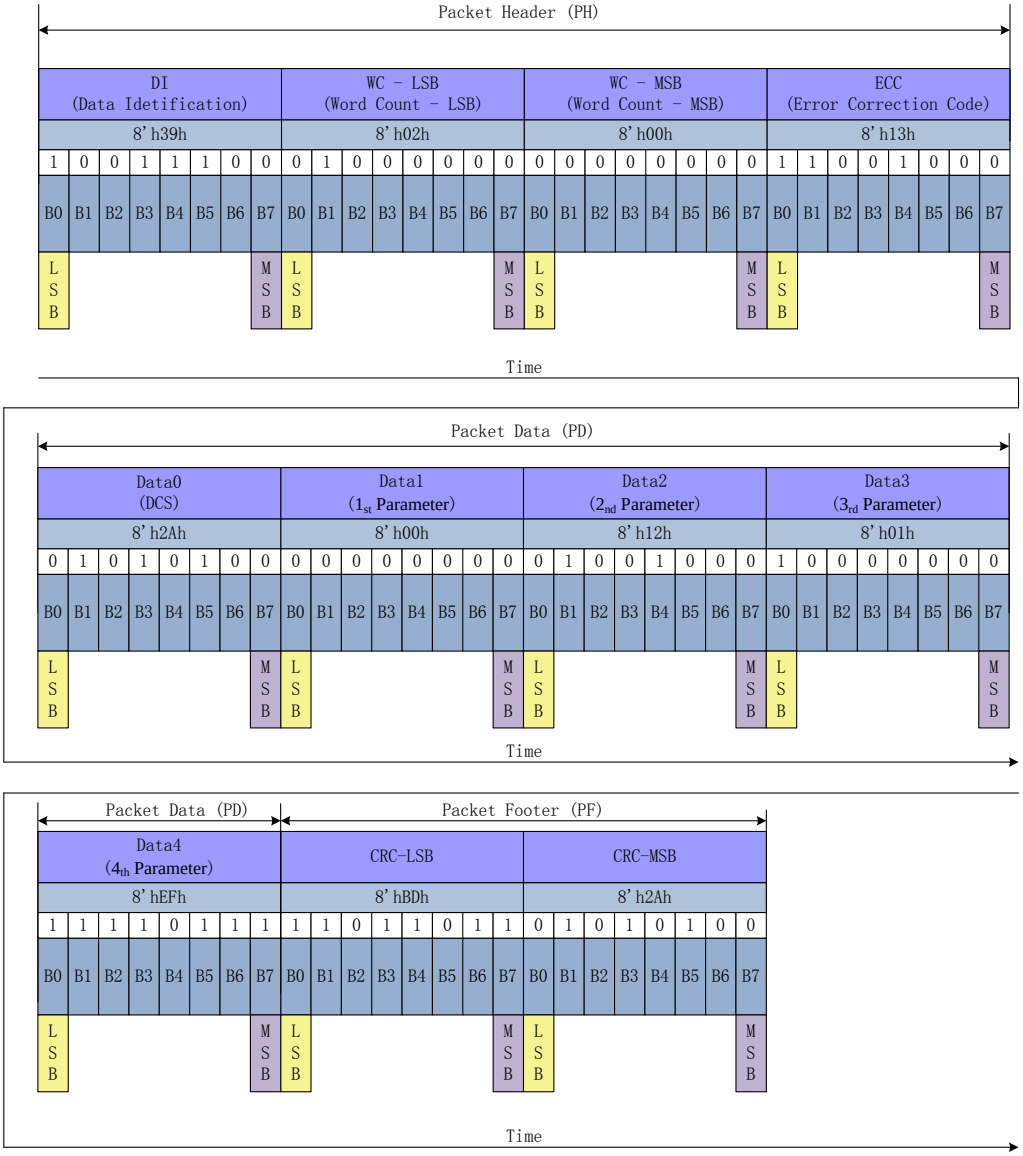
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a command (4 Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)
  - Data 1: 00hex, 1_{st} Parameter of the DCS, Start Column SC [15…8]
  - Data 2: 12hex, 2_{nd} Parameter of the DCS, Start Column SC [7…0]
  - Data 3: 01hex, 3_{rd} Parameter of the DCS, End Column SC [15…8]
  - Data 4: 01hex, 4_{th} Parameter of the DCS, End Column SC [7…0]
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


Packet Header (PH)
DI (Data Idetification)
WC – LSB (Word Count – LSB)
WC – MSB (Word Count – MSB)
ECC (Error Correction Code)
8'h39h
8'h02h
8'h00h
8'h13h
Time
Packet Data (PD)
Data0 (DCS)
Data1 (1st Parameter)
Data2 (2nd Parameter)
Data3 (3rd Parameter)
8'h2Ah
8'h00h
8'h12h
8'h01h
Time
Packet Data (PD)
Packet Footer (PF)
Data4 (4th Parameter)
CRC-LSB
CRC-MSB
8'hEFh
8'hBDh
8'h2Ah
Time

4.3.3.2.1.5 Display Command Set Read, No Parameter (DCSRN-S)

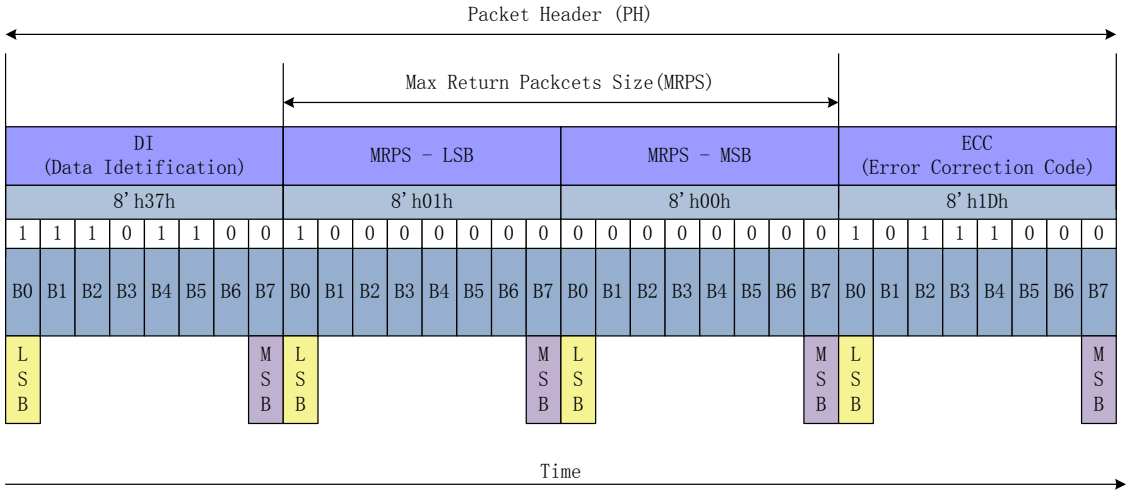
Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to GC9403. These commands are defined on a table below. The 1st parameter (Dummy Data) is not returned as it is done in MCU parallel interface. The first returned parameter is the 2nd parameter in DSI case.

Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh

The MCU has to define to GC9403, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to GC9403. This same sequence is illustrated for reference purposes below.

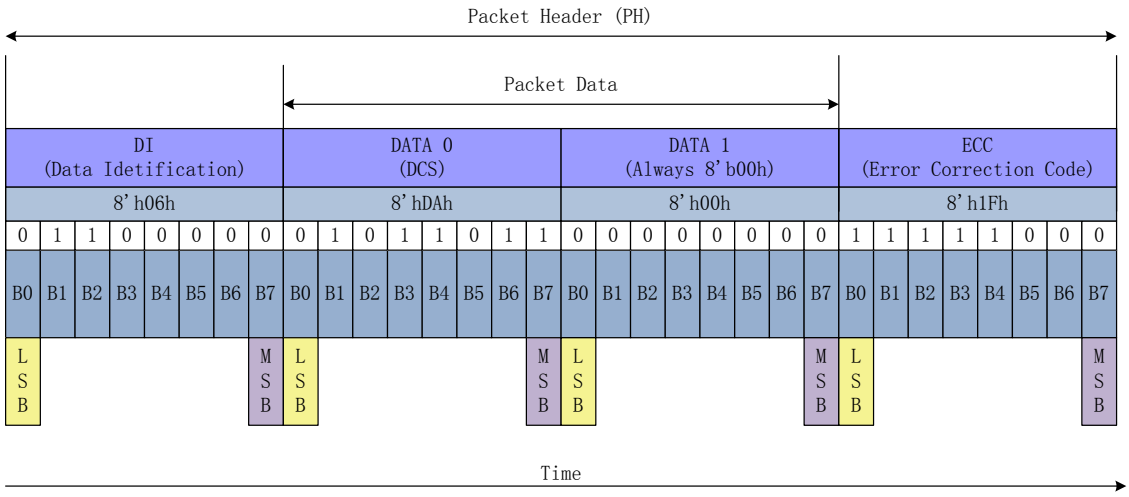
Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to GC9403 when it wants to return one byte from GC9403
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)



Step 2:

- The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to GC9403
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0110b
- Packet Data (PD)
  - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)



Step 3: GC9403 can send 2 different informations to the MCU after Bus Turnaround (BTA)

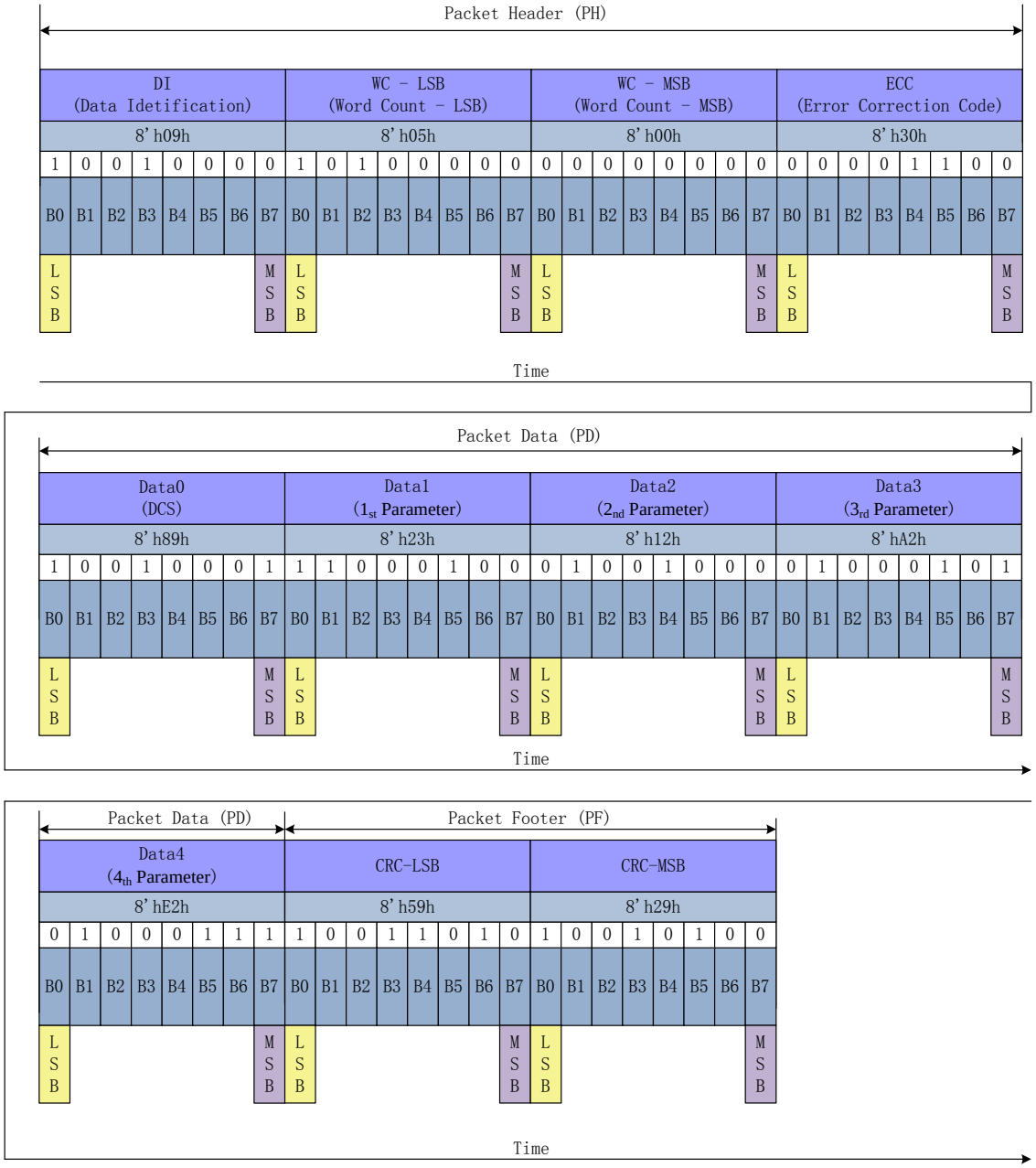
- An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command.
- Information of the received command. Short Packet (SPa) or Long Packet (LPa)

4.3.3.2.1.6 Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 00 1001b), from the MCU to GC9403. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. GC9403 is ignored Packet Data (PD) what the MCU is sending.
Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


Packet Header (PH)
DI
(Data Idetification)
WC - LSB
(Word Count - LSB)
WC - MSB
(Word Count - MSB)
ECC
(Error Correction Code)
8'h09h
8'h05h
8'h00h
8'h30h
1 0 0 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Data0
(DCS)
Data1
(1st Parameter)
Data2
(2nd Parameter)
Data3
(3rd Parameter)
8'h89h
8'h23h
8'h12h
8'hA2h
1 0 0 1 0 0 0 1 1 1 0 0 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0 1 0 1
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB LSB MSB
Time
Packet Data (PD)
Packet Footer (PF)
Data4
(4th Parameter)
CRC-LSB
CRC-MSB
8'hE2h
8'h59h
8'h29h
0 1 0 0 0 1 1 1 1 0 0 1 1 0 1 0 1 0 0 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7 B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB LSB MSB LSB MSB
Time

4.3.3.2.1.7 End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MCU to GC9403. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before"End of Transmission" (EoT), which is an interface level functionality.

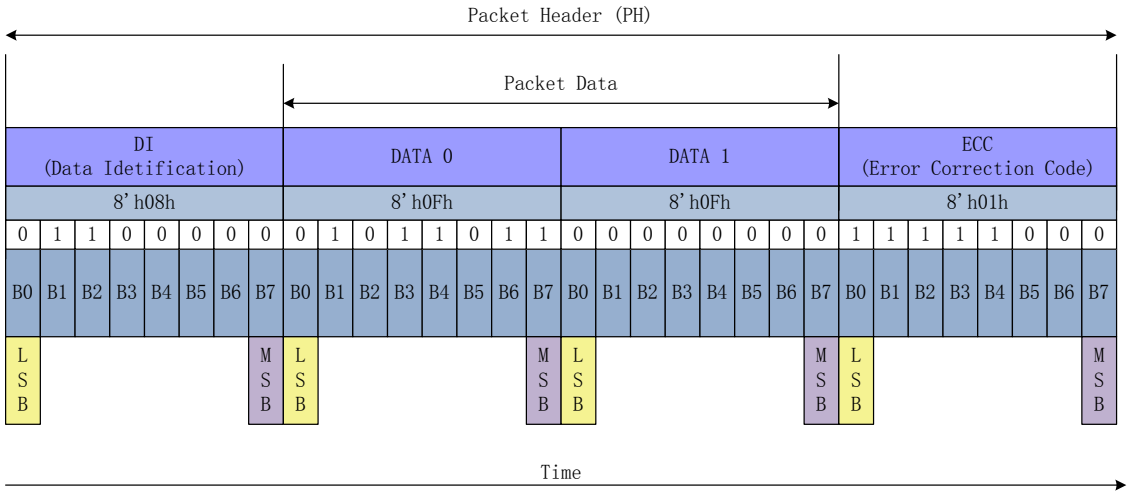
"End of Transmission Packet" (EoTP) should also be supported in the Low Power Data Transmission (LPDT) mode on GC9403e even if this functionality has not been designed for this purposes.

The MCU can decide if it wants to use these "End of Transmission Packet" (EoTP) or not but GC9403 has to be supporting both modes: With or Without "End of Transmission Packet" (EoTP).

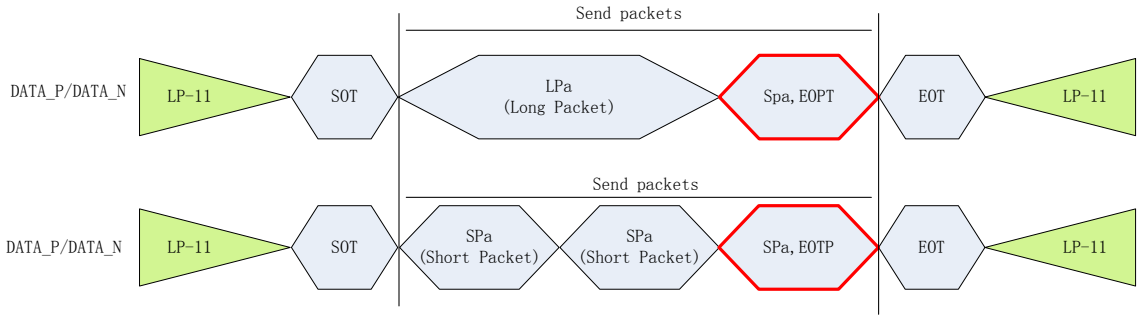
Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code (ECC)
  - ECC: 01hex

This is defined on the Short Packet (SPa) as follows.



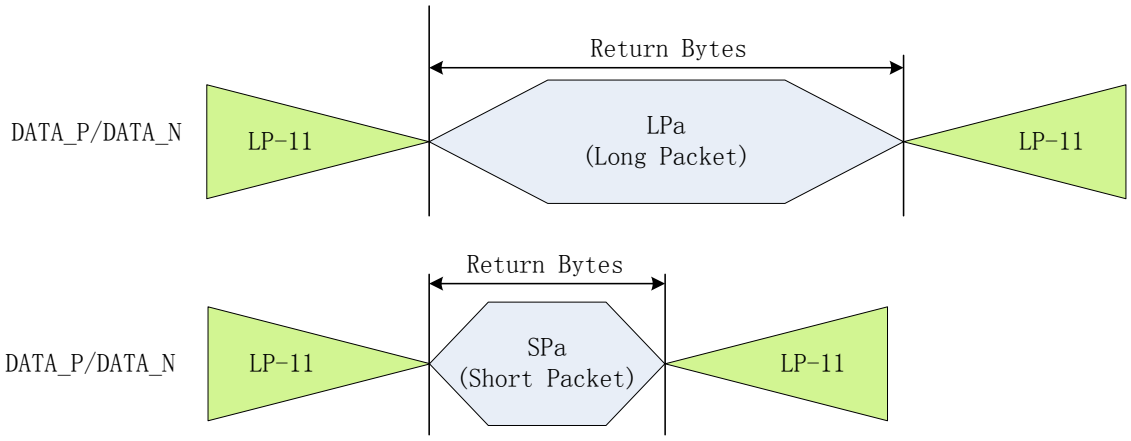
Some use cases of the "End of Transmission Packet" (EoTP) are illustrated only for reference purposes below.


Send packets
DATA_P/DATA_N
LP-11
SOT
LPa
(Long Packet)
Spa, EOPT
EOT
LP-11
Send packets
DATA_P/DATA_N
LP-11
SOT
SPa
(Short Packet)
SPa
(Short Packet)
SPa, EOTP
EOT
LP-11

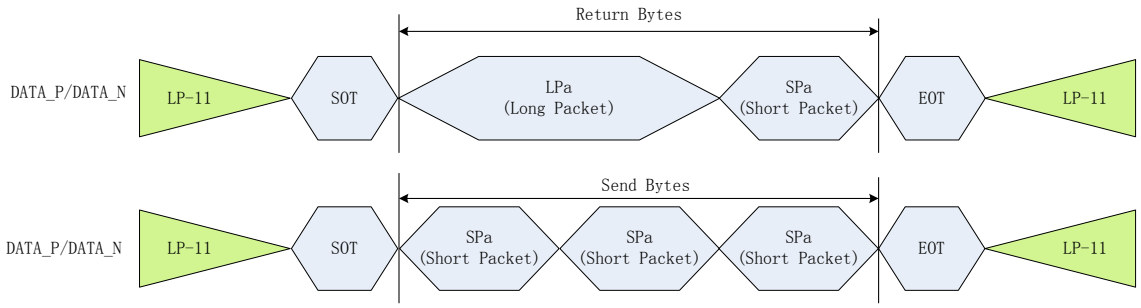
4.3.3.2.2 Packet from GC9403 to MCU

4.3.3.2.2.1 Used Packet Types

GC9403 is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from GC9403. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report (AwER). The used packet type is defined on Data Type (DT).
It is not possible that GC9403 is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.
The return bytes on a single packet are illustrated for reference purposes below.



The return bytes on several packets are illustrated for reference purposes below.



4.3.3.2.2.2 Acknowledge with Error Report

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from GC9403 to the MCU.
The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

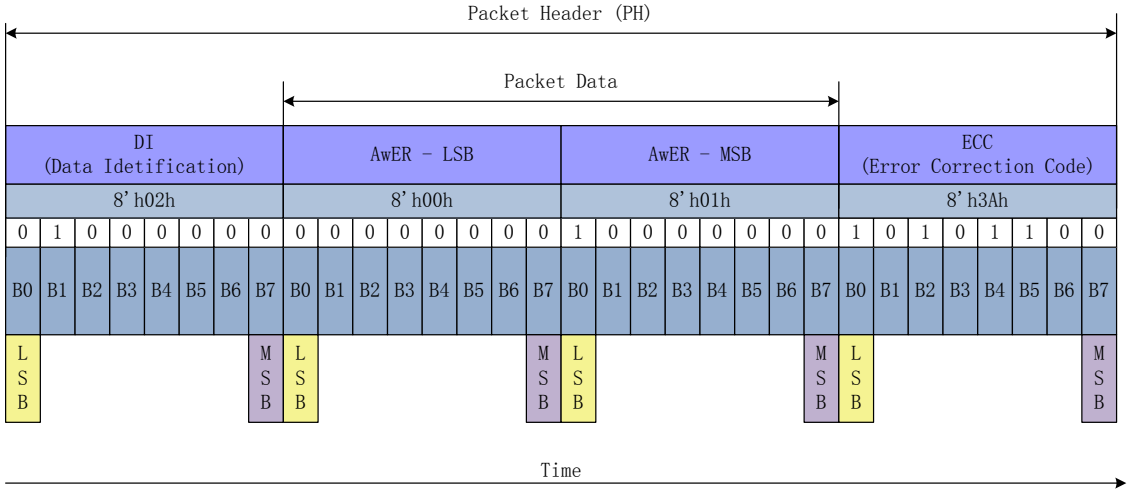
Bit	The Description of Acknowledge Error Report (AwER)	
	Short Packet	Long Packet
0	SoT Error	SoT Error
1	SoT Sync Error	SoT Sync Error
2	EoT Sync Error	EoT Sync Error
3	Escape Mode Entry Command Error	Escape Mode Entry Command Error
4	Low-Power Transmit Error	Low-Power Transmit Error
5	Any Protocol Timer-Out	Any Protocol Timer-Out
6	False Control Error	False Control Error
7	Contention is Detected on the Display Module	Contention is Detected on the Display Module
8	ECC Error, Single-Bit (Detected and Corrected)	ECC Error, Single-Bit (Detected and Corrected)
9	ECC Error, Multi-Bit (Detected, Not Corrected)	ECC Error, Multi-Bit (Detected, Not Corrected)
10	Reserved, Set to '0' internally	Checksum Error
11	DSI Data Type (DT), Not Recognized	DSI Data Type (DT), Not Recognized
12	DSI Virtual Channel (VC) ID Invalid	DSI Virtual Channel (VC) ID Invalid
13	DSI Protocol Violation	DSI Protocol Violation
14	Reserved, Set to '0' internally	Reserved, Set to '0' internally
15	Reserved, Set to '0' internally	Reserved, Set to '0' internally

These errors are included from all packages what has been received from the MCU to GC9403, before Bus Turnaround (BTA). GC9403 ignores the received packet which includes error or errors.

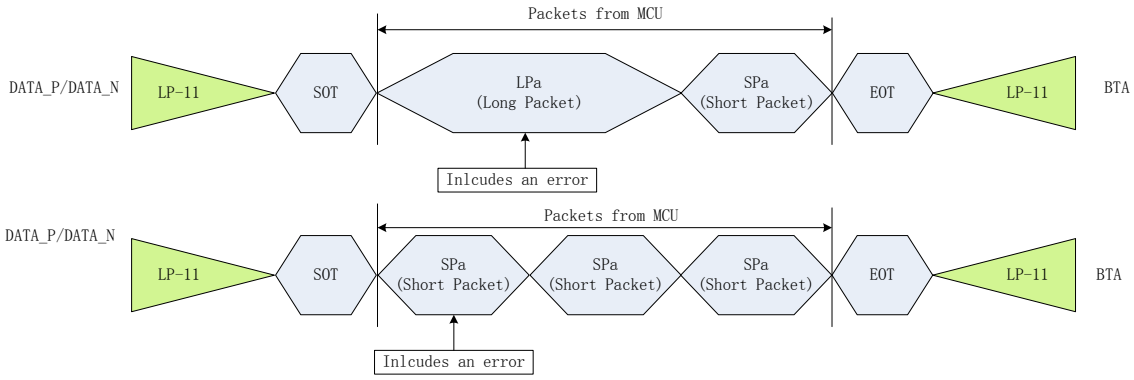
Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

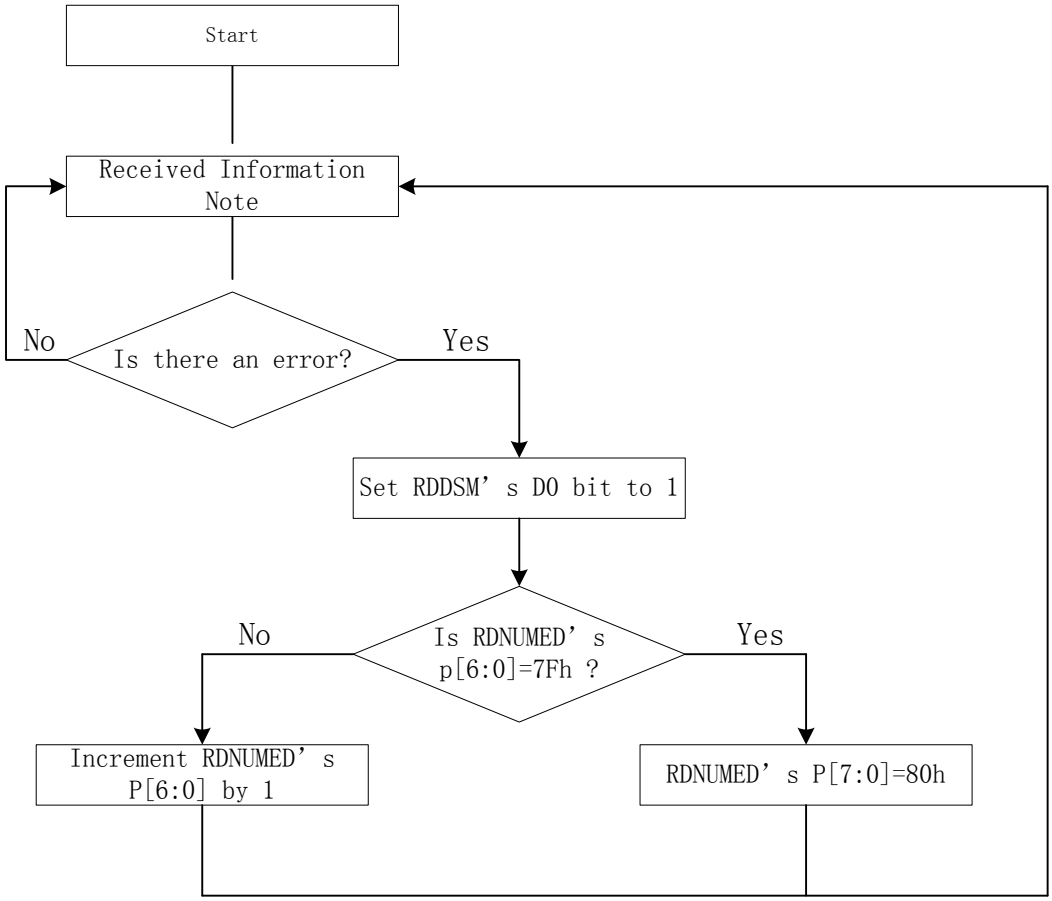


It is possible that GC9403 has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.



Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.
The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.
The numbers of the packets, which are including an error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from GC9403.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note: This information can Interface or Packet Level Communication but it is always from the MCU to GC9403 in this case.

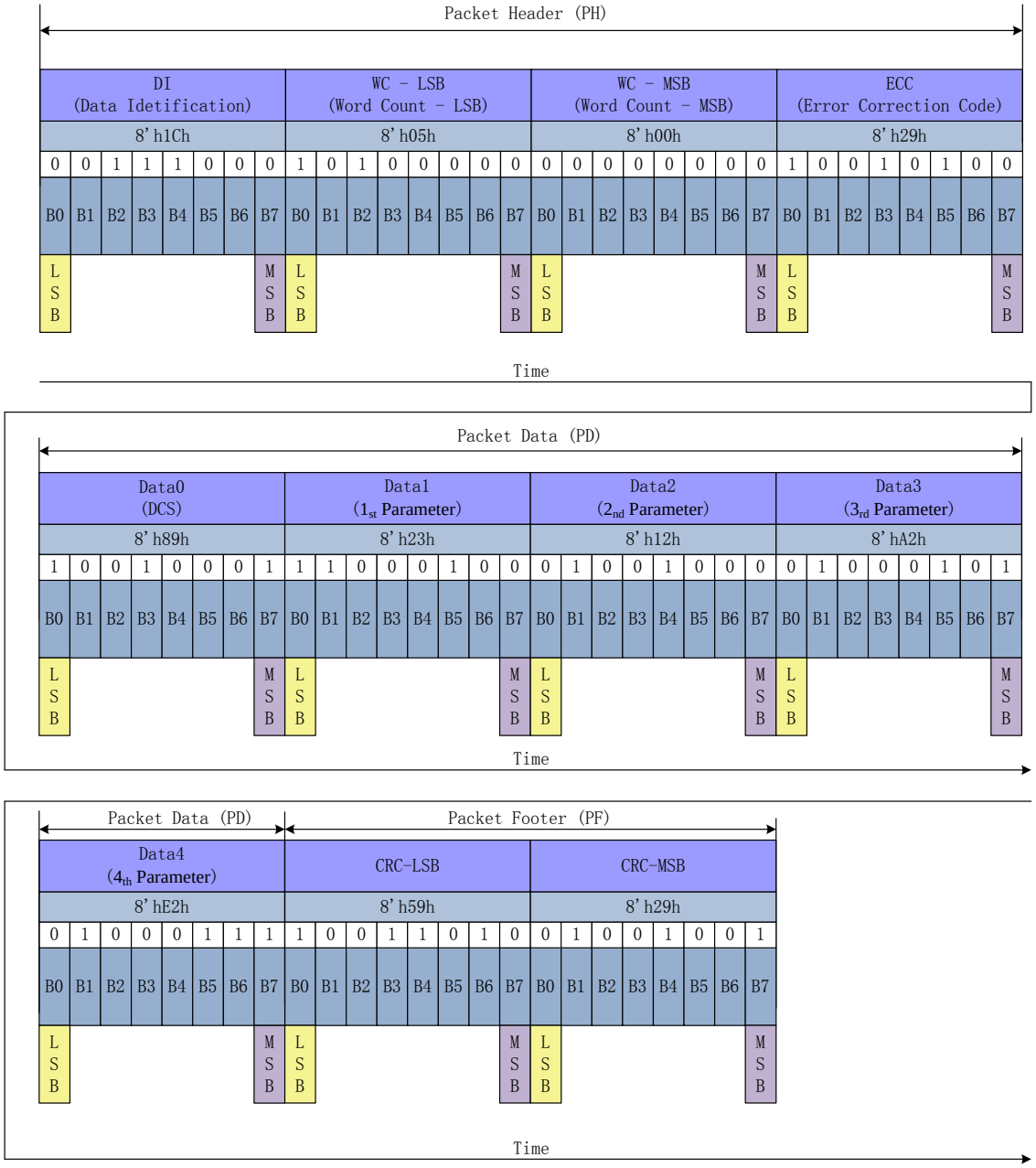
4.3.3.2.2.3 DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from GC9403 to the MCU.
"DCS Read Long Response" (DCSRR-L) is used when GC9403 wants to response a DCS Read command, which the MCU has sent to GC9403.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5⋯0]): 01 1100b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex
  - Data 1: 23hex
  - Data 2: 12hex
  - Data 3: A2hex
  - Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.


Packet Header (PH)
DI
(Data Idetification)
WC - LSB
(Word Count - LSB)
WC - MSB
(Word Count - MSB)
ECC
(Error Correction Code)
8'h1Ch
8'h05h
8'h00h
8'h29h
0 0 1 1 1 0 0 0 | 1 0 1 0 0 0 0 0 | 0 0 0 0 0 0 0 0 | 1 0 0 1 0 1 0 0
B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB | LSB MSB | LSB MSB | LSB MSB
Time
Packet Data (PD)
Data0
(DCS)
Data1
(1st Parameter)
Data2
(2nd Parameter)
Data3
(3rd Parameter)
8'h89h
8'h23h
8'h12h
8'hA2h
1 0 0 1 0 0 0 1 | 1 1 0 0 0 1 0 0 | 0 1 0 0 1 0 0 0 | 0 1 0 0 0 1 0 1
B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB | LSB MSB | LSB MSB | LSB MSB
Time
Packet Data (PD)
Packet Footer (PF)
Data4
(4th Parameter)
CRC-LSB
CRC-MSB
8'hE2h
8'h59h
8'h29h
0 1 0 0 0 1 1 1 | 1 0 0 1 1 0 1 0 | 0 1 0 0 1 0 0 1
B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7 | B0 B1 B2 B3 B4 B5 B6 B7
LSB MSB | LSB MSB | LSB MSB
Time

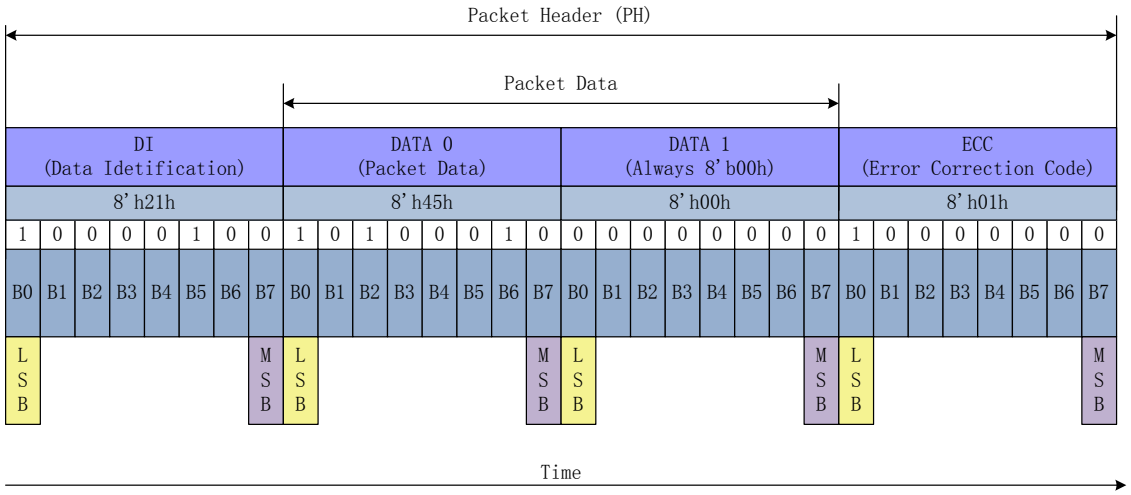
4.3.3.2.2.4 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from GC9403 to the MCU.
"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when GC9403 wants to response a DCS Read command, which the MCU has sent to GC9403.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 00hex (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows



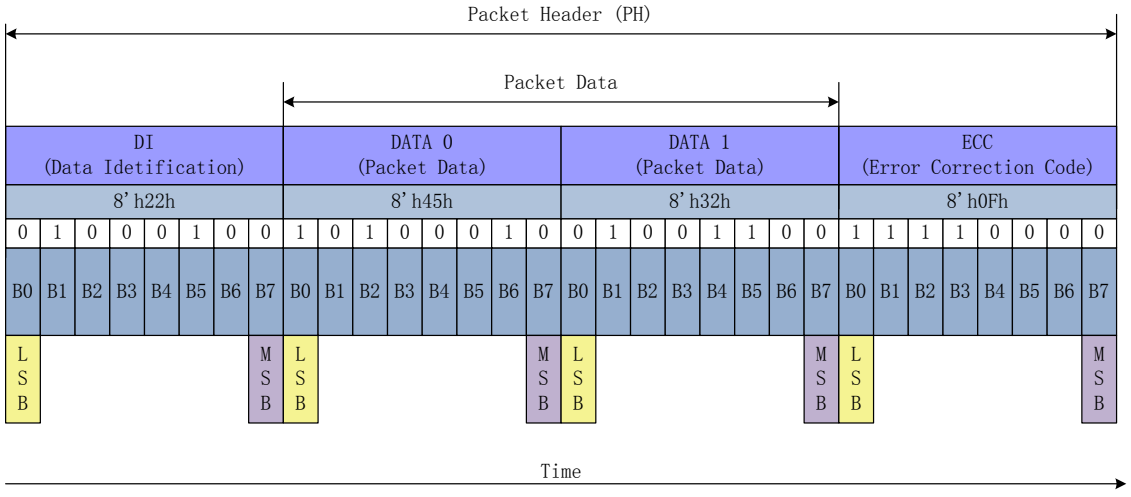
4.3.3.2.2.5 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from GC9403 to the MCU.
"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when GC9403 wants to response a DCS Read command, which the MCU has sent to GC9403.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



4.3.3.3 Communication Sequences

The communication sequences can be done on interface or packet levels between the MCU and GC9403. This communication sequence description is for DSI data lanes (DSI-D0+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.
Functions of the interface level communication are described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low power data transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described on the following table.

Interface	Mode Abbreviation	Packet Size	Interface Action Description
MCU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
GC9403	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

4.3.3.3.1 DCS Write, 1 Parameter Sequence (DCSRR1-S)

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter“4.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, 1 Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, 1 Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9403
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error
9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9403 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

4.3.3.3.2 DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter“4.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 0 Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, 0 Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, 0 Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-S	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9403
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error
9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9403 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

4.3.3.3.3 DCS Write, Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “4.3.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-l	LPDT	→	-	-	
3	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 3						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	
5	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9403
6	-	-	←	LP-11	-	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	-	-	←	ACK		No Error
9	-	-	←	LP-11	-	
10	-	BTA	←→	BTA	-	Interface Control Change from the GC9403 to MCU
11	-	LP-11	→	-	-	End
12						
13	-	-	←	LPDT	AwER	Error Report
14	-	-	←	LP-11	-	
15	-	BTA	←→	BTA	-	
16	-	LP-11	→	-	-	End

DCS Write, Long Parameter Sequence – Example 4						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW1-L	HSDT	→	-	-	Memory Write (2Ch)
3	DCSW1-L	HSDT	→	-	-	Memory Write Continue (3Ch)
4	DCSW1-L	HSDT	→	-	-	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	→			Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	→			End of Transmission Packet
7	-	LP-11	→			End

Note: This is an example where is wanted to send image data in 4 packets.

4.3.3.3.4 DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "4.3.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9403
7	-	-	←	LP-11	-	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is corrected by ECC →Go to Line 19
8						
9	-	-	←	ACK		Responsed 1 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←→	BTA	-	Interface Control Change from the GC9403 to MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error Report
15	-	-	←	LP-11	-	
16	-	BTA	←→	BTA	-	
17	-	LP-11	→	-	-	End
18						
19			←	LPDT	DCSRR1-S	Responsed 1 byte return
20			←	LPDT	AwER	Error Report (Error is Corrected by ECC)

21			←	LP-11	-	
22		BTA	←→	BTA	-	Interface Control Change from the GC9403 to MCU
23		LP-11	→	-	-	End

DCS Read, No Parameter Sequence – Example 2						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	SMRPS-S	HSDT	→	-	-	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	-	-	End of Transmission Packet
5	-	LP-11	→	-	-	
6	-	BTA	←→	BTA	-	Interface Control Change from MCU to GC9403
7	-	-	←	LP-11	-	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is corrected by ECC →Go to Line 19
8						
9	-	-	←	ACK		Responsed 200 byte return
10	-	-	←	LP-11	-	
11	-	BTA	←→	BTA	-	Interface Control Change from the GC9403 to MCU
12	-	LP-11	→	-	-	End
13						
14	-	-	←	LPDT	AwER	Error Report
15	-	-	←	LP-11	-	
16	-	BTA	←→	BTA	-	
17	-	LP-11	→	-	-	End
18						
19			←	LPDT	DCSRR1-S	Responsed 200 byte return
20			←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21			←	LP-11	-	
22		BTA	←→	BTA	-	Interface Control Change from

						the GC9403 to MCU
23		LP-11	→	-	-	End

4.3.3.3.5 Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “4.3.3.2.1.6 Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Null Packet, No Data Sequence – Example						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	NP-L	HSDT	→	-	-	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

4.3.3.3.6 End of Transmission Packet

A Short Packet (SPa) of “End of Transmission Packet (EoTP)” is defined on chapter “4.3.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

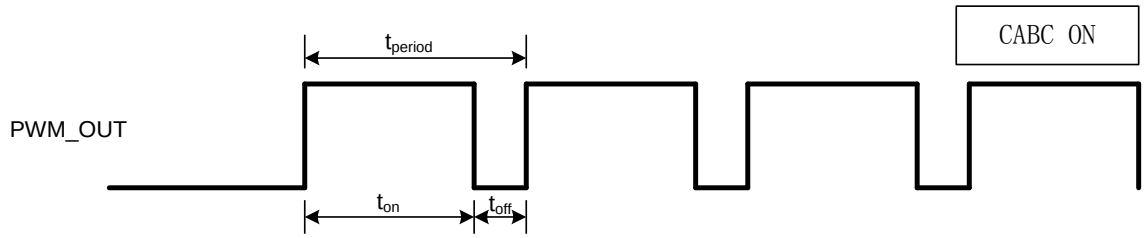
End of Transmission Packet – Example						
line	MCU		Information Direction	GC9403		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	NP-L	HSDT	→	-	-	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	End

4.4 CABC (Content Adaptive Brightness Control)

GC9403 provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. GC9403 will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.
GC9403 can calculate the backlight brightness level and send a PWM pulse to LED driver via PWM_OUT pin for backlight brightness control purpose. The PWM frequency can be adjusted by PWM_DIV parameters and the calculating equation as below:

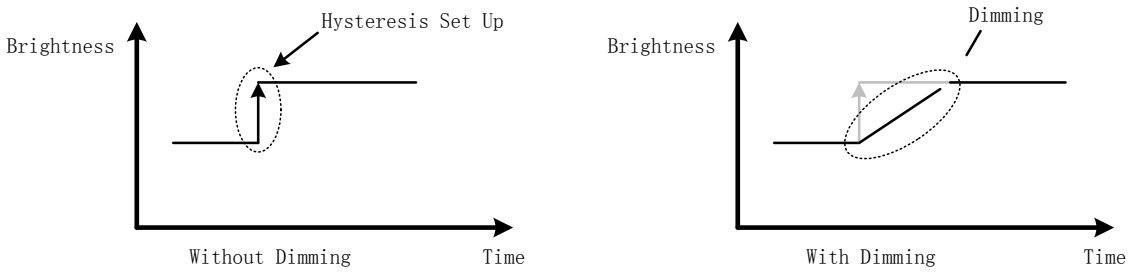
$$f_{PWM\_OUT} = \frac{18MHz}{(PWM\_DIV[7:0]+1)\ X\ 255}$$

The figure in the following is the basic timing diagram which is applied GC9403 to control LED driver.



Display Backlight Dimming Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic idea is described below.

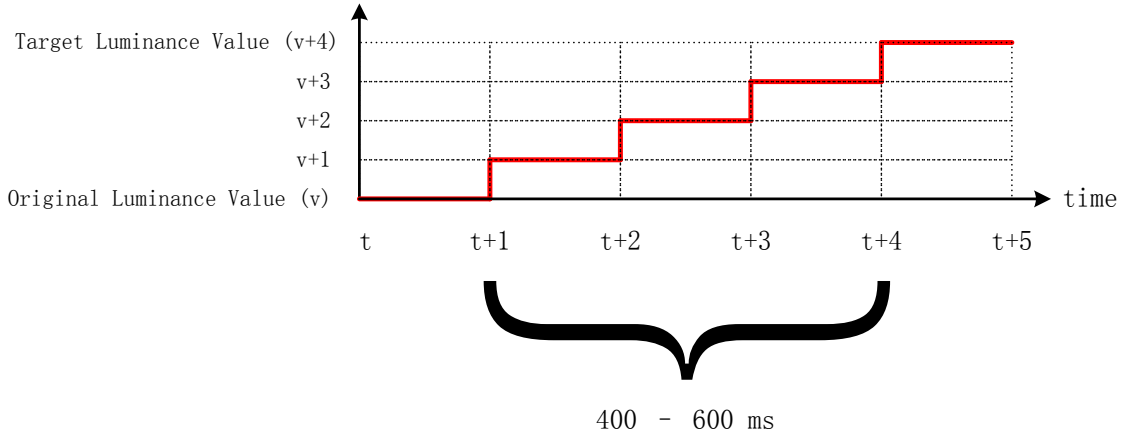


Dimming function can be enabled and disabled. See command “Write CTRL Display(53h), bit3(DD) for more information.

Dimming Requirement

Dimming function in the display module should be implemented so that 400 – 600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions. An upward example is illustrated below.



4.5 Display Data RAM (DDRAM)

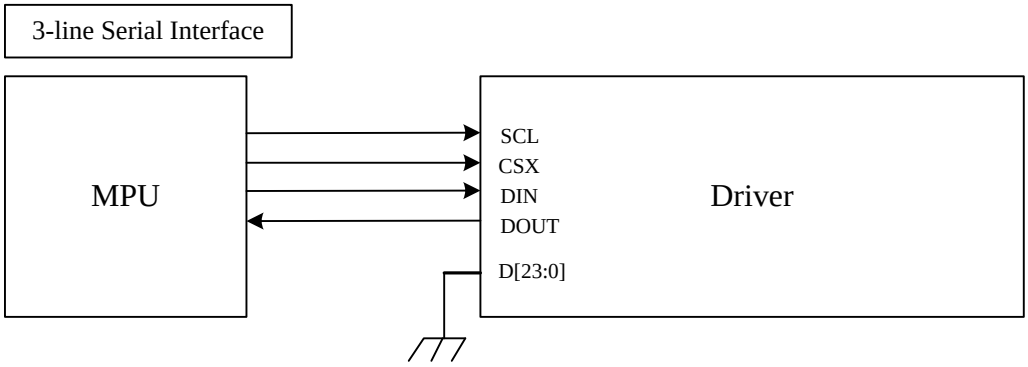
GC9403 has an integrated 320 × 480 × 24-bit graphic type static RAM. This 345,600-byte memory allows storing a 320 × RGB × 480 image with an 24-bit resolution (16.7M-color). No abnormal visual effect shows on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.6 Display Data Format

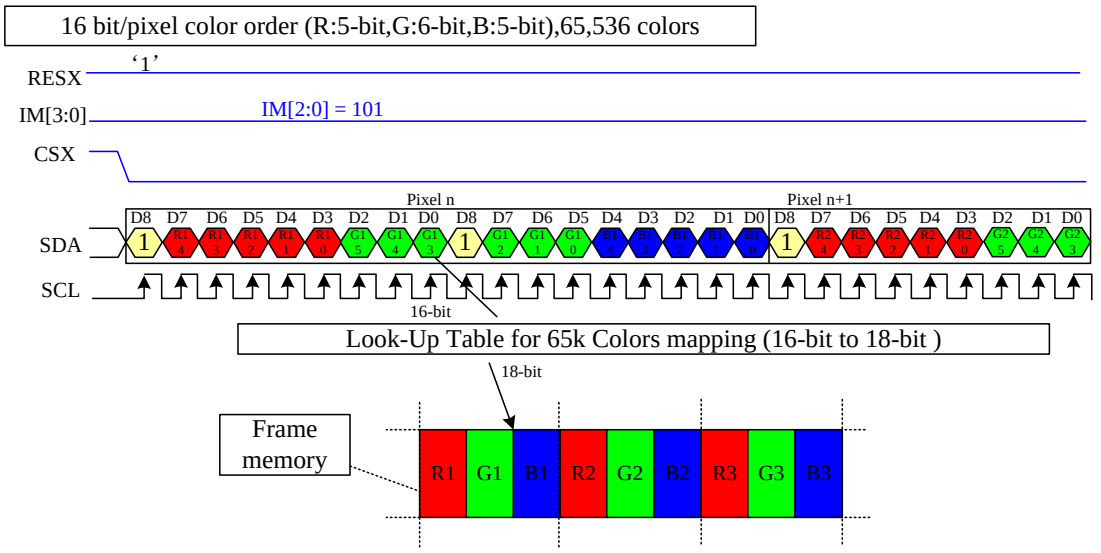
GC9403 supplies 24- / 16- / 9- / 8-bit parallel MCU interface with 8080 series, 3- / 4-line serial interface and 16-/ 18-/ 24-bit parallel RGB interface. The parallel MCU interface and serial interface modes can be selected by external pins IM [2:0].

4.6.1 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9403 is enabled by setting external pins IM[2:0] “101” as shown in the figure below.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.
-65k colors, RGB 5, 6, 5 -bits input
-262k colors, RGB 6, 6, 6 -bits input.
- 16.7M-Colors, RGB 8, 8, 8 -bits input data.

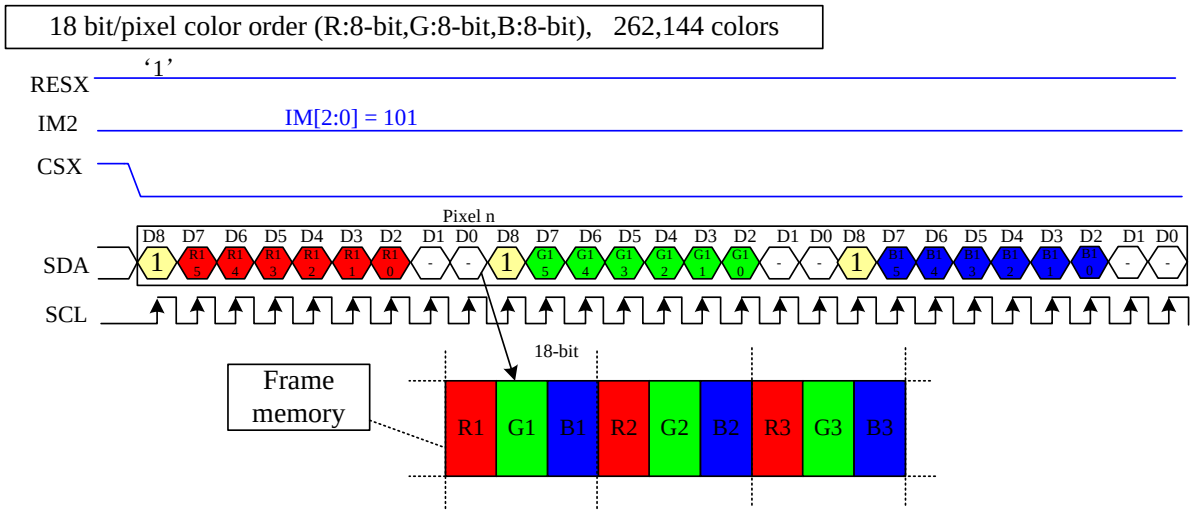


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

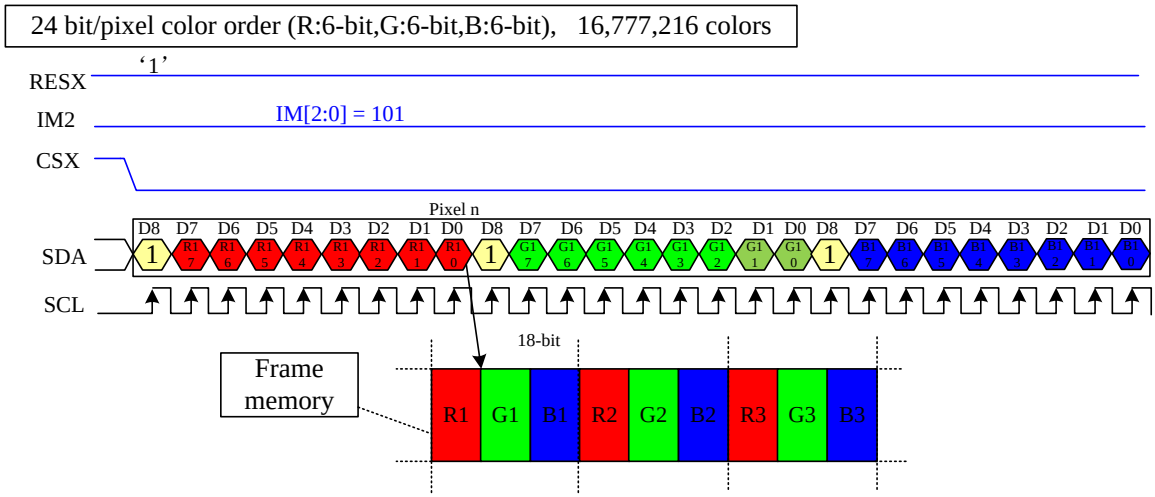


Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".



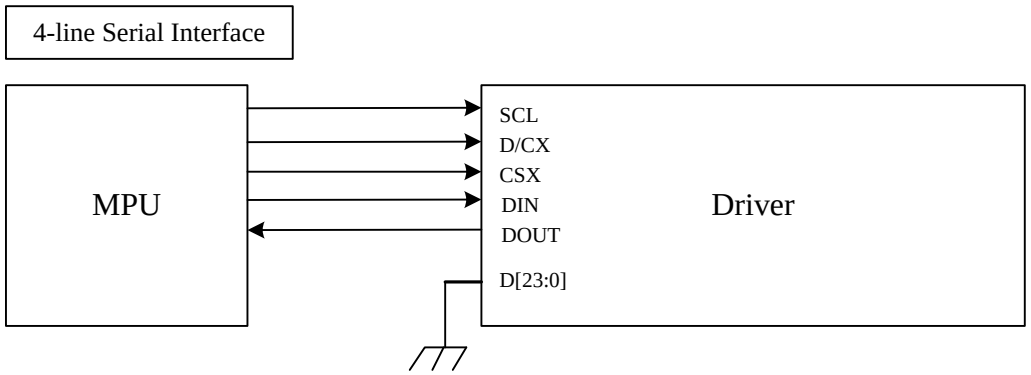
Note 1: The pixel data with 24-bit color depth information.

Note 2: The most significant bits are: Rx7, Gx7 and Bx7.

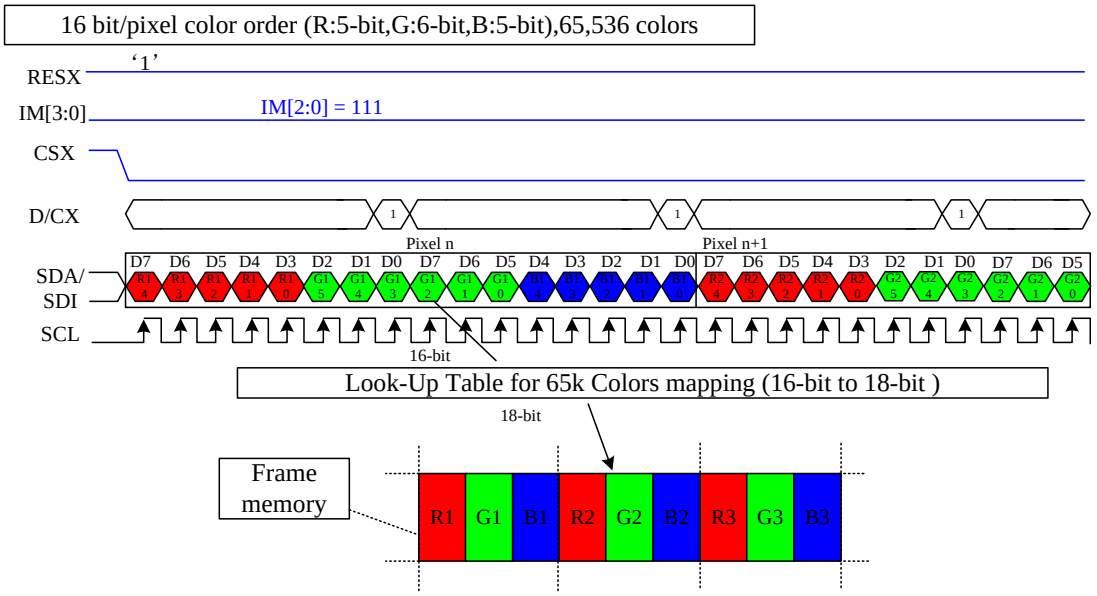
Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

4.6.2 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9403 can be selected by setting external pins IM [2:0] to “111”. The following figure is an example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.
-65k colors, RGB 5, 6, 5 -bits input.
-262k colors, RGB 6, 6, 6 -bits input.
- 16.7M-Colors, RGB 8, 8, 8 -bits input data.

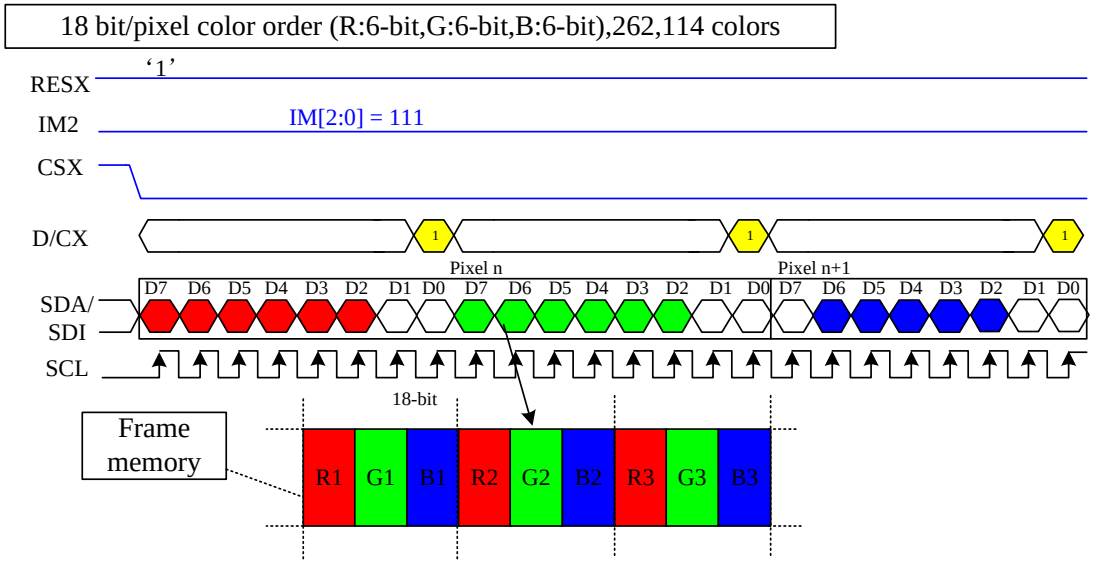


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: ‘-‘= Don’t care –Can be set “0” or “1”.

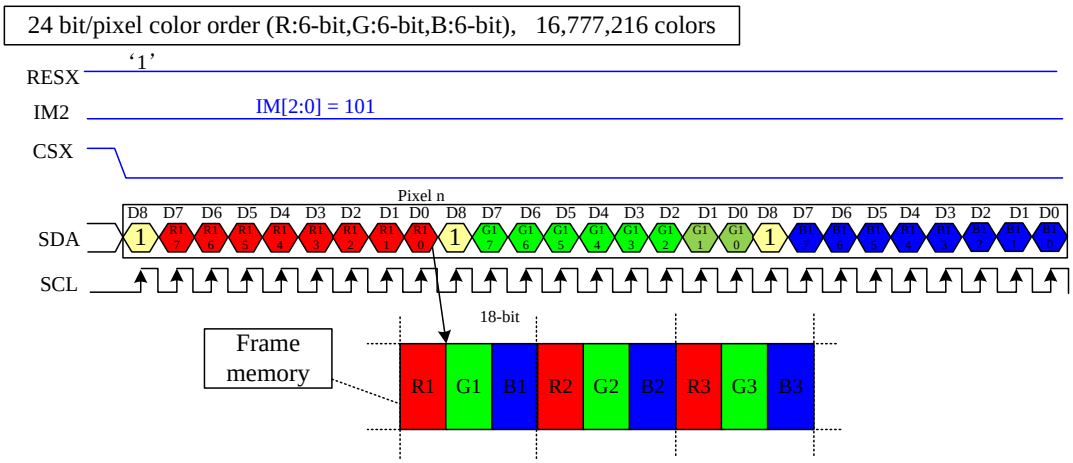


Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".



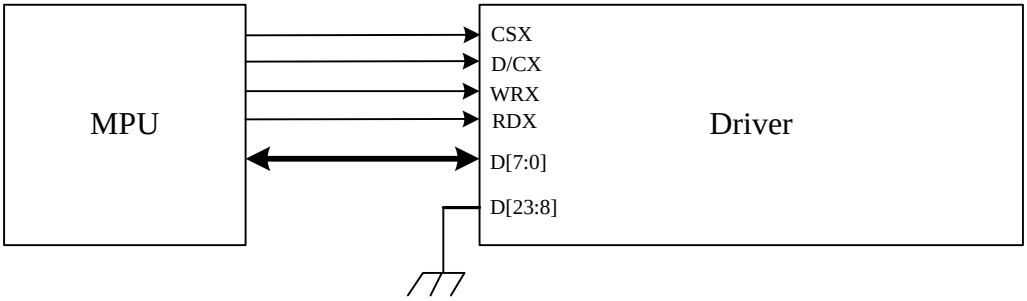
Note 1: The pixel data with 24-bit color depth information.

Note 2: The most significant bits are: Rx7, Gx7 and Bx7.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

4.6.3 8-bit Parallel MCU Interface

The 8080 system 8-bit parallel bus interface of GC9403 can be used by setting external pin as IM [2:0] to“011”.The following shown figure is the example of interface with 8080 MCU system interface.



Different display data formats are available for two color depths supported by listed below.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.
- 16.7M-Colors, RGB 8, 8, 8 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

Data: MSB = D7, LSB = D0.
Sub-pixels: MSB = bit 5, LSB = bit0 for green. MSB = bit 4, LSB = bit 0 for red and blue.

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	478	479	480
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

Data: MSB = D7, LSB = D0.
Sub-pixels: MSB = bit 5, LSB = bit 0 for red, green and blue.

16.7M color: 24-bit/pixel (RGB 8-8-8 bits input)

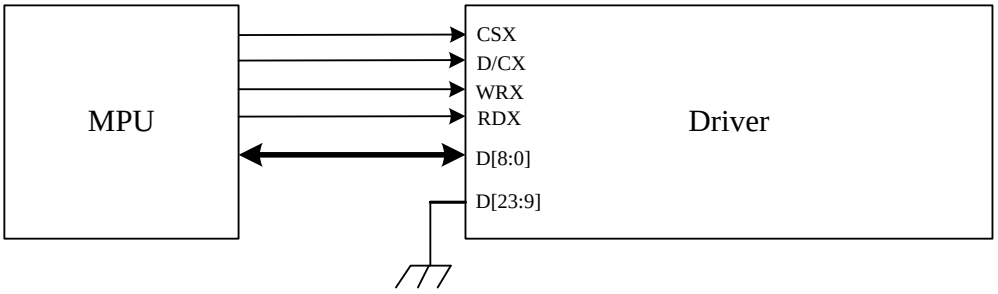
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “111”.

Count	0	1	2	3	…	478	479	480
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R7	0G7	0B7	…	239R7	239G7	239G7
D6	C6	0R6	0G6	0B6	…	239R6	239G6	239G6
D5	C5	0R5	0G5	0B5	…	239R5	239G5	239B5
D4	C4	0R4	0G4	0B4	…	239R4	239G4	239B4
D3	C3	0R3	0G3	0B3	…	239R3	239G3	239B3
D2	C2	0R2	0G2	0B2	…	239R2	239G2	239B2
D1	C1	0R1	0G1	0B1	…	239R1	239G1	239B1
D0	C0	0R0	0G0	0B0	…	239R0	239G0	239B0

Data: MSB = D7, LSB = D0.
Sub-pixels: MSB = bit 7, LSB = bit 0 for red, green and blue.

4.6.4 9-bit Parallel MCU Interface

The 8080 system 9-bit parallel bus interface of GC9403 can be selected by setting hardware pin IM [2:0] to “001”. The following shown figure is the example of interface with 8080 MCU system interface.



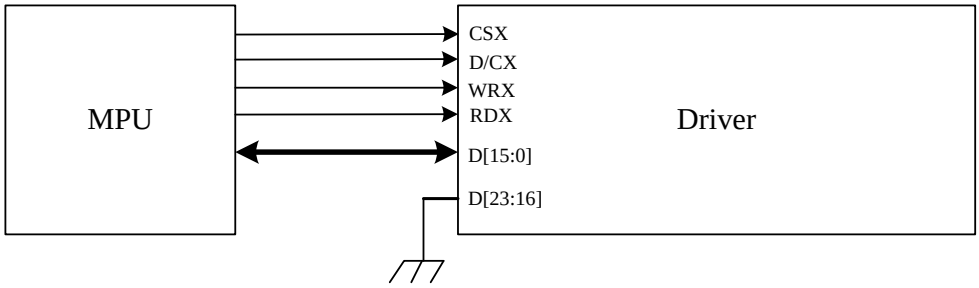
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

4.6.5 16-bit Parallel MCU Interface

The 8080 system 16-bit parallel bus interface of GC9403 can be selected by setting hardware pin IM[2:0] to "010".The following shown figure is the example of interface with 8080 MCU system interface.



Different display data format is available for two colors depth supported by listed below.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.
- 16.7M-Colors, RGB 8, 8, 8 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1							
D0	C0							

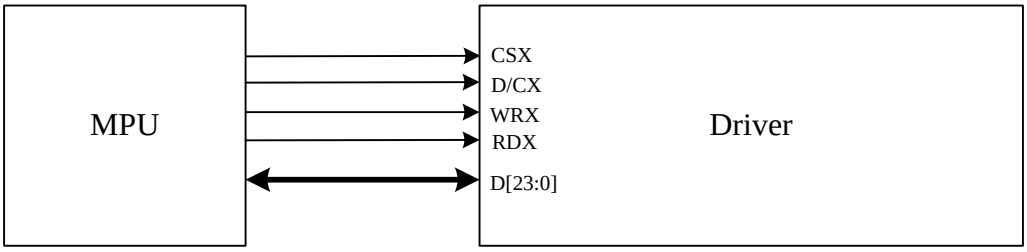
16.7M color: 24-bit/pixel (RGB 8-8-8 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “111”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R7	0B7	1G7	…	238R7	238B7	239G7
D14		0R6	0B6	1G6	…	238R6	238B6	239G6
D13		0R5	0B5	1G5	…	238R5	238B5	239G5
D12		0R4	0B4	1G4	…	238R4	238B4	239G4
D11		0R3	0B3	1G3	…	238R3	238B3	239G3
D10		0R2	0B2	1G2	…	238R2	238B2	239G2
D9		0R1	0B1	1G1	…	238R1	238B1	239G1
D8		0R0	0B0	1G0	…	238R0	238B0	239G0
D7	C7	0G7	1R7	1B7	…	238G7	239R7	239B7
D6	C6	0G6	1R6	1B6	…	238G6	239R6	239B6
D5	C5	0G5	1R5	1B5	…	238G5	239R5	239B5
D4	C4	0G4	1R4	1B4	…	238G4	239R4	239B4
D3	C3	0G3	1R3	1B3	…	238G3	239R3	239B3
D2	C2	0G2	1R2	1B2	…	238G2	239R2	239B2
D1	C1	0G1	1R1	1B1	…	238G1	239R1	239B1
D0	C0	0G0	1R0	1B0	…	238G0	239R0	239B0

4.6.6 24-bit Parallel MCU Interface

The 8080 system 18-bit parallel bus interface of GC9403 can be selected by setting hardware pin IM [2:0] to “000”.The following shown figure is the example of interface with 8080 MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.
- 16.7M-Colors, RGB 8, 8, 8 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D23								
D22								
D21								
D20								
D19								
D18								
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D23								
D22								
D21								
D20								
D19								
D18								
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

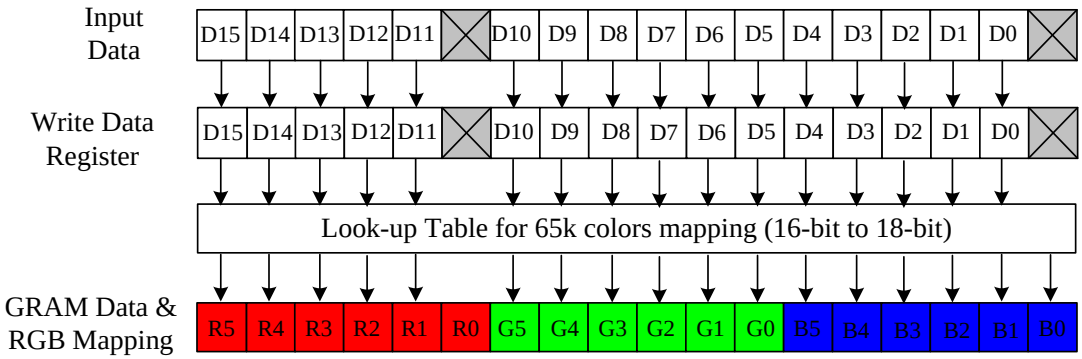
16M color: 24-bit/pixel (RGB 8-8-8 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “111”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D23		0G7	1G7	2G7	…	237G7	238G7	239G7
D22		0G6	1G6	2G6	…	237G6	238G6	239G6
D21		0R5	1R5	2R5	…	237R5	238R5	239R5
D20		0R4	1R4	2R4	…	237R4	238R4	239R4
D19		0R3	1R3	2R3	…	237R3	238R3	239R3
D18		0R2	1R2	2R2	…	237R2	238R2	239R2
D17		0R1	1R1	2R1	…	237R1	238R1	239R1
D16		0R0	1R0	2R0	…	237R0	238R0	239R0
D15		0G7	1G7	2G7	…	237G7	238G7	239G7
D14		0G6	1G6	2G6	…	237G6	238G6	239G6
D13		0G5	1G5	2G5	…	237G5	238G5	239G5
D12		0G4	1G4	2G4	…	237G4	238G4	239G4
D11		0G3	1G3	2G3	…	237G3	238G3	239G3
D10		0G2	1G2	2G2	…	237G2	238G2	239G2
D9		0G1	1G1	2G1	…	237G1	238G1	239G1
D8		0G0	1G0	2G0	…	237G0	238G0	239G0
D7	C7	0B7	1B7	2B7	…	237B7	238B7	239B7
D6	C6	0B6	1B6	2B6	…	237B6	238B6	239B6
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

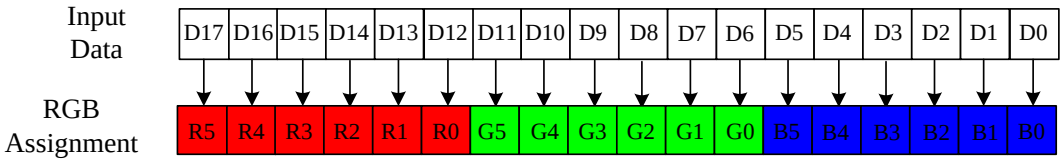
4.6.7 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. Display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM in synchronization with display operation via 16-bit RGB data bus (D [15:0]) according to the data enable signal (DE). Both D17 and D16 pins should be left open to ensure normal operation. Registers can be set by the SPI system interface.



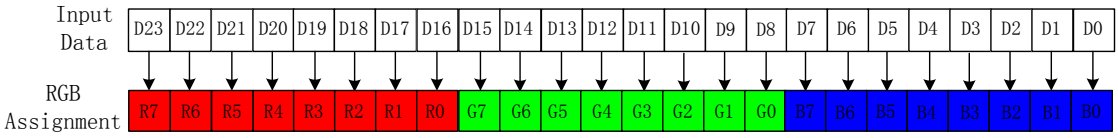
4.6.8 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”.Display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM in synchronization with display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE). Registers can be set by the SPI system interface.



4.6.9 24-bit Parallel RGB Interface

The 24-bit RGB interface is selected by setting the DPI [2:0] bits to “111”.Display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. Display data is transferred to the internal GRAM in synchronization with display operation via 18-bit RGB data bus (D [23:0]) according to the data enable signal (DE). Registers can be set by the SPI system interface.



5 Function Description

5.1 Display data GRAM mapping

The display data RAM stores display dots and consists of 2,764,800 bits (320x18x480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

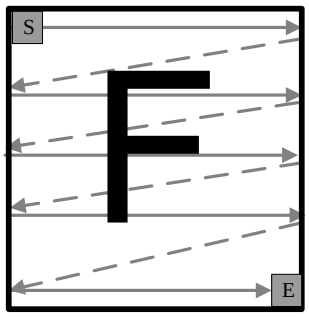
GRAM address for display panel position as shown in the following table

(00,00)h	(00,01)h	…… …	(00,ED)h	(00,13E)h	(00,13F)h
(01,00)h	(01,01)h	…… …	(01,ED)h	(01,13E)h	(01,13F)h
(02,00)h	(02,01)h	…… …	(02,ED)h	(02,13E)h	(02,13F)h
(03,00)h	(03,01)h	…… …	(03,ED)h	(03,13E)h	(03,13F)h
…… …	…… …	…… …	…… …	…… …	…… …
(1DD,00)h	(1DD,01)h	…… …	(1DD,ED)h	(1DD,13E)h	(1DD,13F)h
(1DE,00)h	(1DE,01)h	…… …	(1DE,ED)h	(1DE,13E)h	(1DE,13F)h
(1DF,00)h	(1DF,01)h	…… …	(1DF,ED)h	(1DF,13E)h	(1DF,13F)h

5.2 Address Counter (AC) of GRAM

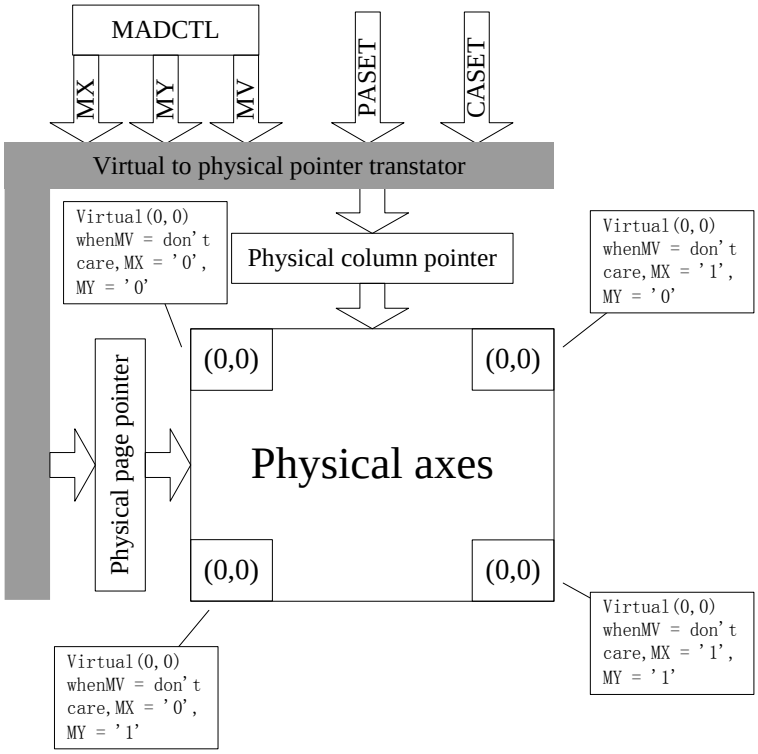
The GC9403 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.
To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

Image data sending order from host and data stream update as shown in the following figure



The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

Image data writing control:

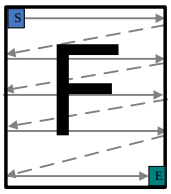
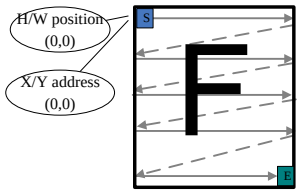
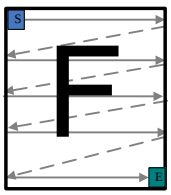
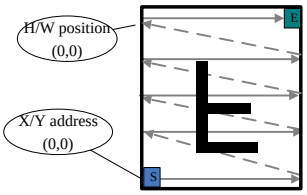
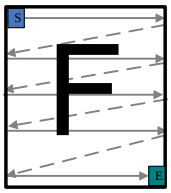
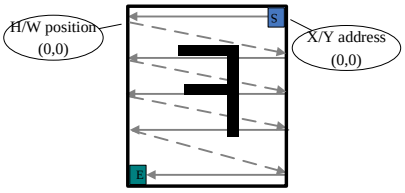
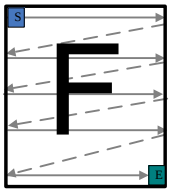
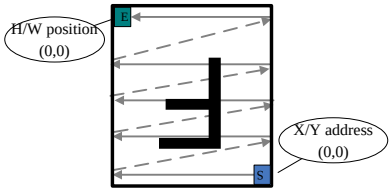
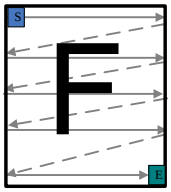
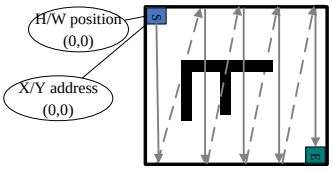
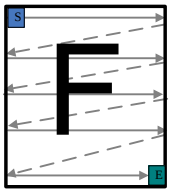
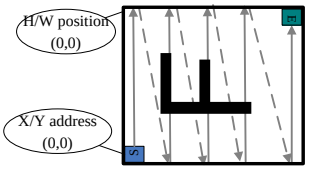
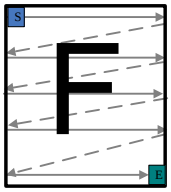
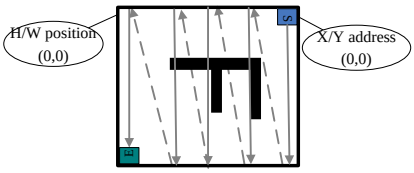
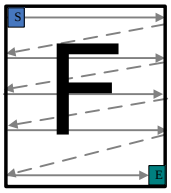
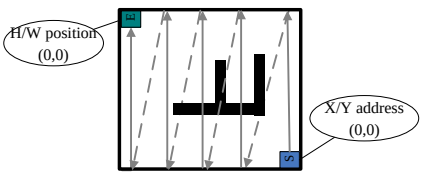


CASET and PASET control for physical column/page pointers:

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319 - Physical Page Pointer)
0	1	0	Direct to (239 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239 - Physical Column Pointer)	Direct to (319 - Physical Page Pointer)
0	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
0	0	1	Direct to (319 - Physical Page Pointer)	Direct to Physical Column Pointer
0	1	0	Direct to Physical Page Pointer	Direct to (239 - Physical Column Pointer)
0	1	1	Direct to (319 - Physical Page Pointer)	Direct to (239 - Physical Column Pointer)

condition	**Column Counter**	**Page Counter**
When RAMWR/RAMRD command is accepted	Return to “Start Column”	Return to “Start Page”
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than “End column.”	Return to “Start Column”	Increment by 1
The Page counter value is larger than “End page”.	Return to “Start column”	Return to “Start Page”

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Display data direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
normal	0	0	0		
Y-invert	0	0	1		
X-ivert	0	1	0		
Y-invert X-invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-invert	1	0	1		
X-Y exchange X-invert	1	1	0		
X-Y exchange Y-invert X-invert	1	1	1		

5.3 GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS**, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

BGR="0"														
Source	**SS="0"**	S1	S2	S3	S4	S5	S6	------	S955	S956	S957	S958	S959	S960
Output	**SS="1"**	S958	S959	S960	S955	S956	S957	------	S4	S5	S6	S1	S2	S3
GRAM X address		"00"h			"01"h			------	"13E"h			"13F"h		
RGB data		R	G	B	R	G	B	------	R	G	B	R	G	B
Pixel		Pixel1			Pixel2			------	Pixel239			Pixel240		
BGR="1"														
Source	**SS="0"**	S3	S2	S1	S6	S5	S4	------	S957	S956	S955	S960	S959	S958
Output	**SS="1"**	S960	S959	S958	S957	S956	S955	------	S6	S5	S4	S3	S2	S1
GRAM X address		"00"h			"01"h			------	"13E"h			"13F"h		
RGB data		R	G	B	R	G	B	------	R	G	B	R	G	B
Pixel		Pixel1			Pixel2			------	Pixel239			Pixel240		

GRAM address and display panel position (GS_Panel =’0’):

S/G	S1	S2	S3	S4	S5	S6	S7	S8	S9	----	S952	S953	S954	S955	S956	S957	S958	S959	S960
G1	0000h			0001h			0002h			----	00EDh			0013Eh			0013Fh		
G2	0100h			0101h			0102h			----	01EDh			0113Eh			0113Fh		
G3	0200h			0201h			0202h			----	02EDh			0213Eh			0213Fh		
G4	0300h			0301h			0302h			----	03EDh			0313Eh			0313Fh		
G5	0400h			0401h			0402h			----	04EDh			0413Eh			0413Fh		
G6	0500h			0501h			0502h			----	05EDh			0513Eh			0513Fh		
⋮	⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G475	13A00h			13A01h			13A02h			----	13AEDh			13A13Eh			13A13Fh		

G476	13B00h	13B01h	13B02h	----	13BEDh	13B13Eh	13B13Fh
G477	13C00h	13C01h	13C02h	----	13CEDh	13C13Eh	13C13Fh
G478	1DD00h	1DD01h	1DD02h	----	1DDEDh	1DD13Eh	1DD13Fh
G479	1DE00h	1DE01h	1DE02h	----	1DEEDh	1DE13Eh	1DE13Fh
G480	1DF00h	1DF01h	1DF02h	----	1DFEDh	1DF13Eh	1DF13Fh

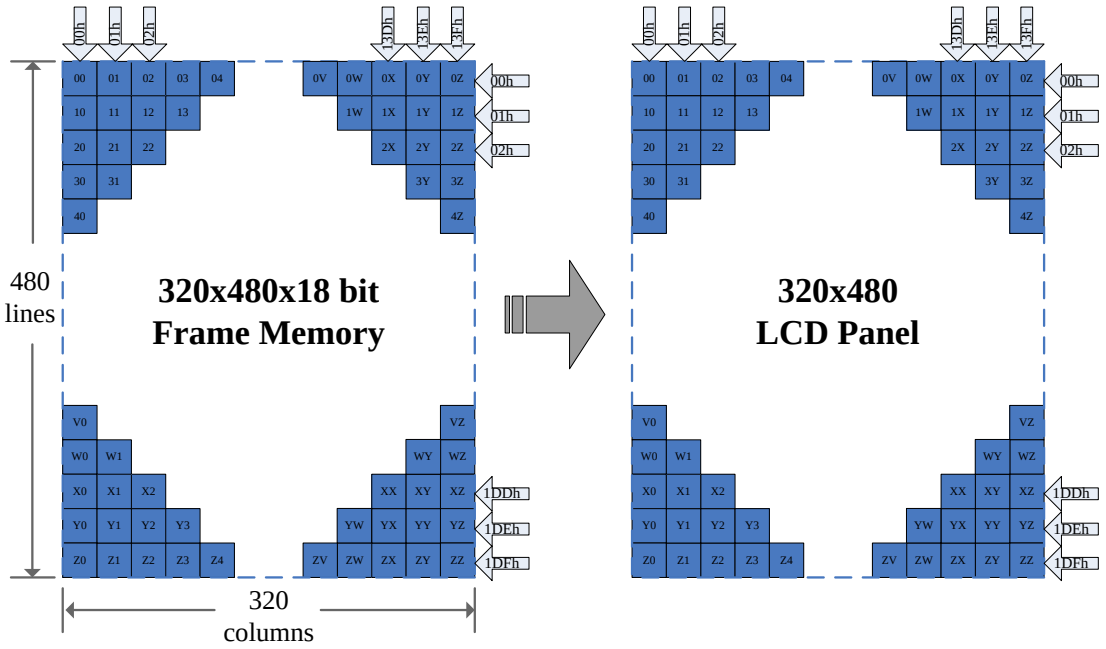
GRAM address and display panel position (GS_Panel =’1’):

S/G	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**	**----**	**S952**	**S953**	**S954**	**S955**	**S956**	**S957**	**S958**	**S959**	**S960**
G480	0000h			0001h			0002h			----	00EDh			0013Eh			0013Fh		
G479	0100h			0101h			0102h			----	01EDh			0113Eh			0113Fh		
G478	0200h			0201h			0202h			----	02EDh			0213Eh			0213Fh		
G477	0300h			0301h			0302h			----	03EDh			0313Eh			0313Fh		
G476	0400h			0401h			0402h			----	04EDh			0413Eh			0413Fh		
G475	0500h			0501h			0502h			----	05EDh			0513Eh			0513Fh		
⋮	⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G6	13A00h			13A01h			13A02h			----	13AEDh			13A13Eh			13A13Fh		
G5	13B00h			13B01h			13B02h			----	13BEDh			13B13Eh			13B13Fh		
G4	13C00h			13C01h			13C02h			----	13CEDh			13C13Eh			13C13Fh		
G3	1DD00h			1DD01h			1DD02h			----	1DDEDh			1DD13Eh			1DD13Fh		
G2	1DE00h			1DE01h			1DE02h			----	1DEEDh			1DE13Eh			1DE13Fh		
G1	1DF00h			1DF01h			1DF02h			----	1DFEDh			1DF13Eh			1DF13Fh		

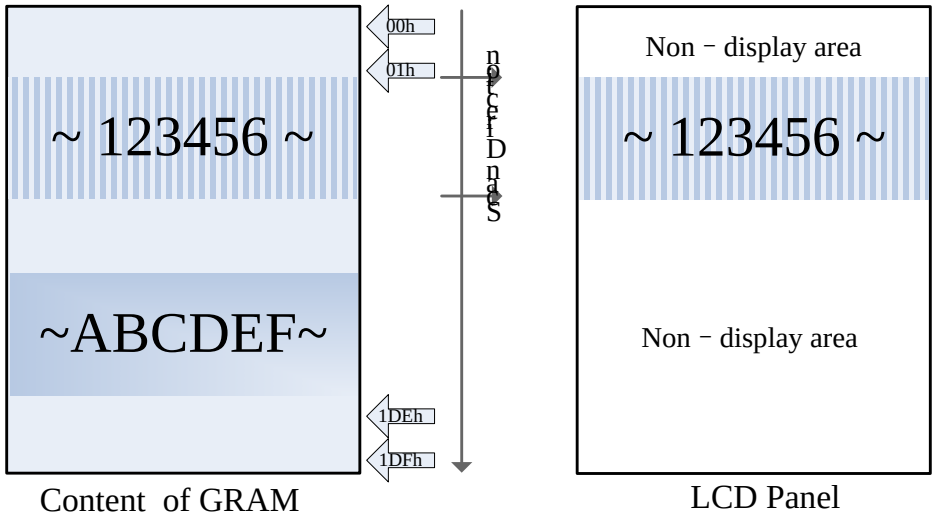
GC9403 supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

5.3.1 Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 0013Fh and page pointer is 0000h to 01DFh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)



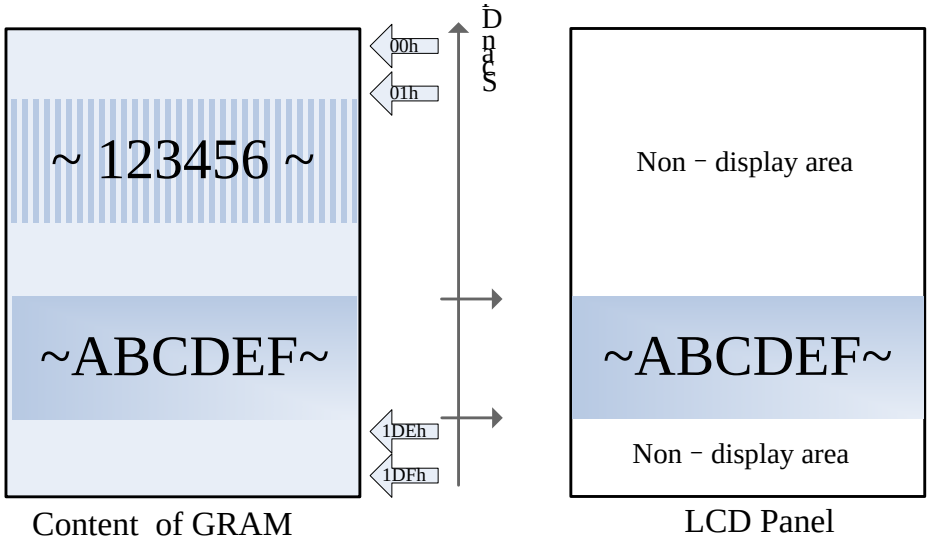
Example1:
(1) partial mode on (setting 12h)
(2) SR [15:0] =50DEC, ER [15:0] =150DEC, MADCTL's B4(ML)='0' (GS='0').



Example2:

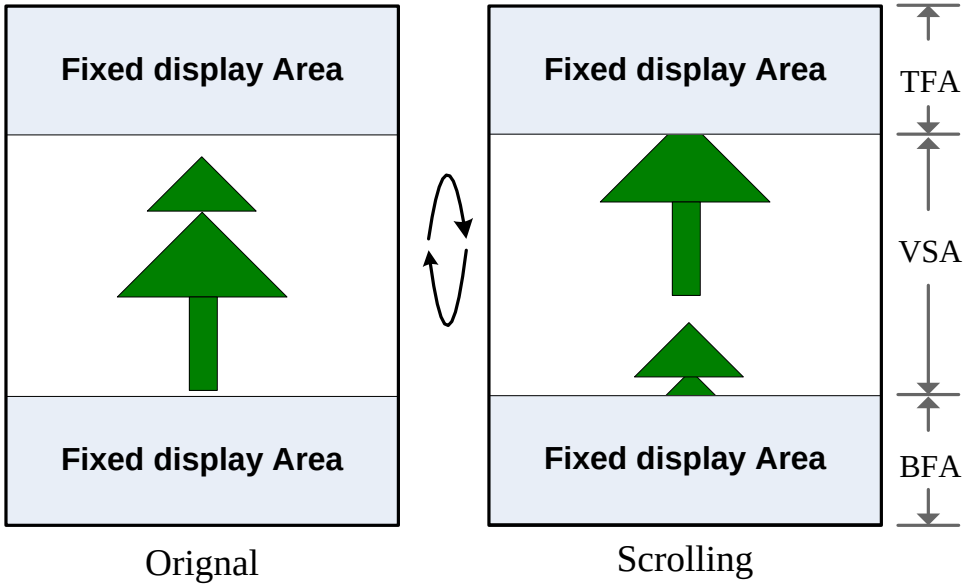
(1) partial mode on (setting 12h)

(2) SR [15:0] =50DEC, ER [15:0] =150DEC, MADCTL's B4(ML)='1' (GS='0').



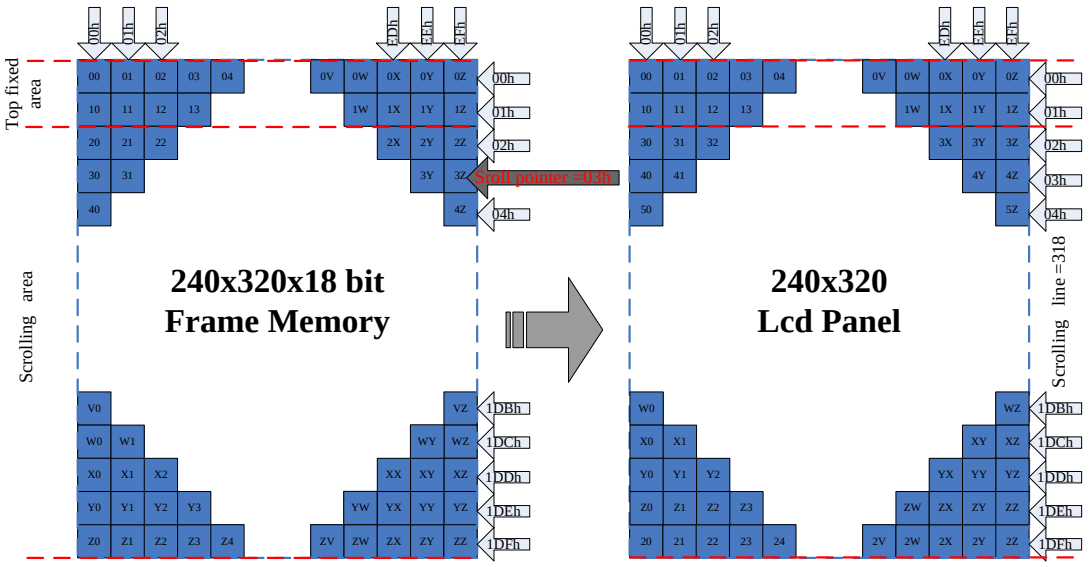
5.3.2 Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).

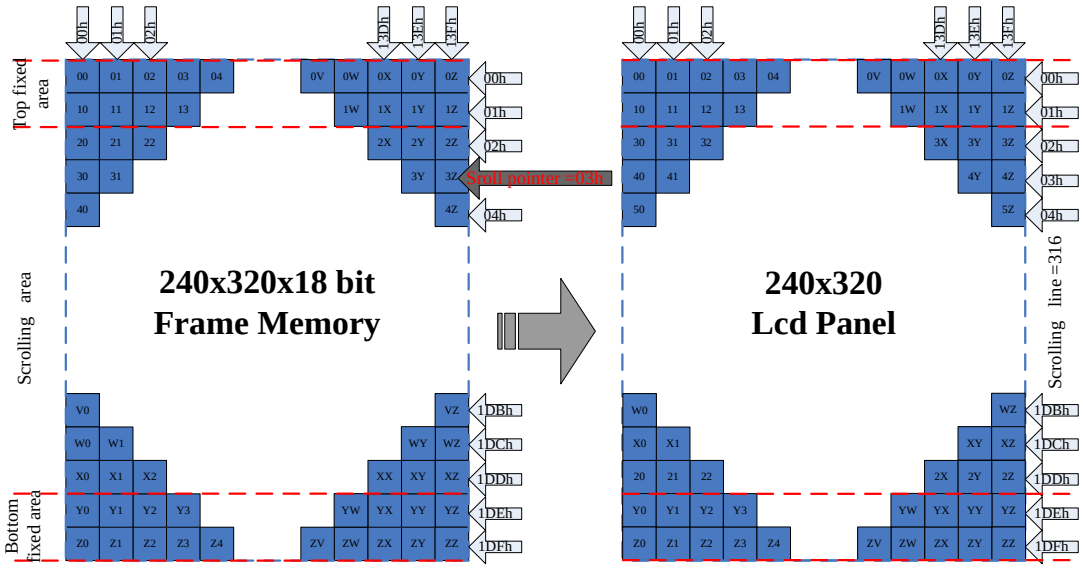


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =480. In this case, scrolling is applied as shown below.

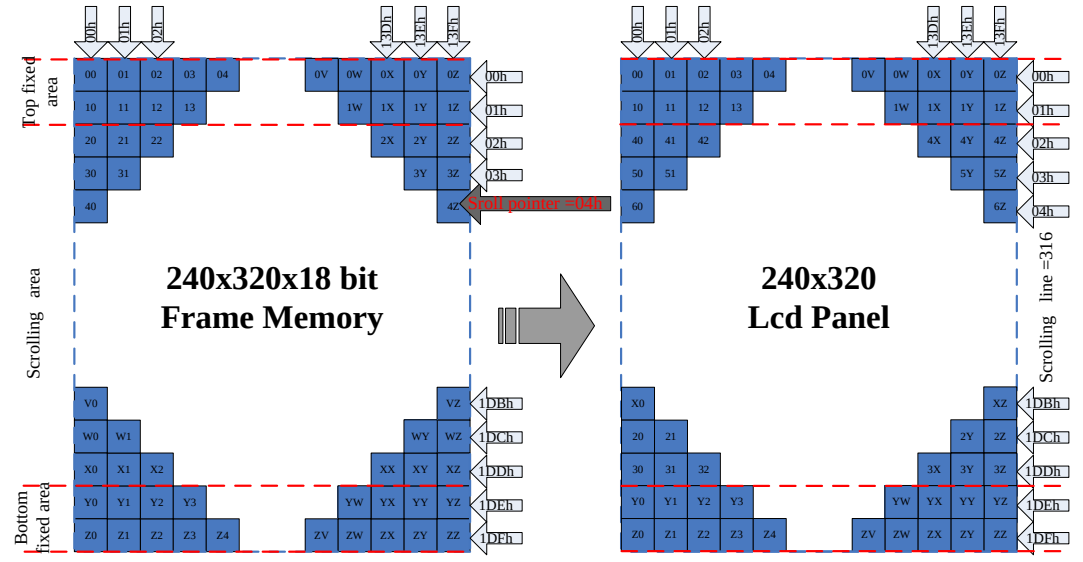
Example 1 .TFA=’2d’, VSA=’478d’, BFA=’0d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 1:



Example 2 .TFA=’2d’, VSA=’476d’, BFA=’2d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 2:



Example 3 .TFA=’2d’, VSA=’476d’, BFA=’2d’, VSP=’4d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 3:



Vertical scroll example

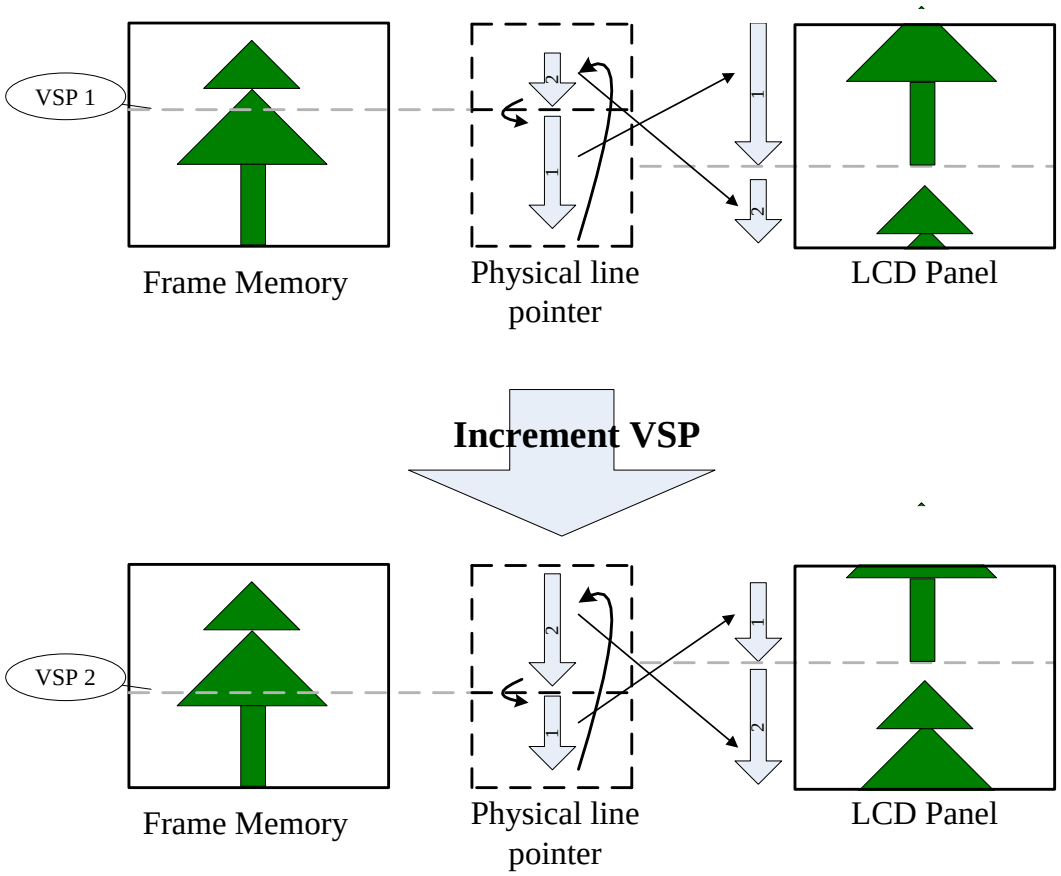
There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits and **VSP** bits

Case 1: TFA + VSA + BFA ≠ ‘480d’

N/A. Do not set TFA + VSA + BFA ≠ ‘480d’. In that case, unexpected picture will be shown.

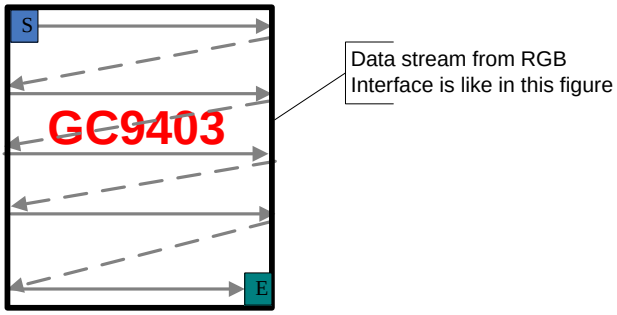
Case 2: TFA + VSA + BFA = ‘480d’ (Scrolling)

Example (1) When TFA=’0d’, VSA=’480d’, BFA=’0d’ and VSP1=’40d’ & VSP2=’140d’ (SS =’0’,GS=’0’)

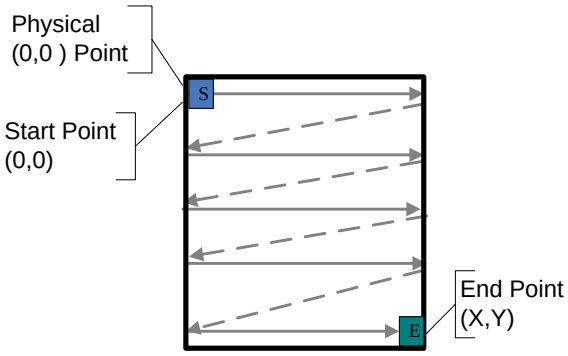


5.3.3 Updating order on display active area in RGB interface mode

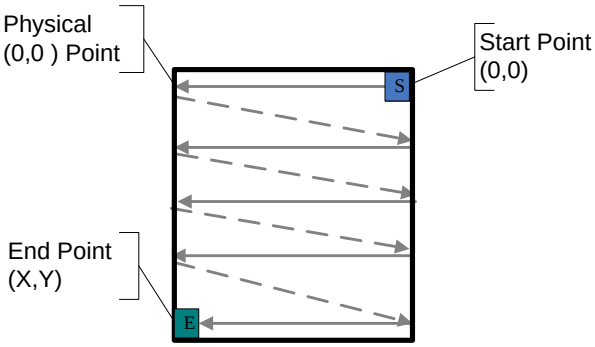
There is defined different kind of updating orders for display in RGB interface mode. These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.



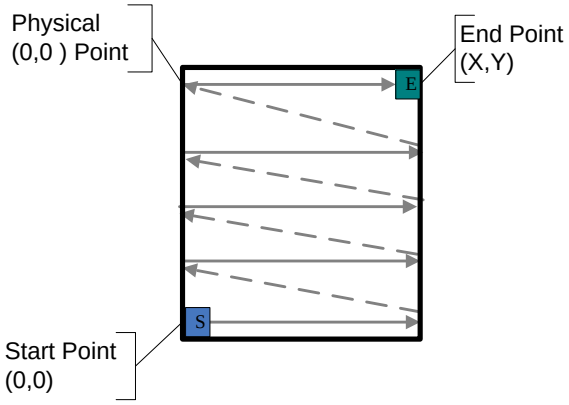
Updating order when MY = '0' and MX = '0'



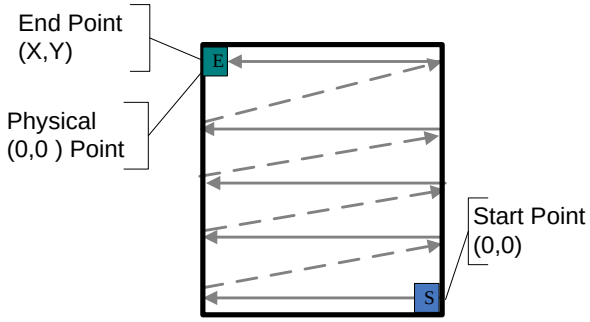
Updating order when MY = '0' and MX = '1'



Updating order when MY = '1' and MX = '0'



Updating order when MY = '1' and MX = '1'



Rules for updating order on display active area in RGB interface display mode:

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 "Start Column"	Return to "Start Page"

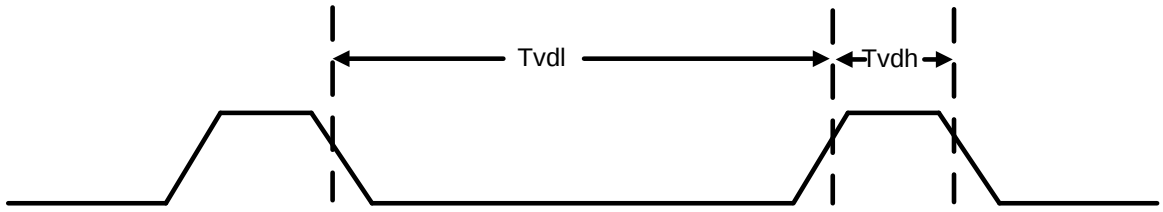
Note: Pixel order is RGB on the display.

5.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.4.1 Tearing effect line modes

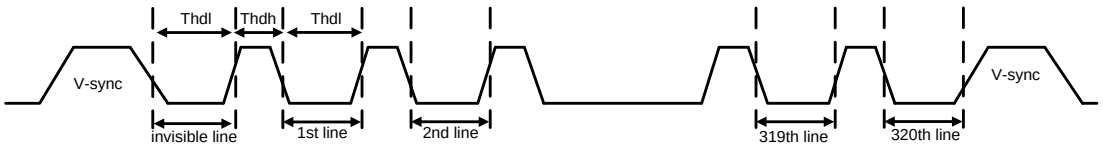
Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:



t_{Vdh}= The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.

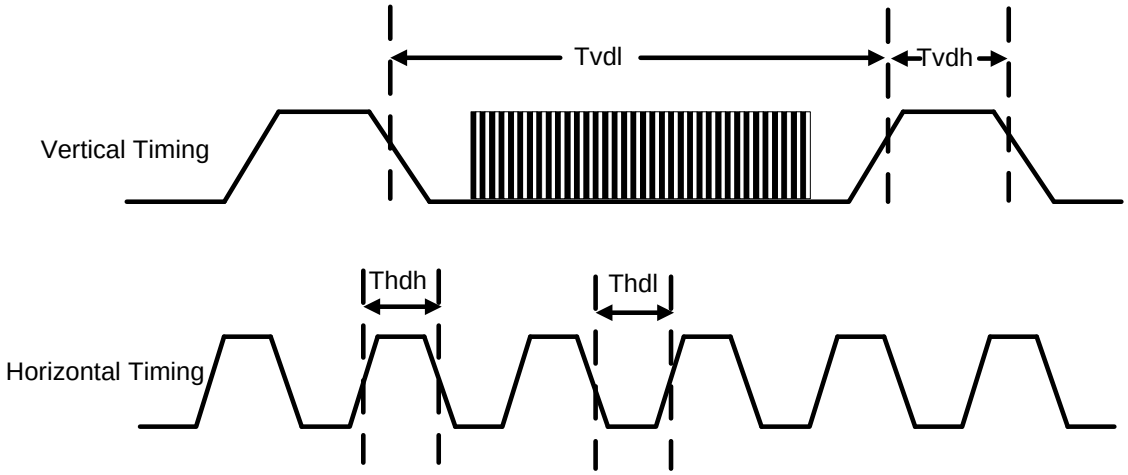


t_{hdh}= The LCD display is not updated from the Frame Memory

t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2 Tearing effect line timing

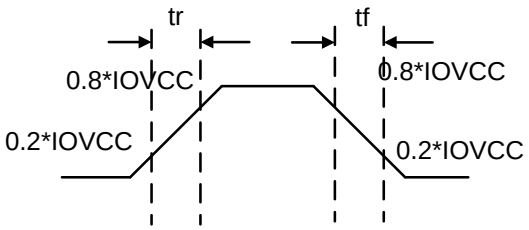
The Tearing Effect signal is described below.



Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) **,**The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5 Source driver

The GC9403 contains a 960 channels of source driver (S1~S960) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 960 channels and generates corresponding gray scale voltage output, which can realize a16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6 Gate driver

The GC9403 contains a 480 gate channels of gate driver (G1~G480) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7 Power Level Definition

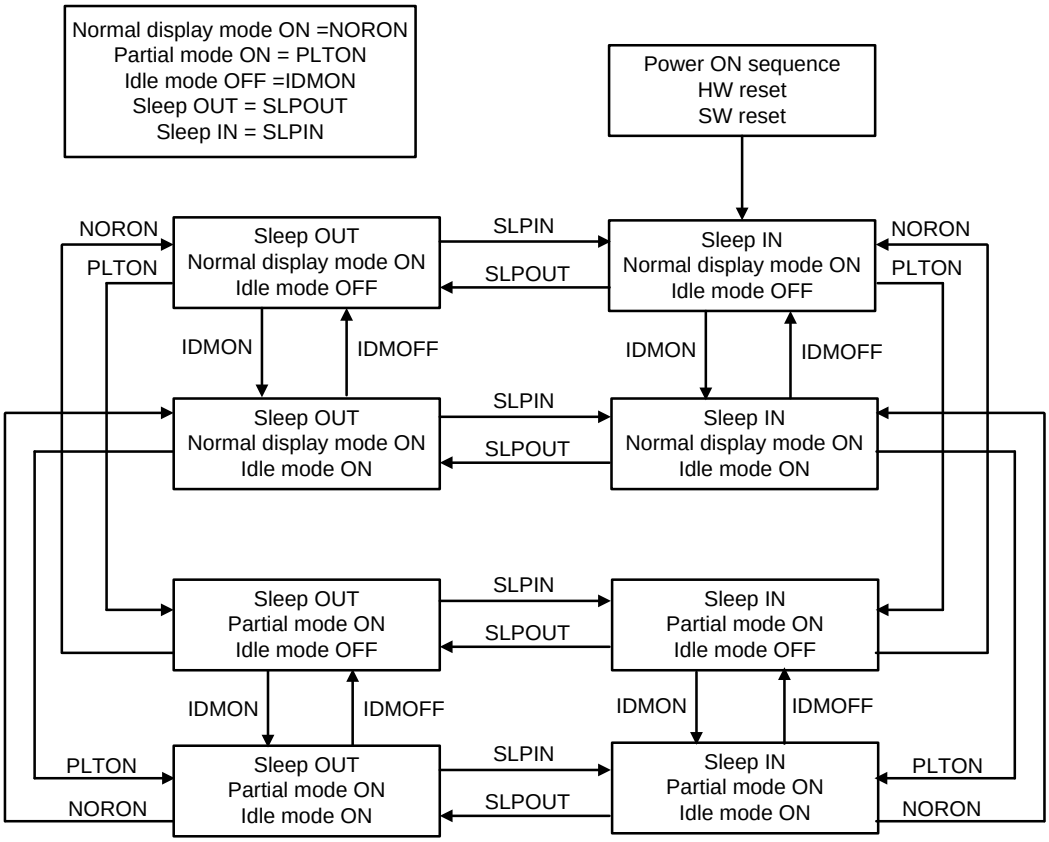
5.7.1 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 16.7M colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 16.7M colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.7.2 Power Flow Chart

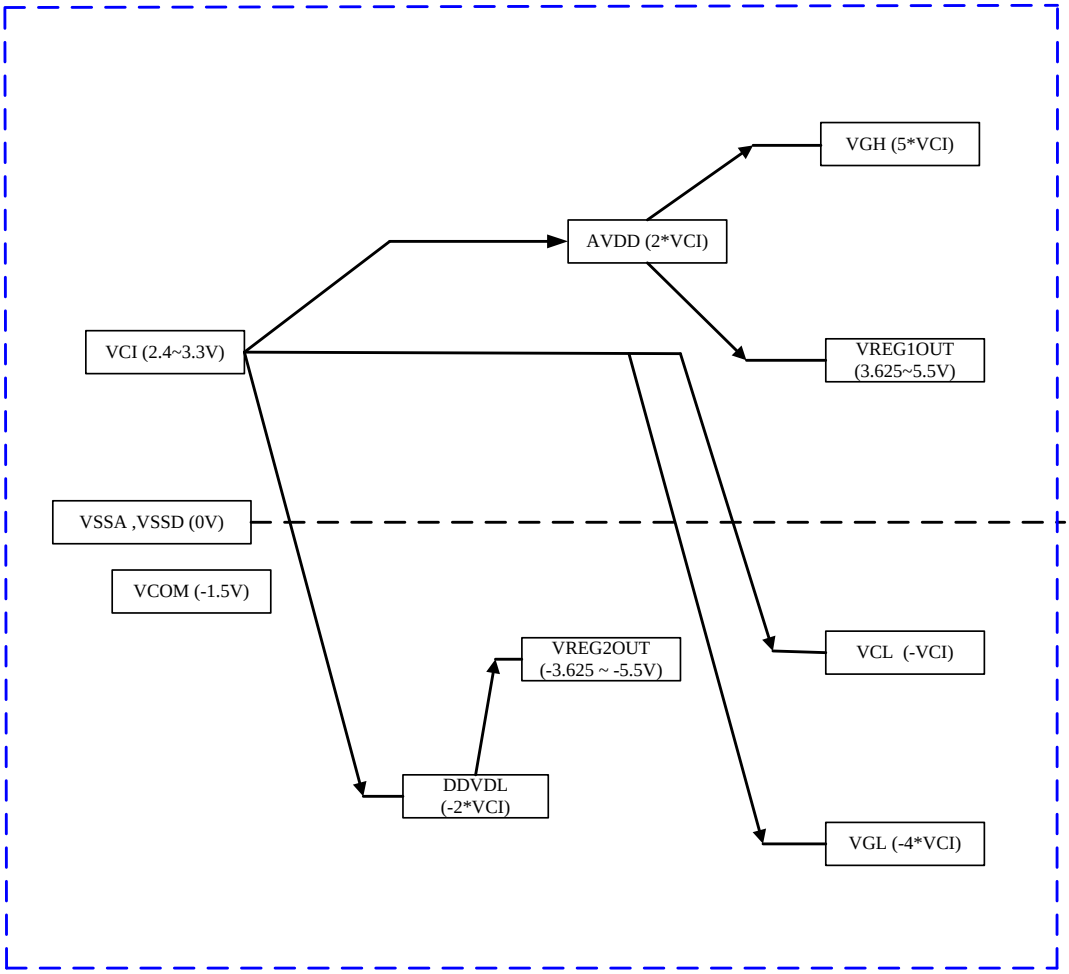


Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.7.3 LCD power generation scheme

The boost voltage generated is shown as below.



LCD power generation scheme

5.8 Input/output pin state

5.8.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB7 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
DOUT	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
CABC_PWM	Low	Low

Characteristics of output pins

5.8.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[23:0]	Input invalid	Input valid	Input valid	Input invalid
IM[2:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6 Command

6.1 Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 1	0	1	↑	XX	0	0	0	0	0	1	0	0	00h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1_1[7:0]								00
	1	↑	1	XX	ID1_2[7:0]								94
	1	↑	1	XX	ID1_3[7:0]								03
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2_1[7:0]								00
	1	↑	1	XX	ID2_2[7:0]								94
	1	↑	1	XX	ID2_3[7:0]								03
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:24]								00
	1	↑	1	XX	D[23:16]								61
	1	↑	1	XX	D[15: 8]								00
	1	↑	1	XX	D[7: 0]								00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7: 0]								08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7: 0]								00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	DPI [2:0]			0	DBI [2:0]			66
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:0]								00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX

	1	↑	1	XX	D[7:0]								00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:6]		0	0	0	0	0	0	F0
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								01
	1	1	↑	XX	EC[7:0]								3F
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00
	1	1	↑	XX	SP[7:0]								00
	1	1	↑	XX	EP[15:8]								01
	1	1	↑	XX	EP[7:0]								DF
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								01
	1	1	↑	XX	ER[7:0]								DF
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	XX								XX
	1	1	↑	XX	XX								XX
	1	1	↑	XX	BFA[15:8]								00

	1	1	↑	XX	BFA[7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
Write CABC value	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	↑	1	XX	0	0	0	0	0	0	C[1:0]		00
Read CABC value	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	0	C[1:0]		00
Write CABC value	0	1	↑	XX	0	1	0	1	0	1	1	1	5Eh
	1	↑	1	XX	CMB[7:0]								00
Read CABC value	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CMB[7:0]								00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX

	1	↑	1	XX	ID2[7:0]								94
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID3 [7:0]								03

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	00
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	0	0	0	0	0	DINV[2:0]			00
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	VFP[7:0]								02
	1	1	↑	XX	VBP[7:0]								02
	1	1	↑	XX	0	0	0	0					00
	1	1	↑	XX	HBP[7:0]								04
Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	0	RCM	RM	DM	0	0	PTS	0	00
	1	1	↑	XX	0	GS	SS	SM	0	0	0	0	00
	1	1	↑	XX	0	0	NL[5:0]						3B
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	EPF[1:0]		0	0	0	GON	DTE	0	06
CABC Control 2	0	1	↑	XX	1	1	0	0	1	0	0	0	C8h
	1	1	↑	XX	0	0	0	0	0	0	0	pwmpol	00
CABC Control 9	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh
	1	1	↑	XX	PWM_DIV[7:0]								18

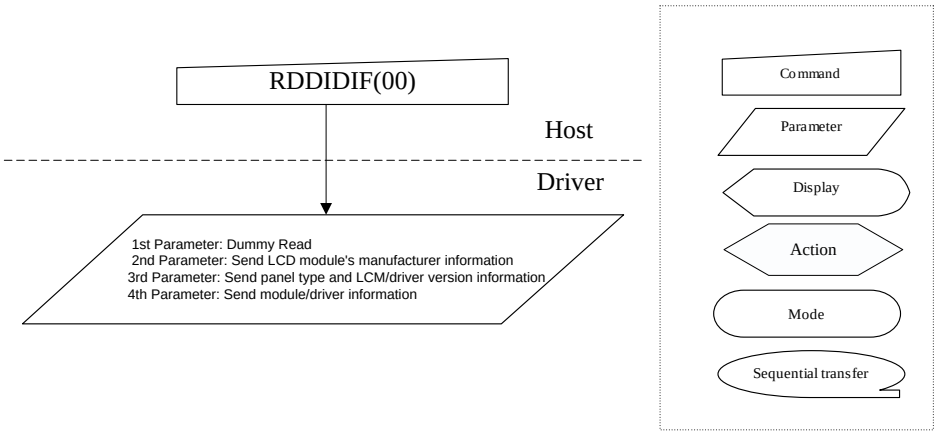
Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Frame Rate and Display Inversion	0	1	↑	XX	1	0	1	0	0	0	1	1	A3h
	1	1	↑	XX					RTN1[3:0]				02
	1	1	↑	XX		RTN2[6:0]							17
Power control 1	0	1	↑	XX	1	0	1	0	0	1	0	0	A4h
	1	1	↑	XX				VRH1[4:0]					1d
Power control 2	0	1	↑	XX	1	0	1	0	0	1	0	0	A5h
	1	1	↑	XX				VRH2[4:0]					1f
VCOM control	0	1	↑	XX	1	1	1	1	1	1	0	1	E5h
	0	1	↑	XX	VCM[7:0]								20
Power control 2	0	1	↑	XX	1	1	1	0	1	1	0	1	EDh
	0	1	↑	XX		dc1[2:0]				dc0[2:0]			55
	0	1	↑	XX		dc3[2:0]				dc2[2:0]			55
SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX					VP0[3:0]				0F
	1	1	↑	XX			VP1[5:0]						3F
	1	1	↑	XX			VP2[5:0]						3F
	1	1	↑	XX					VP4[3:0]				0F
	1	1	↑	XX				VP6[4:0]					1A
	1	1	↑	XX					VP13[3:0]				0F
	1	1	↑	XX		VP20[6:0]							5A
	1	1	↑	XX	VP30[3:0]				VP27[3:0]				64
	1	1	↑	XX		VP43[6:0]							30
	1	1	↑	XX					VP50[3:0]				0A
	1	1	↑	XX				VP57[4:0]					15
	1	1	↑	XX					VP59[3:0]				05
	1	1	↑	XX			VP61[5:0]						19
	1	1	↑	XX			VP62[5:0]						19
	1	1	↑	XX					VP63[3:0]				02
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX					VN0[3:0]				0F
	1	1	↑	XX			VN1[5:0]						3F
	1	1	↑	XX			VN2[5:0]						2F
	1	1	↑	XX					VN4[3:0]				0F

	1	1	↑	XX				VN6[4:0]		15
	1	1	↑	XX					VN13[3:0]	0B
	1	1	↑	XX		VN20[6:0]				3A
	1	1	↑	XX	VN30[3:0]				VN27[3:0]	87
	1	1	↑	XX		VN43[6:0]				2F
	1	1	↑	XX					VN50[3:0]	0A
	1	1	↑	XX				VN57[4:0]		15
	1	1	↑	XX					VN59[3:0]	0F
	1	1	↑	XX			VN61[5:0]			1E
	1	1	↑	XX			VN62[5:0]			18
	1	1	↑	XX					VN63[3:0]	02

6.2 Description of Level 1 Command

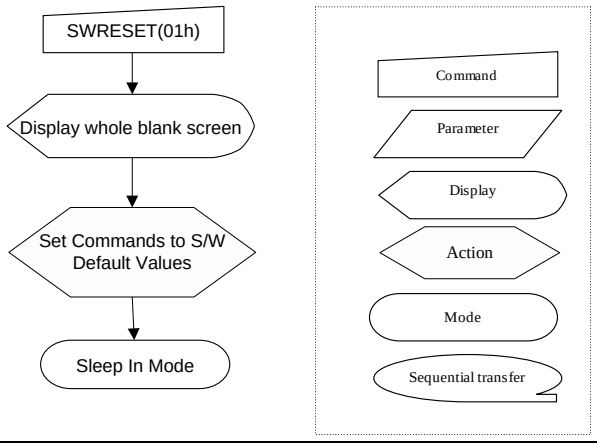
6.2.1 Read display identification information 1 (00h)

<table>
<tr><td>00h</td><td colspan="13">Read display identification information 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1_1[7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1_2[7:0]</td><td>94</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1_3[7:0]</td><td>03</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID1_1 [7:0]): LCD module’s manufacturer ID.
The 3rd parameter (ID1_2 [7:0]): LCD module/driver version ID.
The 4th parameter (ID1_3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h009403h</td></tr><tr><td>SW Reset</td><td>24’h009403h</td></tr><tr><td>HW Reset</td><td>24’h009403h</td></tr></table></td></tr>
</table>

Flow Chart	

RDDIDIF(00)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.2 Software Reset (01h)

<table>
<tr><td>01h</td><td colspan="13">Software Reset</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are unaffected by this command</td></tr>
<tr><td>Restriction</td><td colspan="13">It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.3 Read display identification information 2 (04h)

04h	Read display identification information 2												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID2_1[7:0]								00
3rd Parameter	1	↑	1	XX	ID2_1[7:0]								94
4th Parameter	1	↑	1	XX	ID2_1[7:0]								03
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID2_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID. The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.												
Restriction													

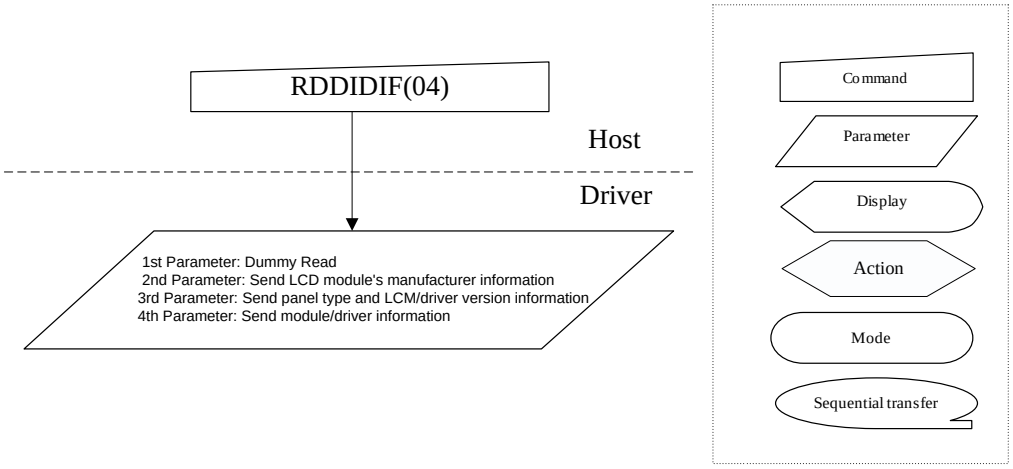
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009403h
SW Reset	24'h009403h
HW Reset	24'h009403h

Flow Chart



6.2.4 Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D[31:25]							0	00
3rd Parameter	1	↑	1	XX	0	D[22:20]			D[19:16]				61
4th Parameter	1	↑	1	XX	D15	0	D13	0	0	D[10:8]			00
5th Parameter	1	↑	1	XX	D[7:5]			0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

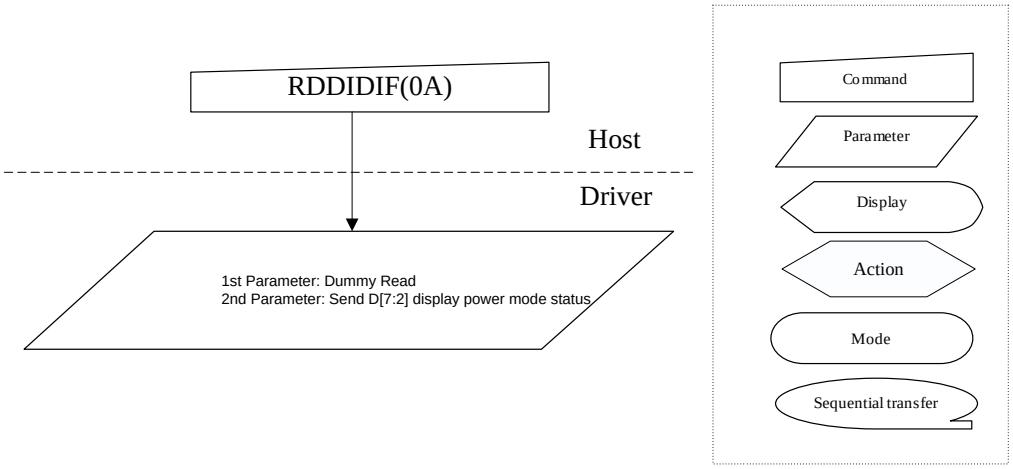
Bit	Description	Value	Status
D31	Booster voltage status	O	Booster OFF
		1	Booster ON
D30	Row address order	O	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	O	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	O	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	O	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
D26	RGB/BGR order	O	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	O	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	O	-
D23	Not used	O	-
D22	Interface color pixel format definition	101	16-bit/pixel
D21		110	18-bit/pixel
D20		111	24-bit/pixel
D19	Idle mode ON/OFF		Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	O	Partial Mode OFF
		1	Partial Mode ON

		D17	Sleep IN/OUT	O	Sleep IN Mode	
				1	Sleep OUT Mode	
		D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.	
				1	Display Normal Mode ON.	
		D15	Vertical scrolling status	O	Vertical Scroll OFF	
				1	Vertical Scroll ON	
		D14	Not used	O	-	
		D13	Inversion status	O	Inversion is OFF	
				1	Inversion is ON	
		D12	Not used	O	-	
		D11	Not used	O	-	
		D10	Display ON/OFF	O	Display is OFF	
				1	Display is ON	
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF	
				1	Tearing Effect ON	
		D[8:6]	Gamma curve selection	000	GC0	
				001	GC1	
				010	GC2	
				011	GC3	
				other	Not defined	
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only	
				1	Mode 2, both H-Blanking and V-Blanking	
		D4	Not used	O	-	
		D3	Not used	O	-	
		D2	Not used	O	-	
		D1	Not used	O	-	
		D0	Not used	O	-	
Restriction						
Register Availability						

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.5 Read Display Power Mode (0Ah)

<table>
<tr><td>0Ah</td><td colspan="13">Read Display Power Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th><th>Comment</th></tr>
<tr><td rowspan="2">D7</td><td>0</td><td>Booster Off or has a fault.</td><td>---</td></tr>
<tr><td>1</td><td>Booster On and working OK.</td><td>---</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td>Idle Mode Off.</td><td>---</td></tr>
<tr><td>1</td><td>Idle Mode On.</td><td>---</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td>Partial Mode Off.</td><td>---</td></tr>
<tr><td>1</td><td>Partial Mode On.</td><td>---</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td>Sleep In Mode</td><td>---</td></tr>
<tr><td>1</td><td>Sleep Out Mode</td><td>---</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td>Display Normal Mode Off.</td><td>---</td></tr>
<tr><td>1</td><td>Display Normal Mode On</td><td>---</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td>Display is Off.</td><td>---</td></tr>
<tr><td>1</td><td>Display is On</td><td>---</td></tr>
<tr><td>D1</td><td>--</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>--</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>See description</td></tr>
<tr><td>SW Reset</td><td>See description</td></tr>
<tr><td>HW Reset</td><td>See description</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDIDIF(0A)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

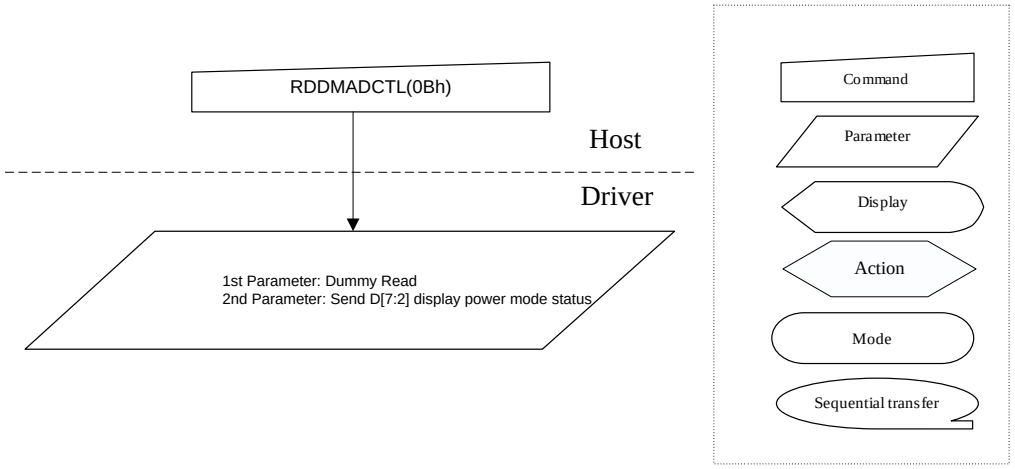
6.2.6 Read Display MADCTL (0Bh)

<table>
<tr><td>0Bh</td><td colspan="13">Read Display MADCTL</td></tr>
<tr><td></td><td>D/</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th><th>Comment</th></tr>
<tr><td rowspan="2">D7</td><td>0</td><td>Top to Bottom (When MADCTL B7=’0’).</td><td>---</td></tr>
<tr><td>1</td><td>Bottom to Top(When MADCTL B7=’1’).</td><td>---</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td>Left to Right (When MADCTL B6=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>Right to Left (When MADCTL B6=’1’)</td><td>---</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td>Normal Mode (When MADCTL B5=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>Reverse Mode (When MADCTL B5=’1’)</td><td>---</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td>LCD Refresh Top to Bottom (When MADCTL B4=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>LCD Refresh Bottom to Top (When MADCTL B4=’1’).</td><td>---</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td>RGB (When MADCTL B3=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>BGR (When MADCTL B3=’1’).</td><td>---</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td>LCD Refresh Left to Right (When MADCTL B2=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>LCD Refresh Right to Left (When MADCTL B2=’1’)</td><td>---</td></tr>
<tr><td>D1</td><td>--</td><td>Switching between Segment outputs and RAM</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>--</td><td>Switching between Segment outputs and RAM</td><td>Set to ‘0’</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

Default

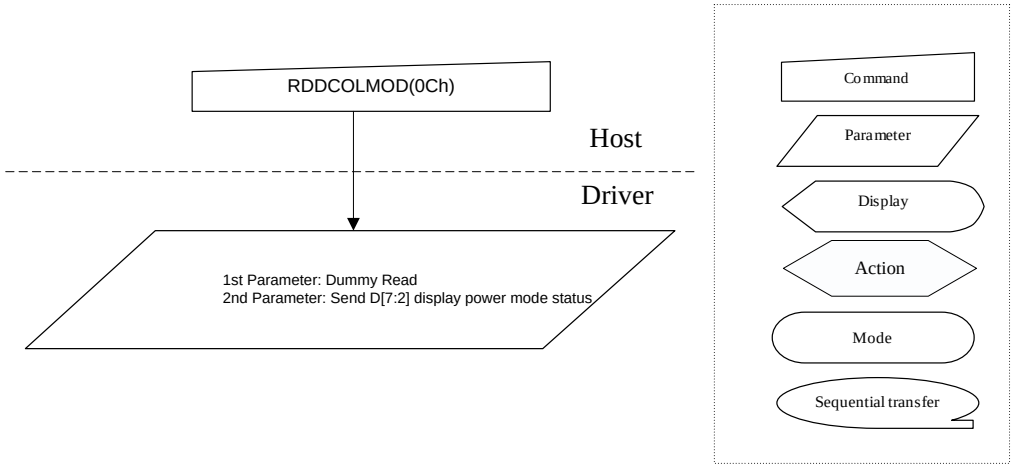
Status	Default Value
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

Flow Chart



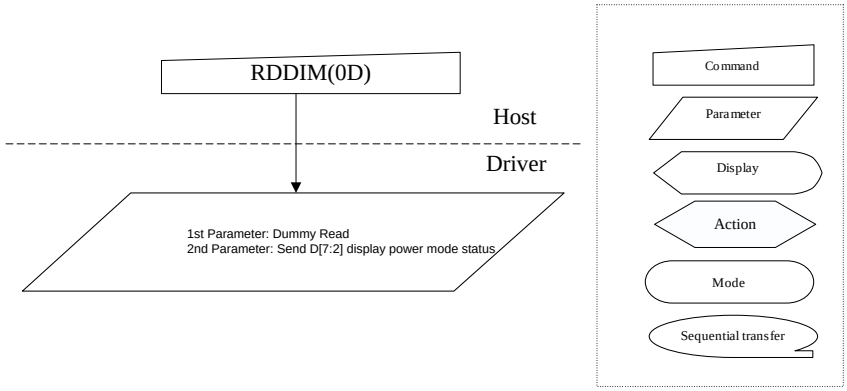
6.2.7 Read Display Pixel Format (0Ch)

<table>
<tr><td>0Ch</td><td colspan="13">Read Display Pixel Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="3">DPI[2:0]</td><td>0</td><td colspan="3">DBI[2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24 bits / pixel</td></tr>
<tr><td colspan="3">others</td><td>Reserved</td></tr>
</table>
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24 bits / pixel</td></tr>
<tr><td colspan="3">others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>RIM</th><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td><td>3’b000</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Chang</td><td>No Chang</td><td>No Chang</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>3’b000</td><td>3’b110</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDCOLMOD(0Ch)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.8 Read Display Image Format (0Dh)

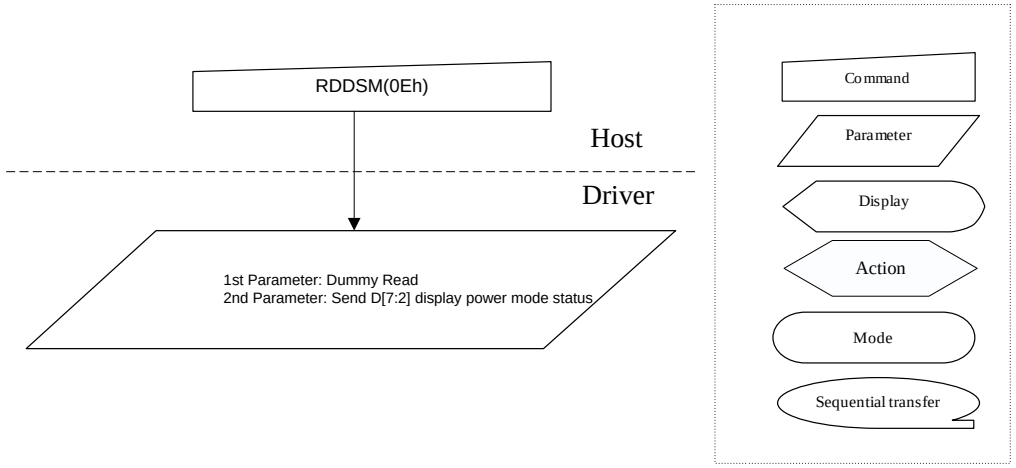
<table>
<tr><td>0Dh</td><td colspan="13">Read Display Image Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>0</td><td>D5</td><td>0</td><td>0</td><td colspan="3">D[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">D7</td><td>Vertical mode off</td><td>0</td></tr>
<tr><td>Vertical mode on</td><td>1</td></tr>
<tr><td rowspan="2">D5</td><td>Inversion off</td><td>0</td></tr>
<tr><td>Inversion on</td><td>1</td></tr>
<tr><td rowspan="5">D[2:0]</td><td>Gamma curve 0</td><td>000</td></tr>
<tr><td>Gamma curve 1</td><td>001</td></tr>
<tr><td>Gamma curve 2</td><td>010</td></tr>
<tr><td>Gamma curve 3</td><td>011</td></tr>
<tr><td>other</td><td>Not define</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>3’b000</td></tr>
<tr><td>SW Reset</td><td>3’b000</td></tr>
<tr><td>HW Reset</td><td>3’b000</td></tr>
</table></td></tr>
</table>

Flow Chart	

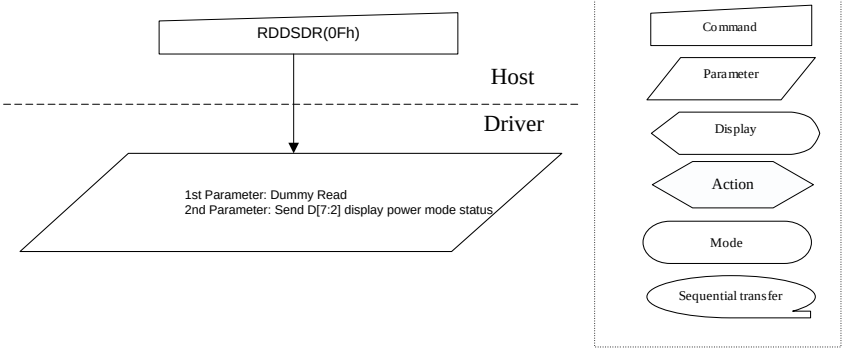
RDDIM(0D)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.9 Read Display Signal Mode (0Eh)

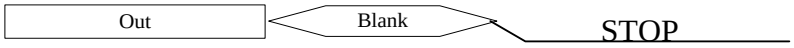
<table>
<tr><td>0Eh</td><td colspan="13">Read Display Signal Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">D7</td><td>0</td><td>Tearing effect line OFF</td></tr>
<tr><td>1</td><td>Tearing effect line ON</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td>Tearing effect line mode 1</td></tr>
<tr><td>1</td><td>Tearing effect line mode 2</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td>Horizontal sync. (RGB interface) OFF</td></tr>
<tr><td>1</td><td>Horizontal sync. (RGB interface) ON</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td>Vertical sync. (RGB interface) OFF</td></tr>
<tr><td>1</td><td>Vertical sync. (RGB interface) ON</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td>Pixel clock (DOTCLK, RGB interface) OFF</td></tr>
<tr><td>1</td><td>Pixel clock (DOTCLK, RGB interface) ON</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td>Data enable (DE,RGB interface) OFF</td></tr>
<tr><td>1</td><td>Data enable (DE,RGB interface) ON</td></tr>
<tr><td>D1</td><td>0</td><td>Reserved</td></tr>
<tr><td>D0</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

Flow Chart	 RDDSM(0Eh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send D[7:2] display power mode status Command Parameter Display Action Mode Sequential transfer

6.2.10 Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><td>0Fh</td><td colspan="13">Read Display Self-Diagnostic Result</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F</td><td>1</td><td>0Fh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>RELD</td><td>FUND</td><td>ATTD</td><td>BRD</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>value</th></tr>
<tr><td>RELD</td><td>Register Loading Detection</td><td>1</td></tr>
<tr><td>FUND</td><td>Functionality Detection</td><td>1</td></tr>
<tr><td>ATTD</td><td>Chip Attachment Detection</td><td>1</td></tr>
<tr><td>BRD</td><td>Display Glass Break Detection</td><td>1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>3’b000</td></tr>
<tr><td>SW Reset</td><td>3’b000</td></tr>
<tr><td>HW Reset</td><td>3’b000</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.11 Enter Sleep Mode (10h)

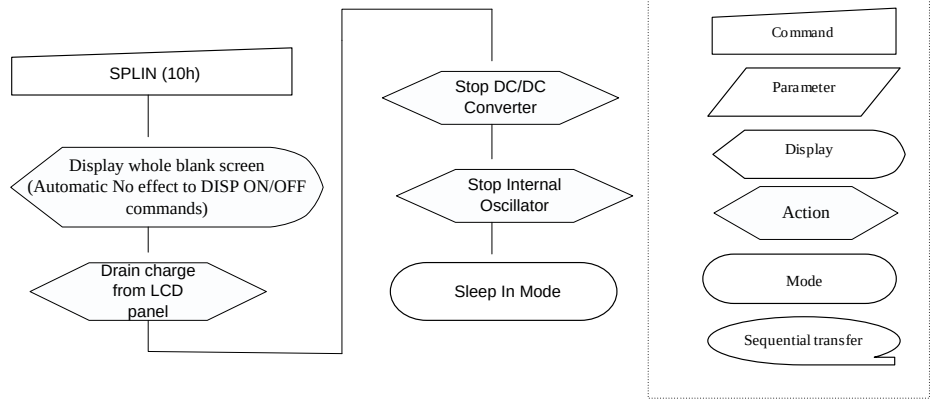
10h	Enter Sleep Mode												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5 msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120 msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued.



6.2.12 Sleep Out Mode (11h)

11h	Sleep Out Mode												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter												
Description	This command turns off sleep mode. The DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												

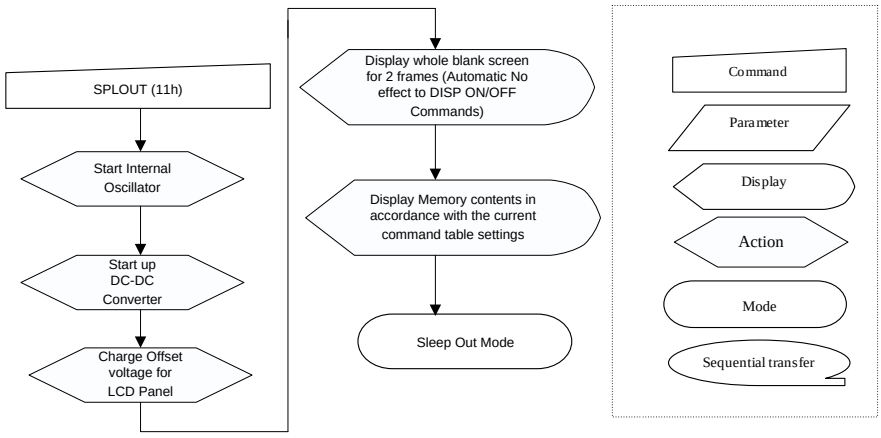
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart



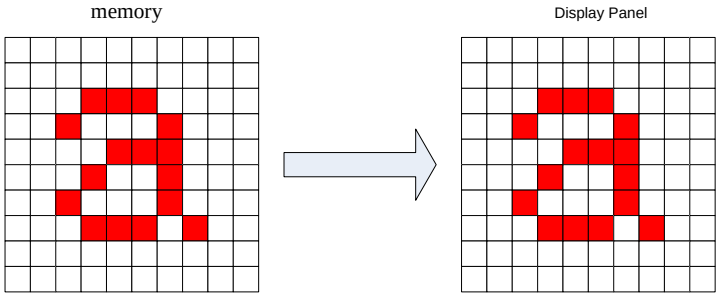
6.2.13 Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

6.2.14 Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

6.2.15 Display Inversion OFF (20h)

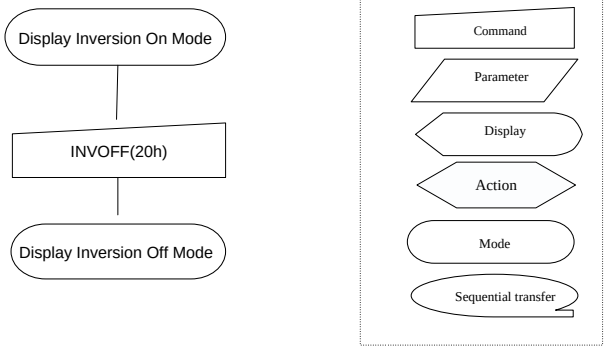
20h	Display Inversion OFF												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. 												
Restriction	This command has no effect when module already is inversion OFF mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

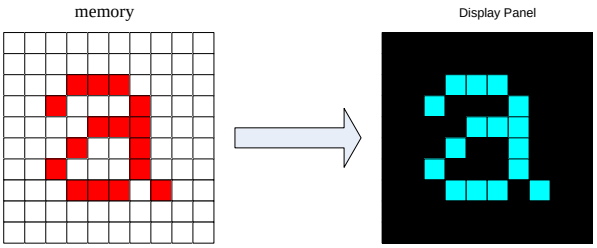
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart	

Display Inversion On Mode
INVOFF(20h)
Display Inversion Off Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.16 Display Inversion ON (21h)

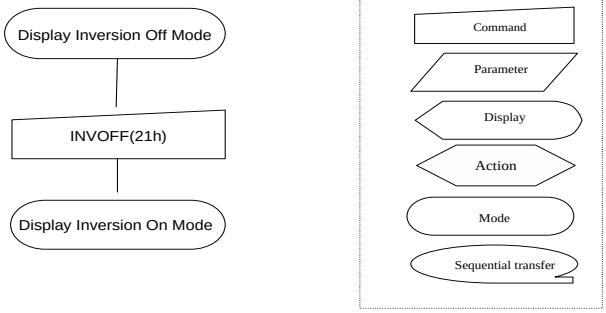
21h	Display Inversion ON												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.. 												
Restriction	This command has no effect when module already is inversion ON mode.												

Register Availability

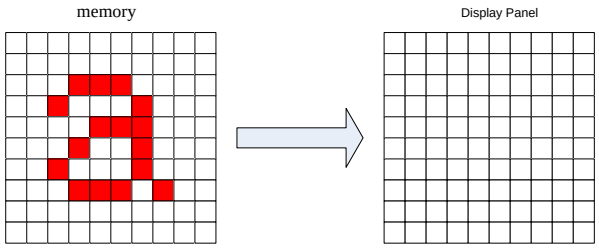
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart	 Display Inversion Off Mode INVOFF(21h) Display Inversion On Mode Command Parameter Display Action Mode Sequential transfer

6.2.17 Display OFF (28h)

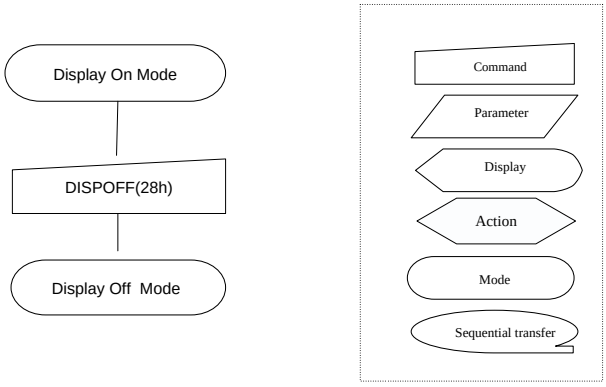
28h	Display OFF												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care												
Restriction	This command has no effect when module is already in display off mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

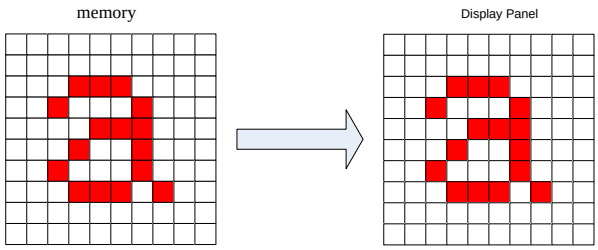
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

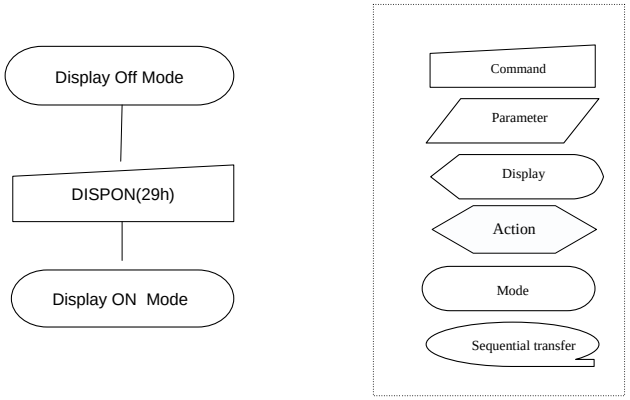
Flow Chart	

Display On Mode
DISPOFF(28h)
Display Off Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.18 Display ON (29h)

<table>
<tr><td>29h</td><td colspan="13">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
</table>

Flow Chart	

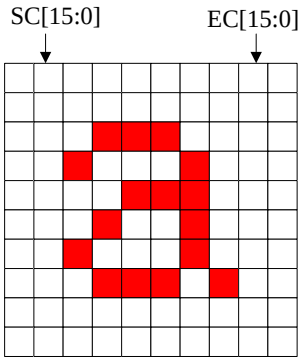
Display Off Mode
DISPON(29h)
Display ON Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.19 Column Address Set (2Ah)

2Ah	Column Address Set												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2nd Parameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note2
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

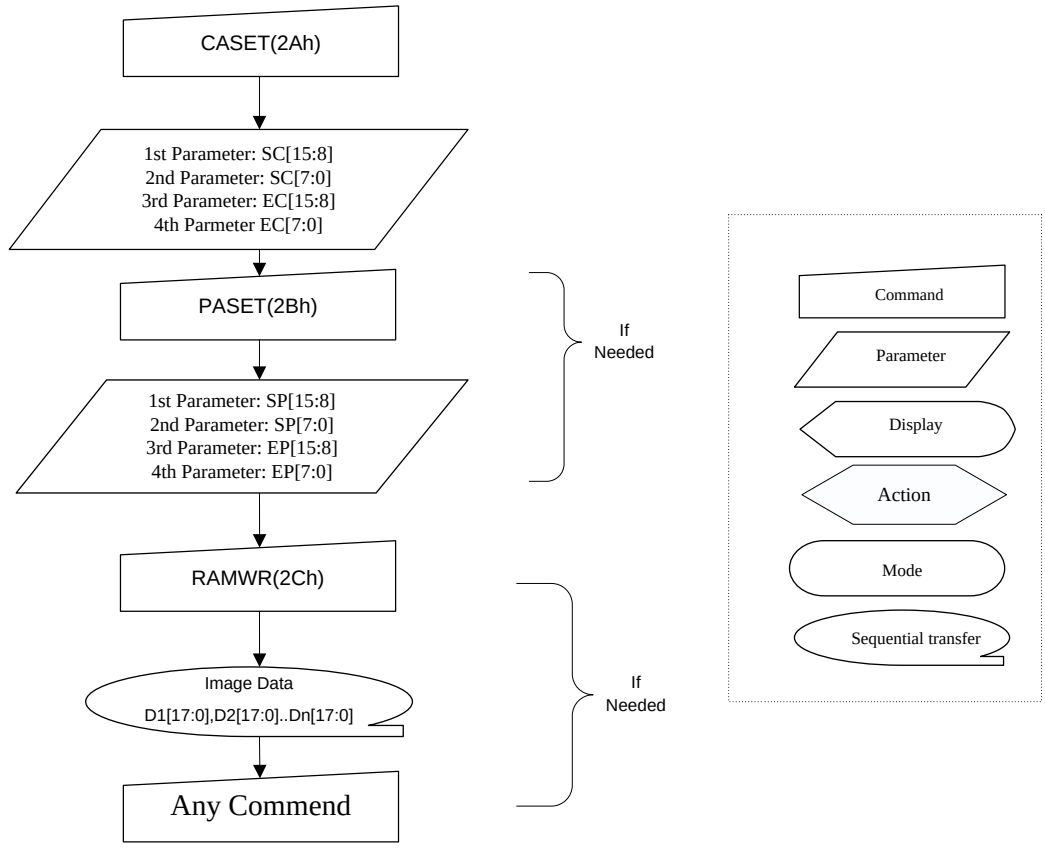
SC [15:0] always must be equal to or less than EC [15:0].
Note 1: When SC [15:0] or EC [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 01DFh (When MADCTL's B5 = 1), data of out of range will be ignored

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

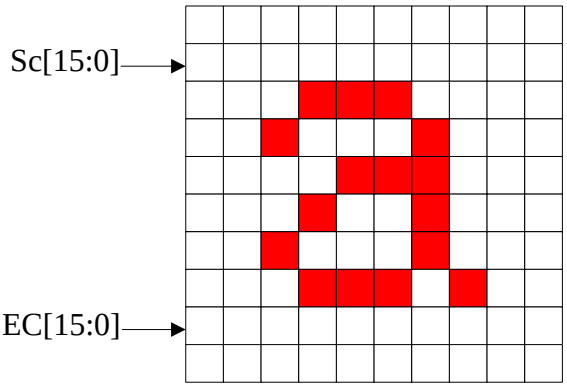
Default

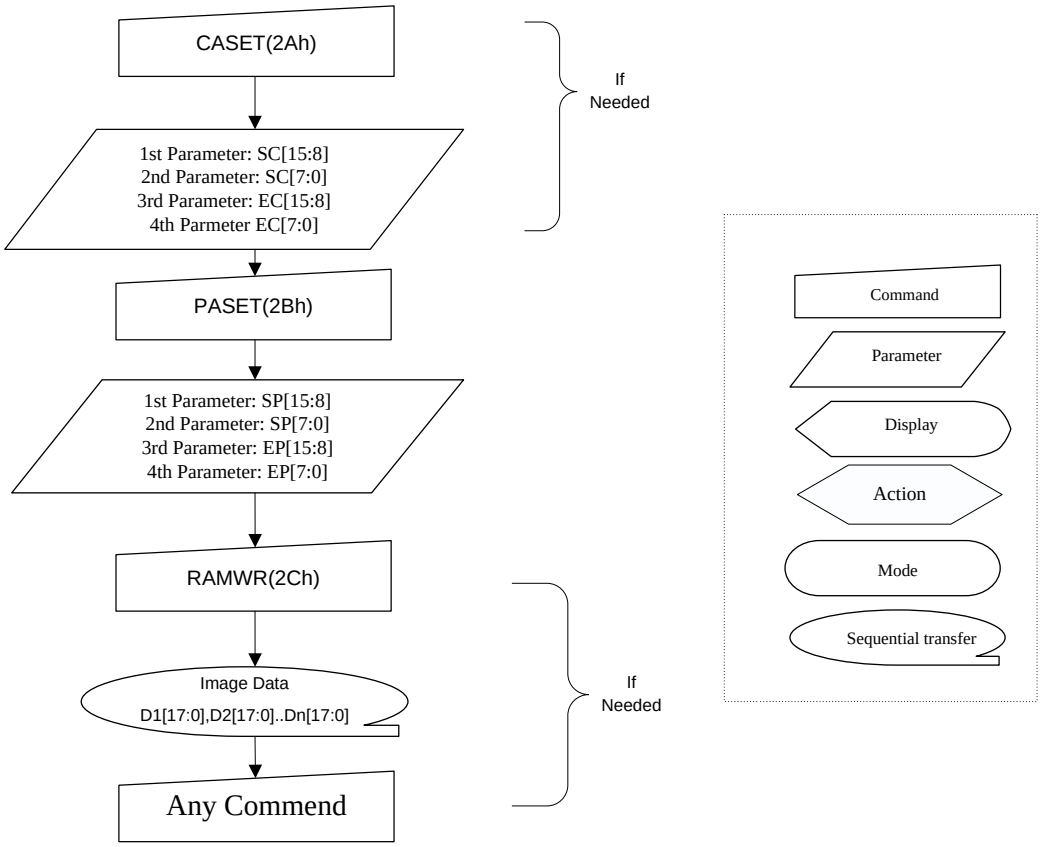
Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=013Fh
SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=013Fh
		If MADCTL's B5 = 1: EC [15:0]=01DFh
HW Reset	SC [15:0]=0000h	EC [15:0]=013Fh

Flow Chart	

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
If Needed
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
If Needed
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.20 Row Address Set (2Bh)

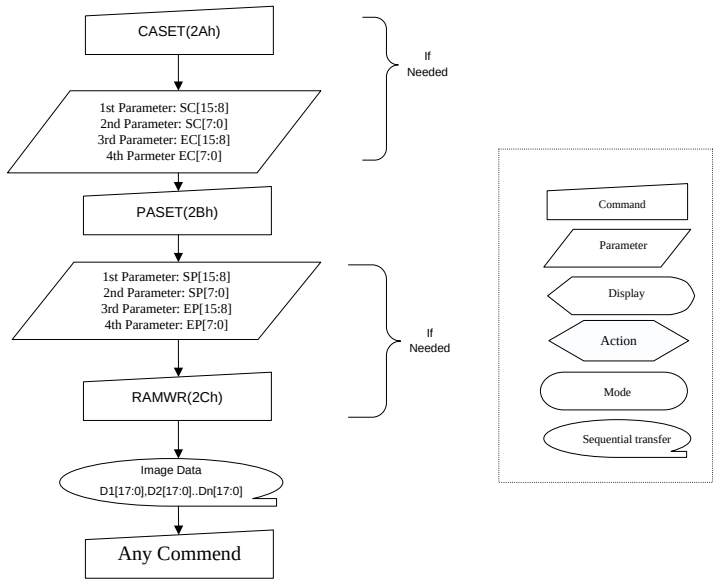
<table>
<tr><td>2Bh</td><td colspan="13">Row Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP15</td><td>SP14</td><td>SP13</td><td>SP12</td><td>SP11</td><td>SP10</td><td>SP9</td><td>SP8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP15</td><td>EP14</td><td>EP13</td><td>EP12</td><td>EP11</td><td>EP10</td><td>EP9</td><td>EP8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP7</td><td>EP6</td><td>EP5</td><td>EP4</td><td>EP3</td><td>EP2</td><td>EP1</td><td>EP0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13">SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 01DFh (When MADCTL’s B5 = 0) or 013Fh (When MADCTL’s B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SP [15:0]=0000h</td><td>EP [15:0]=01DFh</td></tr><tr><td rowspan="2">SW Reset</td><td rowspan="2">SP [15:0]=0000h</td><td>If MADCTL’s B5 = 0: EP [15:0]=01DFh</td></tr><tr><td>If MADCTL’s B5 = 1: EP [15:0]=013Fh</td></tr><tr><td>HW Reset</td><td>SP [15:0]=0000h</td><td>EP [15:0]=01DFh</td></tr></table></td></tr>
</table>

Flow Chart	

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
If Needed
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
If Needed
Any Commend
Command
Parameter
Display
Action
Mode
Sequential transfer

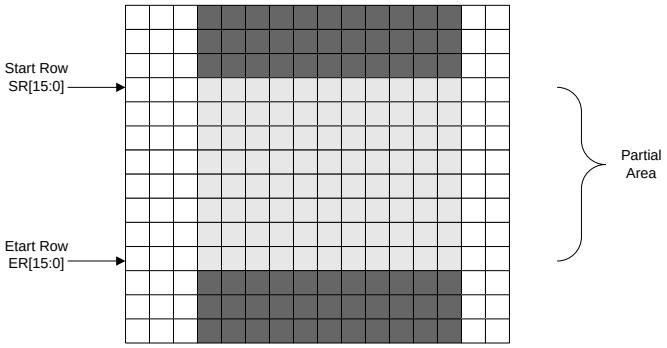
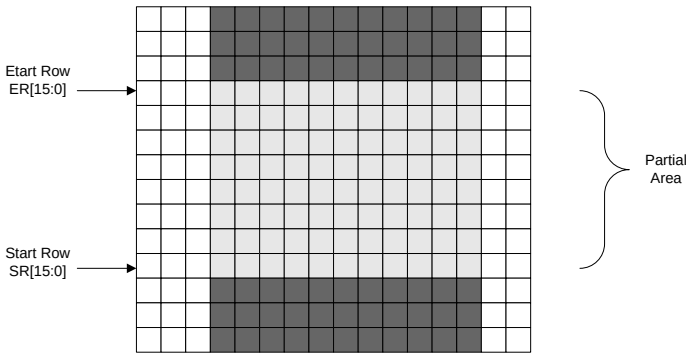
6.2.21 Memory Write (2Ch)

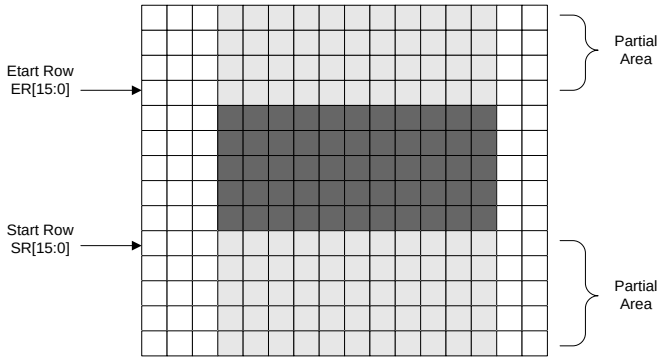
<table>
<tr><td>2Ch</td><td colspan="13">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command transfers image data from GC9403’s frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.
If Memory Access control B5 = 0:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.
If Memory Access Control B5 = 1:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</td></tr>
<tr><td>Restriction</td><td colspan="13">In all color modes, there is no restriction on length of parameters.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is not cleared</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Flow Chart	

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
If Needed
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
If Needed
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.22 Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	DF
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:  If End Row>Start Row when MADCTL B4=1:  If End Row<Start Row when MADCTL B4=0:-													



If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 01EFh.

Register Availability

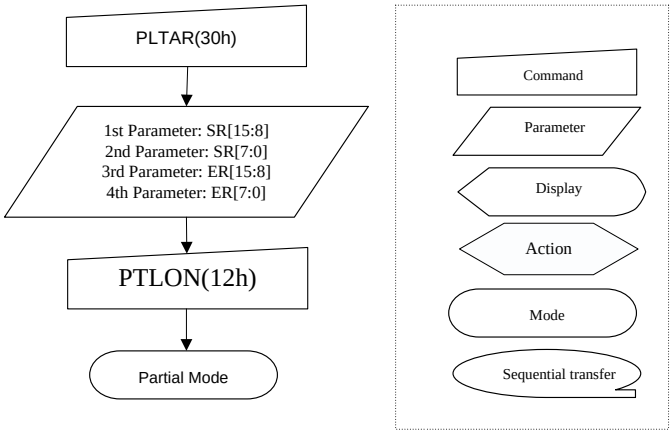
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

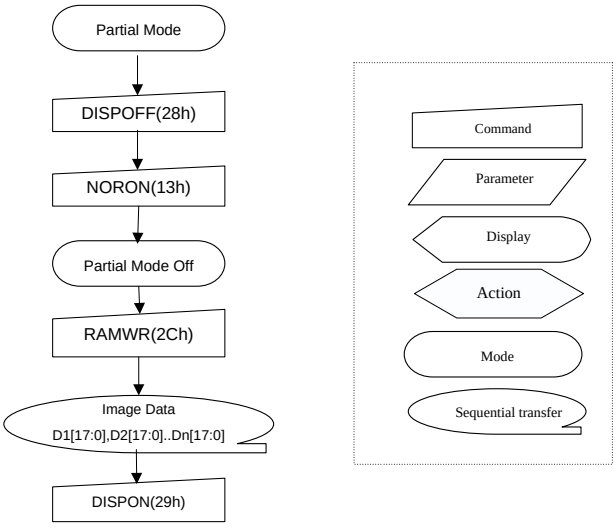
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16’h0000h	16’h01DF
SW Reset	16’h0000h	16’h01DF
HW Reset	16’h0000h	16’h01DF

Flow Chart

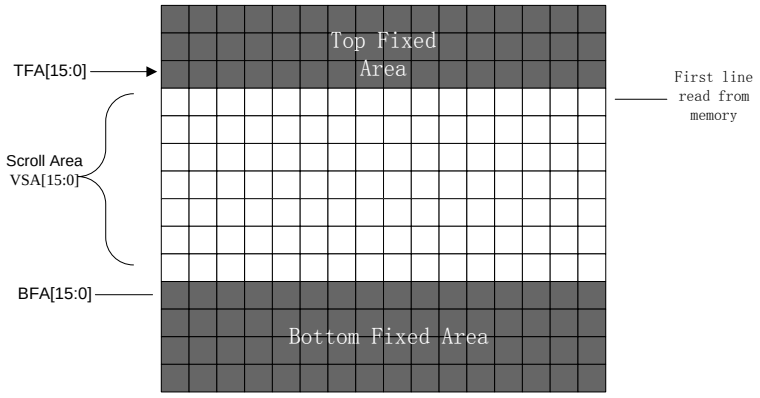
1. To Enter Partial Mode

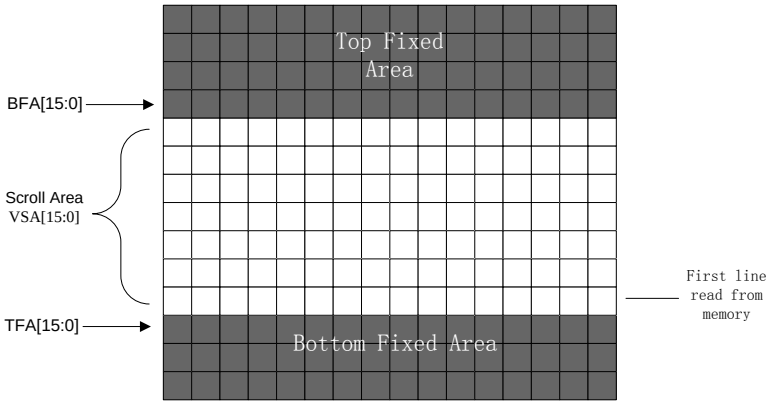


2. To Leave Partial Mode



6.2.23 Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	XX								XX
4th Parameter	1	1	↑	XX	XX								XX
5rd Parameter	1	1	↑	XX	BFA [15:8]								00
6th Parameter	1	1	↑	XX	BFA [7:0]								00
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 5rd & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display) VSA (describes the height of the Vertical Scrolling Area, in No. of lines of the Frame) = 480 – TFA – BFA. Memory [not the display] from the Vertical Scrolling Start Address. The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.  When MADCTL B4=1 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 5rd & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines fromTop of the Frame Memory and Display) VSA (describes the height of the Vertical Scrolling Area, in No. of lines of the Frame) = 480 – TFA – BFA. Memory [not the display] from the Vertical Scrolling Start Address. The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.												



Restriction

Register Availability

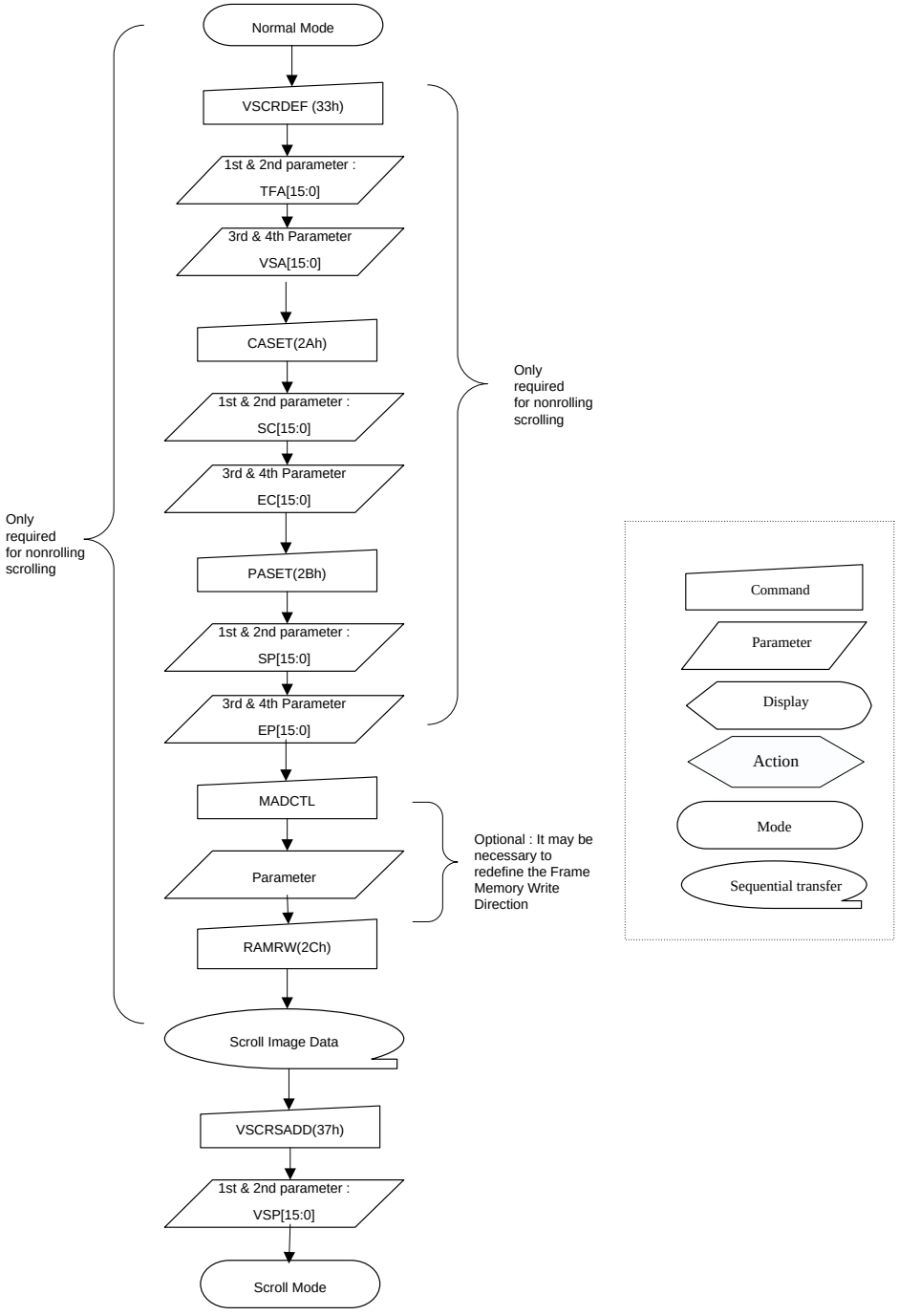
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	BFA [15:0]
Power On Sequence	16'h0000	16'h0000
SW Reset	16'h0000	16'h0000
HW Reset	16'h0000	16'h0000

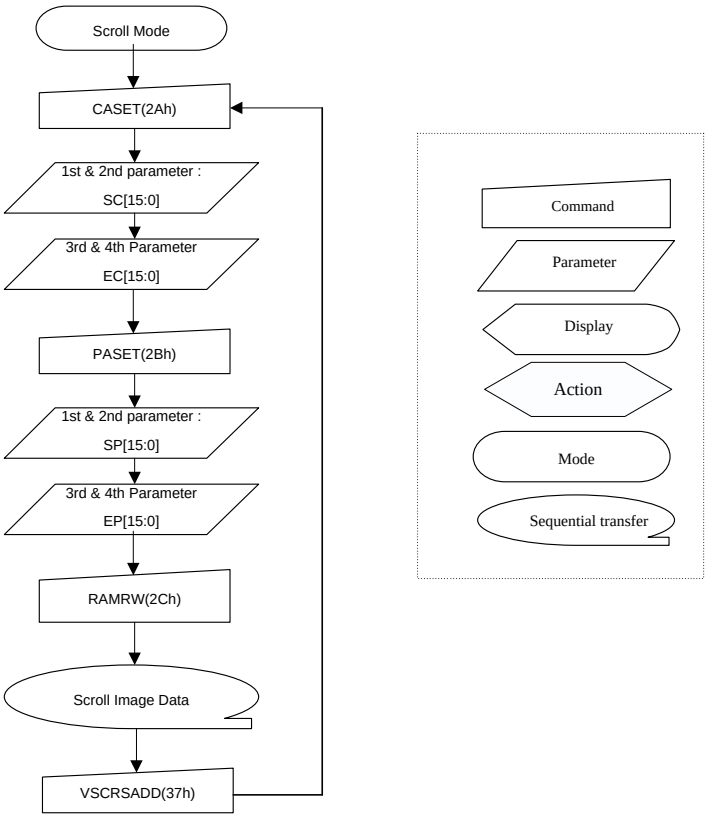
Flow Chart

1. To enter Vertical Scroll Mode :

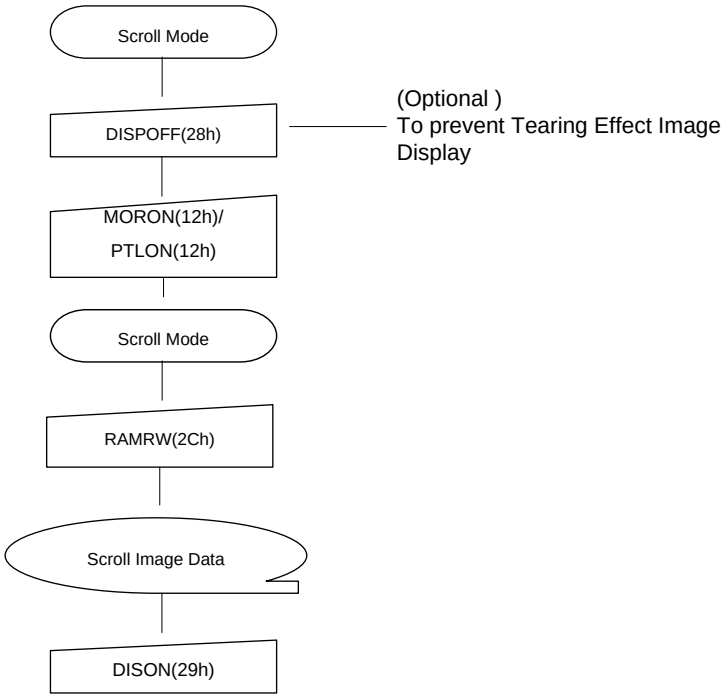


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :

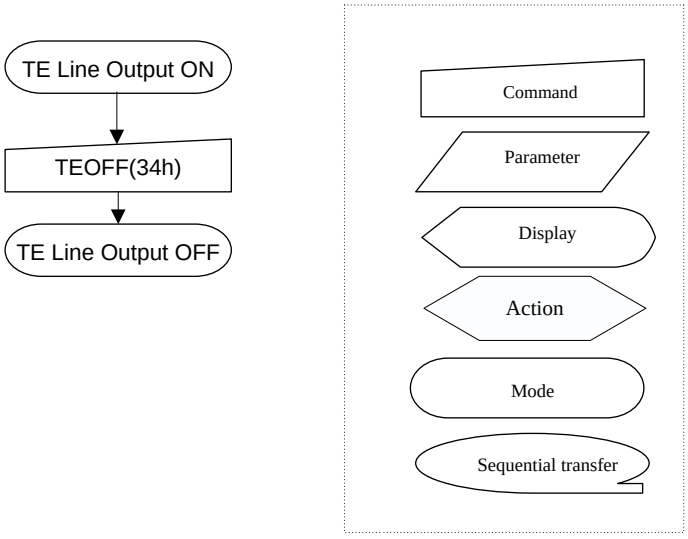


3.To Leave Vertical Scroll Mode:



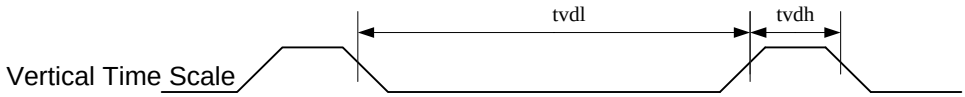
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

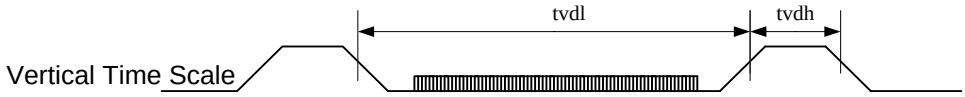
6.2.24 Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

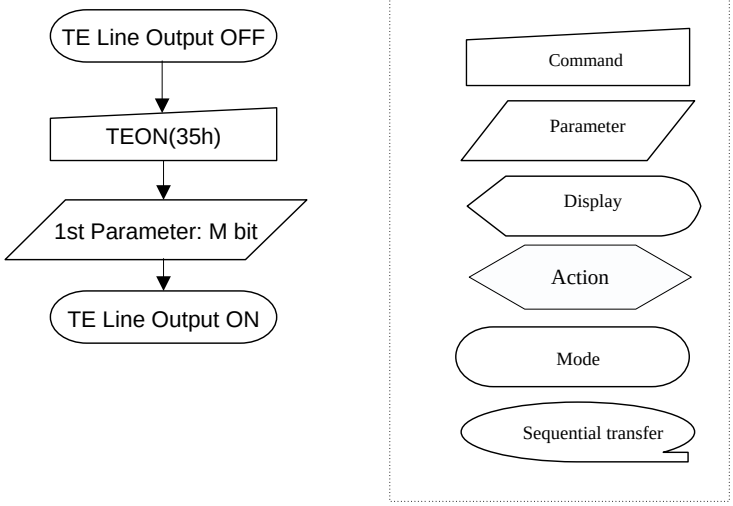
6.2.25 Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.26 Memory Access Control (36h)

36h	Memory Access Control												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

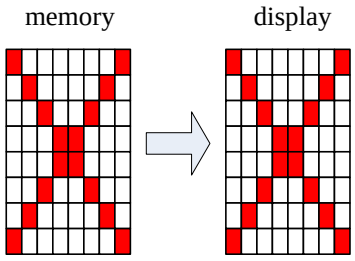
This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

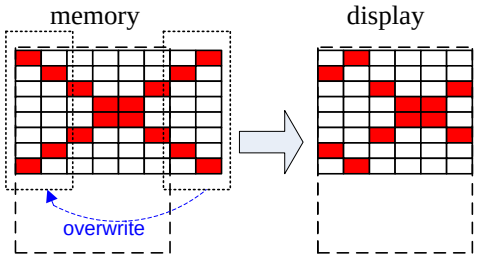
Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

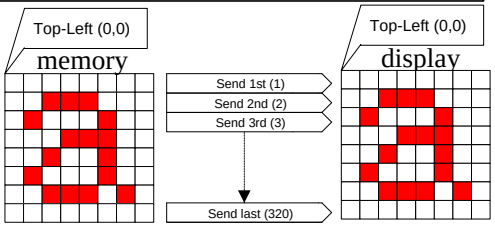
MV(Row / Column Exchange bit)="0"



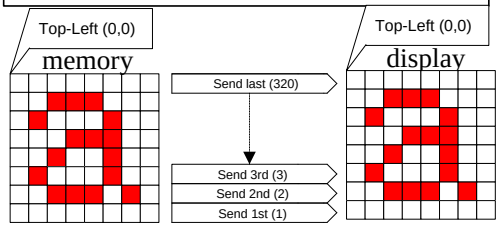
MV(Row / Column Exchange bit)="1"

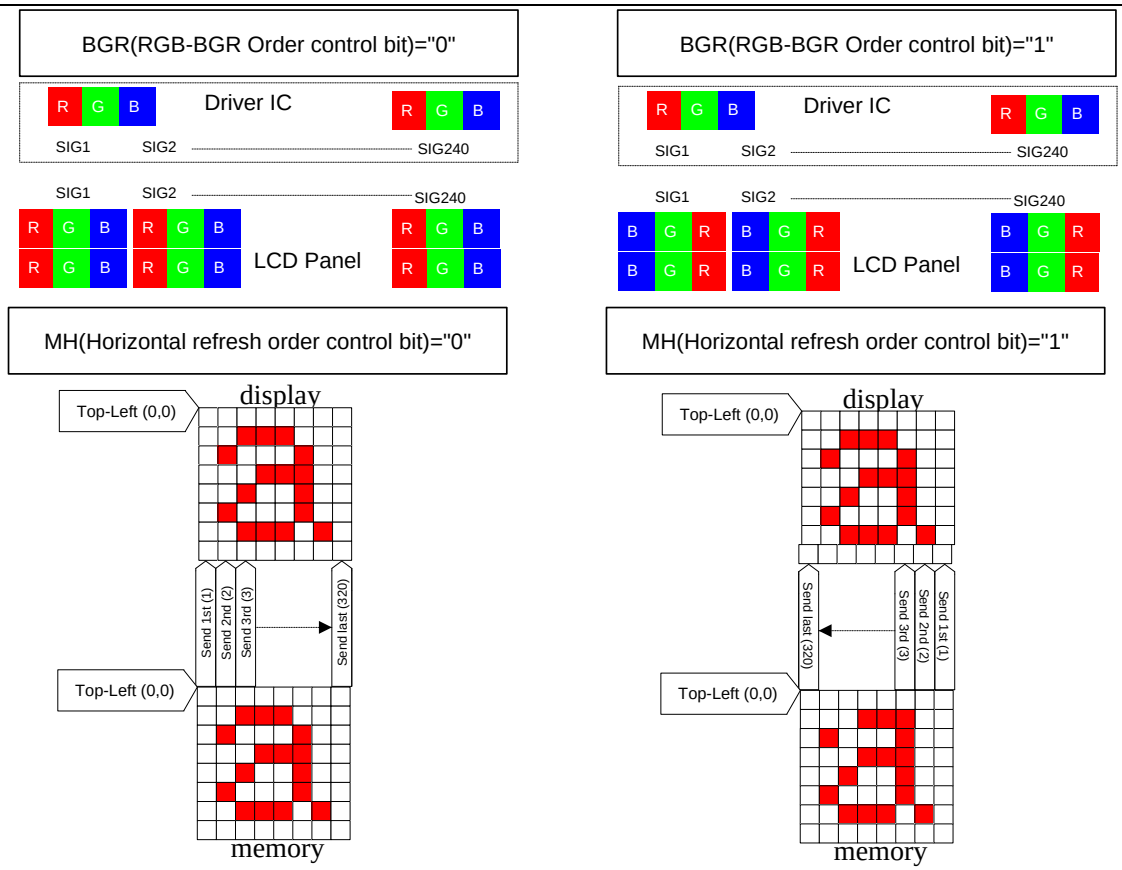


MV(Vertical refresh order bit)="0"

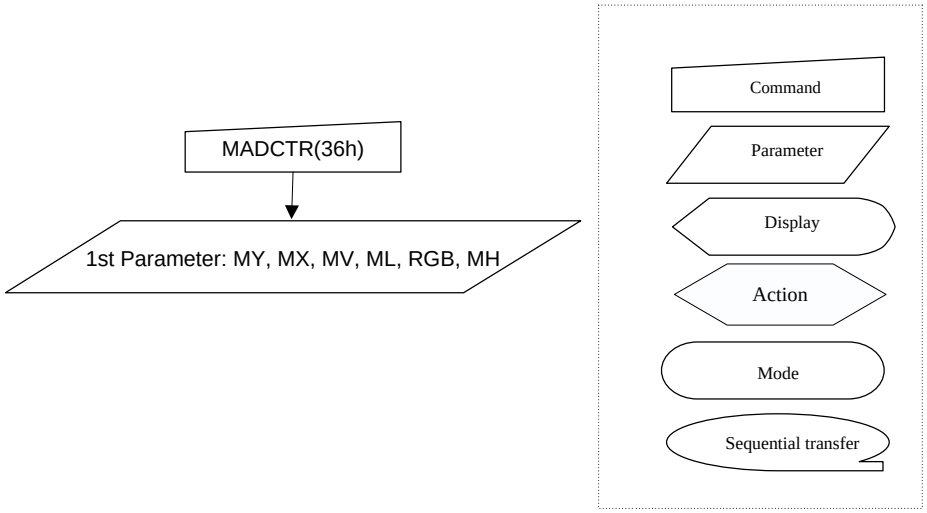


MV(Vertical refresh order bit)="1"



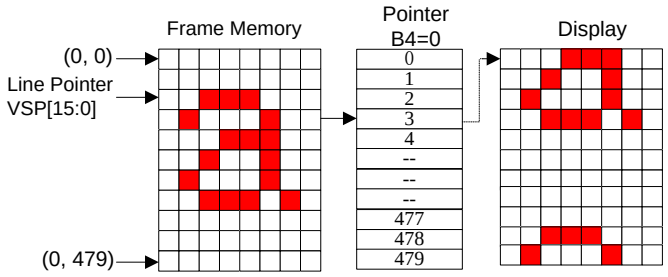
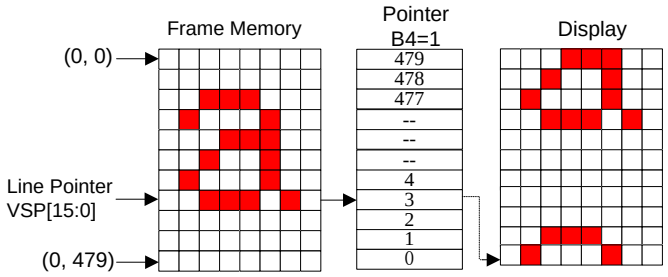
<table>
<tr><td></td><td>


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

MADCTR(36h)
1st Parameter: MY, MX, MV, ML, RGB, MH
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.27 Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								00
2nd Parameter	1	1	↑	XX	VSP [7:0]								00
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When MADCTL B4=0 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 4 and VSP='3'.  When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.  *Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.* *(2) This command is ignored when the GC9403 enters Partial mode.*												
Restriction	This command has no effect when Tearing Effect output is already ON												

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.28 Idle Mode OFF (38h)

38h	Idle Mode OFF												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.												
Restriction	This command has no effect when module is already in idle off mode.												

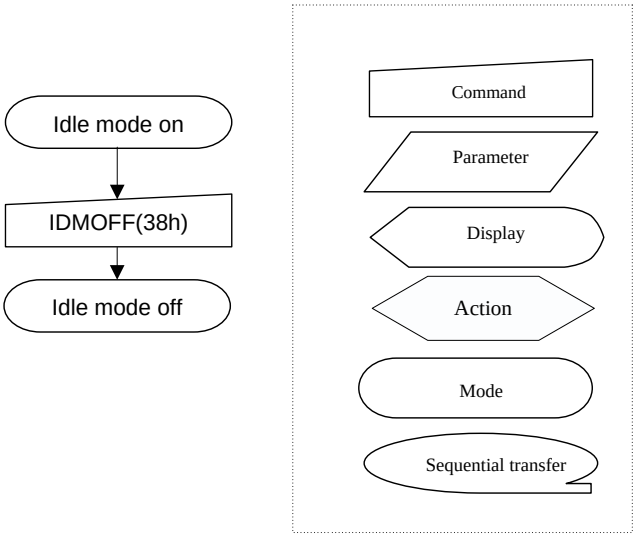
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart

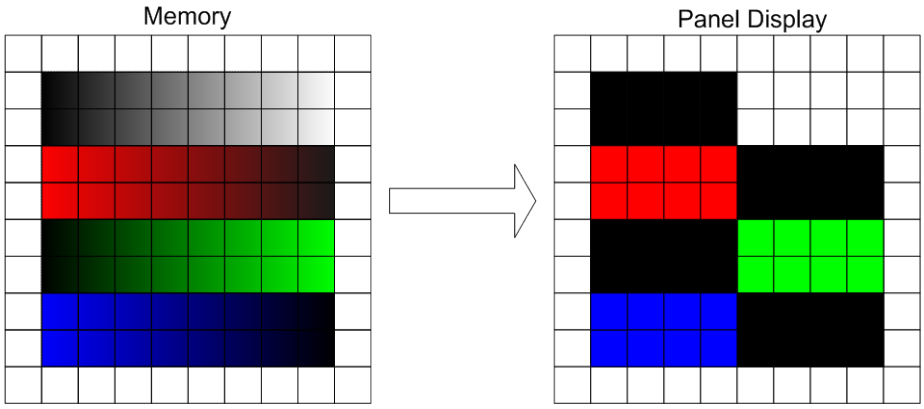


6.2.29 Idle Mode ON (39h)

39h	Idle Mode ON												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



	Memory Contents vs. Display Color		
	R7 R6 R5 R4 R3 R2 R1 R0	G7 G6 G5 G4 G3 G2 G1 G0	B7 B6 B5 B4 B3 B2 B1 B0
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Restriction

This command has no effect when module is already in idle off mode.

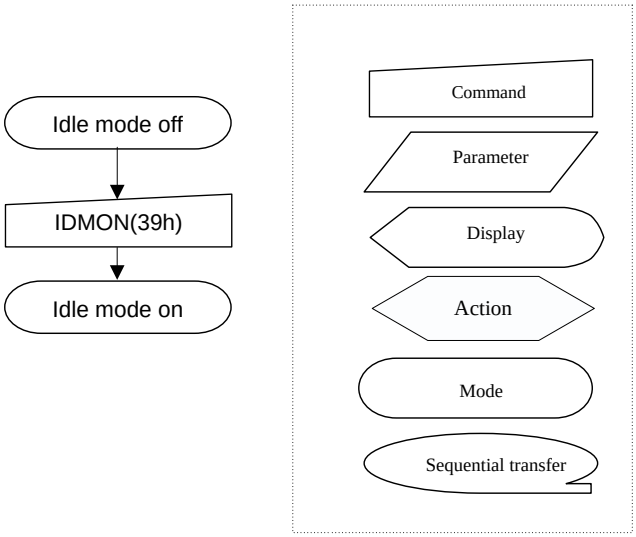
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

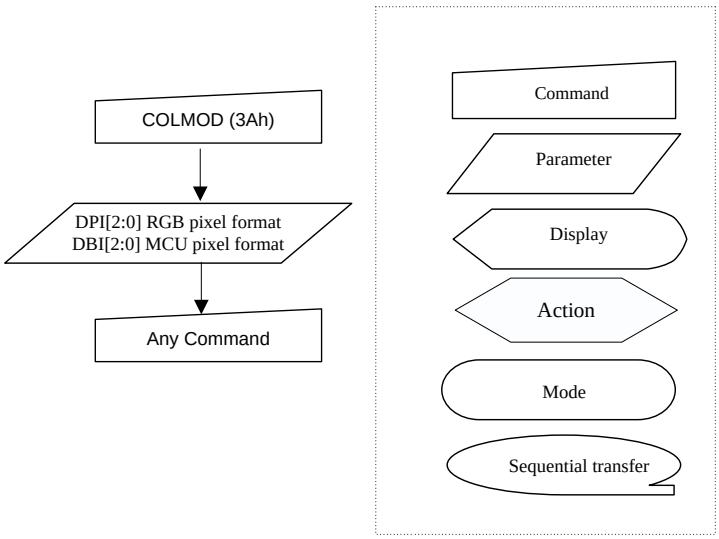
Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



6.2.30 COLMOD: Pixel Format Set (3Ah)

<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="3">DPI [2:0]</td><td>0</td><td colspan="3">DBI [2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24 bits / pixel</td></tr>
</table>
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24 bits / pixel</td></tr>
</table>
If using RGB Interface must selection serial interface.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

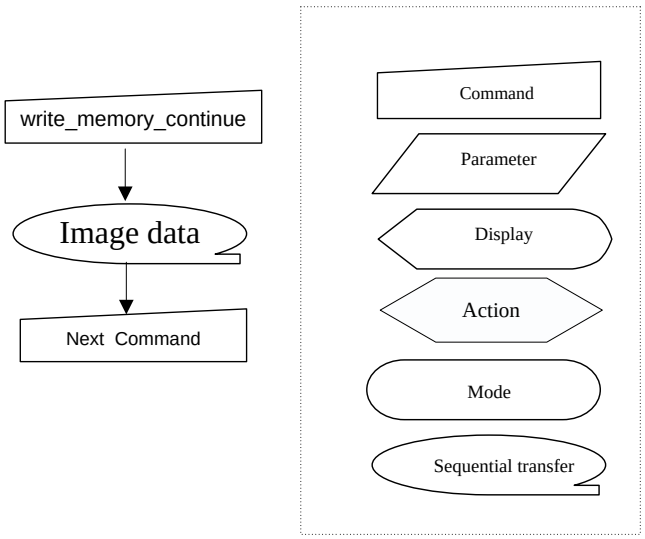
Flow Chart	

COLMOD (3Ah)
DPI[2:0] RGB pixel format
DBI[2:0] MCU pixel format
Any Command
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.31 Write Memory Continue (3Ch)

<table>
<tr><td>3Ch</td><td colspan="13">write_memory_continue</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>3Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1[17:0]</td><td>XX</td></tr>
<tr><td>Xth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx[17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn[17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory, if there is wanted to continue memory write after “Memory Write (2Ch)” command.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on “Memory Write (2Ch)” command.
Then D[17:0] is stored in frame memory and the column register and the page register incremented as table below: Column and Page Counter Control.

<table><tr><th>Condition</th><th>Column counter</th><th>Page counter</th></tr><tr><td>When RAMWR/RAMRD command is accepted</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr><tr><td>Complete Pixel Read/Write action</td><td>Increment by 1</td><td>No change</td></tr><tr><td>The Column counter value is large than “End Column”</td><td>Return to “Start Column”</td><td>Increment by 1</td></tr><tr><td>The Page counter value is large than “End Page”</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr></table>
Sending any other command can stop frame Write.</td></tr>
<tr><td>Restriction</td><td colspan="13">There is no restriction on length of parameters.
No access in the frame memory in Sleep In mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Random value</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>No change</td></tr></table></td></tr>
</table>

Flow Chart	

write_memory_continue
Image data
Next Command
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.32 Write Display Brightness (51h)

51h	Write Display Brightness												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
1st Parameter	1	1	↑	XX	DBV[7:0]								00
Description	This command is used to adjust the brightness value of the display. **DBV[7:0]:** 8 bit, for display brightness of manual brightness setting and CABC in GC9403. There is a PWM output signal, PWM_OUT pin, to control the LED driver IC in order to control display brightness. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												

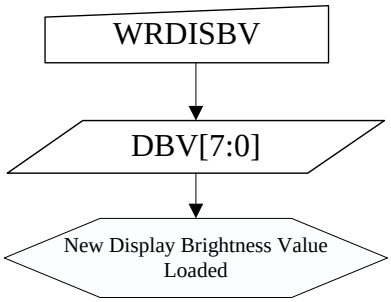
Register Availability

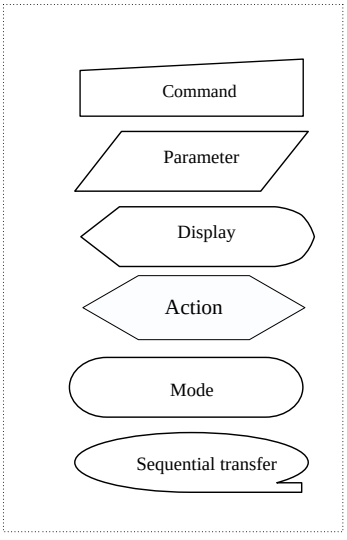
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DBV [7:0]= 8'h00
SW Reset	DBV [7:0]= 8'h00
HW Reset	DBV [7:0]= 8'h00

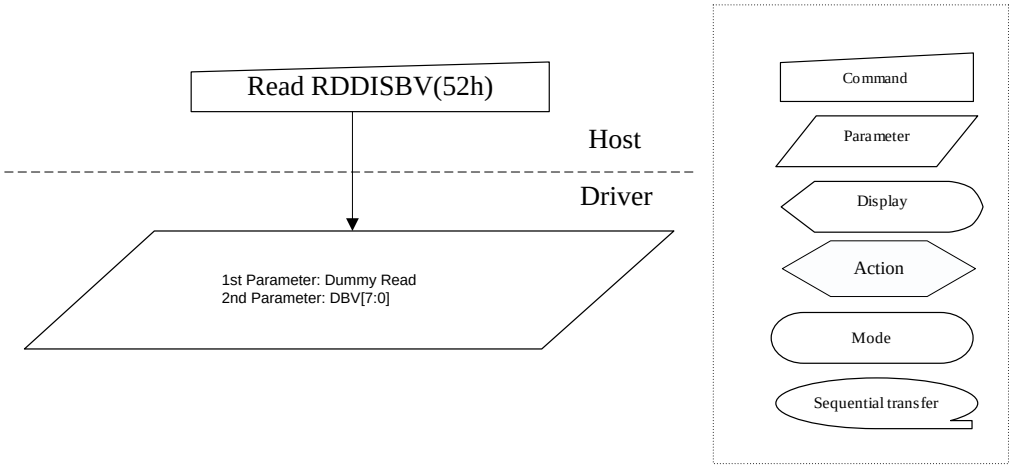
Flow Chart





6.2.33 Read Display Brightness (52h)

<table>
<tr><td>52h</td><td colspan="13">Read Display Brightness</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>52h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XX</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">DBV[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the brightness value of the display.
DBV[7:0] is reset when display is in sleep-in mode.
DBV[7:0] is ‘0’ when bit BCTRL of “Write CTRL Display (53h)” command is ‘0’.
DBV[7:0] is manual set brightness specified with “Write CTRL Display (53h)” command when BCTRL bit is ‘1’.
When bit BCTRL of “Write CTRL Display (53h)” command is ‘1’ and C1/C0 bit of “Write Content Adaptive Brightness Control (55h)” command are ‘0’, DBV[7:0] output is the brightness value specified with “ Write Display Brightness (51h)” command.</td></tr>
<tr><td>Restriction</td><td colspan="13">The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter
(= more than 2 RDX cycle) on DBI Mode.
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>SW Reset</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>HW Reset</td><td>DBV [7:0]= 8’h00</td></tr></table></td></tr>
</table>

Flow Chart	

Read RDDISBV(52h)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: DBV[7:0]
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.34 Write CTRL Display (53h)

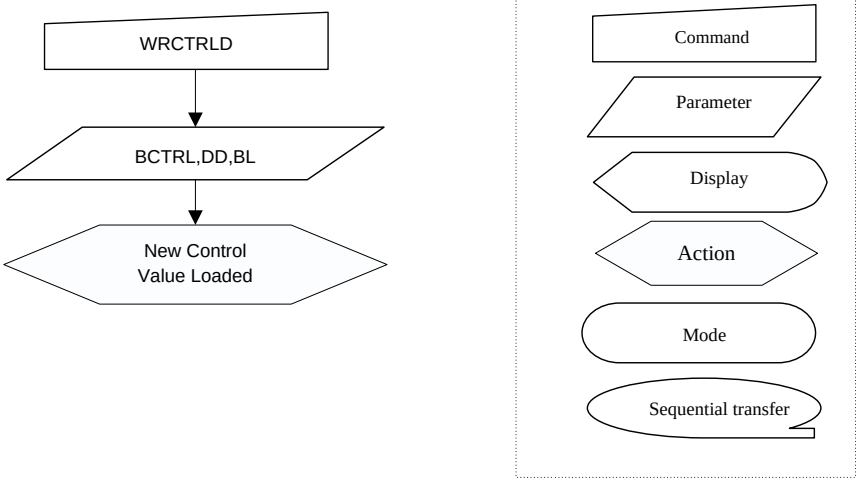
53h	Write CTRL Display												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
1st Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command is used to return brightness setting. **BCTRL**: Brightness Control Block On/Off, '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the DBV[7..0] parameters.) **DD**: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on **BL**: Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

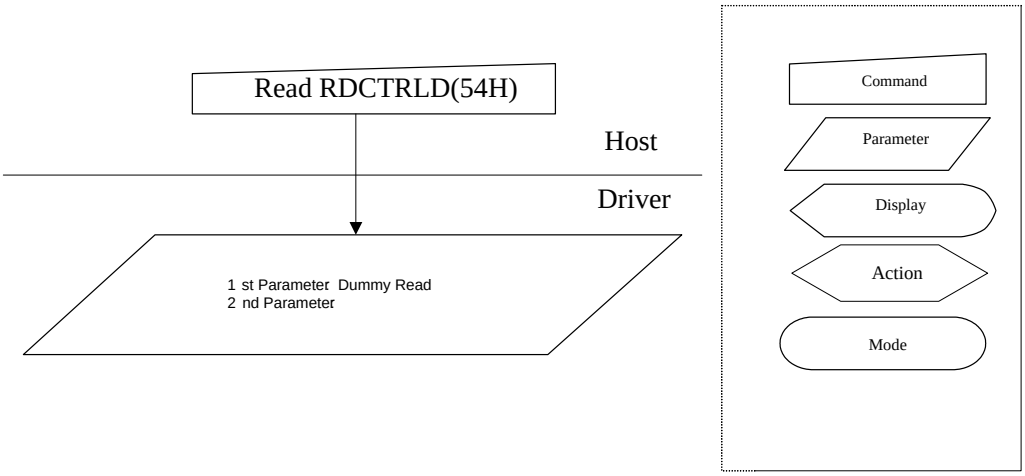
WRCTRLD
BCTRL,DD,BL
New Control
Value Loaded
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.35 Read CTRL Display (54h)

54h	Read CTRL Display												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command is used to control display brightness. **BCTRL**: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) **DD**: Display Dimming, only for manual brightness setting DD = 0: Display Dimming is off DD = 1: Display Dimming is on **BL**: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 →1 or 1→ 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.												
Restriction	None												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1’b0	1’b0	1’b0
SW Reset	1’b0	1’b0	1’b0
HW Reset	1’b0	1’b0	1’b0

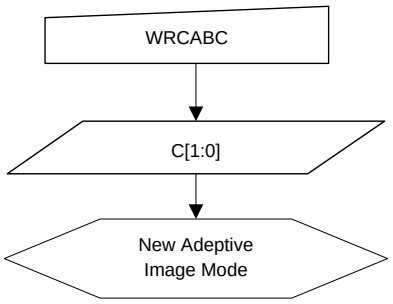
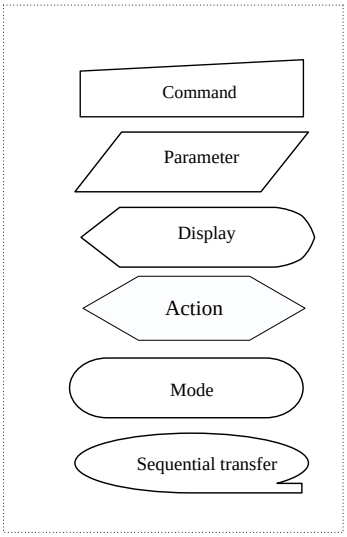
Flow Chart	

Read RDCTRLD(54H)
Host
Driver
1 st Parameter Dummy Read
2 nd Parameter
Command
Parameter
Display
Action
Mode

6.2.36 Write CABC Value (55h)

<table>
<tr><td>55h</td><td colspan="13">Write CTRL Display</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>55h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">C[1:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

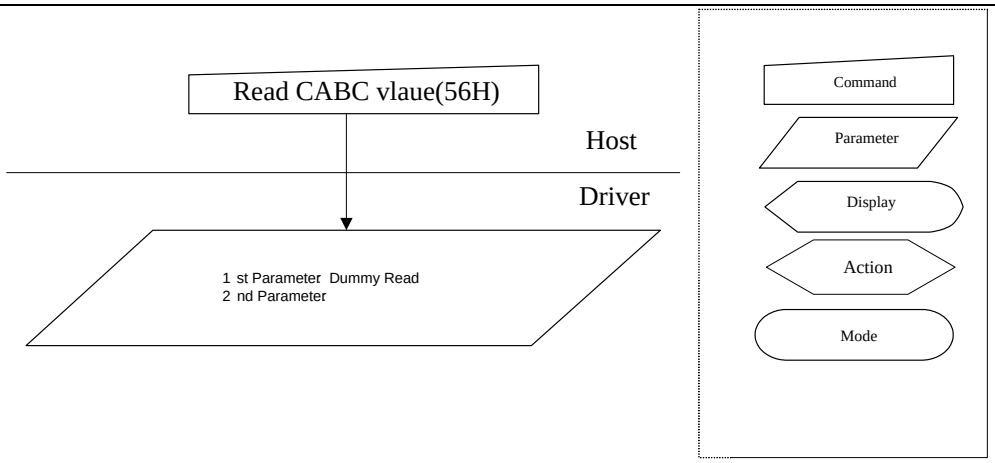
<table><tr><th colspan="2">C[1:0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>CABC OFF</td></tr><tr><td>0</td><td>1</td><td>User Interface Image</td></tr><tr><td>1</td><td>0</td><td>Still Picture</td></tr><tr><td>1</td><td>1</td><td>Moving Image</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table></td></tr>
</table>

Flow Chart	 

6.2.37 Read CABC Value (56h)

<table>
<tr><td>56h</td><td colspan="13">Read CTRL Display</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>56h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XX</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">C[1:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

<table><tr><th colspan="2">C[1:0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>CABC OFF</td></tr><tr><td>0</td><td>1</td><td>User Interface Image</td></tr><tr><td>1</td><td>0</td><td>Still Picture</td></tr><tr><td>1</td><td>1</td><td>Moving Image</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table></td></tr>
</table>

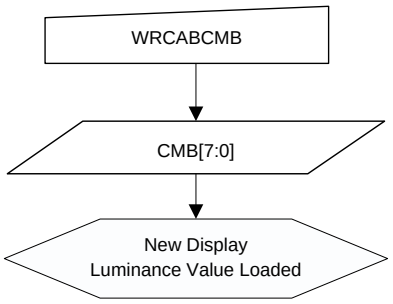
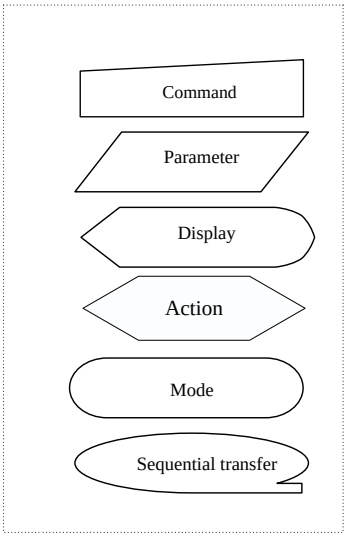
Flow Chart	 Read CABC vlaue(56H) Host Driver 1 st Parameter Dummy Read 2 nd Parameter Command Parameter Display Action Mode

6.2.38 Write CABC Minimum Brightness (5Eh)

5Eh	Write CTRL Display												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
1st Parameter	1	1	↑	XX	CMB[7:0]								00
Description	This command is used to set the minimum brightness value of the display for CABC function. **CMB [7:0]:** CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be et the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												
Restriction													
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	00h
HW Reset	00h

Flow Chart	 WRCABCMB CMB[7:0] New Display Luminance Value Loaded  Command Parameter Display Action Mode Sequential transfer

6.2.39 Read CABC Minimum Brightness (5Fh)

5Fh	Read CTRL Display												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	CMB[7:0]								00
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB [7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (5Eh)” command.												
Restriction	None												

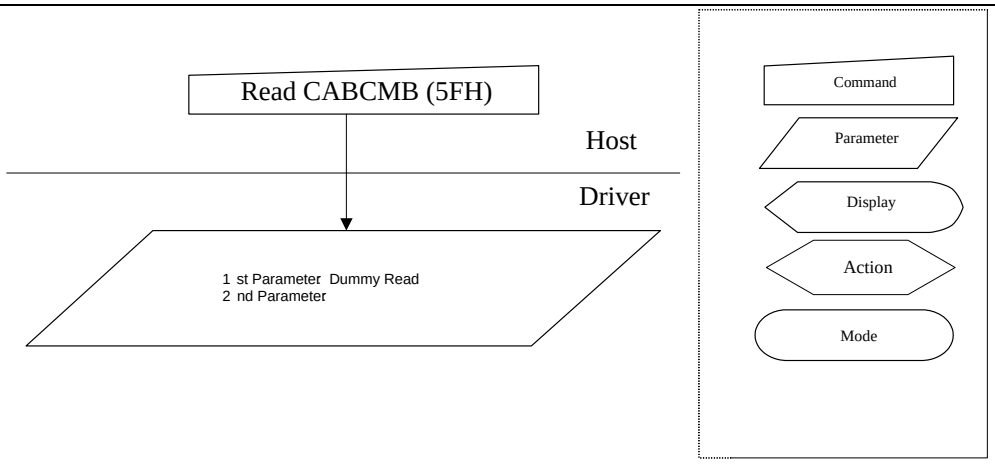
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
HW Reset	00h

Flow Chart



6.2.40 Read ID1 (DAh)

DAh	Read ID1												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1 [7:0]								00
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID.												
Restriction	None												

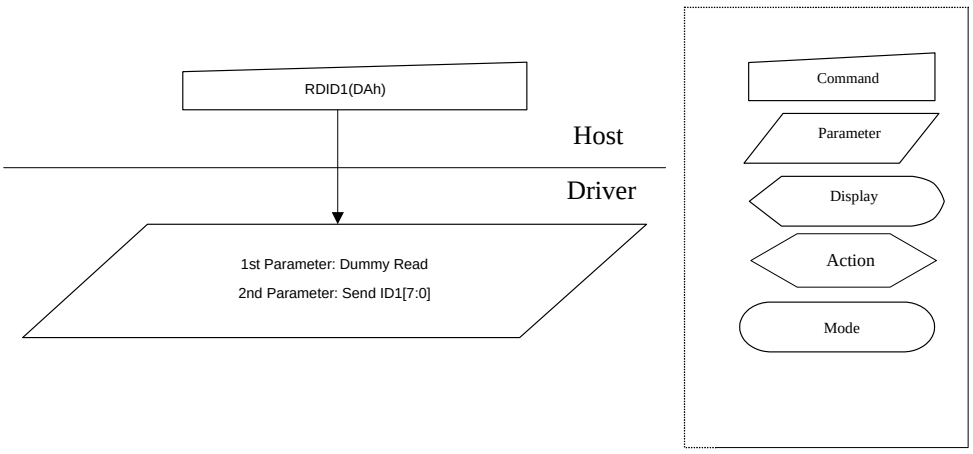
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



6.2.41 Read ID2 (DBh)

DBh	Read ID2												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID2 [7:0]								94
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction	None												

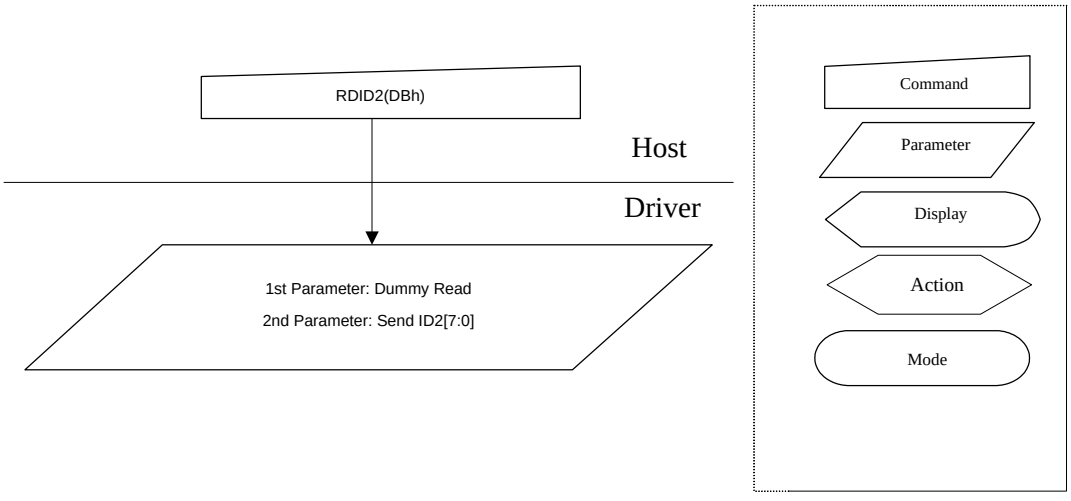
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h94h	MTP value
SW Reset	8'h94h	MTP value
HW Reset	8'h94h	MTP value

Flow Chart



6.2.42 Read ID3 (DCh)

DCh	Read ID3												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								03
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

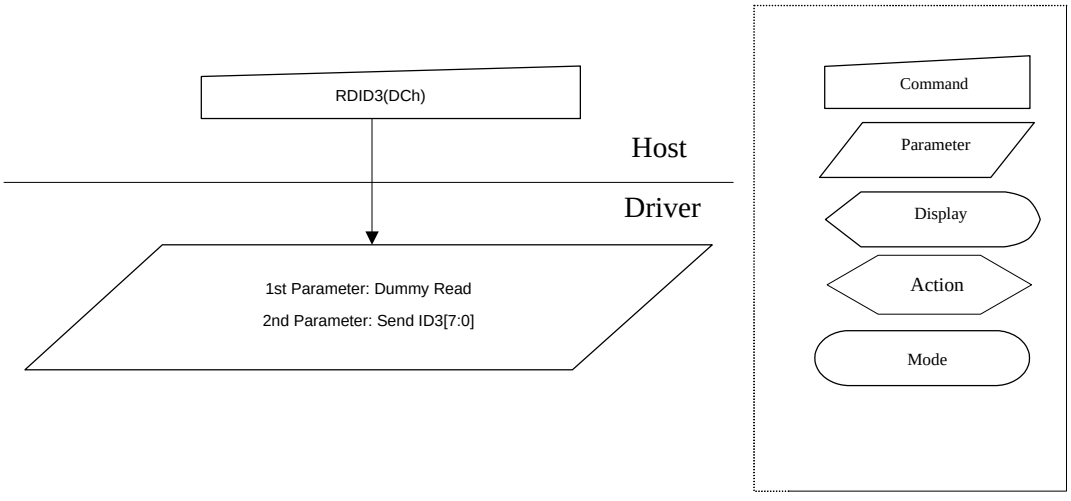
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

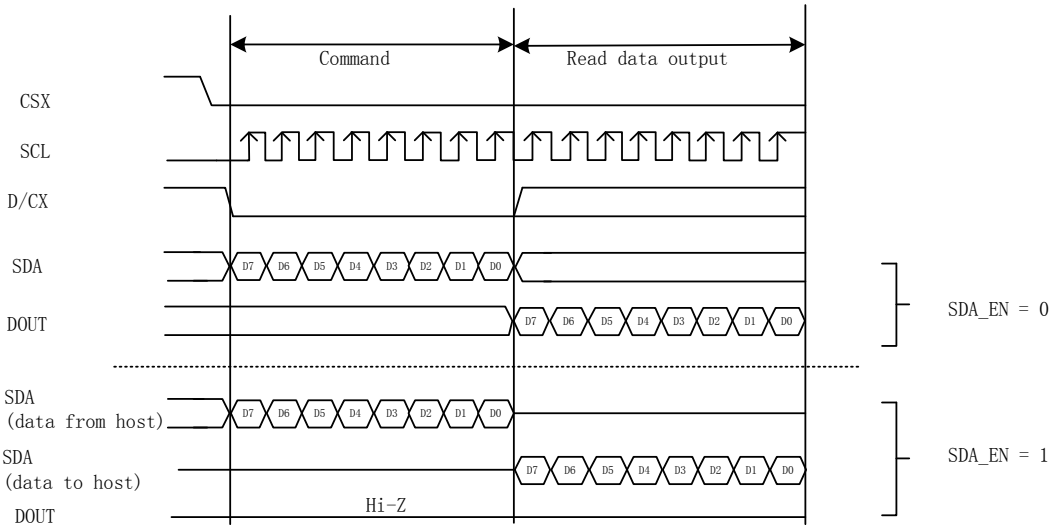
Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h01h	MTP value
SW Reset	8'h01h	MTP value
HW Reset	8'h01h	MTP value

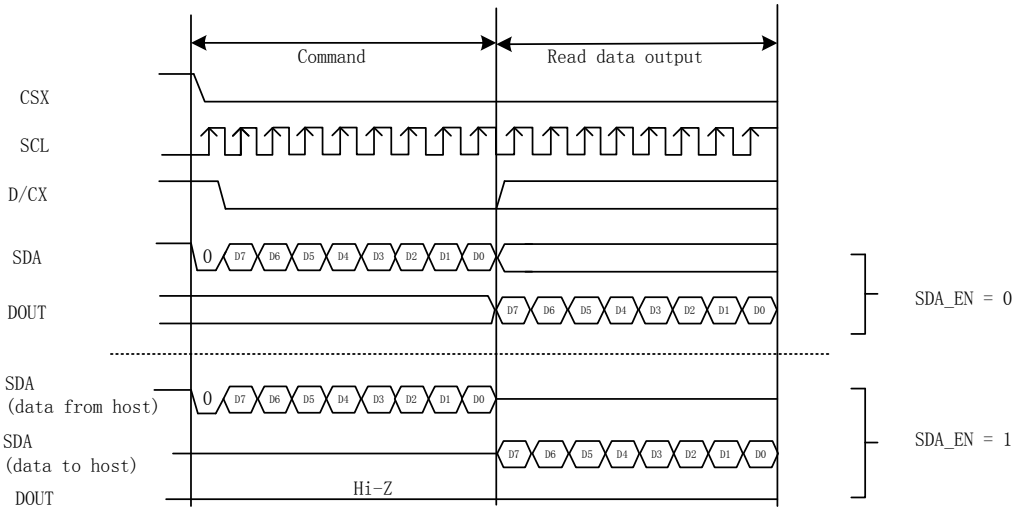
Flow Chart



6.3 Description of Level 2 Command

6.3.1 RGB Interface Signal Control (B0h)

B0h	RGB Interface Signal Control												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
1st Parameter	1	1	↑	XX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	40
Description	Sets the operation status of the display interface. The setting becomes effective as soon as the command is received. **EPL**: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface) **DPL**: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time) **HSPL**: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock) **VSPL**: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock) **SDA_EN**: 3/4 wire serial interface selection SDA_EN = “0”, DIN and DOUT pins are used for 3/4 wire serial interface. SDA_EN = “1”, DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used. 												



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	SDA_EN	VSPL	HSPL	DPL	EPL
Power On Sequence	1’b0	1’b0	1’b0	1’b0	1’b0
SW Reset	1’b0	1’b0	1’b0	1’b0	1’b0
HW Reset	1’b0	1’b0	1’b0	1’b0	1’b0

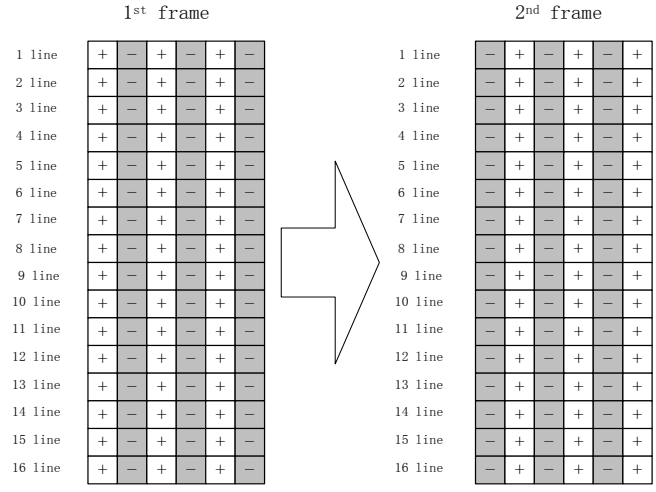
6.3.2 Display Inversion Control (B4h)

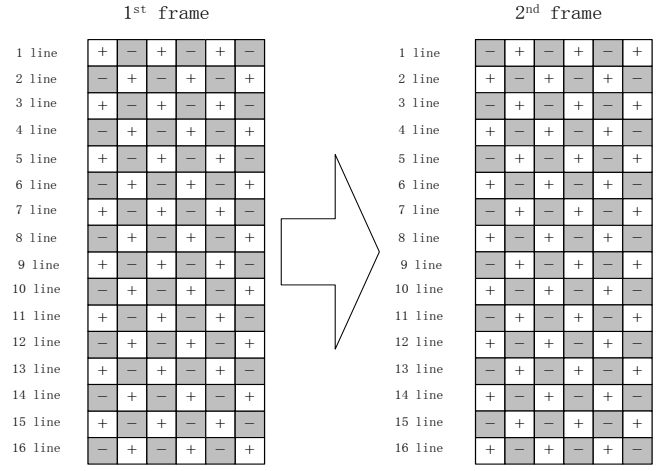
B4h	Display Inversion Control												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	0	0	0	0	0	DINV[2:0]			00

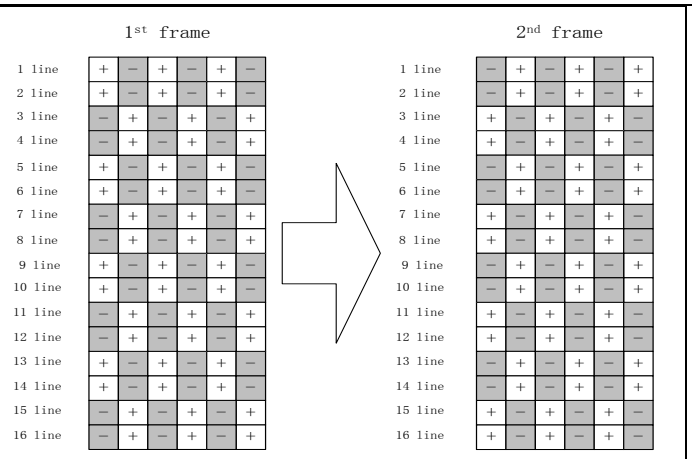
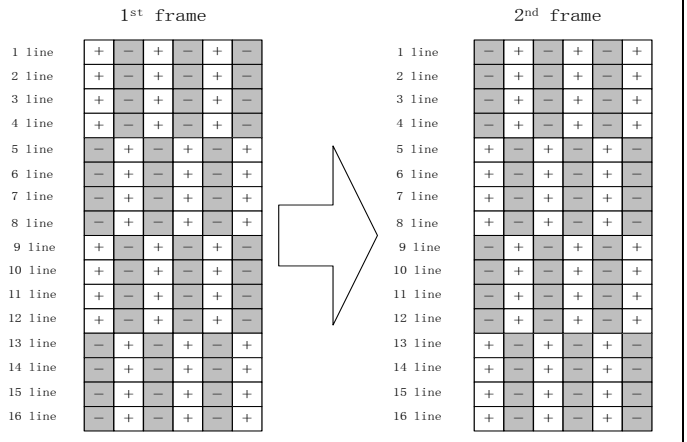
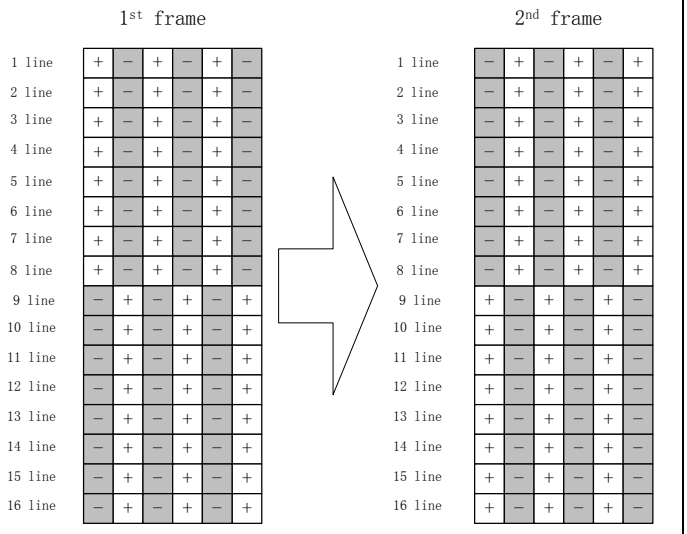
Description

DIN[2:0] : set the inversion mode

DINV[2:0]	Dot inversion mode
3'b000	Colum inversion
3'b001	1-dot inversion





		3'b010	2-dot inversion	
		3'b011	4-dot inversion	
		3'b100	8-dot inversion	
		others	Setting prohibited	
Restriction				

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DINV[2:0]
Power On Sequence	3'b000
SW Reset	3'b000
HW Reset	3'b000

6.3.3 Blanking Porch Control (B5h)

<table>
<tr><td>B5h</td><td colspan="13">Blanking Porch Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>B5h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VFP [7:0]</td><td>02</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VBP [7:0]</td><td>02</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td colspan="5">0</td><td>00</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">HBP [7:0]</td><td>04</td></tr>
<tr><td>Description</td><td colspan="13">
VFP [7:0] / VBP [7:0]: The VFP [7:0] and VBP [7:0] bits specify the line number of vertical front and back porch period respectively.
<table>
<tr><th>VFP [7:0]</th><th>Number of lines of front porch</th><th>VBP [7:0]</th><th>Number of lines of back porch</th></tr>
<tr><td>00000000</td><td>Setting inhibited</td><td>00000000</td><td>Setting inhibited</td></tr>
<tr><td>00000001</td><td>Setting inhibited</td><td>00000001</td><td>Setting inhibited</td></tr>
<tr><td>00000010</td><td>2</td><td>00000010</td><td>2</td></tr>
<tr><td>00000011</td><td>3</td><td>00000011</td><td>3</td></tr>
<tr><td>00000100</td><td>4</td><td>00000100</td><td>4</td></tr>
<tr><td>:
:</td><td>:
:</td><td>:
:</td><td>:
:</td></tr>
<tr><td>11111101</td><td>253</td><td>11111101</td><td>253</td></tr>
<tr><td>11111110</td><td>254</td><td>11111110</td><td>254</td></tr>
<tr><td>11111111</td><td>255</td><td>11111111</td><td>255</td></tr>
</table>
HBP [7:0]: HBP [7:0] bits specify the line number of horizontal front and back porch period respectively.
<table>
<tr><th>HBP [7:0]</th><th>Number of dotclk of front porch</th></tr>
<tr><td>00000000</td><td>Setting inhibited</td></tr>
<tr><td>00000001</td><td>Setting inhibited</td></tr>
<tr><td>00000010</td><td>2</td></tr>
<tr><td>00000011</td><td>3</td></tr>
<tr><td>00000100</td><td>4</td></tr>
<tr><td>00000101</td><td>5</td></tr>
<tr><td>:
:</td><td>:
:</td></tr>
<tr><td>11111101</td><td>253</td></tr>
<tr><td>11111110</td><td>254</td></tr>
<tr><td>11111111</td><td>255</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>VFP [7:0]</th><th>VBP [7:0]</th><th>HBP [7:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h02h</td><td>7’h02h</td><td>7’h04h</td></tr>
<tr><td>SW Reset</td><td>7’h02h</td><td>7’h02h</td><td>7’h04h</td></tr>
<tr><td>HW Reset</td><td>7’h02h</td><td>7’h02h</td><td>7’h04h</td></tr>
</table>
</td></tr>
</table>

6.3.4 Display Function Control (B6h)

B6h	Display Function Control												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	0	RCM	RM	DM	0	0	PTS	0	00
2nd Parameter	1	1	↑	XX	0	GS	SS	SM	0	0	0	0	00
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						3B

Description

RCM: RGB interface selection (refer to the RGB interface section).

RCM	RGB interface mode
0	DE mode
1	VSYNC mode

RM: Select the interface to access the GRAM. When RM='0', the driver will write display data to GRAM via system interface and the driver will write display data to GRAM via RGB interface when RM='1'.

RM	interface for RAM access
0	Internal system clock
1	RGB interface

DM: Select the display operation mode.

DM	interface mode
0	Internal system clock
1	RGB interface

PTS: Determine source output in a non-display area in the partial display mode.

PTS	Source output on non-display area
0	V63
1	V0

GS: Sets the direction of scan by the gate driver

GS	Gate Output Scan Direction
0	G1→G480
1	G480→G1

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction
0	S1 → S960
1	S960 → S1

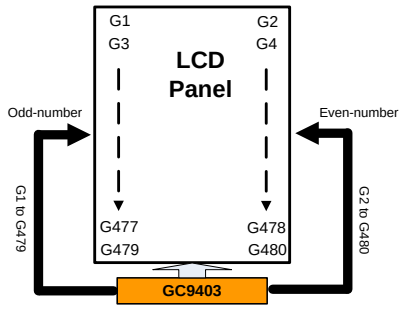
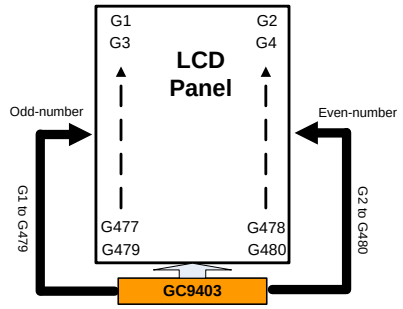
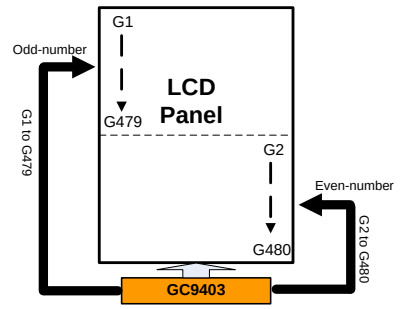
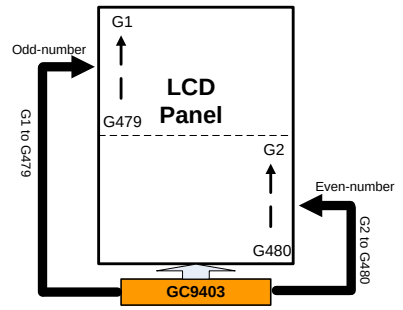
In addition to the shift direction, the settings for both SS and BGR bits are required to change the

assignment of R, G, and B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.

To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1 G2 G3 G4 → G477 G478 G479 G480
0	1		G480 G479 G 478 G477 → G4 G3 G2 G1
1	0		G1 G3 → G477 G479 G2 G4 → G478 G480
1	1		G480 G478 → G4 G2 G479 G477 → G3 G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or

<table>
<tr><td></td><td>more than the number of lines necessary for the size of the liquid crystal panel.

<table>
<tr><th>NL[5:0]</th><th>LCD Driver Lines</th></tr>
<tr><td>6’h00 ~ 6’h3B</td><td>8*(NL[5:0]+1) lines</td></tr>
<tr><td>others</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="8">Default Value</th></tr>
<tr><th>RCM</th><th>RM</th><th>DM</th><th>PTS</th><th>GS</th><th>SS</th><th>SM</th><th>NL[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>6’h3b</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>6’h3b</td></tr>
</table></td></tr>
</table>

6.3.5 Entry Mode Set (B7h)

B7h	Entry Mode Set												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
1st Parameter	1	1	↑	XX	EPF[1:0]		0	0	0	GON	DTE	0	X

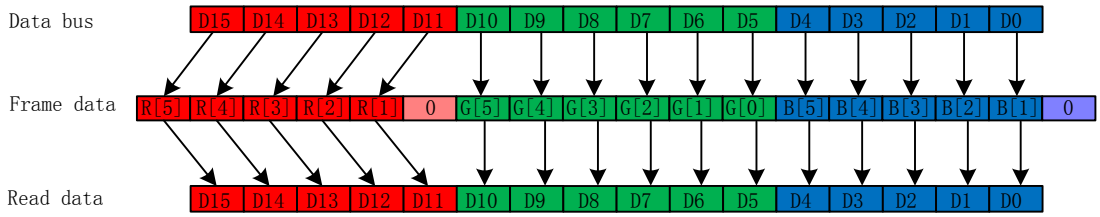
Description

GON/DTE: Set the output level of gate driver G1 ~ G480 as follows

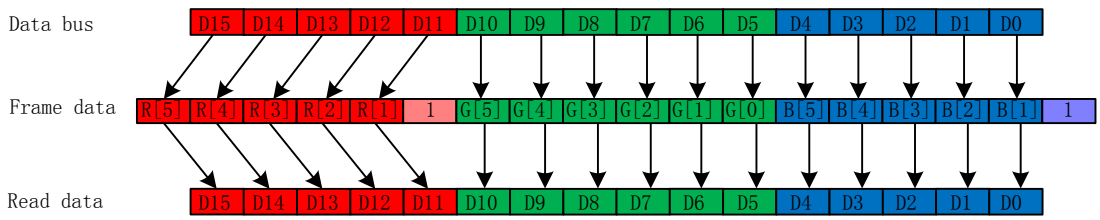
GON	DTE	G1~G480 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM

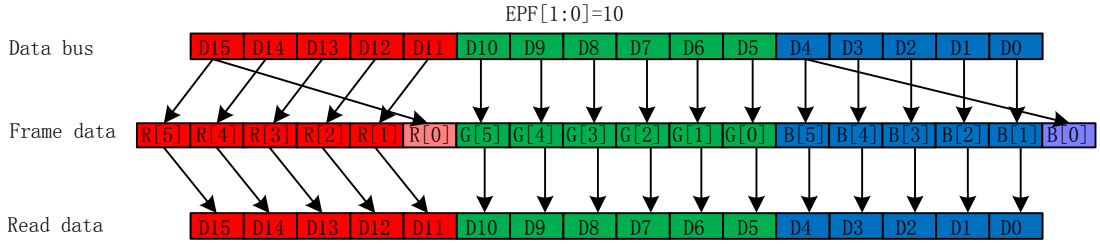
EPF[1:0]=00



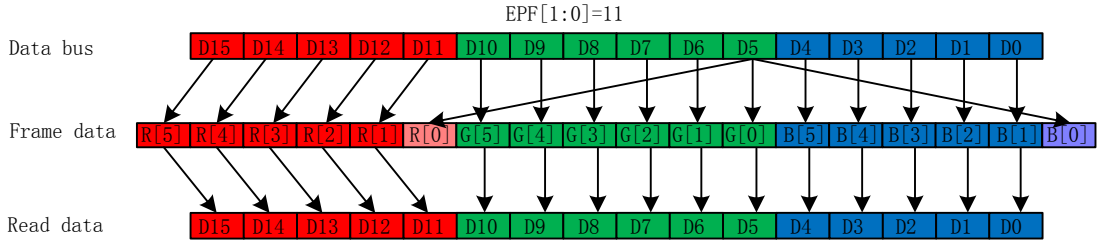
EPF[1:0]=01



EPF[1:0]=10



EPF[1:0]=11



<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>GON</th><th>DTE</th><th>EPF</th></tr>
<tr><td>Power On Sequence</td><td>1’b1</td><td>1’b1</td><td>2’b00</td></tr>
<tr><td>HW Reset</td><td>1’b1</td><td>1’b1</td><td>2’b00</td></tr>
</table>
</td></tr>
</table>

6.3.6 CABC Control 2 (C8h)

C8h	CABC Control 2												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	0	0	C8h
1st Parameter	1	1	1	XX	0	0	0	0	0	0	0	PWMPOL	00
Description	**PWMPOL:** The bit is used to define polarity of CABC_PWM signal.												
Restriction													
Register Availability													
Default													

BL	PWMPOL	CABC_PWM PIN
0	0	Always low
0	1	Always high
1	0	Original polarity of PWM signal
1	1	Inversed□polarity of PWM signal

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

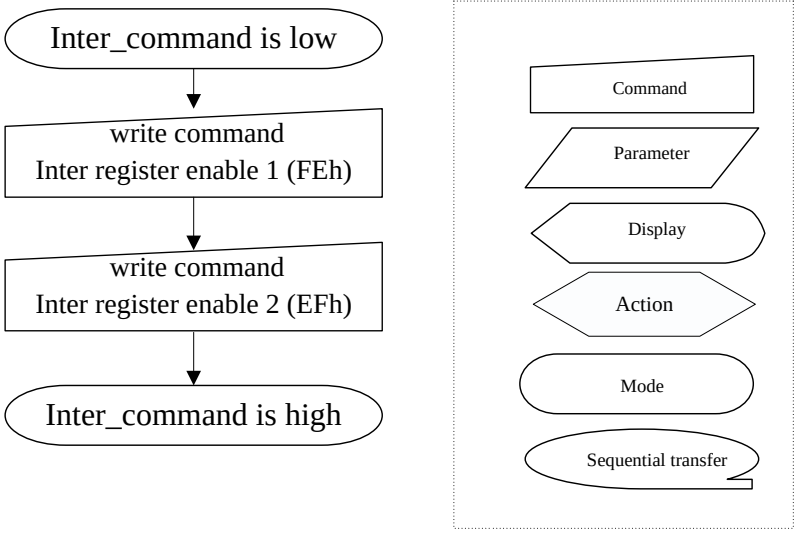
Status	Default Value		
	LEDONR	LENONPOL	PWMPOL
Power On Sequence	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

6.3.7 CABC Control 9 (CFh)

<table>
<tr><td>CFh</td><td colspan="13">CABC Control 3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>CFh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td colspan="8">PWM_DIV[7:0]</td><td>18</td></tr>
<tr><td>Description</td><td colspan="13">PWM_DIV [7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period can be calculated using the equation in the following.
$f_{PWM\_OUT} = \frac{18MHz}{(PWM\_DIV[7:0]+1)\ X\ 255}$
<table><tr><td colspan="8">PWM_DIV[7:0]</td><td rowspan="2">f_{PWM_OUT}</td></tr><tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70.58 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>35.29 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>23.53 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>17.64 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>14.11 KHz</td></tr><tr><td colspan="8">:
:</td><td>:
:</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>280.0 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>264.75.0 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>277.9 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>276.8 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>275.5 Hz</td></tr></table>Note : The output frequency tolerance of internal frequency divider in CABC is ± 10%</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’b00011000</td></tr><tr><td>HW Reset</td><td>8’b00011000</td></tr></table></td></tr>
</table>

6.4 Description of Level 3 Command

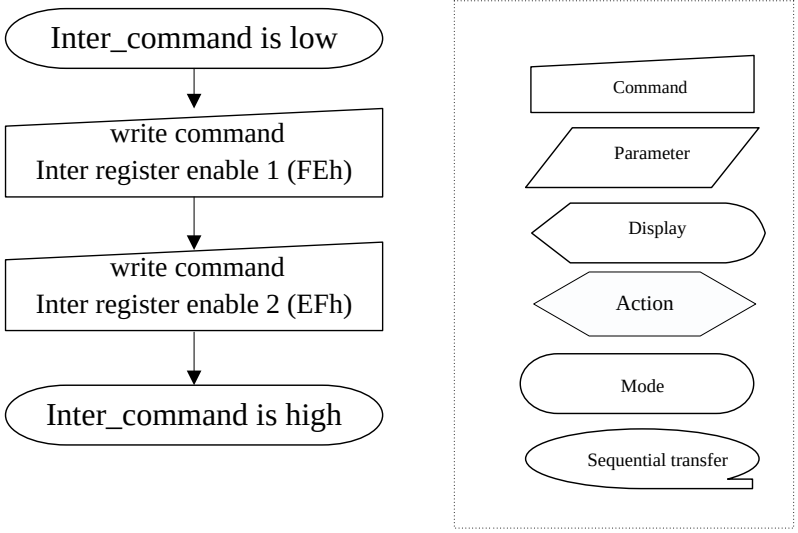
6.4.1 Inter register enable 1 (FEh)

FEh	Inter register enable 1												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.2 Inter register enable 2 (EFh)

EFh	Inter register enable 2												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.3 Frame Rate (A3h)

A3h	Frame Rate and Display Inversion Control												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	0	0	0	1	1	A3h
1st Parameter	1	1	↑	XX	0	0	0	0	RTN1[3:0]				02
2nd Parameter	1	1	↑	XX	RTN2[6:0]								17
Description	**RTN1[3:0]/RTN2[6:0] :**Set the frame rate when the internal resistor is used for oscillator circuit. Frame Rate = 36.44KHz/(96*RTN1+RTN2+288)												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	RTN1[3:0]	RTN2[6:0]
Power On Sequence	4'b0002	7'h17
SW Reset	4'b0002	7'h17
HW Reset	4'b0002	7'h17

6.4.4 Power control 1 (A4h)

<table>
<tr><td>A4h</td><td colspan="13">Power control 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>A4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>VCIRE</td><td colspan="5">VRH1[4:0]</td><td>1D</td></tr>
<tr><td>Description</td><td colspan="13">
VCIRE: Select the external reference voltage VCI or internal reference voltage VCIRE.
<table>
<tr><td>VCIRE=0</td><td>Internal reference voltage 2.5V (default)</td></tr>
<tr><td>VCIRE =1</td><td>External reference voltage VCI</td></tr>
</table>
VRH1[4:0] Set the voltage level value to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.
<table>
<tr><th>VRH1[4:0]</th><th>VREG1OUT</th><th>VRH1[4:0]</th><th>VREG1OUT</th></tr>
<tr><td>5’h00</td><td>0</td><td>5’h10</td><td>4.567</td></tr>
<tr><td>5’h01</td><td>3.629</td><td>5’h11</td><td>4.630</td></tr>
<tr><td>5’h02</td><td>3.692</td><td>5’h12</td><td>4.693</td></tr>
<tr><td>5’h03</td><td>3.754</td><td>5’h13</td><td>4.755</td></tr>
<tr><td>5’h04</td><td>3.817</td><td>5’h14</td><td>4.818</td></tr>
<tr><td>5’h05</td><td>3.879</td><td>5’h15</td><td>4.880</td></tr>
<tr><td>5’h06</td><td>3.942</td><td>5’h16</td><td>4.943</td></tr>
<tr><td>5’h07</td><td>4.004</td><td>5’h17</td><td>5.005</td></tr>
<tr><td>5’h08</td><td>4.067</td><td>5’h18</td><td>5.068</td></tr>
<tr><td>5’h09</td><td>4.130</td><td>5’h19</td><td>5.131</td></tr>
<tr><td>5’h0a</td><td>4.192</td><td>5’h1A</td><td>5.193</td></tr>
<tr><td>5’h0b</td><td>4.255</td><td>5’h1B</td><td>5.256</td></tr>
<tr><td>5’h0c</td><td>4.317</td><td>5’h1C</td><td>5.318</td></tr>
<tr><td>5’h0d</td><td>4.380</td><td>5’h1D</td><td>5.381</td></tr>
<tr><td>5’h0e</td><td>4.442</td><td>5’h1E</td><td>5.443</td></tr>
<tr><td>5’h0f</td><td>4.505</td><td>5’h1F</td><td>5.506</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>VCIRE</th><th>VRH1[4:0]</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td><td>5’h1D</td></tr>
<tr><td>SW Reset</td><td>1’b0</td><td>5’h1D</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>5’h1D</td></tr>
</table>
</td></tr>
</table>

6.4.5 Power control 2 (A5h)

<table>
<tr><td>A5h</td><td colspan="13">Power control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D23-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>A5h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td colspan="5">VRH2[4:0]</td><td>1F</td></tr>
<tr><td>Description</td><td colspan="13">VRH2[4:0] Set the voltage level value to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.
<table>
<tr><th>VRH2[4:0]</th><th>VREG2OUT</th><th>VRH2[4:0]</th><th>VREG1OUT</th></tr>
<tr><td>5’h00</td><td>0</td><td>5’h10</td><td>-4.567</td></tr>
<tr><td>5’h01</td><td>-3.629</td><td>5’h11</td><td>-4.630</td></tr>
<tr><td>5’h02</td><td>-3.692</td><td>5’h12</td><td>-4.693</td></tr>
<tr><td>5’h03</td><td>-3.754</td><td>5’h13</td><td>-4.755</td></tr>
<tr><td>5’h04</td><td>-3.817</td><td>5’h14</td><td>-4.818</td></tr>
<tr><td>5’h05</td><td>-3.879</td><td>5’h15</td><td>-4.880</td></tr>
<tr><td>5’h06</td><td>-3.942</td><td>5’h16</td><td>-4.943</td></tr>
<tr><td>5’h07</td><td>-4.004</td><td>5’h17</td><td>-5.005</td></tr>
<tr><td>5’h08</td><td>-4.067</td><td>5’h18</td><td>-5.068</td></tr>
<tr><td>5’h09</td><td>-4.130</td><td>5’h19</td><td>-5.131</td></tr>
<tr><td>5’h0a</td><td>-4.192</td><td>5’h1A</td><td>-5.193</td></tr>
<tr><td>5’h0b</td><td>-4.255</td><td>5’h1B</td><td>-5.256</td></tr>
<tr><td>5’h0c</td><td>-4.317</td><td>5’h1C</td><td>-5.318</td></tr>
<tr><td>5’h0d</td><td>-4.380</td><td>5’h1D</td><td>-5.381</td></tr>
<tr><td>5’h0e</td><td>-4.442</td><td>5’h1E</td><td>-5.443</td></tr>
<tr><td>5’h0f</td><td>-4.505</td><td>5’h1F</td><td>-5.506</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VRH2[4:0]</th></tr>
<tr><td>Power On Sequence</td><td>5’h1F</td></tr>
<tr><td>SW Reset</td><td>5’h1F</td></tr>
<tr><td>HW Reset</td><td>5’h1F</td></tr>
</table></td></tr>
</table>

6.4.6 Power Control 3 (EDh)

EDh	Power control 2												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	0	1	EDh
1st Parameter	1	1	↑	XX	0	dc1[2:0]			0	dc0[2:0]			55
2nd Parameter	1	1	↑	XX	0	dc3[2:0]			0	dc2[2:0]			55

Description

DC0 [2:0]: Selects the operating frequency of the ddvdh_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1 [2:0]: Selects the operating frequency of the ddvdl_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC2 [2:0]: Selects the operating frequency of the vcl_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC3 [2:0]: Selects the operating frequency of the vgh_vgl_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC0 [3:0]	ddvdh_clk frequency	DC1 [3:0]	ddvdl_clk frequency
3'h0	Fosc/8	3'h0	Fosc/8
3'h1	Fosc/16	3'h1	Fosc/16
3'h2	Fosc/32	3'h2	Fosc/32
3'h3	Fosc/64	3'h3	Fosc/64
3'h4	Fosc/428	3'h4	Fosc/428
3'h5	Fosc/256	3'h5	Fosc/256
3'h6	Fosc/512	3'h6	Fosc/512
3'h7	Fosc/1024	3'h7	Fosc/1024
DC2 [3:0]	vcl_clk frequency	DC3 [3:0]	vgh_vgl_clk frequency
3'h0	Fosc/8	3'h0	Fosc/64
3'h1	Fosc/16	3'h1	Fosc/128
3'h2	Fosc/32	3'h2	Fosc/256
3'h3	Fosc/64	3'h3	Fosc/512

	3'h4	Fosc/428	3'h4	Fosc/1024
	3'h5	Fosc/256	3'h5	Fosc/2048
	3'h6	Fosc/512	3'h6	Fosc/4096
	3'h7	Fosc/1024	3'h7	Fosc/8192

Restriction	Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	DC0	DC1	DC2	DC3
Power On Sequence	3'h5	3'h5	3'h5	3'h5
SW Reset	3'h5	3'h5	3'h5	3'h5
HW Reset	3'h5	3'h5	3'h5	3'h5

6.4.7 VCOM Control (E5h)

E5h	Power control 2												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	1	0	1	E5h
1st Parameter	1	1	↑	XX	VCM[7:0]								20

Description

VCM_REG [7:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.

VCM[7:0]	VCOM	VCM[7:0]	VCOM	VCM[7:0]	VCOM
8'h00	-2.00241	8'h2b	-1.32973	8'h56	-0.6704
8'h01	-1.98677	8'h2c	-1.31408	8'h57	-0.6414
8'h02	-1.97112	8'h2d	-1.29844	8'h58	-0.62575
8'h03	-1.95548	8'h2e	-1.28264	8'h59	-0.61011
8'h04	-1.93984	8'h2f	-1.26715	8'h5a	-0.59447
8'h05	-1.92419	8'h30	-1.25151	8'h5b	-0.57882
8'h06	-1.90855	8'h31	-1.23586	8'h5c	-0.56318
8'h07	-1.8929	8'h32	-1.22022	8'h5d	-0.54753
8'h08	-1.87726	8'h33	-1.20458	8'h5e	-0.53189
8'h09	-1.86162	8'h34	-1.18893	8'h5f	-0.51625
8'h0a	-1.84597	8'h35	-1.17329	8'h60	-0.5006
8'h0b	-1.83033	8'h36	-1.15764	8'h61	-0.48496
8'h0c	-1.81468	8'h37	-1.142	8'h62	-0.46932
8'h0d	-1.79904	8'h38	-1.12636	8'h63	-0.45367
8'h0e	-1.7834	8'h39	-1.11071	8'h64	-0.43803
8'h0f	-1.76775	8'h3a	-1.09507	8'h65	-0.42238
8'h10	-1.75211	8'h3b	-1.07942	8'h66	-0.40674
8'h11	-1.73647	8'h3c	-1.06378	8'h67	-0.3911
8'h12	-1.72082	8'h3d	-1.04814	8'h68	-0.37545
8'h13	-1.70518	8'h3e	-1.03249	8'h69	-0.35981
8'h14	-1.68953	8'h3f	-1.01685	8'h6a	-0.34416
8'h15	-1.67389	8'h40	-1.00121	8'h6b	-0.32852
8'h16	-1.65825	8'h41	-0.98556	8'h6c	-0.31288
8'h17	-1.6426	8'h42	-0.96992	8'h6d	-0.29723
8'h18	-1.62696	8'h43	-0.95427	8'h6e	-0.28159
8'h19	-1.61132	8'h44	-0.93863	8'h6f	-0.26595
8'h1a	-1.59567	8'h45	-0.92299	8'h70	-0.2503
8'h1b	-1.58003	8'h46	-0.90734	8'h71	-0.23466
8'h1c	-1.56438	8'h47	-0.8917	8'h72	-0.21901
8'h1d	-1.54874	8'h48	-0.87605	8'h73	-0.20337
8'h1e	-1.5331	8'h49	-0.86041	8'h74	-0.18773

	8’h1f	-1.51745	8’h4a	-0.84477	8’h75	-0.17208
	8’h20	-1.50181	8’h4b	-0.82912	8’h76	-0.15644
	8’h21	-1.48616	8’h4c	-0.81348	8’h77	-0.14079
	8’h22	-1.47052	8’h4d	-0.79784	8’h78	-0.12515
	8’h23	-1.45488	8’h4e	-0.78219	8’h79	-0.10951
	8’h24	-1.43923	8’h4f	-0.76655	8’h7a	-0.09386
	8’h25	-1.42359	8’h50	-0.7509	8’h7b	-0.07822
	8’h26	-1.40795	8’h51	-0.73526	8’h7c	-0.06258
	8’h27	-1.3923	8’h52	-0.71962	8’h7d	-0.04693
	8’h28	-1.37666	8’h53	-0.70397	8’h7e	-0.03129
	8’h29	-1.36101	8’h54	-0.68833	8’h7f	-0.01564
	8’h2a	-1.34537	8’h55	-0.67268	8’h80~8’hff	inhibit

Restriction	Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.4.8 SET_GAMMA1 (positive gamma control)(F0h)

F0h	SET_GAMMA1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
1st Parameter	1	1	↑	XX					VP0[3:0]				0F
2nd Parameter	1	1	↑	XX			VP1[5:0]						3F
3rd Parameter	1	1	↑	XX			VP2[5:0]						3F
4th Parameter	1	1	↑	XX					VP4[3:0]				0F
5th Parameter	1	1	↑	XX				VP6[4:0]					1A
6th Parameter	1	1	↑	XX					VP13[3:0]				0F
7th Parameter	1	1	↑	XX		VP20[6:0]							5A
8th Parameter	1	1	↑	XX	VP30[3:0]				VP27[3:0]				64
9th Parameter	1	1	↑	XX		VP43[6:0]							30
10th Parameter	1	1	↑	XX					VP50[3:0]				0A
11th Parameter	1	1	↑	XX				VP57[4:0]					15
12th Parameter	1	1	↑	XX					VP59[3:0]				05
13th Parameter	1	1	↑	XX			VP61[5:0]						19
14th Parameter	1	1	↑	XX			VP62[5:0]						19
15th Parameter	1	1	↑	XX					VP63[3:0]				02
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

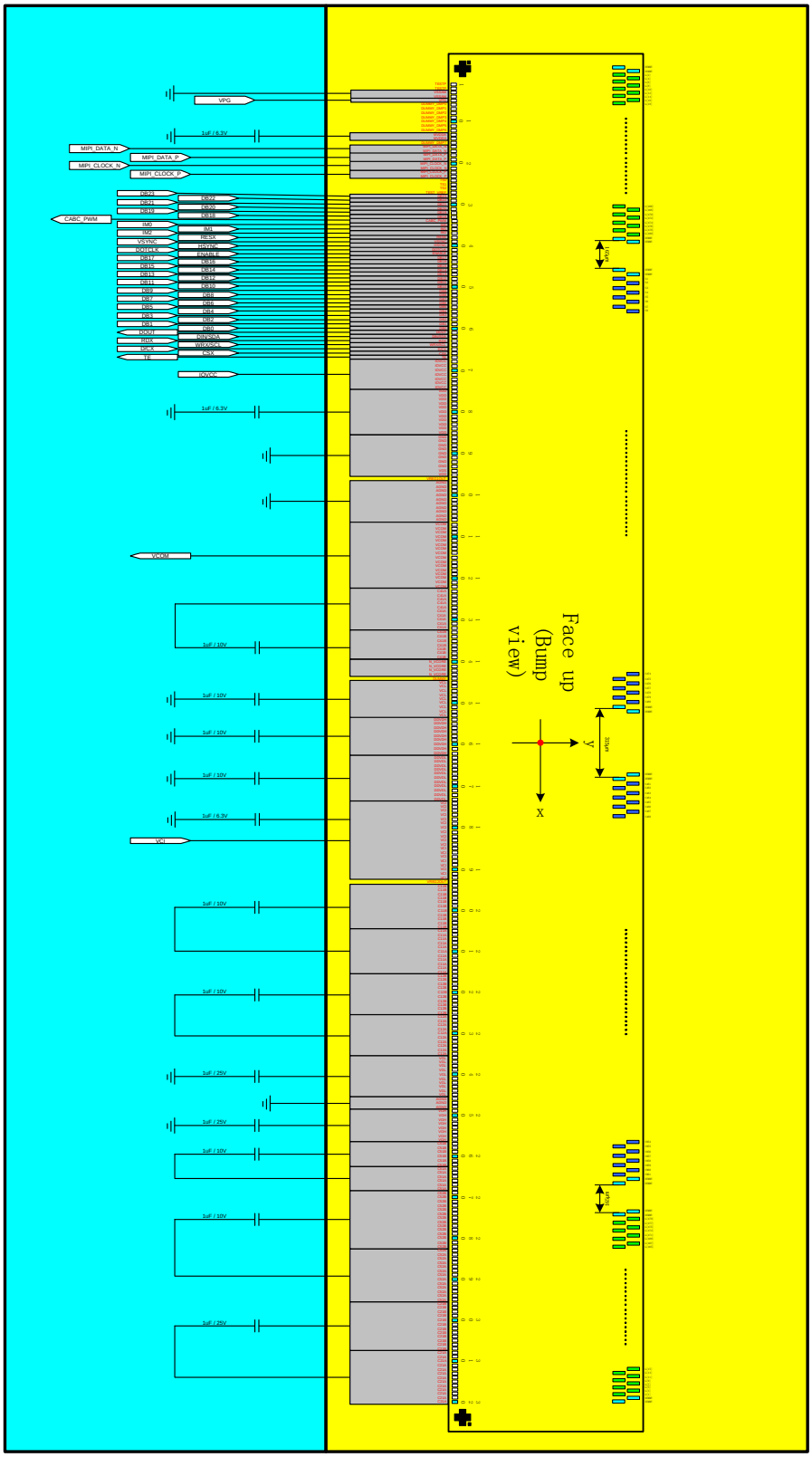
6.4.9 SET_GAMMA2 (negative gamma control) (F1h)

F1h	SET_GAMMA1												
	D/CX	RDX	WRX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	1	F1 h
1st Parameter	1	1	↑	XX					VN0[3:0]				0F
2nd Parameter	1	1	↑	XX			VN1[5:0]						3F
3rd Parameter	1	1	↑	XX			VN2[5:0]						2F
4th Parameter	1	1	↑	XX					VN4[3:0]				0F
5th Parameter	1	1	↑	XX				VN6[4:0]					15
6th Parameter	1	1	↑	XX					VN13[3:0]				0B
7th Parameter	1	1	↑	XX		VN20[6:0]							3A
8th Parameter	1	1	↑	XX	VN30[3:0]				VN27[3:0]				87
9th Parameter	1	1	↑	XX		VN43[6:0]							2F
10th Parameter	1	1	↑	XX					VN50[3:0]				0A
11th Parameter	1	1	↑	XX				VN57[4:0]					15
12th Parameter	1	1	↑	XX					VN59[3:0]				0F
13th Parameter	1	1	↑	XX			VN61[5:0]						1E
14th Parameter	1	1	↑	XX			VN62[5:0]						18
15th Parameter	1	1	↑	XX					VN63[3:0]				02
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

7 Application



Items	Recommended Specification	Pin connection
Capacity 1uF (B characteristics)	6.3V	VDD,MVDDA,VCI
	10V	C41A/B,C11A/B,C12A/B,C51A/B,C52A/B, VCL,DDVDL,DDVDH,
	25V	VGH,VGL,C21A/B

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9403 is used out of the absolute maximum ratings, GC9403 may be permanently damaged. To use GC9403 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9403 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Supply voltage(Digital)	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	℃	-40~+85
Storage temperature	Tstg	℃	-55~+110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2 DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State code	Line DC voltage levels	
	CLOCK_P or DATA_N	CLOCK_N or DATA_P
HS-0	Low(HS)	High(HS)
HS-1	High (HS)	Low (HS)
LP-00	Low(LP)	Low(LP)
LP-01	Low(LP)	High(LP)
LP-10	High(LP)	Low(LP)
LP-11	High(LP)	High(LP)

Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

8.2.1 DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MCU interface.

parameter	symbol	condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA ;Note 2	0.8IOVCC	-	IOVCC	V
Logic Low level output voltage	V_{OL}	I_{OUT}=-1mA ; Note 2	0.0	-	0.2 IOVCC	V
Logic High level input voltage	V_{IHLPCD}	LP-CD ; Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD ; Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLOCK, DATA) ; Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLOCK, DATA) ; Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLOCK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (DATA), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (DATA), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note: (1) Ta=-30℃ to 70℃ (to +85℃ no damage)
(2) PWM_OUT, TE
(3) DSI High Speed mode is off

8.2.2 DC characteristics for DSI HS mode

DC levels of the HS-0 and HS-0 are defined on table below: DC Characteristics for DSI HS mode.

parameter	symbol	condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLOCK_P/N ; Note 2,3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-DATA_P/N ; Note 2,3	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLOCK_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-DATA_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLOCK_P/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-DATA_P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLOCK_P/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-DATA_P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLOCK_P/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-DATA_P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	14	pF

Note: (1) Ta = -30 to 70 °C (to +85 °C no damage), IOVCC = 1.65 to 1.95V, GND = 0V

(2) Includes 50mV (-50mV to 50mV) ground difference

(3) Without $V_{CMRCLKM450}$/$V_{CMRDATAM450}$

(4) Without 50mV (-50mV to 50mV) ground difference

8.2.3 DC Characteristics for Panel Driving

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDD	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	DGND	-	0.2*IOVCC	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or DGND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM Amplitude Voltage	VCOM	V		0	-	-2	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	AVDD -0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3

Output Deviation Voltage(Source Output channel)	Vdev	mV	Sout>=4.2V Sout<=0.8V	-	-	20	Note4
			4.2V>Sout>0.8V	-	-	15	-
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation							
1st Boost（VDD*2) Voltage	AVDD	V	-	4.95 (Note5)	-	5.5 (Note6)	Note3
1st Booster（VDD*2) Drop Voltage	VDD*2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	AVDD -0.2	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

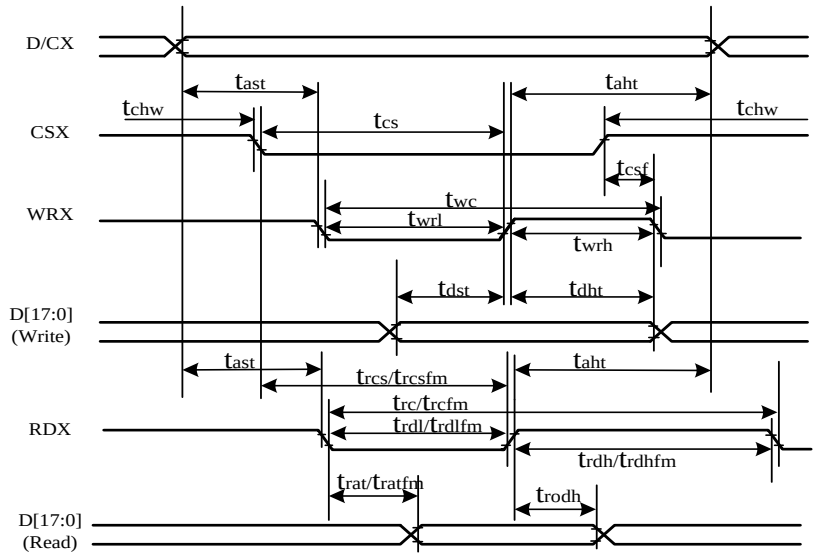
Note5: VCI=2.6V

Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

8.3 AC Characteristics

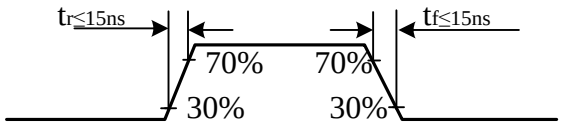
8.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080)



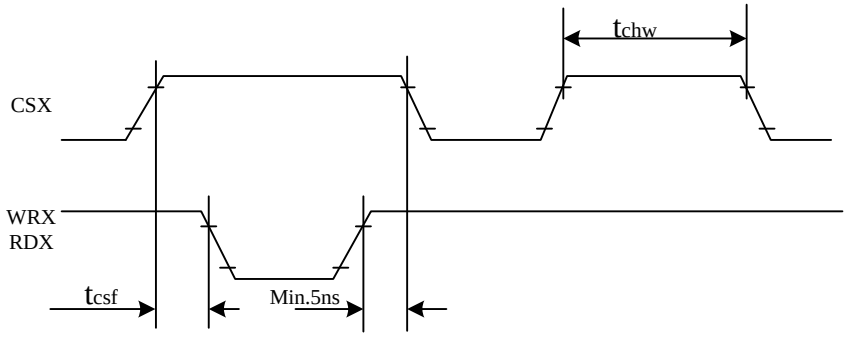
Signal	Symbol	Parameter	max	min	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	45	-	ns	
D[17:0],D[15:0],D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	

	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

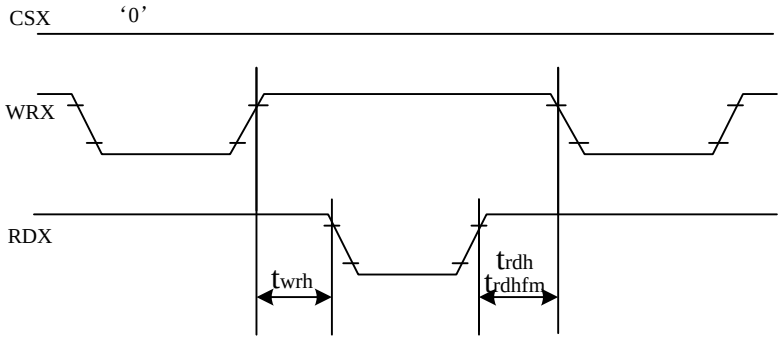


CSX timings :



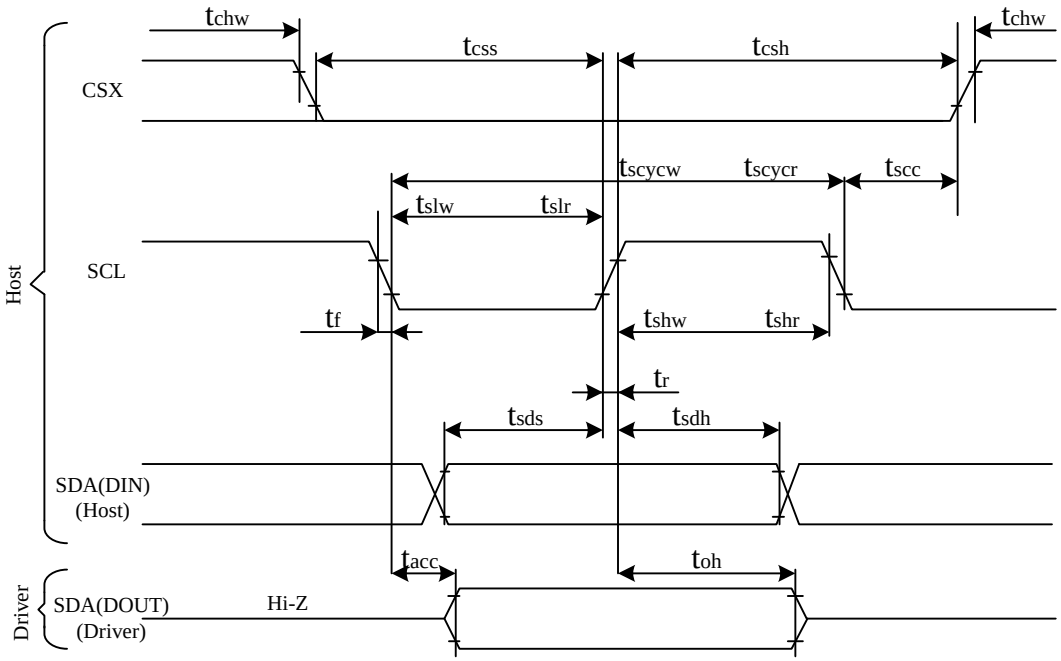
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



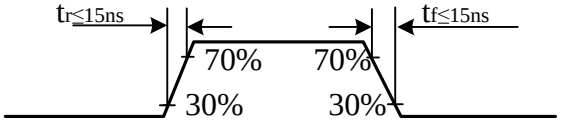
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

8.3.2 Display Serial Interface Timing Characteristics (3-line SPI system)

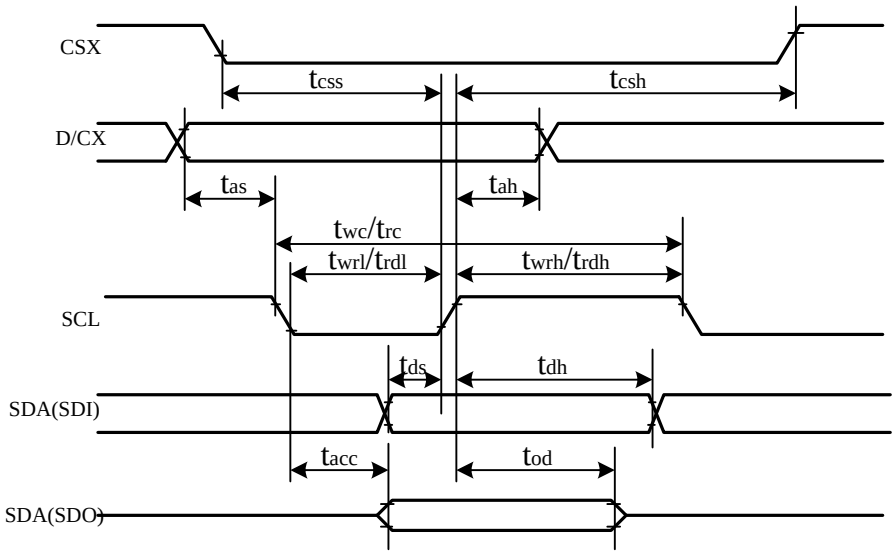


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

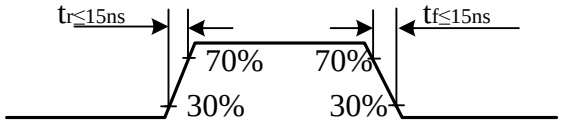


8.3.3 Display Serial Interface Timing Characteristics (4-line SPI system)

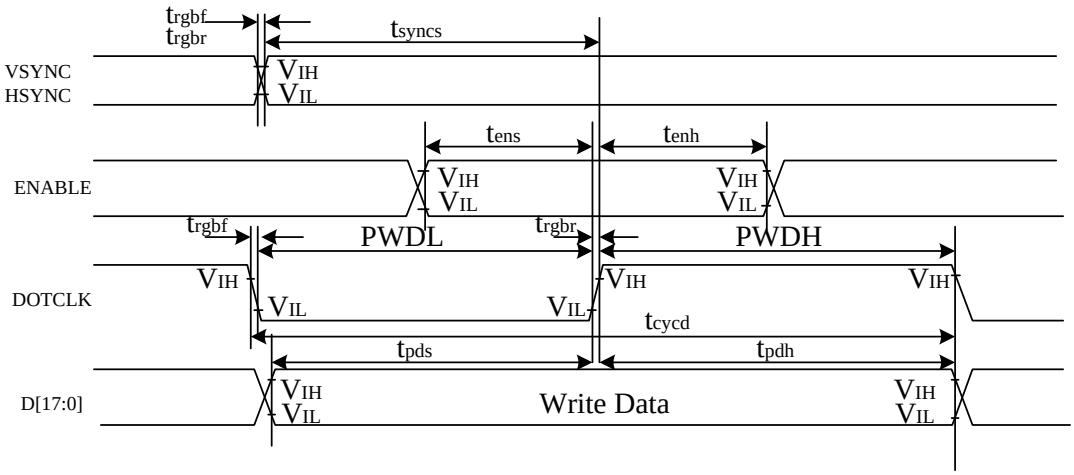


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	100	-	ns	
	twrh	SCL "H" Pulse Width (Write)	40	-	ns	
	twrl	SCL "L" Pulse Width (Write)	40	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	toh	Output disable time (Read)	10	50	ns	For minmum CL=8pF

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

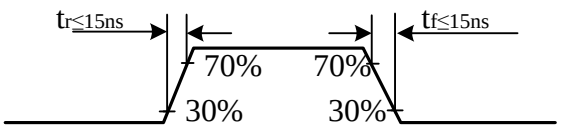


8.3.4 Parallel 18/16/6-bit RGB Interface Timing Characteristics



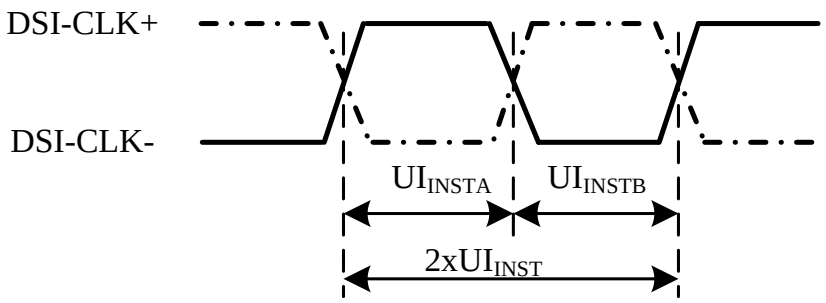
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



8.3.5 MIPI

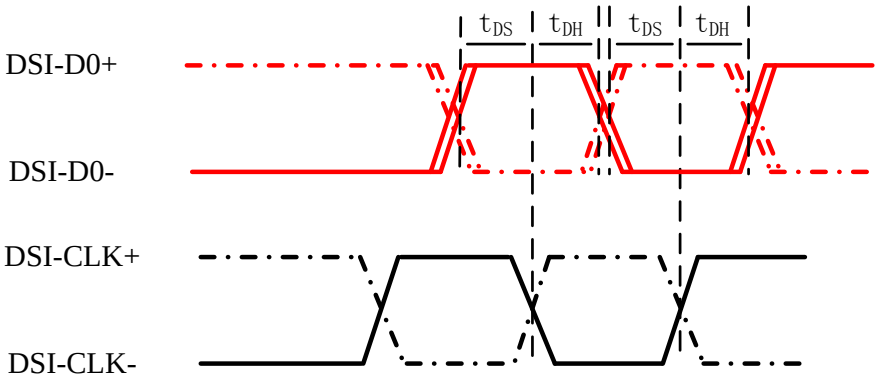
8.3.5.1 High Speed Mode – Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI_CLOCK_P/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI_CLOCK_P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	2	12.5	ns

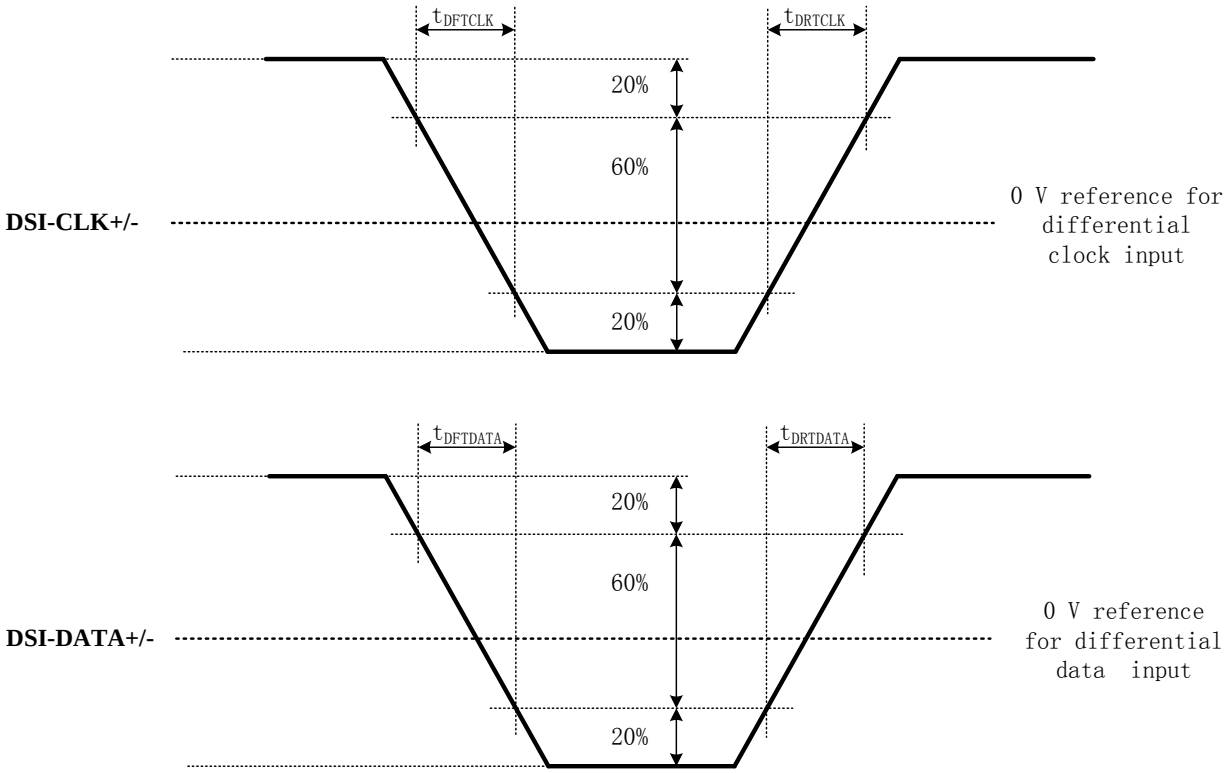
Note: UI = UI_{INSTA} = UI_{INSTB}

8.3.5.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI-DATA_P/N	t_{DH}	Clock to Data Hold Time	300	-	ps
DSI-DATA_P/N	t_{DS}	Data to Clock Setup time	300	-	ps

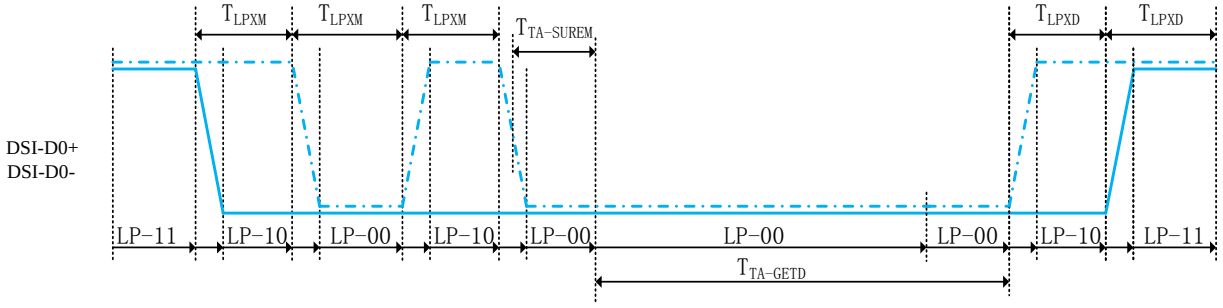
8.3.5.3 High Speed Mode – Rise and Fall Timings



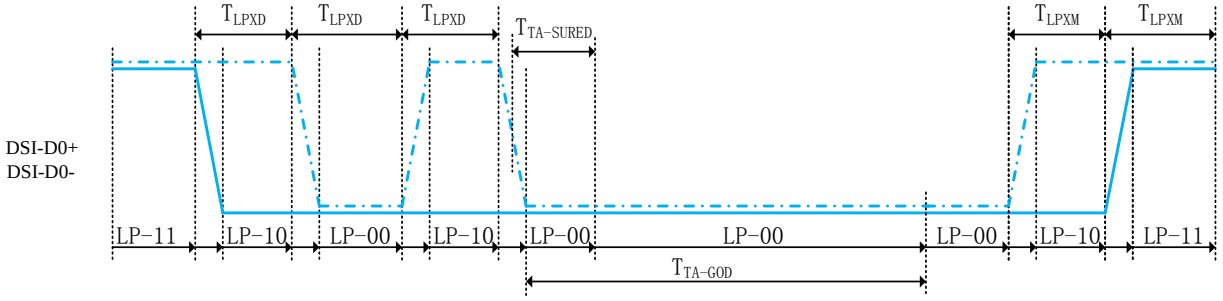
Signal	Symbol	Condition	specification			Unit
			Min	Max	Type	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLOCK_P/N	-	-	900	Ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-DATA_P/N	-	-	900	ps

8.3.5.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the GC9403sequence below.



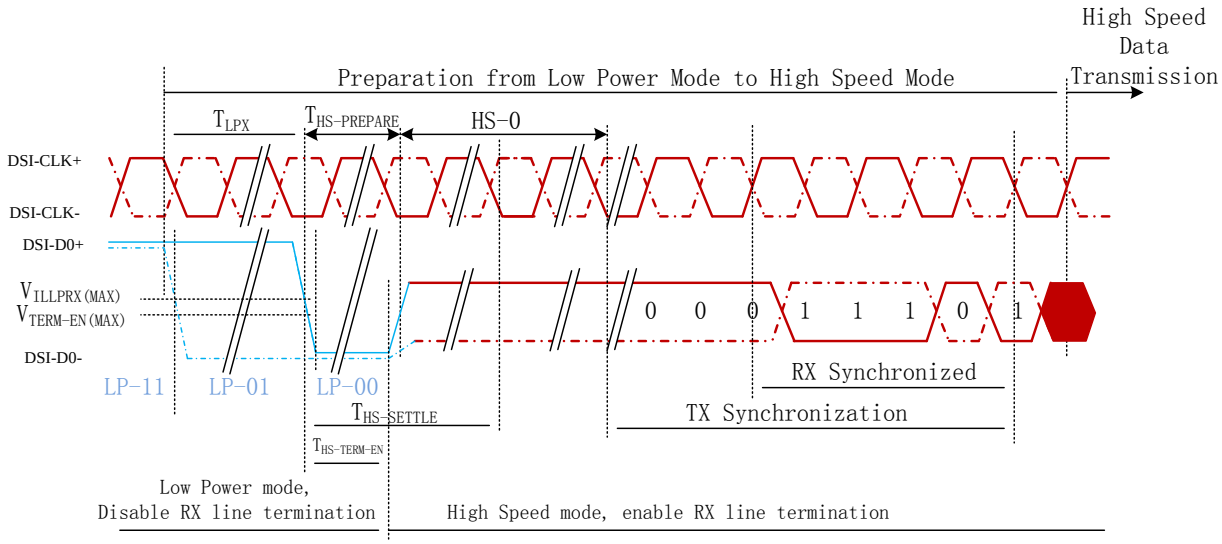
Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from GC9403to the MCU sequence below.



Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → GC9403	50	-	ns
Input (DSI-DATA_P/N)	$T_{TA-SUREM}$	Time-out before the GC9403starts driving	T_{LPXM}	$2xT_{LPXM}$	ns
Output (DSI-DATA_P/N)	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods GC9403→ MCU	50	75	ns
Output (DSI-DATA_P/N)	$T_{TA-SURED}$	Time-out before the MCU starts driving	T_{LPXD}	$2xT_{LPXD}$	

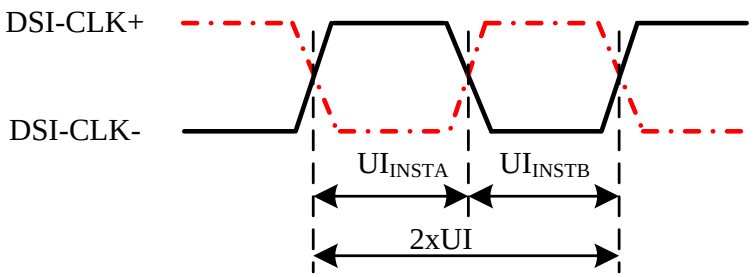
Signal	Symbol	Description	Time	Unit
Input (DSI-DATA_P/N)	$T_{TA-GETD}$	Time to drive LP-00 by GC9403	$5xT_{LPXD}$	ns
Output (DSI-DATA_P/N)	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

8.3.5.5 Data Lanes from Low Power Mode to High Speed Mode

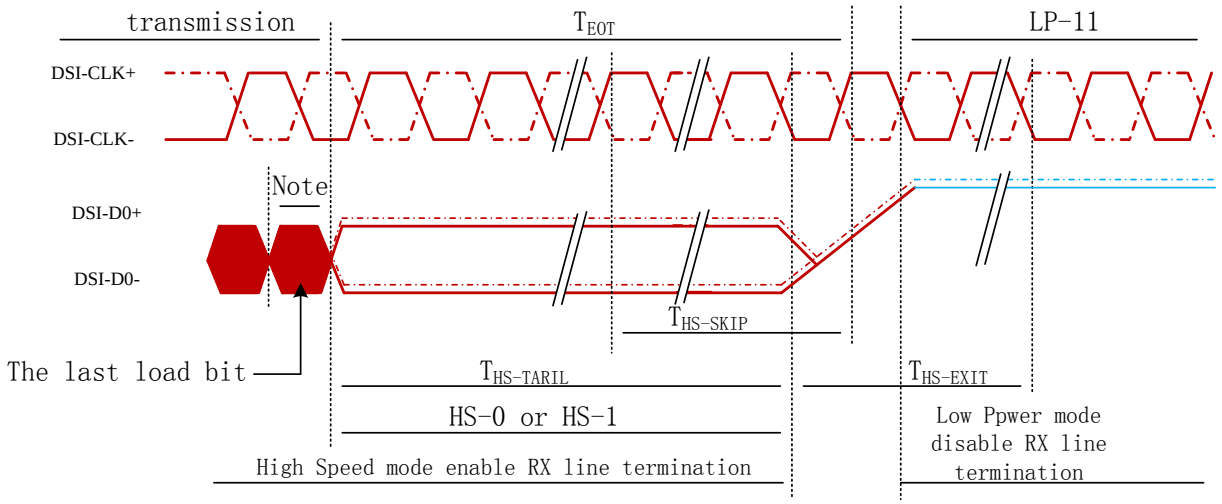


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPX}	Length of any low power state period	50	-	ns
Input (DSI-DATA_P/N)	$T_{HS-PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
Input (DSI-DATA_P/N)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses V_{ILMAX}	-	35+4xUI	ns

Note: UI definition: UI = UI_{INSTA} = UI_{INSTB}



8.3.5.6 Data Lanes from High Speed Mode to Low Power Mode



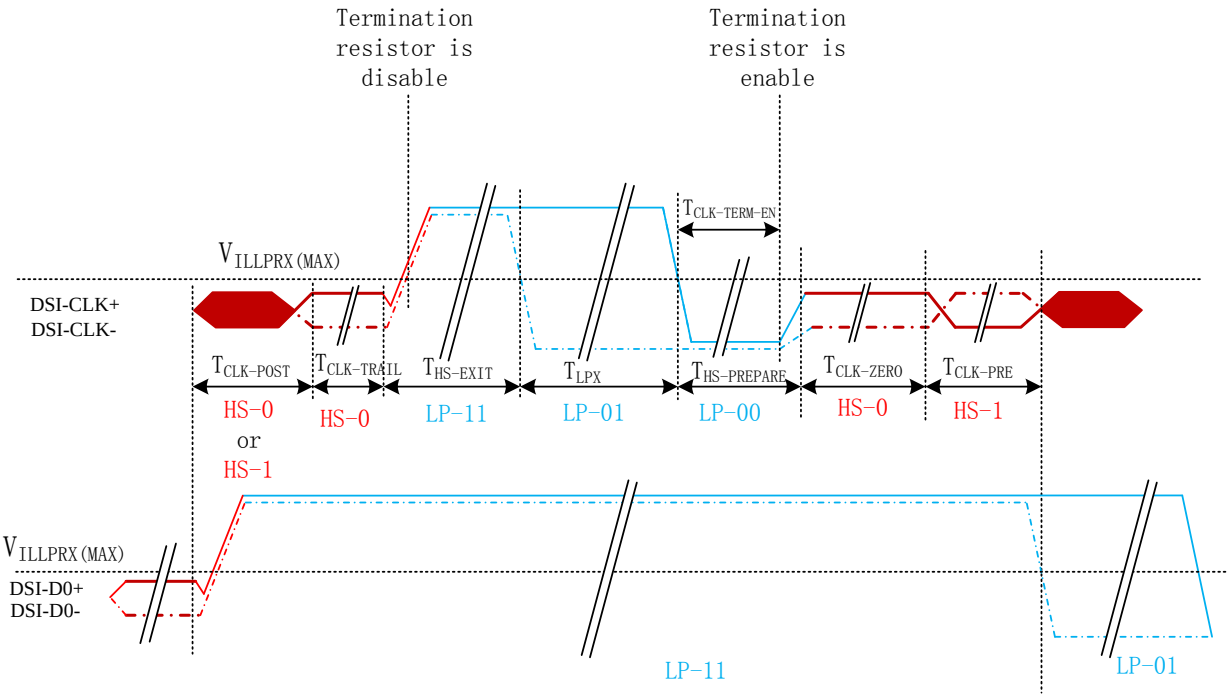
Note:

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

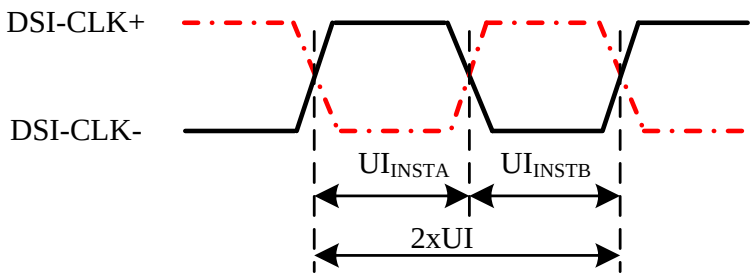
Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{TA-SKIP}$	Time-out at GC9403to Ignore Transition Period of EoT	40	4xUI	ns
Output (DSI-DATA_P/N)	$T_{TA-EXIT}$	Time to Driver LP-11 after HS burst	100	-	ns

8.3.5.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode



Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
Input (DSI-DATA_P/N)	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (DSI-DATA_P/N)	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
Input (DSI-DATA_P/N)	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	
Input (DSI-DATA_P/N)	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	38	-	
Input (DSI-DATA_P/N)	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300		
Input (DSI-DATA_P/N)	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI		

Note: UI definition: UI = UI_{INSTA} = UI_{INSTB}


DSI-CLK+
DSI-CLK-
UIINSTA
UIINSTB
2xUI

9 Revision History

Version No.	Date	Page	Description
V1.00	2014-01-20	All	By Garrote
V1.00	2014-02-12	All	By Jackpop
V1.00	2014-02-18	All	By Lee