

# BAT6

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Solar Panel Emulator

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## **Abstract**

Emulating solar modules in a laboratory environment currently requires expensive and complex equipment, hindering development of new solar power products. To facilitate research into this area, a low-cost solution for emulating solar modules is required.

This report details our efforts in designing and constructing a device for this purpose. We developed a model for describing solar module behavior mathematically, allowing both single-celled panels as well as more complex multi-celled panel configurations to be described. A microcontroller and a voltage converter constitute the hardware design. The microcontroller is responsible for interacting with the outside world, while the converter's purpose is to use the mathematical model to generate the desired voltages and currents on the device's output.

At this point, the interface and most of the circuitry works as intended. Unfortunately, due to a design error, our circuit overloads the voltage converter, causing irreparable damage. Based on measurements and simulations, we consider the likely cause to be overlong connections between the converter and other components. The next step in finalising the device would be to design a new circuit board for fixing this issue.

# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
<b>2</b>	<b>Basic Concept</b>	<b>2</b>
2.1	The Model . . . . .	2
2.2	Implementation of Regulation . . . . .	3
2.3	Hardware . . . . .	4
<b>3</b>	<b>Component Selection</b>	<b>4</b>
3.1	Microcontroller . . . . .	4
3.2	36V Power Supply and Mains Input . . . . .	4
3.3	Voltage Rails . . . . .	4
3.4	LT3741 . . . . .	5
<b>4</b>	<b>PCB Design</b>	<b>11</b>
<b>5</b>	<b>Software</b>	<b>12</b>
5.1	Firmware . . . . .	12
5.2	Front-End . . . . .	12
<b>6</b>	<b>Verification</b>	<b>13</b>
6.1	Test Fixtures . . . . .	13
6.2	Measurement Results . . . . .	16
6.3	Analysis of the Issue . . . . .	16
6.4	Simulating the Issue . . . . .	16
<b>7</b>	<b>Conclusions</b>	<b>18</b>
<b>Appendix A</b>	<b>Specifications</b>	<b>19</b>
<b>Appendix B</b>	<b>LT3471 Circuit</b>	<b>21</b>
<b>Appendix C</b>	<b>List of Components</b>	<b>22</b>
<b>Appendix D</b>	<b>Circuit Schematics</b>	<b>25</b>
<b>Appendix E</b>	<b>Inductors</b>	<b>31</b>
<b>Appendix F</b>	<b>MOSFETs</b>	<b>31</b>
<b>Bibliography</b>		<b>32</b>

## 1 Introduction

Verifying the correct operation of equipment used for testing solar arrays is currently difficult in a controlled laboratory environment, as no affordable solutions for this exist on the open market. To address this issue, the aim of this project was the development of a device capable of emulating the behavior of a photovoltaic module. With this device, test equipment for photovoltaic modules can be verified to function as specified in a laboratory conveniently and affordably.

The primary characteristics of our device should be compactness (usable in a standard laboratory environment), the capability to emulate varying solar irradiation levels, being able to be used in series with other emulators, efficiency with regards to power consumption and losses, and to emulate the characteristic curve of an actual PV module. A more detailed list of the technical requirements can be found in the specifications (see appendix A on page 19f)

A microcontroller and a constant-current, constant-voltage step-down converter constitute the core of our device. The microcontroller performs IO operations and implements the regulation loop used to control the step-down converter, whereas the step-down converter generates the output voltage and output current corresponding to the desired operating point from a DC power supply. The entire design is based around a custom PCB, enabling us to optimise impedances of connections between critical components. Additionally, we can get very close in behavior to a potentially mass-produced product since trace lengths, routing and component placement are crucial (see also section 6, beginning on page 13).

The device has a simple yet powerful user interface which can be controlled by a push-twist button and a modern OLED display. The device can also be remotely monitored and controlled from a PC via USB interface and custom software built on the Qt application framework and is compatible with all major operating systems [10]. Our device can emulate fairly complex configurations of cells thanks to an efficient use of computation resources and its powerful microprocessor.

Section 2 (p. 2ff) of this report deal with the basic concept behind our solution. Component selection and PCB design are documented in sections 3 (p. 4ff) and 4 (p. 11ff), respectively, while section 5 is concerned with software (p. 12ff). Section 6 (p. 13ff) deals with testing the device and our error analysis. Lastly, the conclusion can be found in section 7 on page 18.

## 2 Basic Concept

This section primarily deals with the underlying mathematics used to model the various configurations of solar cells the device needs to be able to emulate. Additionally, it presents a brief overview of the hardware.

### 2.1 The Model

The aim in developing our model was to find the sweet spot between usability and accuracy. It should have a small, comprehensive set of parameters which can be easily understood by the user, while still representing the actual physics accurately enough to yield good results.

#### 2.1.1 Single Solar Cell

The single diode model of the ideal PV cell [11] serves as a basis for our model. The I-V characteristic of this model can be expressed with equation 1, whereby  $I_{pv}$  is the generated current,  $I_o$  is the diode current and  $V_T$  is the thermal voltage.

Although these three parameters depend on the junction temperature, the inclusion of the junction temperature into our model as a parameter would only contribute a minor correction factor, negligible for our purposes. For this reason we can simplify our model if we assume that the temperature is equal to the nominal temperature  $T_n = 298.15K$ . The thermal voltage is defined in equation 2, whereby  $T$  is the junction temperature,  $k$  is the Boltzman constant,  $q$  is the elementary charge and  $a$  is the diode ideality factor, which typically lies around 1.2 for silicon substrates. This gives us  $V_T \approx 30.8mV$  for one cell.

The current generated by the cell is calcualted according to equation 3, whereby  $I_n$  is the nominal current and  $G$  and  $G_n$  is the actual and nominal solar irradiation, respectively.

A common optimisation, according to [11], is to set  $I_n \approx I_{sc}$  and again assume that the temperature is constant ( $T = T_n$ ), giving us  $\Delta_T = 0$  and simplifying equation 3 to equation 4.

Finally, the diode leakage current at the nominal temperature (for other temperatures please see [11]) is calculated with equation 5.

If we insert equations (5) and (4) back into (1) we get equation 6.

If we now assume  $V_{oc} > 5 \cdot V_T$  we can say that  $e^{\frac{V_{oc}}{V_T}} - 1 \approx e^{\frac{V_{oc}}{V_T}}$  and our final formula becomes equation (7).

$$I = I_{pv} - I_o \left[ \exp \left( \frac{V}{V_T} \right) - 1 \right] \quad (1)$$

$$V_T = akT/q \quad (2)$$

$$I_{pv} = (I_n + K_I \Delta_T) \frac{G}{G_n} \quad (3)$$

$$I_{pv} = I_{sc} \frac{G}{G_n} \quad (4)$$

$$I_o = \frac{I_{sc}}{e^{V_{oc}/V_T} - 1} \quad (5)$$

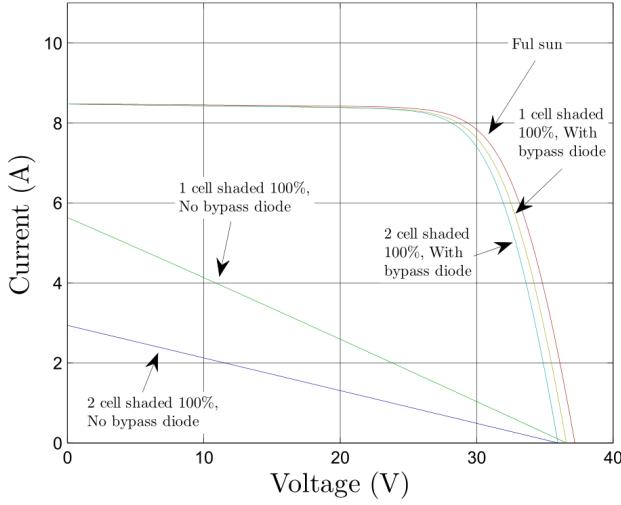
$$I = I_{sc} \left( \frac{G}{G_n} - \frac{e^{\frac{V}{V_T}} - 1}{e^{\frac{V_{oc}}{V_T}} - 1} \right) \quad (6)$$

$$I = I_{sc} \left( \frac{G}{G_n} - e^{\frac{V-V_{oc}}{V_T}} \right) \quad (7)$$

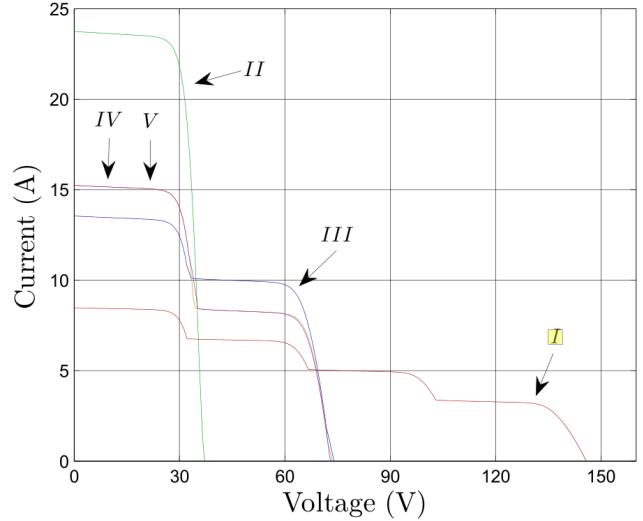
#### 2.1.2 Multiple Cells in Series

If the solar irradiation is the same for every cell in series, then the whole array can be simulated using equation (7), where  $V_{oc}$  and  $V_T$  are linearly scaled with the number of cells.

If the irradiation is not the same for all cells, such as when one cell is shaded, a more complex model must be used.



**Figure 1:** I-V curves for different configurations and shaded cells [5]



**Figure 2:** The typical characteristic of modules connected in series or in parallel

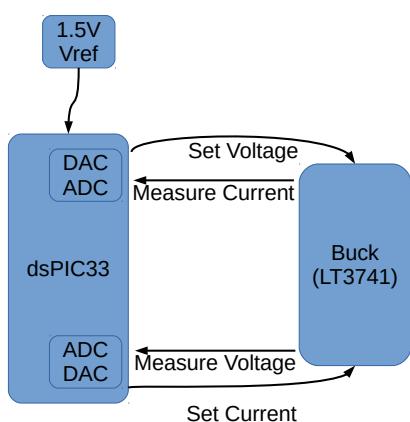
Figure 1 shows various characteristic curves of a shaded PV module and the effect of bypass diodes on them. In our model we can emulate the I-V curve of an array with a shaded cell and no bypass diode by setting  $V_T = V_{oc}$ .

The characteristic curves shown in Figure 2 show how “steps” emerge when two or more modules with bypass diodes, which are each exposed to different irradiation intensities, are connected in series. To emulate this behaviour, we take a number of curves with decreasing short circuit current and increasing open circuit voltage and determine which curve is applicable by checking what curve returns the maximum current for the given voltage.

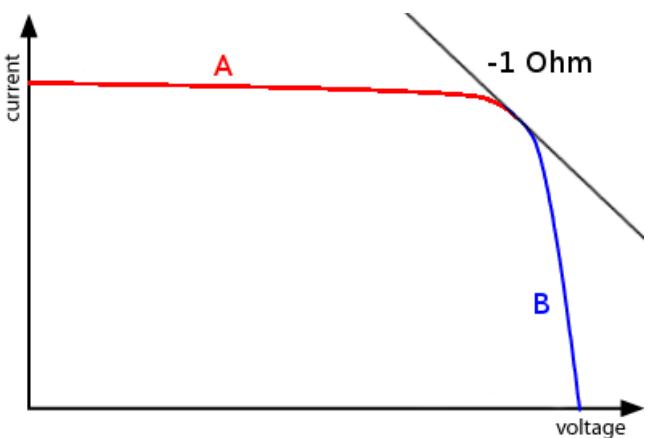
## 2.2 Implementation of Regulation

To increase accuracy in emulating the I-V characteristic curve, both output voltage and output current of the device’s operating point are monitored. If the operating point is above the  $-\frac{1V}{1A} = -1\Omega$  slope (“A” in figure 4), more accurate regulation can be achieved by operating the regulator in constant current mode. In contrast, if the operating point is below the  $-1\Omega$  slope (“B” in figure 4), operating the regulator in constant voltage mode will yield a more accurate result.

A more detailed explanation can be found in section 5.1.2 on page 12.



**Figure 3:** Block diagram of control circuit



**Figure 4:** I-V-Curve with  $-1\Omega$  slope indicated

## 2.3 Hardware

Our device is based on a microcontroller, which is used to handle user input and output and controls the step-down converter. Power delivery is realised with a prebuilt DC power supply unit. In addition to interacting with the device directly, users can also connect a PC to our device by USB and then use our front-end software *Smooth* to interface with the device (section 5.2, p. 12ff).

With an eye towards potential serial production, we developed our own PCB. This allows tight control over impedances in the connections between critical components and brings the behavior of the prototype device much closer to a mass produced version than a breadboard solution could. This is because trace routing lengths and component placement are crucial factors, as is discussed in section 6 (p. 13ff), *Verification*.

## 3 Component Selection

In this section, the selection of the critical components is discussed in detail. Mainly, this concerns the microcontroller, the power delivery (both external and internal) and the circuitry used in conjunction with the step-down converter. A more comprehensive list of components including costs can be found in appendix C beginning on page 22. The complete schematics are located in appendix D on pages 25ff.

### 3.1 Microcontroller

Microchip was chosen as manufacturer because one of our team members was already familiar with their products. Additionally, Microchip provides good developer tools for free. For selecting a specific model, the following criteria eventually lead us to the *dsPIC33EP16GS506*:

- 120 MHz clock (60 MIPS): High enough to allow a fast control loop.
- 2 ADCs and 2 DACs with external voltage reference: Required by the control scheme we use (see section 2.2 on 3).
- PGA (Programmable Gain Amplifier) ( $64 \times$  analog pre-amplifier): Allows measuring the small differential voltages over shunt resistors to measure currents (see section 3.4.5 on pages 8ff).
- Low cost of 4 CHF

### 3.2 36V Power Supply and Mains Input

The maximum required output power of our device was roughly calculated as  $24\text{ V} \cdot 3\text{ A} = 72\text{ W}$  (maximum output voltage times maximum output current, based on the VI-curve in the specifications, see appendix A on page 19). Assuming an efficiency of  $\eta \approx 90\%$  an 80 W power supply is therefore required.

We chose a power supply capable of supplying 28 V at 75 W and mounted it inside the case. It can be plugged into a power outlet by means of an IEC 60320 C13 socket. The socket has a built-in fuse as well as a built-in mains filter, which reduces high frequency coupling back into the mains from the device. A rocker switch is connected in series with the socket and the power supply, allowing for the end user to cut power at any time.

### 3.3 Voltage Rails

In order to power the components used in this design, three different voltage rails are used: 28 V, 5 V and 3.3 V. Each rail has specific requirements concerning electrical noise, power and efficiency. Selecting appropriate voltage regulators requires determining approximate values for the maximum current in each rail.

The power requirements on the 3.3 V rail are primarily determined by the dsPIC33 microcontroller and the LEDs. For maximum processing power, the dsPIC33 will be clocked at its maximum frequency of 120 MHz, consuming  $0.5 \text{ mA MHz}^{-1}$  [7]. Each of the four LEDs consumes 15 mA. This yields a combined current consumption on the 3.3 V rail of

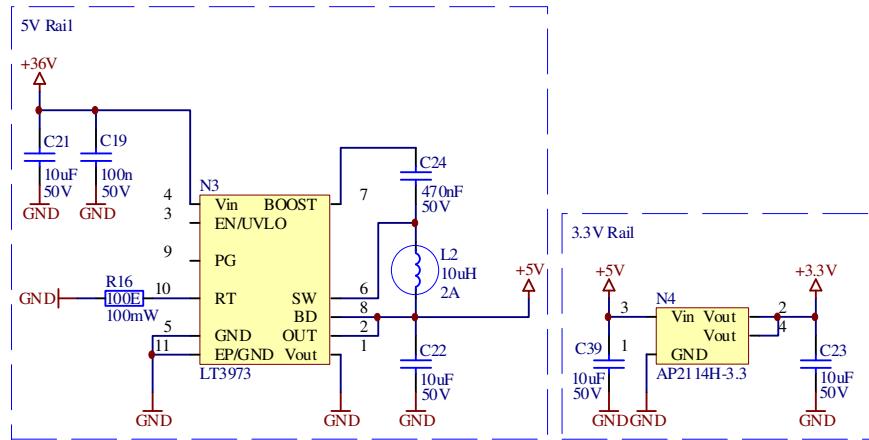
$$I_{3.3\text{V}} = I_{dsPIC} + 4 \cdot I_{LED} = 0.5 \text{ mA MHz}^{-1} \cdot 120 \text{ MHz} + 4 \cdot 15 \text{ mA} = 120 \text{ mA}. \quad (8)$$

The 5 V rail supplies both the 3.3 V rail and the OLED display with power. According to its datasheet [8], the OLED display draws a maximum current of 135 mA. Adding the current for the 3.3 V rail yields an approximate current consumption on the 5 V line of:

$$I_{5\text{V}} = I_{3.3\text{V}} + 135 \text{ mA} = 255 \text{ mA} \quad (9)$$

For generating the lower voltages from the 28 V rail, either linear regulators or switch-mode regulators can be used. Because switch-mode regulators are far more efficient than linear regulators, and efficiency depends on the voltage drop, a switch-mode regulator is used to convert from 28 V to 5 V.

All digital circuitry operates on the 3.3 V rail. Critically, this includes the microcontroller and its digital-to-analog (DAC) and analog-to-digital (ADC) converters. It is therefore crucial for the 3.3 V rail to have as little jitter and noise as possible, making a linear regulator the preferred choice for converting from 5 V to 3.3 V. A low-quality 3.3 V rail could lead to inaccuracies in measuring and regulating output. The circuits for the two conversions from 28 V to 5 V and from 5 V to 3.3 V are illustrated in Figure 5.



**Figure 5:** Supplying the 5 V rail via switch-mode regulator (left) and the 3.3 V rail via linear regulator (right)

### 3.4 LT3741

*Note:* The schematic for the LT3471's circuit is located in appendix B on page 21. It is intended to be folded out while reading this section of the report. This allows for convenient cross-referencing between the circuit schematic and the text without needing to insert multiple copies of the schematic or constantly scrolling back and forth through the report.

The most important reasons we chose the LT3741 to regulate the output voltage are as follows:

- **Proven Technologies.** Switch-mode regulators have been around for decades and have been perfected by many engineers.
- **Voltage and current requirements.** The device is specified to output voltage levels between 0 V and 24 V and current levels between 0 A and 3.5 A. Further, the ripple voltage is specified to be  $\leq 300 \text{ mV}$  and the ripple current is specified to be  $\leq 100 \text{ mA}$ . The LT3741 fulfills all of these requirements.

- **The importance of power absorption.** Most switch-mode regulators are only able to *supply* power, but are incapable of *absorbing* power. Because our device may be connected in series (or parallel) with other power supplies, it must have the ability to absorb power (which is the case if, it were connected to a voltage source outputting a higher voltage level than our own).
- **Control inputs.** The LT3741 has dedicated input control pins to change directly the output current. This simplifies the design because no complicated additional circuitry is required.

Figure 30 on the fold-out (see *Note* above) presents an overview for the LT3741's circuit, parts of which are discussed in more detail in the following paragraphs: Bypass capacitors, switching frequency, inductors, MOSFETs and measuring output current and output voltage.

### 3.4.1 Bypass Capacitors

The LT3741 is powered by the 28 V rail, which can be seen in Figure 30 in the top right. The switching of the MOSFETs causes the LT3741 to consume high amounts of power in short bursts. This leads to the LT3741 feeding high frequency disturbance back into the 28 V rail, which could lead to disturbances in the rest of the circuit if not handled correctly. As a countermeasure, a multitude of different ceramic and electrolytic bypass capacitors in parallel are used. Additionally, we used ferrite beads, placed in series with the supply to absorb any high frequency feedback.

### 3.4.2 Switching Frequency

There is a trade-off when selecting the switching frequency  $f_S$ . The higher  $f_S$ , the lower the output ripple voltage will be. However, the LT3741's power consumption will also increase due to switching losses. Generally,  $f_S$  is to be maximised to reduce ripple.

Because so much depends on  $f_S$ , it is more convenient to determine this value empirically through simulations. The most suitable value was determined to be  $f_S \approx 800$  kHz. In the remaining calculations,  $f_S$  is assumed to be 1 MHz to allow for some leeway.

### 3.4.3 Inductor Selection

The size of the inductor  $L_1$ , as illustrated in Figure 30 on the fold-out, was calculated using the formula below:

$$L_1 = \left( \frac{V_{in} \cdot V_{out} - V_{out}^2}{0.3 \cdot f_S \cdot I_O \cdot V_{in}} \right) = 6 \mu\text{H} \quad (10)$$

where  $V_{in}$  equals the input voltage 28 V,  $V_{out}$  is the output voltage at peak power (which exists at  $V_{out} = 14$  V),  $f_S$  is the switching frequency 1 MHz and  $I_O$  is the maximum output current, assumed to be  $I_O = 5$  A, allowing for some additional leeway. A larger inductor of  $L_1 = 22$   $\mu\text{H}$  was selected to further decrease ripple current.

In addition to the inductance, the maximum current rating, DCR, and saturation current are also important factors to consider. The inductor's peak current is calculated using

$$I_{L_1peak} = I_O + \left( \frac{V_{in} \cdot V_{out} - V_{out}^2}{2 \cdot f_S \cdot L_1 \cdot V_{in}} \right) = 5.2 \text{ A} \quad (11)$$

Where  $V_{in}$  equals the input voltage 28 V,  $V_{out}$  is the output voltage at peak power (which exists at  $V_{out} = 14$  V),  $f_S$  is the switching frequency 1 MHz,  $L_1$  is the value of the selected inductor (22  $\mu\text{H}$ ) and  $I_O$  is the maximum output current, assumed to be  $I_O = 5$  A. The inductor's saturation current was sized 1.2 times higher than the peak current. With this defined, a list of possible inductors could be compiled, shown in Table 1 in appendix E on page 31. We chose the 732-4237-1-ND because it has the lowest DCR (direct current resistance) of the models listed.

### 3.4.4 MOSFET Selection

In contrast to a non-synchronous regulator, our design uses two complementary MOSFETs  $V_2$  and  $V_3$  (in the middle of Figure 30 on the fold-out), whereby  $V_3$  acts as an active replacement for the free wheeling diode typically found in non-synchronous designs. As mentioned earlier, a crucial feature of this device is the ability to *absorb* power.  $V_3$  does this by regulating current in the opposite direction through the inductor  $L_1$ .

When selecting switching MOSFETs, the following parameters are critical in determining the best devices for a given application:  $Q_G$  (Total Gate Charge),  $R_{DS(on)}$  (On-Resistance),  $Q_{GD}$  (Gate to Drain Charge),  $Q_{GS}$  (Gate to Source Charge),  $R_G$  (Gate Resistance),  $V_{GS}$  (gate-to-source voltage),  $V_{DS}$  (drain-to-source-voltage),  $I_{D_{max}}$  (peak drain current) and  $V_{GTHR}$  (gate threshold voltage).

The maximum drain current is equal to the peak inductor current  $I_{L1_{peak}}$  as calculated in equation 11:  $I_{D_{max}} = I_{L1_{peak}} = 5.2 \text{ A}$

The maximum drain-to-source voltage  $V_{DS}$  must be greater than the input voltage  $V_{in} = 28 \text{ V}$ , including transients, otherwise the MOSFETs will be damaged. MOSFETs with  $V_{DS} = 40 \text{ V}$  were therefore selected.

The signals driving the gates of the MOSFETs have a maximum voltage of 5 V with respect to the source. During start-up and recovery conditions, the gate drive signals may be as low as 3 V. Therefore, to ensure that the LT3741 recovers properly, the maximum gate threshold voltage should be less than 2 V. For a robust design, the maximum gate-to-source voltage  $V_{GS}$  should be greater than 7 V.

Power losses in the MOSFETs are related to the on-resistance  $R_{DS(on)}$ , the transition losses related to the gate resistance  $R_G$ , gate-to-drain capacitance  $Q_{GD}$  and gate-to-source capacitance  $Q_{GS}$ . Power loss to the on-resistance is an Ohmic loss,  $I^2 R_{DS(on)}$ . The power loss in the high side MOSFET  $V_2$  can be approximated with equation 12.

$$\begin{aligned} P_{LOSS} &= (\text{ohmic loss}) + (\text{transission loss}) \\ &\approx \left( I_O^2 \cdot R_{DS(on)} \cdot \rho_T \right) + \left( \frac{V_{in} \cdot I_O}{5 \text{ V}} \cdot (Q_{GD} + Q_{GS}) \cdot (2 \cdot R_G + R_{PU} + R_{PD}) \cdot f_S \right) \end{aligned} \quad (12)$$

whereby  $\rho_T$  is a temperature-dependant term of the MOSFET's on-resistance. Using 70 °C as the maximum operating temperature,  $\rho_T$  roughly equals 1.3.  $R_{PD}$  and  $R_{PU}$  are the LT3741 high side gate driver output impedances, 1.3 Ω and 2.3 Ω, respectively.

Driving the gates also causes power loss in switching MOSFETs. The total gate charge,  $Q_G$ , must be charged and discharged switch each switching cycle. The power is lost to the internal LDO within the LT3741. The power lost to the charging of the gates is:

$$P_{LOSS\_LDO} \approx ((V_{in} - 5 \text{ V}) \cdot (Q_{GLG} + Q_{GHG}) \cdot f_S) \quad (13)$$

whereby  $Q_{GLG}$  is the low side gate charge and  $Q_{GHG}$  is the high side gate charge.

Table 2 in appendix F on page 31 lists possible MOSFETs that meet the above constraints. For each one the power losses  $P_{LOSS}$  and  $P_{LOSS\_LDO}$  were calculated. The MOSFET which ended up being selected is not the best model, but it is a lot cheaper than the best fit and has better documentation.

### 3.4.5 Measurement of Output Voltage and Output Current

The LT3741 is both voltage regulated and current regulated. The voltage divider  $R_{11} \parallel R_2$  (Figure 6) allows for the measurement of the output voltage, and a shunt resistor  $R_4$  allows for the exact monitoring of the current going through coil  $L_1$ . The value for resistor  $R_4$  (fold-out overview schematic, Figure 30) was chosen so that the maximum outgoing current can be 5 A.

Monitoring the current is extremely important for a setup in which the outgoing voltage can be constantly changing. It allows to predict the behavior of the output voltage, thus enabling the device to better suppress spikes in output voltage and spikes in the current through coil  $L_1$  (Figure 30 on fold-out).

Furthermore, a controller regulated by current can also be used as a constant current source. This property is of importance when the operating point is in the steeper part of the PV module's I-V-curve (where small changes in voltage can lead to drastic changes in current, see section 2.2 on page 3).

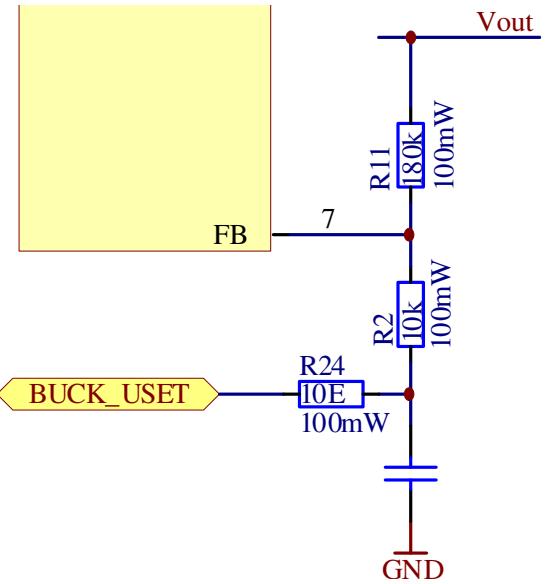
The values for the feedback resistors  $R_2$  and  $R_{11}$  were chosen according to formula 14 so that the output voltage does not exceed 23 V.

By increasing  $BUCK\_USET$  in formula 15, the outgoing voltage can then be modified as needed.  $BUCK\_USET$  is the analog voltage coming from the first DAC. The associated circuit can be found in Figure 6.

In a manner analogous to regulating the output voltage, the maximum output current can also be controlled. By applying an analog voltage between 0 V and 1.5 V at input  $CTRL1$  of the LT3741 controller, the maximum average current going through coil  $L_1$  and therefore the maximum output current can be directly controlled.

The corresponding circuit can be found in Figure 7. The maximum average output current  $I_o$  is calculated using equation 16.

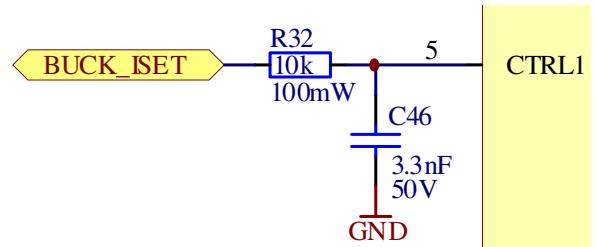
For this,  $V_{CTRL1}$  is the analog reference voltage coming from the second DAC and  $R_4$  is the shunt resistor ( $10 \text{ m}\Omega$ , visible on the fold-out in Figure 30).



**Figure 6:** Circuit for regulating output voltage by changing reference voltage via  $BUCK\_USET$  from the first DAC

$$V_{out} = 1.21 \text{ V} \left( 1 + \frac{R_{11}}{R_2} \right) \quad (14)$$

$$V_{out} = (1.21 \text{ V} - BUCK\_USET) \cdot \frac{R_{11} + R_2}{R_2} \quad (15)$$

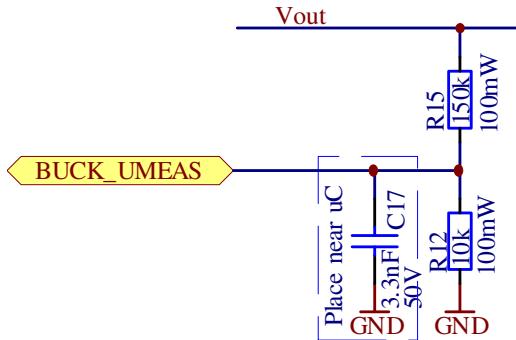


**Figure 7:** Setting the maximum output current via reference voltage between 0 V and 1.5 V

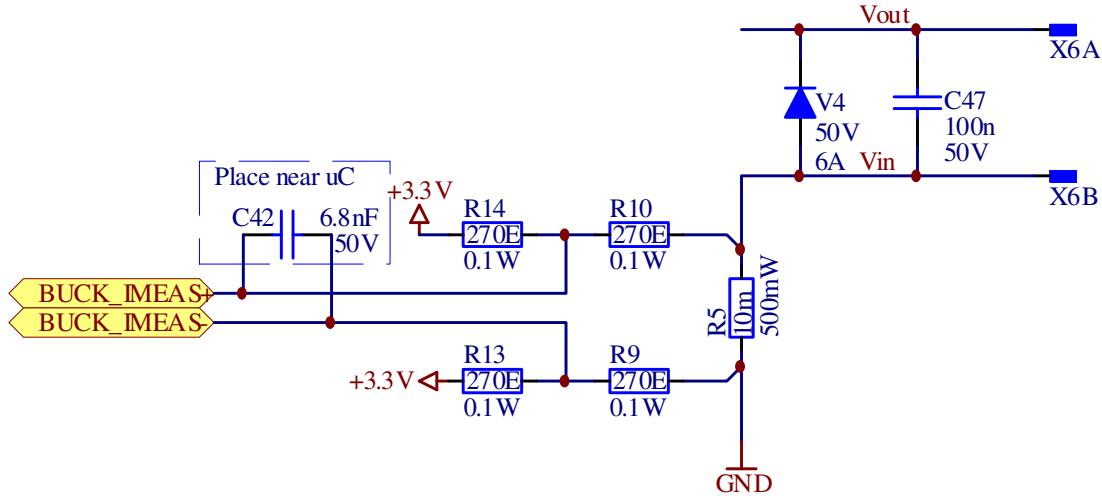
$$I_o = \frac{V_{CTRL1}}{30 \cdot R_4} \quad (16)$$

For the microcontroller to generate appropriate reference voltages, it needs to measure both output voltage and output current. The output voltage is measured with the circuit in Figure 8. The values for resistors  $R_{12}$  and  $R_{15}$  are such that voltage  $BUCK\_UMEAS$  is scaled to the range between 0 V and 1.5 V.

The output current is measured differentially via shunt resistor  $R_5$ . The corresponding circuit can be seen in Figure 9.



**Figure 8:** Measuring output voltage



**Figure 9:** Measuring output current

A particular problem for this measurement is that resistors  $R_{10}$  and  $R_{14}$  cause a bias current to flow through the shunt resistor  $R_5$ , thus leading to an offset  $V_{offset}$  of the measured voltage over  $R_5$ , as calculated by equation 17.

Since the ADC has a resolution of 12 bits and a reference voltage of 3.3 V, one voltage increment amounts to  $V_{step} = \frac{3.3\text{ V}}{2^{12}} = 806\text{ }\mu\text{V}$

Resistors  $R_9$ ,  $R_{10}$ ,  $R_{13}$  and  $R_{14}$  should be as small as possible in order to reduce disturbances in the traces, while at the same time being large enough for  $V_{offset}$  to be smaller than  $V_{step}$ . In order for the ADC's holding time not to be too long (which happens roughly at  $\geq 5\text{ k}\Omega$ ), they should however also not be too large.

Thus, we can now solve for the four resistor values, as seen in on the right.

This yields as its result  $\frac{R_x}{2} \approx 22\Omega$ .

A further limitation, especially for smaller resistors, is not to dissipate too much power. For this reason, the resistors will be dimensioned slightly higher at  $270\Omega$ . Thus, the resulting dissipated power for all four resistors is calculated using equation 18.

$$V_{offset} = \frac{3.3 \text{ V} \cdot R_5}{R_{14} + R_{10} + R_5} \quad (17)$$

$$\begin{aligned}V_{step} &\geq V_{offset} \\ \frac{3.3\text{ V}}{2^{12}} &\geq 3.3\text{ V} \cdot \frac{R_5}{R_x + R_5} \\ \frac{1}{2^{12}} &\geq \frac{R_5}{R_x + R_5} \\ R_x &\geq \left(2^{12} - 1\right) \cdot R_5\end{aligned}$$

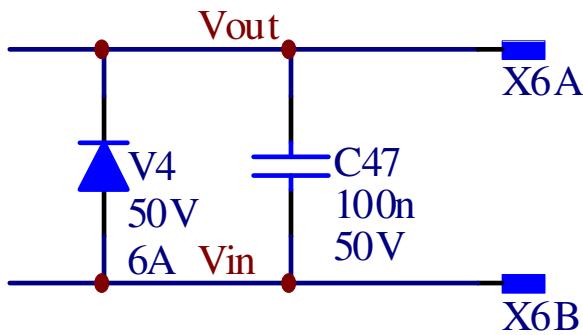
whereby  $\frac{R_x}{2} = R_9 = R_{10} = R_{13} = R_{14}$ .

$$P_{loss} \approx \frac{(3.3\text{ V})^2}{2 \cdot 270\Omega} \approx 20\text{ mW} \quad (18)$$

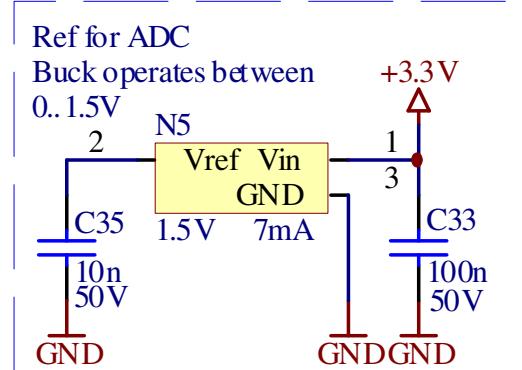
The measured voltage at the shunt resistor is comparatively small. For this reason, we use the microcontroller's integrated pre-amplifier (PGA), which can attain a gain of up to factor 64. The amplified signal is then passed on to the internal differential ADC.

### 3.4.6 Output

Two banana plugs  $X_{6A}$  and  $X_{6B}$  provide the connection to the output voltage, while reverse voltage protection is achieved via diode  $V_4$ . (Figure ). An external reference voltage of 1.5 V is used to ensure that the ADCs and DACs can make accurate measurements and can be used over their full range (see figure 11).



**Figure 10:** Reverse voltage protection at output

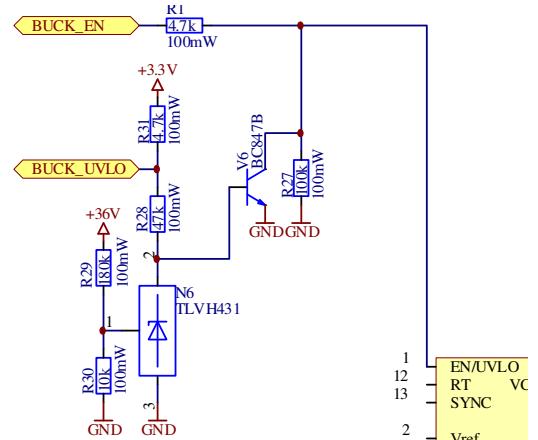


**Figure 11:** 1.5 V reference voltage for full-range operation of DACs and DACs

### 3.4.7 Enable and Under-Voltage Lockout circuit

The LT3741's *Enable* input is enabled and disabled by the microcontroller's *BUCK\_EN* signal on one hand, on the other hand it is can be forcibly disabled in hardware when the 28 V rail drops below 25 V. This allows for a controlled and predictable behavior of the LT3741 during power-on and power-off. The corresponding circuit can be found in Figure 12.

In case of under-voltage,  $N_6$  switches on and the transistor  $V_6$  starts to conduct, thus pulling the *Enable* input to *Low*. Voltage *BUCK\_UVLO* triggers an interrupt in the microcontroller.



**Figure 12:** Under-Voltage Lock-Out (UVLO) allows for controlled power-on and power-off of the controller

## 4 PCB Design

When designing a PCB – especially when a switch-mode power converter is a central component to the design – the location of components and their routing (electrical connections) can be critical for correct operation. Some of the more important items that were considered are listed here.

- High frequency, high power loops are routed as tightly as possible.
- Sensitive, high impedance traces are kept separate from other signals and routed as differential pairs where necessary.
- Digital logic is kept separate from analog and high power circuitry.
- Power rails and their bypass capacitors need to be placed intelligently.
- Larger copper areas can be used to meet heat dissipation requirements.
- The positioning of mechanical parts can be annoying because they take up way more space than what one might initially, naively, expect.

Figure 13 shows how our  $60\text{ mm} \times 60\text{ mm}$  printed circuit board is partitioned. The ground plane has been split from top to bottom, physically separating partition A from the other three partitions. The LT3741 is placed in the centre where top and bottom planes join because it must communicate both with the digital logic as well as the high power circuitry. Partition A contains high power/high frequency components, such as the two switching MOSFETs, the inductor, and the output capacitors, whereas the other partitions contain more sensitive circuitry (in particular partition C). The split helps minimising crosstalk.

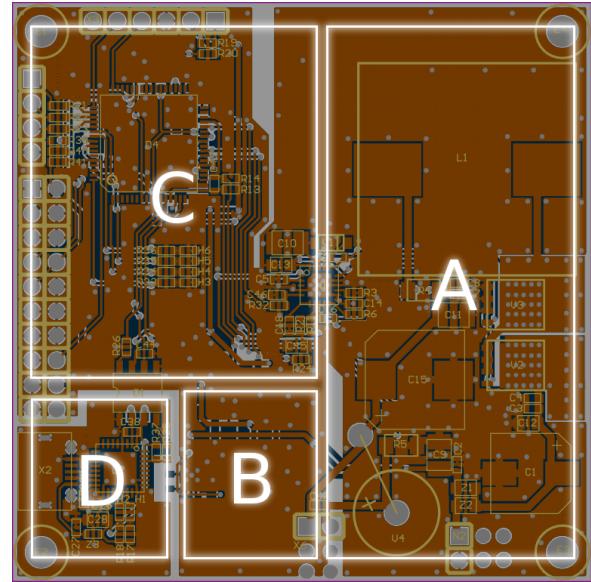
Partition C contains the micro controller, LCD header, push/twist button header and other digital components.

Partition B contains the components responsible for generating the three voltage rails discussed in section 3.3. It was placed at the bottom of the board where the power input is located, to minimize the trace lengths required for power distribution on the board, and it was also placed far away from partition B such that interference with the digital circuitry is minimized.

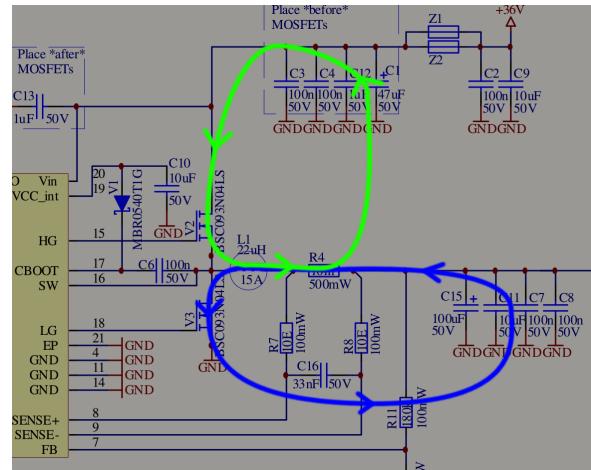
Partition D is electrically isolated from the rest of the circuit and contains the components responsible for USB communication. It was isolated because the voltage potential of a connected USB device may be different than the potential our device is running on.

Figure 14 shows the two critical loops where short intervals of high amounts of current flow in this design. The first (green) loop is active when the switching MOSFET  $V_2$  is conducting and transferring charge from the input bypass capacitors  $C_3$ ,  $C_4$ ,  $C_{12}$  and  $C_1$  through the resistor  $R_4$  into the inductor  $L_1$ .

The second (blue) loop is active when the switching mosfet  $V_3$  is conducting and transferring charge from the inductor  $L_1$  through the resistor  $R_4$  into the output bypass capacitors  $C_{15}$ ,  $C_{11}$ ,  $C_7$  and  $C_8$ .



**Figure 13:** Partitioning scheme of component groups. **A:** High power components **B:** Voltage rails **C:** Digital logic **D:** Isolated transceiver logic



**Figure 14:** Critical high current, high frequency loops in the schematic. Blue indicates the current path of the first critical loop, green the second.

## 5 Software

The software is split into two primary parts: The firmware running on the device itself, and the front-end *Smooth*, used to interface with the device from a PC via USB.

### 5.1 Firmware

#### 5.1.1 Constraints for the uC programm

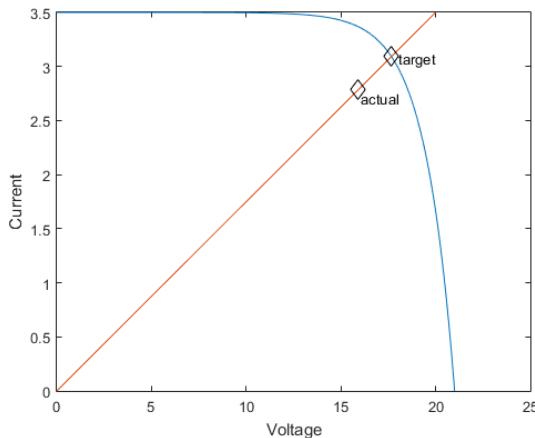
The chosen microcontroller dsPIC33ep provides 16kB of ROM and 2kB of RAM, 12bit resolution in the ADC and DAC and up to 60 MIPS computing power. The anti-aliasing filter of the ADC is set to 5khz, which means that we need to sample with at least 10 kHz. However the LT3741 regulator takes about 300  $\mu$ s to adjust its output voltage – 3 times longer than our sample rate. To remedy this we use Oversampling by factor 4, which has the nice benefits of giving us an additional bit of resolution and making the anti-aliasing filter simpler. The main routine for the adjustment of the regulator should not use more than 25% of the CPU time and must run every 400  $\mu$ s, so it must not take longer than 100  $\mu$ s or about 6000 Instructions to finish one calculation.

#### 5.1.2 I-V Curve and Operating Points

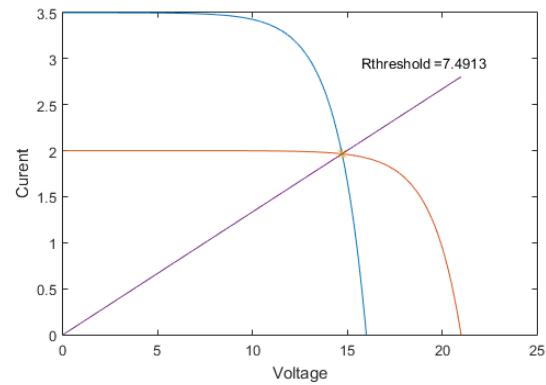
The I-V curve from (7) is implemented using a fixed point library supplied by Microchip. Since this library also provides an exponential function, the implementation is made straightforward.

To find the target operating point, we calculate the load resistance by dividing the voltage on the output by the current on the output  $R_{load} = U_{is}/I_{is}$ . Then we draw the load line  $I = f(U) = U/R_{load}$  and find the intersection with the I-V curve of the model. This process is pictured in Figure 15. The intersection is found by using a binary search algorithm, which is converging slower than newton's method but more stable – Newton's method can fail if  $V_T$  in (7) is small.

If we want to use multiple curves to model the staircase characteristic shown in Figure 2 we need to determine which curve is applicable for a given load. This process can be made less CPU intensive if we precalculate the resistance-thresholds by finding the intersections between two curves. There is always exactly one intersection if  $V_{oc1} > V_{oc2}$  and  $I_{sc1} < I_{sc2}$ .



**Figure 15:** Actual and target operating points



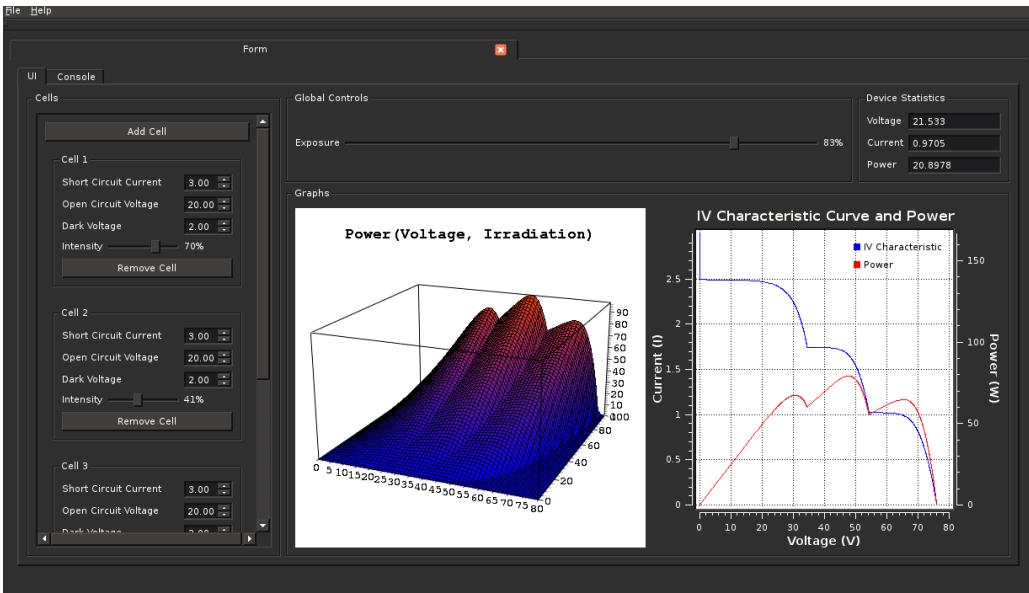
**Figure 16:** Threshold resistance for selecting a curve

### 5.2 Front-End

The front-end is a software tool designed to provide an easy way for users to model complicated behaviours of photovoltaic modules. The software communicates with the device via a USB cable

in real time, which means any changes made in the tool have an immediate effect on the generated output voltage of the hardware device itself.

The front-end was built using the Qt framework [10], Qwt [3] for 2D plots and QwtPlot3D [4] for 3D plots, and was written in C++. Qt was chosen because it supports all major platforms and has a very powerful set of graphical components. Its Graphical User Interface (GUI) can be seen in figure 17. On the left side is a list of cells and their parameters. Cells can be removed or added, and their individual parameters (open circuit voltage, short circuit current, dark voltage and irradiation) can be modified – the effects of which are immediate, as mentioned above. A 2D plot shows what the currently active I-V characteristic curve looks like, along with its corresponding power curve. A 3D plot shows the behaviour of the 2D power curve in function with irradiation. In the top right corner of the GUI the actual measured voltage and current of the device is displayed.



**Figure 17:** Screenshot of the front-end’s Graphical User Interface (GUI)

At this point, the front-end is not yet fully functional as intended. The graphical user interface itself is implemented as planned, but interfacing with the hardware lacks yet a few features. Partially, this is because we could not test all its functionality without the hardware being fully operational. Another reason was the time invested into diagnosing the issues related to the buck converter (section 6.3 on pages 16ff), which needed to be diverted from developing the front-end.

It is however in a solid proof-of-concept stage and ready to be finalised once the device itself operates as intended.

## 6 Verification

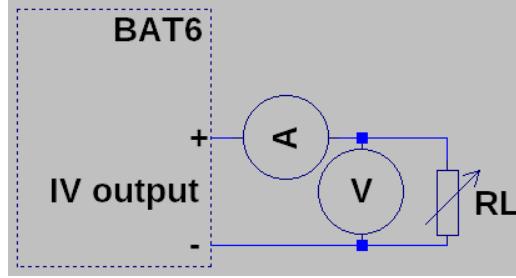
There are a variety of tests that can be conducted to verify the performance and correctness of our device. The following is a list of test fixtures and their expected results based on simulations.

### 6.1 Test Fixtures

#### 6.1.1 Trivial and Non-Trivial I-V Curves

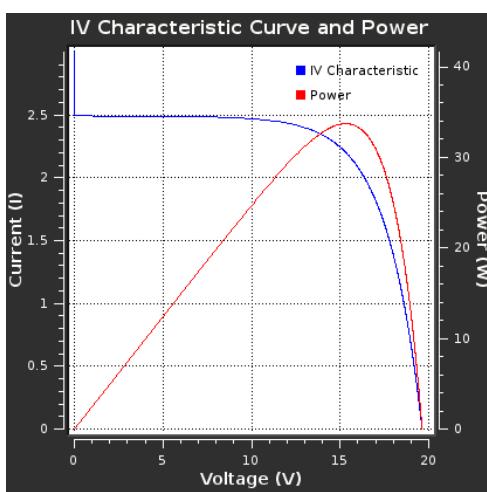
Reproduction of a custom I-V curve is tested by using the test fixture depicted in Figure 18.

The voltage and current is measured using different resistive loads. This measurement is performed twice using two different I-V curve configurations; one “simple” curve (using a single-cell model) and

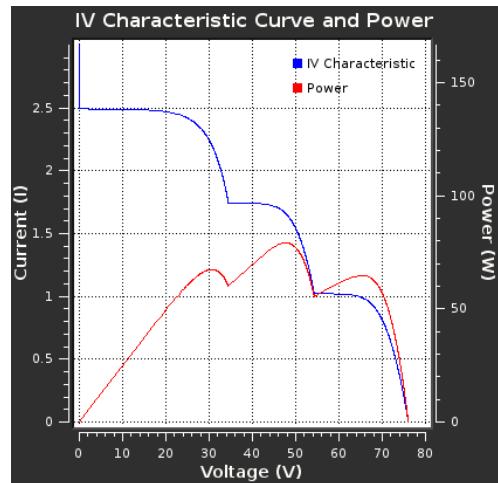


**Figure 18:** Test fixture for measuring the device's IV characteristic curve

one “complicated” curve (using a multi-cell model where some of the cells are shaded). The resulting measurements are then compared with the theoretical curves seen in Figures 19 and 20 and thus the device’s accuracy can be evaluated.



**Figure 19:** Current/voltage characteristic curve (blue) and power/voltage characteristic curve (red) of a single-cell solar panel



**Figure 20:** Current/voltage characteristic curve (blue) and power/voltage characteristic curve (red) of a multi-cell solar panel, some cells are shaded, causing the staircase

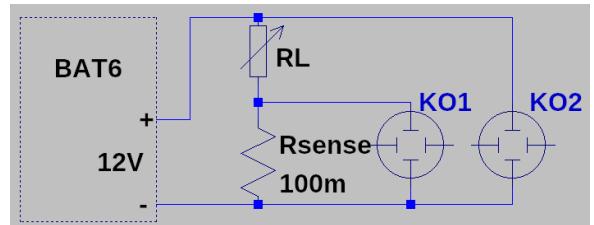
### 6.1.2 Ripple Voltage and Ripple Current vs Resistive Load

Using LTspice [6], the circuit of our regulator was modeled and the peak-to-peak ripple current and voltage was simulated using different resistive loads ranging from  $100\text{ m}\Omega$  to  $1\text{ k}\Omega$  at an output voltage of 12 V. Figure 21 is a plot of the ripple current and voltage versus the resistive load.

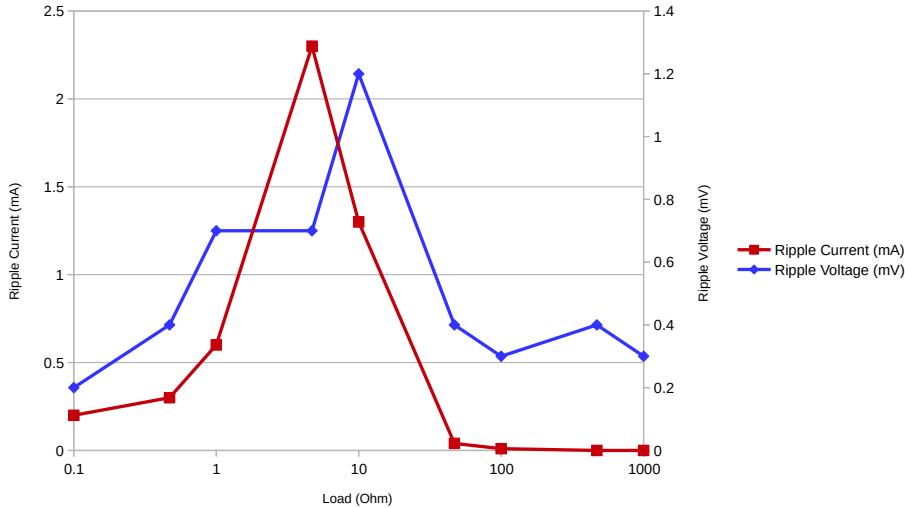
In order to test this on the real device, a constant output voltage of 12 V is programmed and a potentiometer is attached to the device’s output connectors, as illustrated in Figure 22

The ripple current is measured over a small sense resistor  $R_{sense}$  using an oscilloscope. The ripple voltage is measured using a second channel of the oscilloscope by measuring the output voltage.

The peak-to-peak ripple voltage and current is measured for different resistive loads ranging from  $100\text{ m}\Omega$  to  $1\text{ k}\Omega$  and compared to the simulated model.



**Figure 22:** Test fixture for measuring ripple voltage & ripple current of the device



**Figure 21:** Simulation of the amplitude of the ripple voltage and ripple current vs different resistive loads, obtained using LTspice I-V's model of the LT3741

### 6.1.3 Power Absorbtion

As stated in the specifications, the device must have the ability to sink current as well as source current. In order to test this, the device is programmed to output 12 V and is connected in series with a current limiting resistor and a second power source set to a higher voltage, as illustrated in Figure 23.

The second voltage source is slowly increased until 3 A are flowing through the current limiting resistor  $R_1$  (which can be determined by measuring the voltage over said resistor), all while the device's output voltage is closely monitored. The output voltage is expected to remain constant.

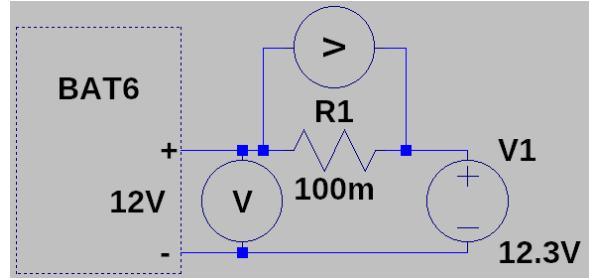
### 6.1.4 Transient Response

This test is used to determine the reaction speed of the regulator and the I-V control algorithm when switching quickly between two extreme resistive loads. The device is programmed to mimic the behaviour of a simple solar panel model. As illustrated in Figure 24 the output voltage is measured using an oscilloscope and various resistive loads are switched on and off over the output using a MOSFET and a signal generator.

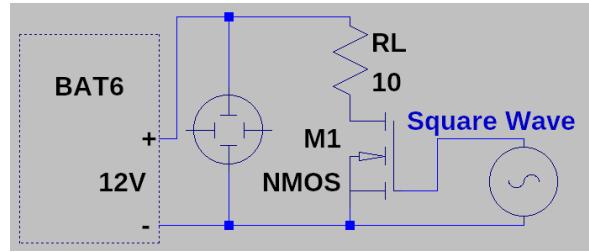
The frequency of the signal generator is set to a low value such that the device's output voltage is always stable before the load is changed. The results of this measurement will make a statement over the propagation delay of the algorithm as well as the time it takes for the voltage to stabilise again.

### 6.1.5 Reactive Loads

In the coarse specification we opted to test the device with various capacitive and inductive loads out of curiosity. During the course of the project we learned that this is not an applicable test because reactive



**Figure 23:** Test fixture for measuring power absorbtion of the device.



**Figure 24:** Test fixture for measuring the transient response of the device

loads are primarily used for testing the behaviour of power factor correction – which, according to the EN61000-3-2 regulations [9], affect devices consuming more than 75 W, meaning that the main power supply we use already implements power factor correction and testing for this would be meaningless. Furthermore, the measurements we obtain from tests using reactive loads would require an immense amount of additional research on our part before the results could be interpreted in any meaningful way. For this reason we have decided to omit this test case.

## 6.2 Measurement Results

Unfortunately, we were unable to operate the LT3741 for a period long enough to conduct any of the measurements listed above. The same regulator model (LT3741) was permanently damaged twice in a row. Please see the next section for a detailed analysis on what we think the issue is and how we would proceed if more time to do so were available.

## 6.3 Analysis of the Issue

The first regulator output the correct voltage of 12 V when being supplied with 32 V. Unplugging the device and re-plugging it into a 36 V power supply instantly damaged it permanently. After some detailed measurements it was concluded that the high-side driver inside the LT3741 was somehow damaged and not operating as it should. Our assumption was that – since we were operating the device very closely to its maximum ratings of 40 V – during switching, the high-side MOSFET driver was exposed to transients exceeding the device's absolute maximum ratings and thus damaging the driver permanently.

The regulator was replaced with a new one and the supply voltage was lowered from 36 V to 28 V in order to give more leeway for the transient voltages. The new regulator appeared to output the correct voltage of 12 V, so a resistive load of  $80\Omega$  was connected to the output of the regulator. After about 20 s of continuous operation, the output voltage again dropped and the device was permanently damaged. Unfortunately, we were unable to capture some vital measurements of the transients we were looking for to confirm our suspicions from the first failure. It is clear, however, that the damage was not caused by the device overheating, as none of the components were remotely warm to the touch. This seems to align with the transient theory.

## 6.4 Simulating the Issue

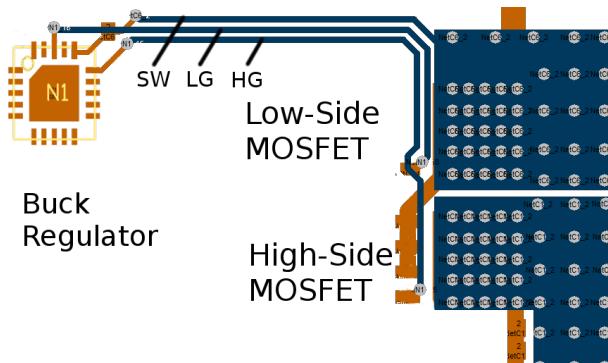
The physical layout of the regulator and the MOSFETs is depicted in Figure 25. The traces connecting the Switch (SW), High Gate (HG) and Low Gate (LG) pins of the regulator to the switching MOSFETs are fairly long ( $>2\text{ cm}$ ). Most of the time, the parasitic inductances and capacitances are negligible. In this case, however, it turned out that they are not.

The series inductance and series resistance is calculated using an on-line calculator [1] [2] (the width, length, and thickness is known to be 0.4 mm, 2 cm and 35  $\mu\text{m}$  respectively) and added to the simulation model seen in Figure 26.

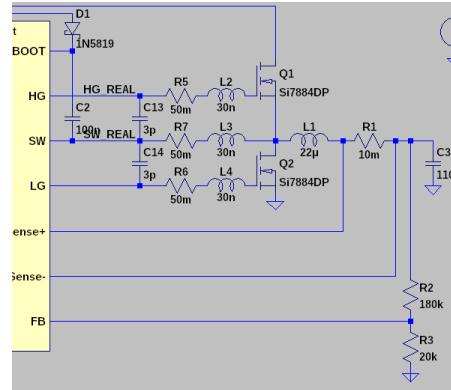
The voltage on the SW pin of the regulator is simulated and plotted. Figure 27 compares the more accurately modelled curve (in blue, labelled *sw\_real*) with the ideal model of the voltage on the SW pin (in yellow, labelled *sw\_ideal*). The two red lines represent the expected maximum voltage (28 V) and the device's absolute maximum rating on the SW pin (40 V).

It is clear that these small parasitic inductances have a huge impact. The real curve (blue) exhibits ringing with an amplitude overshooting the expected maximum voltage by almost 12 V! It is therefore very likely that the high driver was destroyed due to an over-voltage event.

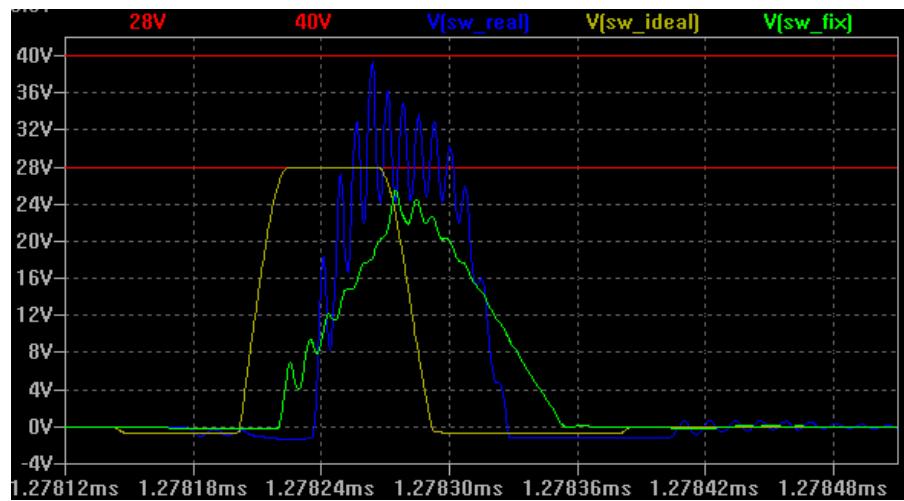
The immediate solution to this problem is to add resistors in series with each of the critical connections to dampen the ringing. The effect of a  $3.3\Omega$  resistor in series with each connection is plotted in figure



**Figure 25:** Physical layout of MOSFETs and regulator



**Figure 26:** Simulation model with long traces



**Figure 27:** Simulation of voltage on SW pin. *Yellow:* Idealised, *blue:* actual, *green:* actual, with series resistors as a fix.

27 (green curve, labelled *sw\_fix*). When compared to the ideal and real curves, we see that the peak voltage has been reduced to a much less dangerous level.

The more optimal solution (more elegant and cheaper) is to modify the PCB layout to drastically reduce the length of these traces.

## 7 Conclusions

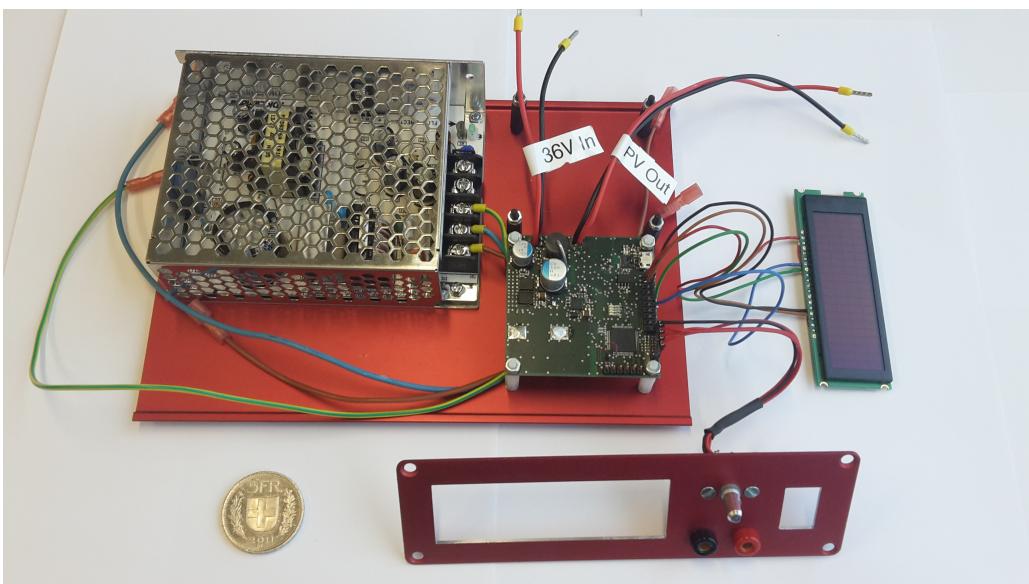
The device is assembled (as can be seen in Figure 28) and has a functioning interface. Thanks to our custom PCB, we were able to make a very compact device (visible in Figure 29). Most sub circuits function as intended (OLED, button, USB, microchip), except for the circuitry related to the buck converter. The front-end software has been successfully brought to proof-of-concept stage and is ready to be implemented fully.

The primary thing which does not function as intended is the buck converter. We were however able to pinpoint the likely cause of the issue and are confident that with more time and a new hardware revision, we could fix this problem.

The next step would now be to print a new PCB with improvements based on our simulations from section 6 and then verify correct functionality of our device.



**Figure 28:** BAT6 assembled, 5 CHF coin for scale



**Figure 29:** BAT6's internals. Note the PCB's compact size. Most of the internal space is taken up by the power supply. 5 CHF coin for scale.

## Appendix A Specifications

## Auftrag / Lastenheft

Windisch, 17.9.15

### PV-Modul Simulator

#### Anlass:

Für das Projekt P4 im nächsten Semester ist die Entwicklung eines Überwachungsgerätes für Photovoltaik-Module (PV-Module) vorgesehen. Um dieses Überwachungsgerät im Labor testen zu können, soll in diesem Semester als P3 Arbeit ein PV-Modul Simulator entwickelt und als Laborgerät aufgebaut werden. Dieser Simulator dient als Labor-Netzgerät mit der Charakteristik eines PV-Moduls und muss die unten aufgeführten Eigenschaften (Anforderungen) aufweisen.

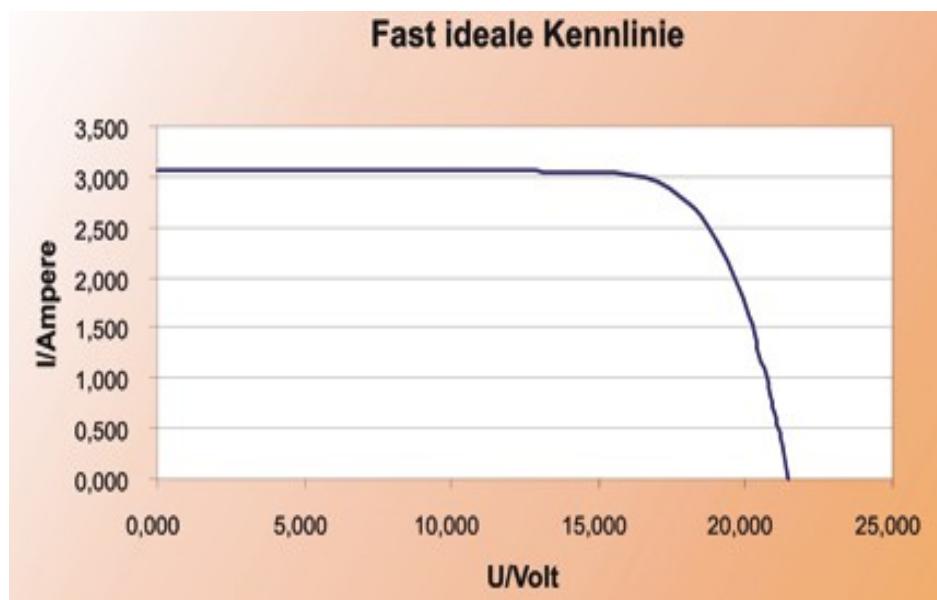
#### Aufgabe:

Sie sollen ein kompaktes Gerät herstellen, welches im Labor als Speise- bzw. Testgerät eingesetzt werden kann und die Eigenschaften eines PV-Moduls aufweist. Wie bei einer Photovoltaik-Anlage, bei der mehrere Module in Serie zu einem String zusammengeschaltet werden, soll auch Ihr Gerät mit den Geräten anderer Gruppen in Serie geschaltet werden können und so eine ganze PV-Anlage bzw. einen String einer Anlage simulieren können.

#### Anforderungen:

- Standard-Elektronik für den Betrieb in Laborumgebung, kompaktes "Laborgehäuse"
- Komponentenkosten max. ca. CHF 200.-
- Betrieb ab Netz mit einem käuflichen Speisegerät (eingebaut oder als Kabelnetzgerät) für die Realisierung der Zwischenkreis-DC-Spannung
- Anschluss der Last über zwei Laborbuchsen (+/-) in der Front des Gerätes
- Bedien- und Anzeigeelemente sind "frei" definier- bzw. realisierbar
- Kennlinie in Microcontroller einprogrammiert
- Funktionsprinzip als Schaltregler (keine Längswiderstände / keine unnötigen Verluste)
- Kennlinie des PV-Moduls nebenan ist zu realisieren.

Die Graphik zeigt die Kennlinie bei einer Einstrahlung von 100%.  
(Der Kurzschlussstrom ist ca. proportional zur Einstrahlung)

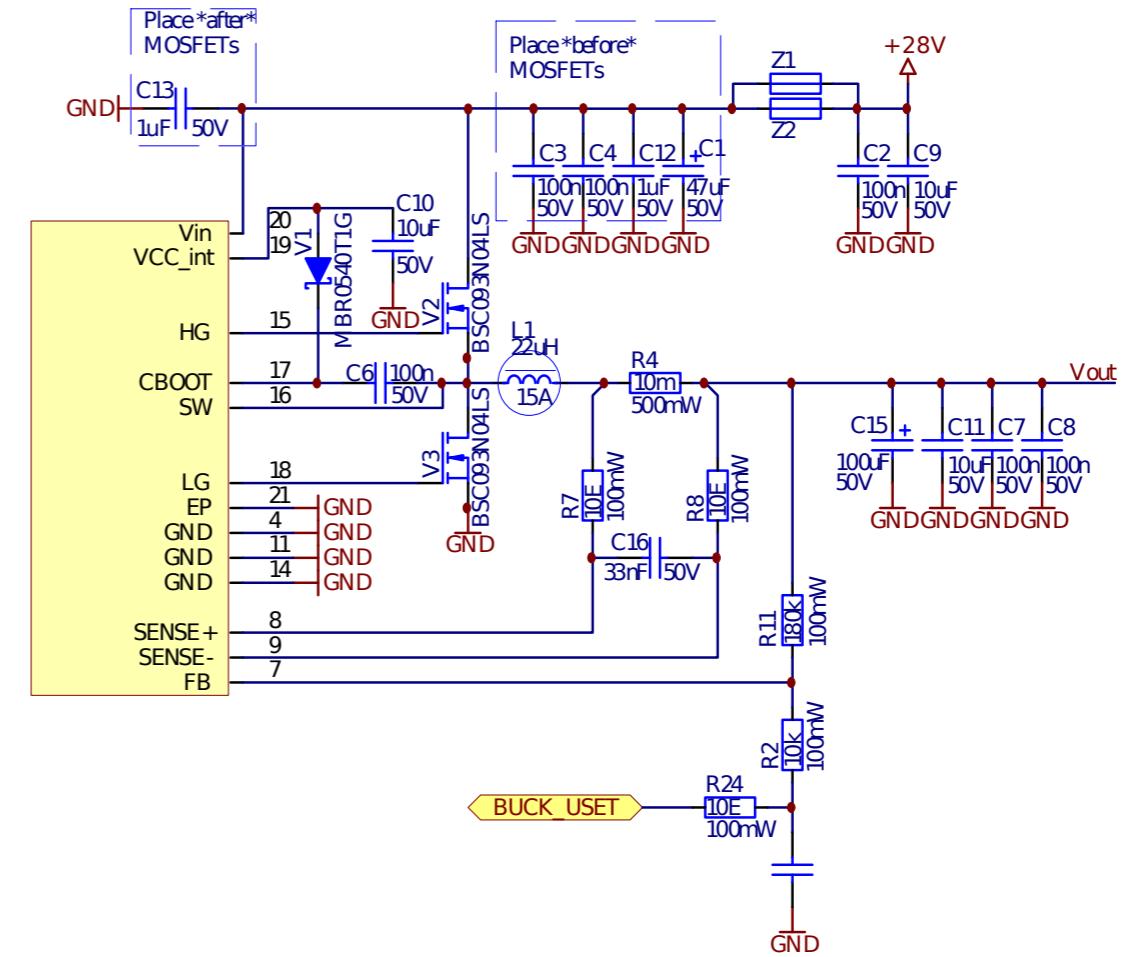


- Die Einstrahlung muss von ca. 20% bis 100% einstellbar sein
- Die Genauigkeit von Strom und Spannung (Rippel) sollte besser +/- 5% sein
- Serieschaltung mit weiteren Geräten muss möglich sein (keine Potenzialbindungen)
- Wirkungsgrad und Kennlinie des Gerätes müssen gemessen und dokumentiert werden.

#### Wunschziele:

- Kennlinien eines verschmutzten und eines teilabgeschatteten Moduls einprogrammiert
- Kennlinien eines defekten (Zellendefekt) Moduls einprogrammiert

## Appendix B LT3471 Circuit



The circuit used to control the LT3471 is described in detail in section 3.4 starting on page 5. For the reader's convenience, the schematic in Figure 30 is intended to be folded out and kept open as a reference while reading that section of this report. This allows for easy cross-checking between text and schematic without needing to constantly scroll through the report's pages or needing to insert multiple copies of Figure .

**Figure 30:** The device's heart: Overview of circuit for the LT3471 CCVC synchronous converter.

**Appendix C List of Components**

# Electronic Components

Quantity	Designator	Value	Value2	Type	Supplier - Digikey	LibRef	Price	Total
1	C1 C2, C3, C4, C5, C6, C7, C8, C19, C20, C25, C26, C29, C30, C31, C32, C33, C34, C38, C40, C41, C44,	47uF	50V		493-4554-1-ND	C_SMD_ALU_47U_50V_20%_PCV1H470MCL7GS	3.42	3.42
22	C47 C9, C10, C11, C21, 7 C22, C23, C39	100n	50V		1276-1936-1-ND	C_SMD_CER_100N_50V_10%_X7R_0603	0.1	2.2
2	C12, C13	1uF	50V		587-2910-1-ND	C_SMD_CER_1U_50V_10%_X7R_0805	0.19	0.38
1	C14	4.7nF	50V		478-1223-1-ND	C_SMD_CER_4N7_50V_10%_X7R_0603	0.1	0.1
1	C15	100uF	50V		493-4558-1-ND	C_SMD_ALU_100U_50V_20%_PCV1H101MCL2GS	5.12	5.12
1	C16	33nF	50V		1276-2042-1-ND	C_SMD_CER_33N_50V_10%_X7R_0603	0.1	0.1
2	C17, C46	3.3nF	50V		490-1503-1-ND	C_SMD_CER_3N3_50V_10%_X7R_0603	0.1	0.2
1	C18	47nF	50V		1276-1063-1-ND	C_SMD_CER_47N_50V_10%_X7R_0603	0.1	0.1
1	C24	470nF	50V		587-3170-1-ND	C_SMD_CER_470N_50V_10%_X7R_0603	0.24	0.24
2	C27, C35	10n	50V		399-1091-1-ND	C_SMD_CER_10N_50V_10%_X7R_0603	0.1	0.2
2	C28, C36	10uF	16V		490-6473-1-ND	C_SMD_CER_10U_16V_10%_X5R_0805	0.2	0.4
1	C37	22uF	6.3V		587-3398-1-ND	C_SMD_CER_22U_6V3_20%_X5R_1206	0.43	0.43
1	C42	6.8nF	50V		1276-1185-1-ND	C_SMD_CER_6N8_50V_10%_X7R_0603	0.1	0.1
1	C45	3.3uF	35V		445-7553-1-ND	C_SMD_CER_3U3_35V_10%_X7R_0805	0.56	0.56
1	D1	ACSL-6210-56RE		516-2916-1-ND	D_ACSL-6210_SO-8		5.09	5.09
1	D2	FT232RQ		768-1008-1-ND	D_FT232RQ		4.5	4.5
1	D3	NHD-0420CW-AR3-ND			D_LCD_80CHAR_20X4_NHD-0420CW-AR3		29.9	29.9
1	D4	DSPIC33EP16GS506DSPIC33EP16GS506-I/PT-ND			D_DSPIC33EP16GS506_TQFP-64		4.09	4.09
4	H1, H2, H3, H4, H5,	M3 Standoffs 20mm		36-25505-ND	E_STANDOFF_20MM_M3_PLASTIC		0.59	2.36
6	H6	Blue		VAOL-S6SB4CT-ND	H_SMD_LED_BLUE_0603		0.5	3
1	L1	22uH	15A		732-4237-1-ND	L_SMD_22U_15A_7MOHM_20%_74435582200	7.83	7.83
1	L2	10uH	2A		732-1200-1-ND	L_SMD_10U_2A_20%_IND_74477710	2.68	2.68
1	L3	4.7uH	1A		732-2956-1-ND	L_SMD_4U7_1A_20%_0806	0.92	0.92
1	N1	LT3741		LT3741EUF#PBF-ND	N_LT3741EUF_QFN-20		8.44	8.44
1	N2	36V	72W		285-1829-ND	N_EXT_ACDC_36V_75W	27.41	27.41
1	N3	LT3973		LT3973EDD-5#PBF-ND	N_LT3973-5_DFN-10-3x3		5.88	5.88
1	N4	AP2114H-3.3		AP2114H-3.3TRG1DICT-ND	N_AP2114H-3.3_SOT223		0.36	0.36
1	N5	1.5V	7mA	ISL21080CIH315Z-TKISL21080CIH315Z-TKCT-ND	N_UREF_1V5_0A007_52UVRMS_ISL21080CIH315Z_SOT-23-3		1.61	1.61
1	N6	TLVH431		296-17972-1-ND	N_TLVH431_SOT23-3		0.72	0.72
6	R1, R31 R2, R12, R19, R30, R32, R37, R38, R39,	4.7k	100mW		YAG1238CT-ND	R_SMD_THINFILM_4K7_0W1_1%_50PPM_0603	0.1	0.6
10	R40, R41	10k	100mW		YAG2321CT-ND	R_SMD_THINFILM_10K_0W1_1%_50PPM_0603	0.1	1
1	R3	43k	100mW		P43KDBCT-ND	R_SMD_THINFILM_43K_0W1_0.1%_25PPM_0603	0.63	0.63
2	R4, R5	10m	500mW		LVK12R010DERCT-ND	R_SMD_THICKFILM_0E01_0W5_0.5%_50PPM_1206	0.74	1.48
2	R6, R28	47k	100mW		YAG3355CT-ND	R_SMD_THINFILM_47K_0W1_1%_50PPM_0603	0.1	0.2
3	R7, R8, R24	10E	100mW		YAG3351CT-ND	R_SMD_THINFILM_10E_0W1_1%_50PPM_0603	0.1	0.3
2	R11, R29	180k	100mW		P180KDBCT-ND	R_SMD_THINFILM_180K_0W1_0.1%_25PPM_0603	0.63	1.26
1	R15	150k	100mW		P150KDBCT-ND	R_SMD_THINFILM_150K_0W1_1%_50PPM_0603	0.63	0.63
6	R16, R17, R18, R21, R22, R23	100E	100mW		YAG2128CT-ND	R_SMD_THINFILM_100E_0W1_1%_50PPM_0603	0.17	1.02
1	R20	470E	0.1W		YAG2128CT-ND	R_SMD_THINFILM_470E_0W1_1%_50PPM_0603	0.17	0.17
1	R25, R9, R10, R13, R14,	270E	0.1W		P270DBCT-ND	R_SMD_THINFILM_270E_0W1_1%_50PPM_0603	0.63	0.63
1	R26	150E	0.1W		P150DBCT-ND	R_SMD_THINFILM_150E_0W1_1%_50PPM_0603	0.63	0.63
1	R27	100k	100mW		YAG2319CT-ND	R_SMD_THINFILM_100K_0W1_1%_50PPM_0603	0.1	0.1

4 R33, R34, R35, R36	33E	0.1W	MCT0603-33.0-CFCT-ND	R_SMD_THINFILM_33E_0W1_1%_50PPM_0603	0.13	0.52	
1 U1		290VAA5F201B1	CT3010-ND	U_ENCODER_2BIT_QUAD_SPST	4.21	4.21	x
1 V1		MBR0540T1G	MBR0540T1GOSCT-ND	V_SMD_SCHOTTKY_MBR0540T1G_40V_0A5_SOD-123	0.36	0.36	x
2 V2, V3		BSC093N04LS	BSC093N04LS GCT-ND	V_SMD_FET_NMOS_40V_13A_24NC_0E0093_PG-TDS0N-8	0.62	1.24	x
1 V4	50V	6A	6A05DICT-ND	V_THT_DIODE_6A05-T_50V_6A	0.43	0.43	x
1 V6		BC847B	BC847BLT1GOSCT-ND	V_SMD_TRANS_NPN_BC847B_50V_0A2_SOT-23-3	0.12	0.12	
1 X1			817-1489-ND	X_POWER_ENTRY_MODULE_W/FILTER_W/FUSE_10A_SMD_	15.96	15.96	x
1 X2		USB Micro B	609-4618-1-ND	X_SMD_USB_MICRO-B_2.0	0.46	0.46	x
1 X3				X_CONNECTOR_P2.54_D0.9_1X6	0		x
1 X4				X_CONNECTOR_P2.54_D0.9_1X4	0		x
1 X6				X_CONNECTOR_P2.54_D0.9_1X2	0		x
1 X7		Rocker Switch	360-1721-ND	X_SWITCH_ROCKER_SPST_6A_250VAC	2.02	2.02	x
2 Z1, Z2	5A	MH2029-600Y	MH2029-600YCT-ND	Z_SMD_FERRITE_5A_60E@100MHZ_0805	0.1	0.2	x
2 Z3, Z4	1.5A	BLM18KG471SN1D	490-5257-1-ND	Z_SMD_FERRITE_1A5_470E@100MHZ_0603	0.1	0.2	x

## Mechanical Components

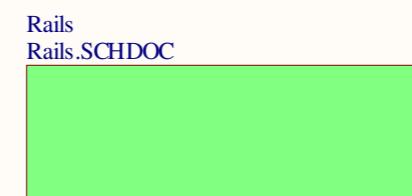
1	Housing	HM1417-ND	30.18	30.18	
1	PCB	Pcb-pool	89.76	89.76	

**Total Cost: 277.76**

## Appendix D Circuit Schematics

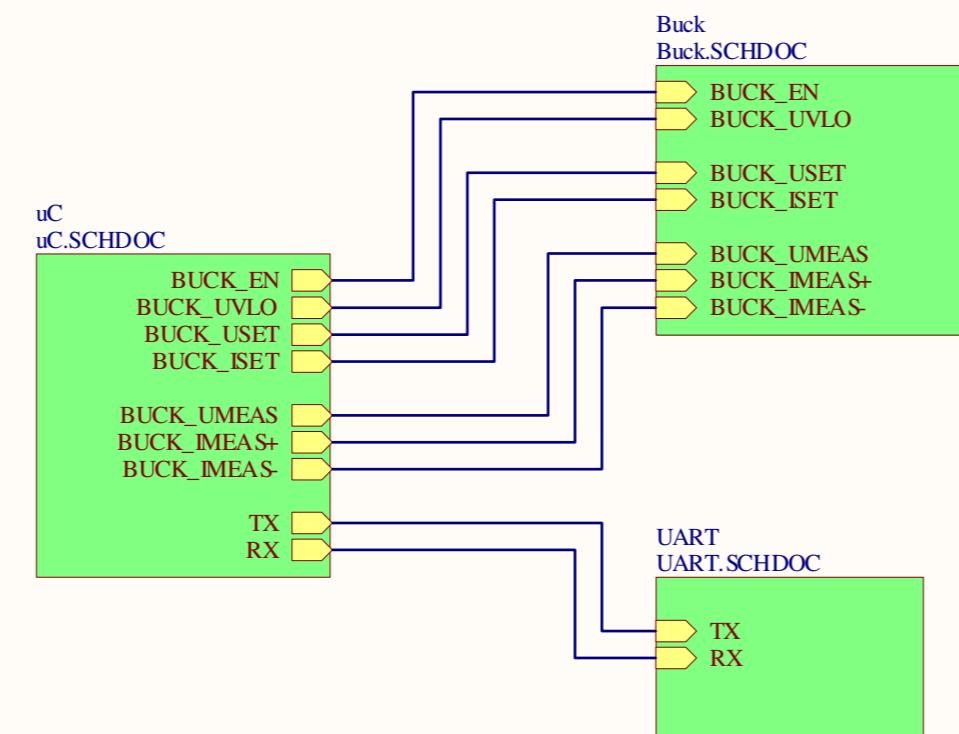
A

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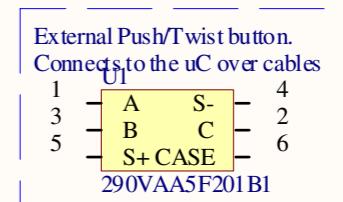
B



C

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- E1 M3 Standoffs 20mm
- E2 M3 Standoffs 20mm
- E3 M3 Standoffs 20mm
- E4 M3 Standoffs 20mm



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## Title

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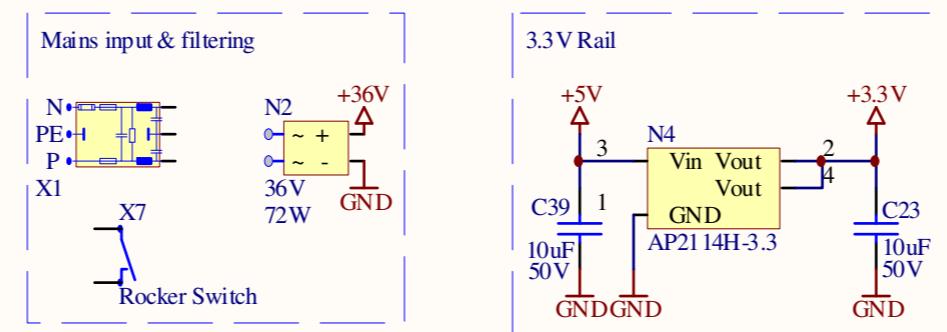
Date: 13/01/2016

Sheet of

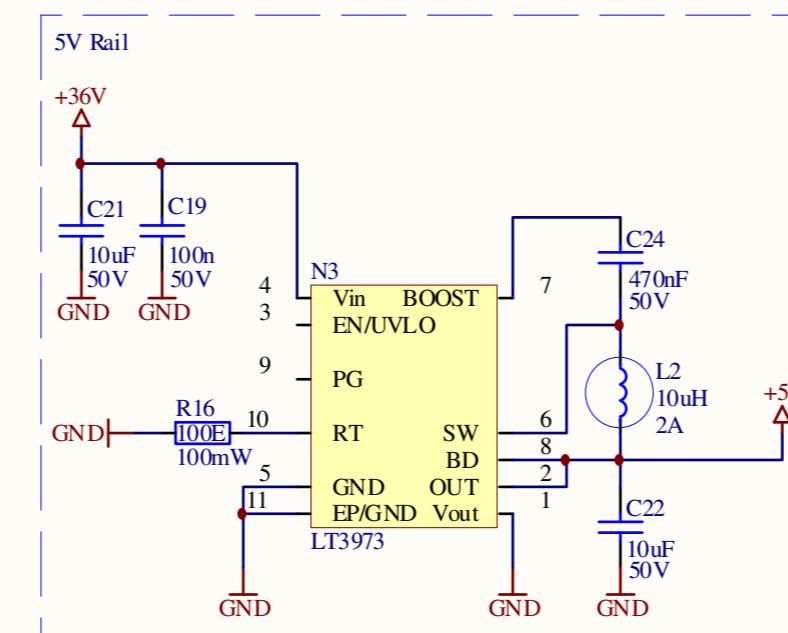
File: C:\Users\IPV-Simulator.SCHDOC

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Date: 13/01/2016

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File: C:\Users\.\Rails.SCHDOC

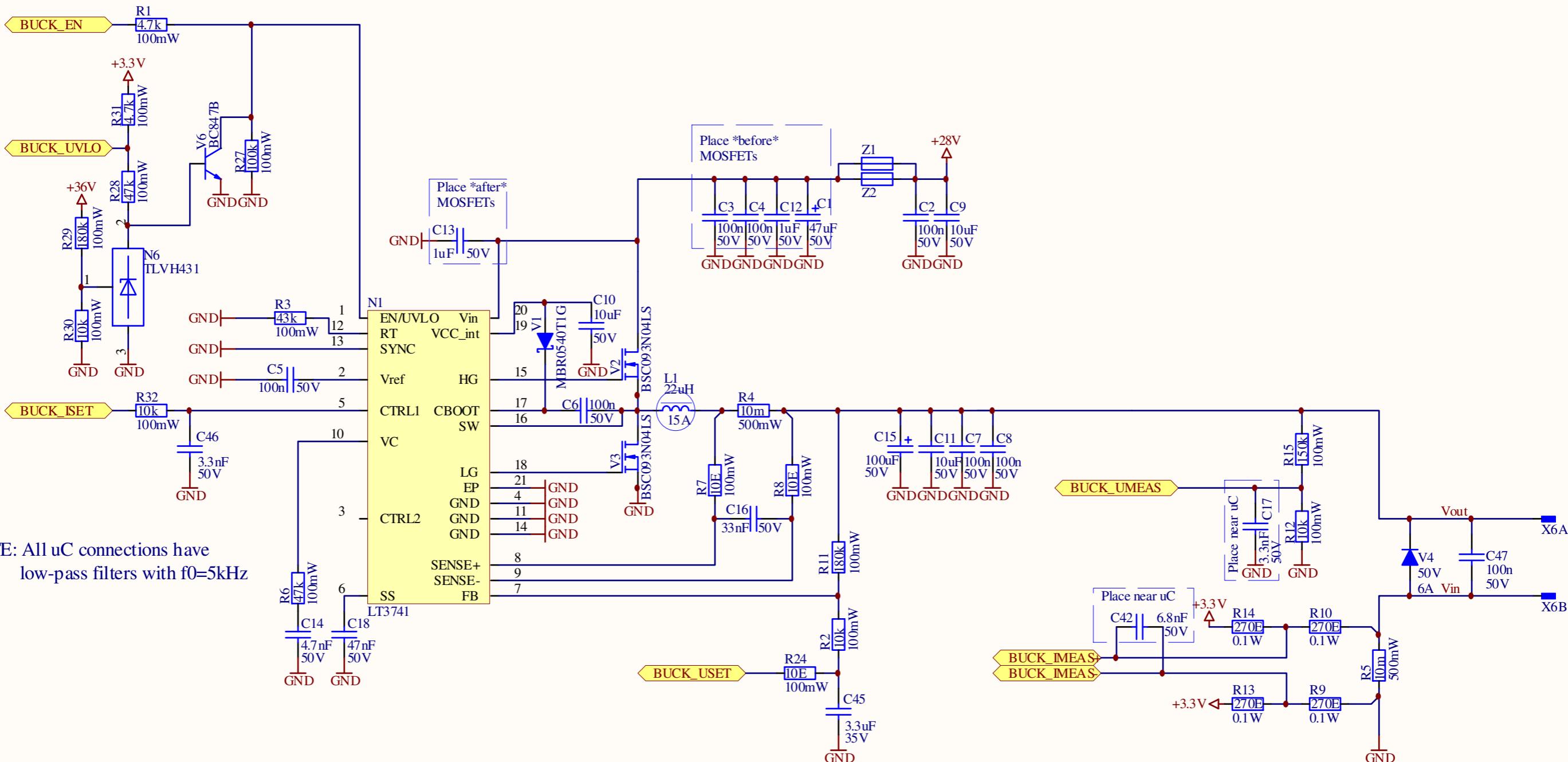
Drawn By

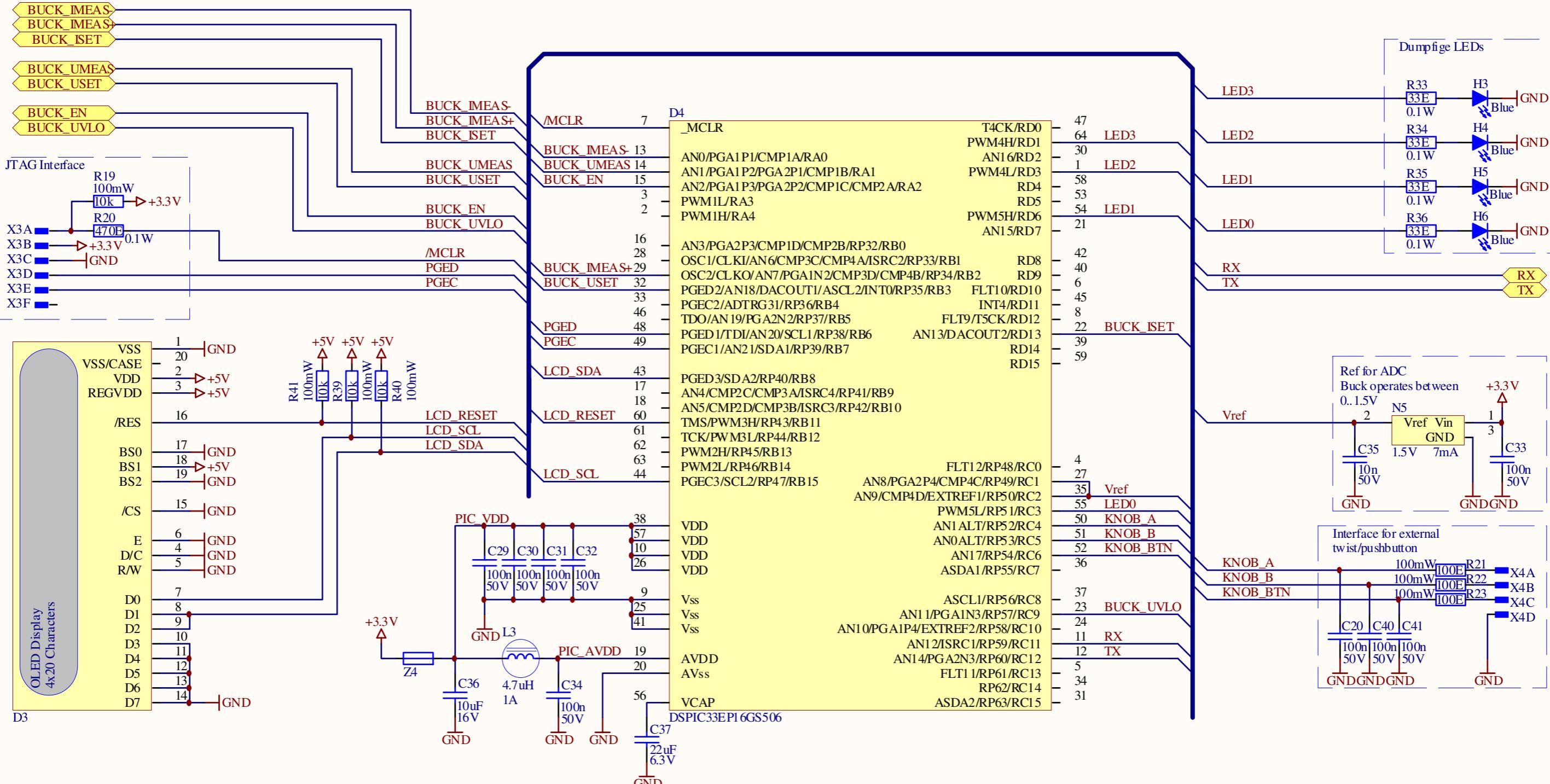
A

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Date:	13/01/2016	Sheet of
File:	C:\Users\.\uC.SCHDOC	Drawn By

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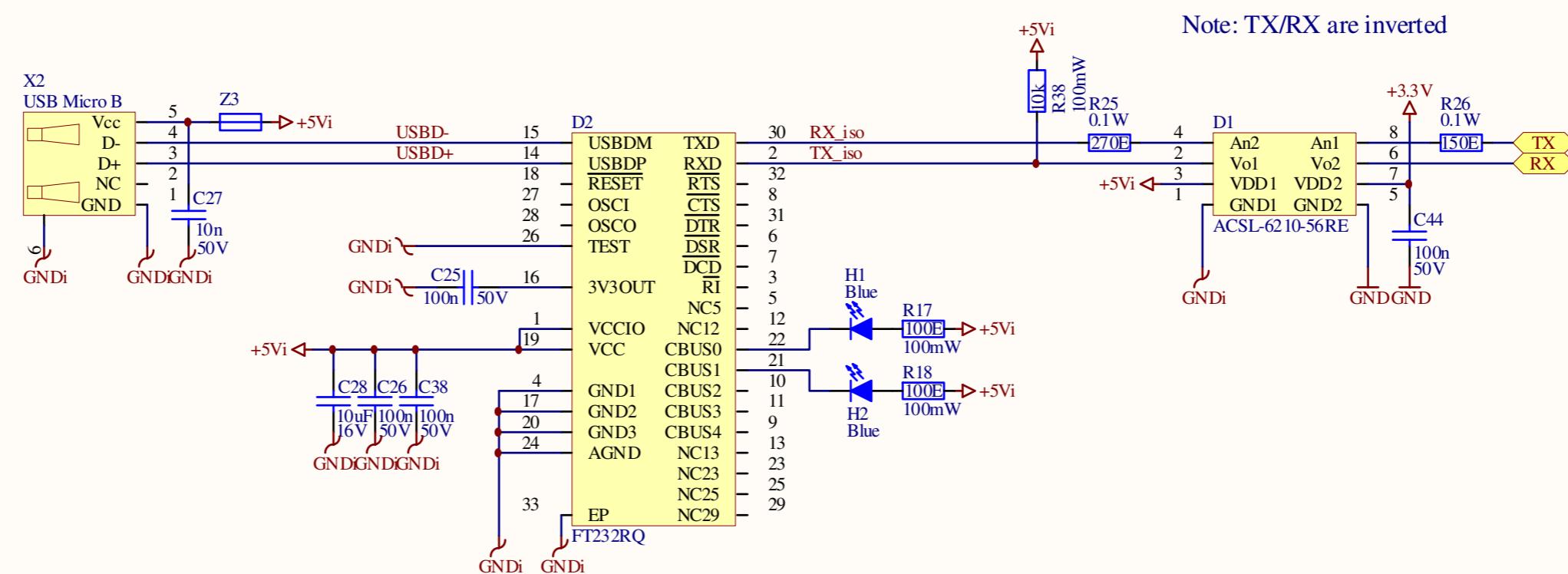
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## Appendix E Inductors

Filtering available inductors according to the criteria outlined in section 3.4.3 on page 6 left us with the models listed in Table 1. The model highlighted in grey was selected due to it having the lowest direct current resistance (DCR).

**Table 1:** List of inductors matching our requirements

Digikey	Price (CHF)	Inductance ( $\mu$ H)	DCR ( $\Omega$ )	Ohmic Loss (W)
732-4237-1-ND	8.03	22	0.007	0.175
732-2179-1-ND	6.4	47	0.0335	0.8375
732-2177-1-ND	6.4	22	0.0146	0.365

## Appendix F MOSFETs

Table 2 lists MOSFETs that meet the constraints outlined in 3.4.4 on 7. For each one the power losses  $P_{LOSS}$  and  $P_{LOSS\_LDO}$  were calculated.

**Table 2:** Possible choices for MOSFETs

$R_{DS(on)}$	$Q_{GD}$	$Q_{GS}$	$R_G$	$V_{GSTHR}$	Ohmic Loss	Transision Loss	Total Loss	Drive Loss
0.0032	4	2.5	0.4	2.5	0.104	1.0296	1.1336	0.806
0.0039	7	9	2.4	3.3	0.12675	4.8384	4.96515	1.984
0.0042	7	9	2.4	3.3	0.1365	4.8384	4.9749	1.984
0.008	2	4.5	3	2	0.26	2.2464	2.5064	0.558
0.0067	5.3	3.9	1.5	1	0.21775	2.18592	2.40367	0.7998
<b>0.0093</b>	<b>2</b>	<b>4.9</b>	<b>1</b>	<b>2</b>	<b>0.30225</b>	<b>1.39104</b>	<b>1.69329</b>	<b>1.488</b>
0.019	8	4	1.3	2	0.6175	2.6784	3.2959	1.798
0.0095	7.5	6	1	3	0.30875	2.7216	3.03035	1.736

The MOSFET highlighted in grey was selected. Though it is not the best model, it is a lot cheaper than the best fit and has better documentation. The same MOSFET is used for both the low-side and the high-side switch.

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