Project 5 – Sensor-Microchip

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In his Master Thesis *Sensor Chip* from 2015, Tobias Burgherr developed a sensor integrated circuit as a base for further projects to use. This IC consists of a programmable pre-amplifier and a sigma-delta analog-to-digital converter with adjustable bandwidth. Typically, sigma-delta ADCs use an internal 1-bit quantizer which gets boosted to the desired resolution of bits via delta-sigma modulation. The goal of his work was to replace the 1-bit quantizer with a successive approximation register (SAR) ADC capable of converting 3 bits at a time instead of 1. This method was referred to as a "Multi-bit quantizer". A complementary 3-bit DAC was also developed to be used internally in the feedback loop of the sigma-delta modulator. Based on his work, two teams modified the existing chip in 2016.

In 2016, Roger Gloor and Patrick Walther modified the preamp in their thesis *Re-Design eines integrierten Verstärkers für einen AD-Wandler-IC*, while Marcel Baier and Kevin Niffenegger worked on the ADC in their thesis *Sensor-Chip mit Sub-SAR-ADC*.

These two projects yielded one redesigned chip each, which are now coming back from fabrication. Our main objectives in this project will broadly be as follows:

- Measure and assess the performance of both chips.
- Examine and understand more closely the chip by Baier and Niffenegger, and propose potential improvements for it.

Microchip design is a rather exotic field, and opportunities to actually understand and work on a microchip are therefore rare. Both of us have been interested in electronics and computers for a long time, and feel compelled to use this opportunity to look under the hood, so to speak.

We seek to answer the following questions with this project:

- Have the design changes by Gloor and Walther brought the desired improvements?
- Is the design choice by Baier and Nyffenegger, which is highly experimental by their own admission, a worthwile path to pursue?

Improving the chip by Baier and Niffenegger will be the main focus of next semester's project, which is why this project's focus is somewhat biased towards that chip.

In a first stage, our main task will be to familiarise ourselves with the fundamental concepts such as sigma-delta ADCs and SAR ADCs, as well as the specific implementations used by the previous teams. They have provided extensive documentation for this. This is particularly important for Baier's and Niffenegger's design, since understanding the system more closely is required for determining what to do with that chip in stage two of our project.

In a second stage, we will measure various properties of the two chips. For the chip by Gloor and Walther, this will mean examining their implementation of the preamp stage (gain, speed, bandwidth, power consumption, ...). For the chip by Baier and Niffenegger, the relevant characteristics cannot be determined with certainty at this point (see above). This will be done once we have familiarised ourselves with the system to judge what is and what is not relevant to assess its performance, and what sorts of tests need to be performed to gain these insights.

In a third stage, the chip by Baier and Niffenegger will be examined more closely for ways in which to further improve upon its design. These conclusions will be the starting point for next

semester's project, where we will simulate and design a new chip based on our conclusions from this semester.

The primary resources will be the documentation provided by the previous teams, the book *Analog Circuit Design* used in the course *Analog Circuits* as well as any supplementary information as needed.

This project is commissioned and supervised by Alex Huber and Hanspeter Schmid of the Institute of Microelectronics. They are its main addressees, along with ourselves and anyone else who will continue this project's work. All relevant documents will be written in English.

Time mismanagement is the primary danger to this project's success. The chip by Gloor and Walther will likely be easier to measure. However, the chip by Baier and Niffenegger will be the foundation for next semester's project, so spending too much time on the first chip will have a direct negative impact on the continuation of this project. It is therefore crucial to properly plan.

Additionally, there is a possibility of equipment being faulty or damaged (either by somebody else or by us), causing significant delays.

Lastly, it could be that either one or both chips do not function correctly or even at all (faulty manufacturing, damage by handling, ...). Should that be the case, depending of the severity of the damage, this might cause delays or prevent us from carrying out the desired measurements on the chip entirely. To determine the course of action, we would consult with our advisers in this case.

At this point, no detailled timetable has been fixed yet. It is our intention to do so by Monday, October 10, 2016.