EXPERIMENT: 7.1
EXAMINATION OF FSK (FREQUENCY SHIFT KEYING) MODULATION

PREPARATORY INFORMATION

FSK modulation is a digital communication method used in industry generally. The data signal is modulated to a signal with two different frequencies in FSK method. When the data signal is **"1"** (ONE), FSK signal frequency is called F1, and when the data signal is **"0"** (ZERO), FSK signal frequency is called F2. When the data signal is **"1"**, FSK signal frequency is called sign signal frequency and when the data signal is **"0"**, FSK signal frequency is called blanking pulse frequency. Bit transmission velocity and baud transmission velocity in FSK modulator are equal to each other. The data signal and FSK modulated signaş for the same time frame are shown in Figure 7.1.1.

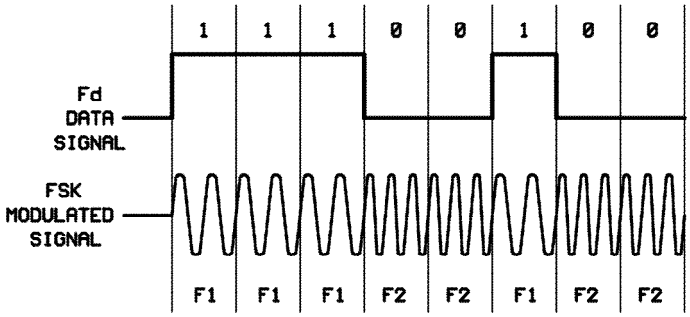


Figure 7.1.1

The difference between F1 and F2 frequencies must be as great as possible for a quality communication. FSK frequencies are constant in certain applications. As an example, sign signal in wireless communication is 2124Hz, blanking pulse is 2975Hz. In cable communication, sign signal is 1070Hz, blanking pulse is 1270Hz or sign signal is 2025Hz and blanking pulse is 2225Hz. Upon the consideration of the frequency intervals, the frequency band necessary for FSK communication must be minimum 200Hz.

A signal with two different frequencies where the data signal is modulated can be generated by using voltage controlled oscillator (**VCO**). The frequencies of the output signal changes as directly proportional to the voltage difference where the data signal is "**0**" and "**1**".

As an example, when the data signal is **"1"**, let the difference between F1 and F2 frequencies to be 200Hz at the modulator output when the amplitude is 5V DC. If we make the amplitude 8V DC when the DATA signal is "**1**", the differences between F1 and F2 frequencies of the modulator becomes greater than 200Hz.

FSK modulation can also be regarded as a system where the voltage level of a digital signal is converted to a frequency. F1 and F2 frequencies used in FSK modulation are values between 800Hz-2500Hz that could be regarded low. The frequency of the data signal is selected lower for the system to work. This value is less than F1/5 in applications. A FSK modulator made by VCO is shown in Figure 7.1.2.

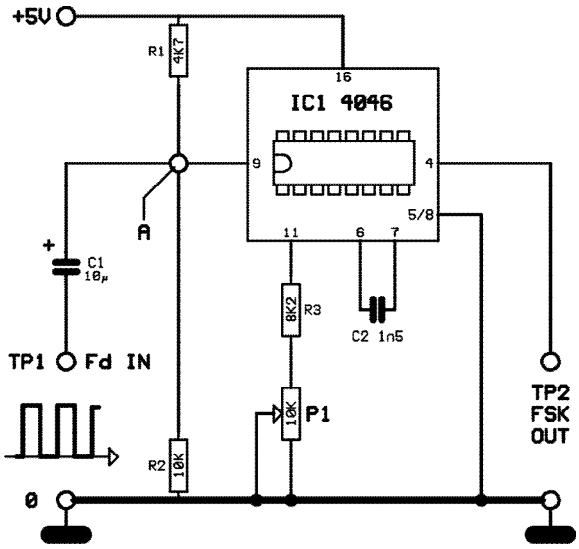


Figure 7.1.2

Voltage controlled oscillators are used most frequently today because their assembly is easy and they have few peripheral components. Voltage controlled oscillators are integrated circuits. There are voltage controlled oscillators whose output signs are square, triangle and sine simultaneously.

IC1=4046 integration consists of one VCO and two PHASE COMPARATORs. VCO section of 4046 and the terminal connections of this section are shown in Figure 7.1.3.

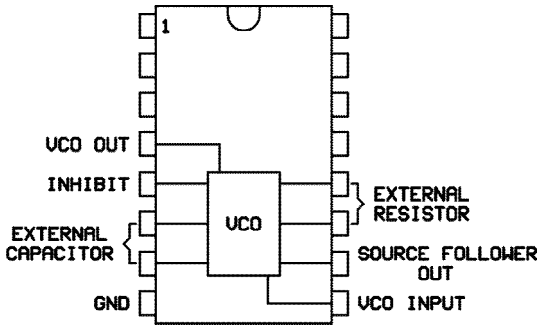


Figure 7.1.3

The output sign of the data signal 4046 applied to VCO input terminal is received from VCO output terminal. When there is no signal at VCO input terminal, in other words, when DATA signal (Fd) is "**0**", a square wave signal is generated at VCO output terminal which is determined by C2 capacitor, R3 resistor and P1 potentiometer values. The frequency of this signal can be adjusted at certain intervals by P1 potentiometer. If DATA signal (Fd) is applied to the circuit, the frequency of the sign at the output terminal of VCO increases when DATA signal is "**1**". The magnitude of this increase is directly proportional to the amplitude of DATA signal.

When looked closely, F1<F2 in FSK signal that is mentioned at the beginning. This setback doesn't cause a problem in the experiment. This setback can be fixed by using an INVERT door at the demodulator output if desired.

EXPERIMENTAL PROCEDURE

Mount Y-0024/007 module at its place. Make the circuit connections as shown in Figure 7.1.4. Apply energy to the circuit.

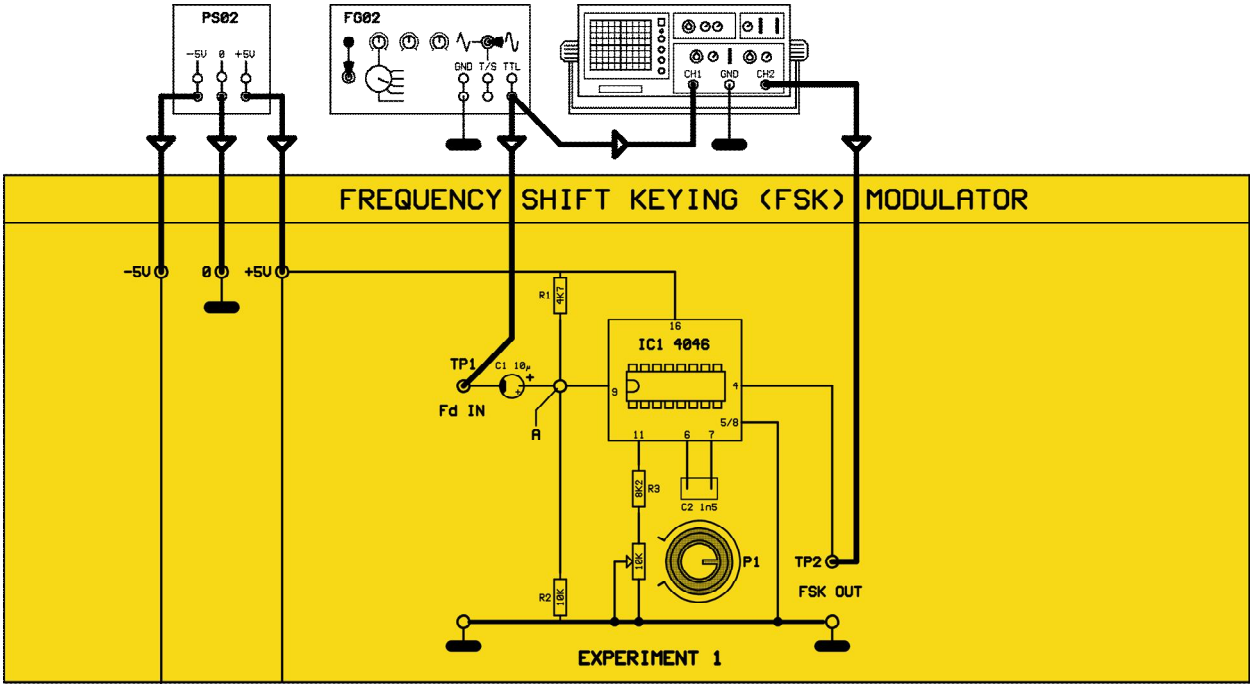
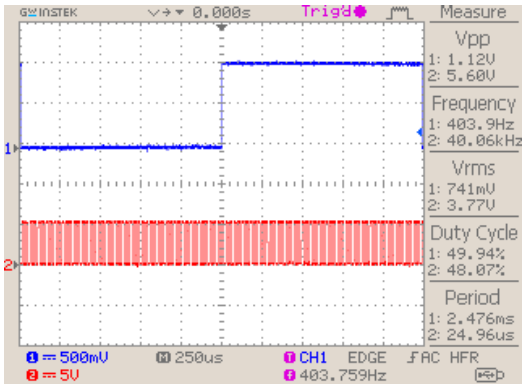


Figure 7.1.4

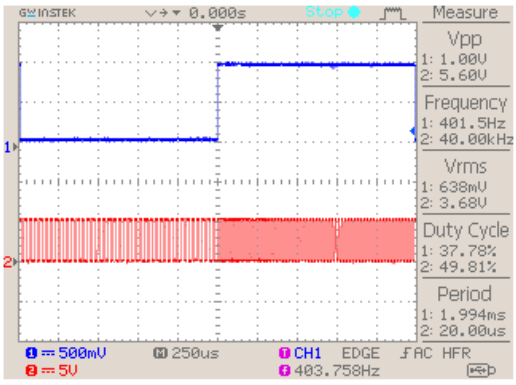
1. Adjust the output sign of the function generator Fd=400Hz and its amplitude to 1Vpp. Separate the signal input from Fd IN (TP1) socket. Connect CH2 channel to Fd OUT (TP2) socket. At this moment, adjust P1 potentiometer until you see 40KHz at FSK OUT (TP2) socket. See the shapes of the two signs.



2. Apply +5V to VCO input socket (point A). Write down the sign shift seen at FSK OUT (TP2) socket.

The frequency of the sign at FSK OUT (TP2) socket increased to approximately 50KHz. There is no change in the amplitude of the sign.

3. Separate +5V at VCO input socket. Connect the output of the function generator to Fd IN (TP1) socket and see the shapes of the two signs and interpret them.



FSK was generated at FSK OUT (TP2) socket which is the modulator output. When Fd (DATA) is "0", the frequency of VCO decreased in time frames and when Fd (DATA) is "1", VCO frequency increased.

EXPERIMENT: 7.2
EXAMINATION OF FSK DEMODULATION

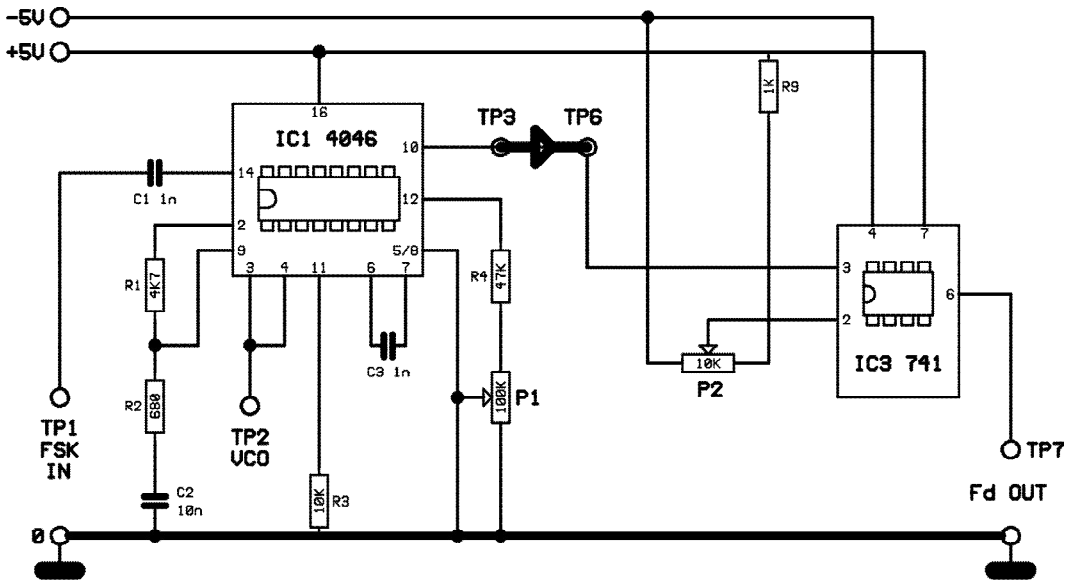


Figure 7.2.1

A FSK demodulator made by phase lock shift method is shown in Figure 7.2.1. Three circuits are necessary for making phase lock shift basically. These are;

1- PHASE COMPARATOR
2- VCO=VOLTAGE CONTROLLED OSCILLATOR
3- LPF=LOW PASS FILTER.

IC1=4046 is an integration consisting of two phase comparators and one VCO. The terminal connection and inner structure of 4046 are shown in Figure 7.2.2.

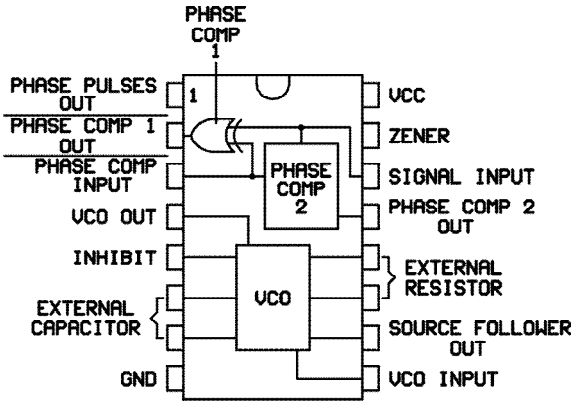


Figure 7.2.2

Operation of a phase lock shift can be understood by a simple block diagram shown in Figure 7.2.3.

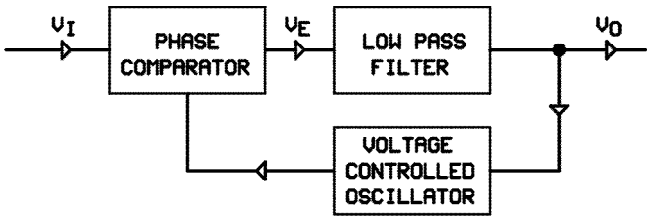


Figure 7.2.3

When there is no signal at the input terminal, voltage controlled oscillator generates a square wave signal with a frequency determined by its peripheral components. This frequency value is called free operation frequency or center frequency (Fo). This signal is applied to the phase comparator. When a signal is applied to the input terminal, the phase comparator compares these two signals and a third signal made of a pulse series is obtained. This signal is called ERROR signal. The signals applied to the comparator determine the phase and frequency of the error signal. The error signal has the direct voltage characteristics. The error signal is designated by VE. The error signal passes through the low pass filter and then it is applied to VCO input.

If the input signal frequency decreases, the error voltage forces to decrease the frequency of voltage controlled oscillator. When the frequency of voltage controlled oscillator approximates sufficiently to the input signal frequency, phase lock shift occurs. The frequencies of the two signs become equal at this moment. A very short time passes for locking during operation.

If the input signal frequency increases, the error voltage forces to increase the frequency of voltage controlled oscillator. When the frequency of voltage controlled oscillator approximates sufficiently to the input signal frequency, again phase lock shift occurs.

If the frequency of the sign at the inputs of PLL circuits is changed within the scope of band that is locked, a voltage is obtained whose amplitude at the output terminals is directly proportional to their frequency. In other words, PLL circuit works like a Frequency/Voltage converter within this frequency interval. This characteristic ensures PLL circuits to be used as a frequency demodulator.

In FSK demodulator circuit in Figure 7.2.1, values of R3 and R4 resistors, P1 potentiometer and C3 capacitor determine the free operation frequency of voltage controlled oscillator. Free operation frequency can be changed within a certain interval by P1 potentiometer. R2 resistor and C2 capacitor works as a low pass filter of VCO.

IC2=741 integration is an operational amplifier working as a non-inverting COMPARATOR in the circuit. The terminal connection of 741 and its symbol used in electronic circuit schemes are shown in Figure 7.2.4.

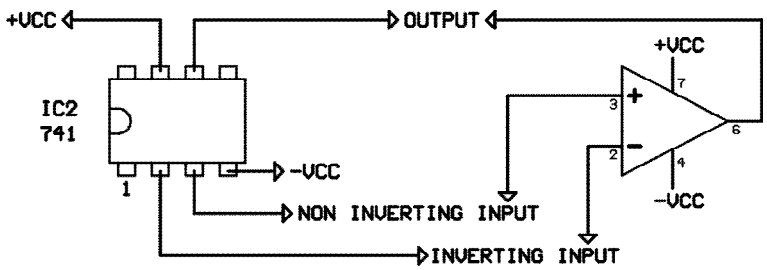


Figure 7.2.4

In the circuit in Figure 7.2.1, bias of no.2 input terminal of the operational amplifier is adjusted by P2 potentiometer. This adjusted value is called "reference voltage". If the amplitude of the sign coming from phase lock shift is greater than its reference voltage, a sign whose resource voltage is close to its positive value is obtained at the output terminal of the comparator. If the amplitude of the sign coming from phase lock shift is smaller than the reference voltage, a sign is obtained close to the positive value of the resource voltage at the output terminal of the comparator. In other words, the amplitude of the sign with small amplitude coming from comparator phase lock shift is increased sufficiently.

The sign obtained at the output of the comparator is a data sign (Fd).

EXPERIMENTAL PROCEDURE

Plug Y-0048/09 module. Make the circuit connections as in Figure 7.2.5. Give energy to the circuit.

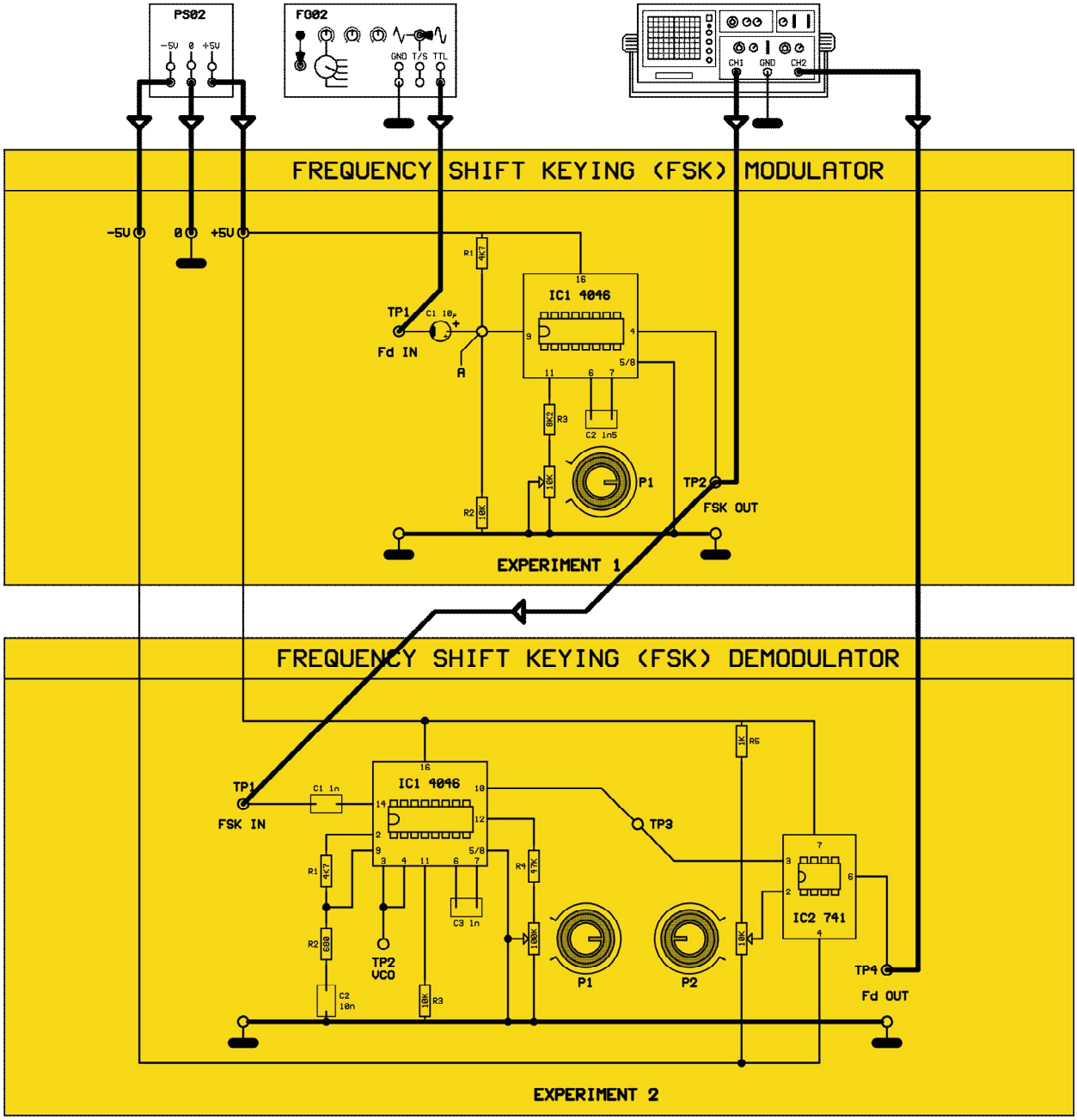
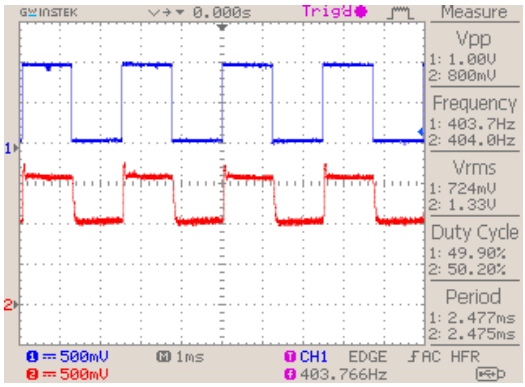
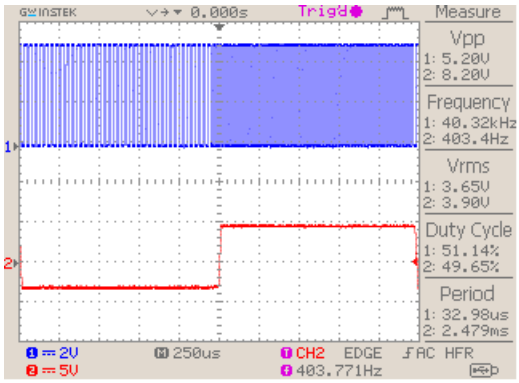


Figure 7.2.5

1. Connect CH1 channel of oscilloscope to FSK IN (TP1) socket of the demodulator and CH2 channel to PLL OUT (TP3) socket. Adjust P1 potentiometer of the demodulator until you obtain a square wave sign without distortion or minimum distortion at TP3 socket. See the two signs.

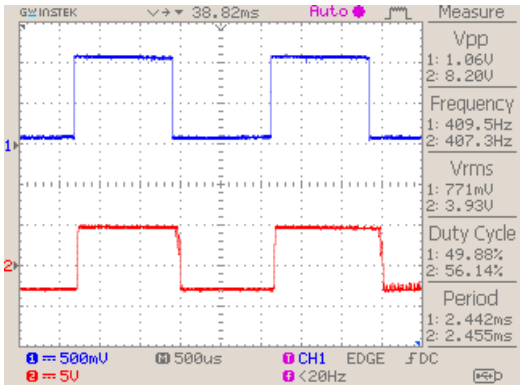


2. Connect CH2 channel of oscilloscope to Fd OUT (TP4) socket. Adjust P2 potentiometer until you see a square wave at (TP4) socket. See the two signs and interpret them.



*When FSK sign frequency is low, (TP4) sign is **"0"**. When FSK sign frequency is high, Fd OUT (TP4) sign is **"1"**. The amplitude of Fd OUT (TP4) sign is over +5V with the effect of the comparator.*

3. Connect CH1 channel of oscilloscope to Fd IN (TP1) socket of FSK modulator and CH2 channel of oscilloscope to Fd OUT (TP4) socket of the demodulator. See the two signs simultaneously and interpret them.



A data signal is obtained at Fd OUT (TP4) socket of the demodulator.