EE463 – Term Project:
AC to DC Motor Drive
Simulation Presentation

-Group Power Quality-

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Outline

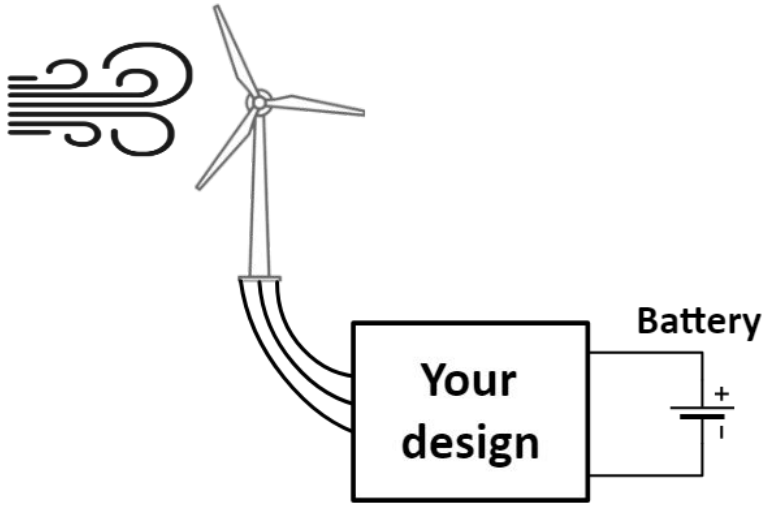
1. Introduction & Specifications
2. Topology Selection
3. Analytical Calculations
4. Component Selection
5. Simulation Results
6. Controller Discussion
7. PCB Design
8. References

1. Introduction & Specifications

Aim: to design an AC to DC motor drive to illuminate the street by the use of a wind turbine generator and a battery.

Specifications:

- **Open circuit voltage peak**: 330 $V_{line\text{-}to\text{-}line}$
- **Battery capacity**: 13 Ah
- **Battery nominal voltage**: 24 V
- **Output current**: 2 A
- **Output current ripple**: %20 of average current
- **Inertia**: 0.00027 kg.m^2
- **Viscous Damping**: 0.005024 N.m.s
- **Poles**: 2
- **Voltage Constant**: 110 Vpeakl-l/krpm
- **Stator Resistance**: 10.58 Ohm
- **Armature Inductance**: 16.7 mH



2. Topology Selection

- The practical implementations on the market limits our options by two:

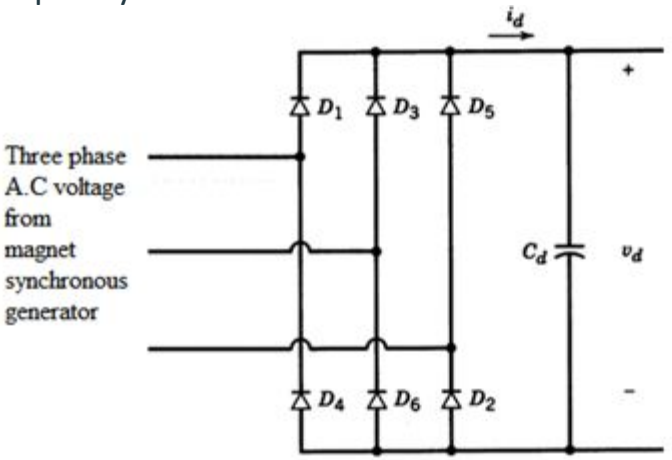
  (as given in the project description)

a. **Diode Rectifier and Buck Converter**

b. **Three-Phase Thyristor Rectifier**

2. Topology Selection
a. Three-Phase Full-Bridge Diode Rectifier and Buck Converter

- two universal bridges at the input side, each has two bridge arms
- a rectifier capacitor at the outputs of the bridges
- a buck converter for lowering the DC output of the rectifier
- by a switching tool of MOSFET
- a capacitor and inductor in series at the output
- a control mechanism for the determination of the switching frequency of MOSFET
- a PWM signal from a controller, analog or microcontroller
- amplitude of PWM signal does not exceed 5V.
- PWM circuit should be isolated from the main power side.



2. Topology Selection
a. Three-Phase Full-Bridge Diode Rectifier and Buck Converter

Pros

a. *Output ripples can be controlled by the output L filter.*

b. *The switching frequency can be controlled easily.*

c. *The efficiency is relatively high.*

Cons

a. *The losses may be high when high frequency switching is used.*

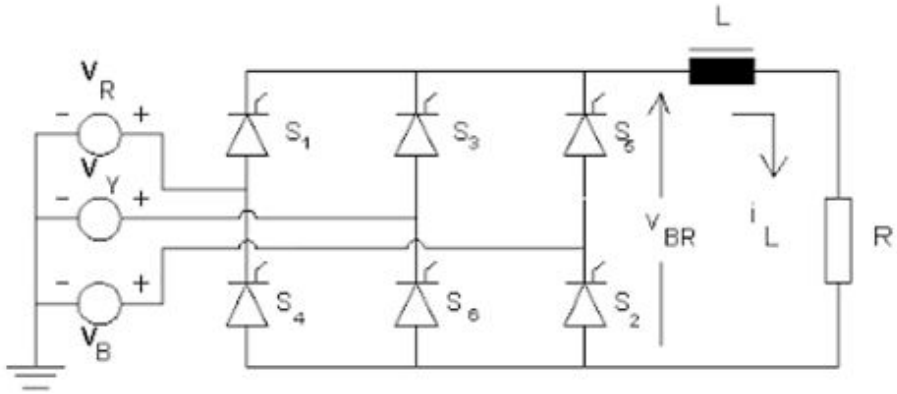
b. *The complexity is relatively high, by means of the number of components.*

c. *The cost may be high as a result of part b.*

d. *One should consider the discontinuous conduction mode of the converter.*

2. Topology Selection
a. Three-Phase Thyristor Rectifier

- six thyristors
- for each gate, PWM signals with 120 degrees of phase shift
- firing angle is arranged
- a control circuitry for gate signals.
- desired negligible ripple without any buck/boost converter or capacitor
- synchronization problem
- controller has to be in phase with the AC input part



2. Topology Selection
a. Three-Phase Thyristor Rectifier

Pros

a. *Output ripples are lower.*

b. *No need for output LC filtering.*

c. *Output voltage is relatively high.*

d. *The efficiency is relatively high*

Cons

a. *Need for a much complicated control circuit for synchronization.*

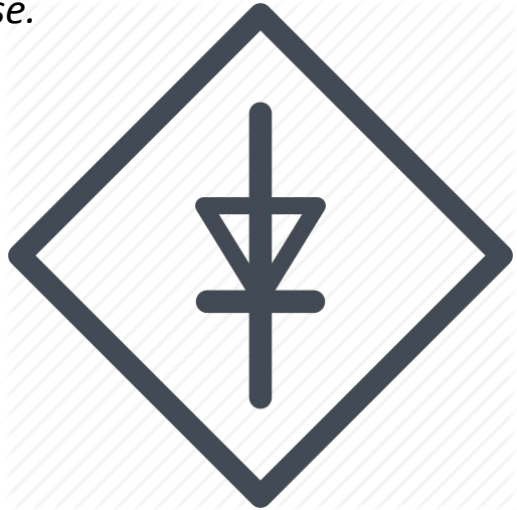
b. *Low power and discrete power factor.*

2. Topology Selection
Decision & Design Considerations

Three-Phase Full-Bridge Diode Rectifier and Buck Converter is selected.

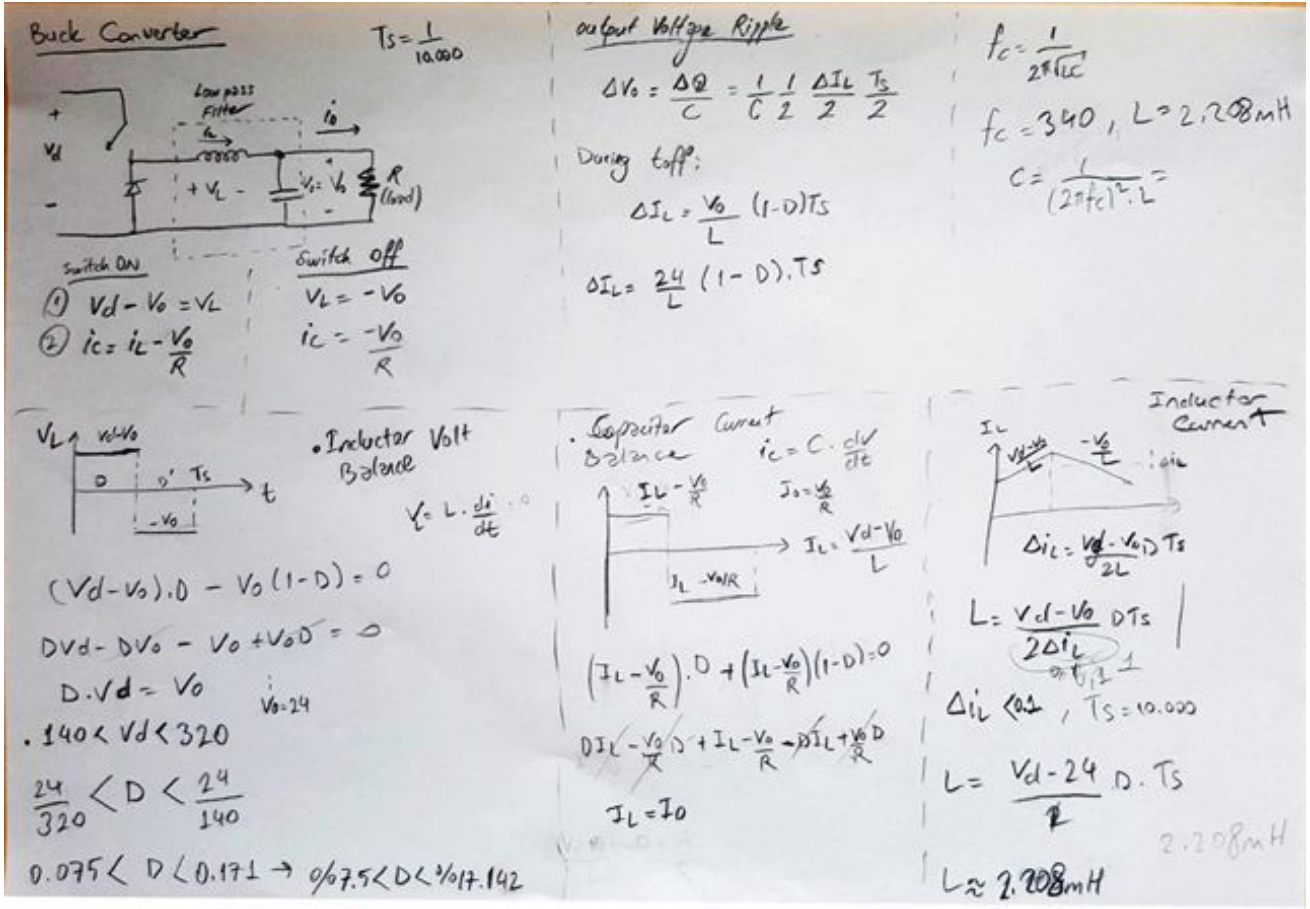
- *The available components in the market are much more diverse.*
- *The frequency range is much broader.*
- *So the output ripple can be adjusted more precisely.*
- *Relatively cheap if we sacrifice from the low output ripple.*
- *For high duty cycle values, it is more efficient*

(which may be the case in our project)



3. Analytical Calculations

(our scratch paper)



3. Analytical Calculations

(our Matlab script)

```
Vout = 24;

Vin = 300; %It will be in a range e.g. 150 to 330V

i_out = 2;

fs = 50000; %switching frequency

fc = 339; %Corner frequency for LC filter

delta_i = 0.2*i_out; %Desired inductor ripple current

delta_Vo = 0.05; %Desired peak to peak output voltage

D = Vout/Vin; %Duty cycle will also be in a range due to Vin variance

L = Vout*(1-D)/(fs*delta_i); %Inductor sizing

C = 1/(((2*pi*fc)^2)*L); %Capacitor sizing related to corner frequency

% C = delta_i/(8*fs*delta_Vo); %Capacitor sizing

Diode_size = i_out*(1-D); %V30K45, shotky
```

4. Component Selection

1. ***Bridge Rectifiers:*** *Z4DGP406L-HF* ***[1]***
2. ***Buck-Capacitor:*** *EEE-FP1V220AR* ***[2]***
3. ***Rectifier-Out Capacitor (DC Link Capacitor):*** *UVZ2G221MRD* ***[3]***
4. ***Current Measurement Resistor:*** *PE0603DRF570R01L* ***[4]***
5. ***Buck MOSFETs:*** *FDT3N40TF* ***[5]***
6. ***Buck Inductor:*** *744822222* ***[6]***
7. ***Controller:*** *LM5117* ***[7]***

4.1. Component Selection - **Bridge Rectifiers** - Z4DGP406L-H

$ 1.03

Parameter	Symbol	Z4DGP406L-HF	Unit
Repetitive Peak Reverse Voltage	V_{RRM}	600	V
Average Forward Current	$I_{(AV)}$	4.0	A
Peak Forward Surge Current, 8.3mS single half sine-wave, superimposed on rated load (JEDEC Method)	I_{FSM}	150	A
Operating Junction Temperature Range	T_J	-55 to +175	°C
Storage Temperature Range	T_{STG}	-55 to +175	°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	IF = 2.0A IF = 4.0A	- -	0.86 0.90	0.90 0.95	V
Repetitive peak reverse current	I_{RRM}	V_R=Max. V_{RRM}, Ta=25°C	-	0.08	5	μA
Current squared time	I^2t	t<8.3ms, Ta = 25°C	-	93.38	-	A^2S
Junction capacitance	C_J	V_R=4V, f=1.0MHz	-	45	-	pF
Thermal resistance	$R_{\theta JA}$	Junction to ambient (Note)	-	35	-	°C/W
	$R_{\theta JL}$	Junction to lead	-	15	-	°C/W
	$R_{\theta JC}$	Junction to case	-	10	-	°C/W

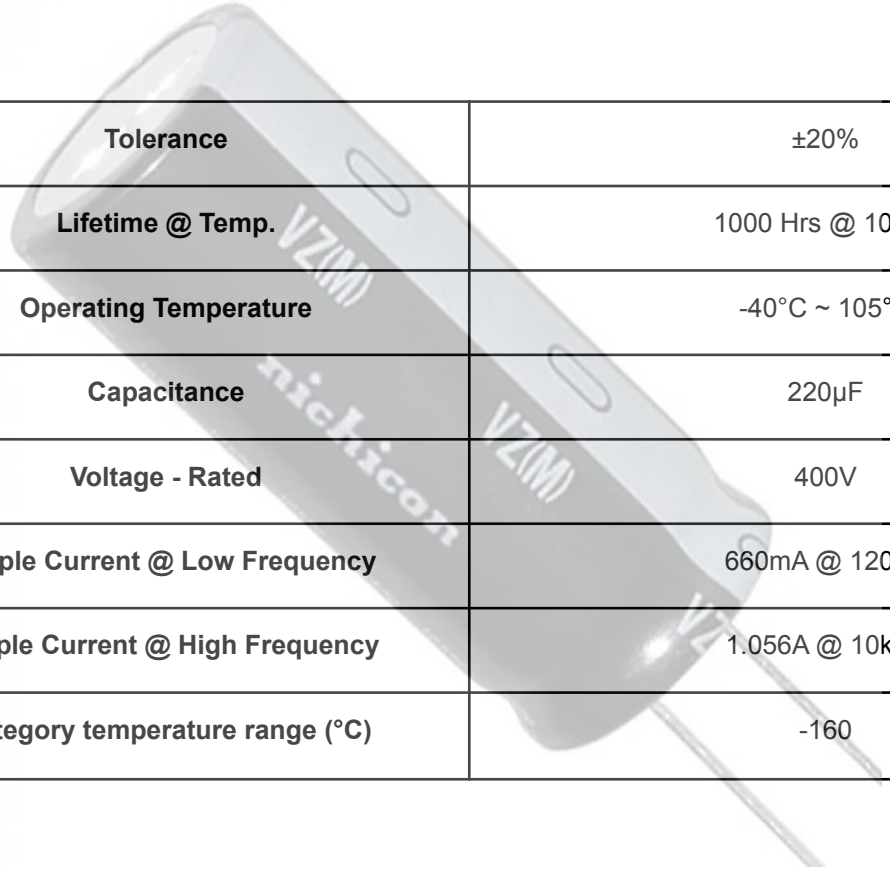
4.2. Component Selection - **Buck-Capacitor** - EEE-FP1V220AR

$ 0.43

Body shape	Surface mount type (vertical mount style)
Polarity type	Polar
Rated voltage (V)	35
Capacitance (µF)	22
Tolerance on capacitance (%)	-40
Tangent of loss angle (max.)	0.12
Leakage current (max.) (µA)	7.7
Category temperature range (°C)	-160

4.3. Component Selection - **DC Link Capacitor** - UVZ2G221MRD

$ 4.23

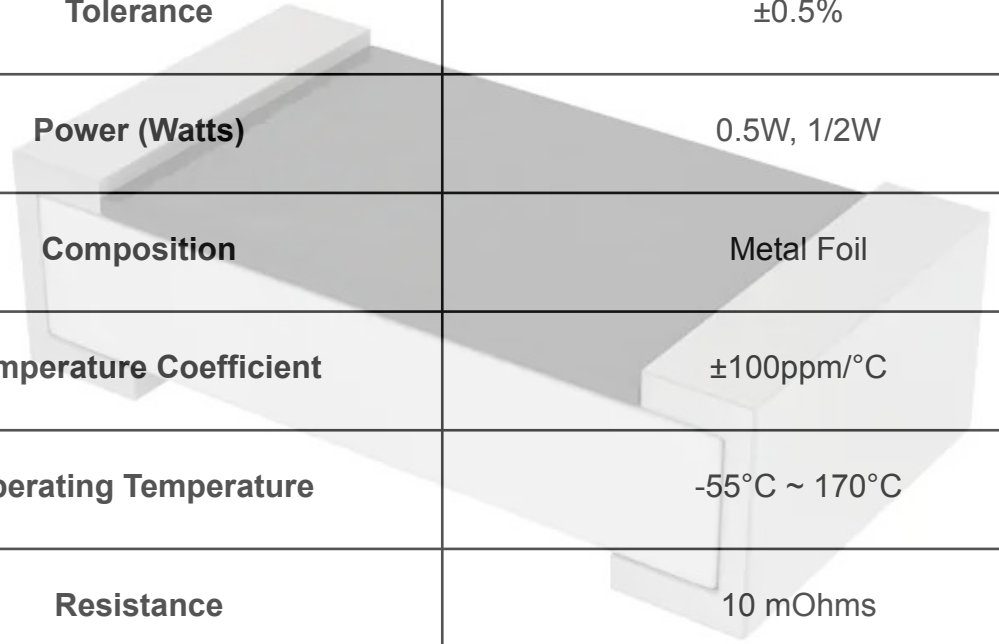


Tolerance	±20%
Lifetime @ Temp.	1000 Hrs @ 105°C
Operating Temperature	-40°C ~ 105°C
Capacitance	220µF
Voltage - Rated	400V
Ripple Current @ Low Frequency	660mA @ 120Hz
Ripple Current @ High Frequency	1.056A @ 10kHz
Category temperature range (°C)	-160

4.4. Component Selection-**Current Measurement Resistor**-PE0603DRF570R0

$ 0.07

Tolerance	±0.5%
Power (Watts)	0.5W, 1/2W
Composition	Metal Foil
Temperature Coefficient	±100ppm/°C
Operating Temperature	-55°C ~ 170°C
Resistance	10 mOhms



4.5. Component Selection- **Buck MOSFETs** - FDT3N40TF

$ 0.65

Technology:	Si
Transistor Polarity:	N-Channel
Number of Channels:	1 Channel
Vds - Drain-Source Breakdown Voltage:	400 V
Id - Continuous Drain Current:	2 A
Rds On - Drain-Source Resistance:	2.8 Ohms
Vgs - Gate-Source Voltage:	- 30 V, + 30 V
Vgs th - Gate-Source Threshold Voltage:	5 V
Qg - Gate Charge:	4.5 nC
Minimum Operating Temperature:	- 55 C
Maximum Operating Temperature:	+ 150 C
Pd - Power Dissipation:	2 W
Channel Mode:	Enhancement
Fall Time:	25 ns
Rise Time:	30 ns
Typical Turn-Off and On Delay Time:	10 ns

4.6. Component Selection - **Buck Inductor** - 744822222

$ 4.43

Inductance:	2.2 mH
Tolerance:	30%
Maximum DC Current:	2 A
Maximum DC Resistance:	70 mOhms
Minimum Operating Temperature:	- 40 C
Maximum Operating Temperature:	+ 125 C

4.7. Component Selection - **Controller** - LM5117

$ 6

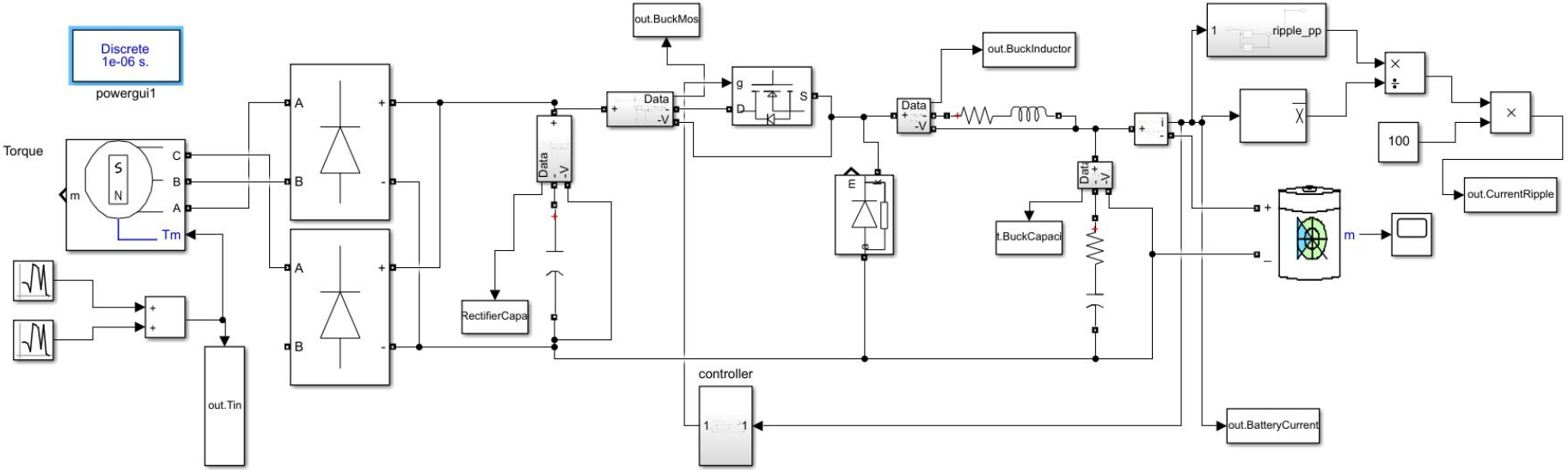
	MIN	MAX	UNIT
VIN to AGND	–0.3	75	V
SW to AGND	–3.0	75	V
HB to SW	–0.3	15	V
VCC to AGND (2)	–0.3	15	V
HO to SW	–0.3	HB + 0.3	V
LO to AGND	–0.3	VCC + 0.3	V
FB, DEMB, RES, VCCDIS, UVLO to AGND	–0.3	15	V
CM, COMP to AGND (3)	–0.3	7	V
SS, RAMP, RT to AGND	–0.3	7	V
CS, CSG, PGND, to AGND	–0.3	0.3	V
Storage Temperature, T_{stg}	–55	150	°C
Junction temperature	–40	150	°C

Absolute Ratings of LM5117

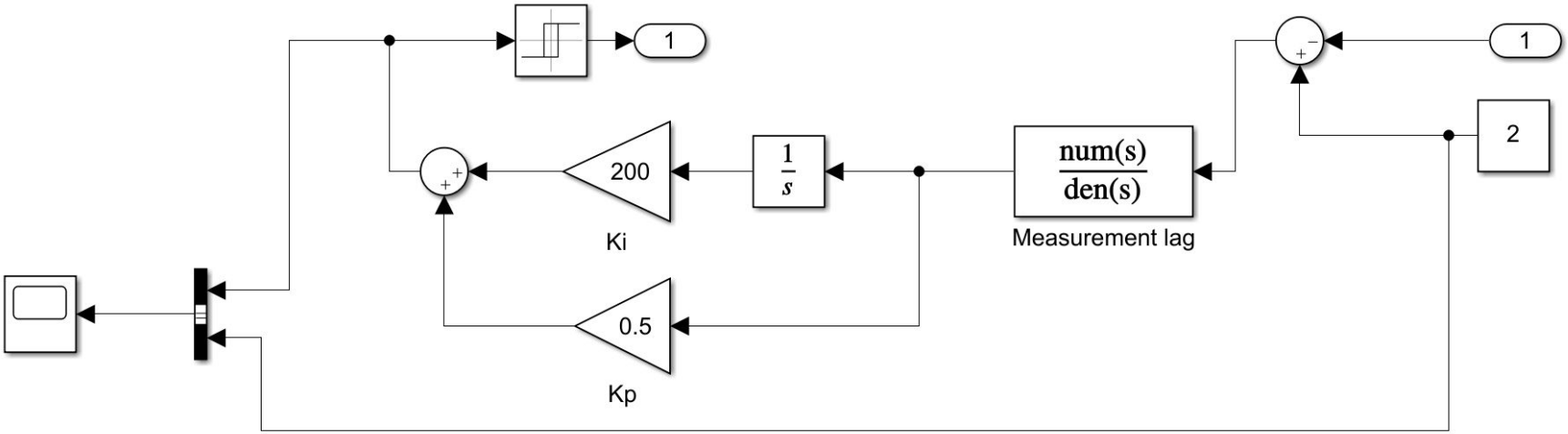
4. Component Selection - **Total Cost**

Component	Amount (#)	Total Cost (USD)
Z4DGP406L-HF	2	2.06
EEE-FP1V220AR	1	0.43
UVZ2G221MRD	1	4.23
PE0603DRF570R01L	1	0.07
FDT3N40TF	2	1.30
744822222	1	4.43
LM5117	1	6.0
Total Cost	9	$ 18.52

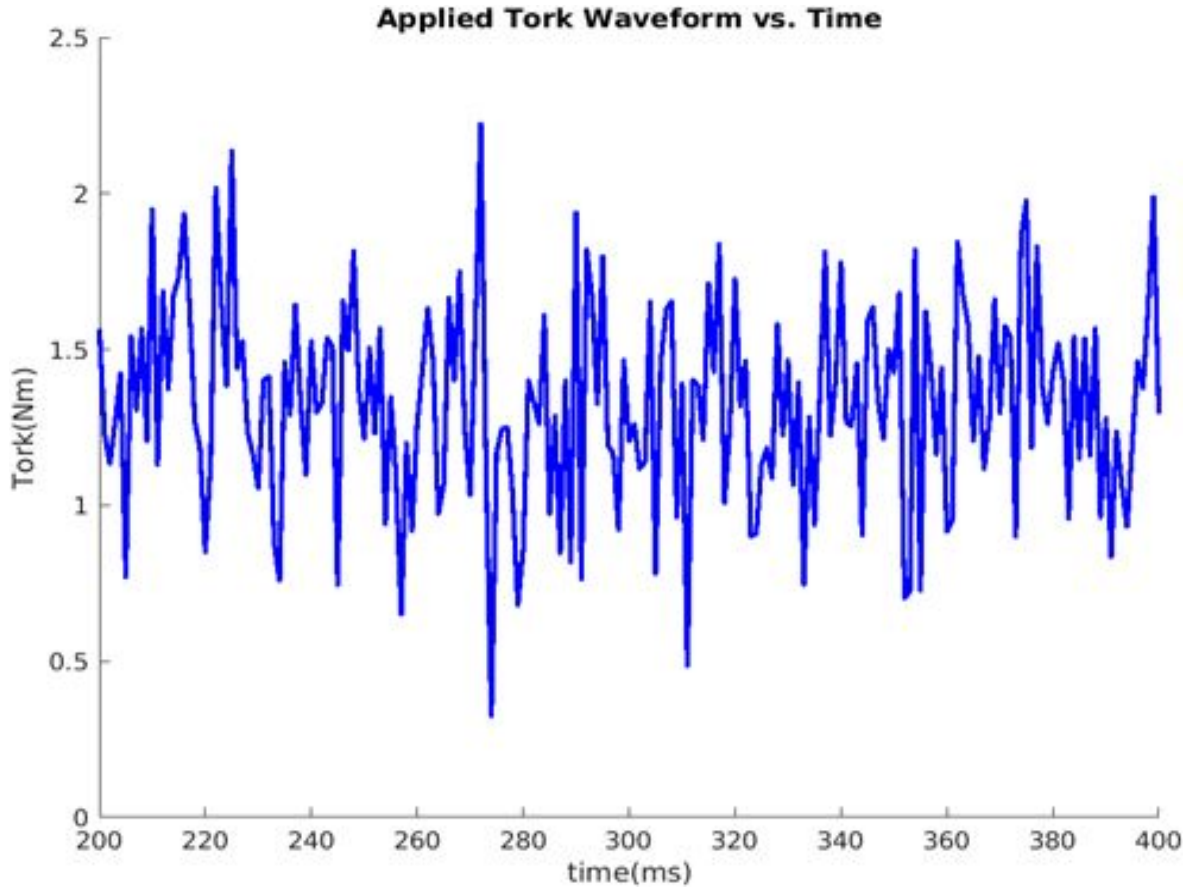
5. Simulation Results - The Schematic



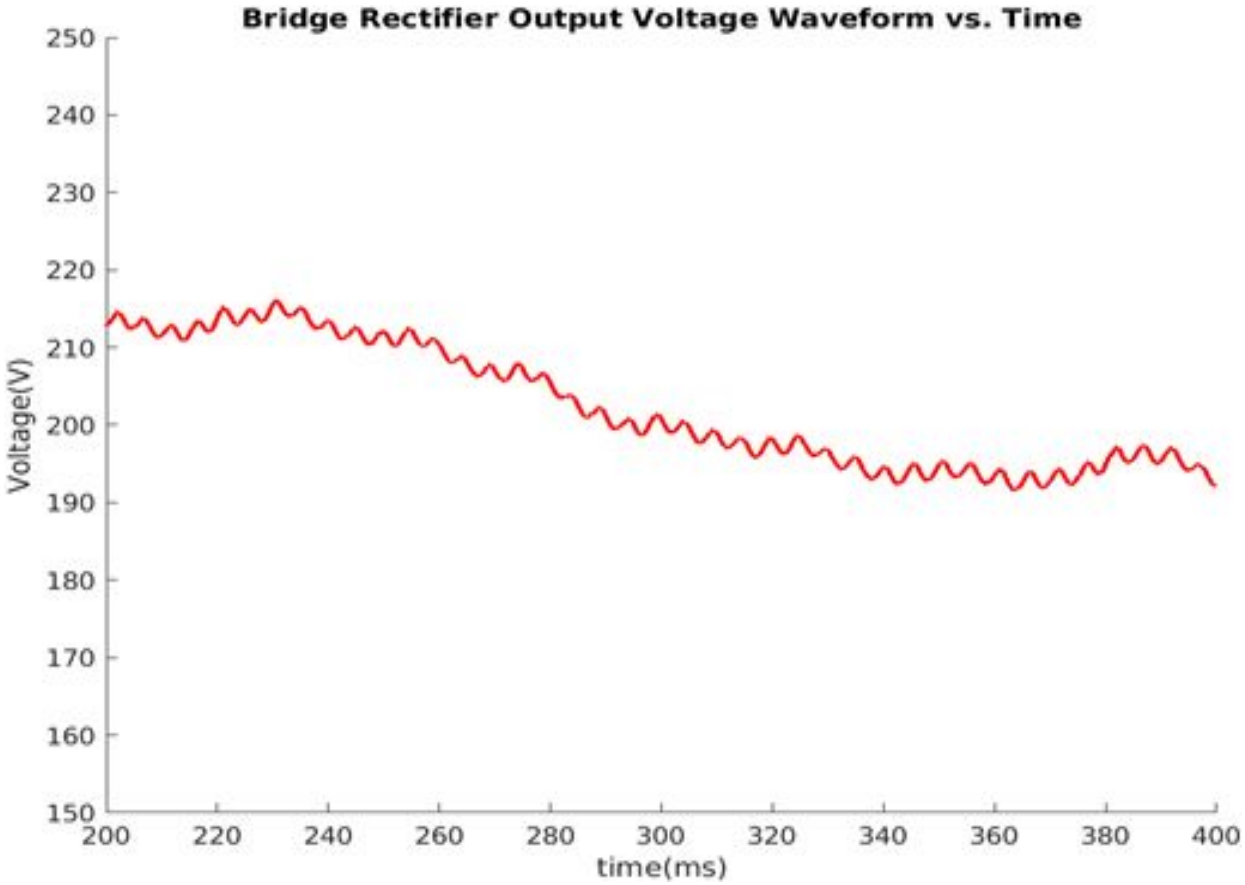
5. Simulation Results - The Schematic of Controller



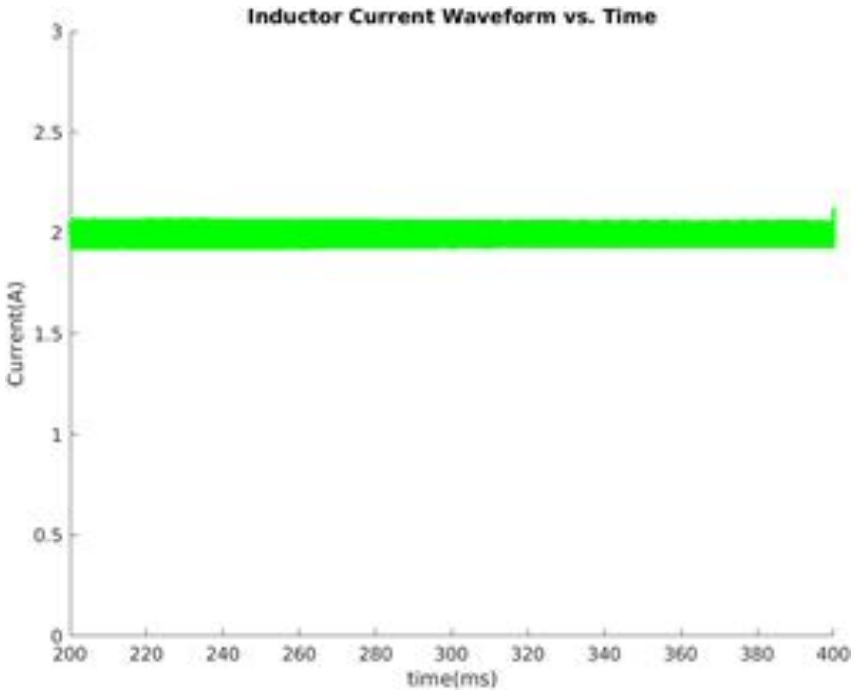
5.1. Simulation Results - **Input Torque Waveform**

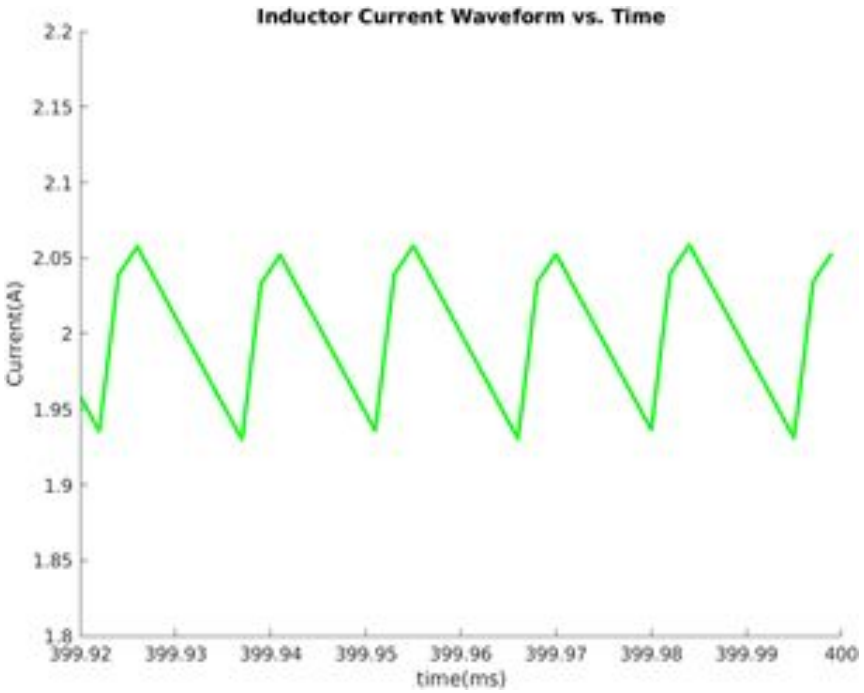


5.2. Simulation Results - **Bridge Rectifier Output Voltage**

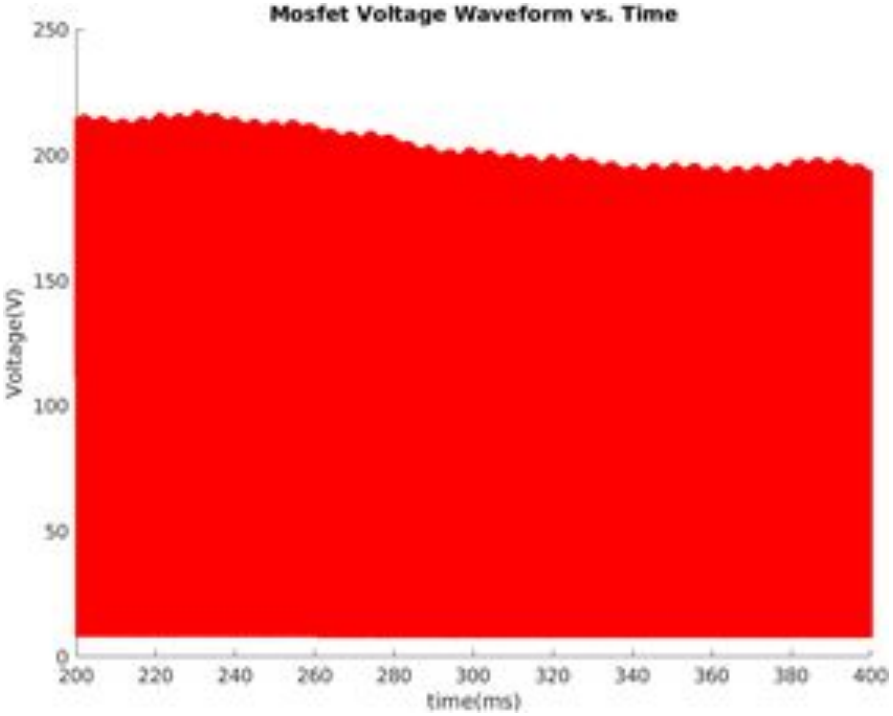


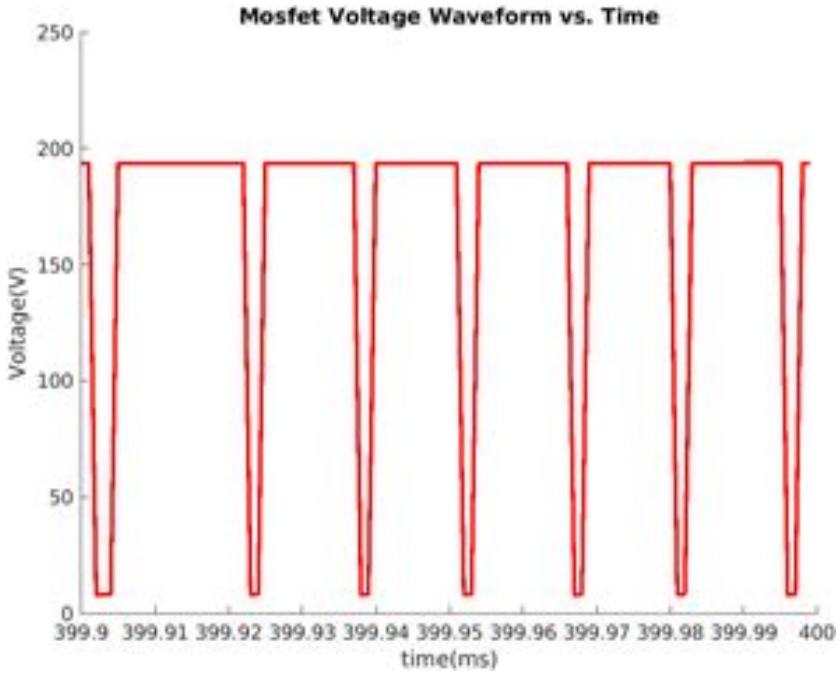
5.3. Simulation Results - **Inductor Current Waveform**



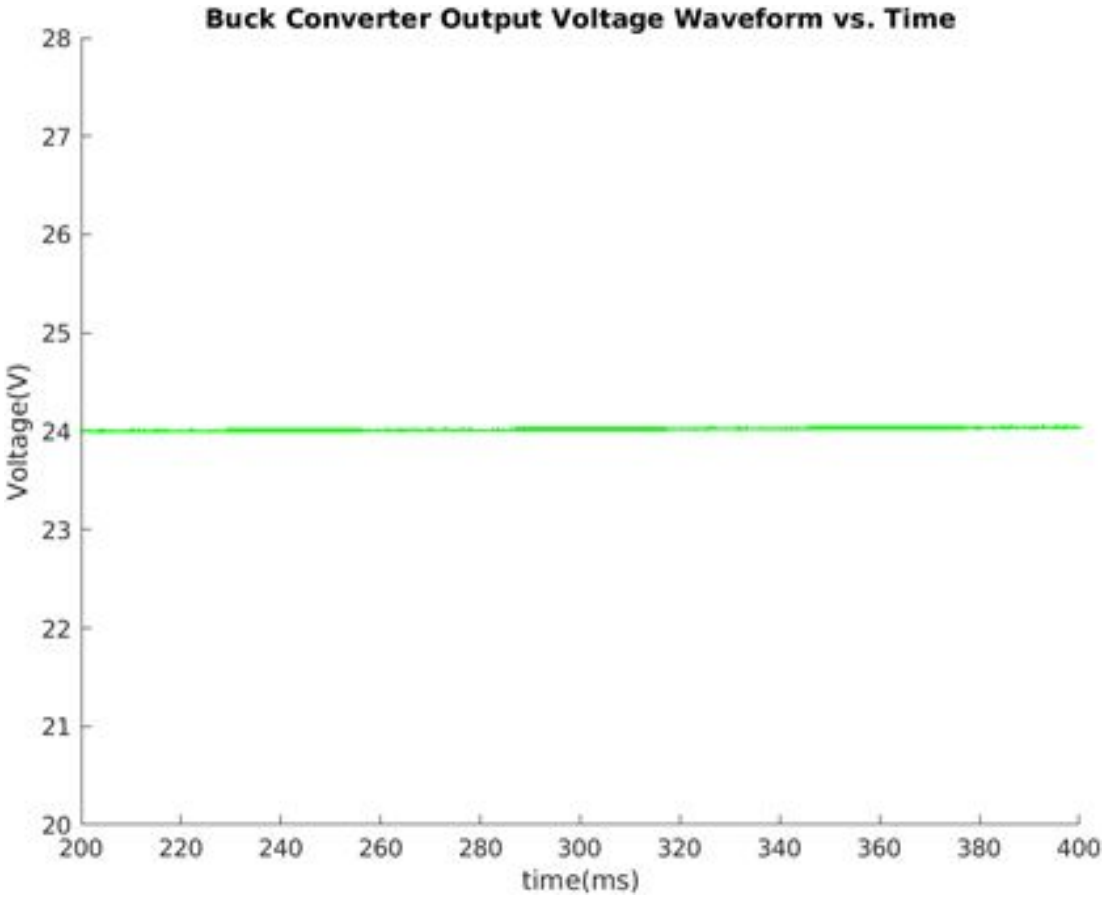


5.4. Simulation Results - **MOSFET Voltage Waveform**

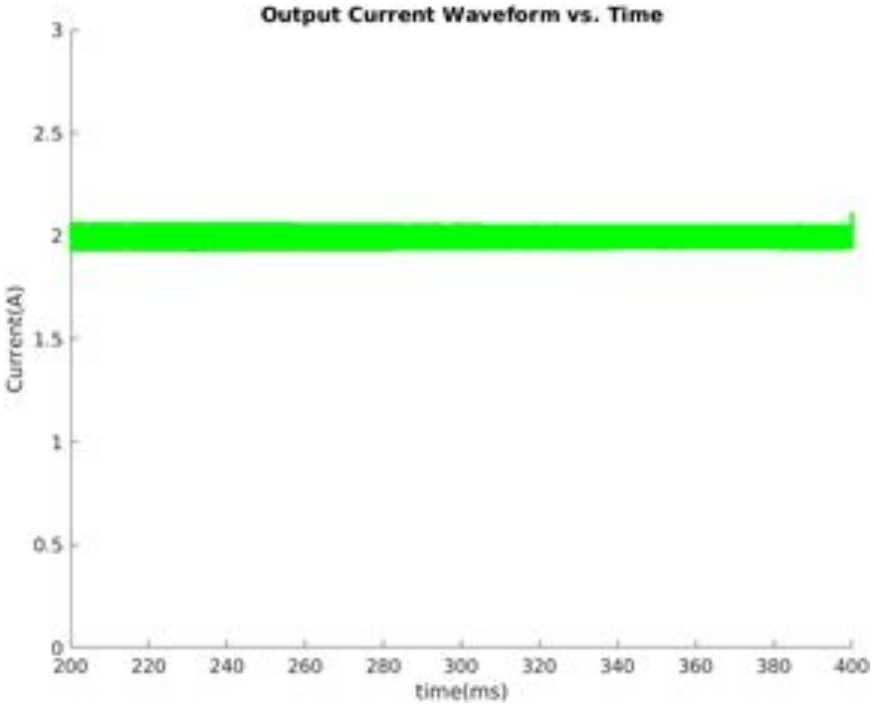


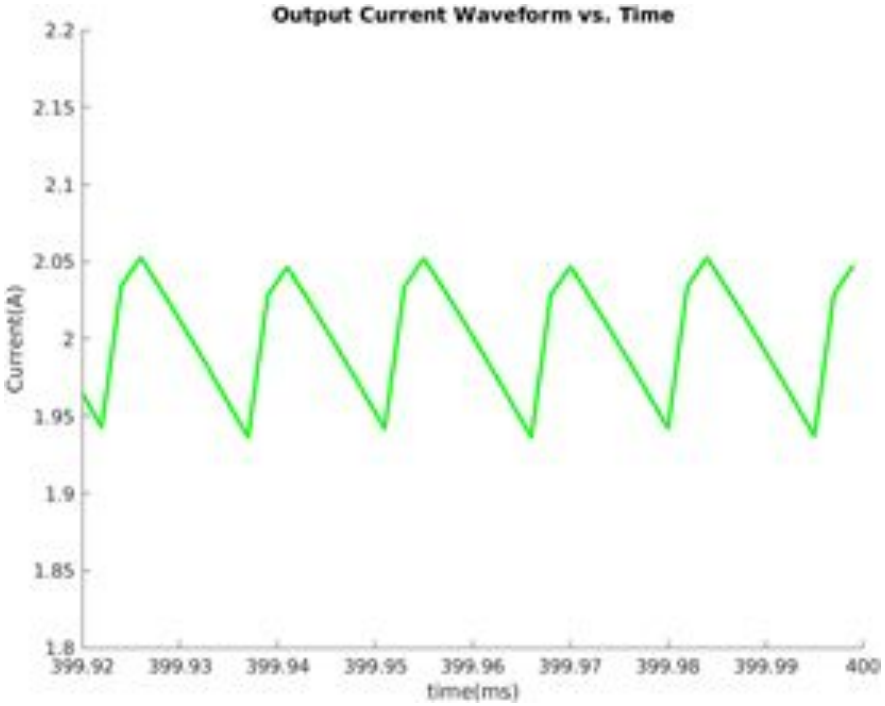


5.5. Simulation Results - **Buck Converter Voltage Waveform**

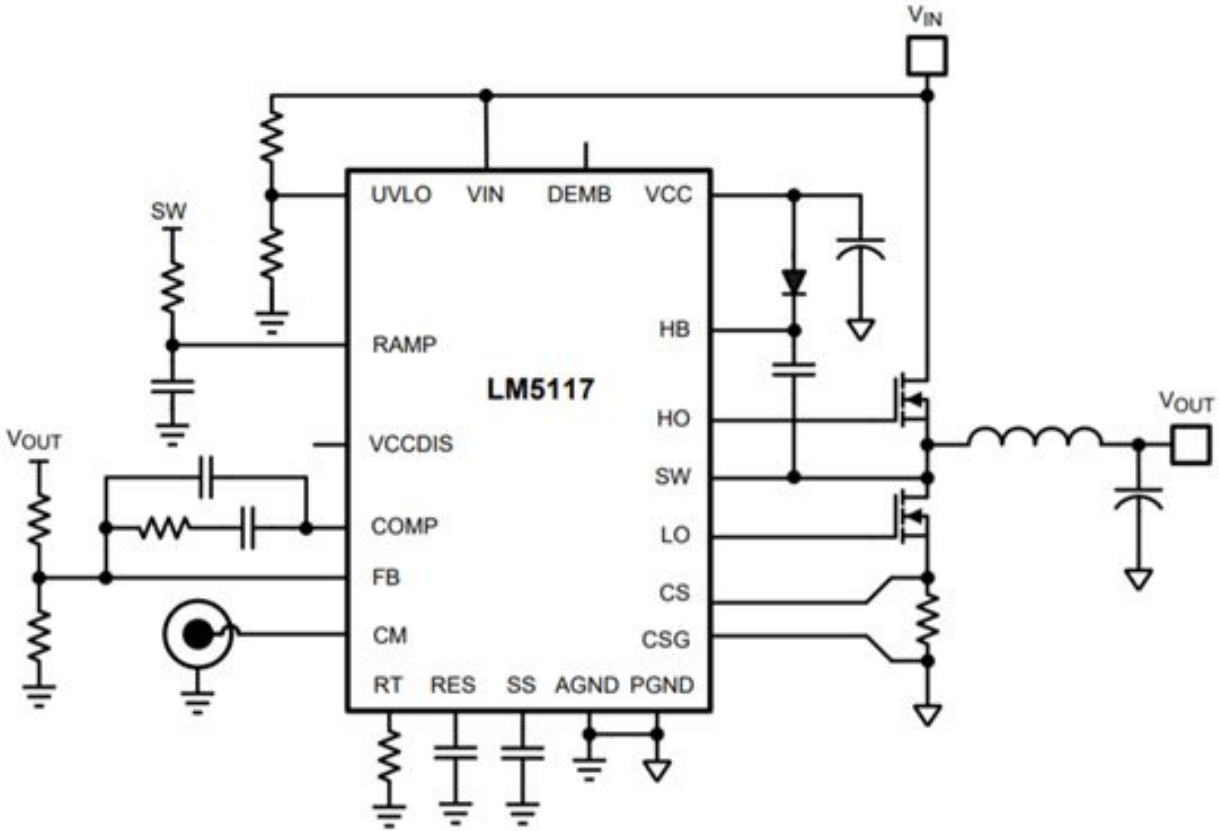


5.5. Simulation Results - **Buck Converter Current Waveform**

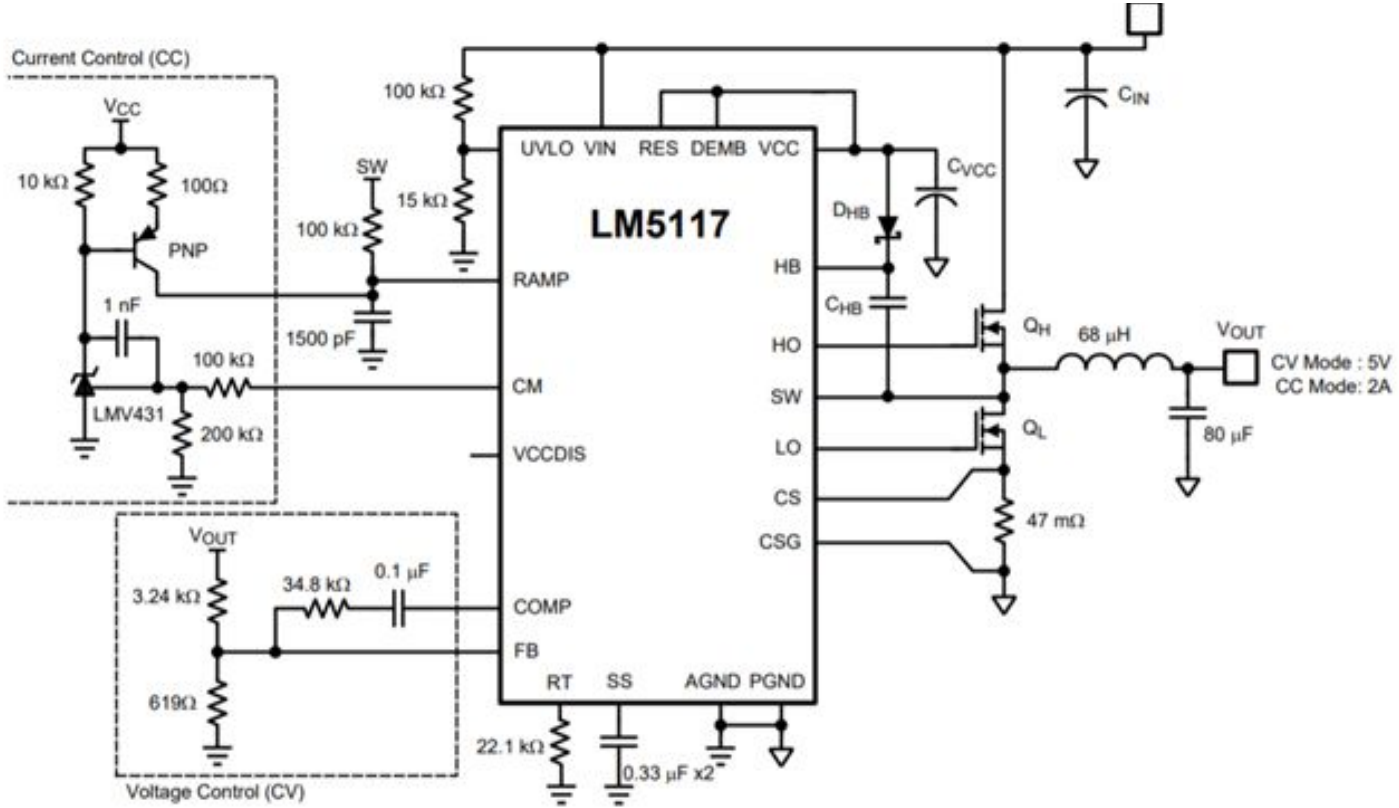




6. Controller Discussion - Typical Application of LM5117



6. Controller Disc. - Constant Voltage Regulator with Accurate Current Limit



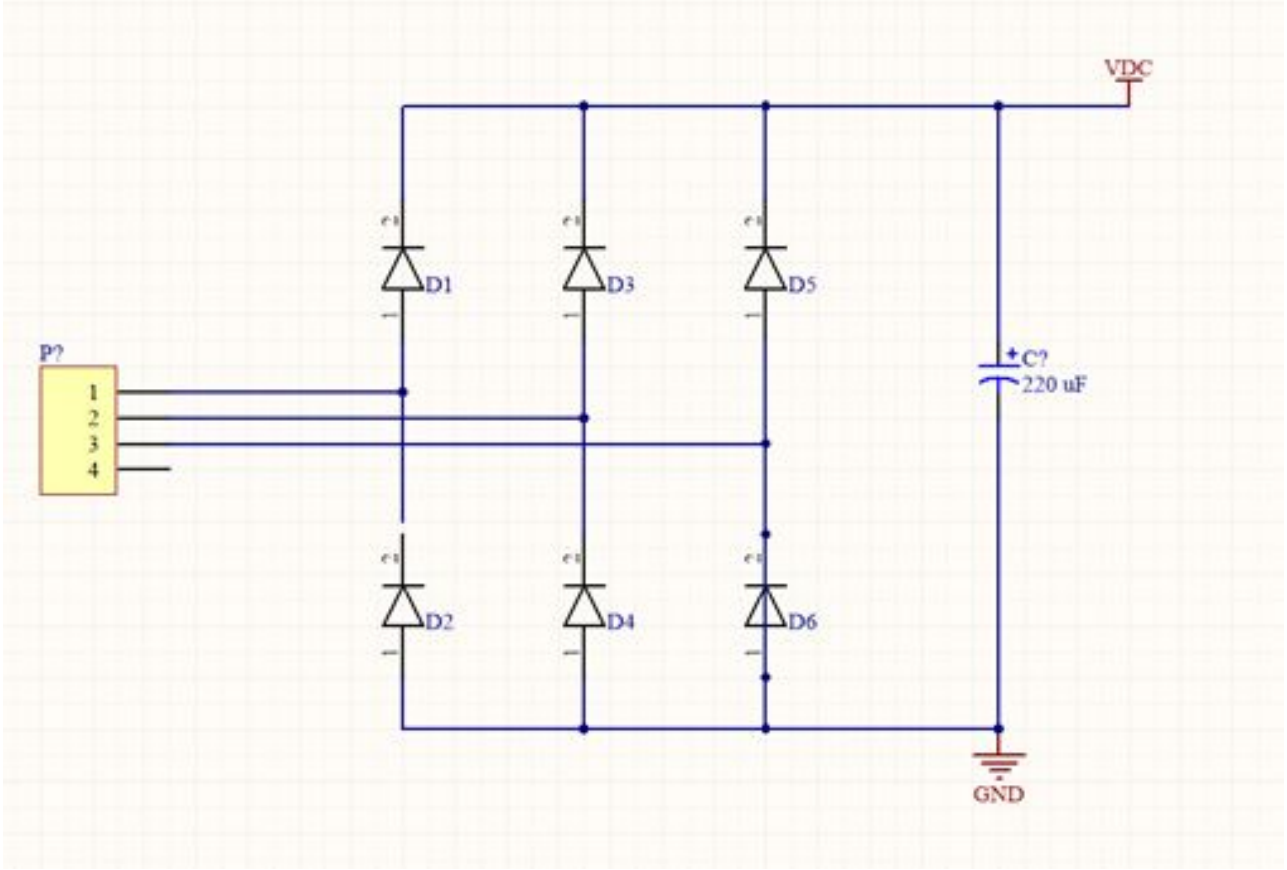
6. Controller Discussion
- Pin functions of LM5117

Design Parameter	Example Value
Output Voltage	24V
Full load current, Iout	2A
Minumum input voltage, Vin(min)	12V considered / not sure
Maximum input voltage, Vin(max)	24V considered / not sure
Switching frequency, fsw	100kHz
Diode emulation	yes
External VCC Supply	yes / 12V considered

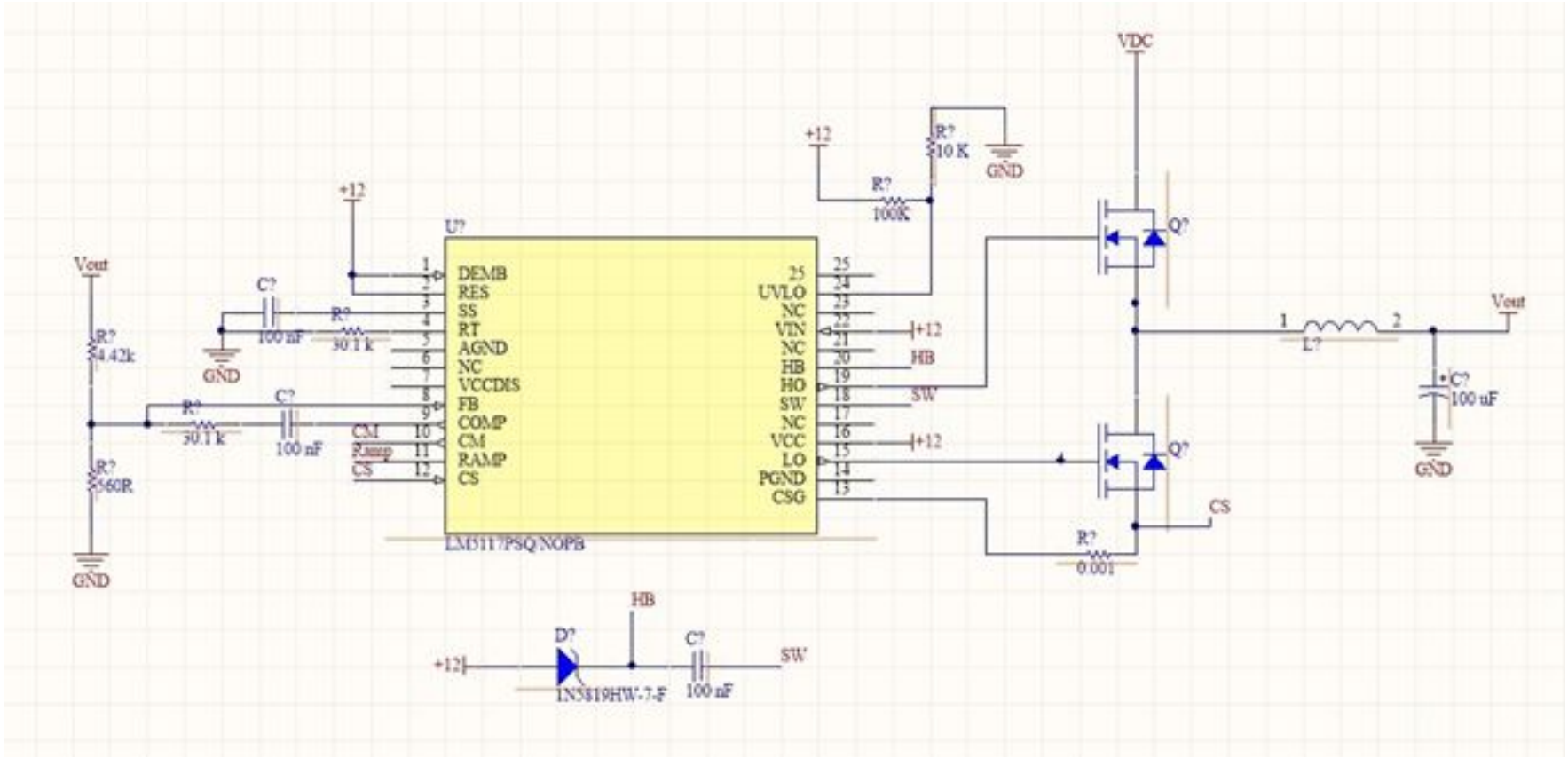
-Detailed Design Procedure for LM5117

PIN			TYPE (1)	DESCRIPTION
HTSSOP	WQFN	NAME		
1	24	UVLO	I	Undervoltage lockout programming pin. If the UVLO pin voltage is below 0.4 V, the regulator is in the shutdown mode with all functions disabled. If the UVLO pin voltage is greater than 0.4 V and less than 1.25 V, the regulator is in standby mode with the VCC regulator operational, the SS pin grounded, and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.25 V, the SS pin is allowed to ramp and pulse width modulated gate drive signals are delivered to the HO and LO pins. A 20µA current source is enabled when UVLO exceeds 1.25 V and flows through the external UVLO resistors to provide hysteresis.
2	1	DEMB	I	Optional logic input that enables diode emulation when in the low state. In diode emulation mode, the low-side NMOS is latched off for the remainder of the PWM cycle after detecting reverse current flow (current flow from output to ground through the low-side NMOS). When DEMB is high, diode emulation is disabled allowing current to flow in either direction through the low-side NMOS. A 50-kΩ pull-down resistor internal to the LM5117 holds DEMB pin low and enables diode emulation if the pin is left floating.
3	2	RES	O	The restart timer pin that configures the hiccup mode current limiting. A capacitor on the RES pin determines the time the controller remains off before automatically restarting. The hiccup mode commences when the controller experiences 256 consecutive PWM cycles of cycle-by-cycle current limiting. After this occurs, a 10-µA current source charges the RES pin capacitor to the 1.25 V threshold and restarts LM5117.
4	3	SS	I	An external capacitor and an internal 10-µA current source set the ramp rate of the error amplifier reference during soft-start. The SS pin is held low when VCC< 5 V, UVLO < 1.25 V or during thermal shutdown.
5	4	RT	I	The internal oscillator is programmed with a single resistor between RT and the AGND. The recommended maximum oscillator frequency is 750kHz. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into the RT pin through a small coupling capacitor.
6	5	AGND	G	Analog ground. Return for the internal 0.8 V voltage reference and analog circuits.
7	7	VCCDIS	I	Optional input that disables the internal VCC regulator. If VCCDIS>1.25 V, the internal VCC regulator is disabled. VCCDIS has an internal 500-kΩ pulldown resistor to enable the VCC regulator when the pin is left floating. The internal 500-kΩ pull-down resistor can be overridden by pulling VCCDIS above 1.25 V with a resistor divider connected to an external bias supply.
8	8	FB	I	Feedback. Inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is 0.8 V.
9	9	COMP	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and the FB pin.
10	10	CM	O	Current monitor output. Average of the sensed inductor current is provided. Monitor directly between CM and AGND. CM should be left floating when the pin is not used.
11	11	RAMP	I	PWM ramp signal. An external resistor and capacitor connected between the SW pin, the RAMP pin and the AGND pin sets the PWM ramp slope. Proper selection of component values produces a RAMP signal that emulates the AC component of the inductor with a slope proportional to input supply voltage.
12	12	CS	I	Current sense amplifier input. Connect to the high-side of the current sense resistor.
13	13	CSG	G	Kelvin ground connection to the current sense resistor. Connect directly to the low-side of the current sense resistor.
14	14	PGND	O	Power ground return pin for low-side NMOS gate driver. Connect directly to the low-side of the current sense resistor.
15	15	LO	P/O/I	Low-side NMOS gate drive output. Connect to the gate of the low-side synchronous NMOS transistor through a short, low inductance path.
16	16	VCC	I/O	Bias supply pin. Locally decouple to PGND using a low ESR/ESL capacitor located as close to controller as possible.
17	18	SW	O	Switching node of the buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side NMOS transistor and the drain terminal of the low-side NMOS through a short, low inductance path.

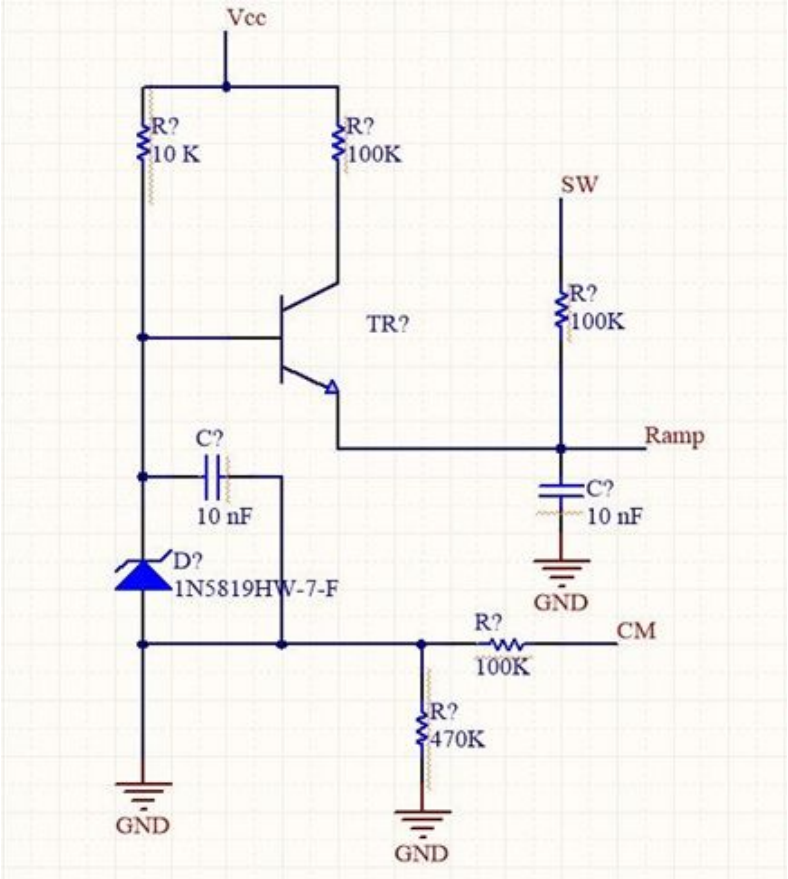
7. PCB Design - Rectifier Circuit Schematic



7. PCB Design - Buck Converter Schematic



7. PCB Design - Current Control Schematic



7. PCB Design - To be Handled

- Selection of the proper controller should be done.
- Power ports should communicate between sheets.
- Compile problems should be understood.
- Missing footprint of 400V rectifier diodes should be added.

8. References

[1]Z4DGP406L-HF Comchip Technology | Discrete Semiconductor Products

[2]EEE-FP1V220AR Panasonic Electronic Components | Capacitors

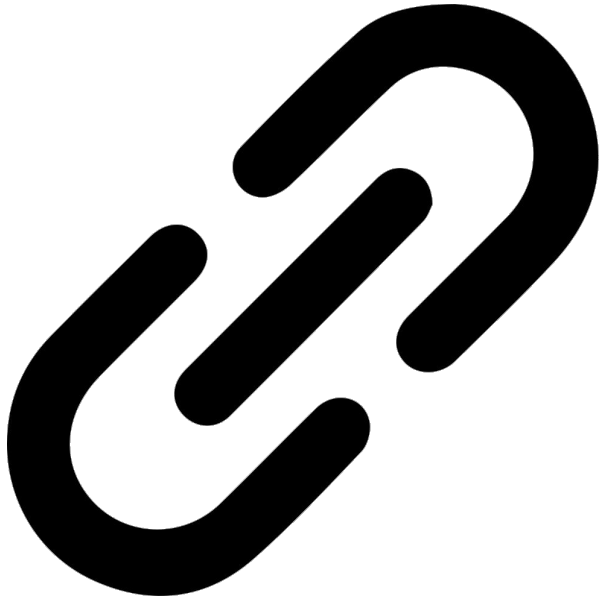
[3]UVZ2G221MRD Nichicon | Capacitors | DigiKey

[4]PE0603DRF570R01L Yageo | Resistors | DigiKey

[5]FDT3N40TF / ON-Semiconductor-Fairchild / Mouser

[6]744822222 / Wurth-Elektronik / Mouser

[7]https://www.ti.com/lit/ds/symlink/lm5117.pdf?ts=1608837436095



Thank You.