Modified grid forming converter controller with fault ride through capability without PLL or current loop

Ahmed Abdelrahim
Electronic and Electrical Engineering Department
University of Strathclyde
Glasgow, United Kingdom
ahmed.abdelrahim@strath.ac.uk

Michael Smailes
ORE Catapult
National Renewable Energy Centre
Blyth, United Kingdom
Michael.smailes@ore.catapult.org.uk

Khaled Ahmed
Electronic and Electrical Engineering Department
University of Strathclyde
Glasgow, United Kingdom
khaled.ahmed@strath.ac.uk

Paul McKeever
ORE Catapult
National Renewable Energy Centre
Blyth, United Kingdom
paul.mckeever@ore.catapult.org.uk

Agusti Egea-Àlvarez
Electronic and Electrical Engineering Department
University of Strathclyde
Glasgow, United Kingdom
agusti.egea@strath.ac.uk

***Abstract*— The electrical power system is facing several challenges as the penetration of converter based renewable power increases, including a reduction of the synchronous based inertia, loss of converter synchronism and weakened grids. Grid forming converter controllers, especially the so-called Virtual Synchronous Machines (VSMs), are seen as a potential solution for some of these issues. VSM controllers mimic the behaviour of a synchronous machine to different degrees of detail. Of these implementations, those that do not use Phase Locked Loops (PLLs) or current loops have been shown to be advantageous. This paper presents several proposals for a Fault Ride Through controller for a VSM controlled converter without a PLL or vector current control loop, which are imposing limitations on the stability of the inverter in low Short Circuit Ratio grids. Also, a method to limit the power and voltage/reactive power references, considering the converter maximum current, is presented. This paper validates and shows the advantages and limitations for the proposed control structures through extensive simulations using MATLAB Simulink for different grid conditions applied to a wind turbine.**

Keywords—Virtual Synchronous Machine, Fault Ride Through, Current Limitation, Fault detection, Voltage Sags, Symmetrical Faults, MATLAB/Simulink.

I. INTRODUCTION

Renewable electrical generation methods are a priority to reduce the effects of climate change [1]. The UK grid operator has set the target to operate the power system with zero carbon operation by 2025 [2]. Renewable energy generation is set to increase significantly in the UK already reaching 35.8% of the total electricity generation in Quarter 1 of 2019 [3]. Wind generation represented 51.8% of the total renewable electricity generation in The U.K. in 2018 [4]. A key component to allow an increase renewable power generation, is the power converter's control. Several studies have showed that the existing converter control techniques might have a negative impact on the stability of the grid [5,6] with high penetrations of renewable energies.

Standard electrical generation units are based on synchronous generators. In case of a frequency event, synchronous machines damp any frequency variation due to the large rotational inertia of the generator's rotor. The decreasing number of synchronous machine-based generation has made the grid more vulnerable grid to frequency disturbances. Limiting the Rate of change of frequency (RoCoF) in grids with high penetration of converters has become a priority. Standard converter controllers are not sensitive to frequency variations therefore new control structures should be studied [7]. At the same time, grids with a high penetration of converters might face other issues like weak grids [8].

A promising solution for the previously mentioned issues is the Grid Forming Converters (GFC), in particular the Virtual Synchronous Machine (VSM) is getting the attention of manufacturers [9] and grid operators [10]. The VSM concept is the emulation of the synchronous machine behaviour by a power converter. As a result, the power converter can provide some inertia in case of frequency disturbances [11-13]. As power converters have no mechanical parts, which could be the source of inertia, the energy should be provided externally. Researchers discuss several potentials such as: Batteries in PV systems [16], Batteries in electric vehicles [24], and the wind turbine's rotating mass [17]. In addition, VSM is a grid forming control type, which can still have stable operation in weak grids [14,15].

There are different proposed architectures for the VSM, each type depends on the degree of emulation of the synchronous machine behaviour [18]. Some implementations emulate the full set of synchronous machines dynamic equations [18,19] and some others are based on simplifications [20-22]. All of the mentioned VSM implementations emulate the swing equation of the synchronous machine on the converter control, which provides inertia during the frequency disturbance.

One of the challenges of the VSM not using an internal current loop is its Fault Ride Through (FRT) capability. Several solutions can be found in the literature but most of them are dependent on the Phase Lock Loop (PLL) or the vector current control approach [21,23].

This paper introduces a number of FRT implementations for the three phase to ground fault without PLL or vector current controller keeping the converter currents and voltages under the nominal value. These suggested implementations are:

- Modifying the VSM structure to limit the current to almost zero.
- Further modification to the VSM structure to inject reactive power during the fault.

Also, a reference current limitation in steady state is presented. The paper is divided into the following sections: Section II discusses the controller architecture; Section III discusses the normal operation current limiting technique; Section IV presents the FRT technique; Section V validates the proposed techniques through several simulations under different conditions; Section VI concludes the paper.

II. Proposed Controller Description

The controller used in this paper, emulates the synchronous machine using a variation of the swing equation to create the active power loop, and the Automatic Voltage Regulator (AVR) for the voltage controller. The full VSM model is shown in Fig. 1. The proposed controller has two different loops, one loop controls the voltage magnitude at the Point of Common Coupling (PCC), while the other loop controls the power acting on the converter voltage angle. The control structure doesn't use a PLL to obtain the angle, so the problems regarding the PLL (i.e. PLL instability in weak grids) are avoided [26,27]. The controller description is discussed in the following sub-sections.

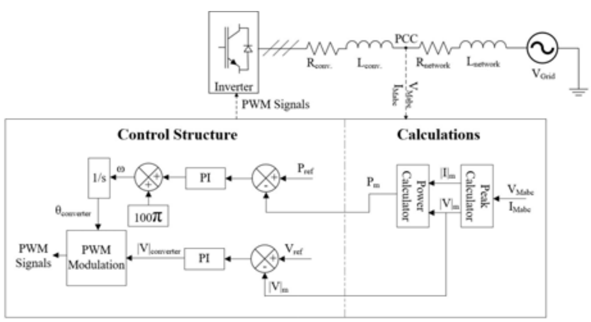

Fig. 1: Simple VSM control structure

A. Active Power Loop Control

The active power loop controls the angle of the voltage output based on the swing equation [21]:

$$P_{mec} - P_{ele} = J\frac{d\Delta\theta}{dt}\frac{d^2\Delta\theta}{dt^2} + D\frac{d\Delta\theta}{dt} \qquad (1)$$

Where P_{mec} is the synchronous mechanical power, P_{ele} is the synchronous machine electrical power, J is the moment of inertia, D is the damping factor and ω is the output frequency.

The power loop Proportional Integral (PI) controller was inspired by the swing equation, emulating the relationship between the active power and the synchronous machine speed. An integrator is added to drive the angle from the speed. This angle can then control active power flow through the converter.

This equation can be implemented as shown in Fig. 2.

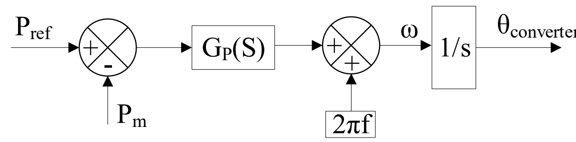

Fig. 2: Active power loop controller emulating the swing equation

The block $G_P(S)$ can be expressed by:

$$G_P = \frac{k_pS + k_i}{S} \qquad (2)$$

Where $G_P(S)$ is a PI controller, where k_p and k_i are the proportional and integral gains of the PI controller. The effect of changing the PI parameters of the active power loop is shown in the waveforms of Fig. 5 and Fig. 6. The active power reference is changed from 3 MW to 5 MW at t=10 sec. In Fig. 3, the response to three different k_p values are shown. It can be seen that by decreasing the proportional gain, the oscillations in the active power response increases as there is less damping. Moreover, the waveforms shown in Fig. 4 show that the settling time in the active power response decreases by decreasing k_i i.e. the inertia.

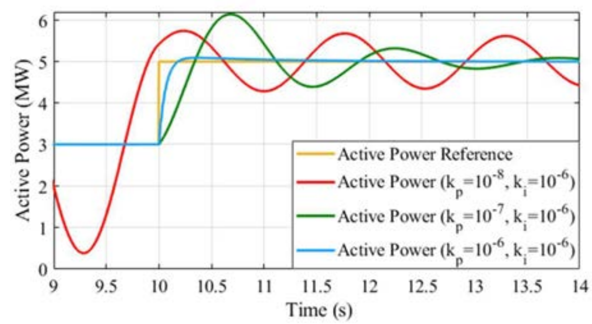

Fig. 3: Active power response to changing the proportional gain of the active power loop PI controller

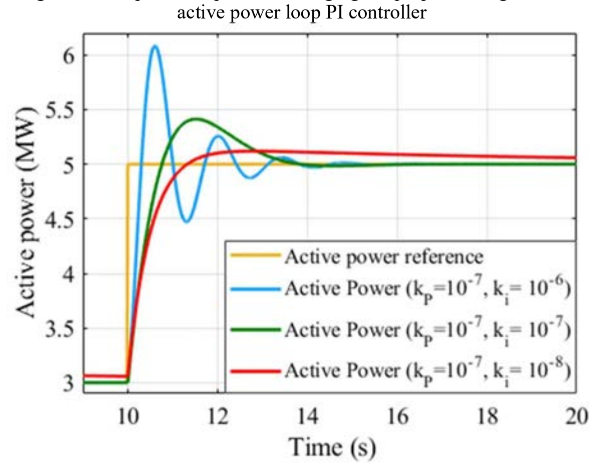

Fig. 4: Active power response to changing the integral gain of the active power loop PI controller

B. Voltage Loop and Reactive Power Control

The voltage controller is inspired by the automatic voltage regulator of the synchronous generator. A simple demonstration for the controller is:

$$G_V(S)(|V|_{ref} - |V|_m) = |V|_{converter} \qquad (3)$$

Where $|V|_{ref}$ is the voltage reference, $|V|_{meas}$ is the measured voltage at the PCC, $|V|_{convereter}$ is the converter voltage magnitude.

$G_V(S)$ is a PI controller, which could be:

$$G_V = \frac{k_{pV}S + k_{iV}}{S} \tag{4}$$

where k_{pv} and k_{iv} are the proportional and integral gains of the voltage loop PI controller respectively. The block diagram for the voltage controller is shown in Fig 5. The PI controller is used to control the voltage, as well as keeping the error to a minimum. The output of the PI controller must be saturated to keep the voltage within the standard voltage limits.

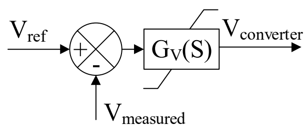

Fig. 5: Voltage loop controller emulating the automatic voltage regulator

An outer reactive power controller could be added to the voltage loop. The block diagram for the reactive power with the voltage loop is shown in Fig. 6.

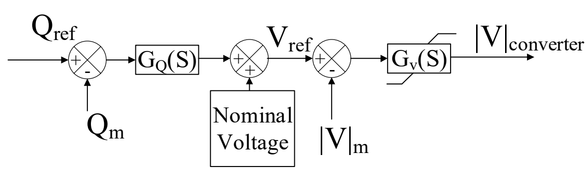

Fig. 6: Reactive power controller and voltage loop controller

The reactive power controller $G_Q(S)$ is a PI controller:

$$G_Q = \frac{k_{pQ}S + k_{iQ}}{S} \tag{5}$$

where k_{pQ} and k_{iQ} are the proportional and integral gains respectively. This controller is used to control the reactive power signal, then the output is added to the nominal voltage. The output is a voltage signal which could be controlled using the voltage controller discussed before.

C. Measurements and Controller Parameters

The voltage and current in *abc* frame are transferred to the $\alpha\beta$ frame using the Clarke transformation:

$$X_\alpha = \frac{2X_{Ma}}{3} - \frac{X_{Mb}}{3} - \frac{X_{Mc}}{3} \tag{6}$$

$$X_\beta = -\frac{X_{Mb}}{\sqrt{3}} - \frac{X_{Mc}}{\sqrt{3}} \tag{7}$$

Where X denotes to the voltage/current, and the subscripts Ma, Mb and Mc are the sinusoidal values for the voltages/currents. The voltage magnitude $|V|_m$ is calculated as:

$$|V|_m = \sqrt{(V_\alpha)^2 + (V_\beta)^2} \tag{8}$$

The active and reactive power can be calculated using equations:

$$P = \frac{3}{2}\,(V_\alpha I_\alpha + V_\beta I_\beta) \tag{9}$$

$$Q = \frac{3}{2}\,(V_\alpha I_\beta - V_\beta I_\alpha) \tag{10}$$

The parameters of the controller should be chosen according to the converter capability and the system limitations. The voltage loop PI parameters are limited by the converter voltage limit for maximum values, as well as the grid voltage recommendations and standards for the minimum values. The active power loop PI parameters must be tuned with a low bandwidth, similar to a synchronous machine. Moreover, the energy storage for inertia emulation should be considered when choosing the power controller gains.

III. Steady State Current Limitation Technique

The current through the converter should be limited to the converter capability. The proposed control architecture doesn't include a current controller, which could lead to converter deterioration. A current limitation strategy is required to avoid such issues with the controller references.

A current limiting strategy is proposed to limit the controller references, providing active or reactive current prioritisation, depending on the selected grid code. The references for the converter controller are active and reactive power, where the apparent power can be defined as:

$$|S| = \sqrt{P^2 + Q^2} \tag{11}$$

Where $|S|$ is the magnitude of the complex power, P is the active power reference and Q is the reactive power reference. The references P and Q are the input of the algorithm. Then, the current magnitude is calculated according:

$$|S| = 3|V||I| \tag{12}$$

Where $|V|$ is the magnitude of the phase voltage measured at the PCC, and $|I|$ is the phase current needed for the limitation process.

The current is compared to a maximum value, to satisfy the condition:

$$|I| > |I|_{max} \tag{13}$$

Then, according to the prioritising sequence, the power references are recalculated using $|I|_{max}$ in (12) and (13) as shown in:

$$|S|_{new} = |V||I|_{max} \tag{14}$$

Where, if the reactive priority is activated, the new active power is recalculated using:

$$P_{new} = \sqrt{|S|_{new}^2 - Q^2} \tag{15}$$

while keeping the reactive reference the same, on the other hand, if the active power priority is activated the reactive power is calculated using:

$$Q_{new} = \sqrt{|S|_{new}^2 - P^2} \tag{16}$$

while keeping the active power with the same value.

However, if the reference is set to zero and the current value still can't satisfy the condition in (13), then the other power reference is decreased while maintaining the initially controlled power set to zero.

The full controller architecture is shown in Fig. 7. The controller uses the measured voltage, the active power and the reactive power to estimate the current as previously discussed.

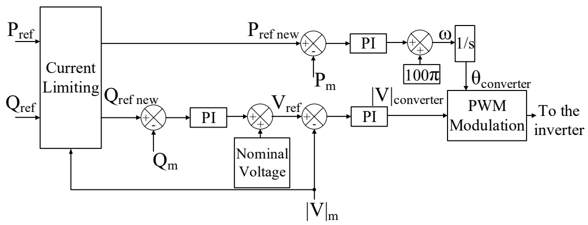

Fig. 7: The first proposed current limiting controller

IV. FAULT RIDE THROUGH STRATEGY

One of the main challenges of VSM is to limit the current during faults. During a fault, the VSM cannot limit the converter current. This is due to the lack of current controller within the VSM controller.

The VSM structure should therefore incorporate a current limiting strategy as an alternative to the current controller. As VSM doesn't limit the current automatically, as in the case of current vector control, the fault must be detected and a FRT strategy activated. The proposed fault detection algorithm uses the voltage and current magnitudes to detect faults or voltage sags. The tripping signal algorithm is shown in Fig. 8.

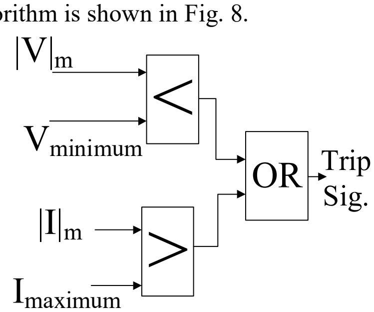

Fig. 8: Fault detection algorithm

The voltage magnitude is compared to the minimum voltage of the voltage maximum magnitude (nominal voltage level), and the current is compared to the current magnitude maximum. Then, if either condition is satisfied, a tripping signal is generated.

A. First FRT Strategy

This strategy is based on applying the same voltage that appears at the converter PCC. In this way the current flow in the coupling reactor is close to zero.

This is done by changing the voltage loop to feedforward the voltage measured during the fault. The references of both control loops are changed. The power controller reference is set to zero to limit the active power. The voltage loop reference is changed to the voltage feedback signal, preventing the voltage controller integrator from increasing during the fault. The control structure is shown in Fig. 9.

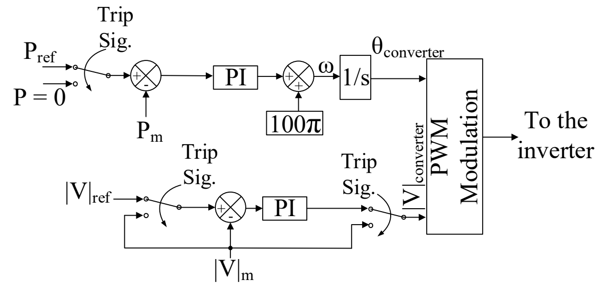

Fig. 9: First switching action controller

B. Second FRT Strategy

An improved architecture is shown in Fig. 10, which allows the converter to provide reactive power during the fault. This is done by adding a voltage component, V_{FRT} to the voltage feedback. V_{FRT} can be calculated a:

$$V_{FRT} = I_{inj} \times Z \tag{17}$$

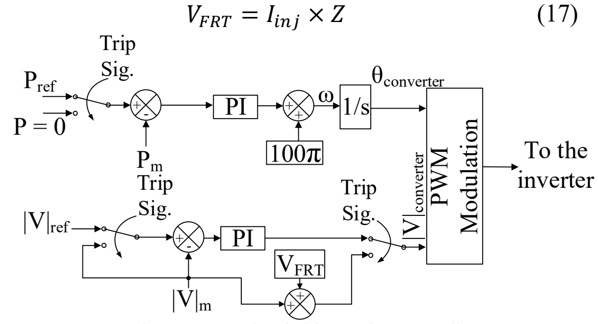

Fig. 10: Second switching action controller

Where I_{inj} is the value of the desired current magnitude needed to be injected during the fault, and Z is the impedance between the converter and the PCC.

V. SIMULATION RESULTS

The simulation was performed using MATLAB/Simulink. The converter ratings is 6MVA and is connected to a 25 kV MV network. The power system architecture is the same as shown in Fig. 1, except for the control structure, which is specified by each simulation case. The magnitude of the grid voltage changes to emulate the voltage sags, and the three phase to ground fault. The simulation parameters are shown in TABLE I.

TABLE I. Simulation Parameters

Parameter	Value
Lconv	0.033157 H
Rconv	1.041667 Ω
Kp	10^{-6}
Ki	10^{-6}
Kiv	0.6
Kpv	8
$V_{minimum}$	18371.173 V
$I_{nominal}$	138.564 A

A. Normal Operation Reference Limitation

Voltage variations or undesired reference changes in the system could raise the current magnitude, above the converter limit. Therefore, a test case was made to ensure that the current is controlled during normal operation through the power references. The controller shown in Fig. 7 is applied to the wind turbine converter shown in Fig. 1. The active power reference is set to 5 MW, and it is kept constant during the simulation. The reactive power reference is changed from 1 Mvar to 2 Mvar to represent voltage variations in the power system. The active power, reactive power and current magnitude are measured at the PCC and are shown in Fig. 11 and Fig. 12.

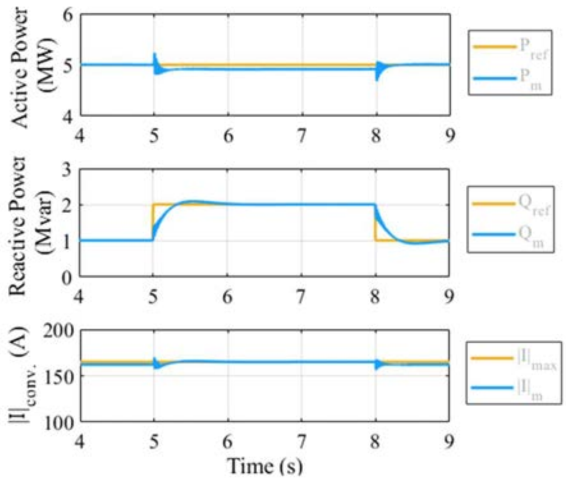

Fig. 11: Active power, reactive power and converter current magnitude (Reactive power priority)

As can be observed in Fig. 11, the algorithm reduces the active power to keep the current magnitude to the set limit (165 A_{peak}) while delivering the desired reactive power.

The active power priority is validated through a second case shown in Fig. 12. The active and reactive power waveforms here show the controller action to reduce the reactive power and hence limit the current magnitude to 165 A_{peak}.

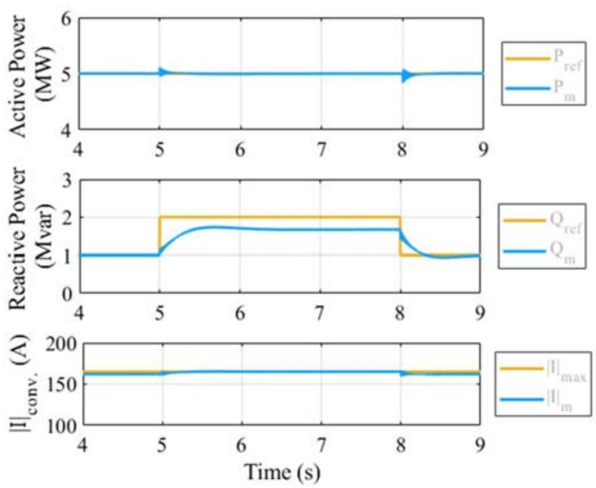

Fig. 12: Active power, reactive power and converter current magnitude (Active power priority)

B. *First FRT Strategy*

Several simulations are adopted to verify the FRT action of the proposed controller, during three-phase faults. The test case includes different voltage sags, and different short circuit ratios (SCR). The following list shows the sequence of voltage sags for each SCR:

1. 100% voltage sag (Three phase to ground fault) starting at t=5 sec. to t=10 sec.
2. 80% voltage sag starting at t=15 sec. to t=20 sec.

The voltage dips duration is not a standard grid code requirement, but it was chosen to test the control action for a couple of seconds. Each case is studied for different SCR keeping constant the control parameters. This is done to validate the control structure for several grid conditions. The cases are discussed as follows:

1) First scenario: 100% voltage sag

The purpose of the first scenario is to show the control performance in weak grids. The control structure is shown in Fig. 9 and the power system structure shown in Fig. 1. The waveforms shown in Fig. 13 are display the active and reactive powers and the current during a 100% voltage sag. Each row represents different SCRs, and the first column is for active (blue line) and reactive (orange line) power waveforms, then the second column is for the initial current transients, and the third one for the final transients of the currents. The currents for all SCRs are almost zero, but the final transients increase by increasing the SCR. The transients in the active and reactive powers are very high.

2) Second scenario: 80% voltage sag

The second scenario is to verify the previous controller on 80% voltage sag. The active, reactive powers and currents waveforms are shown in Fig. 14. The figure is divided as in the same way as the first scenario. The currents are limited to a low value, which makes the controller safe during this type of fault. However, it can be seen that by increasing the SCR, the initial current transients decrease. The active and reactive powers transients are decreased compared to the 100% voltage sag.

C. *Second switching action controller*

The scenarios are repeated to validate the modified controller.

1) First scenario: 100% Voltage Sag

The active, reactive powers and currents for 100% voltage sag are shown in Fig. 15. The controller provides a current during the fault. The final current transients are slightly increased by increasing the SCR. The transients in the active and reactive powers are much decreased compared to the first FRT strategy.

2) Second scenario: 80% voltage Sag

The second scenario is to test the same structure at 80% voltage sag. The active, reactive powers and current waveforms are shown in Fig. 16. The controller is still able to provide some current during the fault. The behaviour of the controller to both voltage sags is almost the same.

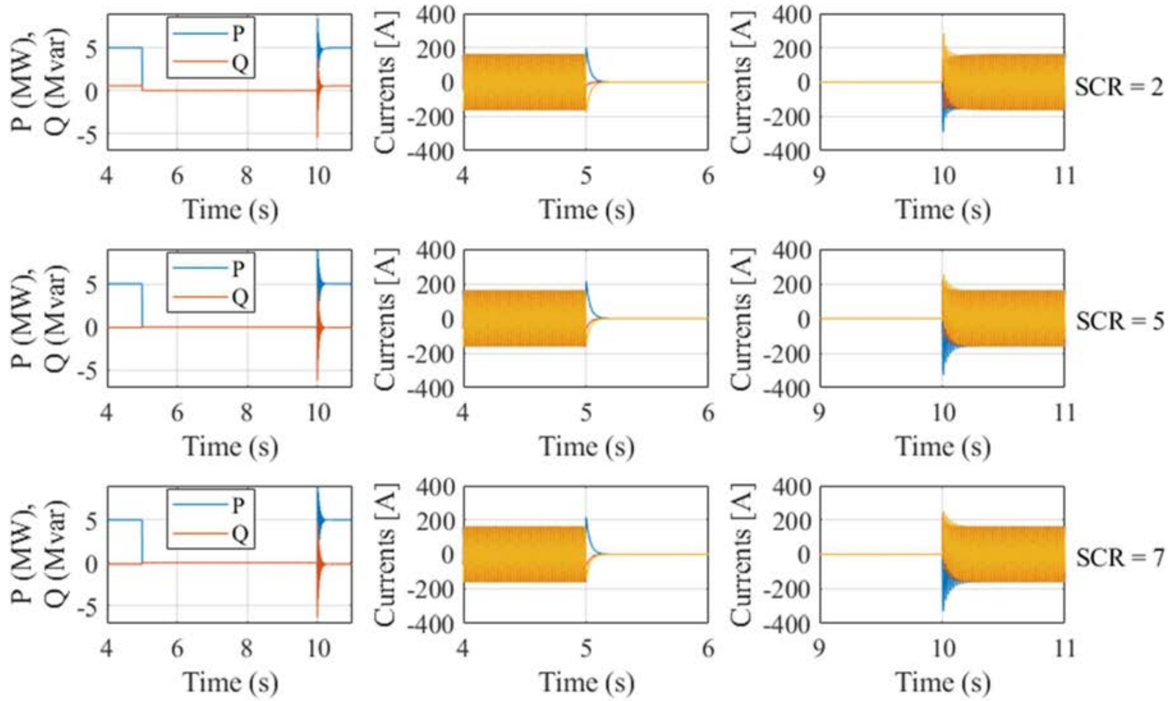

Fig. 13: The voltages and currents for 100% voltage sag for SCR = (2,5,7) for the first switching action controller

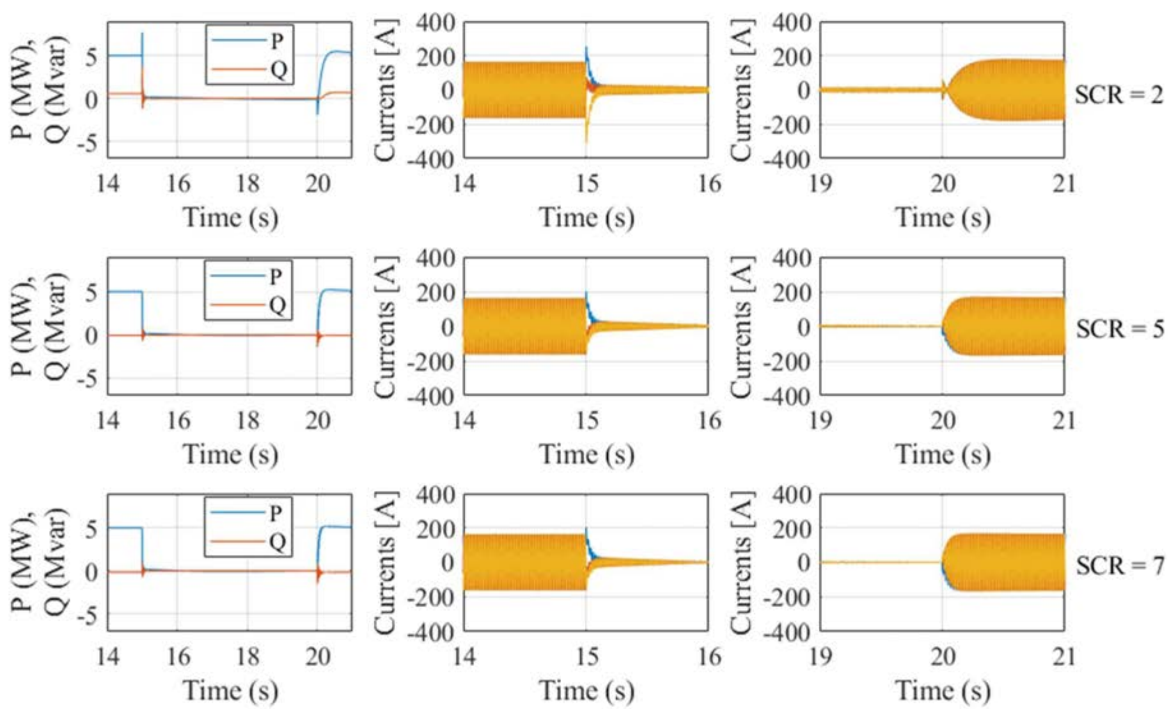

Fig. 14: The voltages and currents for 80% voltage sag for SCR = (2,5,7) for the first switching action controller

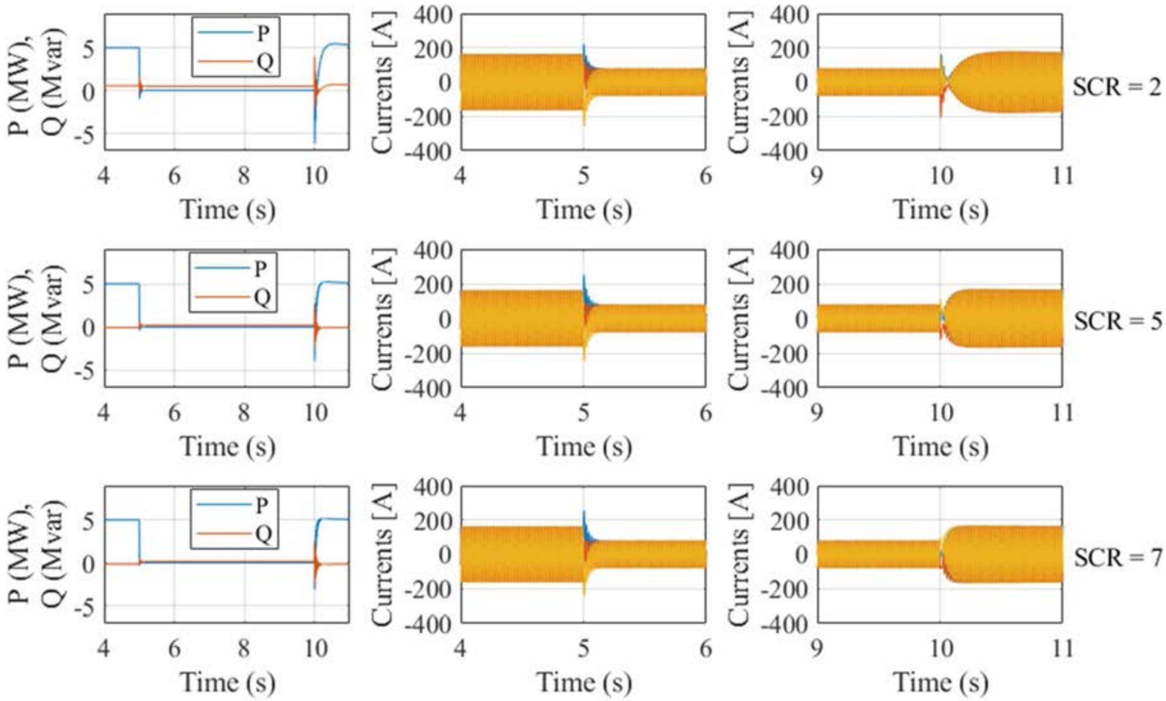

Fig. 15: The voltages and currents for 100% voltage sag for SCR = (2,5,7) for the second switching action controller

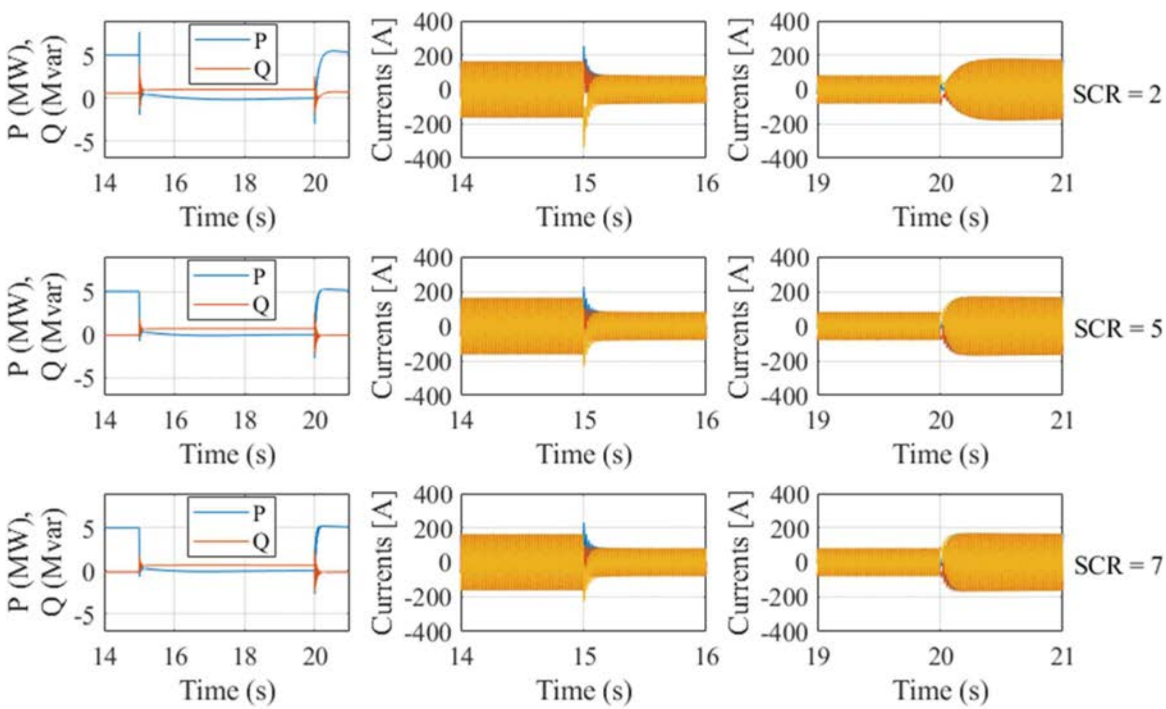

Fig. 16: The voltages and currents for 80% voltage sag for SCR = (2,5,7) for the second switching action controller

VI. Conclusion

The paper discusses the normal operation of a reference saturation algorithm. The results show that the controller can limit the steady state current by controlling the power references. In addition, the algorithm can be set based on the priority given to reactive vs. active power by the local grid code. Two FRT strategies for the converter survival during three-phase faults are suggested. The first control structure addressed the ability of the converter to limit the current to zero during the multiple voltage sags. The second architecture added a constant voltage to the voltage feedback during the fault. This resulted in an improved ability to provide current during the voltage sag. The later structure can therefore provide reactive power to help in voltage level recovery. Several simulations were executed to validate the proposed structures for different SCRs.

VII. Future Work

A new structure for unbalanced faults is currently being developed, which could be used as a generic structure for all types of faults. This structure cannot use a PLL or vector current controller.

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